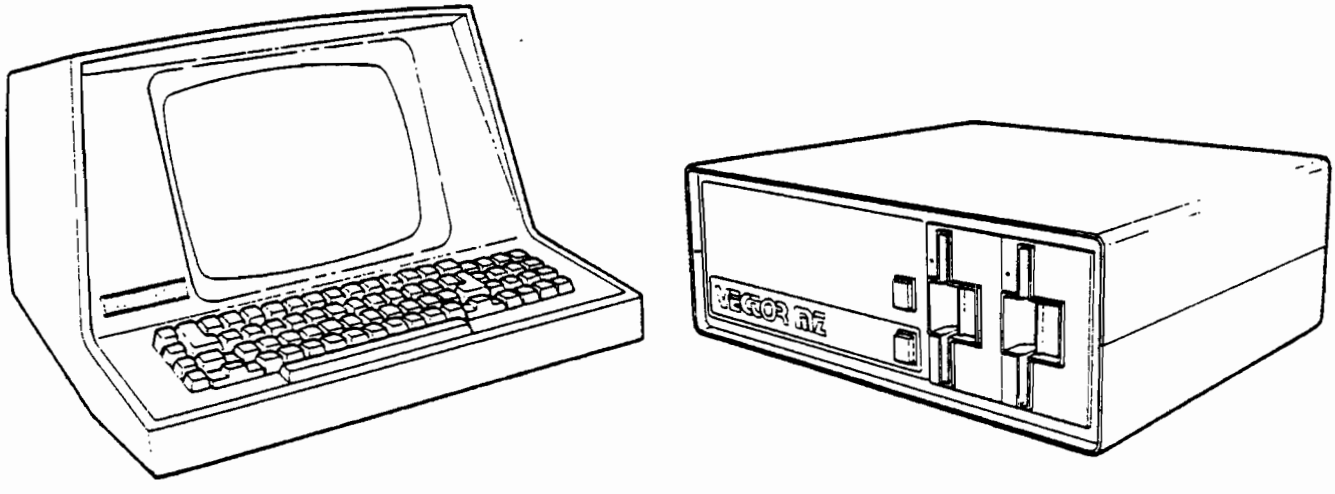
Z-80 Board
Users Manual



Z80 BOARD, REVISION 2

USER'S MANUAL

Revision A

May 17, 1979

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Rev. 2-A 5/17/79

REPAIR AGREEMENT

The Z-80 Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any Z-80 Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the Z-80 Board left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
3. The Z-80 Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the Z-80 Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any Z-80 Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

TABLE OF CONTENTS

I. INTRODUCTION

1.1 SPECIFICATIONS

Bus Compatibility	S-100
Processor	Mostek Z-80A (MK-3880N)
Number of Data Bits	8
Number of Address Bits	16
Instructions	158, including all 78 8080 instructions
Clock speed	2 or 4 MHz, jumper selectable Standard: 4 MHz
Interrupts	All three Z-80 modes S-100 vectored interrupt lines are not handled
I/O devices	256 I/O addresses
Dynamic RAM	Supports dynamic memory by sending Z-80 $\overline{\text{RFSH}}$ on bus line 66; and using fast reset received on line 55
Static RAM	Jumper option to generate reset on Z-80 board instead of fast reset on line 55
MWRITE	Jumper option to generate MWRITE on board Standard: option enabled
Wait state generation for memories slower than about 300 ns.	Jumper option to generate one wait state each time memory is addressed Standard: option not enabled
High address lines during I/O	For peripherals that need it, high address lines mirror low address lines during I/O
Bus load	1 low power TTL load on all inputs
Buffering	All outputs buffered
Card extractors	Standard
Power	+8Vdc @ 450 mA (Typ)

1.2 DESCRIPTION OF THE Z-80 REVISION 2 BOARD

The Vector Graphic Z-80 board is designed around the powerful Z-80 microprocessor chip. The board is fully S-100 bus compatible, providing interchangeability between systems. All input and output lines are fully buffered. Loading on the bus is no more than 1 TTL load.

In addition, the board has the necessary circuitry to work well with dynamic memories, such as Vector Graphic's 48K board.

Simplicity of design has been stressed to enhance reliability of operation by the use of MSI and LSI integrated circuits. This goal has been achieved while not sacrificing any performance factors.

II. USERS GUIDE

For the location of jumper areas, refer to the silk-screen diagram on page 4.1

2.1 SYSTEM COMPATIBILITY

The Z-80 Board is designed for operation in an S-100 system. It generates ALL the S-100 signals originally generated by 8080 CPU boards following the S-100 definition, and accepts as input the S-100 signals intended as input to an 8080 processor board, with two exceptions: 1) Vectored interrupt request lines (S-100 lines 4 - 11) are not received or handled in any way by the board. 2) The timing of some signals, particularly PSYNC and the status signals, is slightly different than that produced by 8080 boards, but the differences are usually inconsequential. Also, a few additional lines are used, required for dynamic memory in a Z-80 based system, and are explained below.

For power, the board only requires the +8V unregulated source on bus line 1.

2.2 USING DYNAMIC MEMORY - BUS LINES 55 AND 66

The Z-80 Board as manufactured is configured for use with dynamic memory boards. The following paragraphs will explain how.

The Z-80 chip provides a $\overline{\text{RFSH}}$ signal on pin 28 used to refresh dynamic memory, thus enabling easier use of dynamic memory in a system. This signal is buffered directly onto line 66 of the bus. Thus appropriately designed dynamic memory boards can be used in conjunction with this Z-80 board, as in the Vector Graphic MZ computer. For use of the $\overline{\text{RFSH}}$ signal in designing dynamic memory components, refer to Z-80 data books.

Dynamic memory requires that each byte be read and rewritten continuously. If the processor is halted for too long an interval, memory data can be lost. The $\overline{\text{RESET}}$ signal which is created by circuitry on the Z-80 board from an incoming $\overline{\text{PRESET}}$ signal on line 75 is too long. Hence, for use with dynamic memory, THE BOARD IS SHIPPED WITH THIS CIRCUITRY DISABLED. Instead,

the dynamic memory board is expected to create a fast reset signal on bus line 55, which is then used as input to the processor $\overline{\text{RESET}}$ pin.

If you have obtained a particular Z-80 board which has had the $\overline{\text{RESET}}$ circuit re-enabled, as described in the following section, then simply reverse the steps in the following section in order to use the board with a dynamic memory board that generates a fast reset on bus line 55.

2.3 NOT USING DYNAMIC MEMORY

If the system is not using the Vector Graphic 48K Dynamic Memory Board or other dynamic memory board which generates a fast reset signal, then you must enable the generation of $\overline{\text{RESET}}$ by the Z-80 board. Once enabled, the board will generate $\overline{\text{RESET}}$ using the $\overline{\text{PRESET}}$ signal on bus line 75, or, when the system is first turned on, using a resistor-capacitor circuit on the board. The necessary circuitry already exists on the board, except as follows. Take the following steps:

a. Install a 100 ohm 1/4 watt resistor in the spot marked to the left of U16.

b. Make sure there is capacitor installed in a marked location very close to the lower left hand corner of the Z-80 chip. If not, install a 22 or 25 MFD 12 to 16 V axial electrolytic capacitor at that spot, with the plus end to the LEFT.

c. Install a jumper across area D, found at the bottom of the board, just above the middle of the end connector. This jumper connects bus line 75 - $\overline{\text{PRESET}}$, to the reset circuitry.

d. Cut the jumper connecting pad E and pad F. It is usually installed on the back of the board. Pad E is at the bottom of the board, on the left side, and F is between U6 and U7. This jumper connects bus line 55 to the Z-80 $\overline{\text{RESET}}$ pin.

2.4 HIGH ORDER ADDRESS LINES DURING I/O

The Z-80 microprocessor presents the peripheral address byte on the low order byte of address (bits 0-7) during an I/O operation. However, some peripheral boards require the address byte to be present on the high order

byte. In order to maintain compatibility in all cases, logic has been included to "mirror" the peripheral address on the low order byte also onto the high order byte during an I/O operation.

2.5 RUNNING THE SYSTEM AT 2 OR 4 MHz

Jumper area: A

Connections as manufactured: none

Function: selects 2 or 4 MHz CPU operation. The Z-80 chip is capable of 4 MHz operation, but some peripheral boards are not. The board is shipped for operation at 4 MHz.

Options: to operate at 2 MHz, install a jumper in area A.

2.6 AUTOMATIC WAIT STATES FOR SLOW MEMORIES

Jumper area: B

Connections as manufactured: none

Function: When this jumper is connected, the Z-80 board will cause one wait state to be inserted in each memory access instruction. This is needed when using memories in the system slower than about 300 ns.

Options: to enable the automatic wait state, add a the jumper in area B.

2.7 GENERATING MWRITE

Jumper area: C

Connections as manufactured: jumper installed.

Function: when connected, the Z-80 board will generate the MWRITE signal (S-100 line 68). You will want to disconnect this jumper if there is some other source of MWRITE in the system, such as a front panel.

Options: if MWRITE generation is not wanted, remove the jumper in area C.

III. THEORY OF OPERATION

3.1 POWER

The Vector Graphic Z-80 board requires only a single 5 volt DC power source and regulates the raw +8V with a 7805 regulator. Ample bypass and filtering is provided by electrolytic and ceramic capacitors distributed on the board.

3.2 CLOCK GENERATION

See Figure 1. This board has been designed to operate at both 2 MHz and 4 MHz. Although the Z-80 requires only a single phase clock for operation, the Vector Graphic Z-80 board has circuitry to generate the 01, 02 and $\overline{CLK}$ signals required by the S-100 bus and components that interface to it.

The basic source of all the clock signals is an on-board 8 MHz crystal oscillator. The 8 MHz signal is applied to divide by 2 and divide by 4 logic formed by flip-flops U8a and U8b. The 2 MHz output at U8-8 is used for the $\overline{CLK}$ signal.

The 8 MHz clock and 4 MHz output at U8-6 are applied to gating logic to select, per jumper position, 2 or 4 MHz system operation. The subsequent output of this gating logic is applied to U7-11. By using both the Q and $\overline{Q}$ outputs of U7 the two phase clock relationship is achieved and by gating the input clock with U7-9 the required delay between clocks is achieved. $\phi 1$ and $\phi 2$ signals are applied to bus lines 24 and 25. The Z-80 is clocked by $\phi 2$.

3.3 HIGH ORDER ADDRESS LINES DURING I/O

As noted in the User's Guide, to satisfy the needs of some peripheral boards, logic has been included to "mirror" the peripheral address on the low order byte also onto the high order byte during an I/O operation. This is implemented by "wire or"ing the buffered low order address bits with the buffered high order address bits. The tri-state buffers used are enabled during an I/O operation only.

3.4 CONTROL SIGNALS

The Z-80 microprocessor has five basic control lines which are used to read or write data to and from memory or I/O devices. these signals are:

1. $\overline{\text{MREQ}}$ - output, active low. The memory request signal indicates that the address bus holds a valid address for a memory reference operation.

2. $\overline{\text{M1}}$ - output, active low. $\overline{\text{M1}}$ indicates that the current machine cycle is the op code fetch cycle of an instruction execution.

3. $\overline{\text{IORQ}}$ - output, active low. The $\overline{\text{IORQ}}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An $\overline{\text{IORQ}}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

4. $\overline{\text{RD}}$ - output, active low. $\overline{\text{RD}}$ indicates that the Z-80 wants to read data from memory or an I/O device.

5. $\overline{\text{WR}}$ - output, active low. $\overline{\text{WR}}$ indicates that the Z-80 data bus holds valid data to be stored in the addressed memory or I/O device.

By logical manipulation of the above signals the S-100 bus type signals are created. Thus, SMEMR is the logical "AND" of $\overline{\text{RD}}$ and $\overline{\text{MREQ}}$, MWRITE is $\overline{\text{WR}}$ and $\overline{\text{MREQ}}$ (produced by NORing $\overline{\text{WR}}$ and SOUT), SOUT is $\overline{\text{WR}}$ and $\overline{\text{IORQ}}$, SINP is $\overline{\text{RD}}$ and $\overline{\text{IORQ}}$, PDBIN is $\overline{\text{RD}}$, and PWR is $\overline{\text{WR}}$. All the previous listed signals are fully buffered to the bus.

The Z-80 microprocessor does not have an equivalent output to PSYNC so circuitry has been included to emulate this function. $\overline{\text{MREQ}}$ and $\overline{\text{IORQ}}$ are logically "OR"ed and applied to the D input of a flip-flop clocked by the system clock. Using the Q output, the PSYNC signal is true for 500 nsec at 2 MHz and 250 nsec at 4 MHz. Refer to figure 2.

3.5 WAIT STATES

See figure 3. The Z-80 CPU board provides for a jumper selectable automatic wait state. For many applications, it may be desirable to use slow memories. The wait logic on the board allows the Z-80 to operate with slower memory. The user may select this wait state generation if required.

The automatic wait state is created by setting U12-9 when either $\overline{\text{MREQ}}$ or $\overline{\text{IORQ}}$ are true (if the appropriate jumper is installed). The following clock time U12 is set to the Q state, thus turning off the wait signal. This circuit guarantees that wait will be true when the Z-80 looks for a wait.

As with 8080-based CPU's, external devices can cause the computer to enter a wait state by applying the appropriate signal to the PRDY bus line.

3.6 MISCELLANEOUS LOGIC

Logic is provided on the board to cause the PINTE bus line to set and reset upon the execution of EI (enable interrupt) and DI (disable interrupt) instructions, respectively.

The Z-80 board includes the capability to use a fast reset signal on bus line 55 to produce the $\overline{\text{RESET}}$ input to the Z-80. Alternately, as described in the User's Guide, existing circuitry on the board can be used to generate $\overline{\text{RESET}}$, using the $\overline{\text{PRESET}}$ input on line 75 of the bus. If this option is used, $\overline{\text{RESET}}$ is also generated on board when the system is initially turned on. (Using an RC time delay connected to VCC, the Z-80 $\overline{\text{RESET}}$ input is low for a short time when the system is first powered up.) Regardless of how it is generated, the $\overline{\text{RESET}}$ signal is used to generate the power on clear ($\overline{\text{POC}}$) output on bus line 99.

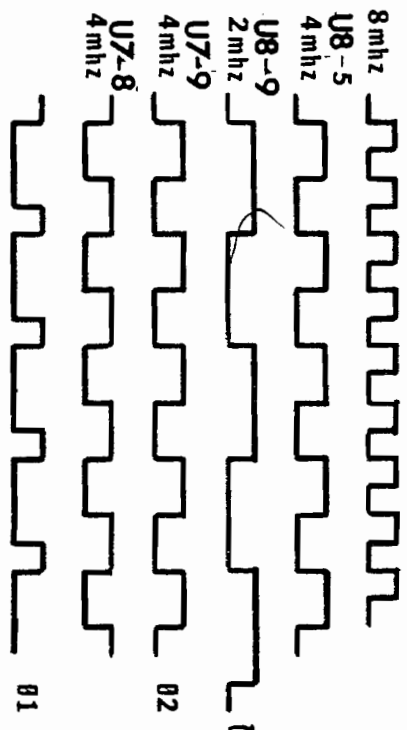

FIGURE 1

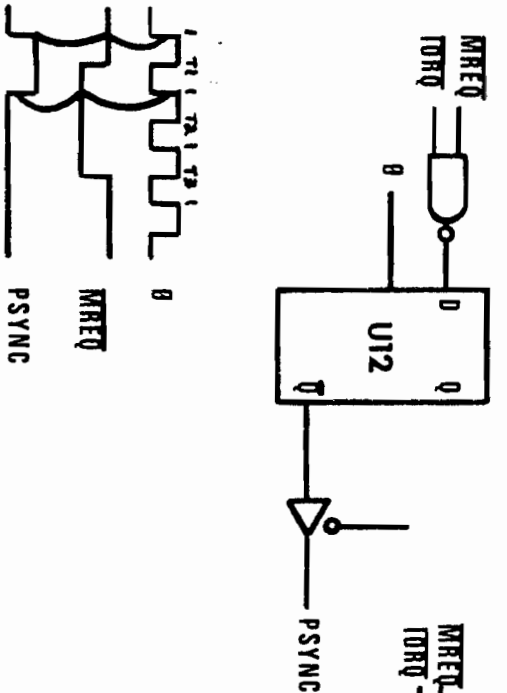

FIGURE 2

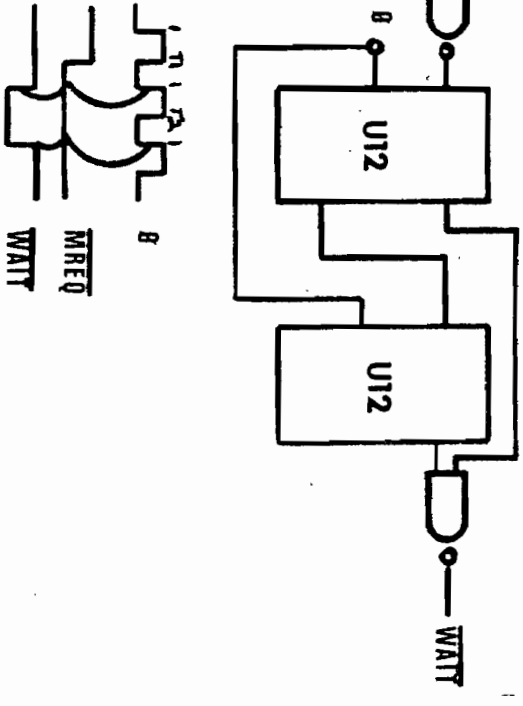

FIGURE 3

Rev. 2-A 5/17/79

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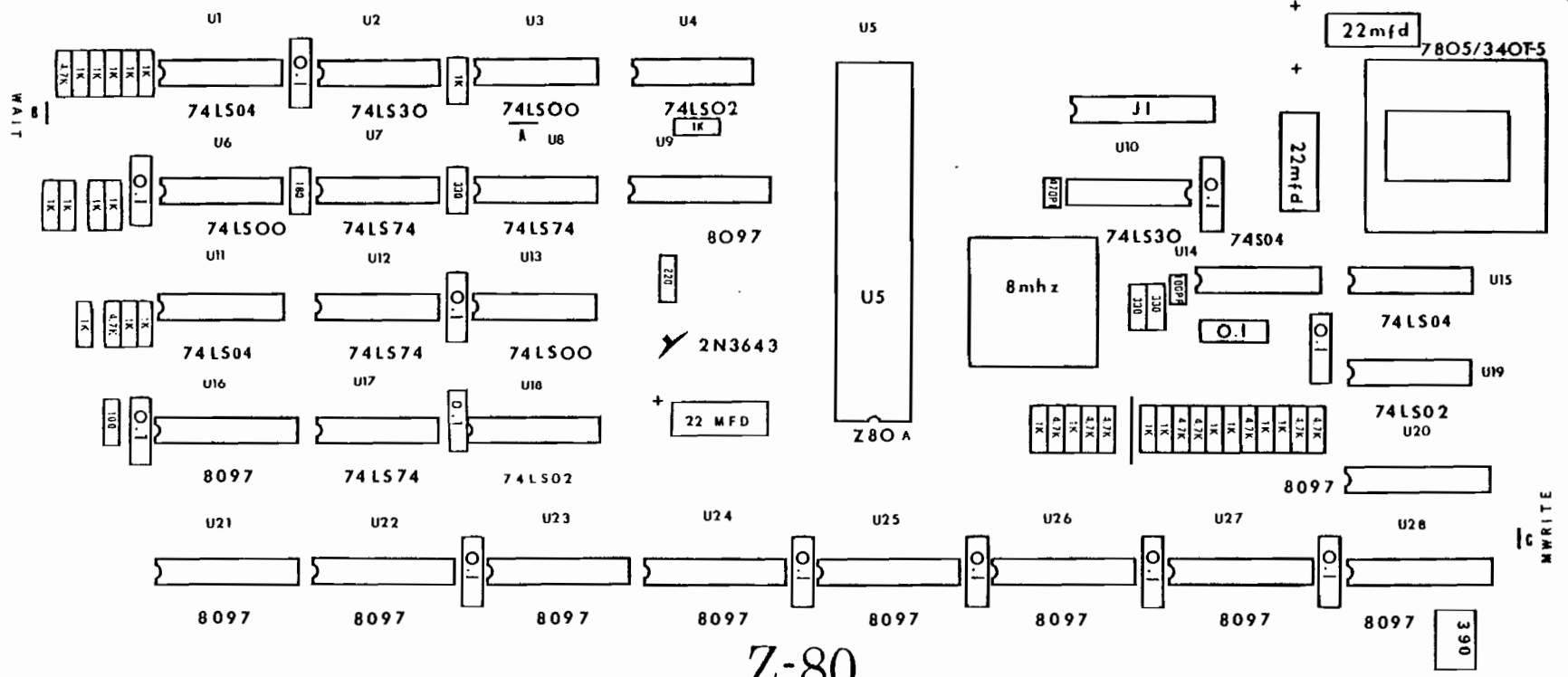

Z-80

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4-1

FE

D

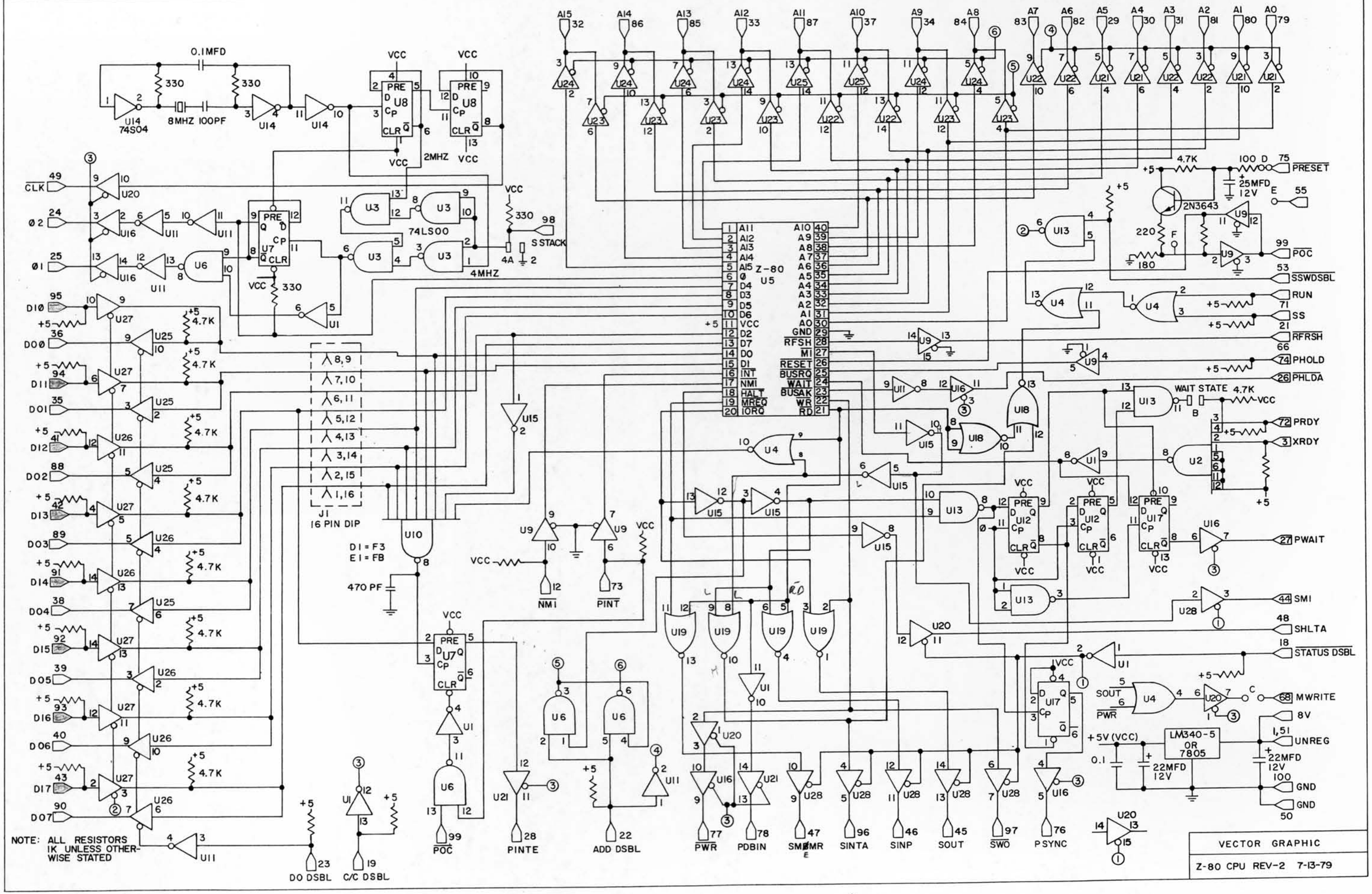
50

SCHEMATIC ERRATA

1. There should be no connection across jumper area D, in the upper right-hand corner of the schematic. The 100 ohm resistor and 25 MFD capacitor connected to it are not shipped on the board, but their places on the board has been set aside. The board is shipped with a jumper from pad E to pad F, in the upper right-hand corner of the schematic.

2. In the lower right-hand quadrant of the schematic, there is an inverter labeled U19, having pins 11 and 12. This should be labeled U20.

3. Jumper are C, near the lower right-hand corner of the schematic, should be shown connected.


0.1MFD
330
330
U14
74S04
8MHZ 100PF
U14
U14
VCC
VCC
U8
PRE
D
CP
CLR
Q
2MHZ
VCC
VCC
U8
VCC
330
98
S STACK
4A
2
4MHZ
74LS00
U3
U7
U16
U11
U6
U1
CLK
Ø2
Ø1
49
24
25
VCC
330
A15 32
A14 86
A13 85
A12 33
A11 87
A10 37
A9 34
A8 84
A7 83
A6 82
A5 29
A4 30
A3 31
A2 81
A1 80
A0 79
U24
U25
U23
U22
U21
Z-80
U5
A11
A12
A13
A14
A15
Ø
D4
D3
D5
D6
VCC
D2
D7
D0
DI
INT
NMI
HALT
MREQ
IORQ
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
GND
RFSH
MI
RESET
BUSRQ
WAIT
BUSAK
WR
RD
+5
4.7K
100 D
75
PRESET
25MFD
12V
E
55
2N3643
220
F
180
99
POC
53
SSWDSBL
RUN
71
SS
21
RFRSH
66
74
PHOLD
26
PHLDA
WAIT STATE
4.7K
VCC
B
72
PRDY
3
XRDY
U13
U4
U9
U18
U15
U2
U1
U12
U17
U16
27
PWAIT
44
SMI
48
SHLTA
18
STATUS DSBL
U28
U20
U19
68
MWRITE
8V
1,51
UNREG
100
GND
50
GND
LM340-5
OR
7805
0.1
22MFD
12V
22MFD
12V
+5V (VCC)
SOUT
PWR
C
DI0 95
DO0 36
DI1 94
DO1 35
DI2 41
DO2 88
DI3 42
DO3 89
DI4 91
DO4 38
DI5 92
DO5 39
DI6 93
DO6 40
DI7 43
DO7 90
U27
U26
U25
8,9
7,10
6,11
5,12
4,13
3,14
2,15
1,16
J1
16 PIN DIP
U10
D1 = F3
E1 = FB
470 PF
U9
NMI
PINT
73
12
U15
PWR
77
PDBIN
78
SMEMR
47
SINTA
96
SINP
46
SOUT
45
SWO
97
PSYNC
76
PINTE
28
ADD DSBL
22
POC
99
DO DSBL
23
C/C DSBL
19
NOTE: ALL RESISTORS
1K UNLESS OTHER-
WISE STATED
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Z-80 CPU REV-2 7-13-79