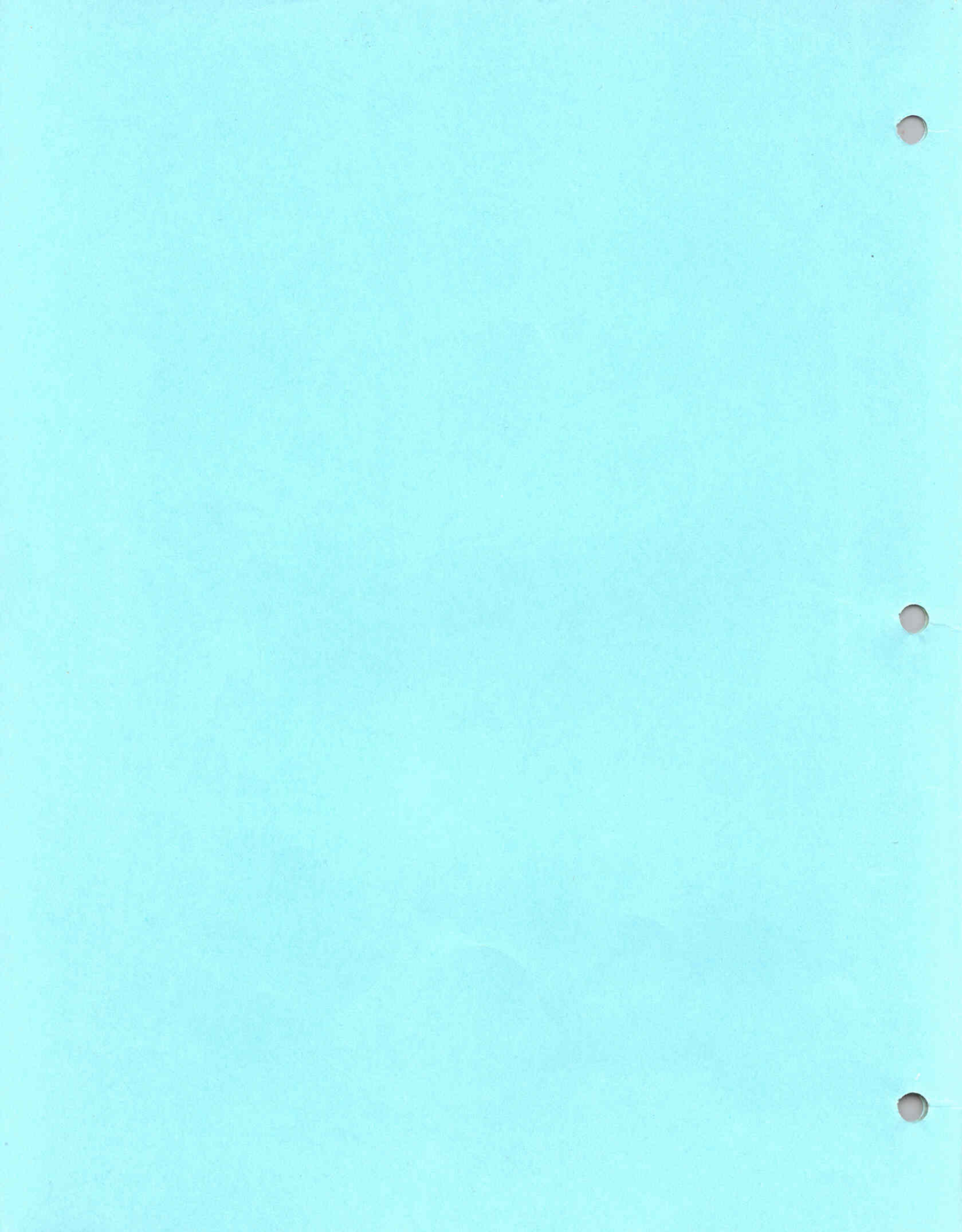


**VDM-1 VIDEO DISPLAY MODULE
ASSEMBLY and TEST INSTRUCTIONS**



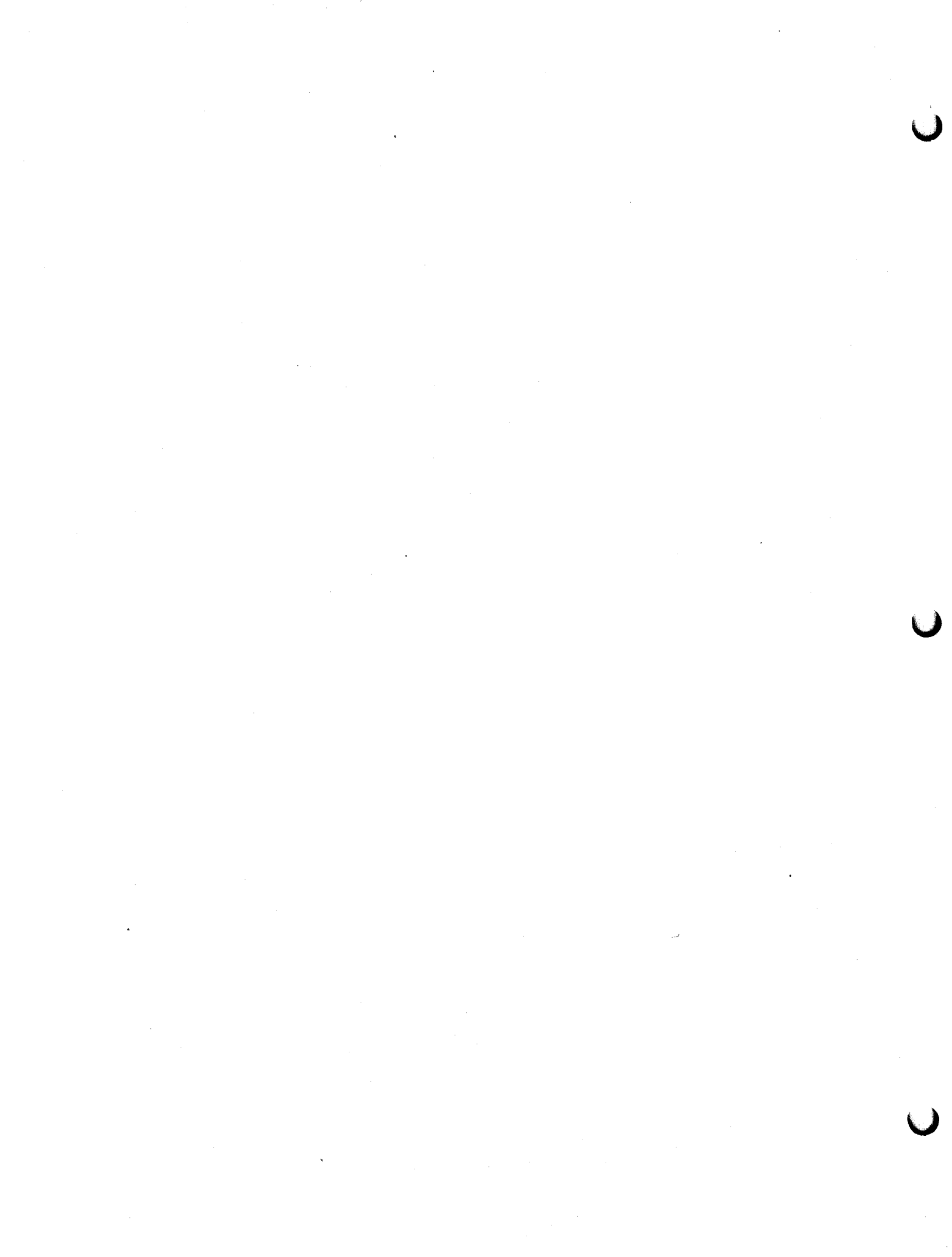
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Emeryville, CA 94608
Phone: (415)652-8080



Dick Peeling

VDM-1 VIDEO DISPLAY MODULE
ASSEMBLY AND TEST INSTRUCTIONS

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Manual No. 208003



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SECTION I

INTRODUCTION and
GENERAL INFORMATION

VDM-1 VIDEO DISPLAY MODULE





1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the VDM-1 Video Display Module. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components listed in the "Parts List" (Table 2-1) in Section II. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from backward installed components and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 VDM-1 Description

The VDM-1 Video Display Module is not a limited "TV Typewriter". It is an ultra-high speed display generator designed to operate with your Altair, IMSAI, or other S100 computer.

This display module generates sixteen 64 character lines from data stored in a 1024 8-bit byte on-card RAM memory (random access memory). Alphanumeric and control characters (the full 128 upper and lower case plus control ASCII character set) are displayed in a 7 x 9 dot matrix. With its EIA video output, the VDM-1 can be used with any standard video monitor. (A TV set can also be easily modified for use with the VDM-1. See Appendix VI.)

A two-port memory permits random read-write access to the screen memory from the memory bus of the CPU. Other features include:

1. Normal (white-on-black background) video display or inverted (black-on-white background) video display, switch-selectable for entire screen or program-controlled for each character.
2. Video inversion block cursor, switch-selectable blink capability, programmable for each character location.
3. Continuously adjustable display position, both vertical and horizontal.
4. Text blanking (switch selectable) from CR control character to end of line and from VT control character to end of screen, excluding CR or VT character.

5. Optional blanking of all control characters (switch selectable).
6. Program-controlled scrolling of display in increments of one to 16 lines without rewriting memory.
7. "Window shade" blanking of text above desired starting location, program controllable.
8. Scroll timer on board available for test by processor.

1.2.2 Receiving Inspection

When your module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology should it become necessary to do so.) If your VDM-1 kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, the parts supplied with the module, as well as the assembled module, are warranted against defects in materials and workmanship for a period of 6 months after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (e.g. DM8131) and/or a complete description (e.g., 6.8 ohm, $\frac{1}{2}$ watt, 5% resistor).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the module to Processor Technology, first obtain authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the module, proceed as follows:

1. Write a description of the problem.
2. Pack the module with the description in a container suitable to the method of shipment.
3. Ship prepaid to Processor Technology, 6200 Hollis Street, Emeryville, CA 94608.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

SECTION II

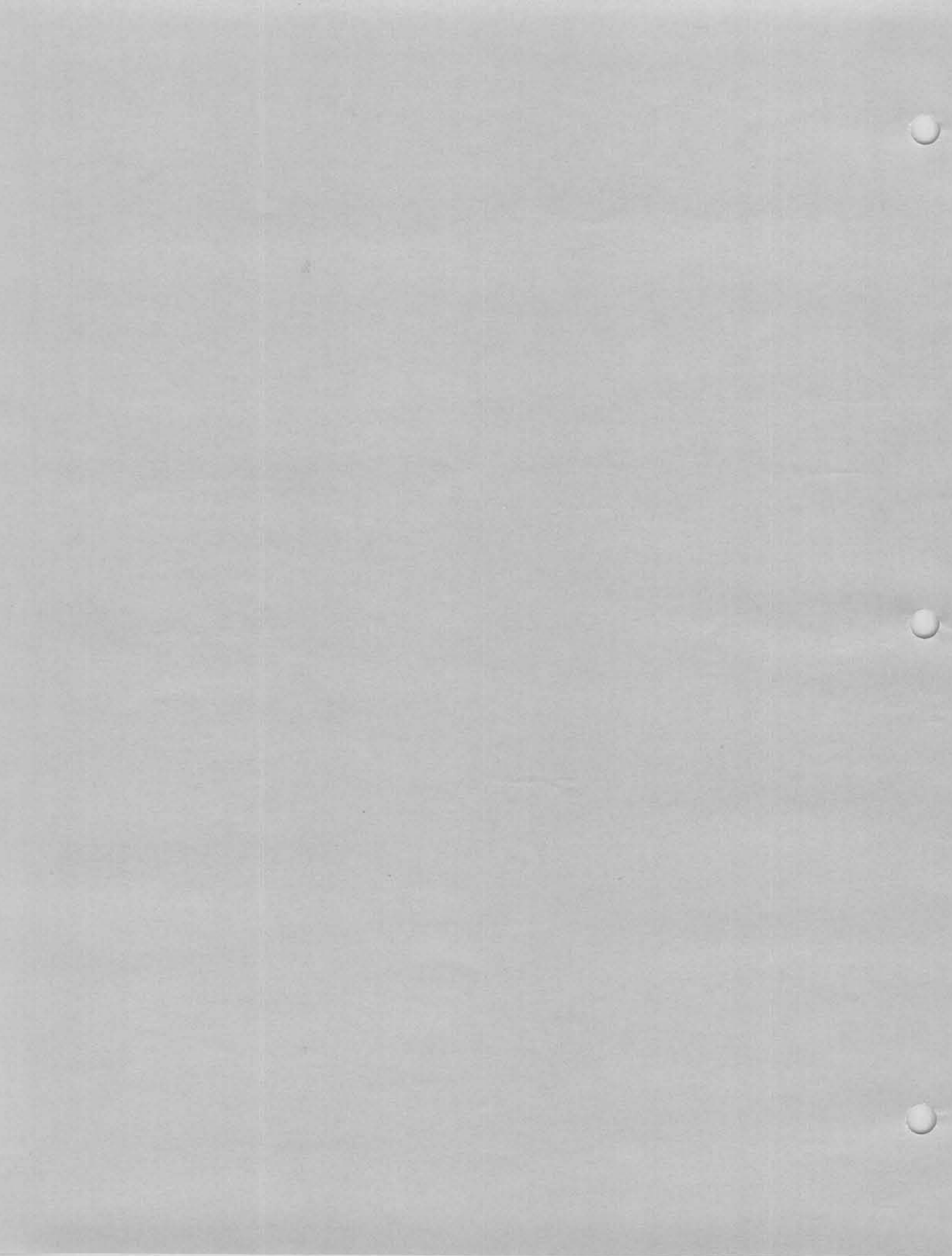
ASSEMBLY

and

TEST

VDM-1 VIDEO DISPLAY MODULE





2.1 ASSEMBLY TIPS

1. Scan Section II in its entirety before you start to assemble the VDM-1.

2. In assembling your VDM-1, you will be following an integrated assembly-test procedure. Such a procedure is designed to progressively insure that individual sections of the module are operating correctly. IT IS IMPORTANT THAT YOU FOLLOW THE STEP-BY-STEP INSTRUCTIONS IN THE ORDER GIVEN.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. When installing components, make use of the assembly aids that are incorporated on the VDM-1 PC board and the assembly drawing: (These aids are designed to assist you in correctly installing the components.)

- a. The circuit reference (R3, C10 and IC20, for example) for each component is silk screened on the PC board near the location of its installation.
- b. An alphanumeric "grid", that divides the board into 90 areas, is also silk screened on the PC board. (In assembly instructions, grid coordinates are used to define the areas in which specific components are located)
- c. Both the circuit reference and value or nomenclature (1.5K and 7406, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that the color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5).

6. Install disc capacitors as close to the board as possible.

7. Heat sink compound is supplied with this kit in a small clear plastic package. It is a thick white substance which improves heat transfer between components and their heat sinks. To use the compound, pierce a small hole near the edge of the top surface of the plastic package, using a pin or sharp knife point. Squeezing the package will cause a small amount of the compound to ooze out of the hole, which may then be applied with a toothpick or small screwdriver blade. Spread a thin film of the compound on the mating surfaces of both the heat-generating component and the heat sink surface which it will contact. Then assemble as directed.

8. Should you encounter any problem during assembly, call on us for help if needed.

2.2 ASSEMBLY PRECAUTIONS

2.2.1 Handling MOS Integrated Circuits

Several MOS integrated circuits are used in the VDM-1, and they can be damaged by static electricity discharge. Always handle MOS ICs so that no discharge will flow through the IC. Also, avoid unnecessary handling and wear cotton--rather than synthetic--clothing when handling these ICs.

2.2.2. Soldering

1. Use a low-wattage iron, 25 watts maximum.

2. Solder neatly and quickly as possible.

3. DO NOT press top of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

4. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

5. The VDM-1 uses a circuit board with plated-through holes. Solder flow through to the component side of the board can produce solder bridges. Check for such bridges after each installation.

6. The VDM-1 circuit board has an integral solder mask (green lacquer) that shields selected areas on the board. This mask minimizes the chances of creating solder shorts during assembly.

7. Additional pointers on soldering are provided in Appendix III of this manual.

2.2.3 Installing and Removing VDM-1

NEVER install the VDM-1 in, or remove it from, the computer with the power on. To do otherwise can damage the board.

2.2.4 Installing and Removing Integrated Circuits

NEVER install or remove integrated circuits with power applied to the VDM-1.

2.3 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the VDM-1:

1. Needle nose pliers

2. Diagonal cutters

3. Controlled heat soldering iron, 25 watts

4. Sharp knife

5. 60-40 rosin-core solder (supplied)

6. Volt-ohm meter
7. Oscilloscope (optional)
8. IC test clip (optional)

2.4 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1). If you have difficulty in identifying any parts by sight, refer to Figure 2-1.

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper righthand corner of the board when the edge connector is positioned at the bottom of the board. In this position, the component (front) side of the board is facing up. Subsequent position references assume this orientation.

2.6 ASSEMBLY-TEST PROCEDURE

Refer to assembly drawing in Section IV.

CAUTION

THIS DEVICE USES SEVERAL MOS INTEGRATED CIRCUITS WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE MOS IC SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN HANDLING THESE ICs.

- (✓) Step 1. Install sockets in locations IC1 through IC48. Each socket should be installed with its end notch oriented as indicated on the assembly drawing. Avoid creating solder bridges between pins and traces.
- (✓) Step 2. Install Q1 (2N2907) in Area G-2. The emitter lead (closest to tab on can) is oriented toward top of board and the base lead to the left. Push straight down on transistor until it is stopped by the leads. Solder and trim.
- () Step 3. Install all resistors in numerical order in the indicated locations. Bend leads to fit distance between mounting holes, insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

Refer to footnotes at the end of this step before installing flagged (*, **, #, ##, @ or @@) resistors.

PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

SECTION II

Table 2-1. VDM-1 Video Display Module Parts List.

<u>INTEGRATED CIRCUITS</u>			
1 4001 (IC30)	1 7406 (IC1)	4 74LS163 (IC2,20,21,22)	
2 4029 (IC26,27)	2 74LS08 (IC33,34)	1 74166 (IC3)	
2 4042 (IC31,32)	2 74LS10 (IC9,40)	3 74LS175 (IC5,6,17)	
1 4049 (IC25)	1 74LS20 (IC7)	2 8097 or 8T97 (IC38,39)	
1 MCM6574,6575 or 6576 (IC4)	1 74LS86 (IC12)	1 8131 (IC29)	
2 74LS00 (IC15,35)	3 74LS109 (IC10,13,16)	1 8836 or 8T380 (IC37)	
1 74LS02 (IC14)	1 74LS132 (IC18)	8 91L02 or 21L02 (IC41 through IC48)	
2 74LS04 (IC19,36)	1 74LS138 (IC11)	1 93L16 (IC8)	
3 74LS157 (IC23,24,28)			
<u>REGULATORS</u>	<u>TRANSISTORS</u>	<u>DIODES</u>	<u>CRYSTALS</u>
1 340T-5.0V or 7805UC (IC49)	1 2N2907 (Q1)	1 1N5225B (D1)	1 HC-18/U (Y1), 14.318 MHz
1 78L12A (IC50)		2 1N4148 (D2,3)	
<u>RESISTORS</u>		<u>CAPACITORS</u>	
1 75 ohm, 1/4 watt, 5%		1 10 pfd, disc	
2 100 ohm, 1/4 watt, 5%		1 680 pfd, disc	
1 200 ohm, 1/4 watt, 5%		3 .001 ufd, disc	
2 330 ohm, 1/4 watt, 5%		1 .001 ufd, mylar	
1 680 ohm, 1/2 watt, 5%		1 .01 ufd, mylar	
5 8.2K ohm, 1/4 watt, 5%		1 .1 ufd, mylar	
3 39 K ohm, 1/4 watt, 5%		31 .1 ufd, disc	
2 50 K ohm potentiometers		4 1 ufd, tantalum	
1 100 K ohm, 1/4 watt, 5%		1 15 ufd, tantalum	
30 1.5K ohm, 1/4 watt, 5%		1 100 ufd, 15V, electrolytic	
2 3.3M ohm, 1/4 watt, 5%			
<u>MISCELLANEOUS</u>			
1 VDM-1 PC Board		1 Tie Wrap	
1 Heat Sink		1 Length Spaghetti	
48 DIP Sockets		3 6-32 Screws	
1 DIP Switch, 6 or 7 position		3 6-32 Lockwashers	
1 Length #24 Bare Wire		3 6-32 Nuts	
9" 8-conductor Ribbon Cable		1 Length Solder	
1 Length 72-ohm Coaxial Cable		1 Manual	

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SECTION II

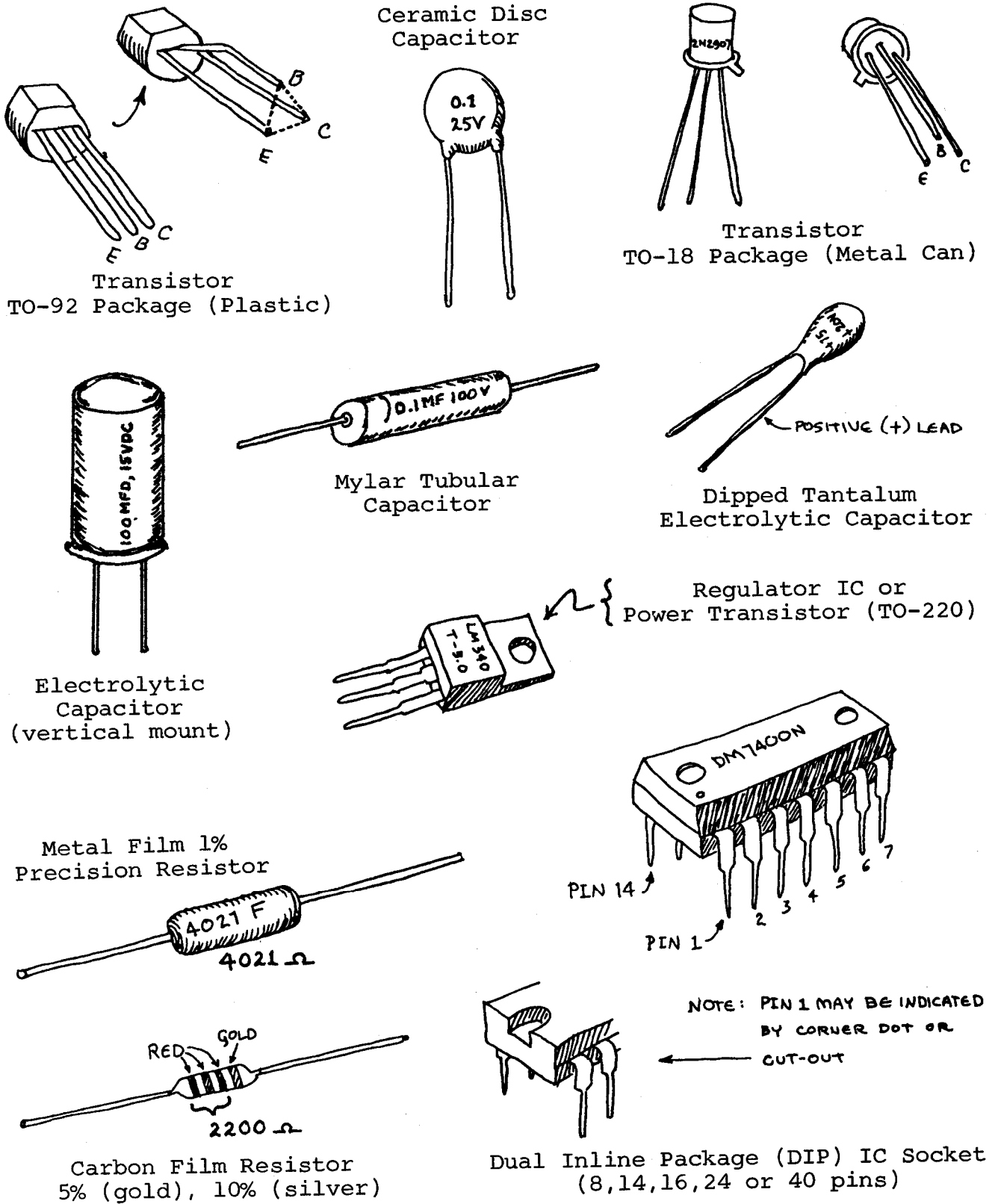


Figure 2-1. Identification of components.

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SECTION II

<u>LOCATION</u>	<u>AREA</u>	<u>VALUE (OHMS)</u>	<u>COLOR CODE</u>
R1*	A-1	75	violet-green-black
R2*	A-1	100 ¼ watt	brown-black-brown
R3*	A-2	100 ¼ watt	brown-black-brown
R4**	A-3	1.5 K	brown-green-red
R5+	A-4	1.5 K	" " "
R6	A-10	680 ½ watt	blue-grey-brown
R7+	B-2	1.5 K	brown-green-red
R8	B-2	39 K	orange-white-orange
R9	B-4	1.5 K	brown-green-red
R10	B-4	1.5 K	" " "
R11	B-5,6	200	red-black-brown
R12	B-10	1.5 K	brown-green-red
R13	C-3,4	1.5 K	" " "
R14	C-4	1.5 K	" " "
R15	C-6,7	1.5 K	" " "
R16*	D-3	330	orange-orange-brown
R17*	D-3	330	" " "
R19+	D-4	1.5 K	brown-green-red
R20	D-6	1.5 K	" " "
R21	E-1,2	3.3 M	orange-orange-green
R22	E-1,2	8.2 K	grey-red-red
R23	E-1,2	100 K	brown-black-yellow
R24	E-3	3.3 M	orange-orange-green
R25	E-4	1.5 K	brown-green-red
R26+	E-5	1.5 K	" " "
R27-32#	E-7,8	1.5 K	" " "
R33##	F-1	50 K	Potentiometer
R34*	F-2	8.2 K	grey-red-red
R35	F-2	8.2 K	" " "
R36@	F-1,2	1.5 K	brown-green-red
R37	F-2	39 K	orange-white-orange
R38	F-2,3	8.2 K	grey-red-red
R39	F-3	39 K	orange-white-orange
R40+	F-5	1.5 K	brown-green-red
R41-48@@	F-7	1.5 K	" " "
R49	F-9	1.5 K	" " "
R50##	G-1	50 K	Potentiometer
R51*	G-2	8.2 K	grey-red-red

NOTE

Unless noted otherwise, all resistors are ¼ watt, 5%.

- * Check for solder bridges to ground plane.
- ** Move R4 away from IC1 (Area A-2,3) toward IC2 (Area A-3,4) before soldering.
- + Be sure leads do not short traces beneath them.

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SECTION II

- # Leads at bottom of board (toward edge connector) must not short to one another.
- ## Install parallel to board with thumb wheels at top edge of board. Check for solder bridges to ground plane after installation.
- @ Take care that R35 and R36 leads do not short.
- @@ Check for solder bridges after installation.
- () Step 4. Install all capacitors in numerical order. Insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through the mounting holes, remove the capacitor and clear the holes of any wax. Reinsert and install.

Refer to footnotes at the end of this step before installing flagged (*, **, @, @@, # or ##) capacitors.

<u>LOCATION</u>	<u>AREA</u>	<u>VALUE (UFD)</u>	<u>TYPE</u>
C1*	A-1,2	100	Electrolytic
C2	A-2,3	.1	Disc
C3	A-2	.1	Disc
C4	A-5	.1	Disc
C5	A-7	.1	Disc
C6	A-8	.1	Disc
C7*	A-8	1	Tantalum, dipped
C8*	A-9	1	Tantalum, dipped
C9*	A-9,10	1	Tantalum, dipped
C10	B-1	.1	Disc
C11	B-5	.1	Disc
C12	B-8	.1	Disc
C13	B-10	.1	Disc
C14	C-2	.1	Disc
C15	C-4	.1	Disc
C16	C-5	.1	Disc
C17	C-9	.1	Disc
C18	D-1	.1	Disc
C19	D-2	10 pfd	Disc
C20	D-2	.1	Disc
C21**	D-3	.001	Disc
C22@	D-4	.1	Disc
C23	D-5	.1	Disc
C24	D-9	.1	Disc

PROCESSOR TECHNOLOGY CORPORATION

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SECTION II

<u>LOCATION</u>	<u>AREA</u>	<u>VALUE (UFD)</u>	<u>TYPE</u>
(S) C25@@	E-1,2	.01	Mylar tubular
(S) C26	E-7	.1	Disc
(S) C27#	F-2	.001	Mylar tubular
(S) C28##	F-2	.001	Disc
(S) C29##	F-3	680 pfd	Disc
(S) C30	F-3,4	.001	Disc
(S) C31	F-4	.1	Mylar tubular
(S) C32	F-6	.1	Disc
(S) C33	F-9	.1	Disc
(S) C34	G-2	.1	Disc
(S) C35	G-4	.1	Disc
(S) C36	G-5	.1	Disc
(S) C37	G-9	.1	Disc
(S) C38	G-10	.1	Disc
(S) C39*, **	H-1	15	Tantalum, dipped
(S) C40	H-1	.1	Disc
(S) C41*, **	H-2	1	Tantalum, dipped
(S) C42	J-5	.1	Disc
(S) C43	J-7	.1	Disc
(S) C44	J-8	.1	Disc
(S) C45	J-9	.1	Disc

* Take care to observe polarity.

** Check for solder bridges to ground plane.

@ Check that C22 lead doesn't short to R19 (Area D-4). Move R19 lead as required.

@@ Do not center C25 between mounting holes. Position it so the capacitor is closer to the top mounting hole and the resulting longer lead at the bottom end.

Check that C27 lead doesn't short to R36 (Area F-1,2). Move R36 lead as required.

Be careful not to interchange C28 and C29.

(S) Step 5. Install diode D1 (1N5225B) in Area A-10. Position D1 so that its band mark (cathode) is on the righthand side. Solder and trim leads.

(S) Step 6. Install diodes D2 and D3 (1N4148) in Area E-1,2. Position these diodes with the band mark (cathode) at top of board. Solder and trim leads.

(S) Step 7. Install heat sink in Area H,J-1,2,3,4. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the triangle of holes is under one of the triangular cut-outs in the sink. Using two 6-32 screws, nuts, and lockwashers, attach the heat sink to the board. Insert screws from back (solder) side of board. (See Figure 2-2.)

- () Step 8. Install IC49 (340T-5.0V or 7805) in Area J-1,2,3. Position IC49 on heat sink and observe how the leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent downwards at a point approximately 0.2 inches further from the body than the other leads. Bend the leads so that no contact is made with the heat sink when IC49 is flat against the sink and its mounting hole is aligned with the hole in the sink. Apply heat sink compound as directed in assembly tip 7 on page II-1. Fasten IC49 to sink using 6-32 screw, lockwasher and nut. Insert screw from back (solder) side of board. Solder and trim leads. (See Fig. 2-2)

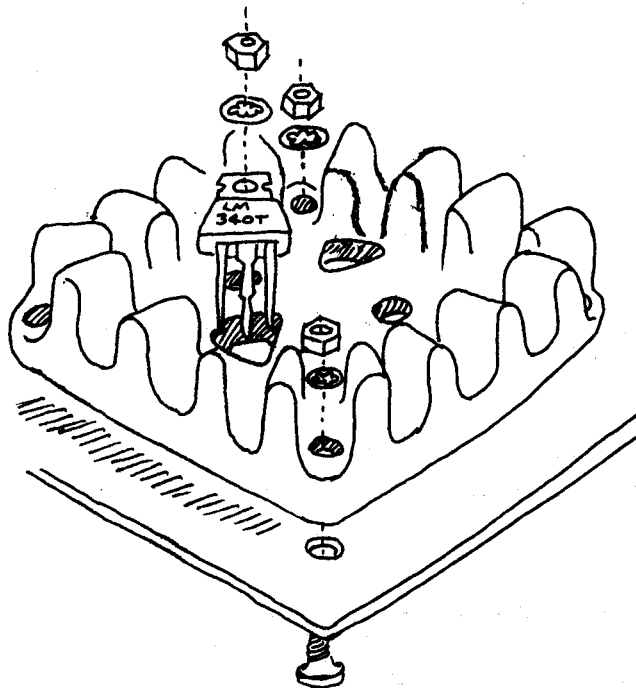


Figure 2-2. Heat sink and IC49 installation.

- () Step 9. Install IC50 in Area A-9. (See detail drawing on component location diagram.) Install IC50 with flat facing left. Bend center lead back to fit into mounting hole. Push straight down until the IC is stopped by its leads. Solder and trim leads.
- () Step 10. Install crystal Y1 in Area D-1,2. (See detail drawing on component location diagram.)
- () Install Y1 so that it lies flat against board as shown (case at top of board), solder leads and trim. Using a piece of excess crystal lead, ground the crystal case as indicated in the detail drawing. First solder on the back side of board. Then solder the lead to the crystal case. (See CAUTIONS on Page II-10.)

CAUTION 1

SOLDER QUICKLY SO THAT EXCESSIVE HEAT WILL NOT BE APPLIED TO CRYSTAL.

CAUTION 2

THE CRYSTAL GROUND LEAD MUST NOT SHORT TO TOP TRACE ON BACK (SOLDER) SIDE OF BOARD. IF THIS SHORT DOES EXIST, THE COMPUTER FUSE WILL BLOW.

- (✓) Step 11. Check that crystal Y1 ground is not shorted to top trace on back (solder) side of board. Use an ohmmeter to measure the resistance between the top trace on the back side of the board and the crystal case. You should measure some resistance. Zero resistance indicates a solder bridge. Correct the condition.

Proceed to Step 12 if you measure some top trace-to-crystal case resistance.

- (✓) Step 12. Check regulator operation. This check is made to prevent potential subsequent damage to the ICs from incorrect voltages.

- (✓) Install VDM-1 in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON. TO DO OTHERWISE CAN DAMAGE THE BOARD.

- () Turn power on and make the following voltage measurements:

<u>MEASUREMENT POINT</u>	<u>AREA</u>	<u>VOLTAGE</u>
Pin 3 of IC50	A-8,9	12 vdc \pm 5%
Anode of D1	A-10	-3 vdc \pm 10%
Pin 14 of IC1	A-2	5 vdc \pm 5%

- () If any voltages are incorrect, determine and correct the cause before proceeding. Especially check for solder shorts.

If voltages are correct, go on to Step 13.

- (✓) Step 13. Install jumper in Area D,E-9. Cover a piece of excess resistor lead with $\frac{1}{4}$ " spaghetti, bend to fit holes, insert, solder and trim.

- () Step 14. Install coaxial cable in Area A,B-1. (See Figure 2-3 for details on how to prepare cable.)
- () Strip away approximately $1\frac{1}{4}$ " of the outer insulation to expose the shield. Unbraid shield, gather and twist into a single lead. Then strip away the inner conductor insulation, leaving about $1/4$ " at the shield end.

CAUTION

WHEN PREPARING AND INSTALLING SHIELD, BE SURE BITS OF BRAID DO NOT FALL ON-TO BOARD. SUCH DEBRIS CAN CREATE HARD-TO-FIND SHORT CIRCUITS.

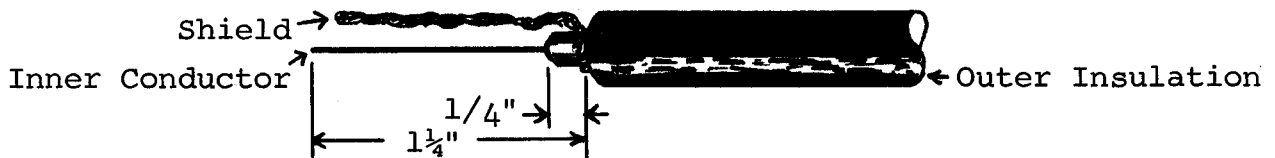


Figure 2-3. Coaxial cable preparation.

- () Insert inner conductor in indicated mounting hole, solder and trim. Solder shield to ground plane and trim. Install tie wrap as shown.

CAUTION

AFTER INSTALLATION, FINE BITS OF THE BRAID FROM THE SHIELD MAY WORK LOOSE AND FALL ONTO THE BOARD AND CREATE HARD-TO-FIND SHORT CIRCUITS. TO PREVENT THIS, COAT ALL EXPOSED BRAID WITH AN ADHESIVE AFTER SOLDERING AND BEFORE TIEING. USE AN ADHESIVE SUCH AS SILICONE, CONTACT CEMENT OR FINGER-NAIL POLISH. DO NOT USE WATER BASE ADHESIVES.

- () Step 15. Install DIP Switch in Area B-1,2. Position it so Switch No. 1 is at left end of pad. As you will note, the DIP Switch pad is designed to accommodate a 7-position switch. If a 6-position (12 pin) switch is supplied, position it as far to the left as possible. (The two holes to the right will be unused in this case.) If a 7-position (14 pin) switch is supplied, remember that Switch No. 7 is not used.

NOTE

The function of the DIP switches is defined in Section III of this manual.

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- () Step 16. Install the following ICs in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Dots on the assembly drawing and PC board indicate the location of pin 1 of each IC.

<u>IC NO.</u>	<u>AREA</u>	<u>TYPE</u>
(✓) IC1	A-2,3	7406
(✓) IC2	A-3,4	74LS163
(✓) IC7	B-3	74LS20
(✓) IC8	B-4,5	93L16
(✓) IC9	B-6,7	74LS10
(✓) IC14	C-4,5	74LS02
(✓) IC15	C-6	74LS00
(✓) IC16	C-7	74LS109
(✓) IC19	D-3,4	74LS04
(✓) IC20	D-5	74LS163
(✓) IC21	D-6	74LS163
(✓) IC22	D-7	74LS163

- () Step 17. Check timing chain operation. If you do not have an oscilloscope, proceed to Step 18.

- (✓) Install VDM-1 in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON.

- (✓) Turn power on. Using an oscilloscope, check for the waveforms given in Figure 2-4 at the indicated observation points and in the order given. The waveforms shown in Figure 2-4 approximate actual waveforms. If any waveforms are incorrect, determine and correct the cause. Especially check for solder bridges and incorrectly installed ICs.

NOTE

Irregularities up to 1 volt are acceptable on positive portions of waveforms. Negative portions, however, should be relatively flat.

If all waveforms are correct, proceed to Step 18.

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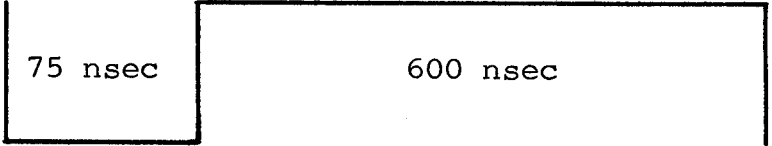





<u>CHECK POINT</u>	<u>AREA</u>	<u>WAVEFORM</u>
() IC19, pin 3	D-3,4	13.5 MHz square wave. (This is not a perfect square wave. It in fact more resembles a poor sine wave.)
() IC19, pin 11	D-3,4	
() IC19, pin 13	D-3,4	
() IC22, pin 11	D-7	
() IC21, pin 11	D-6	
() IC2, pin 11	A-3,4	
() IC8, pin 11	B-4,5	
() IC16, pin 10	C-7	

Figure 2-4. Timing Waveforms

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- () Step 18. Install the following ICs in the indicated locations. Observe the same general instructions given in Step 16.

<u>IC NO.</u>	<u>AREA</u>	<u>TYPE</u>
(✓) IC12	C-2	74LS86
(✓) IC25*	E-3	4049
(✓) IC30*	F-3	4001

*MOS devices. Refer to CAUTION on Page II-3.

- () Step 19. Check synchronization circuits.

- () Set DIP Switch as follows:

Switch No. 1: ON
All other switches: OFF

- () Install VDM-1 in computer. Observe CAUTION given in Step 17. Then connect VDM-1 to video monitor.
- () Set R33 (VERT) and R50 (HORIZ) on the VDM-1 to their mid-range settings. Turn computer and monitor on.

NOTE

In making this check, the Horizontal Hold Control on monitor may always be readjusted to center display.

- () The display raster will be pulled in. Using the monitor vertical hold, you should be able to obtain a slow roll (black horizontal bar moves slowly down the screen) and a stationary raster. Using the monitor horizontal hold, you should be able to adjust for an out of sync raster (numerous black lines cutting across the raster) and a stable raster. If you do not observe these conditions, try adjusting R33 and R50 on the VDM-1. If you are still unable to obtain the indicated conditions, determine and correct the cause before proceeding.

NOTE

For a stable presentation, a few monitors--especially modified TV sets---may require a higher sync amplitude than that supplied by the VDM-1. In such cases, increase sync amplitude by reducing value of R2 (Area A-1). DO NOT DECREASE R2 BELOW 225 OHMS.

- () If the aforementioned vertical and horizontal conditions are realized, turn Switch No. 1 OFF and Switch No. 2 ON. The monitor screen should darken, and you should be able to obtain the previously described vertical and horizontal conditions. If operation is not as described after turning Switch No. 1 OFF and Switch No. 2 ON, determine and correct the cause.

If the synchronization circuits are operating correctly, proceed to Step 20.

- () Step 20. Install the following ICs in the indicated locations. Observe the same general instructions given in Step 16.

<u>IC NO.</u>	<u>AREA</u>	<u>TYPE</u>
() IC3	A-4,5	74166
() IC4*	A-6,7	MCM6575,6576 or 6574
() IC5	A-8	74LS175
() IC6	A-9	74LS175
() IC17	C-8	74LS175

*MOS devices. Refer to CAUTION on Page II-3.

CAUTION 1

TO INSURE THAT IC4 WILL NOT BE DAMAGED BY STATIC DISCHARGE, GROUND YOURSELF TO COMPUTER CHASSIS, REMOVE IC4 FROM PACKAGE AND INSTALL ON VDM-1 BOARD.

CAUTION 2

IC4 IS A CERAMIC PACKAGE AND FRAGILE. USE AN EVENLY DISTRIBUTED, EASY PRESSURE WHEN LOADING IC4.

CAUTION 3

PIN 1 ON IC4 IS INDICATED BY A RAISED BUMP ON TOP OF THE IC. TAKE CARE TO LOAD IT CORRECTLY.

- () Step 21. Check video circuits and character generator (IC4).

- () Using wire jumpers and tack soldering technique, make the following TEMPORARY connections:

IC15 (Area C-6): Pin 2 to 7
 IC17 (Area C-8): Pin 5 to 8
 Pin 4 of IC7 (Area B-3) to pin 1 of IC8 (Area B-4,5)

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- () Set up DIP Switch as follows:
- Switches No. 2 and 5: ON
All other switches: OFF
- () Install VDM-1 in computer. Observe CAUTION in Step 17. Then connect VDM-1 to video monitor.
- () Adjust R33 and R50, and monitor Horizontal Hold Control if required, to center pattern on screen. Check for 16 lines of 64 white dashes (actually ASCII underscore characters) on black background. (See Figure 2-4.)
- () Set Switch No. 1 to ON and Switch No. 2 to OFF. Check for 16 lines of 64 black dashes (ASCII underscores) on white background. (See Figure 2-5.)
- () Set Switch No. 3 to ON. Check for 16 lines of 64 white dashes (ASCII underscores) on black background surrounded by white frame. (See Figure 2-7 on Page II-18.)
- () Set Switch No. 3 to OFF and Switch No. 4 to ON. White frame in preceding presentation should remain and the display should alternate between those in Figures 2-5 and 2-7.
- () Set Switch No. 1 and No. 4 to OFF and Switch No. 2 and No. 3 to ON. Check for 16 lines of 64 black dashes (ASCII underscores) on white background surrounded by black frame. (See Figure 2-6 on Page II-18.)
- () Set Switch No. 3 to OFF and Switch No. 4 to ON. Black frame in preceding presentation should remain and the display should alternate between those in Figures 2-4 and 2-6.
- () If your VDM-1 fails to pass any of the preceding tests, DO NOT PROCEED BEYOND THIS STEP without determining and correcting the problem.
- () If your VDM-1 passes all of the preceding tests, REMOVE TEMPORARY JUMPERS installed at beginning of this step and go on to Step 22.
- () Step 22. Install remaining ICs in the indicated locations. Observe the same general instructions given in Step 16.

	<u>IC NO.</u>	<u>AREA</u>	<u>TYPE</u>
()	IC10	B-7,8	74LS109
()	IC11	B-9	74LS138
()	IC13	C-3	74LS109
()	IC18	C-9,10	74LS132
()	IC23 & 24	D-8,9,10	74LS157

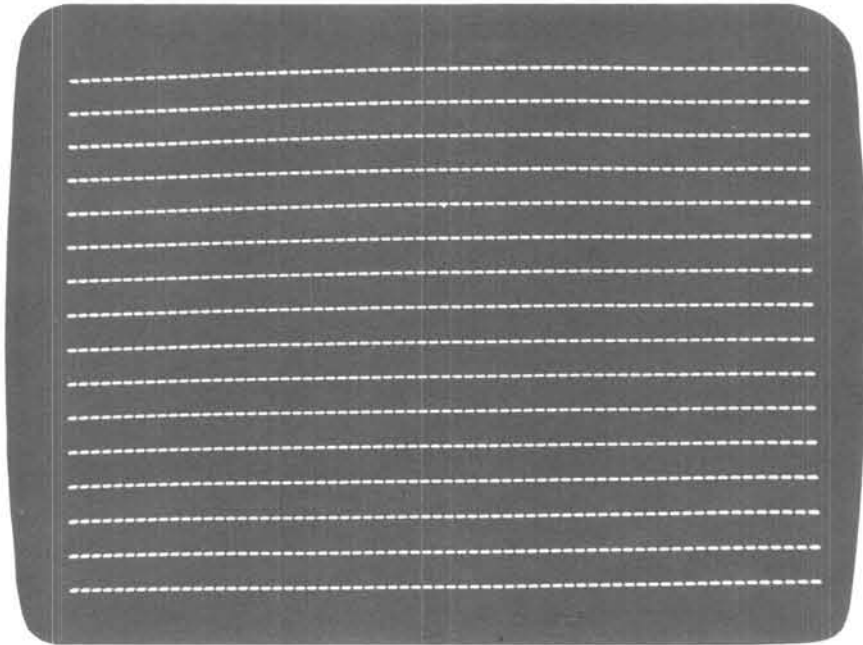


Figure 2-4. Video circuit check: SW2 & 5 ON, SW1,3,4 & 6 OFF.

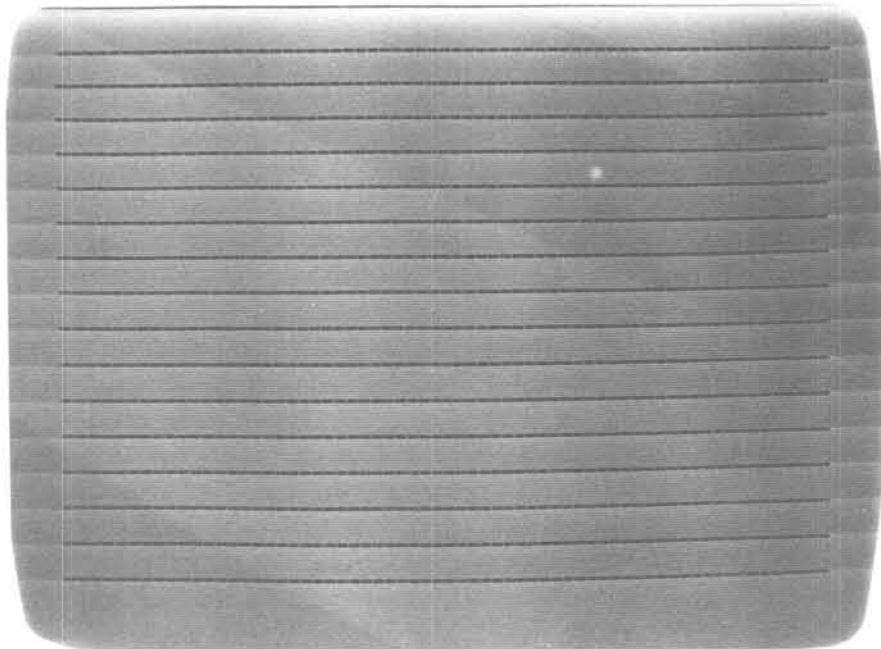


Figure 2-5. Video circuit check: SW1 ON, SW2 OFF.

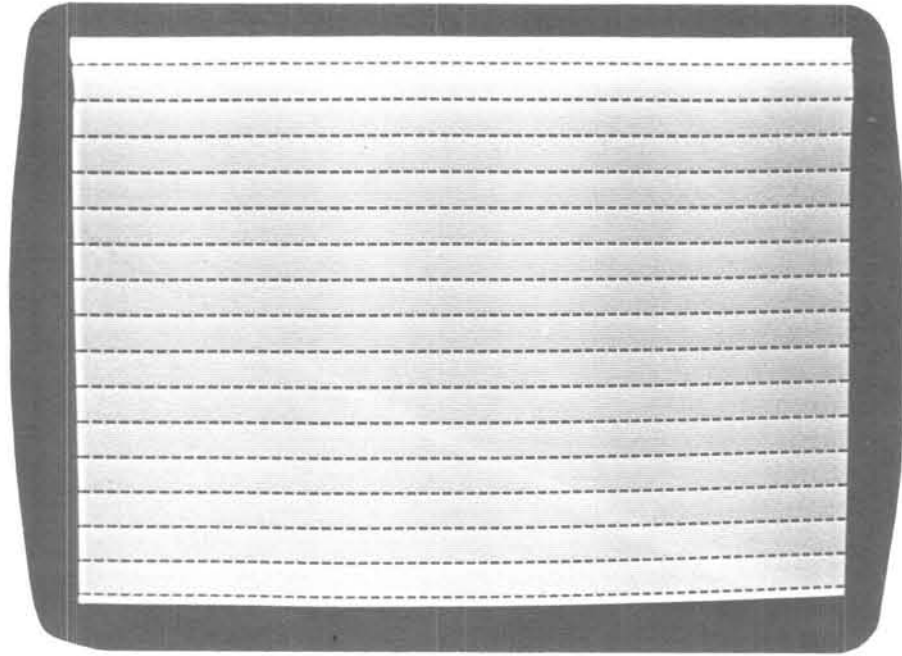


Figure 2-6. Video circuit check: SW1 & 4 OFF, SW2 & 3 ON.

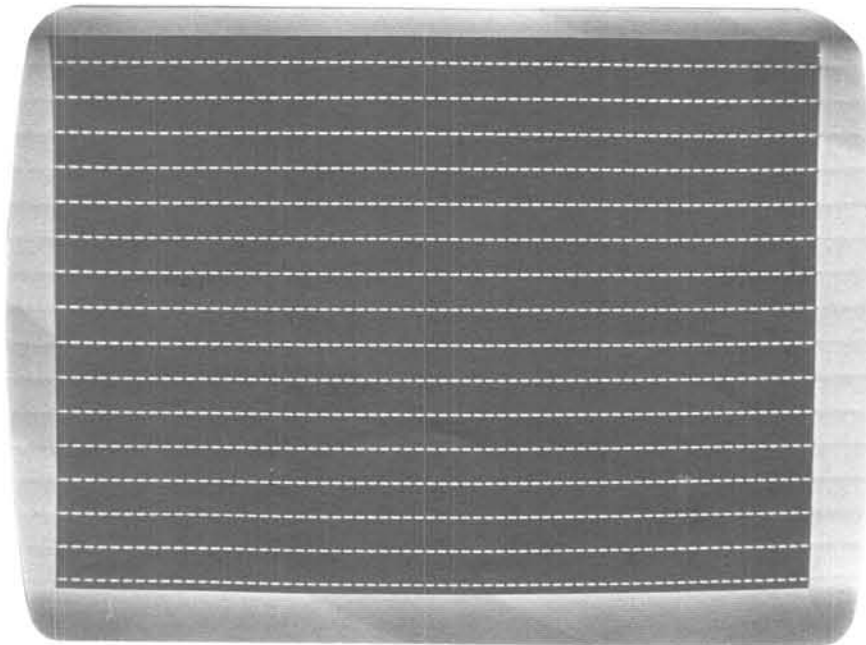


Figure 2-7. Video circuit check: SW1 & 3 ON, SW2 OFF.

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<u>IC NO.</u>	<u>AREA</u>	<u>TYPE</u>
() IC26 & 27*	E-4,5	4029
() IC28	E-6	74LS157
() IC29	E-9	8131
() IC31 & 32*	F-4,5,6	4042
() IC33 & 34	F-8,9,10	74LS08
() IC35	G-3	74LS00
() IC36	G-4,5	74LS04
() IC37	G-5,6	8836 or 8T380
() IC38 & 39	G-8,9,10	8097 or 8T97
() IC40	H-1,2,3	74LS10
() IC41 thru 48*	H,J-5,6,7,8,9	91L02 or 21L02

*MOS device. Refer to CAUTION on Page II-3.

- () Step 23. Set VDM-1 address. The Software included with the VDM-1, as well as future releases, requires setting the VDM memory address to CC00 (hex) and the I/O control port to C8 (hex). To connect the VDM for these "standard" address assignments, wire jumpers as shown in Figure 2-8.

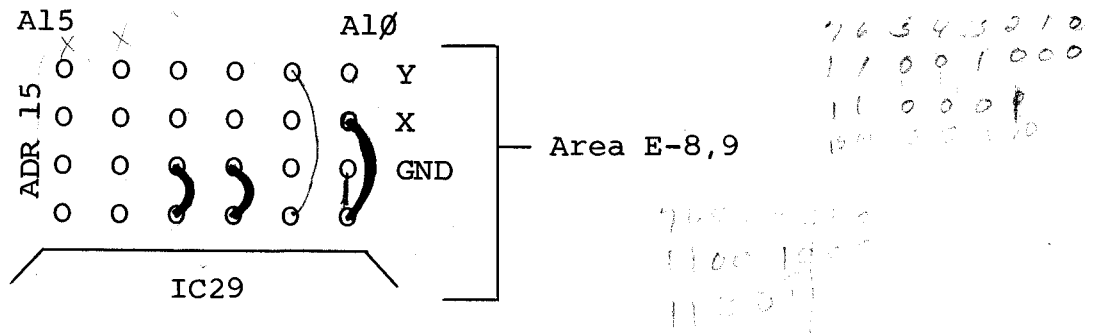


Figure 2-8. VDM-1 address jumpers, "standard" address assignments.

Should you wish to set your VDM-1 for other than the "standard" address assignments, proceed as follows: (Refer to Figure 2-9.)

- () 1. Write down port address in binary form (ADR0-7). ADR0 and 1 must always be zero.
- () 2. Write down six-bit memory page address in binary form (ADR10-15) directly below port address. Place bit 15 below bit 7, bit 14 below bit 6 and so forth.
- () 3. Connect address selection jumpers in Area E-8,9 according to the following rules:
 - a. If both bits in a column (bits 6 and 14, for example) are "1", no jumper is installed.

- b. If both bits in a column (bits 4 and 12, for example) are "Ø", install a jumper between the corresponding output of IC29 and ground (GND).
- c. If the port and memory page address bits in a column are "1" and "Ø" respectively (bits 7 and 15, for example), install a jumper between the corresponding output of IC29 and the Y row.
- d. If the port and memory address bits in a column are "Ø" and "1" respectively (bits 5 and 13, for example), install a jumper between the corresponding output of IC29 and the X row.

Figure 2-9 illustrates the preceding procedure assuming a port address of C4 (hex) and a memory page address of 6400 (hex).

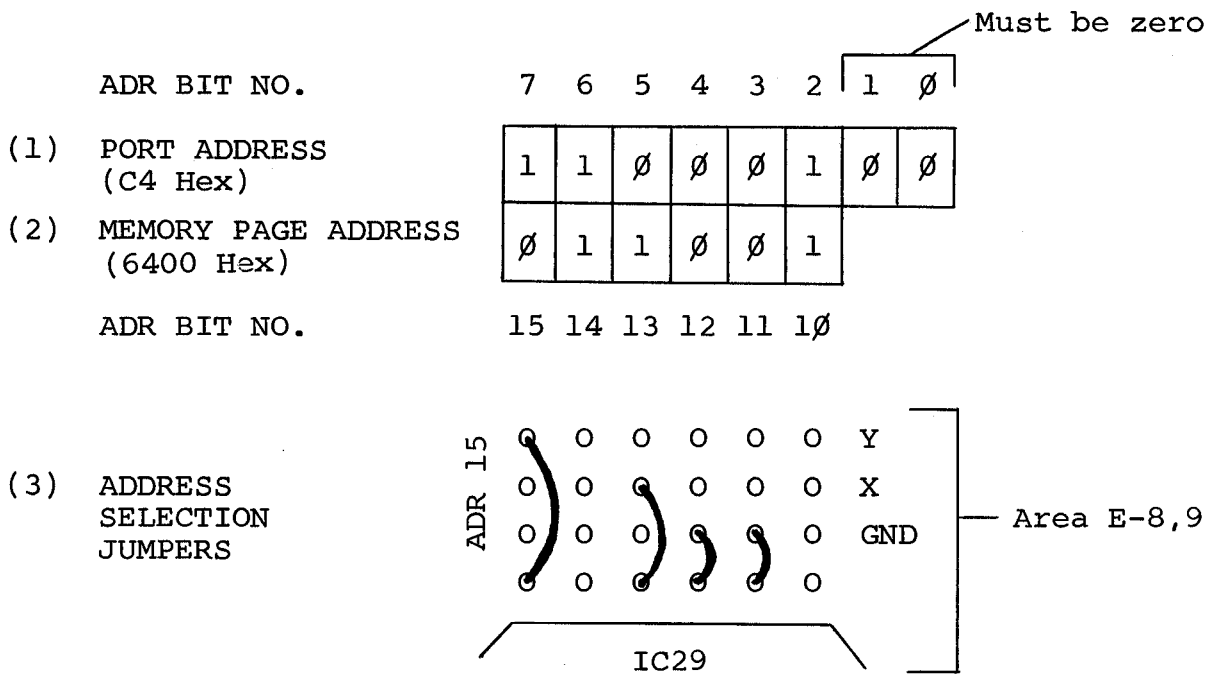


Figure 2-9. Procedure for setting VDM-1 for other than "standard" address assignments.

- () Step 24. Install ready jumper (J2) in Area C-10.
 - () If your Altair has been modified so that the ready driver on the display board is connected to Bus Pin 3, install a jumper between J2 and PRDY.
 - () If this modification has not been made, jumper J2 to XRDY.

() Step 25. Install 9-inch length of 8-conductor ribbon cable on front (component) side of board between J1 in Area A-10 and J1 in Area J,H-10.

() To insure correct terminal-to-terminal interconnection, make a fold midway between the cable ends to form an inverted V. Figure 2-10 clearly illustrates this technique.

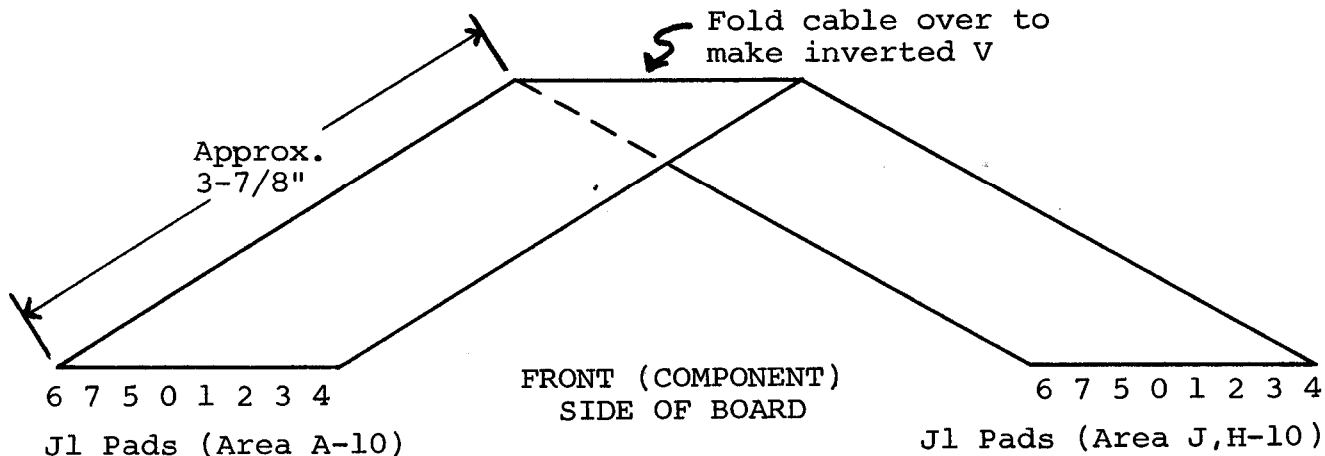


Figure 2-10. 8-conductor ribbon cable installation.

2.7 FINAL TEST PROCEDURES

2.7.1 VDM-1 DIP Switch Settings

- () Set Switches 2, 3, 5 and 6 to ON.
- () Set Switches 1 and 4 to OFF.

NOTE

With above settings, the VDM-1 is configured for normal video display (white on black background), non-blinking cursor, and unblanked control characters.

2.7.2 VDM-1 Installation

- () Install VDM-1 in computer and connect VDM-1 to video monitor. Turn monitor on. Hold STOP Switch on and turn computer on. (This keeps computer from coming on in run mode and insures a random display for scroll test.)

CAUTION

NEVER INSTALL OR REMOVE VDM-1 WITH COMPUTER POWER ON.

NOTE

Each time the VDM-1 is placed into operation, a random (garbled) display may appear on the screen. This is normal.

2.7.3 VDM-1 Status Initialization

- () Enter following program into computer memory beginning at address zero.

<u>HEX</u> <u>ADDRESS</u>	<u>OP CODE</u>	<u>LINE</u> <u>NO.</u>	<u>MNEMONIC</u>	
0000	3E 00	0005	MVI A, 00H	*LOAD ACCUMULATOR
0002	D3 C8	0010	OUT C8H	*OUTPUT TO VDM PORT
0004	C3 00 00	0015	JMP 0	*LOOP

- () Execute this program by turning on the RUN Switch and then flipping it quickly back to STOP. This program initializes the VDM-1 to display all sixteen lines.

2.7.4 Scroll and Status Change Test

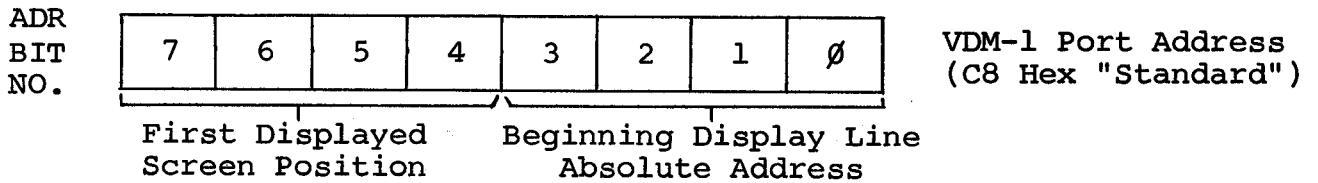
The purpose of this test is twofold: 1) it checks scrolling operation, and 2) it allows you to become familiar with the operation of the VDM-1 status control port.

- () Change first two bytes of program in Paragraph 2.7.3 to DB and FF hexadecimal. Also set the eight Sense Switches on your Altair or IMSAI front panel to OFF (zero). The program, if run continuously, will now output the Sense Switch data to the VDM-1 status control port.
- () With all eight Sense Switches OFF, a full 16 line by 64 character display (1024 characters) should appear on the screen. Note contents of first line in display. Call this line A.
- () As shown in Figure 2-11, Sense Switches 0 through 3 define the first display line in memory. Set Sense Switch 0 to ON (one). First line (A) in preceding display should shift to bottom of screen and the others should move up one line. Try various combinations of Sense Switches 0 through 3 and note where first line (A) appears in display. Once you are familiar with how Sense Switches 0 through 3 affect the display, set them to OFF.
- () As shown in Figure 2-11, Sense Switches 4 through 7 determine the first displayed screen position. Set these four switches to ON. Only the bottom line on the screen

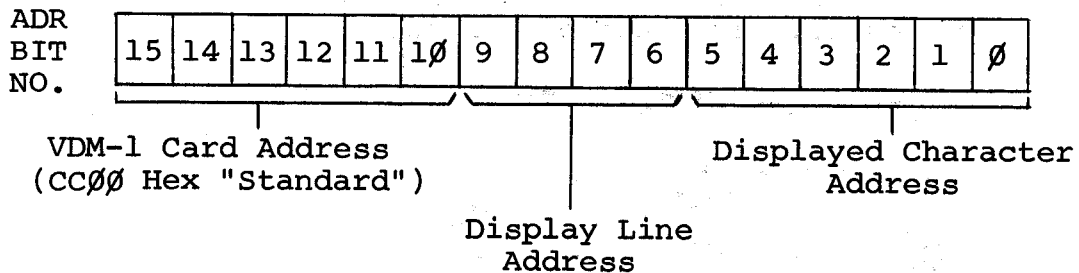
should be displayed. Try various combinations of Sense Switches 4 through 7. As each switch is changed, the display should appear to move up and down the screen with a black area above it. The first line on display, regardless of its vertical position on the screen, should remain the same.

- () After becoming familiar with how Sense Switches 4 through 7 affect the display, try different combinations of all the Sense Switches. Do this until you are familiar with the various ways in which "scrolling" can be performed.

VDM-1 Status Port Bit Functions



VDM-1 Address Allocation



NOTE: Character addresses always correspond to actual screen display position. Depending on status port control word, the line address may or may not correspond to the screen position.

Figure 2-11. VDM-1 status port bit functions and address allocation.

2.7.5 Hardware-Software Function Test

This test checks all VDM-1 hardware-software functions.

- () Enter following program into computer memory beginning at address zero.

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HEX ADDRESS	OP CODE	LINE NO.	MNEMONIC	
0000	3E 00	0010	MVI A,0	*INIT. SCREEN TO SHOW ALL 1024 CHARACTERS
0002	D3 C8	0020	OUT 0C8H	
0004	21 00 CC	0030	LXI H,0CC00H	*INIT. SCREEN POINTER
0007	06 00	0040	MVI B,0	
0009	05	0050	LOOP DCR B	*COUNT DOWN
000A	70	0060	MOV M,B	*PUT (B) ON SCREEN
000B	23	0070	INX H	*INCREMENT SCREEN POINTER
000C	7C	0080	MOV A,H	
000D	FE D0	0090	CPI 0D0H	*COMPARE POINTER WITH END OF SCREEN
000F	C2 09 00	0100	JNZ LOOP	
0012	3E 20	0110	MVI A,20H	*PUT "SPACE" IN (A)
0014	32 00 CC	0120	STA 0CC00H	*MOVE (A) TO SCREEN
0017	32 74 CC	0130	STA 0CC74H	*MOVE (A) TO SCREEN
001A	32 F2 CC	0140	STA 0CCF2H	*MOVE (A) TO SCREEN
001D	76	0150	HLT	*WE'RE DONE!

- () Set all eight Sense Switches on your Altair or IMSAI to OFF (zero) and turn RUN Switch on. The display shown in Figure 2-12 should appear on the screen. Three character positions in this display are blanked to provide reference points. They are as follows:

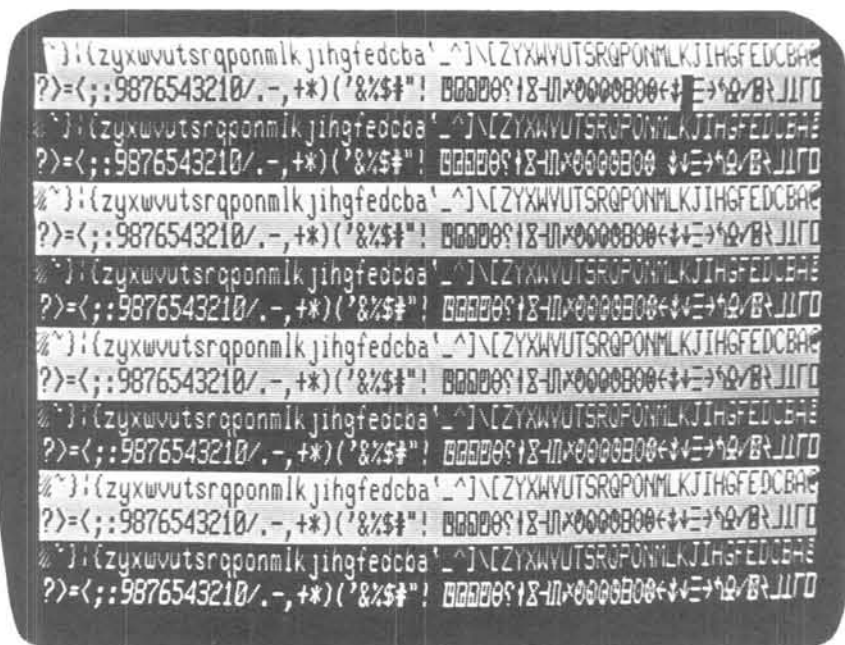


Figure 2-12. VDM-1 hardware-software test pattern (6574 character generator).

1. The first character in the first display line is blanked to identify the first line in the display.
 2. The VT control character (character position 53) in the second display line is blanked to permit a CR blanking test.
 3. The CR control character (character position 51) in the fourth display line is blanked to permit a VT blanking test.
- () Set DIP Switches 1 to ON and 2 to OFF. You should have the same display as shown in Figure 2-12.
- () Set DIP Switch 2 on VDM-1 to OFF and Switch 1 to ON in that order. A reversed video equivalent of the display shown in Figure 2-12 should appear on the screen. That is, the first two display lines will be white on black, the third and fourth lines will be black on white, etc.

NOTE

DIP Switches 1 and 2 should never be on at the same time.

- () Return DIP Switch 1 to OFF and Switch 2 to ON in that order.
- () Set DIP Switch 3 to OFF and Switch 4 to ON in that order. The entire display shown in Figure 2-12 should blink.

NOTE

DIP Switches 3 and 4 should never be on at the same time.

- () Return DIP Switch 4 to OFF and Switch 3 to ON in that order.
- () Set DIP Switch 5 to OFF. The VDM-1 is now configured to blank all control characters. Text blanking from CR to end of line and VT to end of screen is also enabled. The display shown in Figure 2-13 should appear on the screen.

As can be seen, the control characters (character positions 33 through 51) in the second display line are blanked out. Text blanking from, but not including, the CR control character (character position 51) to the end of line accounts for the remaining blanked portion of the line. VT blanking begins with the 54th character position in the fourth display line and blanks out the remainder of the screen.

- () Return DIP Switch 5 to ON and set Switch 6 to OFF. The VDM-1 is now configured to display control characters. Text blanking from CR to end of line and VT to end of screen is also enabled. The display shown in Figure 2-14 should appear on the screen.

As can be seen, the second line is blanked from, but not including, the CR control character to the end of the line. The CR control character as well as the other control characters preceding it are displayed. Again, VT blanking acts on the last 11 character positions in the fourth line as well as on all the following lines. The VT control character and the control characters preceding it in the fourth line are displayed.

- () Return DIP Switch 6 to ON.
- () At this point, if desired, you can put the VDM-1 through its scrolling paces by using the Sense Switches.

2.7.6 Character Generator Test

This test is provided for two purposes: 1) it allows you to check the character generator in the VDM-1 by displaying each character individually, and 2) it gives you an opportunity to become familiar with the ASCII code.

- () Set DIP Switches on VDM-1 as follows:

Switch No. 1 and 4: OFF
All other switches: ON

- () Enter following program into computer memory beginning at address zero.

<u>HEX ADDRESS</u>	<u>OP CODE</u>	<u>LINE NO.</u>	<u>MNEMONIC</u>	
0000	3E 00	0010	MVI A, 0	*CLEAR A
0002	D3 C8	0020	OUT 0C8H	*OUTPUT VDM PORT (STATUS)
0004	DB FF	0030	IN 0FFH	*INPUT SENSE SWITCHES
0006	47	0040	REDO MOV B, A	
0007	3E D0	0050	MVI A, 0D0H	
0009	21 00 CC	0060	LXI H, 0CC0H	*INITIALIZE SCREEN POINTER
000C	70	0070	MOVE MOV M, B	
000D	23	0080	INX H	*INCREMENT SCREEN POINTER
000E	BC	0090	CMP H	*COMPARE POINTER

(Program continued on Page II-28.)

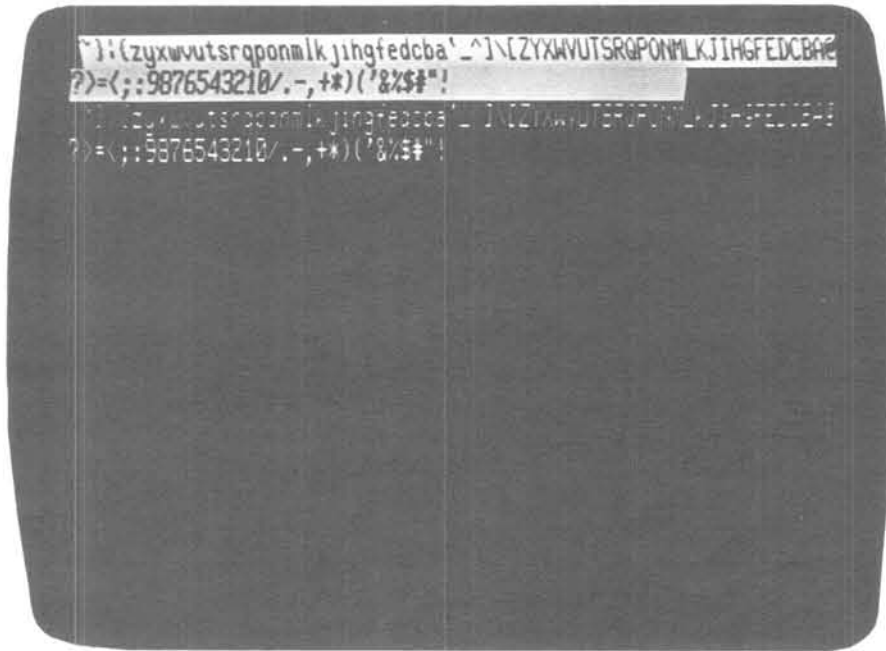


Figure 2-13. Control character and text (VT-CR) blanking (6574 character generator).

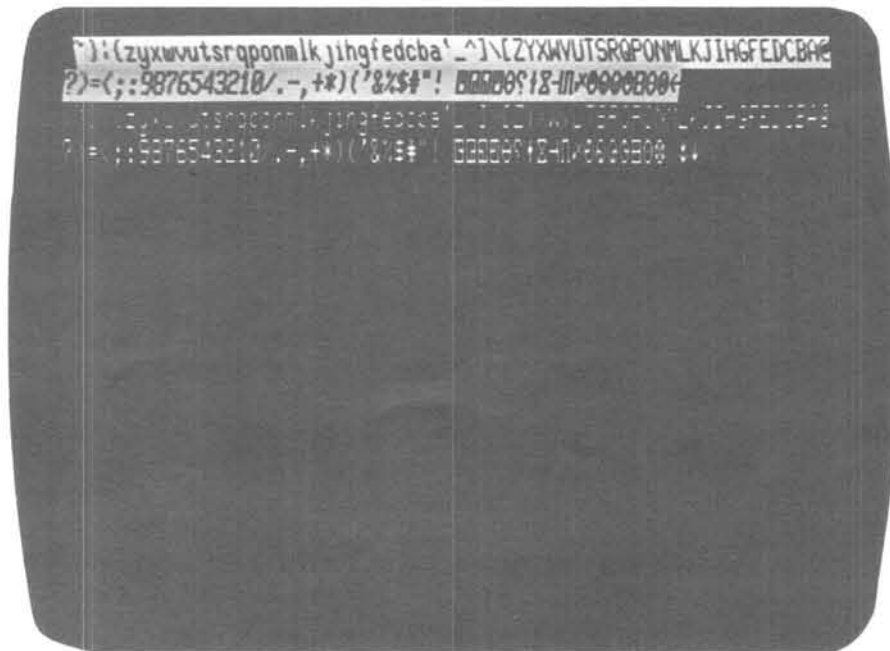


Figure 2-14. Text (VT-CR) blanking (6574 character generator).

<u>HEX ADDRESS</u>	<u>OP CODE</u>	<u>LINE NO.</u>	<u>MNEMONIC</u>	
000F	C2 0C 00	0100	JNZ MOVE	
0012	DB FF	0110	INPUT IN 0FFH	*INPUT SENSE SWITCHES
0014	B8	0120	CMP B	*COMPARE TO B
0015	CA 12 00	0130	JZ INPUT	
0018	C3 06 00	0140	JMP REDO	*LOOP

- () Turn RUN Switch on. The first seven Sense Switches (0 through 6) on your Altair or IMSAI may now be used to address each character in the VDM-1 character generator, for their setting is the binary representation of the addressed ASCII character.

NOTE

The position of the eighth Sense Switch (7) determines whether the cursor is on or off.

- () Using Sense Switches 0 through 6, individually address each of the 128 ASCII characters. (Refer to Figures 3-1A, B and C in Section III for ASCII code.)

For example, setting Sense Switches 0 and 6 to "1" and Sense Switches 1 through 5 to "0" will address the character "A" (ASCII code 10000001). A full screen (16 lines by 64 characters) of A's should appear on the screen.

Setting Sense Switches 0, 2, 4 and 5 to "1" and Sense Switches 1, 3 and 6 to "0" will cause a 5 (ASCII code 0110101) to be displayed.

2.7.7 Modification for 50 Hz. Operation

The European television standard defines a raster of 625 lines at a field rate of 50 Hz. The horizontal rate of the U.S. standard, 15,750 Hz, is maintained. Only the number of scan lines on the screen is increased.

The VDM-1 may be modified for the 50 Hz. standard by following the additional steps below. The effect of the modification is to increase the modulus of the counter IC 8 to eight during the period of VDISP. This results in four extra character lines (52 scan lines) between the bottom and top of the display area, for a total of 312 scan lines per field and 624 scan lines per frame.

The field rate should be close enough to 50 Hz. to reduce any swim effects to less than 0.1 Hz. Some difficulty may be encountered in obtaining centering of the display within the frame. This is because the stand-off time to VSYNC from the bottom of the display is unchanged

from the 60 Hz. standard. If objectionable, increase the value of resistor R34 which is in series with the VPOS control.

To convert for 50 Hz., perform these steps:

- () Locate IC8 on the component side legend. Find pin 5 of this IC on the solder (back) side. Cut the trace connecting pin 5 to pin 6, using a sharp knife point or scribe, so that there is no continuity between these pins.
- () Using a one-eighth inch long piece of small bare wire, such as a resistor lead clipping, solder a jumper between pins 5 and 4 (ground) also on IC8.

2.7.8 Modification for Vectored Interrupt Systems.

If you intend to use the VDM-1 in a host computer which uses a vectored interrupt system, perform the following four additional steps. These steps result in a modification which prevents the VDM-1 from responding inadvertently during SINTA cycles. The modification is necessary even if no connection is made on the VDM-1 to the VI (vectored interrupt) bus pins. Refer to the assembly drawing in Section IV of this manual.

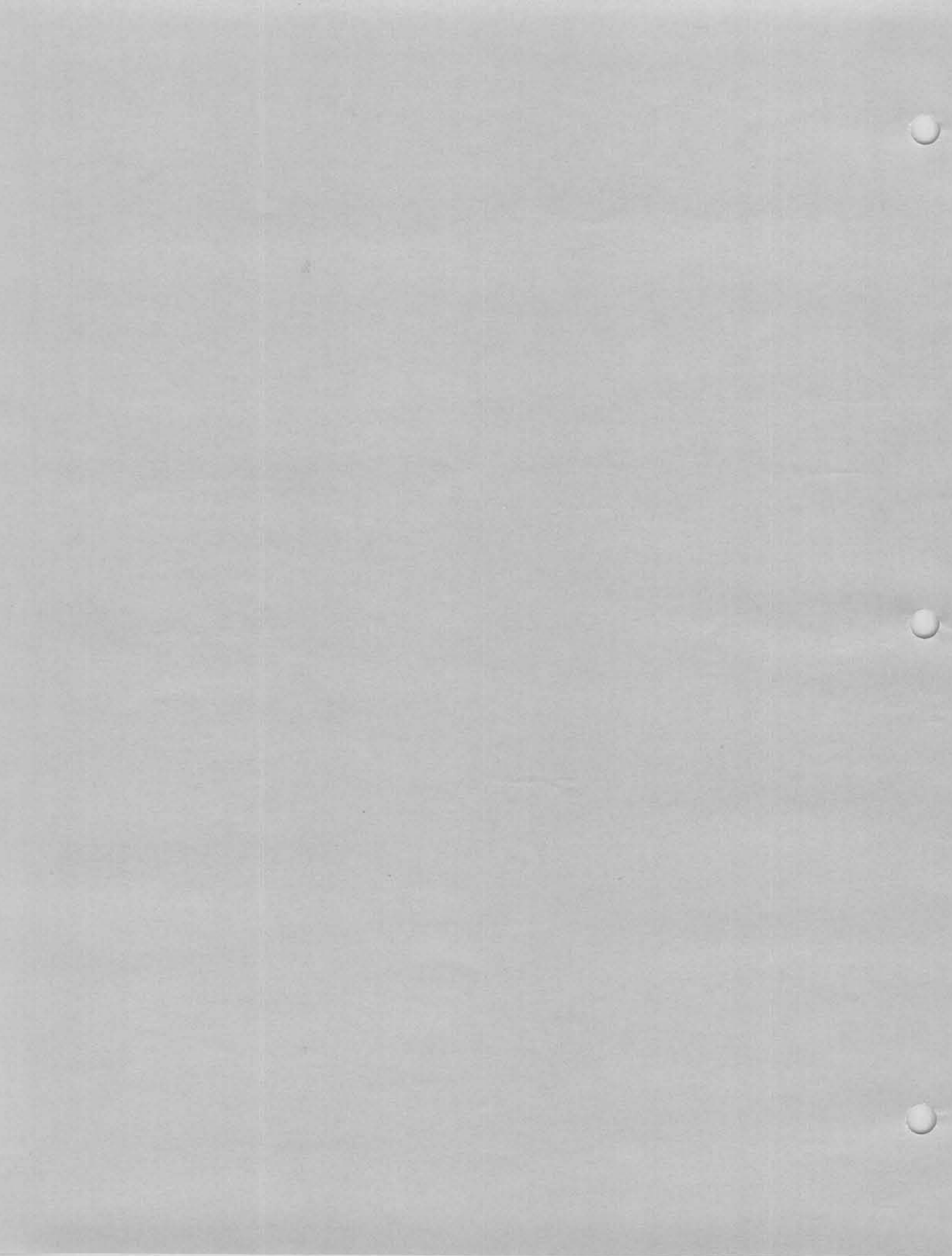
- () Near IC 18, find the two pads marked A1 and PDBIN on the assembly drawing. (Note: on some circuit board legends, the labels for these pads is shown reversed. The assembly drawing and schematic are correct.) Find the trace which connects these pads on the solder (back) side of the board, and cut this trace with a sharp knife or scribe point, so that there is no continuity.
- () Using the same procedure, cut the "V"-shaped trace near IC35 at the point shown by the arrow on the assembly drawing.
- () Using the 24-gauge wire supplied with this kit, install a jumper wire between the pad marked SMEMR on the assembly drawing, which is connected to pin 47 of the S100 connector, and the pad marked A1 near IC18. Solder the jumper at both ends and trim the leads.
- () Install a similar jumper wire between the pad marked PDBIN near IC18 and the pad marked A2 near IC35.

SECTION III

THEORY OF OPERATION

VDM-1 VIDEO DISPLAY MODULE





3.1 THEORY OF OPERATION

The VDM-1 can be broken down into eight functional sections: timing, synchronization and blanking, memory, character generation, cursor, video, scroll and computer interface. For the following discussions, refer to the VDM-1 schematic diagram in Section IV.

3.1.1 Timing

Two inverter gates (IC19)--connected as a high-gain non-inverting amplifier--and crystal Y1 form a crystal-controlled 13.318 MHz DOT CLOCK. This frequency defines the period of one dot in a character display matrix. DOT CLOCK is applied to a binary counter (IC20) which is preset to count seven to divide DOT CLOCK by nine. Two 1.5 MHz outputs are supplied by IC20: LOAD CLOCK and CHARACTER CLOCK. The former is a low-active signal of one DOT CLOCK duration; the latter is a square wave that is high and low for four and five DOT CLOCK periods respectively. Both the LOAD and CHARACTER CLOCK low-to-high transitions occur synchronously to the same DOT CLOCK transition.

CHARACTER CLOCK, which defines the period for one character, is counted down in IC22 and 21, both of which are 4-bit binary counters. IC22 counts from 0 to 15 and provides a carry output to enable IC21. IC21 is preset to count 3 and reset at count 9 by the output of NAND gate IC15. Thus IC21 cycles through six counts, with each count representing 16 CHARACTER CLOCK pulses.

Reset of IC21 defines the lefthand margin of the display, counts 4 through 7 define successive groups of 16 character positions, count 8 defines the righthand display margin, and count 9 defines the first CHARACTER CLOCK in the lefthand margin of the display.

The outputs of IC22 provide the four lower address bits of the character position on display. The two least significant outputs from IC21 supply the two high order address bits. Q_D (pin 11) and Q_C (pin 12) of IC21 are SCAN ADVANCE and HDISP (horizontal display) respectively. The former is used to generate horizontal synchronization signals, and the latter defines the start of a horizontal scan line.

On count 9 of IC21, the output of NAND gate IC15 also enables IC2, the scan divider. IC2 counts the horizontal scan lines that make up a row of characters and supplies the line number to the character generator ROM, IC4. IC2 is preset to count 15 for the first scan line in the row. With this line count, the character generator provides a blank spacer line between the preceding and current character rows. IC2 then counts from 0 to 11 lines. At the end of the 11th count, a decoder comprised of IC14 and 7 supplies a load pulse to IC2 which resets it to count 15.

This load pulse, after inversion, becomes the OVERFLOW LINE signal. OVERFLOW LINE enables the character row divider, IC8. IC8 resets itself with its carry output through IC9, with the reset count being determined by the state of IC16, the vertical display (VDISP) flip-flop. If IC16 is cleared, IC8 is reset to count 0; if IC16 is set, IC8 is reset to count 12. Thus IC8 counts four or 16 character rows when IC16 is set or cleared respectively during load. The total of 20 character rows (260 scan lines) represents a full field on the display raster.

3.1.2 Synchronization and Blanking

Horizontal and vertical synchronization signals are generated by two one-shot multivibrators consisting of three two-input NOR gates in IC30 and two inverters in IC25. Horizontal sync is triggered by SCAN ADVANCE and vertical sync by VDISP. Both circuits generate fixed-length sync pulses with adjustable starting times. C27 and C25 determine the length of the horizontal and vertical sync pulses respectively. The starting times with respect to triggering, are variable with R50 (HORIZ) and R33 (VERT) to provide continuous adjustment of the display position on the raster. An exclusive OR-gate in IC12 combines the two sync pulses into a composite sync (COMP SYNC) signal. Note that the use of the exclusive OR inverts the horizontal sync pulses when the vertical sync pulse appears. Since vertical sync information is extracted in the monitor by an integrating, or averaging, process, this technique maintains horizontal synchronization during the vertical sync period.

Two types of blanking are available in the VDM-1: control character blanking and video blanking. The former blanks control characters and causes cursor information to be displayed in their place. Video blanking forces portions of the video display to a white or black level, depending on whether normal or reverse video is selected with SW1 and SW2. (See Paragraph 3.2.)

Control character blanking, switch selectable with SW5 and SW6, is accomplished with one gate in IC14 and one gate in IC15. When a control character is present in the data latch (IC5 and 6), IC14 is satisfied. Assuming the blanking option is selected, the output of IC14 is gated with LOAD CLOCK in IC15 to clear the video parallel-to-serial converter, IC3. IC3 then loads all zeros instead of the character.

Video blanking is initiated by the PRE BLANK, POST BLANK, or BLANK inputs to IC7, a four-input NAND gate. The fourth input, the video output of the cursor circuit, is blanked when any of the three blanking inputs is active.

The PRE BLANK input provides "window shade" blanking which is analogous to pulling a window shade down from the top of the display. PRE BLANK is generated in one half of IC13. IC13 is reset active during V SYNC and set inactive during START DISPLAY. The

latter is generated by the scrolling circuitry and defines the character row for which the window shade ends. START DISPLAY may begin with any character row from zero through 14.

POST BLANK blanks all character rows following the row in which a VT control character appears if the CR/VT option is selected by SW5 or SW6 (see Paragraph 3.2). POST BLANK is generated in one flip-flop in IC16. This flip-flop is set inactive during V SYNC and reset active during OVERFLOW LINE if the VT flip-flop is set to indicate a VT control character.

The remaining video blanking function concerns the BLANK output from one section of IC17. This signal is a composite of HDISP, VDISP and the two control characters VT and CR. Since the blanking effects of these signals are character-position critical, timing is also critical. Thus, two D-type flip-flops in IC17 are used to insure synchronization.

The first flip-flop is active (low) only when HDISP and VDISP are high at IC15. Thus, the output of this flip-flop is active during the time a displayable character is latched into the data latch (IC5 and 6). The output of the first flip-flop is applied to one input of a three-input gate in IC9. IC9 is active (low) only when all of its inputs are high. A low input to IC9 will therefore override any other high inputs.

Outputs from the VT and CR flip-flops (IC10) are the other two inputs to IC9. VT and CR are active (low) from the first LOAD CLOCK during which either character is present in the data latch. This assumes the CR/VT option is enabled. Both the VT and CR flip-flops are set inactive during SCAN ENABLE. Thus, the blanking effect of VT and CR lasts from the character following VT or CR to the end of the character row.

The VT and CR blanking signals are generated by IC11, IC10, IC16 and their associated circuitry. In order to enable an output from IC11, the inputs to pins 6, 4 and 5 must be active. If pin 6 is grounded with SW5 and 6, the output of IC14 is disabled to de-select the VT/CR option. Otherwise pin 6 will be active (high) when IC14 decodes a control character in the output of the data latch (bits 5 and 6 are zero). Pin 4 is active (low) when IC9 decodes a control character (bit 3 zero and bit 4 high) when PRE BLANK is inactive (high). Pin 5 is active when DISPLAY is active (low). DISPLAY is low during all video display times. With IC11 enabled, it supplies outputs when the three low-order bits from the data latch reflect the VT or CR ASCII code, 0001011 and 0001101 respectively.

The CR output of IC11 (Pin 10) resets the CR flip-flop (IC10) active at the end of the CR control character. VT flip-flop (IC10) is likewise set active by the VT output of IC11 (pin 12). Both sections in IC10 are set inactive by LOAD CLOCK during SCAN ENABLE.

CR and VT blanking are consequently effective from the start of the character position following the control character to the end of the character row. When the VT flip-flop is set inactive at the end of the last scan line in the row, the POST BLANK flip-flop (IC16) is also reset active since OVERFLOW LINE becomes active. Thus, VT initiated blanking continues to the end of the screen.

3.1.3 Screen Memory

Screen memory in the VDM-1 consists of eight 1 x 1024 bit RAM (random access memory) chips, IC41 through IC48. All chips are held enabled. Memory addressing is provided through a two-to-one multiplexer (IC23, 24 and 28) which selects one of two address sources: external address from the computer or internal character address from IC21, 22, 26 and 27. The last two ICs make up the scrolling counter. Normally the internal address is multiplexed to memory. When the computer requests access, the multiplexer switches to the external address lines, ADR0 through 9. The write enable (WE) input to IC41 through 48 are active only during external addressing when WRITE at pin 8 of IC18 is low.

3.1.4 Character Generation

Two latches, IC5 and 6, latch data from the screen memory. The output from IC46 is inverted before being applied to pin 12 of IC5, and the complement (pin 11) of the Q_C output is used in addressing the character generator ROM, IC4. This enables the data latch to present a SPACE code to the ROM when it is cleared. Bit 8 from the latch is used for the cursor and does not enter the ROM.

IC4 has seven character address inputs, four row select inputs and seven data outputs. It is programmed to generate seven bits (dots) of character information for the selected scan line of the character row. The complete pattern of IC4 is shown in Figure 3-1A, B and C.

The ROM output is converted from parallel to serial form in IC3, a shift register, and applied to one gate in IC12. This gate is the first component in the video circuitry.

3.1.5 Cursor Circuit

A blink oscillator (two inverter sections in IC25), a latch (one section in IC17) and their associated components comprise the cursor circuit. The blink oscillator runs continuously at a rate set by R21 and C20. Its output has a nominal 0.5 sec period. If the blink option is selected with SW4 (see Paragraph 3.2), the blink signal is applied to one input of a gate in IC14. The other input to this gate is provided by the cursor latch, one section in IC17. If bit 7 out of the data latch is high, IC17 sets for the time the ROM is active on the character and remains set during the period when video data is shifted out of IC3. The output of IC17

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A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
A6..A4		D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0
000	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
001	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
010	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
011	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
100	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
101	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
110	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
111	RO	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	:	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
	RB	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]

▀ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

Figure 3-1A. MCM6574 pattern.

is gated high through IC14 when BLINK is low. (BLINK) is held low when the blink option is not selected.) The output of IC14 is in turn gated with the video output of IC3 in IC12, an exclusive OR gate. IC12 thus inverts the video if the output of IC14 is high, and no inversion takes place if the output of IC14 is low.

3.1.6 Video Circuit

The video signal, including the cursor, is gated to SW1 and 2 by IC7 in the absence of any blanking signals at the other three inputs to IC7. With SW2 closed, video and COMP SYNC are applied through two inverters in IC1 to a resistive mixer, R1 through R3. This mixer has a 75-ohm output impedance. The two signals are mixed to meet EIA composite video signal requirements and coupled to the output by C1. If only SW1 is closed, another inverter in IC1 inverts the video signal to produce a reverse (black on white) display.

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SECTION III

A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
A6..A4		D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0
000	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
001	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
010	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
011	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
100	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
101	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
110	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
111	RO	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	..	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000
	RB	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000	000000

▀ - Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

Figure 3-1B. MCM6575 pattern.

3.1.7 Scroll Circuit

The scroll circuit is made up of IC26, 27, 31 and 32 and their associated circuitry. IC26 and 27 are up/down counters that are preset by the outputs of latches IC31 and 32. IC31 and 32 latch the character row information specified on DI0 through 7. IC26 is preset during VDISP, the time from the bottom of the displayed text to the top of the next vertical display period. IC26 is held at the preset number during this period, and counting is disabled by OVERFLOW LINE. When the character row divider (IC8) advances at the end of the first character row in the display, IC26 is enabled to count down. IC26 provides a low on its TC output whenever the counter is at count zero. This TC active output is inverted in IC19 to supply the START DISPLAY signal (active high). PRE BLANK blanks the display until START DISPLAY goes active. START DISPLAY goes inactive when IC26 counts below zero during OVERFLOW LINE at the end of the character row.

During the active time of START DISPLAY, IC27 is loaded with the contents of IC32. IC27 is enabled, when OVERFLOW LINE is low, to count up from the start of the end of the first displayed character row. IC27 continues to count with the end of each following character row.

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SECTION III

A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
A6..A4		D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0	D6...D0
000	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
001	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
010	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
011	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
100	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
101	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
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	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
110	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
111	RO	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	...	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣
	RB	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣	▣▣▣▣

▣ = Shifted character The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

Figure 3-1C. MCM6576 pattern.

Since IC27 reloads to its preset value at the line for which the window shade ends, the display may be scrolled up or down by incrementing or decrementing the row number. Incrementing or decrementing the number in IC32 varies the window shade duration. Doing the same thing to the number in IC31, in the absence of window shade blanking, causes the display to scroll.

3.1.8 Computer Interface

IC29 compares the address bits, ADR10 through ADR15 with two possible binary comparison numbers. These numbers are set with the X, Y and GND (ground) jumper arrangement (ADDRESS SELECT). One comparison number, which relates to the page number to which the screen memory responds, is generated when there is no input on SINP or SOUT. The other is generated when either of these inputs is present and represents the six high-order bits of the I/O port address to which the status port responds. Note that the circuit requires that the two low-order bits of the I/O port address always be zero.

During PSYNC, when Ø2 is low, IC29 compares its inputs and the two comparison numbers. An internal latch in IC29 retains the

state of the comparison when its enable input goes high. The output from IC29 drives several circuits.

1. It enables the XRDY driver, IC38.
2. It enables a section in IC37 (low) and IC40 (high).

If SINP and SOUT are low, the other input to IC37 satisfies the gate to generate MEM SELECT (memory select). Should either be high and the two low-order I/O address bits (ADR8 and 9) are low, IC40 generates I/O SELECT.

An active I/O SELECT enables another gate in IC37 and a gate in IC35 to respond to PWR and PDBIN respectively. PWR supplies LOAD STATUS to IC31 and 32. These two latches will thus retain the state of the DO bus as the scrolling parameters. PDBIN generates STATUS OUT to enable IC39 (pin 15) to place the status bit on DIØ.

MEM SELECT performs three functions: 1) it immediately switches the address multiplexer (IC23, 24 and 28) to supply external addressing to the screen memory, 2) it enables one section of IC13, and 3) it enables one section in IC17.

The input to, and Q output of, IC13 are gated during the time preceding the next Ø2 high-to-low transition to IC38, the XRDY driver. Transmission through IC38 causes a wait state in the computer. This wait period allows the screen memory addresses to settle and allows adequate time for the memory to come ready for data input or output.

A MEM GO (memory go) signal from IC13, which occurs with the second Ø2 in the instruction cycle, indicates enough time has elapsed since addressing for the screen memory to transfer data. During the wait period, PDBIN or MWRITE hold in their active state (high). Hence, Either WRITE is given to the screen memory or DATA OUT enables the DI bus drivers as appropriate.

The output of IC17 prevents any possible interference with the display when the screen memory address is changed. When the address is changed, the display is overridden, and spurious data at the memory outputs can interfere with the display. When IC17 is set, it causes the data latch to reset to a SPACE code. The SPACE code remains until the next character clock following removal of MEM SELECT. As a result, a short (but not critical) line segment in the display is lost.

LOAD STATUS from IC37 also triggers a one-shot timer consisting of one section in IC30, one in IC25, and Q1. The buffered output of this one-shot is STATUS. STATUS goes high when the one-shot is triggered and remains high for 0.25 to 0.5 second. The computer, when performing an output instruction from the VDM-1 port,

can thus test the timer status by looking for a high on DI \emptyset . This allows a slow scroll rate without requiring complex timing routines in the CPU.

STATUS is also connected to an unused 7406 inverter section in IC1. The output of this inverter can be jumpered to any of the vector interrupt (VI) pins. In future systems with vectored interrupt, this output will eliminate the need to continuously test the timer status.

The scan advance signal from the group divider counter is output to bit 1 (DI-1) during the port input instruction. A "1" on this bit indicates that the display is just to the right of the right-hand margin. This feature is used in software which presents a flicker-free display.

3.2 SWITCH SELECTABLE OPTIONS

The VDM-1 has several switch-selectable operating features. These are: normal and reverse video display, blinking and non-blinking cursor, text blanking, and control character blanking. These options are selected by SW1 through SW6 in the DIP Switch located in Area B-1,2 on the circuit board.

SW1 and 2 control the video display, SW3 and 4 control cursor, and SW5 and 6 control the text and control character blanking features. The role that each switch serves in configuring the VDM-1 circuitry for the various options can be readily determined by reviewing the schematic diagram in Section IV of this manual. Table 3-1 defines the options that are available with SW1 through 6. (Table 3-1 will be found on Page III-10.)

PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

SECTION III

Table 3-1. DIP Switch States vs Options.

SWITCHES				OPTION
No.	State	No.	State	
1	OFF	2	OFF	No display.
1	OFF	2	ON	Normal video (white on black background).
1	ON	2	OFF	Reverse video (black on white background).
1	ON	2	ON	N O T A L L O W E D.
3	OFF	4	OFF	All cursors suppressed.
3	OFF	4	ON	Blinking cursor.
3	ON	4	OFF	Non-blinking cursor.
3	ON	4	ON	N O T A L L O W E D.
5	OFF	6	OFF	All characters suppressed. Only cursor blocks are displayed. Text blanking from CR to end of line and VT to end of screen enabled.
5	OFF	6	ON	Control characters blanked. Text blanking from CR to end of line and VT to end of screen enabled.
5	ON	6	OFF	Control characters are displayable. Text blanking from CR to end of line and VT to end of screen enabled.
5	ON	6	ON	Control characters are displayable. Text blanking from CR to end of line and VT to end of screen disabled.

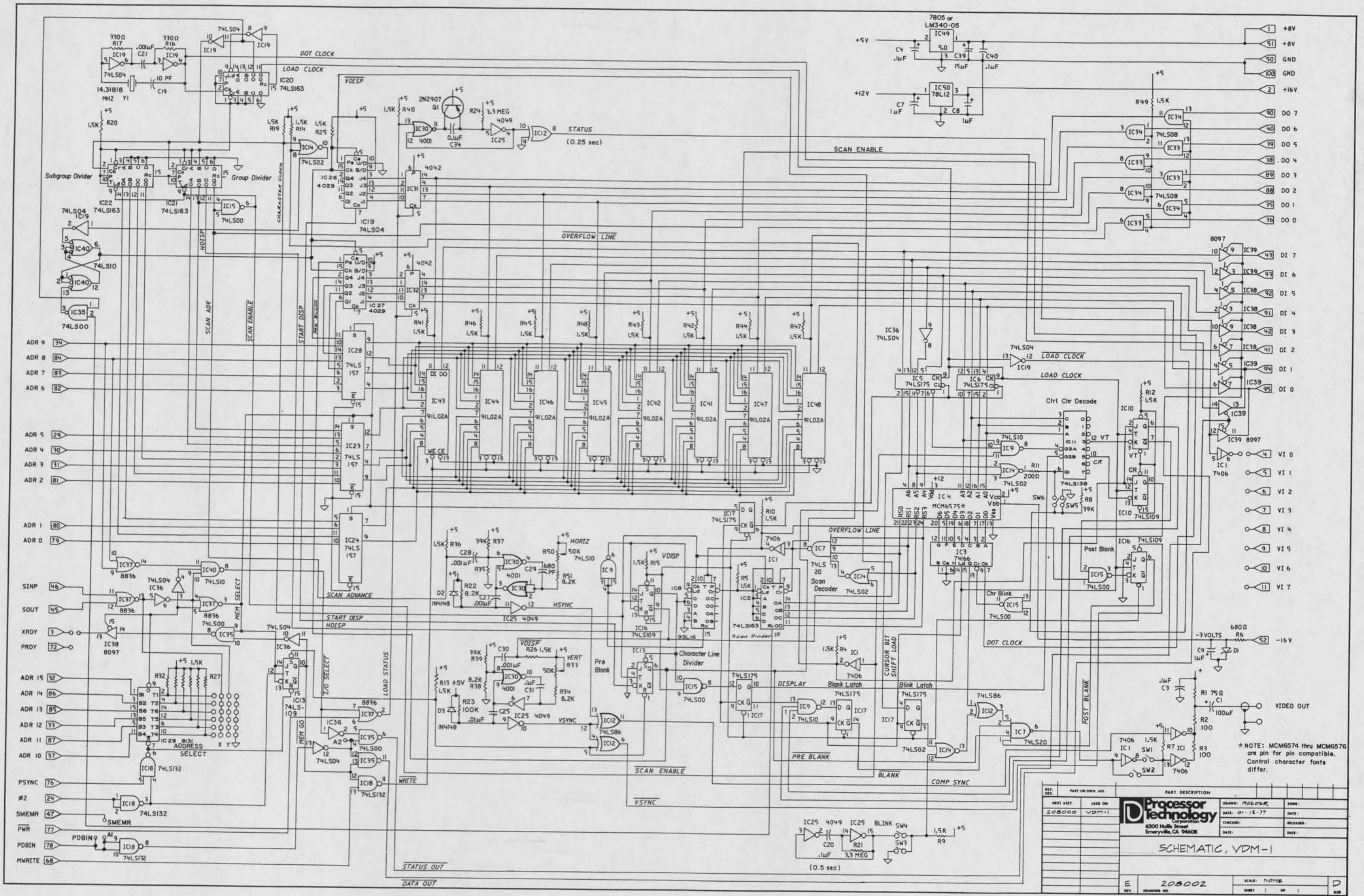
SECTION IV

DRAWINGS

VDM-1 VIDEO DISPLAY MODULE







* NOTE: MCM6574 thru MCM6576 are pin for pin compatible. Control character fonts differ.

REV	DESCRIPTION	DATE	BY
1	SCHEMATIC, VDM-1	01-15-77	

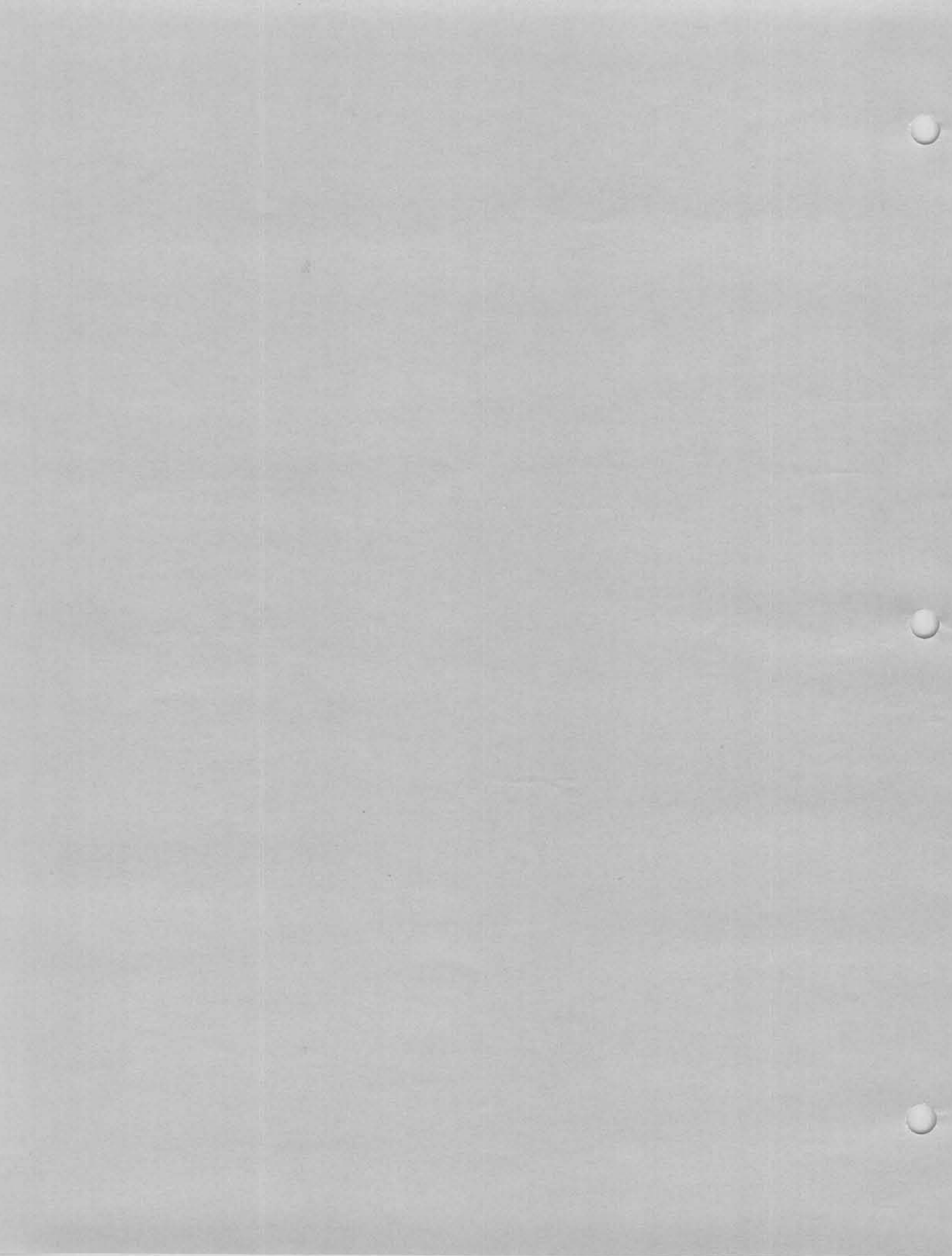
PART OR DWS. NO. 208000	USED ON VDM-1	PART DESCRIPTION Processor Technology Corporation 4200 Hollis Street Emeryville, CA 94608	DRAWN: GOS/GPK DATE: 01-15-77 CHECKED: DATE:	INCH: DATE: RELEASED: DATE:
----------------------------	------------------	---	---	--------------------------------------

E REV: 208002 DRAWING NO.	SCALE: NONE	SHEET 1 OF 1
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APPENDICES

VDM-1 VIDEO DISPLAY MODULE





APPENDIX I

STATEMENT OF WARRANTY





STATEMENT of WARRANTY

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by Processor Technology Corporation are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 6 months following the date of purchase. The defective part must be returned postpaid to Processor Technology Corporation within the warranty period.

Any malfunctioning module, purchased as a kit and returned to Processor Technology within the warranty period, which in the judgement of P.T. Corp. has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, with a minimal charge to cover postage and handling.

Any modules purchased as a kit and returned to P.T. Corp. which in the judgement of P.T. Corp. are not covered by the above conditions will be repaired and returned at a cost commensurate with the work required. In no case will this charge exceed \$20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least 6 months following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same 6 month period. All warranted factory assembled units returned to P.T. Corp. postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.



APPENDIX II

8080 OPERATING CODE



JUMP	CALL	RETURN	RESTART	ROTATE†	MOVE (cont)	ACCUMULATOR*	CONSTANT DEFINITION
C3 JMP	CD CALL	C9 RET	C7 RST 0	07 RLC	58 MOV E,B	80 ADD B	B
C2 JNZ	C4 CNZ	C0 RNZ	CF RST 1	0F RRC	59 MOV E,C	81 ADD C	XRA C
CA JZ	C8 CZ	C8 RZ	D7 RST 2	17 RAL	5A MOV E,D	82 ADD D	XRA D
D2 JNC	D4 CNC	D0 RNC	DF RST 3	1F RAR	5B MOV E,E	83 ADD E	XRA E
DA JC	DC CC	D8 RC	E7 RST 4	CONTROL	5C MOV E,H	84 ADD H	XRA H
E2 JPO	E4 CPO	E0 RPO	EF RST 5	00 NOP	5D MOV E,L	85 ADD L	XRA L
EA JPE	EC CPE	E8 RPE	F7 RST 6	76 HLT	5E MOV E,M	86 ADD M	XRA M
F2 JP	F4 CP	F0 RP	FF RST 7	F3 DI	5F MOV E,A	87 ADD A	XRA A
FA JM	FC CM	F8 RM		FB EI			
E9 PCHL							

MOVE IMMEDIATE	Acc IMMEDIATE*	LOAD IMMEDIATE	STACK OPS	MOVE	OPERATORS
06 MVI B, B	C6 ADI B, D16	01 LXI B, D16	C5 PUSH B	40 MOV B,B	B8 CMP B
0E MVI C, C	CE ACI D, D16	11 LXI D, D16	D5 PUSH D	41 MOV B,C	B9 CMP C
16 MVI D, D	D6 SUI H, H	21 LXI H, H	E5 PUSH H	42 MOV B,D	BA CMP D
1E MVI E, E	DE SBI SP, SP	31 LXI SP, SP	F5 PUSH PSW	43 MOV B,E	BB CMP E
26 MVI H, H	E6 ANI D8			44 MOV B,H	BC CMP H
2E MVI L, L	EE XRI D8			45 MOV B,L	BD CMP L
36 MVI M, M	F6 ORI D8			46 MOV B,M	BE CMP M
3E MVI A, A	FE CPI D8			47 MOV B,A	BF CMP A

INCREMENT**	DECREMENT**	LOAD/STORE	SPECIALS	PSEUDO INSTRUCTION	STANDARD SETS
04 INR B	05 DCR B	0A LDAX B	EB XCHG	ORG Adr	A SET 7
0C INR C	0D DCR C	1A LDAX D	27 DAA*	END	B SET 0
14 INR D	15 DCR D	2A LHL Adr	2F CMA	EQU D16	C SET 1
1C INR E	1D DCR E	3A LDA Adr	37 STC†		D SET 2
24 INR H	25 DCR H		3F CMC†	DS D16	E SET 3
2C INR L	2D DCR L			DB D8	H SET 4
34 INR M	35 DCR M			DW D16	L SET 5
3C INR A	3D DCR A				M SET 6
03 INX B	0B DCX B	02 STAX B			SP SET 6
13 INX D	1B DCX D	12 STAX D			PSW SET 6
23 INX H	2B DCX H	22 SHLD Adr			
33 INX SP	3B DCX SP	32 STA Adr			

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.
 D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.
 * = all Flags (C,Z,S,P) affected
 † = only CARRY affected
 ** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

APPENDIX III

LOADING DIP DEVICES

and

SOLDERING TIPS



LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

- (1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.
- (2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.
- (3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.
- (4) Press the device straight down until it seats on the points where the pins widen.
- (5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

- (1) Use a low-wattage iron — 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.
- (2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.
- (3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

- (4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).
- (5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.
- (6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.
- (7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

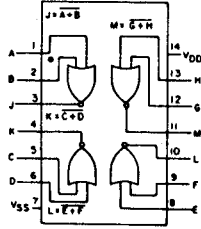


APPENDIX IV

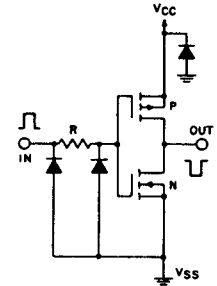
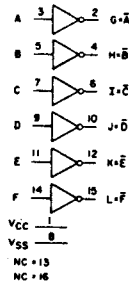
INTEGRATED CIRCUIT PIN CONFIGURATIONS



4001

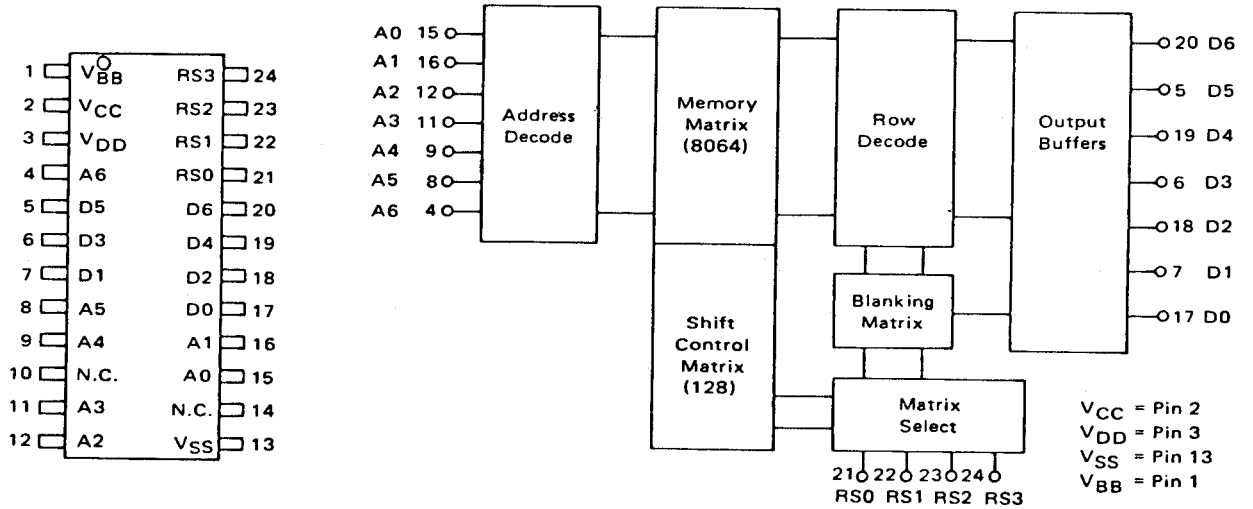


4049



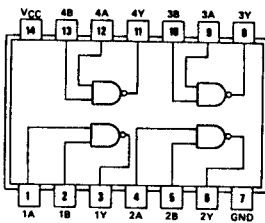
1 of 6 identical units;

MCM6574, 6575 or 6576



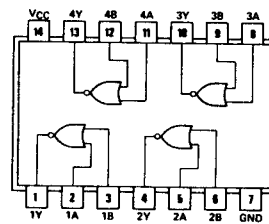
See Section III for complete patterns of these generators.

74LS00



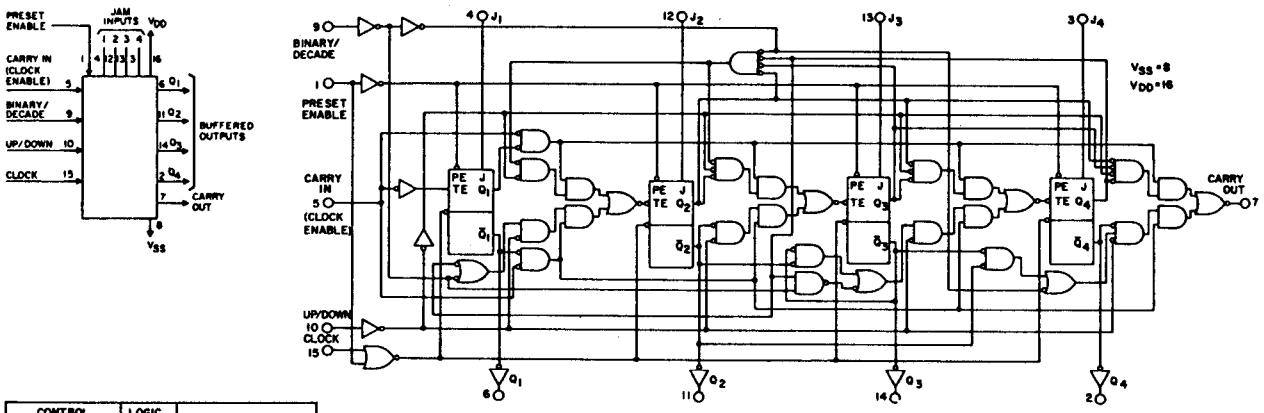
positive logic:
Y = AB

74LS02

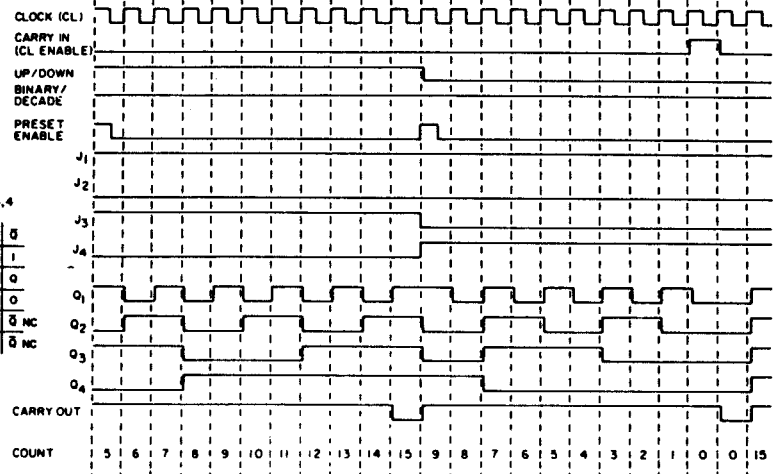


positive logic:
Y = A+B

4029



CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1	BINARY COUNT
BIN/DEC. (B/D)	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
UP/DOWN (U/D)	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
PRESET ENABLE (PE)	0	NO JAM
CARRY IN (CZ) (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
CARRY IN (CZ) (CLOCK ENABLE)	0	ADVANCE COUNTER AT POS. CLOCK TRANSITION



TRUTH TABLE FOR F-F No.1

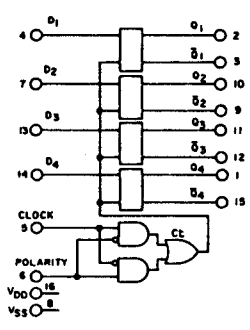
CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
∅	1	1	X	Q	Q̄
X	X	0	1	1	0
∅	0	1	X	Q̄	Q
∅	X	1	X	Q̄	NC

TRUTH TABLE FOR F-F'S 2,3,4

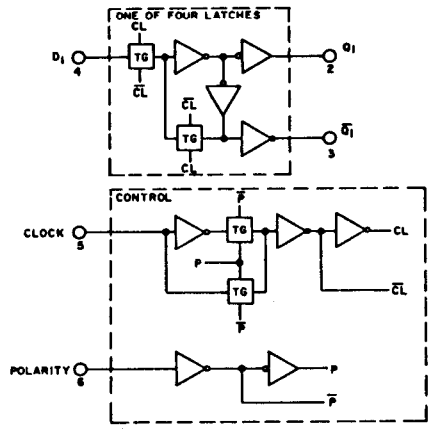
CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
∅	1	1	X	Q	Q̄
X	X	0	1	1	0
∅	0	1	X	Q̄	Q
∅	X	1	X	Q̄	NC

NC-NO CHANGE TE-TOGGLE ENABLE X-DON'T CARE

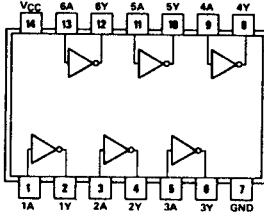
4042



CLOCK	POLARITY	Q
0	0	D
∅	0	LATCH
1	1	D
∅	1	LATCH

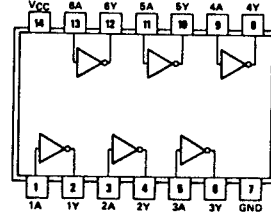


74LS04



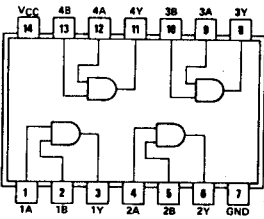
positive logic:
 $Y = \bar{A}$

7406



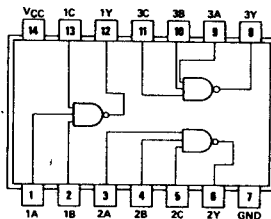
positive logic:
 $Y = \bar{A}$

74LS08



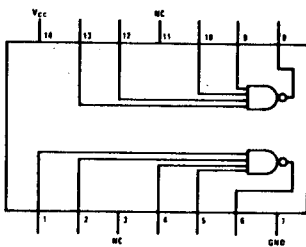
positive logic:
 $Y = AB$

74LS10

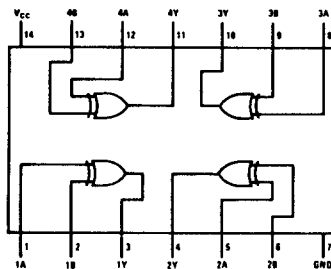


positive logic:
 $Y = \overline{ABC}$

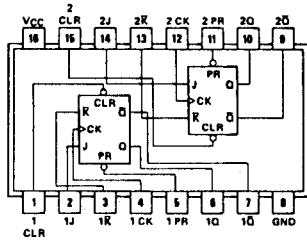
74LS20



74LS86

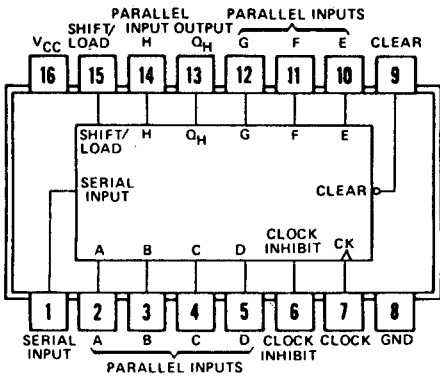


74LS109



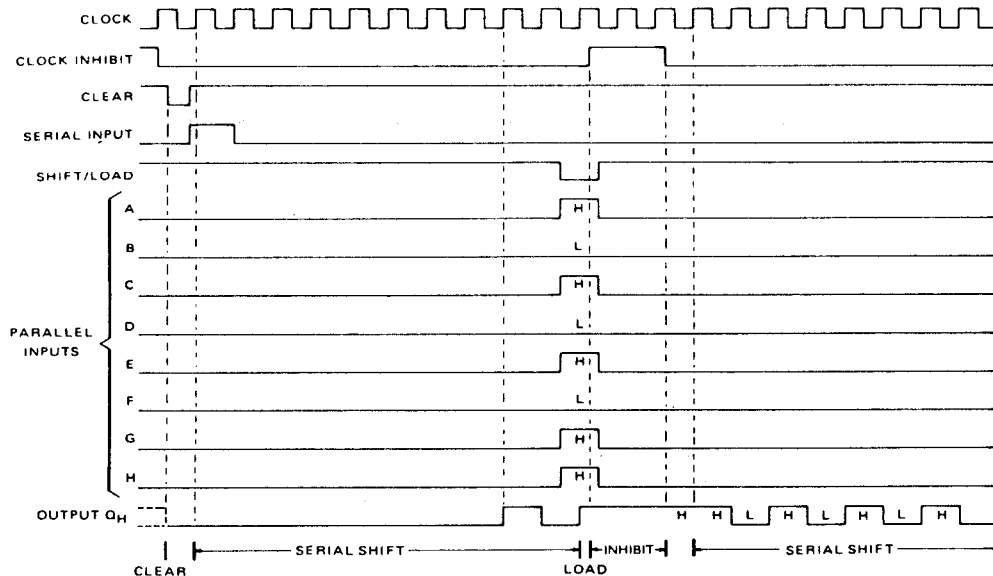
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	\bar{Q}_0

74166

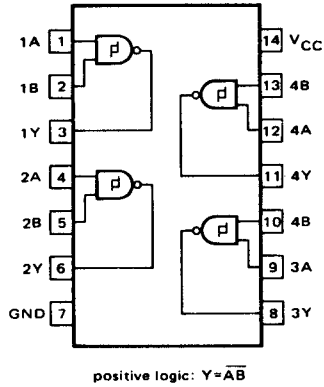


INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q _A	Q _B	Q _H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}

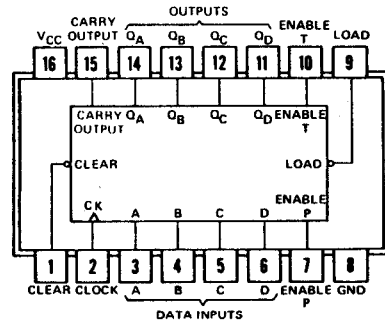
H = high level (steady state), L = low level (steady state)
 X = irrelevant (any input, including transitions)
 ↑ = transition from low to high level
 a...h = the level of steady-state input at inputs A thru H, respectively.
 Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
 Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most-recent ↑ transition of the clock.



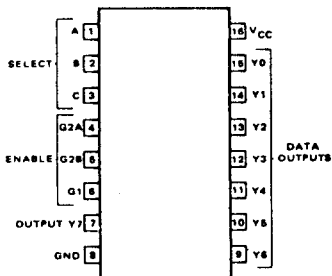
74LS132



74LS163 and 93L16

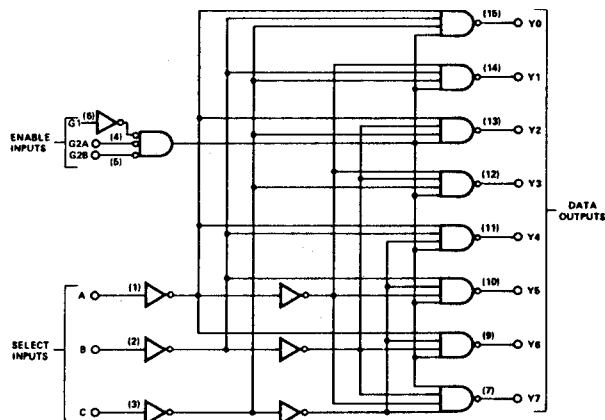


74LS138

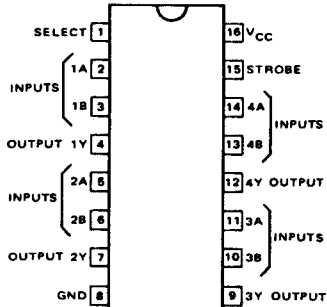


ENABLE		SELECT			OUTPUTS							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
 H = high level, L = low level, X = irrelevant



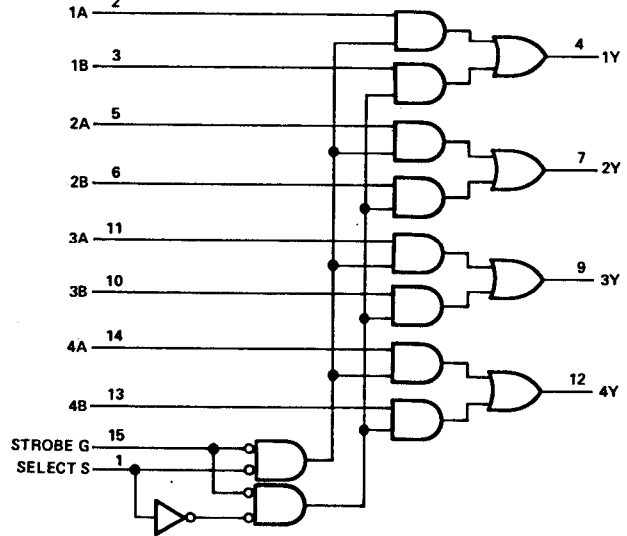
74LS157



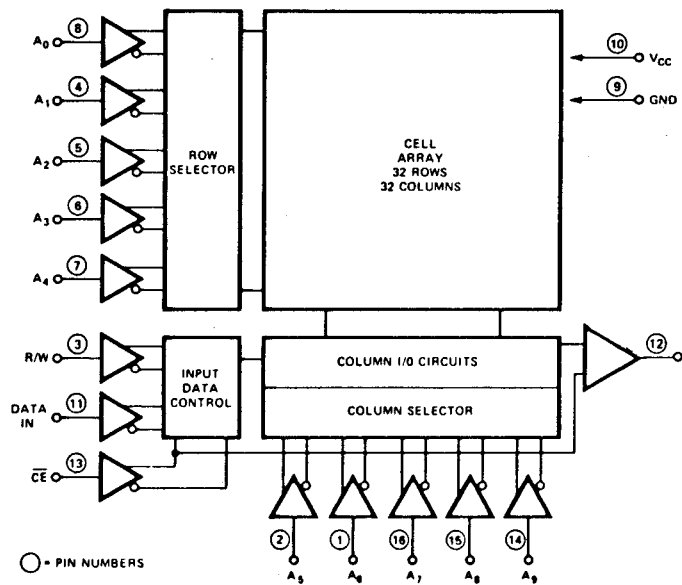
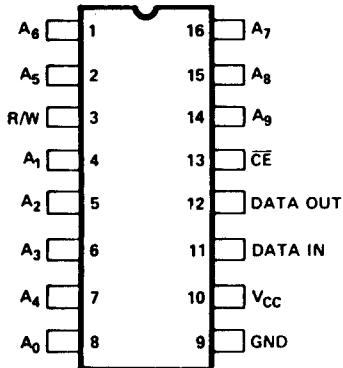
positive logic: low level at S selects A inputs
high level at S selects B inputs

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

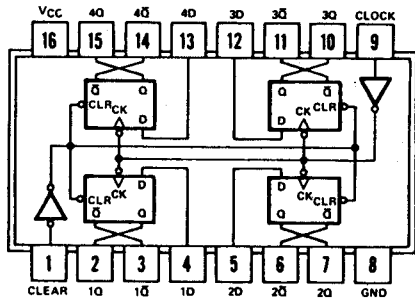


91L02 or 21L02

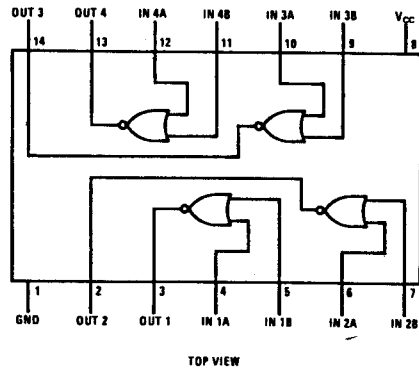


○ = PIN NUMBERS

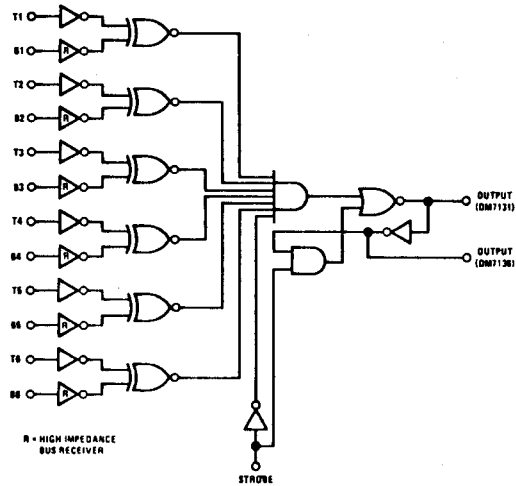
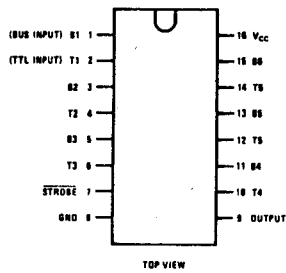
74LS175



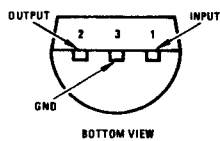
8836 or 8T380



DM8131



78L12A



93L16

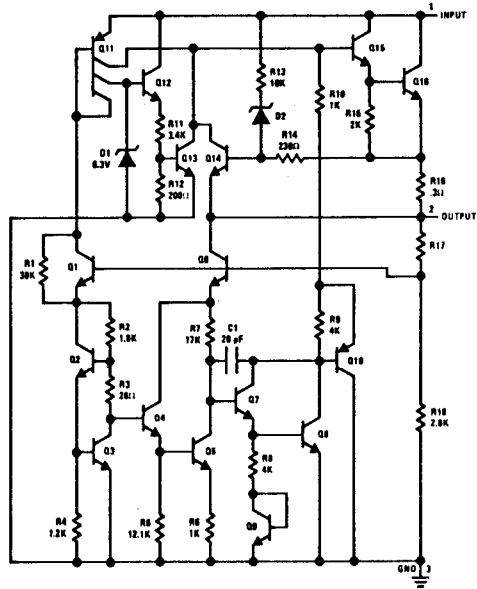
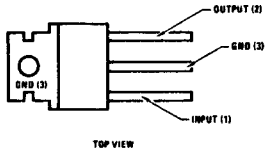
See 74LS163

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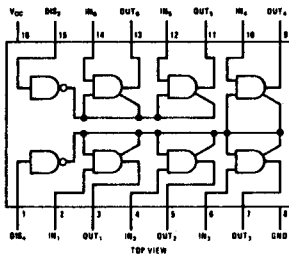
VDM-1 VIDEO DISPLAY MODULE

APPENDIX IV

340T-5.0V or 7805UC



8097 or 8T97

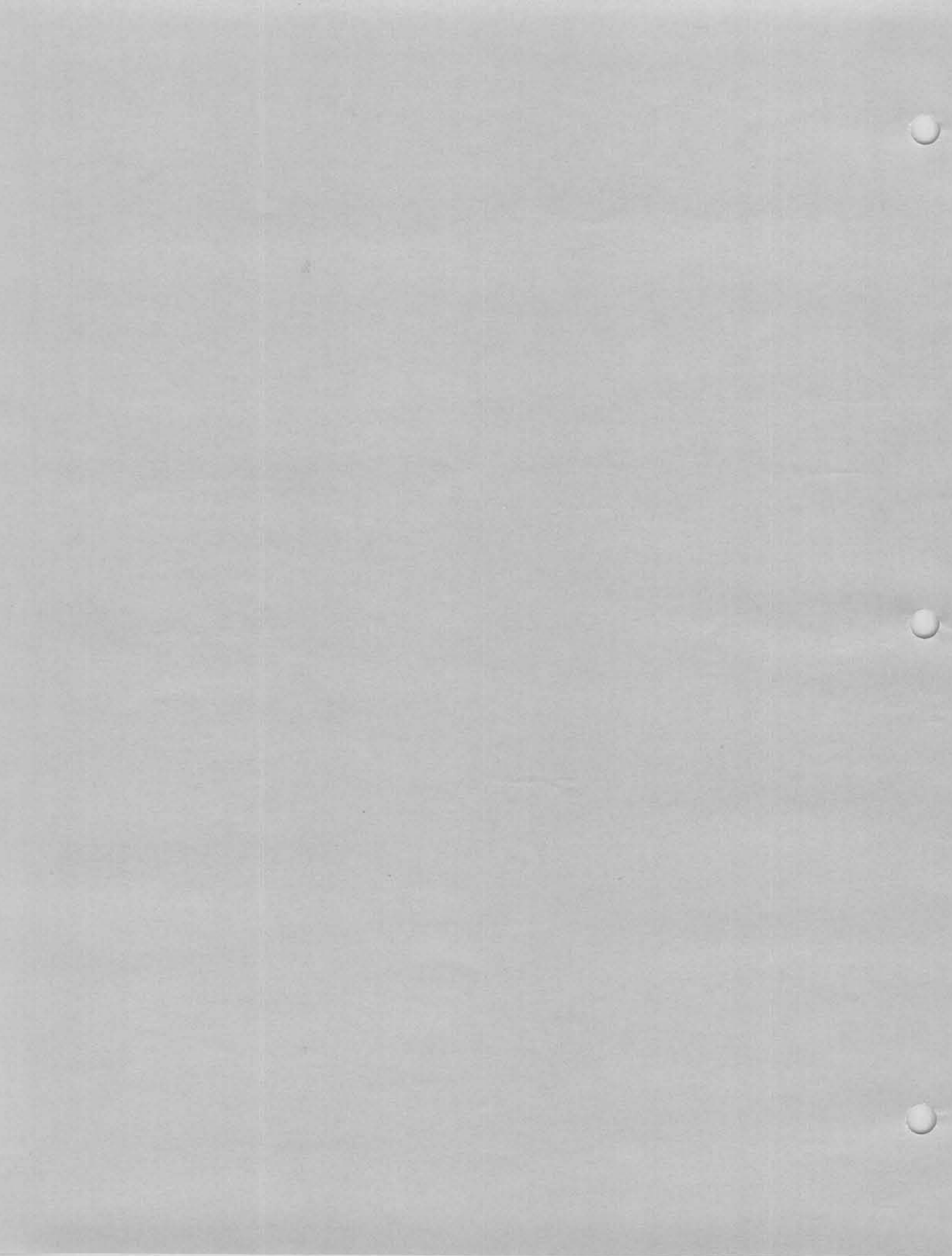


DISABLE DIS ₄	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-Z*
1	X	X	H-Z**

*Output 5-6 only
 **Output 1-4 only
 X = Irrelevant

APPENDIX V

VDM-1 TERMINAL SOFTWARE



<< VDM DRIVER SOFTWARE INSTRUCTIONS >>

The VDM DRIVER SOFTWARE allows the display of printable data onto a television monitor or a modified regular television. The rate at which the data is displayed is controlled from the keyboard used as the input to the computer. The rate may be set from completely stopped to over 2000 characters per second! The entire screen may be cleared from the keyboard and the cursor may be turned on or off as desired. The display format is 16 lines of 64 characters. If the line being displayed exceeds 64 characters the screen is scrolled up and continued on the next screen line. Control characters are not displayed.

The VDM DRIVER program is called by a user output routine or by BASIC depending upon which version is used. In the BASIC version, a sense switch is used to send the data to either the screen or to a printer.

If you wish to use the VDM with MITS BASIC, use the BASIC-VDM DRIVER program which automatically loads the VDM DRIVER SOFTWARE and links itself to BASIC'S output routines.

For use with other programs the machine language VDM DRIVER should be loaded into memory and called by a users program with the data to be displayed in register B.

BASIC-VDM DRIVER

The BASIC version of the VDM DRIVER operates with the same commands as the machine language version. The display speed may be changed during an active screen, (data being presented). The display and program may also be stopped by typing a 'space bar', and then resumed by typing any key except another space. If a number is typed, the display is resumed at the new speed. Changing speed when the display is not active is not possible when running BASIC. The BASIC-VDM DRIVER is also RELOCATABLE and the STATUS BITS and I/O PORTS are AUTOMATICALLY SET to the values your BASIC is running with.

MACHINE LANGUAGE VDM DRIVER

The software requires 512 bytes of memory and may be located anywhere in memory except the first 512 bytes that are used for the relocating hex loader. A simple BINARY loader is used to bootstrap in an Intel format checksum loader that allows the VDM DRIVER software to be placed anywhere in memory. It is usually best to put it in the last 512 bytes of available memory. A users program should CALL to the first location of the VDM DRIVER program with the data in register B. The driver will save the calling programs stack and all of its registers. The data is displayed on the screen and screen operations are performed by the VDM DRIVER, then the calling program's stack and registers are restored and a RETURN is executed.

VDM DRIVER OPERATION

1.) INITIALIZING THE SCREEN AND CURSOR

The first time the VDM software is accessed the ^{SP} cursor position must be set. Type a SHIFT K or LEFT BRACKET "[". The screen is cleared and the cursor is set to the bottom left.

SCREEN CONTROL COMMANDS FOR BASIC

CONTROL Z: CLEAR SCREEN AND INITIALIZE CURSOR

CONTROL A: TURN CURSOR ON/OFF

SCREEN CONTROL COMMANDS FOR MACHINE LANGUAGE SOFTWARE

SHIFT K or LEFT BRACKET ([): CLEAR SCREEN & INITIALIZE CURSOR

SHIFT M or RIGHT BRACKET (]): TURN CURSOR OFF/ON

SHIFT L or BACKSLASH (\): SET SPEED {not in BASIC program}

This command will allow the display speed to be changed when there is no active display movement. " NEW SPEED (1-9)? " will appear on the screen. A number 1 thru 9 may then be typed and the display speed will be adjusted accordingly. Any other character typed will cause no change in the speed.

1 = NO DELAY [about 2000 CPS or 2000 60 chr lines per min]
 9 = GREATEST DELAY [about 1.5 characters per second]

SPEED CONTROL:

During active display, (driver program being accessed), the speed may be changed or the display stopped. Type a number 1-9 and the speed will change and remain set at that speed until changed again. If the SPACE BAR is typed during display action, the screen will freeze until any key other than the space bar is typed. If a number is typed, the display will resume at the new speed, otherwise the display will resume at the last set speed. The SPACE BAR may be used to 'SINGLE STEP' the display.

NOTE: IN PROGRAMS SUCH AS "BASIC" THAT ALTER THE DATA AVAILABLE FLAG, IT MAY BE NECESSARY TO HIT A SPEED CONTROL VALUE TWICE. THE SAME IS TRUE FOR "BREAK" OR CONTROL "C" IN "BASIC".

MACHINE LANGUAGE VDM DRIVER LOADING INSTRUCTIONS

1.) SET THE BINARY BOOTSTRAP LOADER LISTED HEREIN INTO MEMORY STARTING AT LOCATION ZERO (0).

2.) SET THE SENSE SWITCHES TO THE DESIRED MEMORY LOCATION WHERE THE DRIVER SOFTWARE IS TO RESIDE.

THE 8 SENSE SWITCHES ARE USED BY THE LOADER AS THE STARTING HIGH ORDER BYTE OF MEMORY ADDRESS TO LOAD THE SOFTWARE INTO THE CORRECT LOCATION AND TO ADJUST THE HIGH ORDER ADDRESSES REFERENCED BY THE VDM DRIVER PROGRAM INTERNALLY.

Example:

TO LOAD THE DRIVER STARTING AT 4E00 (HEX); {047000 octal}
THE SENSE SWITCHES SHOULD BE SET TO READ 4E (HEX).

A15-down A14-UP A13-down A12-down : A11-UP A10-UP A9-UP A8-down
4 : E

THE DRIVER WILL THEN LOAD INTO LOCATIONS 4E00H TO 4FFFH.
47000Q TO 47400Q

!!! MAKE SURE YOU SET THE SENSE SWITCHES PRIOR TO LOADING !!!!!!

Note: The driver will not load into locations 0-1FF as the loading routine resides there during load time.

3.) READ IN THE VDM DRIVER PAPER TAPE STARTING ON THE BLANK LEADER AT THE BEGINNING OF THE TAPE.

Note: There are two sections of the paper tape. The first is the hex loader that is bootstrapped into locations 25H-138H. The second part starts at the blank area on the tape about 3 feet from the beginning, and is the VDM DRIVER software in hexadecimal checksum relocate format.

The binary load routine first loads the hex loading routine and then jumps to that routine and reads in the hexadecimal format VDM DRIVER software. The jump may be noted by a change in the front panel lights. The 'input' light should be on during the reading of the tape by the load routine.

4.) WHEN THE PAPER TAPE HAS BEEN READ THE PROGRAM OUTPUTS "LOAD COMPLETE" TO THE LOAD DEVICE PORT AND ENTERS A HOLD LOOP. THE VDM DRIVER MAY THEN BE CALLED BY ANY PROGRAM. THE DATA IN REGISTER "B" WILL BE DISPLAYED ON THE SCREEN. THE CALLING POINT WILL BE THE FIRST LOCATION USED BY THE DRIVER.

THE SCREEN MUST BE INITIALIZED THE FIRST TIME IT IS ACCESSED. TYPE 'SHIFT K' TO CLEAR SCREEN AND INITIALIZE CURSOR.

5.) ERRORS DURING LOADING

A. IF THE SENSE SWITCHES INDICATE 0 OR 1, THE PROGRAM WILL PRINT "SET SENSE SWITCHES" TO THE LOAD DEVICE PORT. THE SWITCHES SHOULD BE SET TO THE DESIRED ADDRESS AND THE PAPER TAPE REPOSITIONED TO ITS SECOND BLANK AREA. EXAMINE LOCATION 25H {045Q} AND HIT "RUN", AND TURN ON THE TAPE READER.

B. IF THE LOADER CANNOT VERIFY THAT THE DATA LOADED IS CORRECT, "MEMORY ERROR" WILL BE OUTPUT TO THE LOAD DEVICE PORT. CHECK TO SEE THAT THE SENSE SWITCHES ARE SET TO THE CORRECT ADDRESS AND THAT MEMORY IS UNPROTECTED.

C. IF THE CHECKSUM VALUE EACH 26 BYTES IS NOT CORRECT, "CHECKSUM ERROR" WILL BE OUTPUT. TRY READING THE TAPE AGAIN FROM THE SECOND BLANK AREA. RESTART THE LOADER PROGRAM FROM LOCATION 25H. IF CHECKSUM ERRORS STILL OCCUR, EITHER THE PAPER TAPE IS BAD OR IS NOT BEING READ PROPERLY.

6.) PORT ADDRESS AND STATUS BITS

THE PAPER TAPE AND LISTING ARE SET UP WITH THE FOLLOWING:

```
STATUS PORT      = 0
DATA PORT        = 1
DATA AVAILABLE FLAG BIT      = 40H { 1000 } ACTIVE HIGH
TRANSMITTER BUFFER EMPTY BIT = 80H { 2000 } ACTIVE HIGH
```

ALL REFERENCE TO THIS SET UP IS INDICATED ON THE LISTINGS BY AN ARROW " <-----<<< ".

IF CHANGES ARE NECESSARY FIRST CHANGE THE BINARY BOOT LOADER AND READ THE PAPER TAPE UNTIL THE BLANK AREA 3 FEET FROM THE BEGINNING OF THE TAPE. STOP THE COMPUTER AND MAKE THE CHANGES IN THE HEX LOADER USING THE LISTING AS A REFERENCE. THEN RESTART THE HEX LOADER AT LOCATION 25H AND READ THE REST OF THE PAPER TAPE. AFTER THE TAPE HAS BEEN READ IN, MAKE THE CHANGES TO THE VDM DRIVER AGAIN USING THE LISTING AS A GUIDE. REMEMBER THAT THE HIGH ORDER ADDRESS BYTES WILL BE DIFFERENT ACCORDING TO THE ADDRESS THE PROGRAM WAS SET TO. THE LOW ORDER ADDRESS BYTES WILL CORRESPOND HOWEVER. IF YOUR STATUS IS ACTIVE LOW, CHANGE THE BYTES INDICATED BY AN ARROW " <---[J(N)Z]---<<< " TO "JNZ" OR "JZ" AS NEEDED. IF YOUR STATUS IS ACTIVE LOW, THE INSTRUCTIONS WILL BE THE OPPOSITE OF THOSE IN THE LISTING.

BASIC-VDM DRIVER LOADING INSTRUCTIONS

1.) LOAD BASIC

!!! IMPORTANT !!!

2.) LEAVE AT LEAST 512 BYTES OF MEMORY FREE ABOVE YOUR RESPONSE TO THE QUESTION "MEMORY SIZE?" DURING THE INITIALIAZION OF BASIC. THERE MUST BE ROOM FOR THE DRIVER ABOVE BASIC!

EXAMPLE: IF YOU HAVE 20K OF MEMORY THEN THE DECIMAL EQUIVALENT IS 20480. 20480-512 = 19968 WHICH IS THE MAXIMUM VALUE YOU SHOULD TYPE FOR "MEMORY SIZE".

IT IS A GOOD IDEA TO SET THE "TERMINAL WIDTH" TO 63 FOR USE WITH THE VDM.

3.) AFTER BASIC IS INITIALIZED AND PRINTS "OK", TYPE "NEW", TYPE "NULL 0", AND LOAD IN THE BASIC-VDM DRIVER PROGRAM.

4.) PUT SENSE SWITCH A8 UP AND TYPE 'RUN'. THE PROGRAM WILL ASK FOR INFORMATION REGARDING DESTINATION LOCATION, VDM MEMORY ADDRESS , VDM PORT ASSIGNMENT, ETC..

"WAIT A MOMENT....." !!! IMPORTANT !!!
WHEN THE PROGRAM TYPES "WAIT A MOMENT....", IT IS PEEKING THROUGH ITSELF TO DETERMINE STATUS AND I/O VALUES, PATCH POINTS, AND LOADING THE VDM DRIVER SOFTWARE INTO MEMORY. THIS MAY TAKE 30 TO 60 SECONDS. ALL THE FRONT PANEL LIGHTS GO ON AND THEY LOOK VERY STILL; BUT DON'T START TO WORRY THAT THE PROGRAM HAS CRASHED...UNTIL ABOUT 2 MINUTES.....THEN WORRY.

5.) SENSE SWITCH A8 WILL NOW CONTROL THE DESTINATION OF OUTPUT. WHEN THE SWITCH IS UP, DATA WILL GO TO THE DEVICE BASIC WAS SET UP FOR SUCH AS A TELETYPE. WITH THE SWITCH DOWN, THE DATA WILL BE DISPLAYED ON THE TV SCREEN. THE SWITCH MAY BE CHANGED AT ANY TIME, INCLUDING DURING OUTPUT.

6.) TYPE CONTROL Z
THE FIRST TIME THE SCREEN IS ACCESSED IT MUST BE INITIALIZED.

.....you won't use so much paper now

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

```

0000          0001 *
0000          0002 *
0000          0003 *
0000          0004 *      <<<  VDM DRIVER BOOTSTRAP LOADER  >>>
0000          0005 *      BINARY
0000          0006 *
0000          0007 *      THIS PROGRAM IS USED TO ROOTSTAP IN THE
0000          0008 *      VDM DRIVER SOFTWARE.  THE FIRST PART OF
0000          0009 *      THE VDM TAPE IS AN INTEL HEX CHECKSUM
0000          0010 *      LOADER THAT IS USED TO RELOCATE THE VDM
0000          0011 *      DRIVER CODE ACCORDING TO THE SETTING OF
0000          0012 *      THE SENSE SWITCHES ON THE FRONT PANEL.
0000          0013 *      PLEASE REFER TO LOADING INSTRUCTIONS
0000          0014 *      FOR FURTHER INFORMATION ON THE LOADING
0000          0015 *      PROCEDURE.
0000          0016 *
0000          0017 *      LOAD THIS PROGRAM STARTING AT LOCATION ZERO (0)
0000          0018 *
0000          0019 *
0000 21 25 00    0020 BEGIN LXI  H,STACK  SET MEMORY ADDRESS
0003 F9          0021          SPHL  .      SET STACK POINTER
0004 4C          0022          MOV   C,H     CLEAR REG C
0005 CD 19 00    0023          CALL  IN     GET BINARY BYTE
0008 FE 7F       0024          CPI   7FH    WAIT FOR START BYTE
000A C2 00 00    0025          JNZ   BEGIN
000D             0026 *
000D OD         0027 CHRIN DCR  C      DECREMENT BYTE COUNT
000E CA 25)00    0028          JZ   STACK  JUMP TO HEX LOADER IF DONE
0011 CD 19 00    0029          CALL  IN     GET BYTE
0014 77          0030          MOV   M,A    PUT IT IN MEMORY
0015 23          0031          INX  H      NEXT MEMORY ADDRESS
0016 C3 OD 00    0032          JMP  CHRIN  GET ANOTHER BYTE
0019             0033 *
0019 DB 00       0034 IN   IN   STAT  GET CHR  <-----<<<
001B E6 40       0035          ANI  DAV   DATA AVAILABLE? <-----<<<
001D CA 19 00    0036          JZ   IN    NO- WAIT
0020 DB 01       0037          IN   DATA  GET DATA  <-----<<<
0022 C9          0038          RET
0023             0039 *
0023             0040          DS   2
0025             0041 STACK EQU  $      STACK ADDRESS
0025             0042 *
0025             0043 *
0025             0044 DATA EQU  1      DATA PORT <-----<<<
0025             0045 STAT EQU  0      STATUS PORT <-----<<<
0025             0046 DAV  EQU  40H    DATA AVAILABLE <-----<<<
0025             0047 *
0025             0048 *

```

```

BEGIN 0000 0025
CHRIN 000D 0032
DATA  0001 0037
DAV   0040 0035
IN    0019 0023 0029 0036
STACK 0025 0020 0028
STAT  0000 0034

```


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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

```

0025          0001 *
0025          0002 *
0025          0003 *    << INTEL CHECKSUM HEX LOADER FOR VDM-DRIVER >>
0025          0004 *
0025          0005 *
0025          0006 *          VERSION 2.0  APRIL 11, 1976  S. DOMPIER
0025          0007 *
0025          0008 *    THIS IS A MODIFICATION OF AN INTEL HEX CHECKSUM
0025          0009 *    LOADER TO ALLOW RE-LOCATABLE LOADING OF THE
0025          0010 *    VDM-DRIVER SOFTWARE.  THE HIGH ADDRESS IS RCVD
0025          0011 *    FROM THE SENSE SWITCHES, ZERO OR ONE NOT ALLOWED.
0025          0012 *
0025          0013 *
0025 31 4c 38 01    0014 FIRST LXI  SP,STACK  STACK ADDRESS
0028 06 3A        0015 START MVI  B,':'  START OF RECORD
002A CD 18 01    0016          CALL  INB   GET CHARACTER
002D 90          0017          SUB   B    RECORD MARK?
002E C2 28 00    0018          JNZ  START NO-WAIT FOR RECORD MARK
0031 57          0019          MOV  D,A   CLEAR CHECKSUM
0032 CD C0 00    0020          CALL  READ  GET RECORD LENGTH
0035 CA 7D 00    0021          JZ   DONE   IF RECORD=0 THEN DONE
0038 5F          0022          MOV  E,A   RECORD LENGTH IN REG E
0039 CD E6 00    0023          .CALL OFFSET GET MSB FROM DATA
003C 61          0024          MOV  H,C   GET MSB FROM DATA
003D CD C0 00    0025          CALL  READ  GET LSB OF ADDRESS
0040 6F          0026          MOV  L,A   LSB IN REG L
0041 CD C0 00    0027          CALL  READ  SKIP RECORD TYPE
0044          0028 *
0044 CD E6 00    0029 GETCH CALL  OFFSET GET CHARACTER
0047 71          0030          MOV  M,C   PUT CHR IN MEMORY
0048 BE          0031          CMP  M    CHECK IF MEMORY IS OK
0049 C2 71 00    0032          JNZ  MERR  NO- MEMORY ERROR
004C 23          0033          INX  H    NEXT ADDRESS
004D 1D          0034          DCR  E    RECORD LENGTH -1
004E C2 44 00    0035          JNZ  GETCH  GET MORE
0051 CD C0 00    0036          CALL  READ' GET CHECKSUM
0054 CA 28 00    0037          JZ   START  OK- GET NEXT RECORD
0057          0038 *
0057 21 83 00    0039 CERR  LXI  H,CHKER CHECKSUM ERROR
005A CD FE 00    0040 MSG   CALL  CRLF
005D 7E          0041 MSG2  MOV  A,M
005E FE 58      0042          CPI  'X'
0060 CA 6B 00    0043          JZ   HOLD
0063 47          0044          MOV  B,A
0064 CD 0D 01    0045          CALL  OUTB  PRINT CHR
0067 23          0046          INX  H
0068 C3 5D 00    0047          JMP  MSG2
006B          0048 *
006B CD FE 00    0049 HOLD  CALL  CRLF
006E C3 6E 00    0050 HOLD2 JMP  HOLD2
0071          0051 *
0071 21 92 00    0052 MERR  LXI  H,ERR  MEMORY ERROR
0074 C3 5A 00    0053          JMP  MSG
0077 21 9F 00    0054 WHAT  LXI  H,SENSW SET SENSE SWITCHES
007A C3 5A 00    0055          JMP  MSG
007D 21 B2 00    0056 DONE  LXI  H,LCMP  LOAD COMPLETE
0080 C3 5A 00    0057          JMP  MSG
0083          0058 *
0083 43 48 45 43  0059 CHKER ASC  "CHECKSUM ERRORX"
      4B 53 55 4D
      20 45 52 52
      4F 52 58

```

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0092 4D 45 4D 4F	0060 ERR	ASC	"MEMORY ERRORX"
52 59 20 45			
52 52 4F 52			
58			
009F 53 45 54 20	0061 SENSW	ASC	"SET SENSE SWITCHESX"
53 45 4E 53			
45 20 53 57			
49 54 43 48			
45 53 58			
00B2 4C 4F 41 44	0062 LCMP	ASC	"LOAD COMPLETEX"
20 43 4F 4D			
50 4C 45 54			
45 58			
00C0	0063 *		
00C0 CD D1 00	0064 READ	CALL	NIBBLE GET BYTE
00C3 07	0065	RLC	MOV LSB 4 BITS TO MSB 4 BITS
00C4 07	0066	RLC	
00C5 07	0067	RLC	
00C6 07	0068	RLC	
00C7 4F	0069	MOV	C,A SAVE NIBBLE
00C8 CD D1 00	0070	CALL	NIBBLE
00CB B1	0071	ORA	C ADD TWO NIBBLES TOGETHER FOR A BYTE
00CC 4F	0072	MOV	C,A CHARACTER IN REG C
00CD 82	0073	ADD	D ADD CHECKSUM
00CE 57	0074	MOV	D,A CHECKSUM IN REG D
00CF 79	0075 NO	MOV	A,C
00D0 C9	0076	RET	
00D1	0077 *		
00D1 CD 18 01	0078 NIBBLE	CALL	INB GET CHR
00D4 D6 30	0079	SUI	'0' REMOVE ASCII BIAS
00D6 D8	0080	RC	. DONE IF 0-2FH
00D7 C6 E9	0081	ADI	'0'-'G'
00D9 D8	0082	RC	. DONE IF 47H-OFFH
00DA C6 06	0083	ADI	6
00DC F2 E2 00	0084	JP	NIB2 ADD 10 IF A-F
00DF C6 07	0085	ADI	7
00E1 D8	0086	RC	. DONE IF 3AH-40H
00E2 C6 0A	0087 NIB2	ADI	10
00E4 B7	0088	ORA	A SET ZERO FLAG
00E5 C9	0089	RET	
00E6	0090 *		
00E6 CD C0 00	0091 OFFSET	CALL	READ GET CHR
00E9 D6 08	0092	SUI	8 CHECK IF 8 OR 9
00EB CA F3 00	0093	JZ	YES
00EE FE 01	0094	CPI	1
00F0 C2 CF 00	0095	JNZ	NO
00F3 4F	0096 YES	MOV	C,A
00F4 DB FF	0097	IN	OFFH READ SENSE SWITCHES
00F6 FE 02	0098	CPI	2 MUST BE > 1
00F8 DA 77 00	0099	JC	WHAT NO- ERROR
00FB 81	0100	ADD	C ADD OFFSET
00FC 4F	0101	MOV	C,A
00FD C9	0102	RET	
00FE	0103 *		
00FE 06 0D	0104 CRLF	MVI	B,ODH CARRIAGE RETURN
0100 CD 0D 01	0105	CALL	OUTB
0103 06 0A	0106	MVI	B,0AH LINE FEED
0105 CD 0D 01	0107	CALL	OUTB
0108 06 7F	0108	MVI	B,7FH FILL
010A CD 0D 01	0109	CALL	OUTB
010D	0110 *		
010D DB 00	0111 OUTB	IN	STAT <---<<<

CD 00 F9

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

010F E6 80	0112	ANI	TBE	<---<<<
0111 CA 0D 01	0113	JZ	OUTB	
0114 78	0114	MOV	A,B	
0115 D3 01	0115	OUT	DATA	<---<<<
0117 C9	0116	RET		
0118	0117 *			
0118 DB 00	0118 INB	IN	STAT	CHECK STATUS PORT <---<<<
011A E6 40 02	0119	ANI	DAV	DATA AVAILABLE? <---<<<
011C CA 18 01	0120	JZ	INB	NO- WAIT <---[J(N)Z]---<<<
011F DB 01 02	0121	IN	DATA	GET CHR FROM DATA PORT <---<<<
0121 E6 7F	0122	ANI	7FH	
0123 C9	0123	RET		
0124	0124 *			
0124	0125 *			
0124	0126 STAT	EQU	0	STATUS PORT <---<<<
0124	0127 DATA	EQU	1	DATA PORT <---<<<
0124	0128 DAV	EQU	40H	DATA AVAILABLE <---<<<
0124	0129 TBE	EQU	80H	TRANSMITTER BUFFER EMPTY <---<<<
0124	0130 *			
0124	0131	DS	20	STACK AREA
0138	0132 STACK	EQU	\$	
0138	0133 *			
0138	0134 *			

CERR	0057			
CHKER	0083	0039		
CRLF	00FE	0040	0049	
DATA	0001	0115	0121	
DAV	0040	0119		
DONE	007D	0021		
ERR	0092	0052		
FIRST	0025			
GETCH	0044	0035		
HOLD	006B	0043		
HOLD2	006E	0050		
INB	0118	0016	0078	0120
LCMP	00B2	0056		
MERR	0071	0032		
MSG	005A	0053	0055	0057
MSG2	005D	0047		
NIB2	00E2	0084		
NIBBL	00D1	0064	0070	
NO	00CF	0095		
OFFSE	00E6	0023	0029	
OUTB	010D	0045	0105	0107 0109 0113
READ	00C0	0020	0025	0027 0036 0091
SENSW	009F	0054		
STACK	0138	0014		
START	0028	0018	0037	
STAT	0000	0111	0118	
TBE	0080	0112		
WHAT	0077	0099		
YES	00F3	0093		

0123 - C5
 0124 - F5
 0125 - 060 0
 0127 - 0E 45
 0129 - CD 2F 01
 012C - F1
 012D - C1
 012E - C9
 012F - 0D
 0130 - C8
 0131 - 05
 0132 - CA 2F 01
 0135 - C3 31 01
 0137

TUNE FOR MAX SPD

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0800		0001 *
0800		0002 *
0800		0003 * <<< VDM DISPLAY DRIVER >>>
0800		0004 *
0800		0005 * VERSION 3.0 APRIL 12,1976 S.DOMPIER
0800		0006 *
0800		0007 *
0800		0008 *
0800		0009 * INPUT ROUTINE
0800		0010 *
0800		0011 * THIS ROUTINE SAVES THE CALLING STACK,
0800		0012 * PERFORMS SCREEN OPERATIONS AND RETURNS
0800		0013 * TO THE CALLING PROGRAM AFTER RESTORING
0800		0014 * THE SYSTEM STACK. IT MAY BE USED WITH
0800		0015 * PTCO. "SOFTWARE PACKAGE #1" WITH
0800		0016 * EXELLENT RESULTS. THE CHARACTER TO BE
0800		0017 * DISPLAYED SHOULD BE IN REGISTER B.
0800		0018 *
0800		0019 *
0800		3333 * VDM MEMORY ADDRESS = CCOOH
0800		3333 * VDM PORT = C8
0800		3333 * DATA PORT = 1
0800		3333 * STATUS PORT = 0
0800		3333 * DAV = 40H
0800		3333 * TBE = 80H
0800		3333 *
0800		3333 *
0800		0020 * CALL HERE WITH CHARACTER IN REG B
0800		0021 *
0800		0022 *
0800	22 B7 09	0023 VDM SHLD HLSAV SAVE HL
0803	21 00 00	0024 LXI H,0
0806	39	0025 DAD SP GET SYSTEM STACK POINTER
0807	31 F0 09	0026 LXI SP,STACK SET NEW STACK
080A	E5	0027 PUSH H SAVE SYSTEM STACK POINTER
080B	D5	0028 PUSH D SAVE ALL REGISTERS
080C	C5	0029 PUSH B
080D	F5	0030 PUSH PSW
080E	CD 1A 08	0031 CALL SCREEN DO SCREEN OPERATIONS
0811	F1	0032 POP PSW RESTORE REGISTERS
0812	C1	0033 POP B
0813	D1	0034 POP D
0814	E1	0035 POP H
0815	F9	0036 SPHL RESTORE SYSTEM STACK
0816	2A B7 09	0037 LHLD HLSAV RESTORE HL
0819	C9	0038 RET BACK TO CALLING PROGRAM
081A		0039 *
081A		0040 *
081A		0041 *
081A	78	0042 SCREEN MOV A,B GET CHR
081B	E6 7F	0043 ANI 7FH STRIP MSB
081D	FE 7F	0044 CPI 7FH DON'T WANT DELETE
081F	C8	0045 RZ
0820	FE 5F	0046 CPI 5FH BACKSPACE? (shift O)
0822	CA 2D 09	0047 JZ BKSPA
0825	FE 5B	0048 CPI '[' CLEAR SCREEN? (shift K)
0827	CA CE 08	0049 JZ CLR
082A	FE 5D	0050 CPI ']' CURSOR OFF/ON? (shift M)
082C	CA 41 09	0051 JZ CURTG
082F	FE 50 26	0052 CPI '\ ' SPEED CONTROL? (shift L)
0831	CA 81 08	0053 JZ SETSP
0834	FE 0D	0054 CPI ODH CARRIAGE RETURN?

800
9B9
TB9
F900

'g'(shift)

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

```

0836 CA 15 09      0055      JZ      CHOT2
0839 FE 20      0056      CPI      20H
083B D8      0057      RC      .      DON'T DISPLAY CONTROL CHRS
083C      0058 *
083C      0059 *
083C      0060 *
083C      0061 *      OUTPUT TIMER
083C      0062 *
083C F5      0063 TIMER  PUSH  PSW      SAVE CHARACTER
083D 3A B6 09    0064      LDA      SPEED  GET DELAY TIME
0840 67      0065      MOV      H,A    SET COUNTER IN HL
0841 2E 80      0066      MVI      L,80H
0843 CD A7 09    0067      CALL     STATUS ANYBODY WANT IN?
0846 CA 6E 08    0068      JZ      NEXT2  NO- CONTINUE <-----[ J(N)Z ]---<<<
0849 CD AC 09    0069      CALL     INPUT YES- SEE WHO IT IS
084C CD 52 08    0070      CALL     NUMCK
084F C3 6D 08    0071      JMP      NEXT
0852      0072 *
0852      0073 *
0852      0074 *      CHECK FOR TIME CONTROL VALUE
0852      0075 *
0852 FE 3A      0076 NUMCK  CPI      '9'+1  NO- CHECK IF ASCII NUMBER 1-9
0854 D2 77 08    0077      JNC      WAIT  TO BIG
0857 FE 31      0078      CPI      '1'
0859 DA 77 08    0079      JC       WAIT  TO SMALL
085C E6 0F      0080      ANI      OFH   JUST RIGHT- REMOVE ASCII BIAS
085E 4F      0081      MOV      C,A   SAVE DELAY NUMBER
085F AF      0082      XRA      A     CLEAR ACCUMULATOR
0860 37      0083      STC      .     INITIALIZE DELAY BIT IN CARRY
0861 0D      0084 LESS   DCR      C     DECREMENT DELAY NUMBER
0862 CA 69 08    0085      JZ      FOUND  STOP ROTATING DELAY BIT
0865 17      0086      RAL      .     SHIFT DELAY BIT LEFT
0866 C3 61 08    0087      JMP      LESS  NEXT ROUND
0869 32 B6 09    0088 FOUND  STA      SPEED  STORE DELAY TIME
086C C9      0089      RET
086D      0090 *
086D 2B      0091 NEXT   DCX      H     DELAY MINUS ONE
086E 7C      0092 NEXT2  MOV      A,H   GET HIGH BYTE OF DELAY COUNT
086F B7      0093      ORA      A     IS IT ZERO?
0870 C2 6D 08    0094      JNZ     NEXT  NO- DELAY SOME MORE
0873 F1      0095      POP      PSW   GET CHR
0874 C3 00 09    0096      JMP      CHOUT TO THE SCREEN!
0877      0097 *
0877      0098 *
0877 FE 20      0099 WAIT   CPI      20H   SPACE BAR?
0879 C0      0100      RNZ      .     NO- CONTINUE
087A CD A7 09    0101 WAIT2  CALL     STATUS YES- WAIT FOR KEYBOARD INPUT
087D CA 7A 08    0102      JZ      WAIT2 <-----[ J(N)Z ]---<<<
0880 C9      0103      RET
0881      0104 *
0881      0105 *
0881      0106 *      SET DISPLAY SPEED
0881      0107 *
0881 CD 15 09    0108 SETSP  CALL     CHOT2
0884 21 BA 08    0109      LXI      H,MSG  SPEED MESSAGE
0887 7E      0110 SET1  MOV      A,M
0888 FE 58      0111      CPI      'X'   MESSAGE TERMINATOR
088A CA 96 08    0112      JZ      SET2
088D E5      0113      PUSH     H
088E CD 00 09    0114      CALL     CHOUT  MESSAGE TO SCREEN
0891 E1      0115      POP      H
0892 23      0116      INX      H

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0893 C3 87 08	0117	JMP	SET1	
0896 CD A7 09	0118 SET2	CALL	STATUS	GET NEW SPEED
0899 CA 96 08	0119	JZ	SET2	WAIT FOR IT <-----[J(N)Z]----<<<
089C CD AC 09	0120	CALL	INPUT	GET NUMBER
089F FE 3A	0121	CPI	'9'+1	
08A1 D2 B4 08	0122	JNC	OPPS	TO BIG
08A4 FE 31	0123	CPI	'1'	
08A6 DA B4 08	0124	JC	OPPS	TO SMALL
08A9 F5	0125	PUSH	PSW	SAVE IT
08AA CD 00 09	0126	CALL	CHOUT	DISPLAY IT
08AD CD 15 09	0127	CALL	CHOT2	
08B0 F1	0128	POP	PSW	
08B1 C3 52 08	0129	JMP	NUMCK	
08B4 21 CC 08	0130 OPPS	LXI	H,MSG+18	PRINT "?"
08B7 C3 87 08	0131	JMP	SET1	
08BA 20 4E 45 57	0132 MSG	ASC	" NEW SPEED (1-9)? X"	
20 53 50 45				
45 44 20 28				
31 2D 39 29				
3F 20 20 58				
08CE	0133 *			
08CE	0134 *			
08CE	0135 *		CLEAR SCREEN & INITIALIZE CURSOR	
08CE	0136 *			
08CE 21 00 CC	0137 CLR	LXI	H,VDMBASE	VDM MEMORY ADDRESS <----<<<
08D1 7C	0138	MOV	A,H	
08D2 C6 04	0139	ADI	4	VDM MEMORY TOP
08D4 36 20	0140 CLR2	MVI	M,' '	CLEAR SCREEN
08D6 23	0141	INX	H	
08D7 BC	0142	CMP	H	
08D8 C2 D4 08	0143	JNZ	CLR2	
08DB AF	0144	XRA	A	
08DC 32 B4 09	0145	STA	BOSL	BEGINNING SCREEN LINE
08DF 32 B5 09	0146	STA	BOTL	BEGINNING TEXT LINE
08E2 32 B2 09	0147	STA	CCP	CURRENT CURSOR POINTER
08E5 2F	0148	CMA		
08E6 32 B3 09	0149	STA	CURF	CURSOR FLAG
08E9 3E 0F	0150	MVI	A,15	SET CURSOR AT SCREEN BOTTOM
08EB 32 B1 09	0151	STA	CLN	CURRENT LINE NUMBER
08EE CD F2 08	0152	CALL	VDMOT	SET VDM
08F1 C9	0153	RET		
08F2	0154 *			
08F2	0155 *			
08F2	0156 *		OUTPUT BOSL AND BOTL TO VDM	
08F2	0157 *			
08F2 3A B4 09	0158 VDMOT	LDA	BOSL	INITIALIZE VDM
08F5 07	0159	RLC		
08F6 07	0160	RLC		
08F7 07	0161	RLC		
08F8 07	0162	RLC		
08F9 21 B5 09	0163	LXI	H,BOTL	
08FC B6	0164	ORA	M	
08FD D3 C8	0165	OUT	VDMDEV	VDM PORT ADDRESS <----<<<
08FF C9	0166	RET		
0900	0167 *			
0900	0168 *			
0900	0169 *			
0900	0170 *		STORE CHARACTER IN VDM MEMORY	
0900	0171 *			
0900 4F	0172 CHOUT	MOV	C,A	SAVE CHR
0901 3A B2 09	0173	LDA	CCP	GET CURRENT CURSOR POINTER
0904 47	0174	MOV	B,A	

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0905	3A B1 09	0175	LDA	CLN	GET LINE NUMBER
0908	CD 70 09	0176	CALL	CLNA	CONVERT TO ADDRESS
090B	71	0177	MOV	M,C	PUT CHARACTER ON SCREEN
090C	3A B2 09	0178	LDA	CCP	ADVANCE CURSOR
090F	3C	0179	INR	A	
0910	FE 40	0180	CPI	64	WRAP AROUND?
0912	C2 23 09	0181	JNZ	CHOT1	
0915	3A B2 09	0182	CHOT2	LDA	CCP
0918	47	0183	MOV	B,A	
0919	3A B1 09	0184	LDA	CLN	
091C	CD 9F 09	0185	CALL	CCUR	CLEAR CURSOR
091F	CD 52 09	0186	CALL	SCRL	SCROLL UP
0922	97	0187	SUB	A	SET CURSOR TO LEFT MARGIN
0923	32 B2 09	0188	CHOT1	STA	CCP
0926	47	0189	MOV	B,A	
0927	3A B1 09	0190	LDA	CLN	
092A	C3 83 09	0191	JMP	SCUR	SET CURSOR ON/OFF
092D		0192	*		
092D		0193	*		
092D		0194	*	BACK SPACE AND ERASE LAST CHR	
092D		0195	*		
092D	3A B2 09	0196	BKSPA	LDA	CCP
0930	47	0197	MOV	B,A	GET CURSOR POINTER
0931	3A B1 09	0198	LDA	CLN	
0934	CD 9F 09	0199	CALL	CCUR	CLEAR CURSOR
0937	2B	0200	DCX	H	
0938	36 20	0201	MVI	M, ' '	CLEAR CHR
093A	05	0202	DCR	B	
093B	3A B1 09	0203	LDA	CLN	
093E	C3 83 09	0204	JMP	SCUR	SET CURSOR
0941		0205	*		
0941		0206	*		
0941		0207	*	CURSOR DISPLAY (OFF-ON)	
0941		0208	*		
0941	3A B3 09	0209	CURTG	LDA	CURF
0944	2F	0210	CMA		GET CURSOR FLAG
0945	32 B3 09	0211	STA	CURF	SWITCH IT
0948	3A B2 09	0212	LDA	CCP	GET CURSOR POINTER
094B	47	0213	MOV	B,A	
094C	3A B1 09	0214	LDA	CLN	GET LINE NUMBER
094F	C3 83 09	0215	JMP	SCUR	CURSOR ON/OFF
0952		0216	*		
0952		0217	*		
0952		0218	*	SCROLL SCREEN UP	
0952		0219	*		
0952	21 B5 09	0220	SCRL	LXI	H,BOTL
0955	E5	0221	PUSH	H	
0956	7E	0222	MOV	A,M	
0957	34	0223	INR	M	
0958	96	0224	SUB	M	
0959	01 00 00	0225	LXI	B,0	
095C	CD 70 09	0226	CALL	CLNA	
095F	01 40 20	0227	LXI	B,2040H	
0962	70	0228	SCRL2	MOV	M,B
0963	2C	0229	INR	L	CLEAR BOTTOM LINE
0964	0D	0230	DCR	C	
0965	C2 62 09	0231	JNZ	SCRL2	
0968	E1	0232	POP	H	
0969	7E	0233	MOV	A,M	
096A	E6 0F	0234	ANI	0FH	
096C	77	0235	MOV	M,A	
096D	C3 F2 08	0236	JMP	VDMOT	

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

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0970          0237 *
0970          0238 *
0970          0239 *      CONVERT LINE NUMBER IN REG A AND CHR
0970          0240 *      POSITION IN REG B TO ADDRESS IN HL
0970          0241 *
0970 6F       0242 CLNA   MOV    L,A
0971 3A B5 09 0243     LDA    BOTL   LOAD THE OFFSET FOR LINE 0
0974 85       0244     ADD    L      REG A LOW 4 BITS IS LINE NUMBER
0975 0F       0245     RRC
0976 0F       0246     RRC
0977 6F       0247     MOV    L,A
0978 E6 03    0248     ANI    3
097A C6 CC    0249     ADI    VDMPAGE <---<<<
097C 67       0250     MOV    H,A
097D 7D       0251     MOV    A,L
097E E6 C0    0252     ANI    0COH
0980 80       0253     ADD    B
0981 6F       0254     MOV    L,A
0982 C9       0255     RET
0983          0256 *
0983          0257 *
0983          0258 *      SET CURSOR TO LINE IN REG A AND
0983          0259 *      CHARACTER POSITION IN REG B
0983          0260 *
0983 E6 0F    0261 SCUR   ANI    0FH
0985 32 B1 09 0262     STA    CLN
0988 CD 70 09 0263     CALL  CLNA
098B 78       0264     MOV    A,B
098C 32 B2 09 0265     STA    CCP
098F 3A B3 09 0266     LDA    CURF
0992 B7       0267     ORA    A
0993 7E       0268     MOV    A,M
0994 CA 9B 09 0269     JZ    CCUR2
0997 F6 80    0270     ORI    80H
0999 77       0271     MOV    M,A
099A C9       0272     RET
099B E6 7F    0273 CCUR2  ANI    7FH
099D 77       0274     MOV    M,A
099E C9       0275     RET
099F          0276 *
099F          0277 *      CLEAR CURSOR FROM LINE IN REG A
099F          0278 *      AND POSITION IN REG B
099F          0279 *
099F CD 70 09 0280 CCUR   CALL  CLNA
09A2 7E       0281     MOV    A,M
09A3 E6 7F    0282     ANI    7FH
09A5 77       0283     MOV    M,A
09A6 C9       0284     RET
09A7          0285 *
09A7          0286 *
09A7          0287 *      SPEED CONTROL INPUT ROUTINE
09A7          0288 *
09A7 DB 00    0289 STATUS IN   STAT   STATUS PORT <---<<<
09A9 E6 40    0290     ANI    DAV    DATA AVAILABLE? <---<<<
09AB C9       0291     RET
09AC          0292 *
09AC DB 01    0293 INPUT  IN    DATA   DATA PORT <---<<<
09AE E6 7F    0294     ANI    7FH    STRIP MSB
09B0 C9       0295     RET
09B1          0296 *
09B1          0297 *
09B1          0298 *      RAM STORAGE

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

09B1		0299	*						
09B1	00	0300	CLN	DB	0			CUREENT LINE NUMBER	
09B2	00	0301	CCP	DB	0			CUREENT CURSOR POSITION	
09B3	01	0302	CURF	DB	1			CURSOR DISPLAY FLAG	
09B4	00	0303	BOSL	DB	0			BEGINNING OF SCREEN LINE	
09B5	00	0304	BOTL	DB	0			BEGINNING OF TEXT LINE	
09B6	06	0305	SPEED	DB	6			DELAY BYTE	
09B7		0306	HLSAV	DS	2			USER HL	
09B9		0307	*						
09B9		0308	*						
09B9		0309	SP	EQU	6				
09B9		0310	PSW	EQU	6				
09B9		0311	VDMDEV	EQU	0C8H			VDM OUTPUT PORT <----<<<	
09B9		0312	VDMBASE	EQU	0CC00H			VDM MEMORY ADDRESS <----<<<	
09B9		0313	VDMPAGE	EQU	VDMBASE/256			<----<<<	
09B9		0314	*						
09B9		0315	*						
09B9		0316	STAT	EQU	0			STATUS PORT <----<<<	
09B9		0317	DATA	EQU	1			DATA PORT <----<<<	
09B9		0318	TBE	EQU	80H			TRANSMITTER BUFFER EMPTY <----<<<	
09B9		0319	DAV	EQU	40H			DATA AVAILABLE <----<<<	
09B9		0320	*						
09B9		0321	*						
09B9		0322	STACK	EQU	09F0H			STACK AREA	
09B9		0323	*						
09B9		0324	*						

BKSPA	092D	0047							
BOSL	09B4	0145	0158						
BOTL	09B5	0146	0163	0220	0243				
CCP	09B2	0147	0173	0178	0182	0188	0196	0212	0265
CCUR	099F	0185	0199						
CCUR2	099B	0269							
CHOT1	0923	0181							
CHOT2	0915	0055	0108	0127					
CHOUT	0900	0096	0114	0126					
CLN	09B1	0151	0175	0184	0190	0198	0203	0214	0262
CLNA	0970	0176	0226	0263	0280				
CLR	08CE	0049							
CLR2	08D4	0143							
CURF	09B3	0149	0209	0211	0266				
CURTG	0941	0051							
DATA	0001	0293							
DAV	0040	0290							
FOUND	0869	0085							
HLSAV	09B7	0023	0037						
INPUT	09AC	0069	0120						
LESS	0861	0087							
MSG	08BA	0109	0130						
NEXT	086D	0071	0094						
NEXT2	086E	0068							
NUMCK	0852	0070	0129						
OPPS	08B4	0122	0124						
PSW	0006	0030	0032	0063	0095	0125	0128		
SCREE	081A	0031							
SCRL	0952	0186							
SCRL2	0962	0231							
SCUR	0983	0191	0204	0215					
SET1	0887	0117	0131						
SET2	0896	0112	0119						
SETSP	0881	0053							
SP	0006	0025	0026						

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

SPEED	09B6	0064 0088
STACK	09F0	0026
STAT	0000	0289
STATU	09A7	0067 0101 0118
TBE	0080	
TIMER	083C	
VDM	0800	
VDMBA	CC00	0137
VDMDE	00C8	0165
VDMOT	08F2	0152 0236
VDMPA	00CC	0249
WAIT	0877	0077 0079
WAIT2	087A	0102

PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

```

0000 REM
0002 REM   <<<  BASIC TO VDM-1 LINK PROGRAM  >>>
0004 REM
0006 REM       PROCESSOR TECHNOLOGY CORP.
0008 REM       6200 HOLLIS STREET
0010 REM       EMERYVILLE, CALIFORNIA   94608
0012 PRINT
0014 A$="(HEX) IS YOUR LAST ADDRESS, INPUT:"
0016 B$="GIVE ME YOUR VDM":C$="ADDRESS IN DECIMAL"
0018 PRINT"<<<  VDM TO BASIC LOADING AND LINKING PROGRAM  >>>"
0020 PRINT"   WRITTEN IN BASIC LANGUAGE BY GORDON FRENCH":PRINT
0022 PRINT"REMEMBER, IF YOU DID NOT LEAVE THE LAST 512 BYTES"
0024 PRINT"OF YOUR LAST 4K OF MEMORY FREE WHEN RESPONDING"
0026 PRINT"TO ' ' MEMORY SIZE ? ' ' WHEN THIS BASIC WAS"
0028 PRINT"LOADED, YOU MUST RELOAD BASIC WITH THE CORRECTED"
0030 PRINT"INFORMATION FOR 'MEMORY SIZE'." :PRINT:PRINT
0032 PRINT"INPUT DECIMAL NUMBER OF YOUR LAST 4K BOUNDRY"
0034 PRINT"(EXAMPLE: IF 4FFF "A$" 4(RETURN))"
0036 PRINTTAB(10)"IF 5FFF "A$" 5(RETURN)  "
0037 PRINTTAB(10) "IF AFFF "A$"10(RETURN)  ETC."
0038 INPUT L:IF L<=7 THEN S=0:GOTO 46
0040 PRINT"IS THIS 12K EXTENDED BASIC? (Y/N)":INPUT D$
0042 IF D$="Y" THEN S=65536:GOTO 46
0043 IF D$<>"N"THEN 40
0044 GOTO 84
0046 IF L>15 OR L=0 THEN 32
0048 L=(L*4096)+3584:P=L/256:L=L-S
0050 PRINT"IS YOUR VDM MEMORY ADDRESS CC00(HEX)";
0052 PRINT" WITH PORT=C8? (Y/N)"
0054 INPUT D$:IF D$="Y"GOTO 64
0055 IF D$<>"N" THEN 50
0056 PRINTB$" MEMORY STARTING "C$:INPUT V2
0058 V1=INT(V2/256):V2=((V2/256)-INT(V2/256))*256
0060 PRINTB$" PORT "C$:INPUT V3:IF V3>255 GOTO 60
0062 GOTO 68
0064 V1=204:V2=0:V3=200:V4=192
0068 PRINT"A MOMENT PLEASE..."
0070 S=0
0072 FOR K=0 TO 4096
0074 A=PEEK(K)
0076 B=PEEK(K+1)
0078 IF A = 219 AND B = 0 GOTO 92
0080 IF A = 219 AND B = 1 THEN I=K:GOTO 106
0082 NEXT K
0084 PRINT"IT IS NOT POSSIBLE TO LINK VDM-1";
0086 PRINT" TO THIS BASIC BY MEANS"
0088 PRINT"OF THIS PROGRAM.  SORRY!"
0090 GOTO 146
0092 IF S>0 THEN GOTO 100
0094 C=PEEK(K+2):D=PEEK(K+3):E=PEEK(K+4):F=K+4
0096 IF C<>230 THEN GOTO 82
0098 S=S+1:G=K:GOTO 82

```

PROCESSOR TECHNOLOGY CORPORATION

VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

```
0100 H=PEEK(K+3):J=0
0102 F=F-256:J=J+1:IF F>256 GOTO 102
0104 GOTO 82
0106 FOR Y=L TO L+409
0108 READ Z
0110 IF Z<300 GOTO 138
0112 IF Z=300 THEN Z=V3: GOTO 138
0114 IF Z=400 THEN Z=V2: GOTO 138
0116 IF Z=500 THEN Z=V1: GOTO 138
0118 IF Z=1001 THEN Z=P+1: GOTO 138
0120 IF Z=1000 THEN Z=P: GOTO 138
0122 IF Z=2000 THEN Z=D: GOTO 138
0124 IF Z=3000 THEN Z=E: GOTO 138
0126 IF Z=4000 THEN Z=F: GOTO 138
0128 IF Z=5000 THEN Z=J: GOTO 138
0130 IF Z=6000 THEN Z=H: GOTO 138
0132 PRINT"THIS PROGRAM LOAD IS BAD.";
0134 PRINT" PLEASE RELOAD THIS PROGRAM."
0136 GOTO 146
0138 POKE Y,Z:NEXT Y
0140 POKE G,195:POKE G+1,0:POKE G+2,P
0142 POKE I,205:POKE I+1,110:POKE I+2,P+1:POKE I+3,0
0144 PRINT"VDM-1 IS NOW LINKED TO BASIC":PRINT
0145 PRINT"DO NOT ATTEMPT TO RE-RUN THIS PROGRAM !":PRINT
0146 RESTORE
0148 NULL 0
0150 END
0152 DATA219,255,31,210,13,1000,219,0,230,2000
0154 DATA195,4000,5000,241,230,127,254,32,210,43
0156 DATA1000,254,7,194,30,1000,245,195,6,1000
0158 DATA254,13,202,46,1000,254,1,202,46,1000
0160 DATA254,26,192,254,127,200,245,229,213,197
0162 DATA205,58,1000,193,209,225,241,201,245,58
0164 DATA146,1001,103,46,128,205,105,1001,3000,104
0166 DATA1000,205,110,1001,50,140,1001,254,58,210
0168 DATA112,1000,254,49,218,112,1000,230,15,79
0170 DATA175,55,13,202,100,1000,23,195,92,1000
0172 DATA50,146,1001,43,124,183,194,103,1000,195
0174 DATA181,1000,254,32,194,103,1000,205,105,1001
0176 DATA3000,117,1000,195,103,1000,33,400,500,124
0178 DATA198,4,54,32,35,188,194,132,1000,175
0180 DATA50,144,1001,50,145,1001,50,142,1001,47
0182 DATA50,143,1001,62,15,50,141,1001,205,167
0184 DATA1000,62,13,245,195,181,1000,58,144,1001
0186 DATA7,7,7,33,145,1001,182,211,300
0188 DATA201,58,142,1001,71,241,254,13,202,223
0190 DATA1000,254,95,202,243,1000,254,1,202,3
0192 DATA1001,254,26,202,126,1000,79,58,141,1001
0194 DATA205,50,1001,113,58,142,1001,60,254,64
0196 DATA194,233,1000,58,141,1001,205,97,1001,205
0198 DATA20,1001,151,50,142,1001,71,58,141,1001
0200 DATA195,69,1001,58,141,1001,205,97,1001,43
```

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VDM-1 VIDEO DISPLAY MODULE

APPENDIX V

0202 DATA54,32,5,58,141,1001,195,69,1001,58
0204 DATA143,1001,47,50,143,1001,58,142,1001,71
0206 DATA58,141,1001,195,69,1001,33,145,1001,229
0208 DATA126,52,150,1,0,0,205,50,1001,1
0210 DATA64,32,112,44,13,194,36,1001,225,126
0212 DATA230,15,119,195,167,1000,111,58,145,1001
0214 DATA133,15,15,111,230,3,198,500,103,125
0216 DATA230,192,128,111,201,230,15,50,141,1001
0218 DATA205,50,1001,120,50,142,1001,58,143,1001
0220 DATA183,126,202,93,1001,246,128,119,201,230
0222 DATA127,119,201,205,50,1001,126,230,127,119
0224 DATA201,219,0,230,6000,201,58,140,1001,254
0226 DATA3,194,125,1001,245,175,50,140,1001,241
0228 DATA201,219,1,230,127,254,1,202,46,1000
0230 DATA254,26,202,46,1000,201,0,0,0,1
0232 DATA0,0,6,0,0,0,0,0,0,0



APPENDIX VI

TELEVISION INTERFACE



Television Interface

Anyone with a bunch of memory circuits, control logic and a wire wrap gun can whip up a digital video generator with TTL output levels. The problem as I see it is to get that digital video signal into a form that the TV set can digest. The care and feeding of digital inputs to the TV set is the subject of Don Lancaster's contribution to *BYTE 2* — an excerpt from his forthcoming book, *TV Typewriter Cookbook*, to be published by Howard W. Sams, Indianapolis, Indiana.

... CARL

We can get between a TV typewriter and a television style display system either by an rf modulator or a direct video method.

In the rf modulator method, we build a miniature, low power, direct wired TV transmitter that clips onto the antenna terminals of the TV set. This has the big advantage of letting you use any old TV set and ending up with an essentially free display that can be used just about anywhere. No set modifications are needed, and you have the additional advantage of automatic safety isolation and freedom from hot chassis shock problems.

There are two major restrictions to the rf modulator method. The first of these is that transmitters of this type must meet

certain exactly spelled out FCC regulations and that system type approval is required. The second limitation is one of bandwidth. The best you can possibly hope for is 3.5 MHz for black and white and only 3 MHz for color, and many economy sets will provide far less. Thus, long character line lengths, sharp characters, and premium (lots of dots) character generators simply aren't compatible with clip-on rf entry.

In the direct video method, we enter the TV set immediately following its video detector but before sync is picked off. A few premium TV sets and all monitors already have a video input directly available, but these are still expensive and rare. Thus, you usually have to modify your TV set, either

adding a video input and a selector switch or else dedicating the set to exclusive TV typewriter use. Direct video eliminates the bandwidth restrictions provided by the tuner, i-f strip, and video detector filter. Response can be further extended by removing or shorting the 4.5 MHz sound trap and by other modifications to provide us with longer line lengths and premium characters. No FCC approval is needed, and several sets or monitors are easily driven at once without complicated distribution problems.

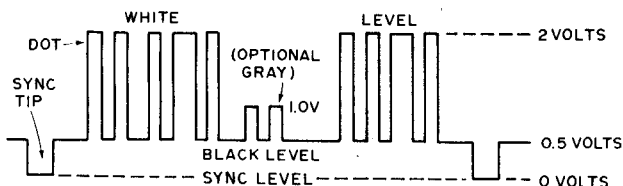
There are two limitations to the direct video technique. One is that the set has to be modified to provide direct video entry. A second, and far more severe, restriction, is that many television sets are "hot chassis" or ac-dc sets with one side of their chassis connected to the power line. These sets introduce a severe shock hazard and cannot be used as TV typewriter video entry displays unless some isolation technique is used with them. If the TV set has a power transformer, there is usually no hot chassis problem. Transistor television sets and IC sets using no vacuum tubes tend to have power transformers, as do older premium tube type sets. All others (around half the sets around today) do not.

Direct Video Methods

With either interface approach, we usually start by getting the dot matrix data, blanking, cursor, and sync signals together into one composite video signal whose

by
 Don Lancaster
 Box 1112
 Parker AZ 85344

Fig. 1. Standard video interface levels. (Source impedance = 72 or 100 Ohms.)



form is useful to monitors and TV sets. A good set of standards is shown in Fig. 1. The signal is dc coupled and always positive going. Sync tips are grounded and blacker than black. The normal open circuit black level is positive by one-half a volt, and the white level is two volts positive. In most TV camera systems, intermediate levels between the half volt black level and the two volt white level will be some shade of gray, proportionately brighter with increasing positive voltage. With most TV typewriter systems, only the three states of zero volts (sync), half a volt (black), and two volts (white dot) would be used. One possible exception would be an additional one volt dot level for a dim but still visible portion of a message or a single word.

The usual video source impedance is either 72 or 100 Ohms. Regardless of how far we travel with a composite video output, some sort of shielding is absolutely essential.

For short runs from board to board or inside equipment, tightly twisted conductors should be OK, as should properly guarded PC runs. Fully shielded cables should be used for interconnections between the TVT and the monitor or TV set, along with other long runs. As long as the total cable capacitance is less than 500 pF or so (this is around 18 feet of RG178-U

miniature coax), the receiving end of the cable need not be terminated in a 72 or 100 Ohm resistor. When terminated cable systems are in use for long line runs or multiple outputs, they should be arranged to deliver the signal levels of Fig. 1 at their output under termination. Generally, terminated cable systems should be avoided as they need extra in the way of drivers and supply power.

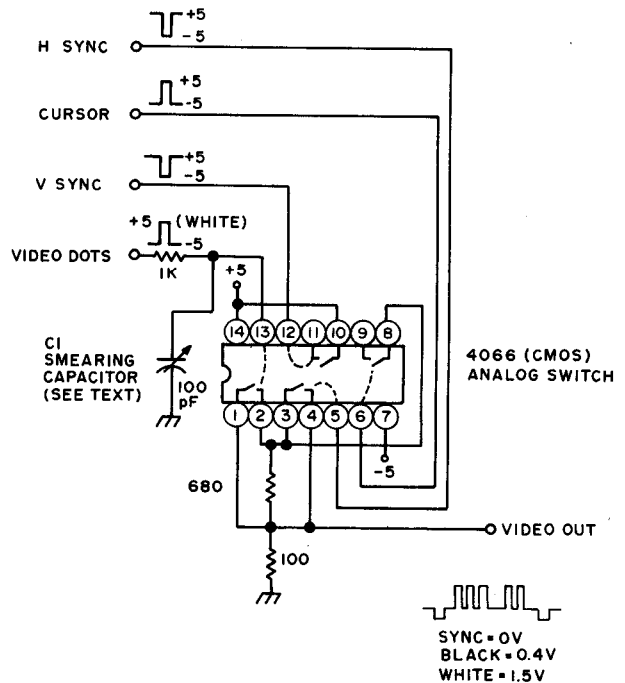
The exact width of the horizontal and vertical sync pulses isn't usually too important, so long as the shape and risetime of these pulses are independent of position control settings and power supply variations. One exception to this is when you're using a color receiver and a color display. Here, the horizontal sync pulse should be held closely to 5.1 microseconds, so the receiver's color burst sampling does in fact intercept a valid color burst. More on this later.

Intentional Smear

Fig. 2 shows us a typical composite video driver using a 4066 quad analog switch. It gives us a 100 Ohm output impedance and the proper signal levels. Capacitor C1 is used to purposely reduce the video rise and fall times. It is called a smearing capacitor.

Why would we want to further reduce the bandwidth and response of a TV system that's already hurting to begin with? In the case of a quality video monitor, we wouldn't. But if we're using an ordinary run-of-the-mill TV set, particularly one using rf entry, this capacitor can

Fig. 2. Analog switch combiner generates composite video.



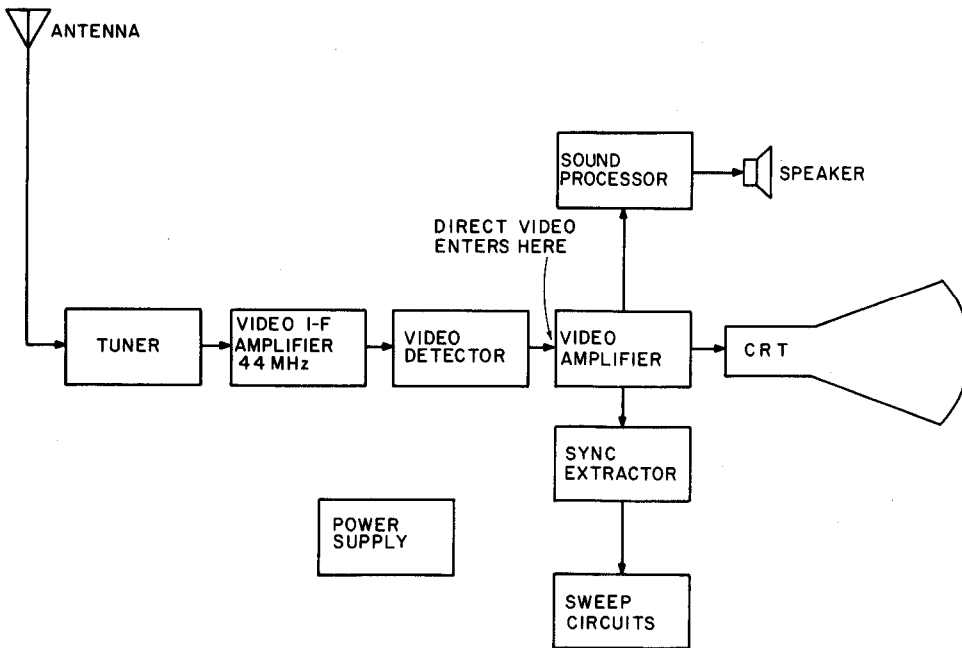
very much improve the display legibility and contrast. Why?

Because we are interested in getting the most legible character of the highest contrast we can. This is not necessarily the one having the sharpest dot rise and fall times. Many things interact to determine the upper video response of a TV display. These include the tuner settings and the i-f response and alignment, the video detector response, video peaking, the sound trap setting, rf cable reflections, and a host of other responses. Many of these stages are underdamped and will ring if fed too sharp a risetime input, giving us a ghosted,

shabby, or washed out character. By reducing the video bandwidth going into the system, we can move the dot matrix energy lower in frequency, resulting in cleaner characters of higher contrast.

For most TV displays, intentional smearing will help the contrast, legibility, and overall appearance. The ultimate limit to this occurs when the dots overlap and become illegible. The

Fig. 3. Block diagram of typical B and W television.



optimum amount of intentional smear is usually the value of capacitance that is needed to just close the inside of a "W" presented to the display.

Adding a Video Input

Video inputs are easy to add to the average television set, provided you follow some reasonable cautions. First and foremost, you must have an accurate and complete schematic of the set to be modified, preferably a Sams Photofact or something similar. The first thing to check is the power supply on the set. If it has a power transformer and has the chassis properly safety isolated from the power line, it's a good choice for a TVT monitor. This is particularly

true of recent small screen, solid state portable TV sets. On the other hand, if you have a hot chassis type with one side of the power line connected to the chassis, you should avoid its use if at all possible. If you must use this type of set, be absolutely certain to use one of the safety techniques outlined later in Fig. 8.

A block diagram of a typical TV set appears in Fig. 3. UHF or VHF signals picked up by the tuner are downconverted in frequency to a video i-f frequency of 44 MHz and then filtered and amplified. The output of the video i-f is transformer coupled to a video detector, most often a small signal germanium diode. The video detector output is filtered to

remove the carrier and then routed to a video amplifier made up of one or more tubes or transistors.

At some point in the video amplification, the black and white signal is split three ways. First, a reduced bandwidth output routes sync pulses to the sync separator stage to lock the set's horizontal and vertical scanning to the video. A second bandpass output sharply filtered to 4.5 MHz extracts the FM sound subcarrier and routes this to a sound i-f amplifier for further processing. The third output is video, which is strongly amplified and then capacitively coupled to the cathode of the picture tube.

The gain of the video amplifier sets the contrast of the display, while the bias setting on the cathode of the picture tube (with respect to its grounded control grid) sets the display brightness. Somewhere in the video amplifier, further rejection of the 4.5 MHz sound subcarrier is usually picked up to minimize picture interference. This is called a sound trap. Sound traps can be a series resonant circuit to ground, a parallel resonant circuit in the video signal path, or simply part of the transformer that is picking off the sound for more processing.

The video detector output is usually around 2 volts peak to peak and usually subtracts from a white level bias setting. The stronger the signal, the more negative the swing, and the blacker the picture. Sync tips are blacker than black, helping to blank the display during retrace times.

Fig. 4 shows us the typical video circuitry of a transistor black and white television. Our basic circuit consists of a diode detector, a unity gain emitter follower, and a variable gain video output stage that is capacitively coupled to the picture tube. The cathode bias sets the brightness, while the video gain sets the contrast. Amplified signals for sync and sound are removed from the collector of the video driver by way of a 4.5 MHz resonant transformer for the sound and a low pass filter for the sync. A parallel resonant trap set to 4.5 MHz eliminates sound interference. Peaking coils on each stage extend the bandwidth by providing higher impedances

and thus higher gain to high frequency video signals.

Note particularly the biasing of the video driver. A bias network provides us with a stable source of 3 volts. In the absence of input video, this 3 volts sets the white level of the display, as well as establishing proper bias for both stages. As an increasing signal appears at the last video output transformer, it is negatively rectified by the video detector, thus lowering the 3 volts proportionately. The stronger the signal, the blacker the picture. Sync will be the strongest of all, giving us a blacker than black bias level of only one volt.

The base of our video driver has the right sensitivity we need for video entry,

accepting a maximum of a 2 volt peak to peak signal. It also has the right polarity, for a positive going bias level means a whiter picture. *But, an unmodified set is already biased to the white level, and if we want to enter our own video, this bias must be shifted to the black level.*

We have a choice in any TV of direct or ac coupling of our input video. Direct coupling is almost always better as it eliminates any

Fig. 4. Typical video circuitry of transistor B and W TV set.

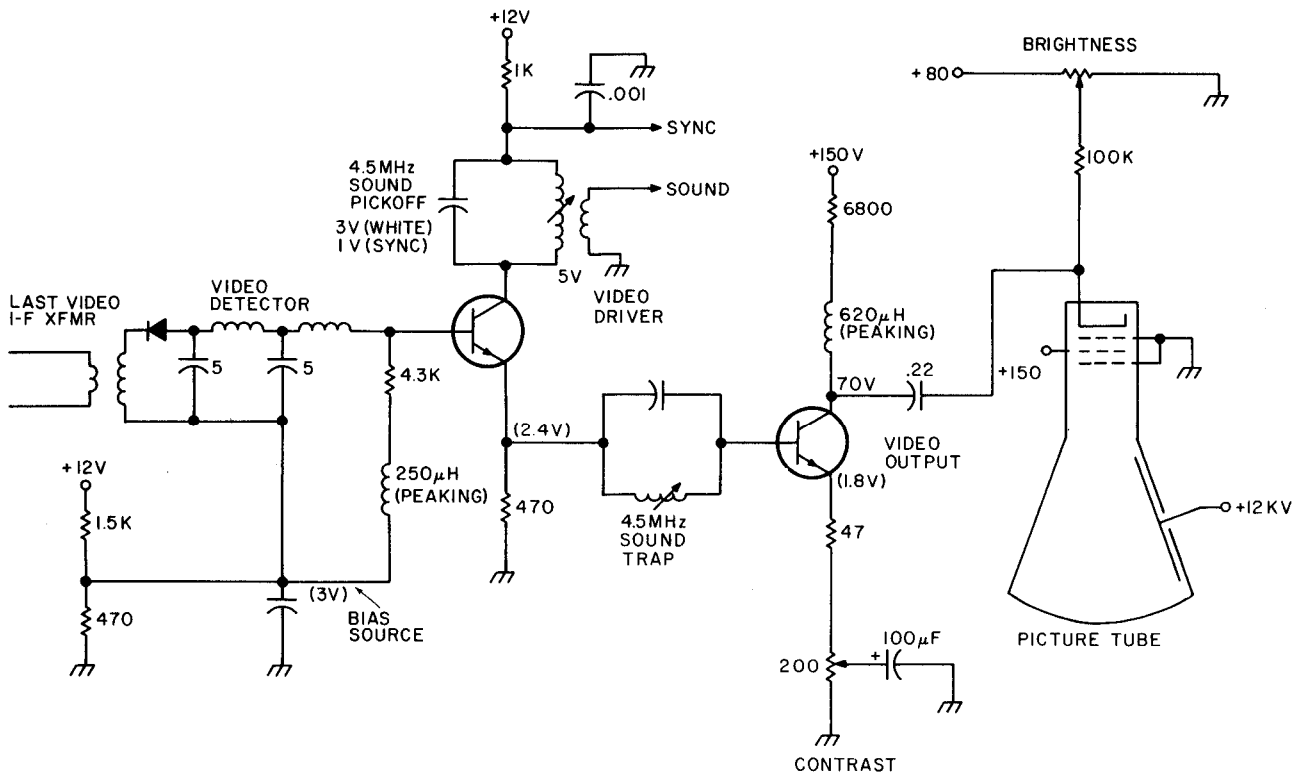
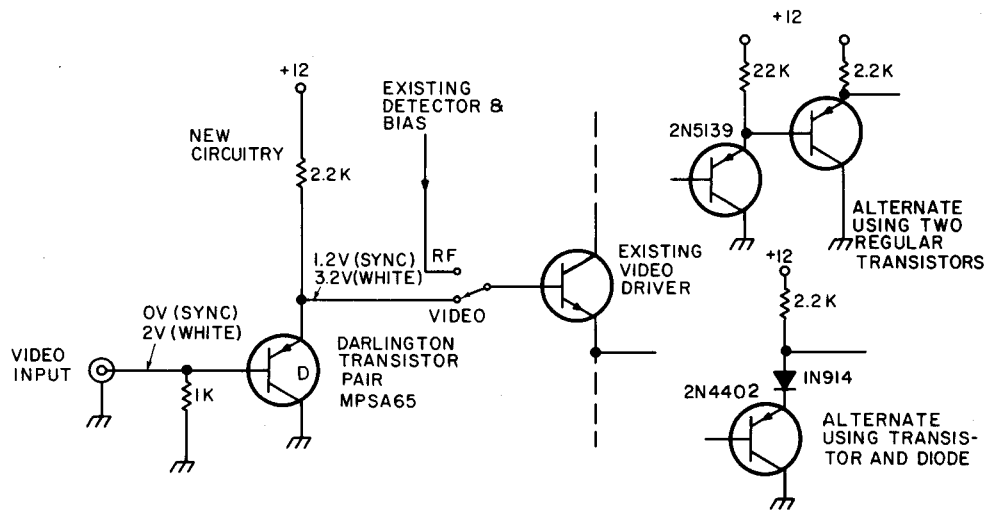


Fig. 5. Direct coupled video uses 1.2 volt offset of Darlington transistor as bias.

shading effects or any change of background level as additional characters are added to the screen. Fig. 5 shows how we can direct couple our video into a transistor black and white set. We provide a video input, usually a BNC or a phono jack, and route this to a PNP Darlington transistor or transistor pair, borrowing around 5 mils from the set's +12 volt supply. This output is routed to the existing video driver stage through a SPDT switch that either picks the video input or the existing video detector and bias network.

The two base-emitter diode drops in our Darlington transistor add up to a 1.2 volt positive going offset; so, in the absence of a video input or at the base of a sync tip, the video driver is biased to a blacker than black sync level of 1.2 volts. With a white video input of 2 volts, the video driver gets biased to its usual 3.2 volts of white level. Thus, our input transistor provides just the amount of offset we need to match the white and black bias levels of our video driver. Note that the old bias network is on the other side of the switch and does nothing in the video position.

Two other ways to offset our video input are to use two ordinary transistors connected in the Darlington configuration, or to use one transistor and a series diode



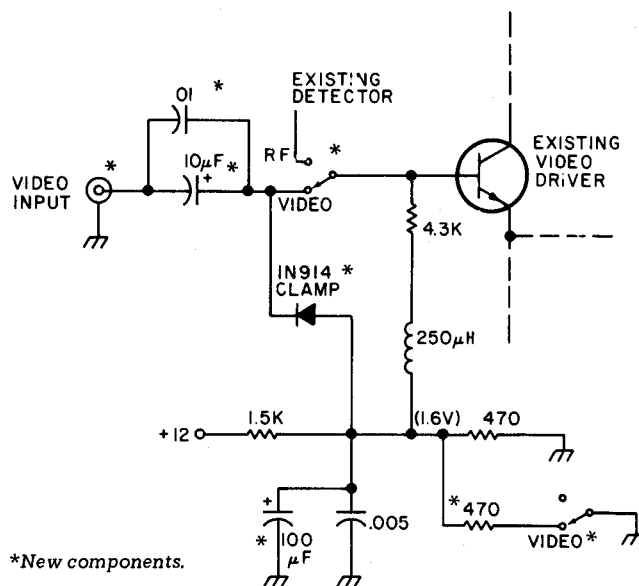
to pick up the same amount of offset, as shown in Fig. 5. If more or less offset is needed, diodes or transistors can be stacked up further to pick up the right amount of offset.

The important thing is that the video driver ends up with the same level for white bias and for black bias in either position of the switch.

Ac or capacitively coupled video inputs should be avoided. Fig. 6 shows a typical circuit. The TV's existing bias network is lowered in voltage by adding a new parallel resistor to ground to give us a voltage that is 0.6 volts more positive than the blacker than black sync tip voltage. For instance, with a 3 volt white level, and

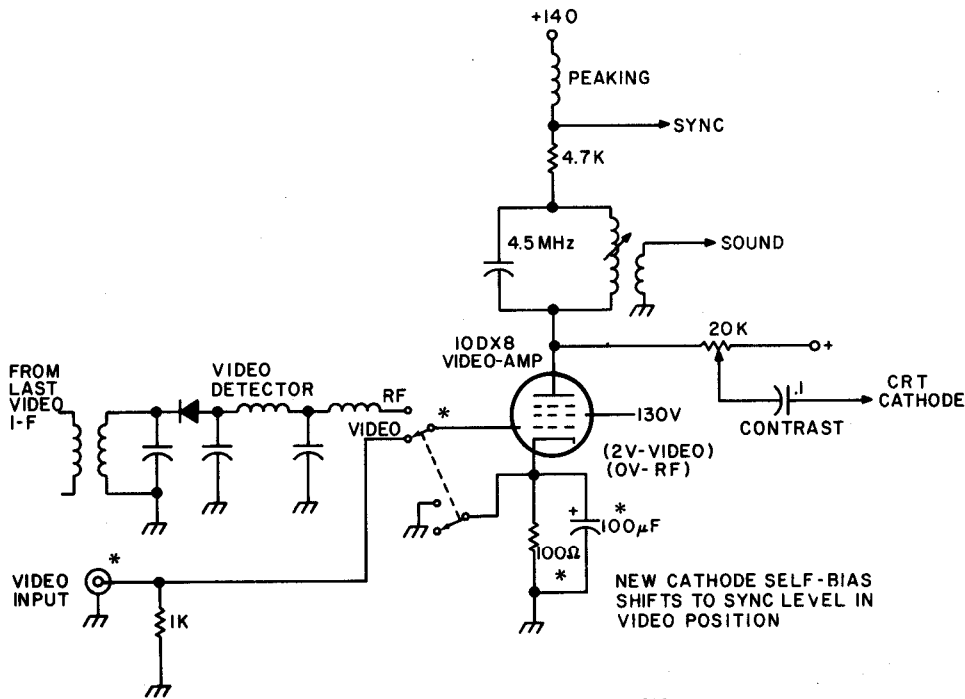
2 volt peak to peak video, the sync tip voltage would be 1 volt; the optimum bias is then 1.6 volts. Input video is capacitively coupled by a fairly large electrolytic capacitor in parallel with a good high frequency capacitor. This provides for a minimum of screen shading and still couples high frequency signals properly. A clamping diode constantly clamps the sync tips to their bias value, with the 0.6 volt drop of this diode being taken out by the extra 0.6 volts provided for in the bias network. This clamping diode automatically holds the sync tips to their proper value, regardless of the number of white dots in the picture. Additional bypassing of the bias network by a large electrolytic may be needed for proper operation of the clamping diode, as shown in Fig. 6. Note that our bias network is used in both switch positions — its level is shifted as needed for the direct video input.

Fig. 6. Ac coupled video needs shift of bias to black level plus a clamping diode.



*New components.

Fig. 7. Direct coupled video added to tube type B and W television.



*New components.

circuit, the white level is zero volts and the sync tip black level is minus two volts. If we can find a negative supply (scarce in tube type circuits), we could offset our video in the negative direction by two volts to meet these bias levels.

Instead of this, it is usually possible to self bias the video amplifier to a cathode voltage of +2 volts. This is done by breaking the cathode to ground connection and adding a small resistor (50 to 100 Ohms) between cathode and ground to get a cathode voltage of +2 volts. Once this value is found, a heavy electrolytic bypass of 100 microfarads or more is placed in parallel with the resistor. Switching then grounds the cathode in the normal rf mode and makes it +2 volts in the video entry mode.

In the direct video mode, a sync tip grounded input presents zero volts to the grid, which is self biased

minus two volts with respect to the cathode. A white level presents +2 volts to the grid, which equals zero volts grid to cathode.

Should there already be a self bias network on the cathode, it is increased in value as needed to get the black rather than white level bias in the direct video mode.

Hot Chassis Problems

There is usually no shock hazard when we use clip-on rf entry or when we use a direct video jack on a transformer-powered TV. A very severe shock hazard can exist if we use direct video entry with a TV set having one side of the

power line connected to the chassis. Depending on which way the line cord is plugged in, there is a 50-50 chance of the hot side of the power line being connected directly to the chassis.

Hot chassis sets, particularly older, power hungry tube versions, should be avoided entirely for direct video entry. If one absolutely must be used, some of the suggestions of Fig. 8 may ease the hazard. These include using an isolation transformer, husky back-to-back filament transformers, three wire power systems, optical coupling of the video input,

and total package isolation. Far and away the best route is simply never to attempt direct video entry onto a hot chassis TV.

Making the Conversion

Fig. 9 sums up how we modify a TV for direct video entry. Always have a complete schematic on hand, and use a transformer style TV set if at all possible. Late models, small screen, medium to high quality solid state sets are often the best display choice. Avoid using junk sets, particularly very old ones. Direct coupling of video is far preferable to ac capacitor coupling. Either method has to maintain the black and white bias levels on the first video amplifier stage. A shift of the first stage quiescent bias from normally white to normally black is also a must. Use short, shielded leads between the video input jack and the rest of the circuit. If a changeover switch is used, keep it as close to the rest of the video circuitry as you possibly can.

Extending Video and Display Bandwidth

By using the direct video input route, we eliminate any bandwidth and response restrictions of an rf

modulator, the tuner, video i-f strip, and the video-detector filter. Direct video entry should bring us to a 3 MHz bandwidth for a color set and perhaps 3.5 MHz for a black and white model, unless we are using an extremely bad set. The resultant 6 to 7 million dot per second rate is adequate for short character lines of 32, 40, and possibly 48 characters per line. But the characters will smear and be illegible if we try to use longer line lengths and premium (lots of dots) character generators on an ordinary TV. Is there anything we can do to the set to extend the video bandwidth and display response for these longer line lengths?

In the case of a color TV, the answer is probably no. The video response of a color set is limited by an essential delay line and an essential 3.58 MHz trap. Even if we were willing to totally separate the chrominance and luminance channels, we'd still be faced with an absolute limit set by the number of holes per horizontal line in the shadow mask of the tube. This explains why video color displays are so expensive and so rare. Later on, we'll look at what's involved in adding color to the shorter line lengths.

With a black and white TV, there is often quite a bit

Fig. 8. Getting Around a Hot Chassis Problem.

Hot chassis problems can be avoided entirely by using only transformer-powered TV circuits or by using clip-on rf entry. If a hot chassis set must be used, here are some possible ways around the problem:

1. Add an isolation transformer.

A 110 volt to 110 volt isolation transformer whose wattage exceeds that of the set may be used. These are usually expensive, but a workable substitute can be made by placing two large surplus filament transformers back to back. For instance, a pair of 24 volt, 4 Amp transformers can handle around 100 Watts of set.

2. Use a three wire system with a solid ground.

Three prong plug wiring, properly polarized, will force the hot chassis connection to the cold side of the power line. This protection is useful only when three wire plugs are used in properly wired outlets. A severe shock hazard is reintroduced if a user elects to use an adaptor or plugs the system into an unknown or improperly wired outlet. The three wire system should **NOT** be used if anyone but yourself is ever to use the system.

3. Optically couple the input video.

Light emitting diode-photocell pairs are low in cost and can be used to optically couple direct video, completely isolating the video input from the hot chassis. Most of these optoelectronic couplers do not have enough bandwidth for direct video use; the Litronix IL-100 is one exception. Probably the simplest route is to use two separate opto-isolators, one for video and one for sync, and then recombine the signals inside the TV on the hot side of the circuit.

4. Use a totally packaged and sealed system.

If you are only interested in displaying messages and have no other input/output devices, you can run the entire circuit hot chassis, provided everything is sealed inside one case and has no chassis-to-people access. Interface to teletypes, cassettes, etc., cannot be done without additional isolation, and servicing the circuit presents the same shock hazards that servicing a hot chassis TV does.

we can do to present long lines of characters, depending on what set you start out with and how much you are willing to modify the set.

The best test signal you can use for bandwidth extension is the dot matrix data you actually want to display, for the frequency response, time delay, ringing, and overshoot all get into the act. What we want to end up with is a combination that gives us reasonably legible characters.

A good oscilloscope (15 MHz or better bandwidth) is very useful during bandwidth extension to show where the signal loses its response in the circuit. At any time during the modification process, there is usually one response bottleneck. This, of course, is what should be attacked first. Obviously the better a TV you start with, the easier will be the task. Tube type gutless wonders, particularly older ones, will be much more difficult to work with than with a modern, small screen, quality solid state portable.

Several of the things we can do are watching the control settings, getting rid of the sound trap, minimizing circuit strays, optimizing spot size, controlling peaking, and shifting to higher current operation. Let's take a look at these in turn.

Control Settings

Always run a data display at the lowest possible contrast and using only as much brightness as you really need. In many circuits, low contrast means a lower video amplifier gain, and thus less of a gain-bandwidth restriction.

Eliminate the Sound Trap

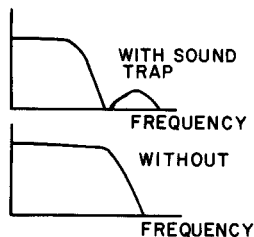
The sound trap adds a notch at 4.5 MHz to the video response. If it is eliminated or switched out of the circuit, a wider video bandwidth automatically

Fig. 9. How to Add a Direct Video Input to a TV Set.

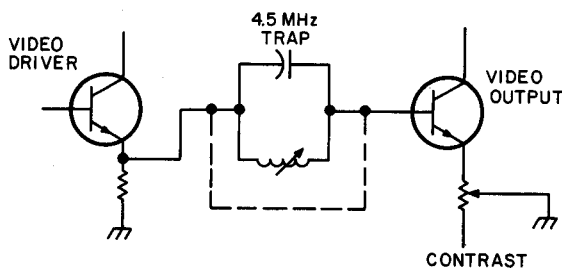
1. Get an accurate and complete schematic of the set — either from the manufacturer's service data or a Photofact set. **Do not try adding an input without this schematic!**
2. Check the power supply to see if a power transformer is used. If it is, there will be no shock hazard, and the set is probably a good choice for direct video use. If the set has one side of the power line connected to the chassis, a severe shock hazard exists, and one of the techniques of Fig. 8 should be used. **Avoid the use of hot chassis sets.**
3. Find the input to the first video amplifier stage. Find out what the white level and sync level bias voltages are. The marked or quiescent voltage is usually the white level; sync is usually 2 volts less. A transistor TV will typically have a +3 volt white level and a +1 volt sync level. A tube type TV will typically have a zero volt white level and a -2 volt sync level.
4. Add a changeover switch using minimum possible lead lengths. Add an input connector, either a phono jack or the premium BNC type connector. Use shielded lead for interconnections exceeding three inches in length.
5. Select a circuit that couples the video and biases the first video amplifier stage so that the white and sync levels are preserved. For transistor sets, the direct coupled circuits of Fig. 5 may be used. For tube sets, the circuit of Fig. 7 is recommended. Avoid the use of ac coupled video inputs as they may introduce shading problems and changes of background as the screen is filled.
6. Check the operation. If problems with contrast or sync tearing crop up, recheck and adjust the white and sync input levels to match what the set uses during normal rf operation. Note that the first video stage must be biased to the **white** level during rf operation and to the **sync** level for direct video use. The white level is normally two volts more positive than the sync level.

Fig. 10. Removing the sound trap can extend video bandwidth.

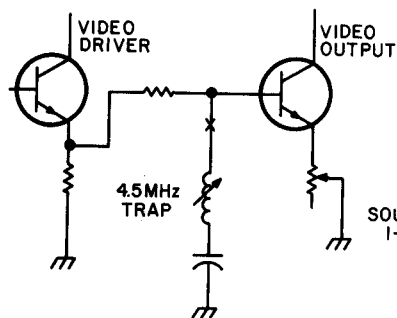
(a) Response



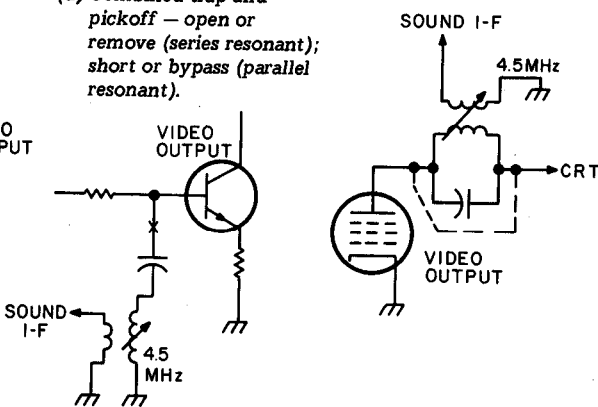
(b) Parallel resonant trap — short or bypass.



(c) Series resonant trap — open or remove.



(d) Combined trap and pickoff — open or remove (series resonant); short or bypass (parallel resonant).



results. Fig. 10 shows us the response changes and the several positions for this trap. Generally, series resonant traps are opened and parallel resonant traps are shorted or bypassed through suitable switching or outright elimination. The trap has to go back into the circuit if the set is ever again used for ordinary program reception. Sometimes simply backing the slug on the trap all the way out will improve things enough to be useful.

Minimizing Strays

One of the limits of the video bandwidth is the stray capacitance both inside the video output stage and in the external circuitry. If the contrast control is directly in the signal path and if it has long leads going to it, it may be hurting the response. If you are using the TV set exclusively for data display, can you rearrange the control location and simplify and shorten the video output to picture tube interconnections?

Additional Peaking

Most TV sets have two peaking networks. The first of these is at the video detector output and compensates for the vestigial sideband transmission signal that makes sync and other

low frequency signals double the amplitude of the higher frequency ones. The second of these goes to the collector or plate of the video output stage and raises the circuit impedance and thus the effective gain for very high

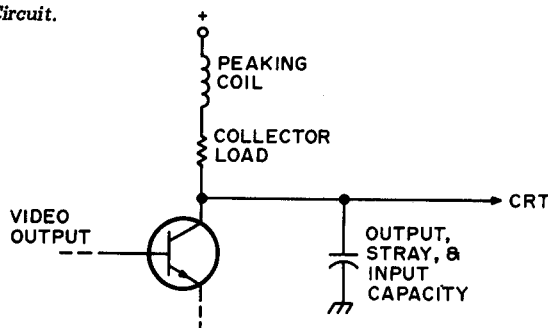
frequencies. Sometimes you can alter this second network to favor dot presentations. Fig. 11 shows a typical peaking network and the effects of too little or too much peaking. Note that the stray capacitance also enters into the peaking, along with the video amplifier output capacitance and the picture tube's input capacitance. Generally, too little peaking will give you low contrast dots, while too much will give you sharp dots, but will run dots together and shift the more continuous portions of the characters objectionably. Peaking is changed by increasing or decreasing the series inductor from its design value.

Running Hot

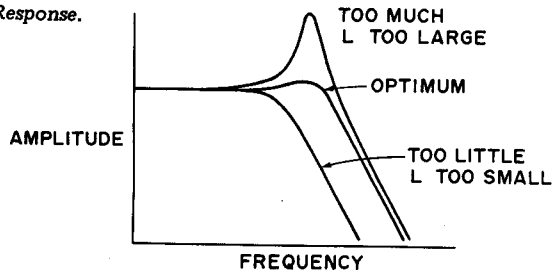
Sometimes increasing the operating current of the video output stage can increase the system bandwidth — IF this stage is in fact the limiting response, IF the power supply can handle the extra current, IF the stage isn't already parked at its gain-bandwidth peak, and IF the extra heat can be gotten rid of without burning anything up. Usually, you can try adding a resistor three times the plate or collector load resistor in parallel, and see if it increases bandwidth by 1/3. Generally, the higher the current, the wider the bandwidth, but watch

Fig. 11. Adjusting the peaking coil can extend video response.

(a) Circuit.



(b) Response.



carefully any dissipation limits. Be sure to provide extra ventilation and additional heatsinking, and check the power supply for unhappiness as well. For major changes in operating current, the emitter resistors and other biasing components should also be proportionately reduced in value.

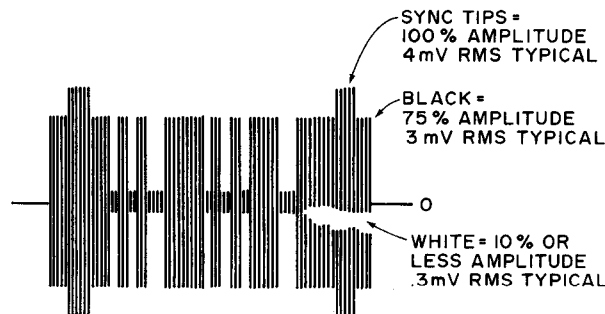
Spot Size

Even with excellent video bandwidth, if you have an out-of-focus, blooming, or changing spot size, it can completely mask character sharpness. Spot size ends up the ultimate limit to resolution, regardless of video bandwidth.

Once again, brightness and contrast settings will have a profound effect, with too much of either blooming the spot. Most sets have a focus jumper in which ground or a positive voltage is selected. You can try intermediate values of voltage for maximum sharpness. Extra power supply filtering can sometimes minimize hum and noise modulation of the spot.

Anything that externally raises display contrast will let you run with a smaller beam current and a sharper spot. Using circularly polarized filters, graticule masks, or simple colored filters can

Fig. 13. Standard rf interface levels. Impedance = 300Ω Carrier frequency per Fig. 14.



minimize display washout from ambient lighting. Fig. 12 lists several sources of material for contrast improvement. Much of this is rather expensive, with pricing from \$10 to \$25 per square foot being typical. Simply adding a hood and positioning the display away from room lighting will also help and is obviously much cheaper.

Direct Rf Entry

If we want the convenience of a "free" display, the freedom from hot chassis problems, and "use it anywhere" ability, direct rf entry is the obvious choice. Its two big limitations are the need for FCC type approval, and a limited video bandwidth that in turn limits the number of characters per line and the number of dots per character.

An rf interface standard is shown in Fig. 13. It consists of an amplitude modulated carrier of one of the standard television channel video frequencies of Fig. 14. Channel 2 is most often used

with a 55.250 MHz carrier frequency, except in areas where a local commercial Channel 2 broadcast is intolerably strong. Circuit cost, filtering problems, and stability problems tend to increase with increasing channel number.

The sync tips are the strongest part of the signal, representing 100% modulation, often something around 4 millivolts rms across a 300 Ohm line. The black level is 75% of the sync level, or about 3 millivolts for 4 millivolt sync tips. White level is less than 10% of maximum. Note that the signal is weakest when white and strongest when sync. This is the exact opposite of the video interface of Fig. 1.

Rf modulators suitable for clip-on rf entry TV typewriter use are called Class 1 TV Devices by the FCC. A Class 1 TV device is supposed to meet the rules and regulations summarized in Fig. 15.

Fig. 16 shows us a block diagram of the essential parts of a TV modulator. We start

Fig. 14. Television Picture Carrier Frequencies.

Channel 2	55.25 MHz
Channel 3	61.25 MHz
Channel 4	67.25 MHz
Channel 5	77.25 MHz
Channel 6	83.25 MHz

Fig. 15. FCC Regulations on Class 1 TV Devices. More complete information appears in subpart H of Part 15 and subpart F of Part 2 of the Federal Communications Commission Rules and Regulations. It is available at many large technical libraries.

A Class 1 TV device generates a video modulated rf carrier of a standard television channel frequency. It is directly connected to the antenna terminals of the TV set.

The maximum rms rf voltage must be less than 6 millivolts using a 300 Ohm output line.

The maximum rf voltage on any frequency more than 3 MHz away from the operating channel must be more than 30 dB below the peak in-channel output voltage.

An antenna disconnect switch of at least 60 dB attenuation must be provided.

No user adjustments are permitted that would exceed any of the above specifications.

Residual rf radiation from case, leads and cabinet must be less than 15 microvolts per meter.

A Class 1 TV device must not interfere with TV reception.

Type approval of the circuit is required. A filing fee of \$50 and an acceptance fee of \$250 is involved.

Fig. 12. Contrast Enhancing Filter Materials.

Circularly polarized filters:

Polaroid Corp.
Cambridge MA 02139

Anti-reflection filters:

Panelgraphic Corp.
10 Henderson Dr.
West Caldwell NJ 07006

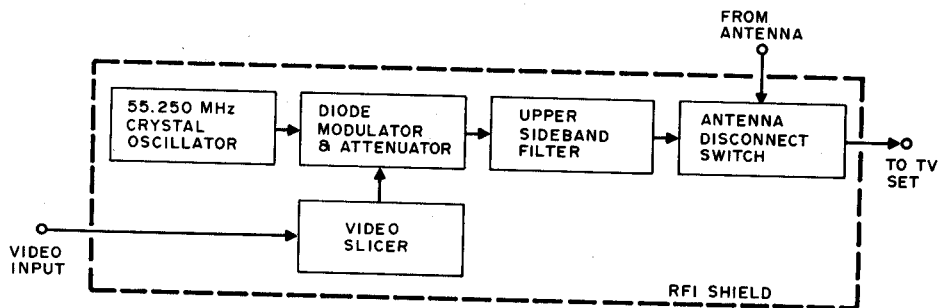
Light control film:

3M Visual Products Div.
3M Center
St. Paul MN 55101

Acrylic plexiglas filter sheets:

Rohm and Haas
Philadelphia PA 19105

Fig. 16. Block diagram of rf modulator.



with a stable oscillator tuned to one of the Fig. 14 frequencies. A crystal oscillator is a good choice, and low cost modules are widely available. The output of this oscillator is then amplitude modulated. This can be done by changing the bias current through a silicon small signal diode. One milliampere of bias current makes the diode show an ac and rf impedance of 26 Ohms. Half a mil will look like 52 Ohms, and so on. The diode acts as a variable resistance attenuator in the rf circuit, whose bias is set and changed by the video circuit.

Since diode modulators are non-linear, we can't simply apply a standard video signal to them and get a standard rf signal out. A differential amplifier circuit called a video slicer may be used to compensate for this non-linearity. The video slicer provides three distinct currents to the diode modulator. One of these is almost zero for the white level, while the other two provide the black and sync levels. A contrast control that sets the slicing level lets you adjust the sync tip height with respect to the black level. The video slicer also minimizes rf getting back into the video. An attenuator to reduce the size of the modulated signal usually follows the diode modulator.

An upper side band filter removes most of the lower sideband from the AM modulated output, giving us a

vestigial sideband signal that stays inside the channel band limits. This same filter eliminates second harmonic effects and other spurious noise. The filter's output is usually routed to an antenna disconnect switch and the TV's antenna terminals. A special switch is needed to provide enough isolation.

Some of the actual circuitry involved is shown in Fig. 17. The video slicer consists of a pair of high gain, small signal NPN transistors, while the oscillator is a commercially available module.

Rf entry systems always must be direct coupled to the antenna terminals of the set and should never provide any more rf than is needed for a minimum snow-free picture. They should be permanently tuned to a single TV channel. Under no circumstances should an antenna or cable service hookup remain connected to the set during TVT use, nor should radiation rather than a direct rf cable connection ever be used.

Color Techniques

We can add a full color capability to a TV typewriter system fairly easily and cheaply — provided its usual

black and white video dot rate is low enough in frequency to be attractively displayed on an ordinary color TV. Color may be used to emphasize portions of a message, to attract attention, as part of an electronic game, or as obvious added value to a graphics display. Color techniques work best on TV typewriter systems having a horizontal frequency very near 15,735 Hertz.

All we basically have to do is generate a subcarrier sine wave to add to the video

output. The phase of this subcarrier (or its time delay) is shifted with respect to what the phase was immediately after each horizontal sync pulse to generate the various colors.

Fig. 18 shows us the differences between normal color and black and white operation. Black and white baseband video is some 4 MHz wide and has a narrow 4.5 MHz sound subcarrier. The video is amplitude modulated, while the sound is narrow band frequency

Fig. 17. Channel two oscillator, modulator, video slicer and attenuator. R sets output level.

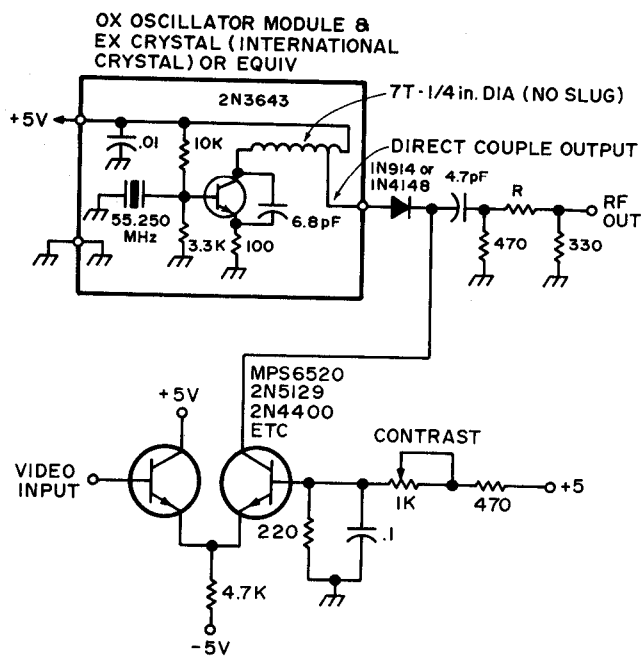
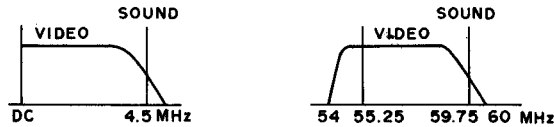


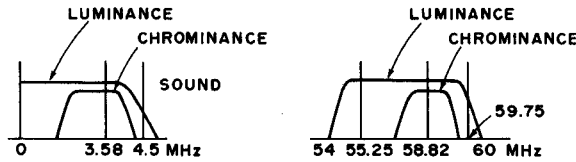
Fig. 18. Differences between color and black and white spectra.

(a) Black and white – baseband video.



(b) Black and white – Channel two rf.

(c) Color – baseband video.



(d) Color – Channel two rf.

modulated. This translates up to a 6 MHz rf channel with a vestigial lower sideband as shown in Fig. 18(b).

To generate color, we add a new pilot or subcarrier at a magic frequency of 3.579545 MHz – see Fig. 18(c). What was the video is now called the luminance, and is the same as the brightness in a black and white system. The new subcarrier and its modulation is called the chrominance signal and determines what color gets displayed and how saturated the color is to be.

Since the black and white information is a sampled data system that is scanned at the vertical and horizontal rates, there are lots of discrete holes in the video spectrum that aren't used. The color subcarrier is designed to stuff itself into these holes (exactly in a NSTC color system, and pretty much in a TVT display). Both chrominance and luminance signals use the

same spectral space, with the one being where the other one isn't, overlapping comb style.

The phase or relative delay of the chrominance signal with respect to a reference determines the instantaneous color, while the amplitude of this signal with respect to the luminance sets the saturation of the color. Low amplitudes generate white or pastel shades, while high amplitudes of the chrominance signal produce saturated and deep colors.

At least eight cycles of a reference or burst color phase are transmitted immediately following each horizontal sync pulse as a timing reference, as shown in Fig.

19. The burst is around 25% of maximum amplitude, or about the peak to peak height of a sync pulse.

The TV set has been trained at the factory to sort all this out. After video detection, the set splits out the chrominance channel with a bandpass amplifier and then synchronously demodulates it with respect to an internal 3.58 MHz reference. The phase of this demodulation sets the color and the amplitude sets the saturation by setting the

ratios of electron beam currents on the picture tube's red, blue and green guns.

Meanwhile, the luminance channel gets amplified as brightness style video. It is delayed with a delay line to make up for the time delay involved in the narrower band color processing channel. It is then filtered with two traps – the 4.5 MHz sound trap, and a new trap to get rid of any remaining 3.58 MHz color subcarrier that's left. The luminance output sets the overall brightness by modulating the cathodes of all three color guns simultaneously.

Just after each horizontal sync pulse, the set looks for the reference burst and uses this reference in a phase

Fig. 19 Adding a color reference burst to the back porch of the horizontal sync pulses.

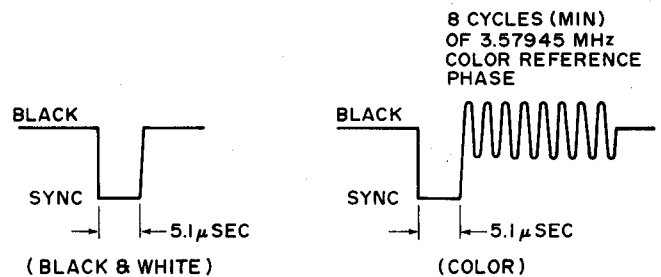


Fig. 20. Colors Are Generated by Delaying or Phase Shifting the Burst Frequency.

Color	Approximate Phase	Approximate Delay
Burst	0°	0
Yellow	15°	12 nanoseconds
Red	75°	58 nanoseconds
Magenta	135°	105 nanoseconds
Blue	195°	151 nanoseconds
Cyan	255°	198 nanoseconds
Green	315°	244 nanoseconds

detector circuit to keep its own 3.58 MHz reference locked to the version being transmitted.

Fig. 20 shows us the phase angles related to each color with respect to the burst phase. It also shows us the equivalent amount of delay we need for a given phase angle. Since we usually want only a few discrete colors, it's far easier to digitally generate colors simply by delaying the reference through gates or buffers, rather than using complex and expensive analog phase shift methods.

Strictly speaking, we should control both the chrominance phase and amplitude to be able to do both pastel and strongly saturated colors. But simply keeping the subcarrier amplitude at the value we used for the burst — around 25% of video amplitude — is far simpler and will usually get us useful results.

A circuit to add color to a TV typewriter is shown in Fig. 21. A 3.579545 MHz crystal oscillator drives a string of CMOS buffers that make up a digital delay line. The output delays caused by the propagation delay times in each buffer can be used as

is, or can be trimmed to specific colors by varying the supply voltage.

The reference phase and the delayed color outputs go to a one-of-eight data selector. The data selector picks either the reference or a selected color in response to a code presented digitally to the three select lines. The logic that is driving this selector must return to the

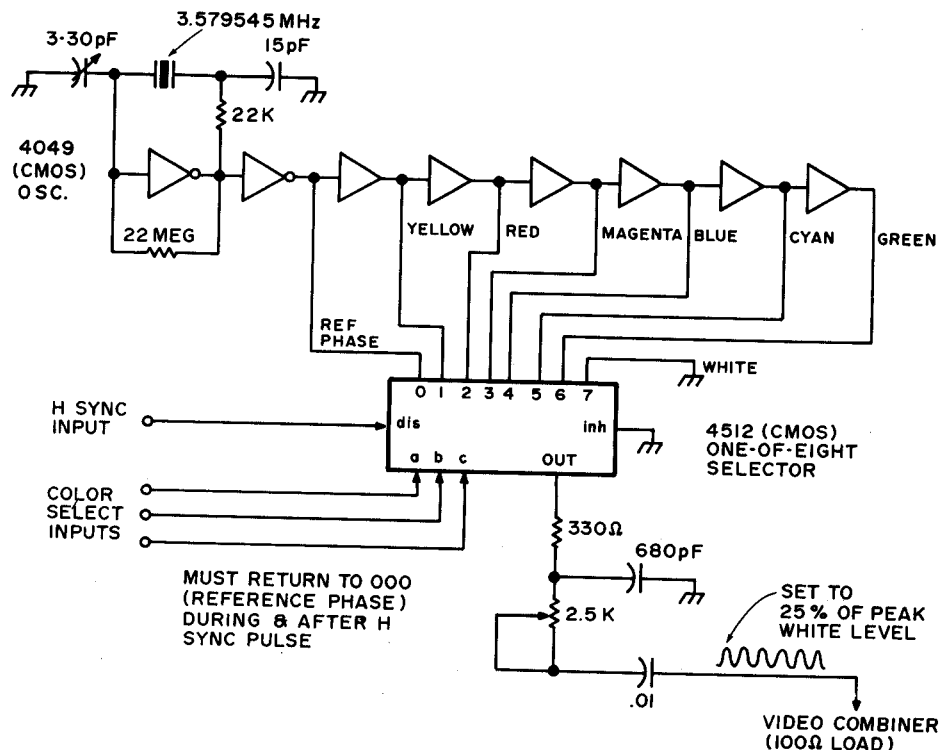
reference phase position (000) immediately before, during and for a minimum of a few microseconds after each horizontal sync pulse. This gives the set a chance to lock and hold onto the reference color burst.

The chrominance output from the data selector should be disabled for the duration of the sync pulses and any time a white screen display is

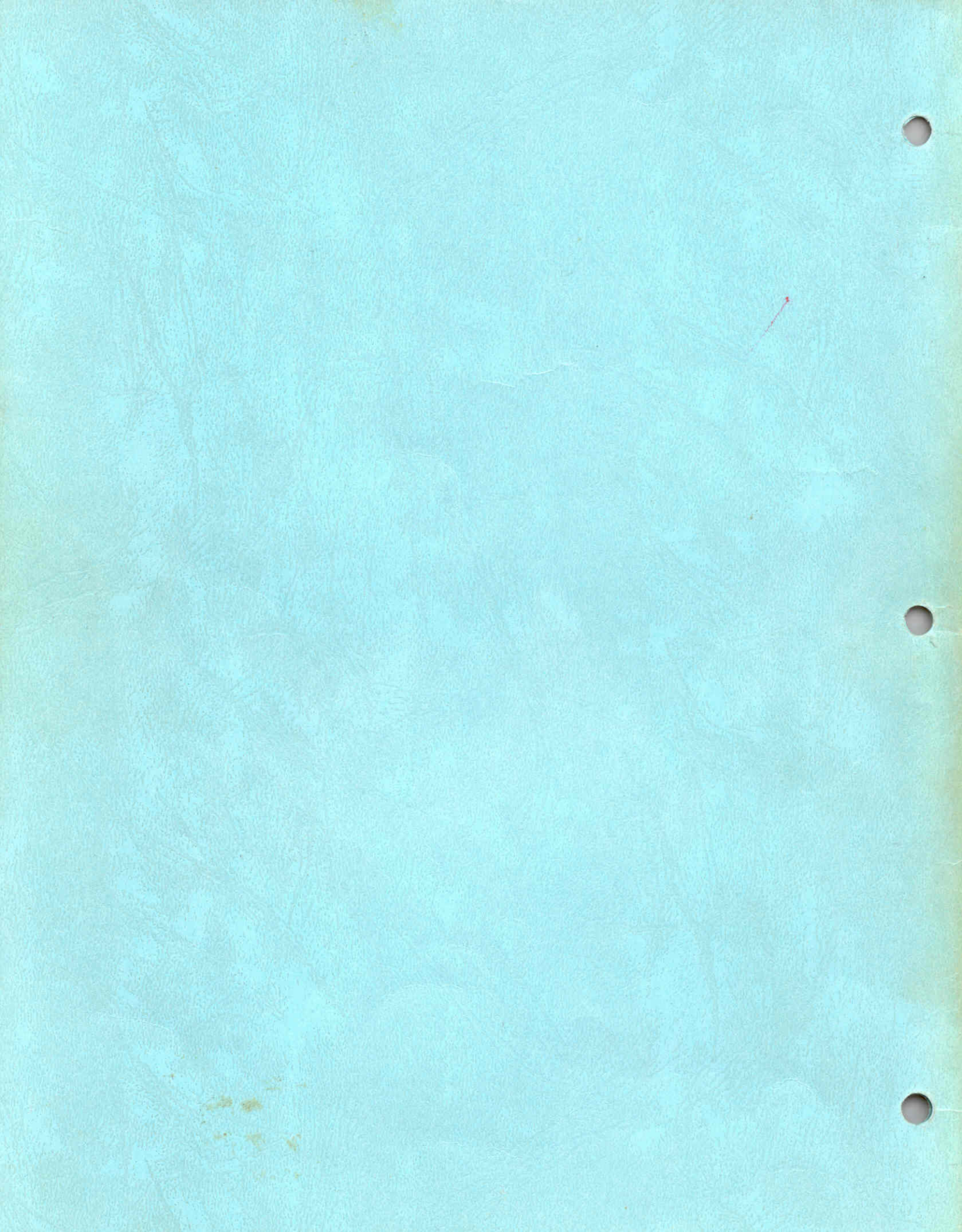
wanted. The output chrominance signal is RC filtered to make it somewhat sinusoidal. It's then cut down in amplitude to around one-quarter the maximum video white level and is capacitively coupled to the 100 Ohm video output of Fig. 2 or otherwise summed into the video or rf modulator circuitry. For truly dramatic color effects, the amplitude and delay of the chrominance signal can be changed in a more complex version of the same circuit.

More information useful in solving television interface appears in the *Television Engineering Handbook*, by Donald Fink, and in various issues of the *IEEE Transactions on Consumer Electronics*.

Fig. 21. Color subcarrier generator. Hex buffer used as delay line. Use supply voltage variation on 4050 to trim colors.







Received: 77 Oct 17

Maybe it's just my imagination, but it seems that a lot of people aren't utilizing the Z-80 to its fullest. Everyone is so used to writing code for the 8080 that they don't seem to bother upgrading their software when they upgrade their CPU. Or maybe, as in my case, since we've been eating and sleeping in Intel Octal for so long that we just can't seem to catch on to all the enhancements of the added Z-80 functions and instructions. I would like to see you guys (or, someone else) come out and explain all the nifty Z-80 tricks. I know I can't be the only one that is stuck in the rut of 8080 code. (Please!! Don't tell me I swapped my CPU board JUST for speed—the software potential is fantastic.)

Michael Settle 751 Washington #115
Arlington, TX 76011

How about it? Anyone care to send us something on "Taking full advantage of Z-80's inner mysteries"?—TRW

MICROCOMPUTER SOFTWARE INDEX

News Release

Received 77 Nov 28

A great quantity of software has been published in micro-computer books and magazines since late 1975. These programs range from complete BASICs to assemblers, routines, games and direct application programs.

The Schreier Software Index, An Index to Published Micro-computer Software, indexes hundreds of published micro-computer programs. The S S I contains cross references and over 130 program divisions. Many of the cited programs specify chip description. In addition, the S S I features complete publication documentation and bibliographic data. Locating a random number routine for a 6800 or an 8080, for example, takes but seconds.

Direct orders may be placed with S S I, 4327 East Grove Street, Phoenix, Arizona 85040. Price postpaid in the United States, Mexico and Canada is \$5.00. The S S I is also available from a number of microcomputer dealers across the U.S.

THESE CHANGES WERE ADDED TO SAVE THE Y REGISTER WHEN CALLING HIM ROUTINES OUTHC & PITYXT

```
KIM
C3DC 20 G
C3DC- 20 00 02 JSF 5C200 begin
C3DF- 40 4F 10 JNP 51C4F start
C3E2- 84 EE STY SEE savey
P3E4- 20 A0 1E JST 51EAC outhc
C3E7- A4 EE LDY 51EE gety
C3E9- 60 FTS
C3EA- 84 EE STY SEE savey
C3EC- 20 3E 1E JSF 51E3E prtbyt
C3EF- A4 EE LDY SEE gety
C3F1- 60 ITS
```

THESE ARE THE TABLES

```
KIM
C3DC 20 44
C344 F2 DC.
C345 03 3DC
C3LC 20 17F7
17F7 FF DC. end of tables
17F8 FF 03.
17F9 LA C300 start of tables
C300 45 C
:1B03C045C3D0C840C9C0224533D00E40C940C24533D0F0E402040C00E58A
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Received: 77 Dec 2

```
0005 * THIS IS THE VDM-1 DRIVER ORIGINATED
0010 * BY LI CHEN WANG (DR. DOBB'S JOURNAL,
0015 * VOLUME #1, ISSUE #6).
0020 *
0025 * MODIFIED TO INCLUDE SPEED CONTROL AND
0030 * GENERALLY EMULATE THE SOFTWARE DRIVER FOR
0035 * PROCESSOR TECHNOLOGY'S VDM-1 VIDEO DISPLAY.
0040 * THIS PROGRAM WILL ALSO ACT AS THE DRIVER
0045 * FOR SOLID STATE MUSIC'S VB-1 DISPLAY.
0050 *
0055 * WRITTEN BY JOHN MOORHEAD, 928 J STREET,
0060 * DAVIS, CA. 95616 TEL NO 916-758-2495
0065 *
0070 * MAY 5, 1977
0075 *
0080 * BACKSPACE = CONTROL H OR B.S. KEY
0085 * SCREEN CLEAR = "CANCEL" = CTRL-X
0090 * AUTO CRLF ON INPUT OF A CARRIAGE RETURN
0095 * CHANGE SPEED BY TYPING NUMBER DURING OUTPUT
0100 * STOP DISPLAY BY TYPING SPACE BAR
0105 * START DISPLAY BY TYPING ANY CHARACTER
0110 *
0115 * NOTE - A SCREEN CLEAR MUST BE THE FIRST
0120 * CHARACTER SENT IN ORDER TO INITIALIZE THE
0125 * CURSOR AT THE BOTTOM LEFT CORNER OF THE
0130 * SCREEN AND ENSURE PROPER SCROLLING.
0135 *
0140 *
0145 * ENTER WITH CHARACTER IN THE ACCUMULATOR
0150 *
0155 *
0160 STRT PUSH H SAVE SYSTEM REGISTERS
0165 PUSH D
0170 PUSH B
0175 PUSH PSW CHAR IS IN THE ACCUM
0180 LHLD VDMP GET SCREEN POSITION POINTER
0185 CPI 0DH IS THE CHAR A CARRIAGE RET?
0190 JZ CR YES - SCROLL, OUTPUT A CR
0195 CPI 08H IS IT A BACKSPACE?
0200 JZ BS YES - MOVE CURSOR BACK
0205 CPI 18H IS IT A CTRL - X (SCREEN CLEAR)?
0210 JZ CLEAR YES - ERASE ENTIRE SCREEN
0215 CPI 7FH IS IT A RABOUT CHARACTER?
0220 JZ SPEED DON'T DISPLAY (FOR ALS-8 ONLY)
0225 CPI 20H DON'T DISPLAY CONTROL CHARS
0230 JC SPEED EXIT TO CHANGE SPEED
0235 MOV M,A IT HAS TO BE DATA
0240 INX H UPDATE CHAR POSITION ON SCREEN
0245 MVI M,0A0H PUT CURSOR ON SCREEN
0250 JMP LINOV TEST FOR LINE OVERFLOW
0255 BS MVI M,20H REMOVE CURSOR
0260 DCX H BACK UP POINTER
0265 JMP BS-5
0270 CR MVI M,20H CHAR IS A CARRIAGE RETURN
0275 MOV A,L UPDATE NEXT CHAR POSITION
0280 ANI 0COH
0285 ADI 40H SETTING UP FOR NEW LINE
0290 MOV L,A ADDRESS OF NEW LINE
0295 MVI A,0
0300 ADC H ADD WITH CARRY
0305 MOV H,A
0310 LINOV SHLD VDMP SAVE POINTER FOR NEXT CHAR
0315 MVI A,7FH
0320 ANA L
0325 JNZ SPEED EXIT
0330 MVI M,20H
0335 LXI H,0CFC0H SET UP DATA LINE (LINE 16)
0340 SHLD VDMP SAVE POINTER
0345 LXI H,0CC40H 15 LINES OF SCREEN DATA
0350 LXI D,0CC00H TOP OF SCREEN. SET UP
0355 LXI B,03COH TO SCROLL 15 LINES
0360 SCROL MOV A,M START SCROLLING UP
```

```

0365 STAX D
0370 INX H
0375 INX D
0380 DCX B COUNT DOWN
0385 XRA A
0390 CMP B 15 LINES SCROLLED?
0395 JNZ SCROL NOT YET COMPLETE
0400 CMP C
0405 JNZ SCROL STILL NOT COMPLETE
0410 LXI H,0CFC0H SET DATA LINE (LINE 16)
0415 ERASE MVI M,20H PUT BLANK ON SCREEN
0420 INX H ERASE ENTIRE DATA LINE
0425 MOV A,L
0430 ANI 3FH
0435 JNZ ERASE LINE NOT YET ERASED
0440 LXI H,0CFC0H SET DATA LINE (LINE 16)
0445 MVI M,0A0H PUT CURSOR ON SCREEN
0450 SPEED CALL STATS LOOK AT KEYBOARD STATUS BIT
0455 CNZ GETIT IF BUSY, GET ASCII DATA
0460 LDA NEWSP LOAD NEW SPEED BYTE
0465 MOV H,A CHANGE SPEED WITH ASCII 1-9
0470 MVI L,80H
0475 DELAY DCX H DELAY ROUTINE FOR
0480 MOV A,H VARIABLE OUTPUT SPEED
0485 ORA A
0490 JNZ DELAY JUMP FOR MORE TIME
0495 POP PSW DELAY COMPLETE
0500 POP B GET READY TO RETURN
0505 POP D TO USER PROGRAM
0510 POP H
0515 RET . RETURN
0520 GETIT CALL DATA INPUT ASCII DATA FROM KBD
0525 CPI '9'+1 IS THE CHAR AN ASCII 1-9?
0530 JNC WAIT TOO BIG
0535 CPI '1'
0540 JC WAIT TOO SMALL
0545 ANI 0FH REMOVE ASCII BIAS
0550 PUSH B SAVE REGISTER
0555 MOV C,A SAVE DELAY NUMBER
0560 XRA A CLEAR ACCUMULATOR
0565 STC . INITIALIZE DELAY CARRY BIT
0570 LESS DCR C DECREMENT DELAY NUMBER
0575 JZ FOUND STOP ROTATING DELAY BIT
0580 RAL . SHIFT DELAY BIT LEFT
0585 JMP LESS NEXT ROUND
0590 FOUND POP B RESTORE REGISTERS
0595 STA NEWSP
0600 RET
0605 WAIT CPI 20H IS IT A SPACE BAR?
0610 RNZ . NO - CONTINUE
0615 WAIT2 CALL STATS WAIT TILL A KEY IS PRESSED
0620 JZ WAIT2 TO CONTINUE SCREEN OUTPUT
0625 RET
0630 CLEAR LXI H,0CC00H CLEAR SCREEN
0635 MVI A,0DOH BOTTOM OF SCREEN CHECK
0640 CLER1 CMP H TEST FOR END OF SCREEN
0645 JZ DONIT YES - DONE
0650 MVI M,20H PUT BLANK ON SCREEN
0655 INX H CLEAR MORE SCREEN
0660 JMP CLER1
0665 DONIT LXI H,0CFC0H SET DATA LINE (LINE 16)
0670 MVI M,0A0H PUT CURSOR ON SCREEN
0675 SHLD VDMP SAVE POINTER TO DATA LINE
0680 XRA A
0685 OUT 0C8H CLEAR VDM-1 STATUS LATCH
0690 JMP SPEED
0695 VDMP DS 02H CURRENT CURSOR POSITION
0700 NEWSP DW 00H CURRENT OUTPUT SPEED
0705 *
0710 *
0715 * THESE ARE AUXILLIARY ROUTINES
0720 * FOR INPUT AND OUTPUT OF THE
0725 * DISPLAY SPEED INFORMATION FROM THE
0730 * KEYBOARD. THEY ARE NORMALLY
0735 * PART OF THE CALLING PROGRAM.
0740 *

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\$1250 MICROKIT ICE UNIT

news release

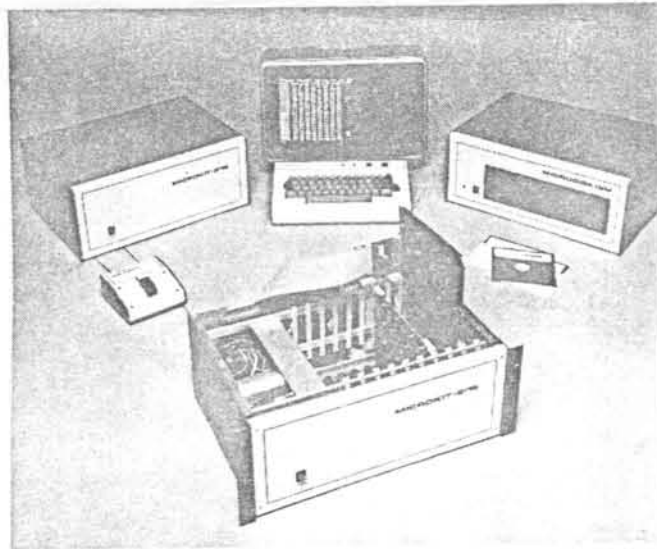
Received: 77 Ju

Los Angeles, California — Microkit, Inc., a leading manufacturer of ready-to-use, low-cost, universal microcomputer systems, has announced availability of a new in-circuit emulator/EPROM programmer.

The new MICROEMULATOR extends the editing, assembling and debugging capabilities of Microkits's 8086/8088/8080/Z-80 Product Development Systems directly into prototype or production system. The MICROEMULATOR probe plugs directly into a prototype's CPU socket and allows debugging of the prototype in its own environment. Programs residing in the microcomputer's RAM memory can execute and access the memory and I/O devices, emulating actual usage. In addition to basic monitor commands, provisions are made for enabling emulation mode, single step and trace execution, hardware breakpoints and 2708/2704 EPROM programming.

Applications include hardware/software development and integration, production test and depot maintenance of microprocessor systems. MICROEMULATORS are offered for 8080, 6800 or Z-80 microprocessors and are compatible with any of Microkit's tape-based or disk-based systems, including high-speed QUICKRUN "in-memory" operating systems which provide the only co-resident assembly and interactive debugging system in the industry.

The complete system package consisting of an M8-MICROEMULATOR and M8-41 Debug and EPROM programmer is priced at \$1250.00. Availability is from stock. Manufacturer: MICROKIT, INC., 11205 So. La Cienega Blvd., Los Angeles, CA 90045. Sales Contact: Bob Schaaf (213) 641-7700.



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0745 *
0750 STATS IN 00H INPUT FROM STATUS PORT
0755 ANI 40H LOOK AT KEYBOARD STATUS BIT
0760 RET .
0765 DATA IN 01H INPUT FROM DATA PORT
0770 ANI 7FH REMOVE PARITY BIT
0775 RET .

```