REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR		[illegible]	6/19/91

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTERS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED:
   U135, J26, C183, Y1, R244, E1
   CR14, DS4, JP6, SW2, TP13, K1, Q1
5. POWER AND GROUND:

REF.DES.	GND	+5V
U37-40, 42, 46 67, 68, 78, 99, 110	7	14
U41, 43, 44, 90, 93, 97, 98, 100, 111, 112	8	16
U50, 63-65, 91 92, 95, 96, 113	10	20
U60, 61	14	28
U62	16, 53	14, 49

6. UNUSED REFERENCE DESIGNATORS
   R107 - R199
7. ⏚ = DIGITAL GROUND

8 INSTALL THIS RESISTOR IF THE 68000 IS INSTALLED.
9 INSTALL THIS RESISTOR IF THE 68030 IS INSTALLED.

Note: The following configurations are valid for the PROM jumpers:
27256, JP4 (open)
27512, JP4 (1 to 2)

Note: The POWER ON initialization routine must provide a delay of 130 usec prior to using the dynamic memory. This delay insures that the memory's receive at least 8 CAS before RAS cycles before they are used.

Note: The Kernel test plug will not work with with most emulators. The input buffers in most emulators increase the loading such that the resistors cannot force the Moveq instruction on the bus properly.

Note: Any 68000 emulator which is used with this board must support continuous Address Strobe, otherwise the DRAM will NOT be refreshed.

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION REDMOND, WASH.
CHECKED: Kin Enshen	6-27-91	TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.
ENGR APP: [illegible]	6-27-91	
MECH CHK: P. Sandman	6-27-91	SIZE D / FSCM NO. 54193 / DRAWING NO. 30-701-2313
MFG CHK: [illegible]	6-27-91	
QUAL ASSUR: [illegible]	6-27-91	SCALE: NONE / [illegible] 6/27/91 / SHEET 1 OF 9

P/N: 701-2313-002

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91

FLOPPY DISK CONTROLLER

POWER-LOSS WRITE PROTECT

FSM INT ENABLE

PSM/FSM CHANGE DETECTOR

INTERRUPT CONTROLLER

POWER ON RESET

THIS CIRCUIT ALSO INSURES THE DISK DRIVE IS WRITE PROTECTED DURING POWER ON AND POWER OFF.

NOTE: THE 1N4623 WAS CHOOSEN FOR LOW LEAKAGE CURRENT AND SHOULD NOT BE SUBSTITUTED.

1.2V HYSTERESIS

FLOPPY DISK CONNECTOR

POWER AND GROUND:

REF.DES.	GND	+5V
U30	12	3
U36, 68, 73, 40, 119, 116, 114	7	14
U106, 75, 76, 105, 107, 117, 103	8	16
U104, 115	10	20
U102	14	15

UNUSED GATES:

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION REDMOND, WASH.	
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:			
MECH CHK:		SIZE D	FSCM NO. 54193
MFG CHK:		DRAWING NO. 30-701-2313	
QUAL ASSUR:		SCALE: NONE	SHEET 2

PIN CONTROL UNIT

PCU 4.C7

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91

PD 7.87
IPULSE
PCUINT-
68K 1.C2

PROGRAM COUNTER
74LS161A
INCADR
+5V
R74 750
TSTCLR
C181 150PF
R218 68
RWELO-
ROELO-
U26
U19
U27
74F08 U109
LDPCUA-
C182 150PF
R219 68
RWEHI-
ROEHI-

CONTROL STORE RAM
CY7C185A
U25
U29

74HCT244
U24
U104
PCU ADDRESS READBACK
RDPCUA-
PCURST-
BOARDREV
R75 180
CLK8

74LS299
U11
RDSHFT-
SERIAL READ REGISTER
R242 68
C173 150PF
PCUDLY

74HCT373
U49
U70

TIMER
CLK0.5 0.5Mhz (50/50 DUTY CYCLE)
CPUCLK 10Mhz (50/50 DUTY CYCLE)
CLK8 8Mhz (60/40 DUTY CYCLE)
CLK4 4Mhz (50/50 DUTY CYCLE)
CLK2 2Mhz (50/50 DUTY CYCLE)
CLK1 1Mhz (50/50 DUTY CYCLE)
CLOCK CONTROLLED BY PCU

CLOCK SELECTOR
74LS151
U69
MCLK
STRTPCU-
PUP1
RDPCUA-

PCUHOLD-
16R8A
U28
INSTRUCTION DECODER

74LS161A
U51
U52
U54
U72
U108
U71
FAST COUNTER
LOOK-AHEAD RIPPLE CARRY
74F10 U110
FAST
SLOW COUNTER

74LS574
U74
START/STOP TIMING GENERATOR
74F374
U17
CMP
BPCLK
(BUFFERED PCLK)

VCS/AEN TIMING GENERATOR
DAT/DLY
ADR/CNT
EVOKE-
74F174
U79
74F00 U78
74F08 U109
XAEN-
XVCS-
PCUHLT-
XPCLK
START-
INCADR

START PULSER
74LS74
U120

TEST POINTS
RCLK TP8
PCLK TP9
VCS TP10
PHLT TP11
TEST TP12

POWER AND GROUND:		
REF.DES.	GND	+5V
U53, 78, 110, 109, 120, 74	7	14
U19, 26, 52, 71, 27, 54, 72, 108	8	16
U11, 24, 17, 28, 49, 70, 104	10	20
U25, 29	12	24
U51, 79, 69	8	16

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION REDMOND, WASH.	
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:			
MECH CHK:		SIZE D	FSCM NO. 54193
MFG CHK:		DRAWING NO. 30-701-2313	
QUAL ASSUR:		SCALE: NONE	SHEET 3

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91

Note: The zener's, caps, and series resistors shown in the serial circuit provide ESD protection and reduce the EMI.

POWER AND GROUND:

REF.DES.	GND	+5V	+12V	-12V
U1, 2, 3	4		8	5
U8, 12, 13, 120	7	14		
U6, 7, 16	8	16		
U14	20	40		

DRAWN: Gerald Ryder	DATE: 1/4/91	DATA I/O CORPORATION	REDMOND, WASH.
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:		SIZE: D	FSCM NO.: 54193
MECH CHK:		DRAWING NO.: 30-701-2313	
MFG CHK:		SCALE: NONE	SHEET 4
QUAL ASSUR:			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91

PCU 3.02

68K 1.02

INTERNAL PIN DRIVER BUS IPD 8.B8

FSM PIN DRIVER BUS FPD 7.A8

PIN LOGIC READBACK BUFFER

OR READ DATA FROM FSM AND INTERNAL BUS

BUS TERMINATION

Note: R1, R2 shown above are located at the far end of the IPD bus

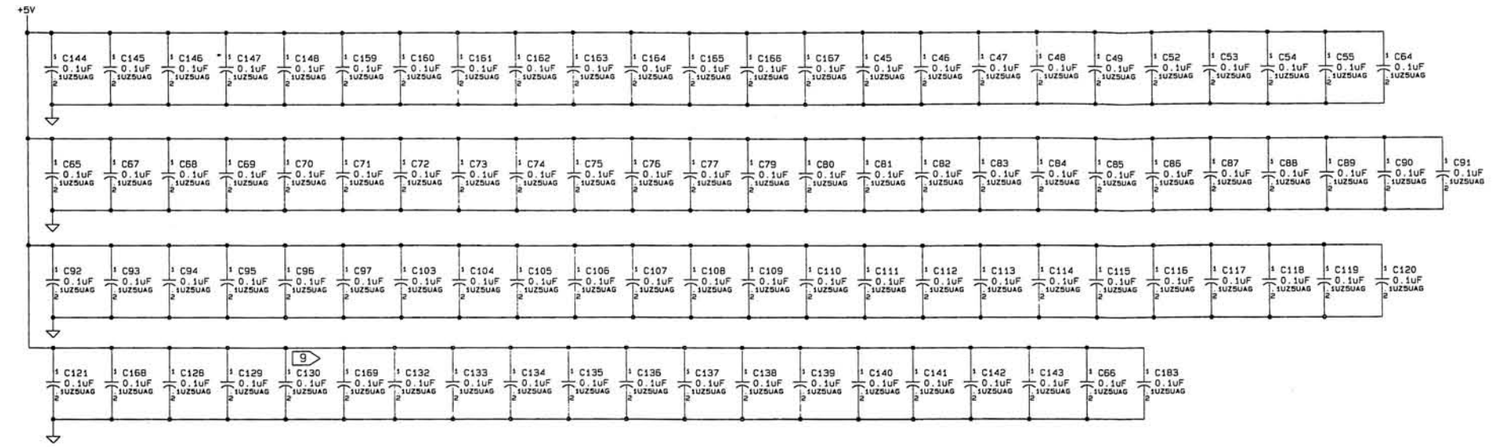
TO PSM

PPD 7.C3

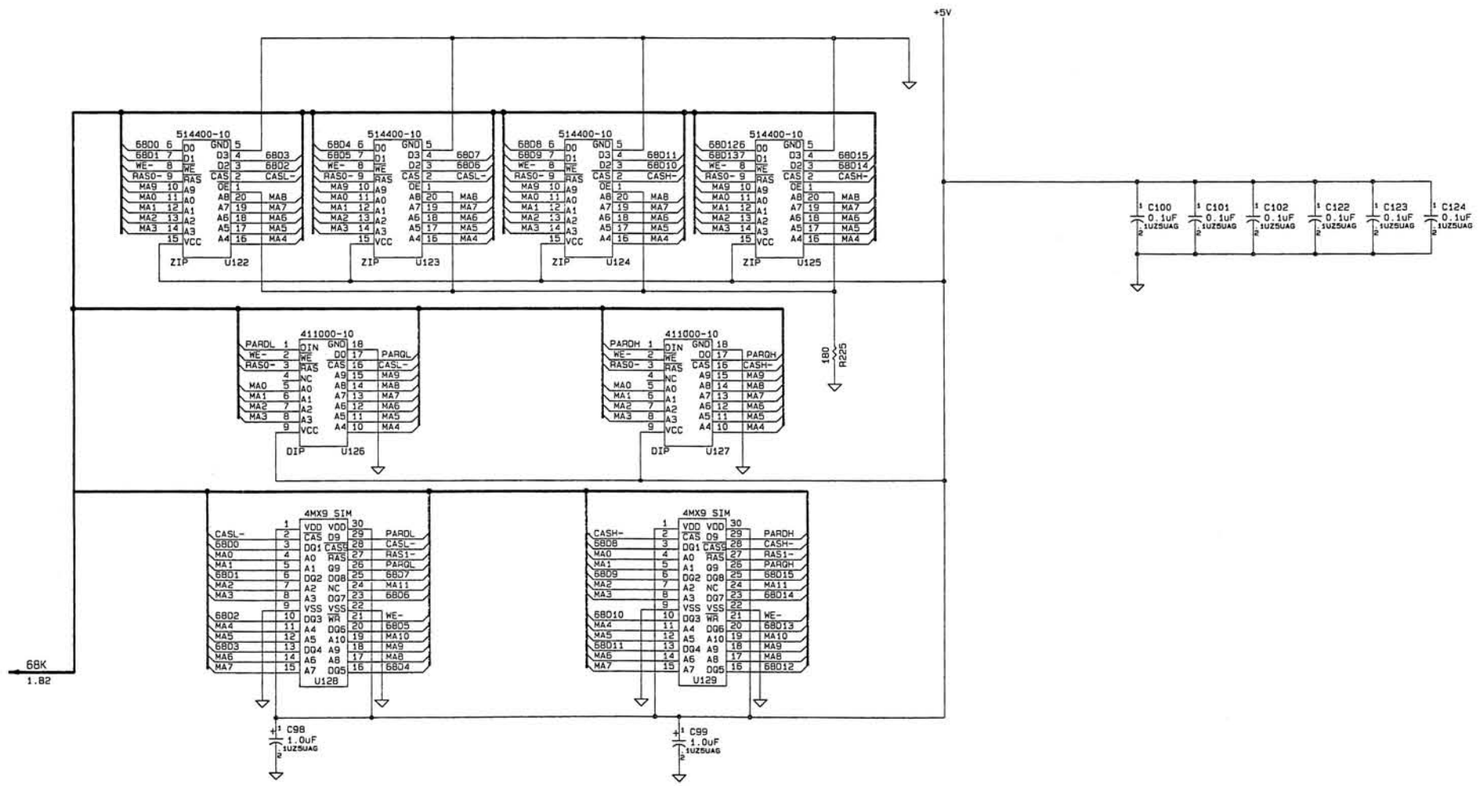
POWER AND GROUND:		
REF.DES.	GND	+5V
U4, 5, 40, 116	7	14
U77, 118	8	16
U9, 10, 15, 16, 21, 23, 48, 113	10	20

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION REDMOND, WASH.	
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:			
MECH CHK:		SIZE D	FSCM NO. 54193
MFG CHK:		DRAWING NO. 30-701-2313	
QUAL ASSUR:		SCALE: NONE	SHEET 5

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91



POWER AND GROUND:		
REF.DES.	GND	+5V
U31-35, U80-U89, U55-U59	18	9



DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION REDMOND, WASH.	
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:			
MECH CHK:		SIZE D	FSCM NO. 54193
MFG CHK:		DRAWING NO. 30-701-2313	
QUAL ASSUR:		SCALE: NONE	SHEET 6

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91

TEST POINTS

Note: The test points shown below are located immediately next to the power connector, along front edge.

Note: Locate R233 near U30 (Left hand side) Install to short AGND to GND at this location.

Note: The ground test point shown below is located directly below the 68000.

POWER SUPPLY CONNECTOR

THIS RESISTOR MAINTAINS CURRENT THROUGH THE CONNECTOR TO KEEP THE CONTACT CLEAN. THE POWER SUPPLY SHALL SOURCE 1.0 MA AT 2.7 VOLTS WHILE POWER IS VALID.

68K 1.82

PCU 3.82

PD 8.88

FPD 5.03

PPD 5.A2

WAVEFORM BOARD CONNECTOR

SENSE LINE SELECTOR

(FSM / BENCH TEST) CONNECTOR

NOTE: THIS CAPACITOR IS USED TO DECREASE THE CURRENT SPIKE GENERATED BY PLUGGING IN THE PSM.

PSM CONNECTOR

NOTE: ABOVE CIRCUIT IS FOR ESD PROTECTION

Notes:

1) DGND (digital ground) is tied to PGND (programming ground) and at the power connector.

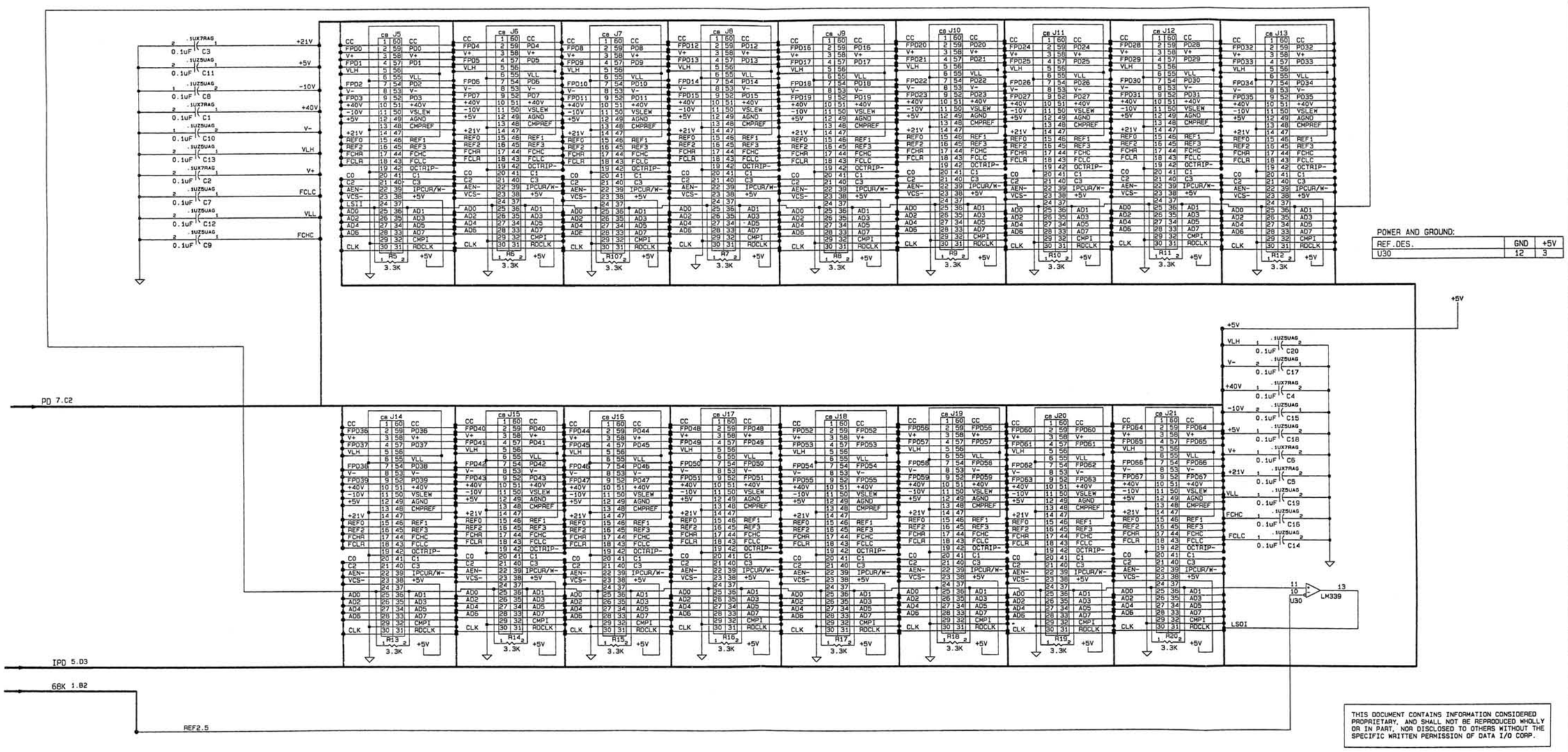
2) AGND is a sense line of the DUT ground used on the waveform board

POWER AND GROUND:		
REF.DES.	GND	+5V
U68, 73, 99	7	14
U20, 22, 45-47, 101	10	20

3) = PROGRAMMING GROUND
= DIGITAL GROUND

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION	REDMOND, WASH.
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:			
MECH CHK:		SIZE D	FSCM NO. 54193
MFG CHK:		DRAWING NO. 30-701-2313	
QUAL ASSUR:		SCALE: NONE	SHEET 7

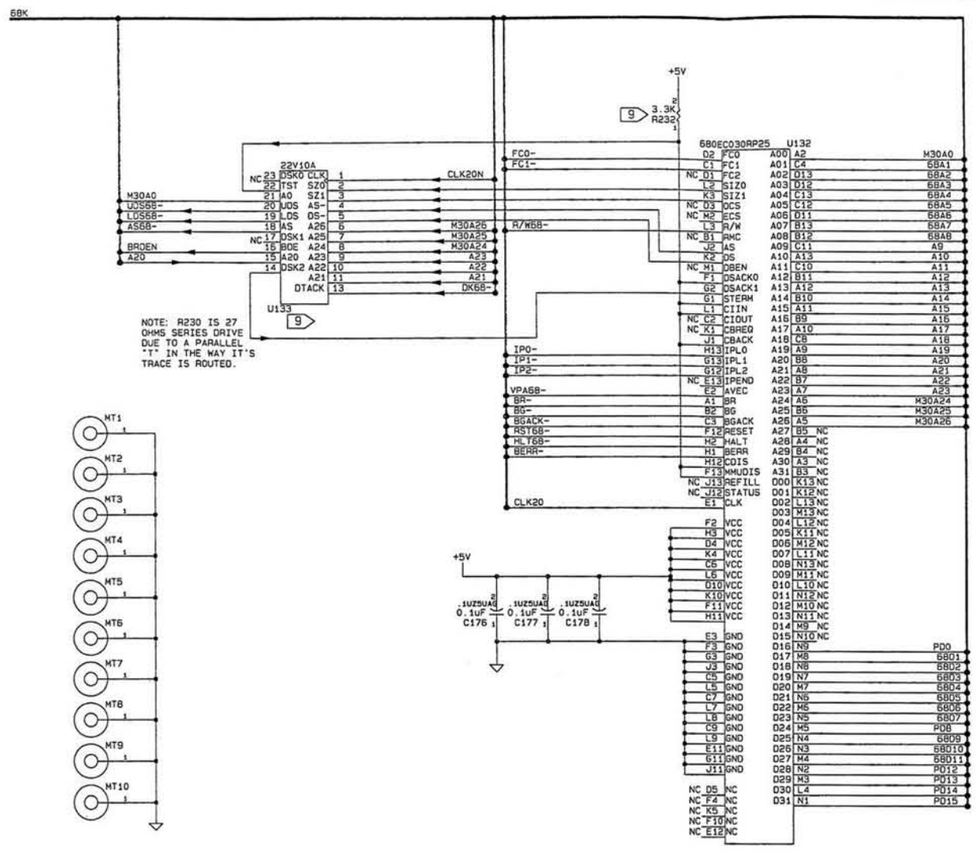
REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91



POWER AND GROUND:		
REF.DES.	GND	+5V
U30	12	3

DRAWN: Gerald Ryder	DATE 1/4/91	DATA I/O CORPORATION	REDMOND, WASH.
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:		SIZE D	FSCM NO. 54193
MECH CHK:		DRAWING NO. 30-701-2313	
MFG CHK:		SCALE: NONE	SHEET 8
QUAL ASSUR:			

LTR	DESCRIPTION	DR	CHK	APPRD	DATE
A	RELEASE	GLR			6/19/91



DRAWN: Gerald Ryder	DATE 3/5/91	DATA I/O CORPORATION REDMOND, WASH.	
CHECKED:		TITLE: SCHEMATIC DIAGRAM, UNISITE CONTROLLER BD.	
ELEC CHK:		SIZE D	FSCM NO. 54193
MECH CHK:		DRAWING NO. 30-701-2313	
MFG CHK:		SCALE: NONE	SHEET 9
QUAL ASSUR:			