REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	G'R	BV	PS	9/86
B	INC ADCN A1, A2 PER ECP # 0000	LW	BV 5-27-87	gw	5/87

NOTE: These resistor pull-ups shall force all ones if a location is read that does not have a ram board installed. These pull-ups also insure no parity error will occur if no ram board is installed. (assume (6(20pf)+50pf) x 1.8K => 310ns to 3.1V)

NOTICE: The drams must have IOL > 4.2 ma
(5/1764) + LS245 (200ua) + LS74 (200ua) + F280 (600ua)
IOL > 2.85 ma + 1.00ma => 3.85 ma

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTERS ARE IN OHMS, 1/8 W, 2%
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REFERENCE DESIGNATOR USED: U40, J1, C45, R19, TP1
4. REFERENCE DESIGNATOR NOT USED: C33, U5, R12, R13
5. POWER AND GROUND:

REF.DES.	GND	+5V
U6, 7, 8, 9, 15, 19	7	14
U24, 28		
U16, 17, 25, 27, 38	8	16
U39, 40		
U18, 37	10	20

6. UNUSED GATES:

Note: Servicing Rev A PWB's 410-2114-001A This schematic shows several unused gates above, these gates are also not used on the the Rev A PWB. The connections of unused gates is slightly different on the Rev A PWB.

Note: Parity enable/disable
At reset, the parity detect is disabled
Write a 1 to location $60001 to enable
Write a 0 to location $60001 to disable

Note: To establish the amount of ram in the system, a simple test write followed by a read for the following two words of data should be used: $5A5A, $A5A5

Note: At power on, all locations with parity must be written to with any data pattern to initialize the parity bits. The best method would be to write a random number followed by a read for a simple fast test.

Note: To test the parity bit a regular ram test shall be used which writes and reads both an even and odd number of ones to both the upper and lower bytes of memory.
If a parity error occurs, no Dtack is sent for that location, and the controller will provide a bus error in 3 usec. The bus error handler routine can determine if a parity error occured by looking at the error address and comparing to valid memory

Note: Any 68000 emulator which is used with this board must support continuous Address Strobe, otherwise the DRAM will NOT be refreshed.

REFRESH ALTERNATOR
1 => REFRESH RAS0, RAS1, RAS3, RAS4
0 => REFRESH RAS2, RAS5, RAS6

THE REFRESH ALTERNATOR CUTS MAXIMUM REFRESH CURRENT IN HALF

REFRESH EVERY 6.4 USEC

2 TO 3 WAIT STATES
=> 600 OR 700NS RAM CYC

For App Micro Sys 68000 emulator

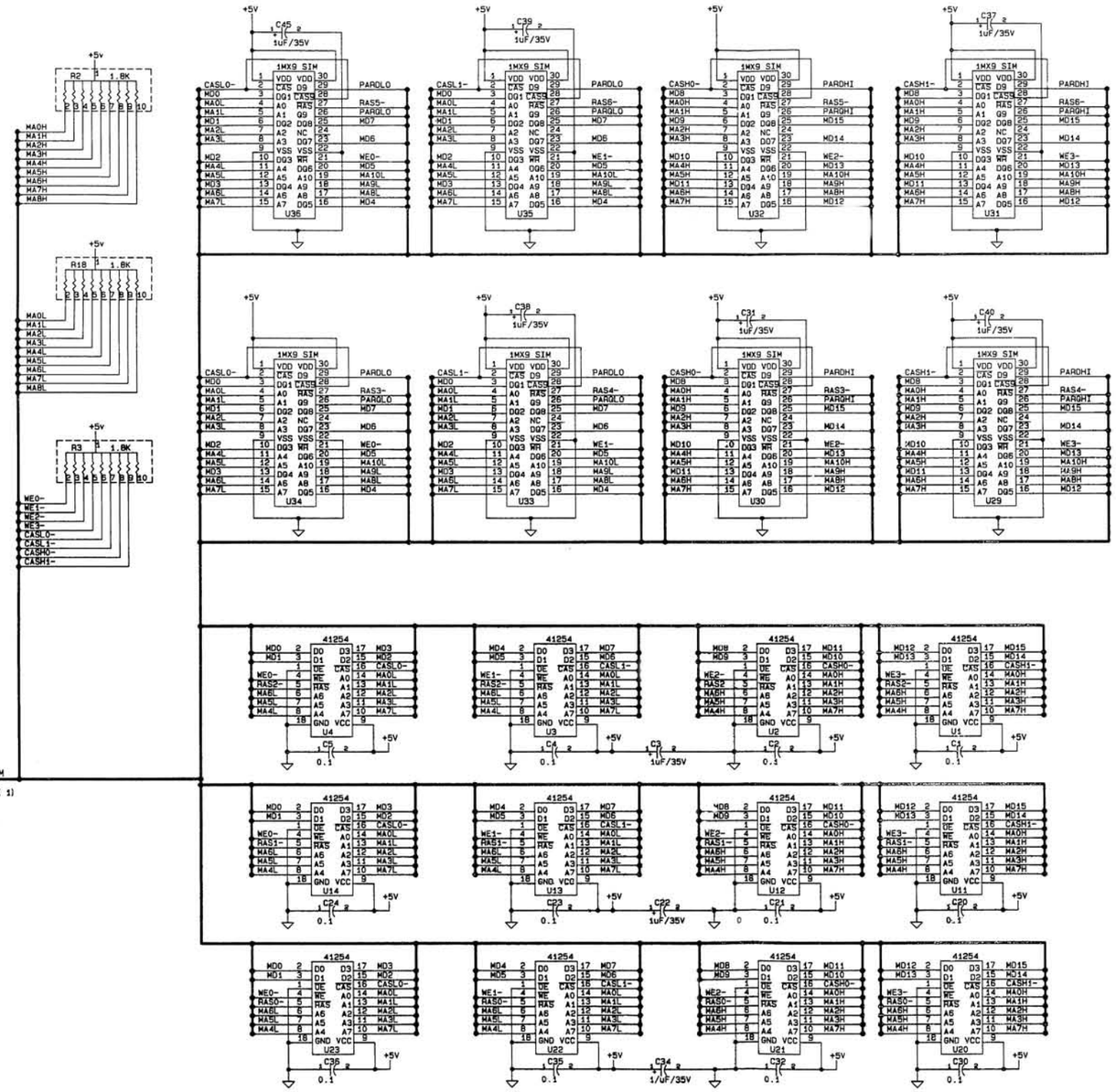
ADDRESS MULTIPLEXER

RAM (PAGE 2)

P/N: 701-2114-001

DRAWN G RYDER	DATE 9/86	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. Valdivia	5/7/87	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, EXPANSION RAM BOARD
ELEC ENG K. CRISAFULLI	9/86		
MECH ENG D NIERESCHER	9/86		
MFG ENG C JENSEN	9/86	DO NOT SCALE DRAWING	SIZE D / FSCM NO. 54193 / DRAWING NO. 30-701-2114
QUAL ASSUR M FOLKERTS	9/86		SCALE — / D.A.D. / SHEET 1 OF 2
APPD P.SHREVE	9/86		

REVISIONS						
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	SEE SHEET ONE	LW	BV 3-27-84		



DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM EXPANSION RAM BOARD
ELEC ENG			
MECH ENG		DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54193 · DRAWING NO 30-701-2114
MFG ENG			SCALE — · SHEET 2 OF 2
QUAL ASSUR			
APPD			