TeleVideo® TS 816 Maintenance Manual

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TS 816 THEORY OF OPERATION

This theory of operation describes the physical layouts and the hardware function of the TS 816 logic boards.

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1.0 INTRODUCTION

The TS 816 is a multi-user system which supports 16-user stations (ie. TS 800A, TS 802, TS 1602 etc.). It has a three board microcomputer based on the Z80A microprocessor and the Z80A family of support LSI ICs.

The system functions as a central resource manager for the user stations via RS422 SDLC communication links. The central storage devices are an 8" Winchester disk drive and a 1/4 inch tape cartridge.

BLOCK DIAGRAM OF THE TS 816 AS A RESOURCE MANAGER

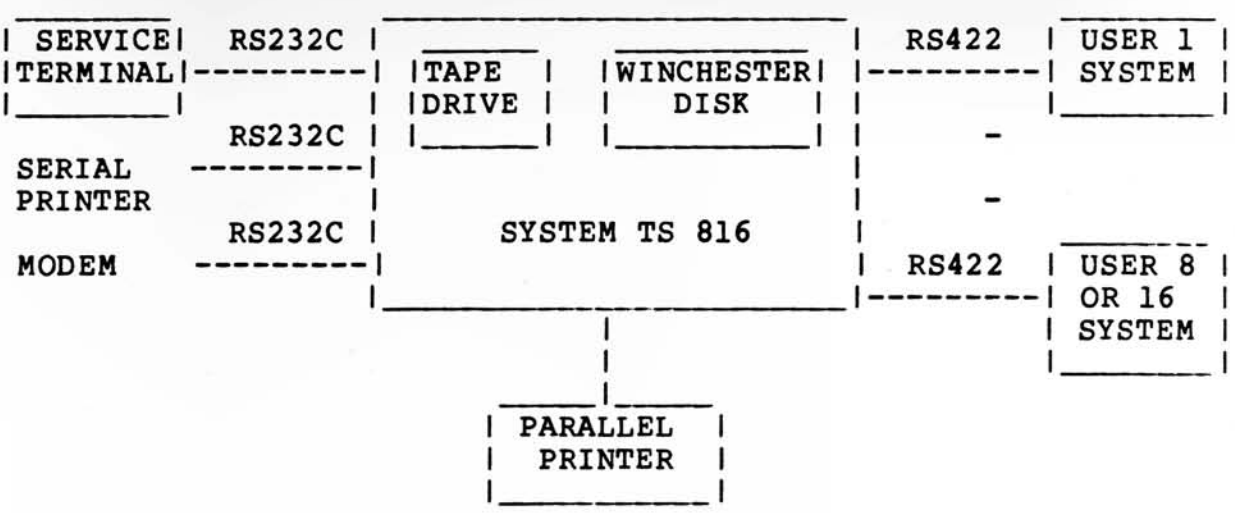


FIG. 1 SYSTEM TS 816 CONFIGURATION

2.0 GENERAL DESCRIPTION

a. Z80A CPU
The main processing unit in the system (4.0MHZ operation).

b. Z80A CTC
Counter/Timer IC, generating the baud rates for RS232C serial channels.

c. Z80A-PIO
Parallel I/O IC, providing Centronic type printer interface.

d. Z80A SIO
Serial I/O ICs, providing RS232C interface (data rate to 19.2 KB) and RS422 high speed serial interface with data at a rate of 800 Kbits/sec. The SIO also provides the serial interface to the cassette tape drive.

e. Z80A DMA
Direct memory access controller IC is used for direct transfer of data between memory and peripheral I/O, such as SIO's and Winchester hard disk interface.

f. MEMORY
Main memory available is 128 Kbytes, which is implemented using 64K X 1 dynamic RAM ICs. 4 Kbytes of PROM is used for system firmware (during power-up or reset only).

g. HARD DISK INTERFACE
Interface is provided to talk to a Fujitsu M2302K 8 inch Winchester disk drive.

h. CASSETTE TAPE INTERFACE
Interface is provided to talk to a DEI (Data Electronic Inc.) CMTD-3400S2 6400BPI cartridge tape drive.

3.0 FUNCTION

The facilities available are 128 Kbytes of main memory, interface to communicate with Fujitsu's 8 inch Winchester drive, interface to communicate with DEI's tape drive which is used as backup to the Winchester and a parallel port for high speed Centronic type interface. In addition three channels of RS232 interface and 16 channels of RS422 interface to communicate with the user stations.

There are two banks of dynamic memory of 64 Kbytes each. Only one bank at a time can be accessed by the cpu through the use of "EN DRAM" latch and "2ND BANK" latch which are software programmable.

4 Kbytes of PROM is used for system inialization, diagnostic, boot and hard disk/tape drive control during the power-up or reset sequence. This PROM is not accessible to the users. After the initial program in the PROM is run, it maps itself off and returns a full complement of DRAM.

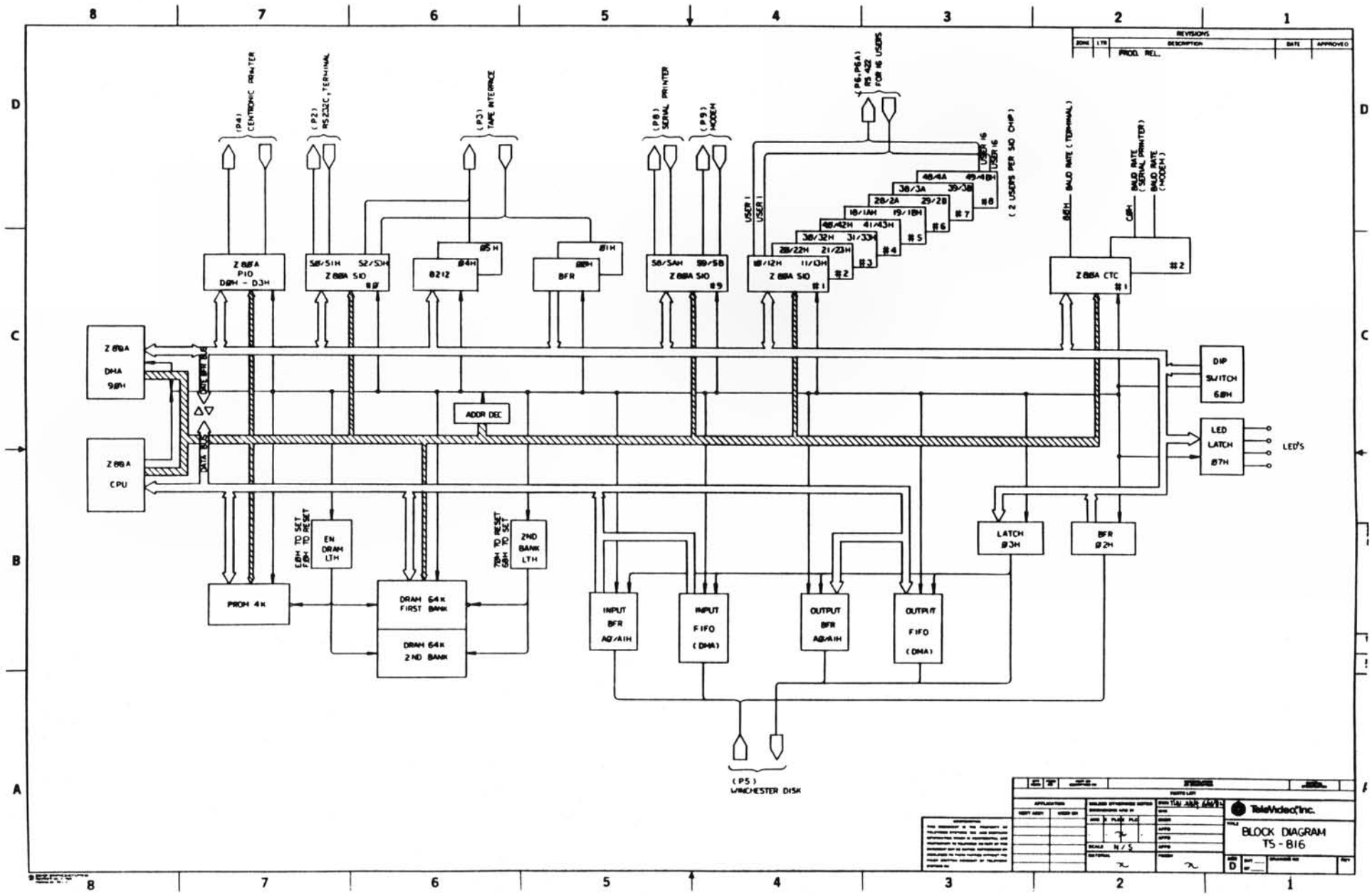
The DMA funtion in the TS 816 is to transfer data between memory and I/O devices, memory to memory and also I/O device to I/O device.

The CTC IC provides interrupt capability for the hard disk interface,a second CTC generates the baud ratesforthe RS232 channels. The first RS232C port is reserved for a service terminal and its baud rate is selected by a dip switch (A13) being read by the software and then loading the CTC with the appropiate value. The baud rates of the other two RS232C ports is set by the operating system at the time it is loaded.

Four LED indicators are used for diagnostic purposes during power-up to help in debugging the logic board.

The system block diagram is shown in figure 2, I/O port assignment is shown in table 1 and the baud rate switch configuration is shown in table 2.

Figure 2 System Block Diagram of the TS 816



ADDRESS BIT #									I/O PORT
7	6	5	4	3	2	1	0	HEX	
0	0	0	0	0	0	0	0	00H	TAPE STATUS BYTE 1
					0	0	1	01H	TAPE STATUS BYTE 2 & DIAGNOSTIC MODE
					0	1	0	02H	HARD DISK STATUS
					0	1	1	03H	HARD DISK OUPUT LATCH
					1	0	0	04H	TAPE OUTPUT LATCH BYTE 2
					1	0	1	05H	TAPE OUTPUT LATCH BYTE 1
					1	1	1	07H	INDICATOR LOAD (LED)
0	0	0	1	0	X	0	0	10H	SIO 1, CH A DATA REG.
						1	0	12H	COM/STAT REG (USER 1)
						0	1	11H	CH B DATA REG.
						1	1	13H	COM/STAT REG (USER 2)
0	0	1	0	0	X	0	0	20H	SIO 2, CH A DATA REG.
						1	0	22H	COM/STAT REG (USER 3)
						0	1	21H	CH B DATA REG.
						1	1	23H	COM/STAT REG (USER 4)
0	0	1	1	0	X	0	0	30H	SIO 3, CH A DATA REG.
						1	0	32H	COM/STAT REG (USER 5)
						0	1	31H	CH B DATA REG.
						1	1	33H	COM/STAT REG (USER 6)
0	1	0	0	0	X	0	0	40H	SIO 4, CH A DATA REG.
						1	0	42H	COM/STAT REG (USER 7)
						0	1	41H	CH B DATA REG.
						1	1	43H	COM/STAT REG (USER 8)
0	1	0	1	0	X	0	0	50H	SIO 0, CH A DATA REG.
						1	0	52H	COM/STAT REG (RS232 #1)
						0	1	51H	CH B DATA REG.
						1	1	53H	COM/STAT REG (TAPE INTERFACE)
0	1	1	0	0	X	X	X	60H	DIP-SWITCH READING
1	0	0	0	0	X	0	0	80H	CTC 1, CH 0(BAUD RATE A)
						0	1	81H	CH 1
						1	0	82H	CH 2
						1	1	83H	CH 3
1	0	0	1	0	X	X	X	90H	DMA
1	0	1	0	0	X	X	0	A0H	WDC STATUS/COMMAND REG.
							1	A1H	DATA REG.
1	1	0	0	0	X	0	0	C0H	CTC 2, CH 0(BAUD RATE B)
						0	1	C1H	CH 1(BAUD RATE C)
						1	0	C2H	CH 2
						1	1	C3H	CH 3
1	1	0	1	0	X	0	0	D0H	PIO CH A DATA REG.
						1	0	D2H	COM/STAT REG
						0	1	D1H	CH B DATA REG.
						1	1	D3H	COM/STAT REG
1	1	1	0	0	X	X	X	E0H	SET 'EN DRAM' LATCH
1	1	1	1	0	X	X	X	F0H	RESET 'EN DRAM' LATCH
0	0	0	1	1	X	0	0	18H	SIO 5, CH A DATA REG.
						1	0	1AH	COM/STAT REG (USER 9)
						0	1	19H	CH B DATA REG.
						1	1	1BH	COM/STAT REG (USER 10)
0	0	1	0	1	X	0	0	28H	SIO 6, CH A DATA REG.

TABLE 1 I/O PORT ASSIGNMENTS

ADDRESS BIT #									I/O PORT
7	6	5	4	3	2	1	0	HEX	
						1	0	2AH	COM/STAT REG (USER 11)
						0	1	29H	CH B DATA REG.
						1	1	2BH	COM/STAT REG (USER 12)
0	0	1	1	1	X	0	0	38H	SIO 7, CH A DATA REG.
						1	0	3AH	COM/STAT REG (USER 13)
						0	1	39H	CH B DATA REG.
						1	1	3BH	COM/STAT REG (USER 14)
0	1	0	0	1	X	0	0	48H	SIO 8, CH A DATA REG.
						1	0	4AH	COM/STAT REG (USER 15)
						0	1	49H	CH B DATA REG.
						1	1	4BH	COM/STAT REG (USER 16)
0	1	0	1	1	X	0	0	58H	SIO 9, CH A DATA REG
						1	0	5AH	COM/STAT REG (RS232 #2)
						0	1	59H	CH B DATA REG.
						1	1	5BH	COM/STAT REG (RS232 #3)
0	1	1	0	1	X	X	X	68H	SET '2ND BANK' LATCH
0	1	1	1	0	X	X	X	70H	RESET '2ND BANK' LATCH

TABLE 1 I/O PORT ASSIGNMENTS CONT.

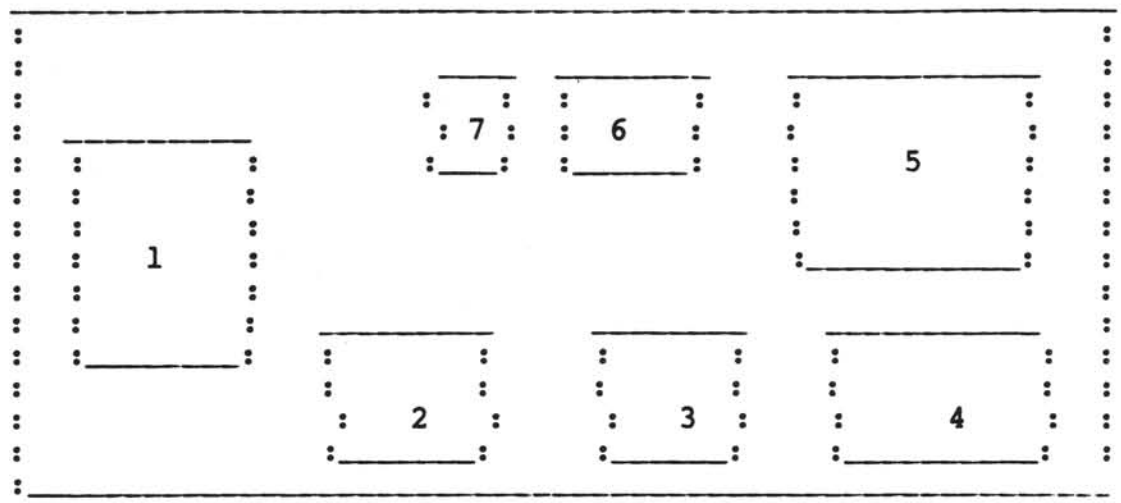
DIP SWITCH KEYS: 1 2 3	BAUD RATE OF RS232C # 1
0 0 0	19.2 KB
0 0 1	9.6 KB
0 1 0	4.8 KB
0 1 1	2.4 KB
1 0 0	1.2 KB
1 0 1	600 B
1 1 0	300 B
1 1 1	150 B

NOTE: 0 : CLOSE
1 : OPEN

TABLE 2. BAUD RATE SWITCH (A13) FOR RS232C #1

4.0 CIRCUIT DESCRIPTION

The overall layout of the TS 816 logic board is below in Figure 3.



1) 16-USER SERIAL I/O
2) TAPE INTERFACE
3) CPU AND DMA
4) MEMORY
5) WINCHESTER DRIVE INTERFACE
6) PARALLEL I/O FOR CENTRONIC TYPE PRINTER
7) CLOCK

FIGURE 3

The TS 816U board consists mainly of 26LS32 receivers (A9,A10,A11, A12,A13,A14,A15 and A16 in TS 816U board) and 26LS31 drivers (A1,A2,A3, A4,A5,A6,A7 and A8 in TS 816U board) for the standard RS422 interface of 8 users per board.

4.1 RESET

The reset circuitry has a 74LS00 IC (A92), which generates the reset debouncing signal when the reset switch is depressed (pin 13 is normally low and pin 9 is normally high). -Reset must be active for at least three clock cycles for the CPU to properly accept it. As long as -Reset remains active, the address and data bus float and the control signal outputs are inactive. Two internal T cycles are used before the CPU returns to normal operation. -Reset clears the PC register so that the CPU starts program execution from address 0000 hex again.

4.2 CLOCK GENERATION

The 16MHZ clock from the oscillator is divided down to 4MHZ using a 93S16 IC (A36) and a transistor (TR 2N2907) is used to drive the proper system clock level needed by the Z80 ICs. This circuit also insures enough driving current for the clock signal going to other devices.

To get the baud rates from the CTC for the RS232C interface, an 8MHZ signal from the 93S16 IC is fed into a 74LS163 IC (A37) to generate a frequency of 1/6.5 times the system clock to be the CTC clock.

The transmit clock for the SIO RS422 interface is generated through

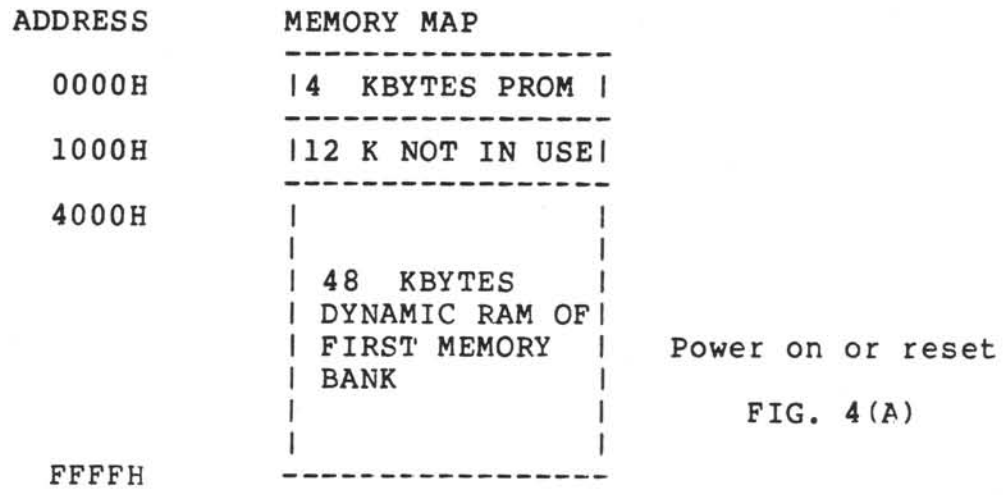
another 74LS163 IC (A73) and a 74S04 IC (A72) using system clock (4MHZ).

4.3 MEMORY

PROM : A 4K X 8 PROM (A96) is used. PROM is automatically enabled upon power-up or reset. PROM selection circuitry consists of one 74LS138 IC (A84) and other common gates. By using the Z80 I/O instruction the PROM is enabled or disabled. When the PROM is enabled the -CAS signal for dynamic RAM column address goes inactive which makes dynamic RAM disabled and the prom active. During PROM operation one wait state is generated to give sufficient time for the slower PROM access speeds.

DYNAMIC RAM : Sixteen ICs of 65,536 X 1 bits each are used for main memory (A110 thru A125). These ICs are divided into two banks of 64K X 8 bits each. There are two latches involved in the selection of the different combinations of working memory. The first latch is "EN DRAM" (A69-2) which remains reset upon power on or a hardware reset. The latch is programmable to be set by doing an I/O write instruction to port E0H. The second latch is "2ND BANK" (A69-1) which remains reset during power on and is programmable by writing to port 68H (set) or 78H (reset).

The following is a pictorial of the memory configurations:



Power on or reset

FIG. 4(A)

B. After setting 'EN DRAM' latch (write I/O port E0H) and '2ND BANK' latch remains reset:

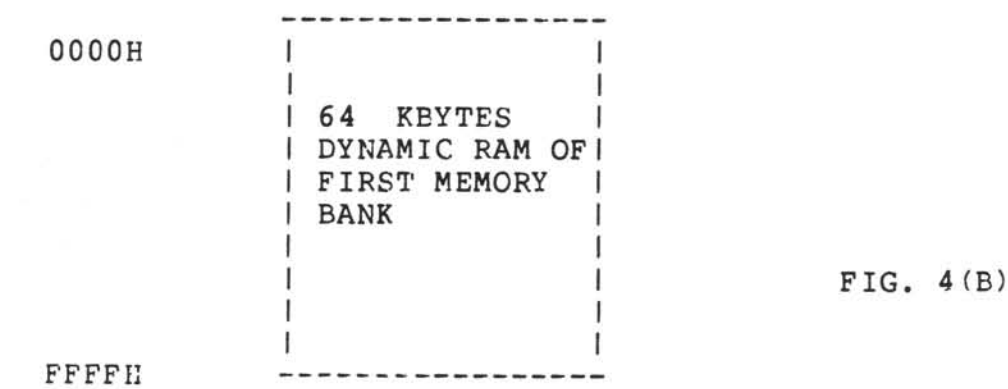


FIG. 4(B)

C. After setting both 'EN DRAM' latch and '2ND BANK' latch, the memory map looks as follows:

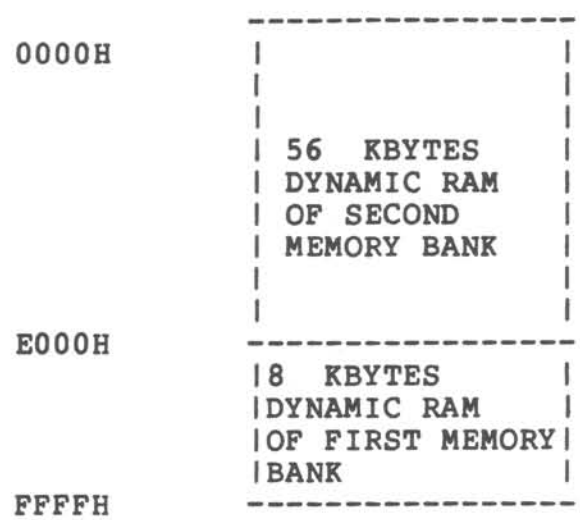


FIG. 4(C)

Figure 4 Memory Map

To read or write the dynamic RAM -CAS and -RAS are provided to specify column and row addresses which gives the means to access the 64K memory space. Two 74S74 IC (A53, A70) and other related ICs generate -CAS and -RAS from the -M1 and -MREQ signals. "SEL CLM" chooses either addresses A0-A7 or A8-A15 as row and column address. When dynamic RAM is enabled it activates -CAS so all RAM locations can be accessed by the user. During refresh -RAS is activated and a row per RAM is refreshed each CPU cycle. The following diagrams show the timing for the memory signals.

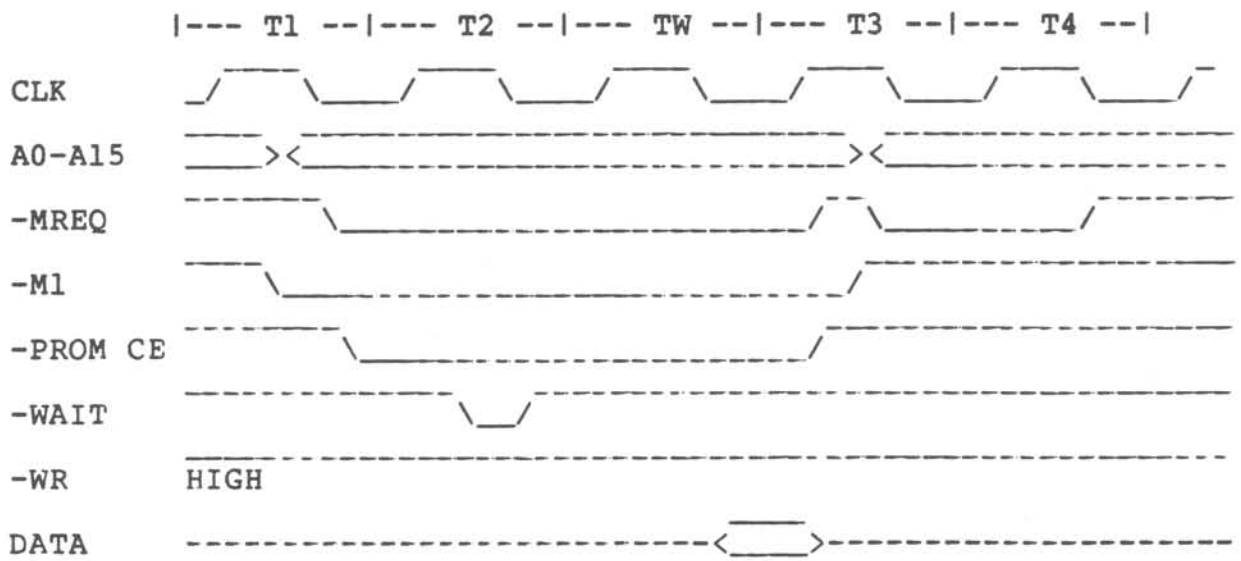


FIG. 5 INSTRUCTION FETCH FROM PROM

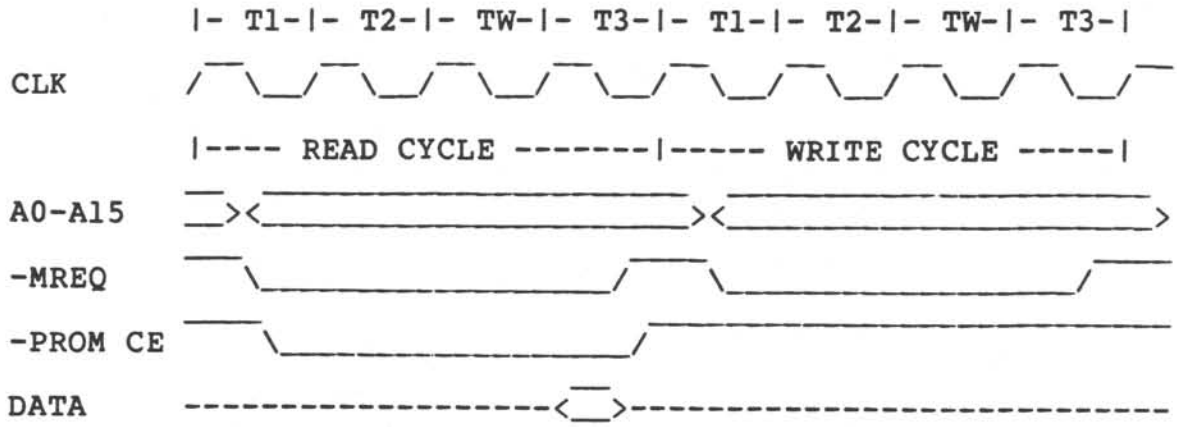


FIG. 6 READ/WRITE ON PROM

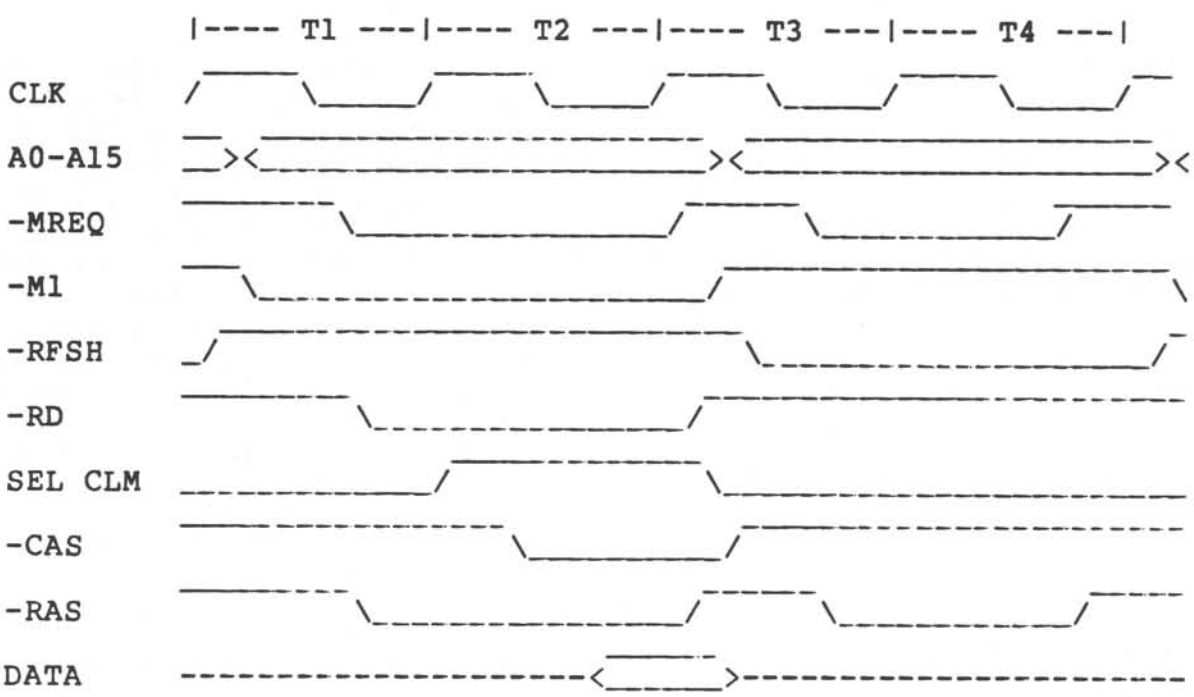


FIG. 7 INSTRUCTION FETCH FROM DRAM

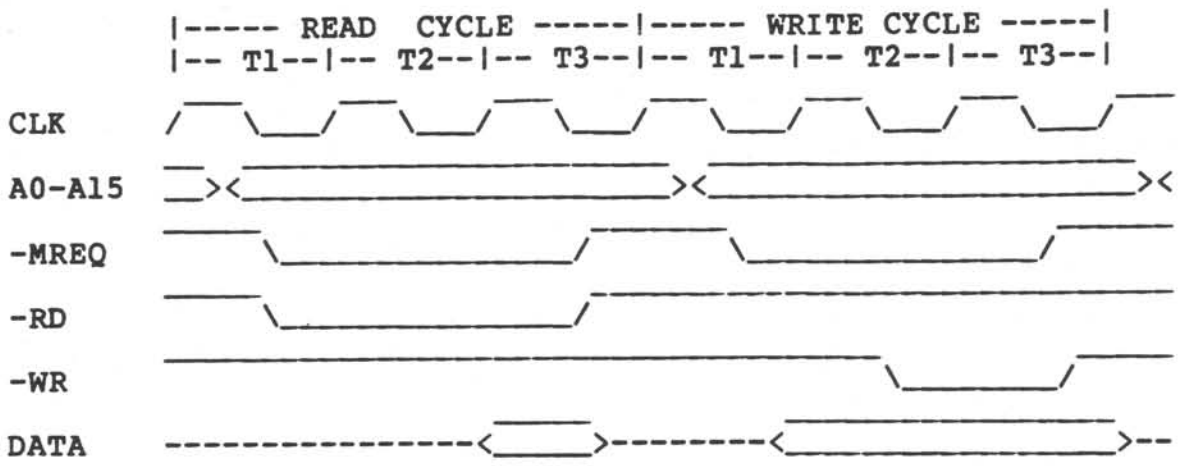


FIG. 8 READ/WRITE FROM DRAM WITHOUT WAIT STATES

4.4 DMA OPERATION

The DMA "RDY" line is monitored to determine when a peripheral device is ready for a read or write operation. When the DMA is enabled to operate the "RDY" line indirectly controls that operation. -BUSREQ is used by the DMA to request control of the address, data and control buses from the CPU. When the CPU receives an active -BUSREQ it sets the buses to the high impedance state as soon as the current CPU machine cycle is terminated. The CPU then sends a -BUSAK signal to indicate to the DMA that it now has control of the buses (Figure 9 illustrates this timing).

On every rising edge of clock the ready line is sampled to see if it is at an active level. When the DMA detects a low -BAI for two consecutive rising edges of clock it begins transferring data on the next rising edge of clock.

Figure 10 and 11 explain the timing of the ready line in burst mode and continuous mode operation of the DMA.

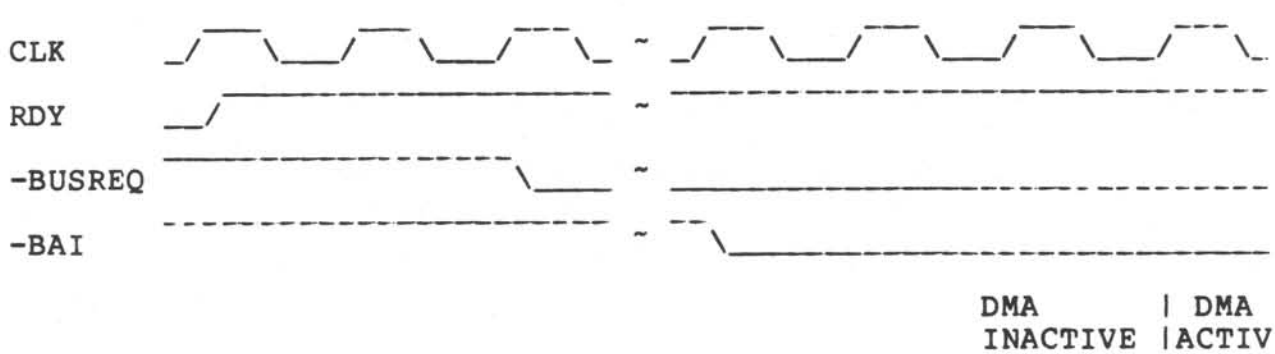


FIG. 9 BUS REQUEST AND ACCEPTANCE TIMING

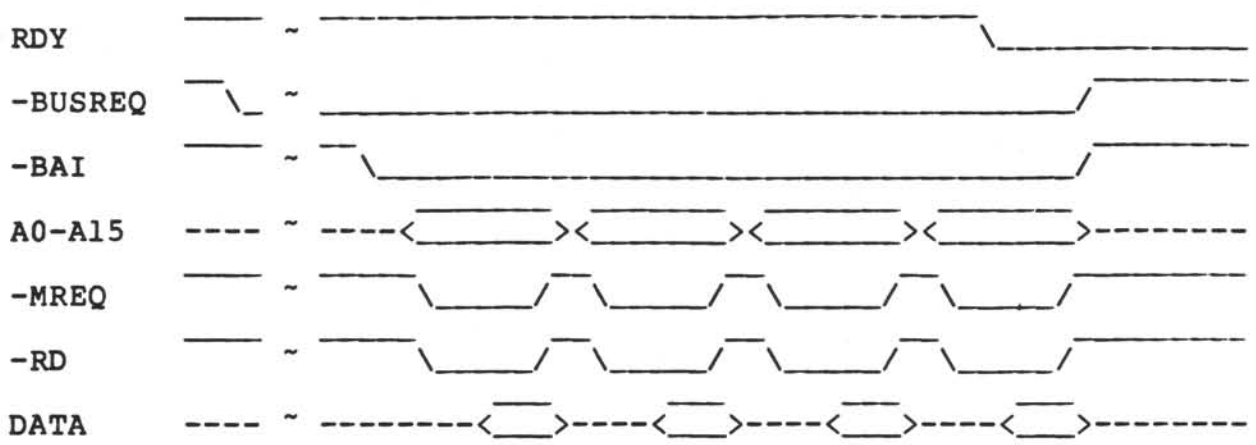


FIG. 10 RDY LINE IN BURST MODE

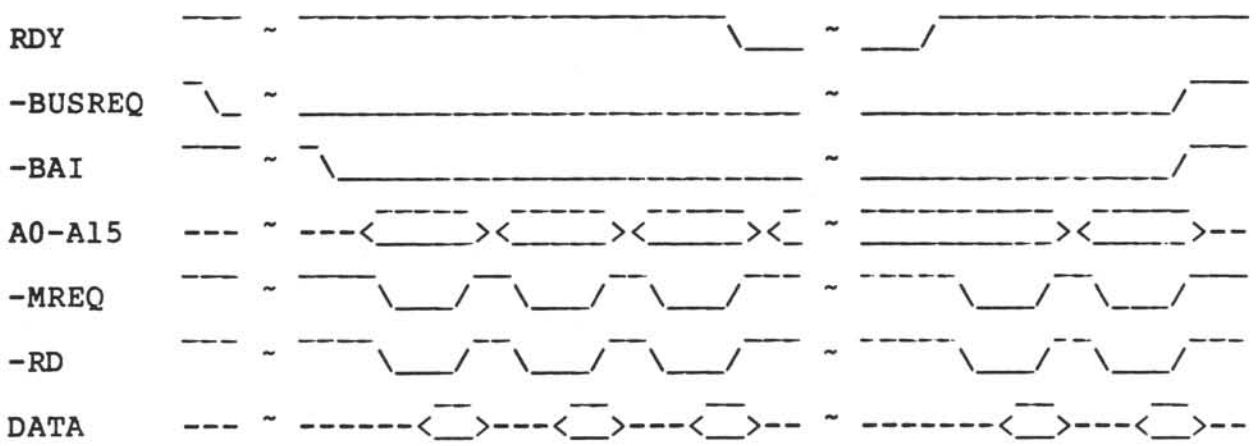


FIG. 11 RDY LINE IN CONTINUOUS MODE

4.5 I/O OPERATIONS

The Z80A CPU can handle up to 256 I/O ports presently only 128 ports are provided for using the lower eight address lines for this purpose. The I/O port address decoding is done by four 74S138 or 74LS138 IC (A45, A46, A47 & A91) so that only one I/O port is activated at a time. For an I/O read/write IORQ signal "nanded" with RD/WR signal to provide an -IORD/ -IOWR signal. During the I/O operation the CPU automatically inserts a single wait state (TW). This extra wait state allows sufficient time for the I/O port address to be decoded.

There are a total of 10 SIO ICs; eight of them (A2, A3, A27, A28, A29, A55, A86, A87 & A4) are for the 16 user RS422 interfaces which requires 16 channels of serial to parallel and parallel to serial interface. Two channels of the SIO at A4 are for an RS232C interface (RS232 #2 & RS232 #3) that uses the standard 75188 driver and 75189 receiver IC set. One channel of the SIO at A29 is for an RS232C

interface which is the diagnostic or service port. The other channel of the SIO at A29 is for the tape drive interface which includes two output latches (8212 A88, A89) and two input status receivers (74LS240 A103, A102). A more detailed description of the tape interface is given in section 4.6. The timing for an input instruction to read data or status byte from an SIO and output instructions to write data or send the control byte to a SIO are illustrated in Figure 12.

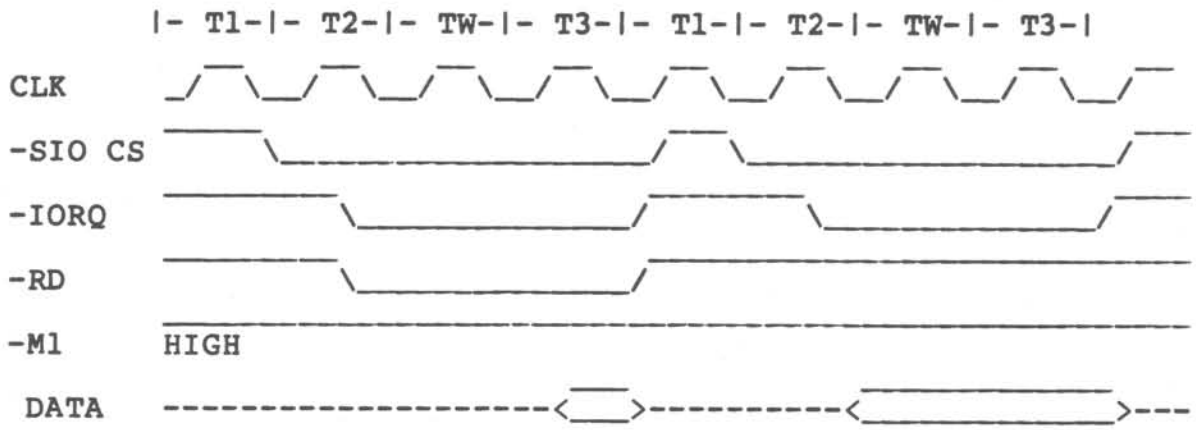


FIG. 12 TIMING DIAGRAM FOR READ/WRITE OF SIO

4.6 TAPE OPERATION

The following devices are involved with the tape operation one channel of an SIO (A29), two output latches 8212 IC (A88, A89) and two input inverted buffers 74LS240 IC (A103, A102). The output latches are called "Tape output latch 1" (05H) and "Tape output latch 2" (04H). The input inverters are called "Tape input status 1" and "Tape input status 2".

Data word for "Tape output latch 2"

-TR2	-TR1	-SL4	-SL2	-SL1	X	X	X	X
D7	D6	D5	D4	D3	D2	D2	D1	D0

Track select is via D7 and D6 according to the following chart with a low being true. The track selection will select all heads for a given track (erase, write & read). The last track selection will be stored in the tape drive even after deselection by the controller.

TRACK #	TR2	TR1
1	H	L
2	L	H
3	L	L
4	H	H

Tape drive select is via D5, D4 AND D3; Together these bits determine the tape drive address (low true). The address function will process and remain active during any other drive I/O. The following chart shows the address selection.

DRIVE #	SL4	SL2	SL1
1	H	H	L
2	H	L	H
3	H	L	L
4	L	H	H
5	L	H	L
6	L	L	H
7	L	L	L
8	H	H	H

D2, D1 & D0 are not used and will not effect the system.

Data word for "Tape output latch 1"

SLG	X	-RWD	FB	-WEN	-HSP	-FWD	-REV
D7	D6	D5	D4	D3	D2	D1	D0

Reverse direction (-REV) is D0; active low causes the tape to move in the reverse direction. Forward direction (-FWD) is D1 causes the tape to move in the forward direction. High speed (-HSP) causes the tape to move at high speed in the direction selected.

Tape motion will continue until command signals go false. This can be triggered by the end of the tape when going forward or the beginning of the tape when in reverse. If both directions are given at the same time the tape will also stop. Two more situations that will stop the tape are if the ready signal goes inactive and if a rewind command is given which is a higher priorty command.

In high speed motion the speed will drop to low speed when the upper loading point hole is sensed in the reverse direction or if upper early warning hole is sensed in the forward direction.

Write enable (-WEN) will enable writing and erasing functions for the selected track. The writing or erasing operations will only be allowed is the tape cartridge is in the unprotected state. Write enable should not be reset until the drive has stopped and it should be set prior to the tape going in motion. At least two milliseconds are needed between the reset of write enable and the selection of a new track. The write enable signal is reset by either reverse or high speed commands.

Feedback (FB) is for general use and can be read also through port 0CH at D4.

Rewind (-RWD) causes the tape to be positioned at the beginning at high speed. The drive must be selected to start a rewind but may be deselected after the sequence has started.

D6 this bit is not used.

Select gate (SLG) allows selection per the select and address codes. It is used to prevent unwanted selection during the change of a select operation.

"Tape input status 1" address is 00H

RDY	LPS	EWS	FLG	FUP	WEN	BSY	SLD
D7	D6	D5	D4	D3	D2	D1	D0

Ready (RDY) is true when the tape cartridge is installed, the sensor lamp is drawing current and five volts is applied to the tape drive.

Load point sensed (LPS) is set and latched when the upper load point hole (the warning for the start of the tape) is passed in the reverse direction. The signal will be reset when the load point is passed with

the tape going in the forward direction. When this signal is true the high speed signal will be disabled in the reverse direction; at this time reverse tape motion is allowed to proceed until the beginning of tape hole is encountered at which time the drive will stop and only accept forward commands.

Early warning sensed (EWS) is set and latched when the upper early warning hole (warning for end of the tape) is passed in the forward direction. This signal will be reset when the hole is passed in the reverse direction. When this signal is true the high speed signal is disabled and forward motion is allowed to proceed until the end of tape hole at which time the tape will stop and only accept reverse direction commands.

Flag (FLG) is set when the automatic sequence to position the tape at the beginning has been executed or a rewind command has been completed. This signal is reset by a subsequent receipt of a forward command.

File unprotected (FUP) is true when a tape cartridge is installed and it is in the unprotected state (meaning the tape can be written on).

Write enable (WEN) is true when a write enable is latched within the tape drive.

Busy (BSY) is true when the drive is performing an automatic rewind sequence (a cartridge is initially installed), normal rewind, forward or reverse command. This signal will go true when the command is received and will remain true until tape motion has stopped; the time for slow speed is 30 milliseconds and 80 milliseconds for high speed commands.

Selected (SLD) is true when the tape drive has received its proper address.

"Tape input status 2" address 01H

DIAG	X	DAD	FB	X	X	X	X
D7	D6	D5	D4	D3	D2	D1	D0

Diagnostic (DIAG) is reserved for starting the diagnostic routines which can be initiated by power up or reset.

Data Detected (DAD) is true when the data has been detected during a read from the tape cartridge at either low or high speed.

Feedback (FB) is the same as bit four in "Tape output status 2".

DATA COMMUNICATION WITH THE TAPE DRIVE:

The preamble for tape data is thirtynine "zeros" followed by a "one" at the beginning of each data block. The postamble is the reverse of this with a "one" followed by 39 "zeros" at the end of each data block. The preamble is stripped from the read data when data is being read in the forward direction. The postamble is stripped from the read data when the data is read in the reverse direction.

Example of a data block on the tape cartridge:

39 'ZEROS'| 1 'ONE'|ADDRESS | DATA | 1 'ONE | 39 'ZEROS'|

To create preambles and postambles -DTR must be low on the SIO for the equivalent of a five byte transmission time before and after the data is transmitted. During data transfer -DTR is at a high level.

4.7 OPERATION OF WINCHESTER DRIVE INTERFACE

The 8" Winchester drive interface consists of four 74S225 FIFO (first in-first out) memory ICs at locations A22, A23, A38 and A39. Four output drivers using 7438's (A36, A50, A66, A67), buffer ICs using 74LS244's (A24, A40, A41), an inverter IC 74LS240 at location A25 and miscellaneous gates providing control signals for the FIFO's.

The "Hard disk output latch" (I/O port 03H) is an eight bit latch which is automatically reset to all zeroes on power-up or during a hardware reset. The contents of the bits are as follow:

BIT 0 - WDSL 1	Lower bit of the drive select
BIT 1 - WD SL 2	Higher bit of the drive select (Note: The interface can talk four drives, we only have one drive in the system and it is designated as drive #0 and is selected with both bits 0 and 1 low.)
BIT 2 - WR OP	This bit should be high during a data write operation low during a data read operation.
BIT 3 - WD SFT RST	This bit, when high, sends a reset signal to the hard disk drive.
BIT 4 - WD FIFO RST	This bit, when high, resets all of the FIFO ICs.
BIT 5 -	Unused.
BIT 6 -	Unused.
BIT 7 -	Unused.

The "Hard disk input status" (I/O port 02H) is a four-bit input buffer whose contents are described as follows:

BIT 0 - WDC INT	This bit reflects the interrupt signal directly from the hard disk drive. When high, it indicates that the hard disk is in the interrupt phase.
BIT 1 - WDC ATN	This bit reflects the attention signal direc from the hard disk drive.
BIT 2 - WDC BSY	This bit reflects the busy signal directly from the hard disk drive.
BIT 3 -	Unused.

The Winchester drive requires a nominal data transfer rate of 1.68 microseconds per byte. Therefore FIFO buffers are needed to match the data transfer rate of the DMA burst mode which is programmable from 1.5 to 1.75 microseconds or faster. In the cases where the DMA runs faster, FIFO's are still needed because occurrence of the first byte is unpredictable and some delay is needed for the DMA to freeze the system data bus. The FIFOs are five bytes wide and two each are needed for read and write operations.

In the data read operation the drive sends a data request signal when it is ready to send a byte of data. The read enable signal is generated by the interface and sent to the drive. The data is then available at the input buffer (A25) and is clocked into the input FIFO ICs (A22, A23) where it is propagated to the last latch in the FIFO's. As soon as the input FIFO's have a byte of data ready to be transfered to the memory an output ready (OR) is sent from the FIFO creating a "WDC RDY" to initiate DMA operation. The DMA gets the byte out of the FIFO by giving an "IORD" to the I/O port (A0H) and giving a "FIFO output enable" which clocks the byte out of the last latch of FIFO's. Normal operation requires that the input FIFO ICs never be full; this is why the DMA transfer rate must be faster than 1.68 microseconds per byte.

The status register of the drive is readable directly by the cpu thru I/O port A0H. The data from the status register is passed through the input buffer (A25), bypasses the FIFO's and goes through another buffer (A24) to the system data bus.

During the data write operation the DMA keeps the output FIFO's (A38, A39) full by doing I/O writes to port A1H. The DMA is operating in burst mode and continues filling the FIFO's until their input enable (IR) signal goes inactive. The inactive "IR" releases "WDC RDY" and stops the DMA operation. As long as the FIFO's have data to be sent the output ready (OR) signal generates a write enable to the drive and transfering data at the speed of the data request signal from the drive. Normal operation requires that the output FIFO's never be empty during a data transfer which means the DMA data transfer rate must be 1.68 microseconds per byte.

The command register for the drive can be sent through the interface by doing an I/O write to port A0H. The data bypasses the output FIFO's and is sent to the drive via output buffers A40 and A41.

5.0 CONNECTOR DESCRIPTION OF TS 816 BOARD

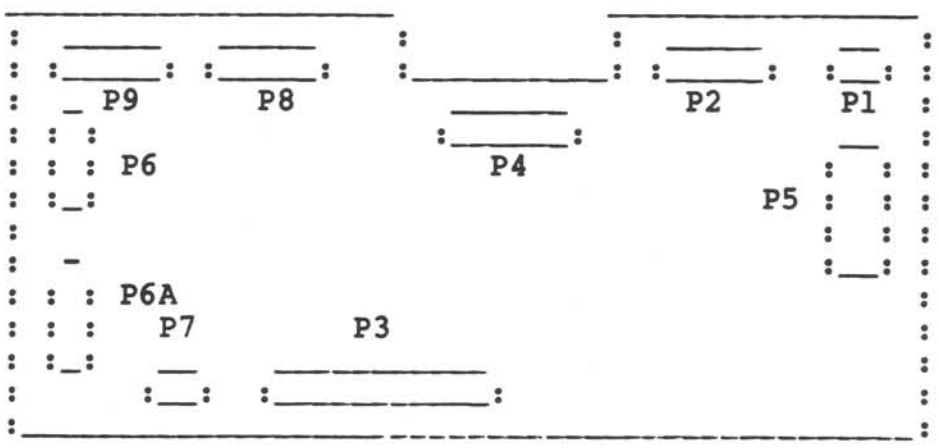


FIG 17. CONNECTORS ON THE TS 816 BOARD

CONNECTOR #	DESCRIPTION
P1	POWER
P2	RS232C # 1 (FOR SERVICE TERMINAL)
P3	CARTRIDGE TAPE INTERFACE
P4	CENTRONIC TYPE PRINTER INTERFACE
P5	WINCHESTER DISK DRIVE INTERFACE
P6	TS 816UBOARD INTERFACE (1STBOARD)
P6A	TS 816U BOARD INTERFACE (2ND BOARD)
P7	RESET INTERFACE
P8	RS232C # 2 (FOR SERIAL PRINTER)
P9	RS232C # 3 (FOR MODEM)

TABLE 3. CONNECTOR ASSIGNMENT OF THE TS 816 BOARD

5.1 POWER CONNECTOR (P1: 5 PIN)

PIN NO.	DESCRIPTION
1	-12 V
2	UNUSED
3	GND
4	+5 V
5	+12 V

TABLE 4. POWER CONNECTOR CONFIGURATION

5.2 RS 232C CONNECTOR (P2,P8,P9: 25 PIN)

PIN NO.	DESCRIPTION	
1	FRAME GROUND	
2	TRANSMIT DATA	
3	RECEIVE DATA	
4	REQUEST TO SEND	
5	CLEAR TO SEND	
7	SIGNAL GROUND	
8	DATA CARRIER DETECT	
15	TRANSMIT CLOCK INPUT	(ONLY IN P9)
17	RECEIVE CLOCK INPUT	(ONLY IN P9)
20	DATA TERMINAL READY	
24	TRANSMIT CLOCK OUTPUT	(ONLY IN P9)
25	(IN P2,RESERVED FOR MANUFACTURER'S USE)	
	(IN P8 & P9, NO CONNECTION)	

NOTE: 1) P9 IS CONFIGURED FOR THE CONNECTION TO A MODEM
P8 IS CONFIGURED FOR THE CONNECTION TO A SERIAL PRINTER
P2 IS CONFIGURED FOR THE CONNECTION TO A TERMINAL
2) POLARITY OF DATA SIGNALS : - (NEGATIVE) : TRUE
POLARITY OF CONTROL SIGNALS : + (POSITIVE) : TRUE

TABLE 5. RS232C CONNECTOR CONFIGURATION

5.3 CARTRIDGE TAPE INTERFACE CONNECTOR (P3: 50 PINS)

PIN NO.	I/O	DESCRIPTION
2	I	-SLD, SELECTED
4	I	-RDY, READY
6	I	-WND, WRITE ENABLED
8	I	-FLG, FLAG
10	I	-LPS, LOAD POINT SENSED
12	I	-FUP, FILE UNPROTECTED
14	I	-BSY, BUSY
16	I	-EWS, EARLY WARNING SENSED
18	O	-RWD, REWIND
20	O	-REV, REVERSE
22	O	-FWD, FORWARD
24	O	-HSP, HIGH SPEED
26	O	-WEN, WRITE ENABLE
28	O	-SL1, UNIT SELECT (2 EXP 0)
30	O	-SL2, UNIT SELECT (2 EXP 1)
32	O	-SL4, UNIT SELECT (2 EXP 2)
34	O	-SLG, SELECT GATE
36	I	-RNZ, READ NRZ DATA
38	I	-RDS, READ DATA STROBE
40	I	-DAD, DATA DETECTED
42	O	-WDE, WRITE DATA ENABLE
44	O	-WNZ, WRITE NRZ DATA
46	O	-TR2, TRACK SELECT (2 EXP 1)
48	I	-WDS, WRITE DATA STROBE
50	O	-TR1, TRACK SELECT (2 EXP 0)

ALL THE ODD NUMBER PINS ARE GROUNDED.

TABLE 6. CARTRIDGE TAPE CONNECTOR CONFIGURATION

5.4 WINCHESTER HARD DISK DRIVE INTERFACE CONNECTOR (P5: 50 PIN)

PIN NO.	I/O	DESCRIPTION
1	O	-DBCK, DATA BUS CHECK
3		(SPARE)
5	O	-SL2, UNIT SELECT (2 EXP 1)
7	O	-SL1, UNIT SELECT (2 EXP 0)
9	I	-ATN, ATTENTION
11	I	-BSY, BUSY
13	I	-TX, TRANSFER
15	O	-TC, TERMINATE CONTROL
17	I/O	-DB7, DATA BUS BIT 7
19	I/O	-DB6, DATA BUS BIT 6
21	I/O	-DB5, DATA BUS BIT 5
23	I/O	-DB4, DATA BUS BIT 4
25	I/O	-DB3, DATA BUS BIT 3
27	I/O	-DB2, DATA BUS BIT 2
29	I/O	-DB1, DATA BUS BIT 1
31	I/O	-DB0, DATA BUS BIT 0
33	I/O	-DBP, DATA BUS PARITY BIT
35	O	-RST, RESET
37	O	-DACK, DATA ACKNOWLEDGE
39	I	-DRQ, DATA REQUEST
41	I	-INT, INTERRUPT
43	O	-CS, CONTROLLER SELECT
45	O	-W, WRITE
47	O	-R, READ
49	O	-A, ADDRESS

ALL EVEN NUMBER PINS ARE GROUNDED.

TABLE 7. WINCHESTER DRIVE INTERFACE CONNECTOR CONFIGURATION

5.5 CENTRONIC TYPE PRINTER INTERFACE CONNECTOR (P4: 40 PIN)

The 40 pin right angle header on the board is different in its pin configuration when compared to the 36 pin connector on the rear panel. Figure 18 shows the physical comparison and table 8 gives the signal association to the pin outs.

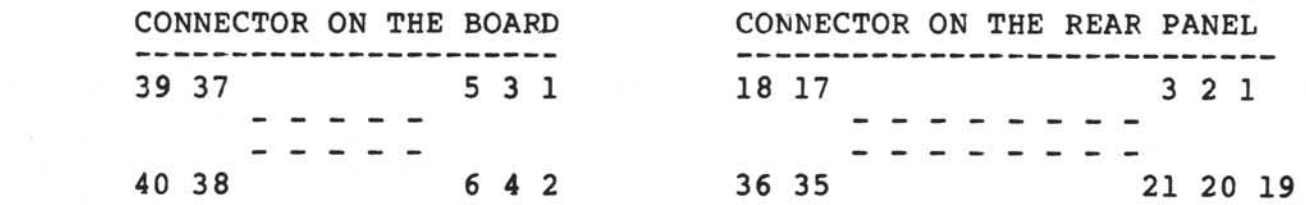


FIG 18. COMPARISON OF TWO CONNECTORS FOR PRINTER

PIN NO. ON REAR PANEL	PIN NO. ON TS 816 BOARD	DESCRIPTION	
1, 19	1, 2*	-DATA STROBE	
2, 20	3, 4*	DATA 0	
3, 21	5, 6*	DATA 1	
4, 22	7, 8*	DATA 2	
5, 23	9, 10*	DATA 3	
6, 24	11, 12*	DATA 4	
7, 25	13, 14*	DATA 5	
8, 26	15, 16*	DATA 6	
9, 27	17, 18*	DATA 7	
10, 28	19, 20*	-ACKNLG	
11, 29	21, 22*	BUSY	
12	23	PE (PAPER EMPTY)	(**5)
30	24	(NOT USED)	(**6)
13	25	SELECT	(**4)
31	26	(NOT USED)	(**8)
14	27	(NOT USED)	(**7)
32	28	-FAULT	(**3)
15	29	(NOT USED)	
33	30	LIGHT DETECT	(**2)
16	31	GND	
34	32	(NOT USED)	
17	33	GND	
35	34	(NOT USED)	
18	35	(NOT USED)	
36	36	(NOT USED)	
	37 THRU 40	(NOT USED)	

* SECOND PIN NUMBER INDICATES RETURN
**2 GROUNDED (NO LIGHT DETECT) IF JUMPER 'W2' IS CONNECTED
**3 ALWAYS HIGH (NO FAULT) IF JUMPER 'W3' IS CONNECTED
**4 ALWAYS HIGH (SELECT ENABLED) IF JUMPER 'W4' IS CONNECTED
**5 GROUNDED (NO PAPER EMPTY) IF JUMPER 'W5' IS CONNECTED
**6 GROUNDED IF JUMPER 'W6' IS CONNECTED
**7 GROUNDED IF JUMPER 'W7' IS CONNECTED
**8 'INPUT PRIME' IS GENERATED IF JUMPER 'W8' IS CONNECTED

TABLE 8. CONFIGURATION OF PRINTER INTERFACE CONNECTOR ON THE BOARD.

5.6 TS 816U INTERFACE CONNECTOR (P6,P6A : 50 PIN)*

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TXD1	26	TXD8
2	-DTR1	27	-DTR8
3	TXD2	28	RXD5
4	-DTR2	29	-RXC5
5	TXD3	30	-DCD5
6	-DTR3	31	RXD6
7	TXD4	32	-RXC6
8	-DTR4	33	-DCD6
9	RXD1	34	RXD7
10	-RXC1	35	-RXC7
11	-DCD1	36	-DCD7
12	RXD2	37	RXD8
13	-RXC2	38	-RXC8
14	-DCD2	39	-DCD8
15	RXD3	40	(NOT USED)
16	-RXC3	41	GND
17	-DCD3	42	TXC1
18	RXD4	43	GND
19	-RXC4	44	TXC5
20	-DCD4	45	(NOT USED)
21	TXD5	46	(NOT USED)
22	-DTR5	47	(NOT USED)
23	TXD6	48	(NOT USED)
24	-DTR6	49	(NOT USED)
25	TXD7	50	-DIAG MODE

* P6 IS TO BE CONNECTED TO THE FIRST TS 816U BOARD IN THE 8 USER INVIRONMENT.IN CASE OF 16 USER ENVIRONMENT, A SECOND TS 816U BOARD IS CONNECTED THROUGH P6A CONNECTOR

TABLE 9. TS 816U INTERFACE CONNECTOR CONFIGURATION

5.7 RESET CONNECTOR (P7: 3 PIN)

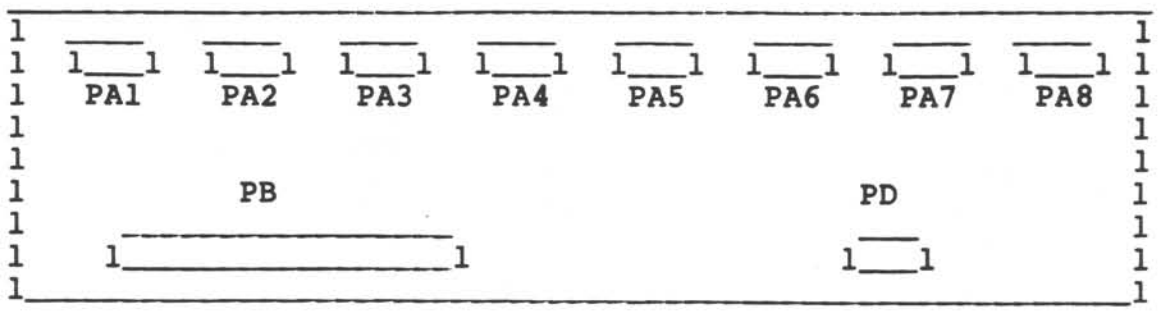
PIN NO.	DESCRIPTION
1	GND
2	RESET SW (NORMALLY HIGH)
3	RESET SW (NORMALLY LOW)

TABLE 10. RESET CONNECTOR CONFIGURATION

5.8 DIAGNOSTIC LED'S

CR2	CR3	CR4	CR5	TEST DESCRIPTION
O	O	O	●	Test Memory Bank 1; if fail light stays on.
O	O	●	O	Test Memory Bank 2; if fail LED blinks and message.
●	O	O	O	Test hard disk; if fail light stays on.
O	O	O	O	Test complete (all lights off)

6.0 CONNECTOR CONFIGURATION OF TS 816U BOARD



PA1 ~ PA8 RS422 USER INTERFACE
PB TS 816 INTERFACE
PD POWER

FIG. 19 CONNECTOR CONFIGURATION OF TS 816U BOARD

6.1 CONNECTOR OF RS422 USER INTERFACE(PA1 THRU PA8: 15 PINS)

PIN NO.	DESCRIPTION
1	SHIELD GROUND
2	TXD
3	RXD
4	RTS
5	CTS
6	-TXC
7	-RXC
8	SIGNAL GROUND
9	-TXD
10	-RXD
11	-RTS
12	-CTS
13	TXC
14	RXC
15	(RESERVED)**

** PIN 15 OF PA1 IS CONNECTED TO PIN 50 OF PB. THIS IS USED FOR DIAGNOSTICS PURPOSES.

TABLE 11. CONNECTOR CONFIGURATION OF RS422 USER INTERFACE

6.2 CONNECTOR CONFIGURATION OF TS 816 INTERFACE(PB: 50 PIN)

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TXD1	26	-DTR7
2	-DTR1	27	TXD8
3	TXD2	28	-DTR8
4	-DTR2	29	RXD5
5	TXD3	30	-RXC5
6	-DTR3	31	-DCD5
7	TXD4	32	RXD6
8	-DTR4	33	-RXC6
9	RXD1	34	-DCD6
10	-RXC1	35	RXD7
11	-DCD1	36	-RXC7
12	RXD2	37	-DCD7
13	-RXC2	38	RXD8
14	-DCD2	39	-RXC8
15	RXD3	40	-DCD8
16	-RXC3	41	GROUND
17	-DCD3	42	TXC1
18	RXD4	43	GROUND
19	-RXC4	44	TXC5
20	-DCD4	45	(UNUSED)
21	TXD5	46	(UNUSED)
22	-DTR5	47	(UNUSED)
23	TXD6	48	(UNUSED)
24	-DTR6	49	(UNUSED)
25	TXD7	50	-DIAG MODE

TABLE 12. CONNECTOR CONFIGURATION OF TS 816 INTERFACE

6.3 CONNECTOR CONFIGURATION OF POWER (PD: 5 PINS)

PIN NO.	DESCRIPTION
1	(UNUSED)
2	(UNUSED)
3	GROUND
4	+5V
5	(UNUSED)

TABLE 13. CONNECTOR CONFIGURATION OF POWER

7.0 DIP ADAPTOR PLUG

PLUG NO.	LOCATION
DIP 1	A33
DIP 2	A35

The highest priorty is assigned to the DMA (IEI) by having it tied high at the dip plug adaptors.