## 32 K Memory for Mark-8

By Bryan K. Blackburn 10/2006

In 2006, I built a memory board for my Mark-8 in order to be able to run large programs like SCELBAL and Galaxy (Star Trek), \& etc. The most the Mark-8 can address is 16 K , but the chips I had on hand were 32K. Rather than waste the other 16 K , this design employs bank switching to make better use of the available memory.

The first version did not work. It took me a few minutes to figure out the problem... Duh! The memory chip is a high speed SRAM from an old PC. The memory was done writing before the data latches were finished with address \& etc. So, I added the delay. Now it works just fine.

I'm afraid I did not keep my hook up diagram, but it is pretty simple. Just hook up power and ground, address and data lines, reserving one address line to connect either to a toggle switch (manual bank select) between +5 and Ground or to an unused output port (program controlled bank select). Use the three 'select' lines to pick when the memory will be active-I wired mine to ignore the lower 4 k of addressable space, in order to use my original memory, and to reserve an unswitched portion of program space. Those connections were made directly to my memory card to avoid duplicating the select circuitry.

If you don't know enough about how the Mark-8 works to do this on your own, you should learn more before you begin anyway-now is a good time to start! ©

My memory board was built in a single evening using point-to-point wiring, soldering wire wrap wire to standard sockets on perf board. I hate wire wrap sockets; they take up too much room! I considered ordering a PC board, but I would have had to wait for it! If you decide to do a PC board, make one for me too!!!! ©

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# Write Delay for Fast Memory Chip 



74123

9/06
Using a 15 ns 32 K memory chip, it was found that even with fast buffers, data was not stable at memory chip inputs before the write began or finished (?). Written data was often wrong. $: *$ It is hoped that with this mod, data will have time to stabilize before the write pulse, and that the write cycle will end before data inputs become unstable.

I really think this will work!
P.S., all chips have bypass caps.

Update 10/06: It worked. ©

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