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## Alan R.:Miller



# THE 8080/Z-80 ASSEMBLY LANGUAGE TECHNIQUES FOR IMPROVED PROGRAMMING 

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## Preface

On first thought, it might seem strange that another book on the 8080 and Z-80 should appear at this time. Z-80 CPU cards generally became available in 1977 and the 8080 CPU is even older. But the Z-80 computer seems to become more popular with time. For example, the TRS-80 Model II announced recently by Radio Shack, and Heath's H-89 both use the CPU. High-level languages such as Pascal, APL, BASIC, FORTRAN, and C are now run on the 8080 and Z-80. Furthermore, Microsoft has available a Z-80 CPU card that can be easily inserted into the Apple II computer. There should be an increasing interest in the 8080 and Z-80 CPUs in the coming years, and I believe, a great increase in the number of 8080 and Z-80 programmers. So, there is a growing need for a book that covers programming for the 8080 and Z-80 assembly languages.

The combination of 8080 and Z-80 programming concepts into a single work is quite natural. The Z-80 CPU is upward compatible from the 8080 so that all commercially available 8080 software will run on the Z-80. Furthermore, 8080 assemblers, such as ASM provided with CP/M, can be used to create programs that will run on either an 8080 system or a Z-80 system.

The purpose of this book is twofold. First, I want to provide a single reference source for both 8080 and Z-80 assembly language programmers. The appendixes are designed with this goal in mind. They begin with the ASCII character set and a 64 K memory map. These two appendixes are as useful to those using higher level languages as they are to assembly language programmers.

The 8080 and Z-80 instruction sets are listed both alphabetically and numerically in the next four appendixes. This is followed by a cross reference between the 8080 and the Z-80 mnemonics. An appendix describing each instruction in detail then follows. Common acronyms are identified
next in Appendix I, and some undocumented Z-80 instructions are discussed in the final appendix. Collectively, the appendixes contain all of the reference material needed to write 8080 or Z-80 assembly language programs.

The second purpose of this work is to demonstrate some useful techniques of assembly language programming. As an editor for Interface Age, I have seen numerous examples of inefficient or improper programming. General principles of assembly language programming are discussed in Chapters One through Five; specific programming examples are given in Chapters Five through Ten. The reader can actually assemble the programs and try them out.

The organization and operation of the 8080 and Z-80 CPUs is covered in Chapter One. This includes a discussion of the general-purpose registers, the flag registers, logical operations, branching, double-register operations, rotation and shifting. The concepts of hexadecimal, octal, and binary numbers, one's and two's complement arithmetic, and the use of logical operations are presented in Chapter Two.

Stack operations with PUSH, POP, CALL and RET commands and the passing of data between calling program and subroutine are given in Chapter Three. Chapter Four is devoted to input and output techniques, including an interrupt-dirven keyboard routine and a telephone transmission program. Assembler macros are discussed in Chapter Five. Examples show how to generate Z-80 instructions with an 8080 macro assembler, and how to emulate Z-80 instructions on an 8080 CPU.

The reader can develop a small, powerful monitor in Chapter Six using the top-down programming method. The monitor contains the usual commands of dump, load, and go. In addition, there is a memory test, a routine to search for one or two hex bytes or ASCII characters, a routine to replace all occurrences of one byte with another, and a routine to perform input and output through any port.

In Chapter Seven the monitor is converted to Z-80 instructions and some additional features are added. Assembly-language subroutines for interconverting between binary numbers and ASCII characters coded in one of the common number bases are given in Chapter Eight. These routines perform all of the input and output through the system monitor developed in Chapter Six. Paper tape and magnetic tape routines are given in Chapter Nine. This method of data transfer is still very popular. I frequently am asked to read information on paper tape into our Z-80 computer so that it can be transmitted over the telephone line to our campus Dec- 20 computer.

CP/M is currently the most popular 8080/Z-80 operating system. Chapter Ten demonstrates how assembly language programs can utilize CP/M for all input and output by presenting three programs. One of these programs allows the user to branch to any address from the system level. Nevertheless, the use of $\mathrm{CP} / \mathrm{M}$ is not the subject of this book. More information on the use of the $\mathrm{CP} / \mathrm{M}$ operating system can be obtained from Using $C P / M: A$ Self-Teaching Guide by Judi Fernandez and Ruth Ashley (John Wiley and Sons, Inc., 1980).

The assembly language programs in this book have all been assembled on an Altair 8800, with an Ithaca Z-80 CPU card and North Star doubledensity disks. The Lifeboat 2.0 version of CP/M was used as the operating system. The system monitor given in Chapter Six was additionally programmed to run on a TRS-80 Model II, using a Lifeboart 2.2 version CP/M operating system. The alternate version of the input and output routines was used in this case. The Digital Research assembler MAC was used for the 8080 instructions and the Microsoft assembler MACRO-80 was used for the Z-80 code. All of the assembly listings have been reproduced directly from the original computer printouts. The manuscript was created and edited with MicroPro's Word-Master and formatted with Organic Software's Textwriter.

Thanks to Heidi for typing the manuscript. Also, I should like to acknowledge the programmers at Microsoft, Digital Research, and Lifeboat Associates for the many things they have taught me about programming.

Alan R. Miller
June 1980

## Contents

Chapter One Introduction ..... 1The 8080 CPU, 3The Memory Register, 5The Flag Register, 5Flags and Arithmetic Operations, 6Flags and Logical Operations, 7Increment, Decrement, and Rotate Instructions, 8Rotation of Bits in the Accumulator, 9
Flags and Double-Register Operations, 10
The Z-80 CPU, 10
Z-80 Relative Jumps, 12
Z-80 Double-Register Operations, 13
Z-80 Input and Output (I/O) Instructions, 14
Shifting Bits, 14
Chapter Two Number Bases and Logical Operations ..... 16
Number Representation in Binary, BCD, and ASCII, 19
Logical Operations, 20
The Two's Complement, 21
Logical OR and Logical AND, 23
Setting a Bit with Logical OR, 24
Resetting a Bit with Logical AND, 25
Logical Exclusive OR, 26
Logical NAND and NOR gates, 26
Making Other Gates, 28
Chapter Three The Stack; ..... 30
Storing Data on the Stack, ..... 31
The Accumulator and PSW as a Double Register, ..... 34
Z-80 Index Registers, ..... 35
Subroutine Calls, 35
Passing Data Improperly to a Subroutine, 37
Passing Data Properly to a Subroutine, 37
Passing Data Back from a Subroutine, 39
Setting up a New Stack, 40
Calling a Subroutine in Another Program, 41
Calling One Subroutine from Another, 42
Bypassing a Subroutine on Return, 43
A PUSH Without a POP, 44
Getting Back from a Subroutine, 44
Automatic Stack Placement, 45
Chapter Four Input and Output ..... 48
Memory-Mapped I/O, 48
Distinct Data Ports, 49
Looping, 50
Polling, 52
Hardware Interrupts, 52
An Interrupt-Drive Keyboard, 55
Scroll Control and Task Abortion, 64
Data Transmission by Telephone, 64
Parity Checking, 66
Chapter Five Macros ..... 69
Generating Three Output Routines with One Macro, 71
Generating Z-80 Instructions with an 8080 Assembler, 73
Emulating Z-80 Instructions with an 8080 CPU, 75
The Repeat Macros, 77
Printing Strings with Macros, 79
Chapter Six Development of a System Monitor ..... 85
Program Development Details, 86
Version 1: The Input and Output Routines, ..... 87
Version 2: A Memory Display, 95
Version 3: A CALL and GO Routine, 100
Version 4: A Memory-Load Routine, 101
Version 5: Useful Entry Points, 103
Version 6: Automatic Memory Size, 105
Version 7: Command-Branch Table, 107
Version 8: Display the Stack Pointer, 109
Version 9: ZERO and FILL routines, 110
Version 10: A Block-Move Routine, 111
Version 11: A Search Routine, 113
Version 12: ASCII Load, Search, and Display, 115
Version 13: Input and Output to Any Port, 117
Version 14: Hexadecimal Arithmetic, 119
Version 15: Memory-Test Program, 120
Version 16: Replace One Byte with Another, 121
Version 17: Compare Two Blocks of Memory, 123
Automatic Execution of the Monitor, 125
Chapter Seven A Z-80 System Monitor ..... 128
Conversion of the Monitor to Z-80 Mnemonics, ..... 143
Reducing the Monitor Size, 144
Getting More Free Space, 145
Peripheral Port Initialization, 146
Printer Output Routines, 147
Delay After a Carriage Return, ..... 148
Chapter Eight Number-Base Conversion ..... 150
The ASCII Code, 150
Conversion of ASCII-Encoded Binary Charactersto an 8-Bit Binary Number in Register C, 152Conversion of ASCII Decimal Charactersto a Binary Number, 156Conversion of ASCII Hexadecimal Charactersto a 16-Bit Binary Number In HL, 159
Conversion of Two ASCII Hexadecimal Charactersto an 8-Bit Binary Number in Register C, 162Conversion of ASCII Octal Charactersto a 16-Bit Binary Number in Register HL, 163
Conversion of Three ASCII Octal Charactersto an 8-Bit Binary Number in Register C, 166
Conversion of Two ASCII BCD Digits to an 8-Bit Binary Number in Register C, 168
Conversion of an 8-Bit Binary Number in C to a String of Eight ASCII Binary Characters, 169
Conversion of an 8-Bit Binary Number into Three ASCII Decimal Characters, 172
Conversion of a 16 -Bit Binary Number into Five ASCII Decimal Characters, 175
Conversion of an 8-Bit Binary Number into Two ASCII Hexadecimal Characters, 178
Conversion of a 16 -Bit Binary Number into Six ASCII Octal Characters, 180
Conversion of an 8-Bit Binary Number into Three ASCII Octal Characters, 181
Conversion of a 16 -Bit Binary Number to Split Octal, 182
Chapter Nine Paper Tape and Magnetic Tape Routines ..... 187
The Checksum Method, 188An ASCII-Hex Tape Program, 188A Tape-Labeling Routine, 203A Binary Tape Monitor, 204
Chapter 10 Linking Programs to the CP/M Operating System ..... 214 CP/M Memory Organization, 216
Changing the Peripheral Assignment, 217
Incorporating the IOBYTE into Your CBIOS, 219
Using STAT to Change the IOBYTE, 225
A Routine to Go Anywhere in Memory, 226
A List Routine with Date and Time, 229
Copy a Disk File into Memory, 242
Appendixes A. The ASCII Character Set ..... 253
B. A 64 K Memory Map ..... 255
C. The 8080 Instruction Set (Alphabetic) ..... 258
D. The 8080 Instruction Set (Numeric) ..... 261
E. The Z-80 Instruction Set (Alphabetic) ..... 264
F. The Z-80 Instruction Set (Numeric) ..... 272
G. Cross-Reference of 8080 and Z-80 Instructions ..... 280
H. Details of the Z-80 and 8080 Instruction Set ..... 283
I. Abbreviations and Acronyms ..... 311
J. Undocumented Z-80 Instructions ..... 313
Index ..... 317

## CHAPTER ONE

## Introduction

There was a time when computers were gigantic machines containing racks upon racks of vacuum tubes. The invention of the transistor and the development of the integrated circuit (IC) changed all that. Today, it is possible to place tens of thousands of transistors on a single "chip" of silicon that is smaller than a quarter of an inch square. As a result of this technology. computers have become smaller and cheaper.

Computers are commonly classified into three categories, based on size and capability. The largest are known as main frame computers, the middlesized ones are called minicomputers, and the smallest are termed microcomputers. A computer consists of three parts: the central processing unit (CPU), the main memory, and the peripherals.

The CPU directs the activities of the computer by interpreting a set of instructions called operation codes, or op codes for short. These instructions are located in the main memory. The memory is also used for the storage of data.


The CPU communicates with the user through such peripherals as the console, the printer, the disks, and so on. There are several electrical lines which are used to connect the CPU to the memory and to the peripherals. These lines are collectively known as the buss, or bus.

The CPU contains a set of registers, which are internal memory locations used for data storage and manipulation. One of these is a special register
called the accumulator. It receives the results of certain CPU operations. The CPU will also have a status register to indicate the nature of a previous operation, e.g., whether the result is zero or negative or positive. It will also indicate whether a carry or a borrow occurred during the operation.

Additional registers are used for auxiliary storage. They may contain general information such as a number that is about to be added to the accumulator. Alternately, a register may contain a number that refers to an address in the main memory. The value is called a memory pointer in this case. A special portion of main memory may be set aside for storing data. This area is called a stack. A special register called a stack pointer refers to this region. Another register, the program counter, tells the CPU where to find the next instruction in memory.

Computer operations are controlled by a computer program. Those programs which are used to solve engineering and physics problems are called application programs. On the other hand, computer programs which deal with the operation of the computer's own peripherals are known as systems programs.

The instruction set used by the CPU can be very large and difficult to use. Consequently, symbolic programming languages are commonly used instead. An application program may be written in a language such as BASIC, FORTRAN, or Pascal. This is called a source program. Then a separate processor program called a compiler or an interpreter is used to convert the user's source program into an object program that corresponds to the instructions needed by the computer.

A microcomputer's instruction set is relatively small compared to that of a larger computer. But even so, it is more convenient to write systems programs in a symbolic language called assembly language, rather than in the machine language of the computer. A processor program, called an assembler, is then utilized to translate the source program into the corresponding instructions of the computer. A major difference between assembly language and higher-level languages such as Pascal is that each line of an assembly language program represents one computer instruction. By contrast, one line of a Pascal source program might represent many computer instructions.

A line of an assembly language program can contain up to four elements: the label, the mnemonic, one or two operands, and a comment.

| Label Mnemonic oferand | Commert |
| :--- | :---: | :---: |
| START: | CALL |
| FIRST |  |

The label, which is usually terminated by a colon, is used to transfer control from one portion of the source program to another. The mnemonic represents the desired CPU instruction. The operand might reference a CPU register, a memory location, or simply a constant. Finally, a comment, preceded by a semicolon, can be used to explain the instruction. The comment, of course, is ignored by the assembler.

The remainder of this chapter is devoted to a general discussion of some of the features of the 8080 and Z-80 CPUs. The complete instruction sets
for these CPUs are listed in the appendix. Specific details of each instruction are given in Appendix H. If you are already familiar with these instruction sets, then you might want to go on to the next chapter.

## THE 8080 CPU

The 8080 CPU is an integrated circuit that has 40 pins (legs). It requires three power supply voltages $-12 \mathrm{~V}, 5 \mathrm{~V}$, and -5 V , and a two-phase clock that runs at $2 \mathrm{Megahertz}(\mathrm{MHz})$. There is an accumulator, a flag register, six general-purpose registers, a stack pointer, and a program counter. The accumulator is sometimes known as register A. The flag register is usually called the PSW (the letters being an acronym for program status word). The general-purpose registers are designated by the letters $\mathrm{B}, \mathrm{C}, \mathrm{D}, \mathrm{E}, \mathrm{H}$, and L . Sometimes the registers are paired into 16 -bit double registers known as BC , DE , and HL. The accumulator and flag register may also be paired. There are 78 different instruction types that produce a total of 245 different op codes.


Figure 1.1. The 8080 CPU registers.
Some of the 8080 instructions explicitly refer to the accumulator or to one of the general-purpose registers ( $B, C, D, E, H$, and $L$ ).

| remor | oferand | comment |
| :---: | :---: | :---: |
| INR | A | 仑increment accumulator |
| ICR | H | foecrement resister $B$ |
| MOV | M, D | imove conterits of II to |
| MUI | Cu4 | ffut value of 4 irito $C$ |

When there are two operands, data moves from the right operand (the source) into the left operand (the destination). There are additional 8080 commands that implicitly refer to the accumulator.

| mriemoric | operand |  | comment |
| :---: | :---: | :---: | :---: |
| RAR |  | \% | rotate accumulator risht |
| RAL |  | ¢ | rotate accumulator left |
| IN | 0 | t | infut a bute to A fromport 0 |
| QUT | 1 | ¢ | output a bute from A to fort 1 |
| ANI | 7 | ; | losical AND with $A$ and 7 |
| ORI | 3 | \% | losical OR with $A$ and 3 |

For certain 8-bit operations, the accumulator is implicitly one of the source registers and will contain the result of the operation.

| mriemonic oferand |  |
| :---: | :---: |
| ADI | C |
| SUR | II |
| ANA | $H$ |
| ORA | $\mathbb{B}$ |

    commerit
    - add C to A
و subtract in from A
t losical AND of A with H
; losical OR of $A$ and $B$

Other instructions refer to coupled pairs of 8-bit registers. These extended operations treat the BC , the DE , and the HL register pairs as 16 -bit entities. Sometimes the stack pointer and program counter are included in these instructions. The X symbol in the mnemonic refers to these extended 16-bit operations.

| memonic | oper |  | commerit |  |
| :---: | :---: | :---: | :---: | :---: |
| INX | H | \% | incremerit | HL resister fa |
| ncx | SP' | \% | decremerot | stack Fointer |
| LXI | 11.0 | ; | load zero | into DE Fair |

Additional instructions deal specifically with the HL register pair. The following two instructions move two bytes of data between memory and the HL double register.


The LHLD instruction copies the value at memory location 3 into the L register and the value at location 4 into the $H$ register. The SHLD operation reverses the process.

The XCHG operation interchanges the 16 -bit HL register pair with the 16-bit DE register pair.


The SPHL command copies the HL register into the stack pointer register. The PCHL instruction copies the HL register pair into the program counter register.

There are several instructions that perform double-register addition. The number in one of the 16 -bit registers is added to the number in HL. The sum appears in the HL register pair.

| nAD | D | gadd IIE to HL |
| :--- | :--- | :--- |
| DAD | SF | istack pointer +HL |

## THE MEMORY REGISTER

There is another 8 -bit register for the 8080 that is not shown in Figure 1.1. It is located in main memory. The 16 -bit address contained in HL defines the location of this memory register, i.e., HL is a memory pointer. The instruction

MOU M,E $\quad$ move $E$ to memors
will copy the contents of register $E$ into the memory location pointed to by the HL register pair. The instruction

INR M . M increment memory
will increment this byte in memory.

## THE FLAG REGISTER

Four bits of the PSW register can be used to control program flow. The bits or flags are used in conjunction with conditional jump, conditional call, and conditional return instructions. We say that a flag is set if it has a value of 1 or is reset if it has a value of zero.

The CPU sets the sign flag (S) if the result of a previous operation is positive; the flag is reset if the result is negative. The CPU sets a second flag, the zero flag ( Z ), if the result is zero; it is reset if not zero. A third flag, the carry flag (C), is set if there is a carry on addition or borrow on subtraction; it is reset otherwise. A fourth flag, the parity flag (P), indicates the parity of the result. Parity is even if there is an even number of ones (or zeros) and odd otherwise.


Figure 1.2. The PSW (flag) register.
The use of the flag register can be demonstrated with a simple routine. Suppose that a group of instructions is to be executed eight times. The following code will do this.

|  | MUI | B, 8 | frut 8 into B |
| :---: | :---: | :---: | :---: |
| LOOF: | - + |  |  |
|  | $\stackrel{+}{\text { ICR }}$ | B | A decrement B |
|  | JNZ | LOOF' | ¢loof if rot zero |

The B register is initialized to the value of 8 . The DCR B instruction near the end of the loop decrements the B register each time the loop is executed. This will reset the zero flag on each of the first seven passes through the loop since $B$ has not reached zero. The following conditional jump instruction, JNZ LOOP, causes the CPU to return to the line labeled LOOP in this case.

On the eighth pass through the loop the original value of 8 in the $B$ register will have been decremented to zero. Now the zero flag will be set and the conditional jump instruction will not cause a branch. The instruction immediately following the jump will be executed instead.

## FLAGS AND ARITHMETIC OPERATIONS

The results of addition and subtraction operations can be characterized from the PSW flags. Three of the flags are of interest here: "the carry flag, the zero flag, and the sign flag. If the sum of two numbers exceeds 255 ( 1 less than 2 to the eighth power), then the result is too large to fit into the 8 -bit accumulator. The carry flag will be set to reflect this overflow. During subtraction, the carry flag is set when a larger number is subtracted from a smaller one. In this case, the flag becomes an indication that borrowing has taken place.

Sometimes all eight bits of a register or memory location are used to represent a number. This is then an unsigned number. At other times it is convenient to utilize only the low-order seven bits (bits 0-6) for the magnitude of a number. The remaining high-order bit (bit 7) is then used to indicate the sign.

unsisned number


Numbers represented in this way are known as signed numbers. A 0 in bit 7 means that the number is positive and a 1 means that the number is negative. An 8-bit signed number can range in magnitude from -128 to 127, whereas an unsigned 8 -bit number can range from 0 to 255 .

The sign flag is set after certain operations if the value of bit 7 is 1 and it is reset if bit 7 is 0 . If the sum of two numbers is exactly 256 , the result in the 8 -bit accumulator will be a zero. This occurs because 256 is 1 greater than the largest 8 -bit number (255). The zero flag will be set in this case. In addition, the carry flag will be set because there is an overflow. The parity
flag will be set, since there is an even number of ones. (Zero is an even number.) Finally, the sign flag will be reset because bit 7 is a zero.

## FLAGS AND LOGICAL OPERATIONS

In the case of arithmetic operations such as addition and subtraction, there can be a carry or borrow from one bit to another. But the logical operations AND, OR, and XOR (exclusive OR) operate on each bit separately; there is never a carry from one bit to the next. These logical operations, therefore, always reset the carry flag. The zero and parity flags, however, will be set or reset according to the result of the particular operation. We will discuss logical operations more fully in Chapter 2.

A value in the accumulator can be compared to a value in another register or to the byte immediately following the instruction byte in memory. The CPU performs the comparison by subtracting the value of the operand from the value in the accumulator. In the case of a regular subtraction, the difference is placed in the accumulator. For example, the arithmetic instruction

SUB C
subtracts the value in register C from the accumulator and places the difference into the accumulator. The logical comparison operation

## CMF C

also subtracts the value in register C from the value in the accumulator. However, unlike the regular subtraction operation, the difference in this case is not actually saved. The flags, of course, will reflect the result of the operation. If the value in C is equal to the value in the accumulator the difference between them will be zero. In this case the zero flag is set indicating the equality. The carry flag will be reset since there was no borrow during the subtraction.

If the two values are not equal, then A is either larger or smaller. If A is larger, the comparison operation will reset the carry flag (and, of course, the zero flag). If A is smaller, then the carry flag will be set, because a larger number has been subtracted from a smaller one. Thus, if the carry flag has been set after a comparison, then the value originally in the accumulator must have been smaller than the value with which it was compared.

The following instructions can be used to determine if the value in register C is less than, greater than, or equal to the value in the accumulator.

| CMF | c | \% | subt | act | A from | C |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $J Z$ | ZERO | $\hat{\text { b }}$ | if $A$ | equa | 15 C |  |
| JC | LESS | ¢ | if $A$ |  | than |  |
| - |  | \% | if $A$ | sreat | ter t |  |

The comparison instruction is executed first. This operation subtracts the value of C from the value in the accumulator. If the two numbers are equal, then their difference is zero. In this case, the zero flag is set and the JZ instruction causes a branch to the label ZERO. Otherwise, the next instruction is executed. Another possibility is that the value in C is greater than the value in the accumulator. The subtraction in this case requires a borrow so the carry (borrow) flag is set. The JC instruction then causes a branch to the label LESS. The last possibility is that the value in the accumulator is larger than that in register C. For this case, both the zero and the carry flags are reset, and the program continues.

## INCREMENT, DECREMENT, AND ROTATE INSTRUCTIONS

The 8-bit increment and decrement instructions present an interesting case. Mathematically, the increment operation simply adds 1 to the current value in a register. Likewise, the decrement operation subtracts 1 from the present value. Thus, the two instructions

| INR | $A$ | and |
| :--- | :--- | :--- |
| AIII | 1 |  |

both increase the value in the accumulator by 1 and the operations

| UCR | $A$ | and |
| :--- | :--- | :--- |
| SUI | 1 |  |

both decrease the value in the accumulator by 1 . The zero, parity, and sign flags correctly reflect the result in all cases.

The carry flag, however, responds differently for the two cases. The flag correctly reflects the result of the operation in the case of addition, but it is unaffected in the case of an increment or decrement operation. Thus, if you need to increment or decrement a value without disturbing the carry flag, then you should use the INR or DCR instructions. On the other hand, if you need to know whether a carry or borrow occurred during an increment or decrement, then use an add or subtract operation.

The instructions following the label GETCH in Listing 6.1 (in Chapter 6) are used to set ASCII characters from the console input buffer. As each character is obtained, the count of the remaining characters is decremented. When the count has been decremented past 0 , then the routine is finished. Subtracting 1 from 0 requires a borrow so the carry flag should be set. But since the regular decrement operation doesn't alter the carry flag, the subtract instruction must be used instead.

## ROTATION OF BITS IN THE ACCUMULATOR

There are four 8080 instructions that rotate the bits in the accumulator. The operations move each bit by one position. Two instructions rotate the bits to the right and two rotate them to the left. The right circular rotation

## RRC

moves each bit one position to the right. The rightmost (low-order) bit is moved to the high-order bit and into the carry flag.


The left circular rotation
RLC
moves the bits the other way.


Each bit is moved one position to the left. The high-order bit goes to both the low-order bit and to the carry flag.

The rotate accumulator right instruction
RAF
moves each bit one position to the right. But this time, the carry flag moves into the high-order bit and the low-order bit moves into the carry flag.


The instruction
RAL
moves each bit one position to the left. The carry flag moves into the loworder bit and the high-order bit moves into the carry flag.


## FLAGS AND DOUBLE-REGISTER OPERATIONS

Double-register, or extended, operations involving HL, DE, and BC affect the flags very differently from the single-register operations. We saw that singleregister increment and decrement operations did not alter the carry flag. The extended increment and decrement commands never alter any of the flags. This means that if a program is to loop until a double register has been decremented to zero, the following set of instructions will not work.

The proper procedure is to compare the two 8 -bit halves with each other. This can be done by moving one of the registers to the accumulator.

Then the accumulator is compared to the other half by performing a logical OR. The result of this operation will set the zero flag only if both halves are zero. The complete operation looks like this.


The double-register add instruction correctly sets the carry flag if there is an overflow from the 16 bits, but zero, parity, and sign flags are not altered.

## THE Z-80 CPU

The Z-80 CPU is a 40 -pin IC just like the 8080 . All of the 8080 instructions are common to the Z-80, thus we say the Z-80 is upward compatible from the 8080 . In general, any program that runs on an 8080 will also run on a

Z-80. The one exception is that the 8080 parity flag is affected by arithmetic operations, while the Z-80 parity flag is not. Thus, one can use an 8080 assembler to generate 8080 code on a Z-80.

The Z-80 requires only a single 5 -volt power supply and a single-phase clock that can run as fast as 6 MHz . There are 158 instruction types that give a very large number of total commands with all variations. These are given briefly in Appendixes E and F and in more detail in Appendix H. The Z-80 contains all of the 8080 general-purpose registers, plus an alternate set for easy interrupt processing. The alternate set is indicated with a prime symbol: $\mathrm{A}^{\prime}, \mathrm{B}^{\prime}$, and so on. Only one of the two general sets of registers can be used at any time, therefore, data cannot be transferred directly from one set to the other. There are also two 16 -bit index registers called IX and IY, an 8-bit interrupt register (I), and an 8-bit refresh register (R).


Figure 1.3. The Z-80 CPU registers.
An operand for an assembly-language instruction may consist of a value that is used directly, or it may refer to a location that contains the value. For example, the command
LII A.G
instructs the CPU to place the value of 6 into register A. Similarly, the instruction

LII AgD
will move the contents of register D into register A. Alternately, the operand may be a pointer to another location. Thus the command

LD $\quad A,(6)$
will move the byte located at address 6 into the accumulator. Similarly, the instruction

LD $A \rho(H L)$
tells the CPU to move the byte pointed to by the HL register into the accumulator. The Z-80 mnemonics clearly differentiate a pointer by means of the parentheses, whereas the corresponding 8080 mnemonics do not make such a clear distinction.

## Z-80 RELATIVE JUMPS

Computer instructions are generally executed in order, one after the other. But it is sometimes necessary to branch out of the normal sequence of statements. Branching statements can be classified as either conditional or unconditional. An unconditional or absolute branch always causes the computer to execute instructions at a new location, out of the normal flow. Conditional branching, on the other hand, is based upon the condition of one of the flags.

Programs utilizing the Z-80 instruction set can be significantly shorter than those written with 8080 operation codes, especially if the relative jump instructions are used. Relative jumps are performed by branching forward or backward relative to the present position. Absolute jumps, on the other hand, are made to a specific memory location. Furthermore, there are both unconditional and conditional branch instructions. The absolute, unconditional jump op code and the conditional jump codes based on the state of the zero and parity flags are all three-byte instructions.

| $J P$ | ADDR1 | ¢ | unicond | 31 | jumber |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| JP | ZgAlLIRE2 | ¢ | Jumb if | zero | flas | set |
| JP | NZ, ADMR3 | \% | jump if | zero | ples | reset |
| JP | C.ADLIR4 | \% | jumb if | carry | flas | set |
| JF | NC, ALIARS | ¢ | Jumife if | carry | P13s | rese |

The above instructions are available on both the 8080 and the Z- 80 CPUs. In addition, the $\mathrm{Z}-80$ has a relative, unconditional jump and five relative, conditional jumps.

| JR | ALIDR | \$ | unconditional | , |
| :---: | :---: | :---: | :---: | :---: |
| JR | Z.ADNRG | ; | zero |  |
| JR | NZ, ADMR7 | ¢ | not zero |  |
| JR | C, ADIIR8 | ¢ | carry |  |
| JR | NC, ADDR9 | ¢ | not carrs |  |
| IIJNZ | ALIDR10 | ¢ | decry jump not | zer |

The relative jumps are only two bytes long as opposed to three bytes for the regular jumps, but the relative jump is limited to a displacement of less than 126 bytes forward or 128 bytes backward from the address of the current instruction. These numbers derive from the magnitude of the signed 8 -bit displacement. Bit 7 is used for the sign of the number. A 0 in bit position 7 means a forward or positive displacement, a 1 in this bit position means a backward or negative displacement. The remaining seven bits are used for the magnitude of the jump.

Absolute jumps are specified with a 16-bit address that gives the new location. Relative jumps on the other hand are position-independent. The resulting code can be placed anywhere in memory. The last operation above, DJNZ, is a combination of two instructions. The B register is decremented. If the result is not zero, then there is a relative jump to the given argument ADDR10. This two-byte instruction requires four bytes on an 8080 CPU.

## Z-80 DOUBLE-REGISTER OPERATIONS

While some of the Z-80 instructions appear to be shorter than their 8080 counterparts, they may not actually reduce the program size. Suppose, for example, that we want to move a block of data from one memory location to another. There is a single Z-80 instruction for accomplishing this task. The problem is that no verification is performed during the move. Thus, if there were no memory at the new location, or if the memory were defective, this fact would not immediately be discovered. If you want to check each location as the data are moved, then the Z-80 block-move instruction cannot be used.

A better way to move data is to define the beginning of the original memory block with HL and the end with DE. The BC register defines the beginning of the new block. We can work our way through the original block by incrementing HL and BC at each step along the way.

The end of the block can be detected when HL exceeds DE. We subtract the two 16 -bit registers and observe the carry flag. The HL register pair will initially be less than the DE pair. Therefore, if we subtract DE from HL, we will set the carry (borrow) flag.

Eventually, the number in the HL register will equal the value in the DE pair. This time, the subtraction will not set the carry flag and the task will be completed. Since the 8080 doesn't have a 16 -bit subtract instruction, the routine might look like this.

| LOOP: | - * . |  | ¢ | 8080 ver | ion |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MOUE | AgL | ; | GET L |  |  |
|  | SUB | E | ; | SUBTRACT | $E$ |  |
|  | MOU | A, H | t | GET H |  |  |
|  | SBB | $\square$ | ; | SUBTRACT | 11 AND | EORFROW |
|  | JC | LOOP | ¢ | IF NOT How | NE |  |
|  | RET |  |  | HONE |  |  |

As long as HL is less than DE , the subtraction will set the carry flag and the loop will be repeated. But as soon as HL equals DE, the carry flag will be reset and the subroutine is finished.

The Z-80 has a 16 -bit subtract instruction that can simplify the operation. But since the result of the subtraction is placed in the HL register pair rather than in the accumulator, the data originally present in HL will have to be saved somewhere else, say, on the stack. The Z-80 code is:


The necessary Z-80 instructions require just as many bytes as the corresponding 8080 code. And if the carry flag on the Z-80 has not been reset by a previous instruction, it will have to be reset at the beginning with a logical OR instruction. This latter problem occurs because the Z-80 16-bit subtraction includes the carry flag in its calculations.

## Z-80 INPUT AND OUTPUT (I/O) INSTRUCTIONS

A useful pair of Z-80 instructions deals with input and output, i.e., the transfer of data between the CPU and peripherals such as the console, the printer, and the disk. The 8080 can only input and output data from the accumulator, and the address of the peripheral device must immediately follow the IN or OUT instruction in memory.

| OUT | 10 |
| :--- | :--- |
| IN | 11 |

This usually means that for read-only memory (ROM), there must be separate input and output routines for each peripheral.

In contrast, the Z-80 can input or output a byte from any of the general-purpose registers when the peripheral address is in the C register. In this case, it may be possible to use a single set of I/O routines for all peripherals. This approach is discussed more fully in Chapter 4.

## SHIFTING BITS

The Z-80 CPU extends the four 8080 rotate instructions to the generalpurpose registers B, C, D, E, H, and L. The memory byte referenced by HL, IX, and IY is also included.

The Z-80 instruction set includes three shift operations. Shifts are similar to rotations since each bit moves one position and the bit that is
shifted out of the register is moved into the carry flag. The difference is in the bit that is shifted into the register.

The arithmetic shift left

SLA
shifts all bits to the left. A zero bit moves into the low-order bit.


The operation doubles the original 8 -bit value. This operation can be performed on the accumulator of an 8080 by using an

AIID A
instruction.
A logical shift right
SRL
is the inverse of the arithmetic shift left operation. Each bit shifts one position to the right. A zero bit is shifted into the high-order position.


This operation halves the original 8 -bit value. The carry flag is set if the original value was odd, that is, if there is a remainder from the division.

The arithmetic shift right

## SRA

shifts each bit one position to the right, but the original high-order bit is unchanged.


This operation can be used to divide a signed number in half. The high-order bit, the sign bit, is unchanged. As with the logical shift right, the carry flag is set if the original number was odd.

## CHAPTER TWO

## Number Bases

## and Logical Operations

In this chapter we will consider how numbers are stored in a computer. We will also look at some of the operations that can be performed on these numbers. But first we will review the representation of numbers in general. When we write a number such as 245 , we usually mean the quantity 5 plus 40 plus 200.


This is the ordinary decimal or base-10 representation of a number. The rightmost digit gives the number of units. The digit immediately to the left is the number of tens (the base). The next digit to the left is the number of 100s (the base squared).

In assembly language programs it is sometimes convenient to represent numbers with a base of 2,8 , or 16 . In the octal, or base- 8 , system, for example, the number 245 is equivalent to the decimal number 165 ( 5 plus 32 plus 128).

| 245 | (octal) |
| :---: | :---: |
|  | $5 \times 1=5$ |
|  | $4 \times 8=32(4 \times$ the base $)$ |
|  | $2 \times 64=128$ ( $2 \times$ the base squared) |
|  | 165 (decimal) |

This example demonstrates how to convert numbers from other bases into the decimal representation by adding up the decimal equivalent of each digit.

In the binary, or base- 2 , system, only the digits 0 and 1 are used. The individual digits are called bits, an acronym for binary digits. The rightmost bit represents the units. The bit immediately to the left is the number of 2 s (the base). The next bit to the left is the number of 4 s (the base squared). We continue in this way through all of the bits. For example, the binary number

10100101
is equivalent to the decimal number 165. The conversion is obtained in the following way.


We have seen that the decimal system utilizes ten different digits ( $0-9$ ). The octal system, however, utilizes only eight digits ( $0-7$ ), and the binary system uses only two ( $0-1$ ). The hexadecimal, or base-16, system is also commonly used in computer programs. With this method, we need 16 different digits. The problem is that if we use all of the digits $(0-9)$ from the decimal system, we will still be six digits short. The solution is to use the letters A through F to represent the digits beyond 9. Thus, the hexadecimal number A5 is equivalent to the decimal number 165 . We can convert a hexadecimal number into decimal in the usual way if we remember that A stands for decimal 10, B for 11 , and so on.


The first 16 integers of the decimal, binary, octal, and hexadecimal systems are shown in Table 2.1.

Table 2.2. The first 16 integers represented in various number systems.

| decimal | binary | octal | hex |
| :---: | :---: | :---: | :---: |
| 0 | 0000 | 000 | 00 |
| 1 | 0001 | 001 | 01 |
| 2 | 0010 | 002 | 02 |
| 3 | 0011 | 003 | 03 |
| 4 | 0100 | 004 | 04 |
| 5 | 0101 | 005 | 05 |
| 6 | 0110 | 006 | 06 |
| 7 | 0111 | 007 | 07 |
| 8 | 1000 | 010 | 08 |
| 9 | 1001 | 011 | 09 |
| 10 | 1010 | 012 | 0 A |
| 11 | 1011 | 013 | $0 B$ |
| 12 | 1100 | 014 | 0 C |
| 13 | 1101 | 015 | 0 D |
| 14 | 1110 | 016 | 0 E |
| 15 | 1111 | 017 | 0 F |

Table 2.1 shows the common practice of displaying leading zeros on numbers expressed in bases other than 10. Thus we write 5 for a decimal number, but we may write 005 if it is an octal number or 05 if it is a hexadecimal number. We may explicitly represent the base by a suffix. In books, for example, we typically utilize a subscript in smaller size type. Thus we will write:

| $1010_{2}$ | (binary) |
| :---: | :--- |
| $17_{8}$ | (octal) |
| $17_{10}$ | (decimal) |
| $17_{16}$ | (hexadecimal) |

Alternately, we use suffixes of $\mathrm{B}, \mathrm{Q}, \mathrm{D}$, and H to designate, respectively, binary, octal, decimal, or hexadecimal mode in computer programs where subscripts are not available.

| 1010 B | (binary) |
| :--- | :--- |
| 17 Q | (octal) |
| 17 D | (decimal) |
| 17 H | (hexadecimal) |

(The letter Q is used instead of an O for an octal number to avoid confusion with zero.)

Binary numbers such as
011001101111
can be difficult to read, so it is common practice to represent them in octal or hexadecimal form. Conversion to octal is easy if the bits are grouped by threes.

| 011 | 001 | 101 | 111 | (binary) |
| ---: | ---: | ---: | ---: | :--- |
| 3 | 1 | 5 | 7 | (octal) |

Grouping by fours facilitates the conversion to hexadecimal.

| 0110 | 0110 | 1111 | (binary) |
| ---: | ---: | ---: | :--- |
| 6 | 6 | F | (hexadecimal) |

## NUMBER REPRESENTATION IN BINARY, BCD, AND ASCII

All information is ultimately stored in computers as a series of binary digits. There are, however, several different coding schemes for representing the original data. The simplest method is to use straight binary coding, as shown in Table 2.1. Notice that we might choose to represent a binary value in decimal, octal, or hexadecimal notation. The number itself is unchanged by this. The decimal number 12, for example, is stored as the binary number 1100.

A different method of representing data is called binary coded decimal (BCD). Actually, there are two types of BCD: unpacked and packed. With unpacked $B C D$, each byte contains a single decimal digit from 0 to 9 . Packed BCD can have one or two decimal digits in each byte. Thus, a packed BCD number can range from 0 to 99 . By comparison, an 8 -bit binary number can range from 0 to 255 . Table 2.2 shows the first 16 integers in BCD. The first column gives the decimal equivalent, the second column the corresponding bit pattern.

Table 2.2. The first 16 integers represented in decimal and binary-coded decimal (BCD).

| decimal | BCD |  |
| :---: | :---: | :---: |
| 0 | 00000000 |  |
| 1 | 00000001 |  |
| 2 | 00000010 |  |
| 3 | 00000011 |  |
| 4 | 00000100 |  |
| 5 | 0000 | 0101 |
| 6 | 0000 | 0110 |
| 7 | 0000 | 0111 |
| 8 | 0000 | 1000 |
| 9 | 0000 | 1001 |
| 10 | 00010000 |  |
| 11 | 00010001 |  |
| 12 | 00010010 |  |
| 13 | 00010011 |  |
| 14 | 00010100 |  |
| 15 | 0001 | 0101 |

Notice that the binary representation for the decimal numbers 0 through 9 is the same for both binary and for BCD.

A third method for encoding data is called ASCII. This scheme is commonly used with peripherals such as printers and video terminals. When the key labeled 2 of an ASCII console is pressed, the bit pattern

00110010
is generated. Table 2.3 gives the bit patterns for the ASCII digits $0-9$ in binary and hexadecimal notation.

Table 2.3. The bit pattern for the ASCII digits 0-9.
$\left.\begin{array}{ccc}\text { digit } & \text { binary } & \text { hexadecimal } \\ 0 & 0011 \quad 0000 & 30 \\ 1 & 0011 \quad 0001 & 31 \\ 2 & 0011 & 0010\end{array}\right] 32$

## LOGICAL OPERATIONS

The fundamental operations of a computer involve electrical signals that can have only one of two values. The two voltage levels might be zero and 5 volts, for example, or they might be something else. The actual value is unimportant at this point. Instead, we refer to the two allowable states as TRUE and FALSE. The TRUE state is also called a logical 1, or high state, and the FALSE state is also known as a logical 0 , or low state.

$$
\begin{array}{ll}
\text { TRUE }=1 & \text { (high) } \\
\text { FALSE }=0 & \text { (low) }
\end{array}
$$

Computers store numbers in binary form as a series of 1 s and 0 s . These two possible values correspond to the two possible voltage levels of the electronic circuitry. We can therefore utilize the expressions TRUE and FALSE to describe the state of each bit.

The collection of transistors, resistors, and so forth that makes up the physical computer is called the hardware. The computer program used to direct the activities of the computer is termed the software. In this sense, the hardware and software are distinctly different. But sometimes we use these terms a little differently.

Consider, for example, one of the major differences between minicomputers and microcomputers. Minicomputers contain electronic circuitry for the multiplication of two numbers. Since microcomputers do not contain such circuitry, multiplication is performed instead by executing a special computer program. We say that minicomputers perform multiplication by hardware, but that microcomputers must do multiplication by software.

Hardware operations are performed by electronic devices called gates. The internal structure of the gate is unimportant if we are only interested in the logic of its operation. There are input signal lines that are sampled by the gate, and there is an output signal that is generated by the gate. When we consider the logical operations that are performed by a computer, we can imagine that they are accomplished either by hardware or by software. The answer is the same.

A common logical operation is the complement or inversion of a binary digit. The complement of 0 is 1 and the complement of 1 is 0 . The hardware complement is performed with an inverter or NOT gate. The electronic symbol for this gate, shown in Figure 2.1, is a triangle with one apex to the right (usually) or to the left (sometimes). A small circle or triangle at this apex completes the symbol.


Figure 2.1. The electronic symbol for the NOT or inverter gate.
Letters of the alphabet are used to designate input or output signals. These binary signals can have one of two states, termed TRUE (1) or FALSE (0). The letter A with a bar over it ( $\overline{\mathrm{A}}$ ) represents the complement of A and is called NOT A. A truth table is used to summarize the possible states.

| A | $\bar{A}$ | or | A | $\overline{\text { A }}$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 1 |  | FALSE | TRUE |
| 1 | 0 |  | TRUE | FALSE |

## THE TWO'S COMPLEMENT

If each bit of an 8 -bit byte is complemented, we produce a result that is termed the one's complement of the byte.

$$
\begin{aligned}
& 00001001=9 \\
& 11110110=\text { one's complement of } 9
\end{aligned}
$$

Both the 8080 and the Z- 80 CPUs provide an operation code for complementing the accumulator. A slightly different operation is the two's complement. It is obtained by incrementing (adding 1 to) the one's complement of a number. For example:

```
    0000 1001 = 9
    1111 0110 = one's complement of 9
+0000 0001 add one
    11110111 = two's complement of 9
```

It is interesting to note that the sum of a number and its two's complement is zero.

```
    1010 1010 = 170
    0101 0101 = one's complement of 170
+0000 0001 add one
    0101 0110 = two's complement of 170
    0101 0110 = two's complement of 170
+1010 1010=170
    0000 0000 sum
```

Adding the two's complement of a number produces the same result as subtracting the number itself. For example, we can subtract 170 from 223 by adding the two's complement of 170 . The result is the same.

$$
\begin{aligned}
11011111 & =223 \\
-10101010 & =170 \\
000110101 & =53
\end{aligned}
$$

or

```
    \(11011111=223\)
\(+01010110=2\) 's complement of 170
    \(00110101=53\)
```

The 8080 CPU can perform both addition and subtraction with 8 -bit numbers and it can add 16 -bit numbers, but there is no 16 -bit subtraction operation. We can effectively perform a 16 -bit subtraction, however, by adding the two's complement. Suppose that the HL register pair contains the decimal value 10,005 and we want to subtract 10,000 from it. The difference between 10,005 and 10,000 can be obtained by adding the two's complement. Consider the bit pattern for the number 10,000 .
$0010011100010000=10,000$

We first form the one's complement, then increment the result to form the two's complement.

$$
\begin{aligned}
& 1101100011101111 \\
&+0000000000000001=\begin{array}{l}
\text { one's complement of } 10,000 \\
\text { add one }
\end{array} \\
& \hline 1101100011110000=\text { two's complement of } 10,000
\end{aligned}
$$

Finally, we add this two's complement to the value in HL.

$$
\begin{aligned}
0010011100010101 & =10,005 \text { in HL } \\
+\begin{array}{ll}
110110001110000
\end{array} & =\text { two's complement of } 10,000 \\
\hline 0000000000000101 & \text { difference (sum) is } 5
\end{aligned}
$$

When an assembler encounters a negative argument, it will automatically calculate the corresponding two's complement. Thus the 8080 expression

$$
\text { LXI }=\mathrm{DY}-10000
$$

will place the bit pattern

$$
1101100011110000
$$

in the DE register pair. The instruction

## DAII II

will then effectively perform a 16 -bit subtraction on the number in HL.

## LOGICAL OR AND LOGICAL AND

In the previous section, we considered the logical operation of NOT. Two other important logical operations are OR and AND. Both of these operations reflect the usual English meaning. The logical OR of two bits results in a value of TRUE (1) if either or both the original values are TRUE. The result is FALSE otherwise. The logical AND of two values gives an answer of TRUE (1) if and only if both of the original values are TRUE. If either or both the original values are FALSE, then the answer is FALSE.

Equations of logical operations can be written using the appropriate symbols. Two OR operators are in common use: a plus symbol and a Vshaped symbol. The AND operator is either a dot or an inverted V. The schematic representations of the OR and AND gates are shown with their corresponding mathematical representations in Figure 2.2.



Figure 2.2. The OR and the AND gates.
The truth table is

|  |  | $(\mathrm{OR})$ | $(\mathrm{AND})$ |
| :---: | :---: | :---: | :---: |
| A | B | $\mathrm{A}+\mathrm{B}$ | $\mathrm{A} \cdot \mathrm{B}$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

where zero means FALSE and 1 means TRUE. The origin of the + symbol for the OR operation and $\cdot$ symbol for the AND operation can be seen from the truth table. Logical operations are performed separately on each bit, and there is never a carry. The logical OR (sum) of A and B gives zero if both bits are zero, but 1 otherwise. (Binary digits can't be larger than 1.) The logical AND (product) of A and B gives zero if either or both bits are zero and unity otherwise.

## SETTTING A BIT WITH LOGICAL OR

Sometimes, we need to set one or more bits of the accumulator. We can use the logical OR operation for this purpose. From the truth table in the previous section, we can see that a logical OR of 1 with either a 0 or a 1 will give a result of 1 .

| A | B | A+B |
| :---: | :---: | :---: |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Thus, a logical OR of any bit with a 1 will set that bit. On the other hand, a logical OR of 0 and another bit gives the result of that other bit.

| A | B | A+B |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |

In this case, the second bit is not changed.
Suppose that the accumulator contains a binary 5 and we want to convert it to an ASCII 5.

$$
\begin{aligned}
& 00000101=\text { binary } 5 \\
& 00110101=\text { ASCII } 5
\end{aligned}
$$

If we compare the two bit patterns, we can see that they are the same except for bits 4 and 5 . These bits can be set by executing a logical $O R$ with an ASCII zero.

```
        0000 0101 = binary 5
OR 0011 0000 = ASCII zero
0011 0101 = ASCII 5
```

The OR operation has set the bit corresponding to the location of the 1 , but it has left the other bits unchanged.

A logical OR of a register with itself does not change the value.

$$
\begin{aligned}
01011010 & =5 \mathrm{~A} \text { hex } \\
\text { OR } 01011010 & =5 \mathrm{~A} \text { hex } \\
01011010 & =5 \mathrm{~A} \text { hex }
\end{aligned}
$$

But this operation can be used to set the flags. In this example, the zero, carry, and sign flags are reset and the parity flag is set.

## RESETTING A BIT WITH LOGICAL AND

A logical AND operation can be used to reset any particular bit of the accumulator; the truth table shows how. A logical AND of 0 and either a 0 or a 1 will always give a result of 0 .

| A | B | $\mathrm{A} \cdot \mathrm{B}$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 0 |

Thus, the bit is reset. On the other hand, a logical AND of 1 and another bit will give the value of the other bit.

| A | B | A•B |
| :---: | :---: | :---: |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Thus the AND instruction can be used to reset or "turn off" particular bits. This step is sometimes called a masking AND operation.

When the CPU reads an ASCII character from the console, it gets an 8 -bit byte. But since the ASCII code contains only 7 bits, the high-order bit is not needed. The console-input routine typically resets this bit by performing a masking AND operation. Suppose that the console transmitted an ASCII 5 with the high-order bit set. The bit pattern looks like this.

The high-order bit can be reset with an AND operation.

```
    1 0 1 1 0 1 0 1 ~ ( o r i g i n a l ~ b y t e )
AND 0111 }1111\mathrm{ (mask)
    0011 0101 (ASCII 5)
```


## LOGICAL EXCLUSIVE OR

The ordinary OR operation is sometimes called an inclusive-or operation to distinguish it from the exclusive OR (XOR) operation. For this latter operation, the result is TRUE only if the corresponding bits of both values are different. Either A or B must be TRUE, but not both. The XOR operation is represented by a plus symbol surrounded by a circle. The complement of the XOR is the exclusive NOR or XNOR. It can be used as a comparator. The hardware implementation is sometimes used in circuitry to enable memory boards. The result is TRUE if and only if both corresponding bits are identical. The result is FALSE otherwise. The truth table is:

| A | B | $\mathrm{A} \Theta \mathrm{B}$ | $\overline{\mathrm{A} \Theta \mathrm{B}}$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

The exclusive OR of a bit with itself will always be FALSE. Therefore the XOR of the accumulator with itself will set it to zero.

$$
\text { XOR } \begin{aligned}
& 01111100=7 \mathrm{C} \text { hex } \\
& \frac{01111100}{}=7 \mathrm{C} \text { hex } \\
& 00000000=\text { zero }
\end{aligned}
$$

The corresponding electronic symbols for the hardware implementation of the XOR and XNOR are shown in Figure 2.3.


Figure 2.3. The exclusive or (XOR) and comparator (XNOR) gates.

## LOGICAL NAND AND NOR GATES

By combining an inverter gate in series with the AND and OR gates, a new set of gates is formed. The NOT AND gate is called a NAND gate; it is shown
in Figure 2.4. The NOT OR gate is known as a NOR gate; it is shown in Figure 2.5.


Figure 2.4. The NAND gate can be produced from an AND gate and a NOT gate.



Figure 2.5. The NOR gate can be formed from the OR gate and the NOT gate.
From the truth table, it can be seen that the outputs of the NOR and NAND gates are the inverse of the corresponding OR and AND gates.

| A | B | $\overline{\mathrm{A}+\mathrm{B}}$ | $\overline{\mathrm{A} \cdot \mathrm{B}}$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

If both inputs of the NOR gate are connected together, then the gate behaves like a NOT gate. The same is true for the NAND gate. This can be seen by comparing the first and last rows of the truth tables. In this way, two NOR gates can be combined serially to produce an OR gate. The result is a NOT NOT OR gate that is equivalent to an OR gate. This is shown in Figure 2.6. In a similar way, two NAND gates can be used to make an AND gate as shown in Figure 2.7. Since OR and AND gates cannot be similarly combined to produce the NOR and NAND gates, we will find that NAND and NOR gates are more common.


Figure 2.6. An OR gate is formed from two NOR gates.


Figure 2.7. Two NAND gates are combined to produce an AND gate.

## MAKING OTHER GATES

NOR and NAND gates are very versatile. NOR gates or NAND gates can be combined to produce all of the other gates. This can be seen from the following truth table.

| A | B | $\overline{\mathrm{A}}$ | $\overline{\mathrm{B}}$ | $\mathrm{A}+\mathrm{B}$ | $\mathrm{A} \cdot \mathrm{B}$ | $\overline{\mathrm{A}}+\overline{\mathrm{B}}$ | $\overline{\mathrm{A}} \cdot \overline{\mathrm{B}}$ | $\overline{\mathrm{A}+\mathrm{B}}$ | $\overline{\mathrm{A} \cdot \mathrm{B}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Notice that column 7 of the truth table has the same values as the last column. Similarly, columns 8 and 9 are identical. These relations follow De Morgan's theorem, which can be expressed mathematically as:

$$
\begin{aligned}
& \overline{\mathrm{A}}+\overline{\mathrm{B}}=\overline{\mathrm{A} \cdot \mathrm{~B}} \quad \text { and } \\
& \overline{\mathrm{A}} \cdot \overline{\mathrm{~B}}=\overline{\mathrm{A}+\mathrm{B}}
\end{aligned}
$$

The corresponding digital gates are shown in Figures 2.8 and 2.9.


Figure 2.8. A NAND gate is formed from four NOR gates.


Figure 2.9. A NOR gate is obtained from four NAND gates.
The use of a small circle to represent inverted output brings up another approach to the understanding of digital logic gates. In the more commonly used system, the small circles are used only on the output side of the gate.

Another approach, however, is to always connect active-high outputs to active-high inputs, and active-low outputs to active-low inputs. For this latter system, NAND gates will sometimes appear as OR gates with inverted inputs, and NOR gates will sometimes appear as AND gates with inverted
inputs. According to De Morgan's theorem, the NAND gate is equivalent to the OR gate with inverted input signals. This is demonstrated in Figure 2:10. The circuit shown is logically the same as the one shown in Figure 2.9. Notice that the active-low outputs of the first NAND gates are connected to the active-low inputs of the next OR gate. That is, there are small circles on the outputs of the first gates and on the inputs of the second gate.


Figure 2.10. A NOR gate is produced from four NAND gates. The middle NAND gate is shown in its alternate representation.

## CHAPTER THREE The Stack

When main memory is used to store a collection of data, each member of the data set is individually accessible. This type of storage is termed random access memory (RAM). Magnetic tape storage, by contrast, is serial or sequential access memory. In this latter case, only one item of the set is available at any one time. There are two ways of storing and retrieving the items in a serial memory buffer: one is by means of a first-in, first-out (FIFO) buffer, and the other is by means of a last-in, first-out (LIFO) buffer. We can visualize the serial buffer as a long string of information. With the FIFO buffer, items are added at one end and removed from the other. This buffer is analogous to an escalator: the people who ride the escalator are like the data-those who get on first, get off first.


Figure 3.1. The first-in, first-out (FIFO) buffer.
With the LIFO buffer, on the other hand, the data are added and removed at the same place. This arrangement is analogous to a very long, narrow elevator. Those who get on first, have to wait until everyone else is
off before they can get off. It can be seen that magnetic tape is a FIFO medium.


Figure 3.2. The last-in, first-out (LIFO) buffer.
Sometimes, a special area of main memory is designated as a LIFO buffer even though each member of the buffer is individually accessible. This region is known as a stack. As an example, Hewlett-Packard calculators utilize a very short LIFO stack, consisting of registers known by the letters $\mathrm{Y}, \mathrm{Z}$, and T. An item in any of the registers is individually accessible, yet the stack as a whole can be manipulated. As data is entered from the keyboard, it is placed into the X register. This information can then be transferred to the stack (register Y in this case) by pressing the ENTER key. We say that the contents of the X register are pushed onto the stack. Items can be retrieved from the stack and placed in the $X$ register with the roll-down ( $R$ ) key. We say that data are popped from the stack into the X register by this means. Another stack operation is performed by the EXCHANGE key which is used to swap the contents of the X and Y registers.

## STORING DATA ON THE STACK

We have seen in the previous chapters that the 8080 and Z- 80 microprocessors incorporate general-purpose registers for the storage of information. But these registers are limited in number. Consequently, a special area of main memory is designated for the additional storage of information. This area, called the stack, is implemented on the Z-80 and 8080 as a last-in, first-out serial buffer even though each item in the stack is individually accessible. One of the CPU registers, the stack pointer, references the current location in memory. This is the address of the most recently added item. The stack pointer is decremented as items are added and incremented as items are removed. The programmer may place the stack anywhere in memory by loading the stack pointer with the desired address. For example, the instruction

| LIG | $5 F, 4000 H$ | $(Z-80)$ | or |
| :--- | :--- | :--- | :--- |
| LXI | $5 F, 4000 H$ | $(8080)$ |  |

initializes the stack to location 4000 hex.

Data can be placed on the stack with one of the PUSH operations. A command of
$(Z-80)$

PUSH $\quad$ HL $\quad$| (8080) |
| :--- |
| PUSH |

will move a copy of HL to the stack. Since main memory is addressed eight bits at a time, the PUSH operation is actually performed in two stages. The stack pointer is decremented, then the H register (the high half) is copied to the stack. The stack pointer is decremented a second time and the L register (the low half) is copied to the stack. The stack pointer register now contains the address of the low byte. Figure 3.3 demonstrates the action of a PUSH HL command. The region of memory devoted to the stack is shown with higher memory upward. The arrow represents the stack pointer.


Figure 3.3. The HL register is pushed onto the stack.
The POP instruction reverses the PUSH process. For example, a POP DE command copies 16 bits from the stack into the DE register. Because the stack operates in a LIFO manner, the most recently added byte is removed first. This is placed into register $E$ (the low half of the DE pair). The stack pointer is automatically incremented and the next byte is transferred from memory to register D (the high half). The stack pointer is then incremented a second time. Figure 3.4 demonstrates the operation. Notice that the data originally pushed onto the stack is still present.


Figure 3.4. Two bytes are popped from the stack into DE.

It can be seen that the stack grows downward in memory as data are pushed into it, and it moves back up as data are popped off. For this reason, it is common practice to initialize the stack pointer to the top of usable memory. Actually, the stack pointer can start at one address above the top of memory since the stack pointer is always decremented before use.

If the general-purpose registers contain important information but they are needed for a calculation, it will be necessary to save the original data. This can be easily done by pushing the contents onto the stack. The registers are restored at the end of the calculation with the three corresponding POP commands. The operation goes like this.


Notice that the order of the POP commands is reversed from that of the PUSH sequence. This is necessary because of the stack's LIFO operation.


Figure 3.5. The contents of the general-purpose registers are saved on the stack.


Figure 3.6. The original contents of the general-purpose registers are restored from the stack.

## THE ACCUMULATOR AND PSW AS A DOUBLE REGISTER

The 8 -bit accumulator and the 8 -bit flag register are treated as a 16 -bit double register for the PUSH AF and POP AF instructions. In this case, the accumulator is treated like the high byte since it is pushed onto the stack first. The flag register is pushed onto the stack second. Figure 3.7 demonstrates this.


Figure 3.7. Contents of the accumulator and flag registers are pushed onto the stack.

Data can be moved from one register pair to another by using a PUSH/POP combination. For example, the two 8080 commands

```
PUSH H
FOP I
```

will move $H$ to $D$ and $L$ to $E$. This is not the most efficient way to accomplish the move, however. The sequence requires access to main memory and so is slower than the direct register moves

```
MOU D.H
```

MOU Eil

## Z-80 INDEX REGISTERS

The Z-80 has two, 16-bit index registers that can participate in the PUSH and POP operations. However, the instructions each require two bytes compared to the other PUSH and POP instructions which only require one byte each. As a result, the execution time is slower than the other PUSH and POP instructions. There are no official instructions for moving data between the index registers and the general-purpose registers. This transfer can be performed, however, by use of the PUSH and POP commands. The two instructions

```
FUSH IX
FOF BC
```

will copy the IX register into the BC register.

## SUBROUTINE CALLS

We have seen that the PUSH instructions can be used by the programmer to store data on the stack. The 8080 and Z-80 CPUs use the stack for a second purpose: storing the return address when a subroutine is called. Subroutines are used to efficiently code a set of instructions needed at several different places in a computer program. A subroutine is called by using the assemblylanguage mnemonic CALL. At the end of the subroutine, indicated by the return statement, control is automatically returned to the calling program.


The input and output routines which control the console may be needed at several locations in a program. Consequently, they are coded as
subroutines. The 8080 assembly language subroutine for the console might look like this.

| OUTFUT: IN | STATUS | CHECK STATUS |
| :--- | :--- | :--- |
| ANI | INMSK | INFUT MASK |
| IZ | OUTFUT | NOT READY |
| MOU | AッB | GET MATA |
| OUT | IATA | SENI MATA |
| RET |  | DONE |

Data can be output from anywhere in a program by placing the byte in the $B$ register and calling the output subroutine. The following examples of 8080 assembly language mnemonics show how a question mark and a colon can be printed by calling the console output routine.

```
WHAT& MUI Eg'?' #OUTPUT A ?
    CALL OUTFUT
COLON: MUİ B,': {OUTPUT A COLON
    CALL OUTPUT
```

The above examples utilize the unconditional subroutine call and unconditional return instructions. Conditional call and return instructions are also available. These commands perform the appropriate call or return only if the referenced PSW flag is in the desired state. The four flags--zero, sign, carry, and parity - give rise to eight conditions.

```
zero
not zero
plus
minus
carry
not carry
parity even
parity odd
```

These instructions are discussed in more detail in Appendix H.
The stack provides the mechanism for subroutine operation. When a CALL instruction is encountered, the address immediately following the CALL statement is automatically pushed onto the stack. The subroutine address is then loaded into the program counter register. The program counter tells the CPU which instruction to execute next. Since a subroutine CALL uses the stack, the programmer must be sure that the stack is properly defined prior to a subroutine CALL. When a return instruction is subsequently encountered, the return address is popped off the stack and placed into the program counter. After return from a subroutine, program execution continues with the instruction following the CALL statement.

## PASSING DATA IMPROPERLY TO A SUBROUTINE

Since the stack can be used for storing both data and subroutine return addresses, the programmer must ensure that there are no conflicts. First, there should normally be as many POP instructions as PUSH instructions. Second, one must be careful not to PUSH data onto the stack, CALL a subroutine, then POP data off the stack. The LIFO nature of the stack will cause trouble in this case.


Figure 3.8 shows an example of improper mixing of data and the return address on the stack. Higher memory is upward and lower memory is downward. The arrow indicates the current stack pointer position.


Figure 3.8. Improper mixing of data and the return address on the stack.
In this example, the data is first pushed onto the stack while in the main program. The return address is then pushed onto the stack next, when the CALL instruction is encountered. The POP instruction in the subroutine will actually load the HL register pair with the subroutine return address rather than the data that was expected. This occurs because the data was pushed onto the stack before the return address. Worse yet, the RET instruction will load the program counter with the data, rather than with a useful address. Strange things are likely to happen when the CPU attempts to execute instructions at an address defined by the data.

## PASSING DATA PROPERLY TO A SUBROUTINE

This section demonstrates a proper way to pass data into a subroutine by using the stack. The task can be accomplished with the 8080 XTHL instruction
or the Z-80 EX (SP),HL instruction. This operation exchanges the HL register pair with the two bytes at the current stack position. The instruction is analogous to the X/Y EXCHANGE key on an HP calculator.

The method works in the following way. The data is pushed onto the stack while control is in the calling program. When the subroutine is called, the return address is pushed onto the stack, just after the data. A POP instruction, executed in the subroutine, delivers the return address to the HL register. Now, the XTHL instruction exchanges the HL register with the stack. The desired data is now in HL and the return address is on the stack. Finally, a return instruction will correctly return control to the calling program.


Figure 3.9. Proper mixing of data and return address on the stack.

It is important to note that the XTHL command only works with the HL register. There is no equivalent instruction for the DE or BC registers.

## PASSING DATA BACK FROM A SUBROUTINE

A variation of the XTHL technique is also possible. Data can be pushed onto the stack from within a subroutine, then retrieved after returning to the calling program.

|  | CALL POP | FETCH H | OGET THE DATA |
| :---: | :---: | :---: | :---: |
|  | * * |  |  |
| FETCH: | $\cdots \cdot \stackrel{ }{*} \cdot$ |  |  |
|  | LXI | H: IIATA | PPUT IN HoL |
|  | XTHL |  | ©SWITCH STACK |
|  | PUSH | H | ORET ALILK |
|  | RET |  |  |

DATA in this case is predefined and is part of the LXI instruction.


Figure 3.10. Using the stack to pass data back from a subroutine.

An extension of the XTHL technique allows additional data to be passed on the stack.

|  | CALL | FETCH |  |
| :---: | :---: | :---: | :---: |
|  | POP | B | DDATA 3 |
|  | POP | 1 | finda 2 |
|  | POP | H | - DATA 1 |
|  | - ${ }^{\text {- }}$ |  |  |
| FETCH: |  |  |  |
|  | $\begin{aligned} & \text { LHLD } \\ & \text { XTHL } \end{aligned}$ | datal | - datal to hol SWITCH STACK |
|  | XCHG |  | 引STACK TO DE |
|  | LHLD | dataz | gGet lataz |
|  | PUSH | H | ¢PUT ON STACK |
|  | LHLI | datas | gGET dataj |
|  | PUSH | H | 乡PUT ON STACK |
|  | PUSH | II | ¢RET AIIdR to stack |
|  | RET |  |  |

In this example, the return address is first moved to the HL pair with the XTHL command. Then it is moved to the DE register pair with the XCHG instruction. Three sets of 16 -bit data are obtained from the memory addresses pointed to by the arguments of the LHLD instructions DATA1, DATA2, and DATA3. The first set is placed on the stack with the XTHL command. Then the other two are pushed onto the stack. Next, the return address, previously saved in the DE register pair, is pushed onto the stack. A final RET instruction pops the return address from the stack into the program counter.

## SETTING UP A NEW STACK

Sometimes it is desirable to save the current stack pointer and set up a new one. When this happens, the original stack pointer is restored at the conclusion of the task. The technique is particularly useful when one independent program is executed by another. The original stack pointer is saved in a memory location, then retrieved at the end of the program.

If the current program was reached through a subroutine call, the return address for the calling program should be the current address on the original stack. It is this address that must be saved.

There is a Z-80 instruction that allows the old stack pointer to be stored directly in main memory. The instruction looks like this.

```
* Z-80 UERSION
%
START: LU (OLISTK),SP gsave stack.
    LII SP.STACK bnew stack
    * * *
    LD SP,(OLMSTK) iset old stack
    RET \hat{dorie}
```

At the conclusion of the task, the old stack pointer is restored. With an 8080 CPU, the job is more complicated since the stack pointer cannot be directly saved. In this case, the stack pointer is moved to the HL register pair which is in turn saved in memory. This is done by first zeroing HL, then adding in the stack pointer. At the end of the routine, the old stack pointer is loaded into the HL register pair then copied into the stack pointer register. Finally, a RET instruction is given.

| START: | LXI | HyO | gzero HL |
| :---: | :---: | :---: | :---: |
|  | LIAL | SF | ¢ SP to HL |
|  | SHLII | OLDSTK | psave stack. |
|  | LXI | SF,STACK | onnw stack. |
|  | - . |  |  |
|  | LHLD | OLIOSTK | pset old stack. |
|  | SPHL |  | prestore stack. |
|  | RET |  |  |

## CALLING A SUBROUTINE IN ANOTHER PROGRAM

A program may need to call a subroutine that resides in another program. But if the second program is revised, the subroutine address in the second program will change. This means that the argument of the CALL statement in the first program will also have to be changed.

There are two ways to solve this problem. One method is to provide a jump instruction near the beginning of the second program. The address of the jump instruction will always be the same. However, its argument, the internal subroutine address, can change from one version to the next. The first program simply calls CHEK2, and CHEK2 causes a jump to CHEK, the desired subroutine. The RET instruction at the end of CHEK will effect a proper return to program 1.


Of course, the second program may need to save the incoming stack, then restore it before returning to program 1.

A second solution is to place just the two-byte address of the subroutine near the beginning of the second program.
START: JMP CONTIN ; Frosram 2
CHEK2: HW CHEK

Now the calling program must put its own return address on the stack and get the address of CHEK into the program counter. The following example is a way to do this. Notice that program 1 does not enter program 2 with a CALL instruction. It uses instead the PCHL instruction which copies the contents of HL into the program counter.

|  | FUSH | H | ¢SAVE | Hs L |
| :---: | :---: | :---: | :---: | :---: |
|  | LXI | HyNEXT | ¢ RET | ALDMR |
|  | PUSH | H | \$ONTO | STACK |
|  | LHLII | CHEK2 |  |  |
|  | PCHL |  | \& INTO | PC |
| NEXT: | POP | H | pORIG | $\mathrm{H} / \mathrm{L}$ |

## CALLING ONE SUBROUTINE FROM ANOTHER

A subroutine called by a main program may in turn call another subroutine. When the first subroutine, SUB1, is called, the return address to the main program, MAINA, is pushed onto the stack. When the second subroutine, SUB2, is called, the return address SUB1A is next pushed onto the stack. After the second subroutine has been called, there will be two return addresses on the stack: one to get back to SUB1 from SUB2, and the other to get back to the main program from SUB1.


Figure 3.11. One subroutine calls another.

## BYPASSING A SUBROUTINE ON RETURN

It may be that an operation in the sectond subroutine SUB2 makes it desirable to return directly to the main program from SUB2, bypassing SUB1. This is easily accomplished if the stack pointer is raised by two bytes before executing the return instruction. Of course, care should be taken to see if data has been pushed onto the stack after one or both return addresses were placed on the stack. The one-byte instruction to increment the stack pointer (INX SP) can be executed twice, to raise the stack pointer two bytes. Alternately, a one-byte POP command can be used if there is a free register pair available.


CALL SUB2 POP H RET

Figure 3.12. Skipping one level of subroutine during the return.

Suppose that an ordinary return from subroutine SUB2 back to subroutine SUB1 is desired if the zero flag is set to 1 . On the other hand, an unusual return directly back to the main program is desired if the zero flag is reset to a value of zero. Here is a way to do this.


The POP PSW instruction raises the stack two bytes so that the final RET instruction delivers the return address of MAIN1 to the program counter. This effectively bypasses the intermediate subroutine.

## A PUSH WITHOUT A POP

Near the beginning of the system monitor, explained in Chapter 6, there is a restart address called WARM. The program normally branches back to this point at the conclusion of each task. Thus the final instruction of each task could be:

## JMP WARM

A more efficient method, however, is to push this restart address WARM onto the stack at the beginning of the task. Then if the task does not terminate within a subroutine, a simple return instruction, rather than a jump, can be given at the end of the task. This causes a branch back to WARM.


This example is an exception to the rule that we should have a POP instruction for every PUSH. Here, there is a PUSH but no POP. Of course there is also a RET with no CALL. So everything is all right-or is it? What happens if termination occurs from a subroutine?

## GETTING BACK FROM A SUBROUTINE

If a particular task terminates in a subroutine, then this subroutine's return address must be popped off the stack (or an INX SP instruction must be executed twice) before the return is issued.


The stack pointer grows downward through memory during use. It is therefore common practice to place the stack as high as possible in available memory. But the system monitor may be located at the actual top of memory. In this case the stack can initially be placed lower in memory at the beginning of the monitor.

START:
LXI SF,START

On the other hand, the monitor may be placed in read-only memory (ROM). In this case, the stack can be located at the actual top of read/write memory. (While both read/write memory and ROM are random-access memoryRAM, it is customary to refer to read/write memory as RAM and read-only memory as ROM. This convention will be followed here.)

## AUTOMATIC STACK PLACEMENT

The placement of the stack at the top of RAM can be done automatically, so that the total amount of RAM can be changed without having to reprogram the PROM monitor. A short routine can test each block of memory starting at zero until it finds a location that can't be changed. The stack is then put at the beginning of this block. Remember, the stack pointer is always decremented before use; therefore, it can be initially defined as one location above usable memory.

The first part of the program is a memory search routine that starts at address zero. It moves the byte from that location into the accumulator, complements it, then moves the complemented byte back to the original location. A comparison is made to see if the memory location does indeed contain the complemented byte. If it does, the accumulator is complemented back to the original byte and returned to memory. Such an algorithm is often called a nondestructive memory test.

The first byte of each subsequent block of memory is checked in this way until a failure is found. This will usually reflect the top of usable memory, but of course, it could indicate defective memory. The following program will work properly if placed in read-only memory.

```
\hat{0}
& ROUTine to automatically flace the
; STACK AT THE TOP OF MEMORY
; 8080 CODE
%
NEXTP: LXI MOU H,O AFIRST ANIN
    CMA ¢COMFLEMENT
    MOU M&A #PUT IT BACK
    CMF M ;COMPARE?
    JNZ TOP $NO, DONE
    CMA #BACK TO ORIG
    MOU M&A gFUT IT BACK
    INR H {NEXT BLOCK
    JMP NEXTP #KEEP GOING
\hat{}
TOP: SPHL #SET STACK
    CALL OUTHL 引PRINT IT
```

This program might not work, however, if it is placed in read/write memory. The problem occurs because the routine is changing various locations in memory. If it happens to change its own instructions, then the results will be unpredictable.

The shortcomings of the previous program are solved with the following version. The improved version will operate properly no matter where it is placed. The stack will be placed at the top of contiguous RAM unless the routine itself is in that part of memory. In that case, the stack will be placed at the beginning of the program. The Z-80 version is shown, but the program can be run on an 8080 if two minor changes are made. The relative jump instruction must be changed to an absolute jump and the DJNZ instruction must be changed to the equivalent DCR B and JNZ combination.


The new version works in the following way. The B register initially contains the block number of the routine itself. The value in $B$ is decremented as each successive block is checked. If the routine is in ROM, then the end of usable memory will be found, as in the previous version. The program will loop between the label NEXTP and the DJNZ NEXTP instruction. At some point, the CP (HL) instruction will reset the zero flag and the computer will jump to the address of TOP. The stack will then be placed at the top of RAM.

Alternately, if this routine is placed in the lower memory area, then the DJNZ instruction will decrement the B register all the way to zero. The zero flag will be set and the program will move on to TOP. Now the stack will be set to the beginning of the memory block that contains the program itself.

The START SHR 8 expression at the beginning of the routine instructs the assembler to calculate the high byte of the address of START and make it the second operand of the LD B instruction. It does this by shifting the
address of START by eight bits to the right, then taking the low-order eight bits of the result. Some assemblers allow an equivalent operand of

## HIGH START

which is easier to comprehend. This automatic stack routine is incorporated into the system monitor explained in Chapter 6.

## CHAPTER FOUR

## Input and Output

Computers would not be very useful if they could not interact with the outside world. Commands and data are sent to the computer from the keyboard, magnetic tape, disk, and other peripherals. Results of computations are sent back from the computer to the printer, video terminal, tape unit, disk, and so on. Such input and output (I/O) transfers on a microcomputer are typically accomplished through special memory locations called I/O ports. One type of port is distinctly different from main memory. The other type of arrangement utilizes one of the regular main memory locations. The peripheral in this latter case is then said to use memory-mapped I/O. Each method has advantages and disadvantages. In either case, the I/O port will transfer eight bits, the natural word size for the 8080 and Z-80 CPUs.

## MEMORY-MAPPED I/O

The I/O instructions on the 8080 microprocessor are rather limited compared to memory operations. There is a single IN and a single OUT instruction for transferring eight bits of data. In contrast, there is a much larger collection of memory operations available.

| (8080 Mn | (ics) | (2-80 | mnemonics) |
| :---: | :---: | :---: | :---: |
| STA | 80 | LD | (80):A |
| LDA | 81 | LD | A, (81) |
| mov | Mg C | LD | (HL) , C |
| Stax | D | LID | (DE), $A$ |
| SHLII | 84 | L. | (84) 9 HL |

These additional instructions can be utilized with memory-mapped I/O, greatly increasing the versatility of the Z-80 and 8080 I/O operations.

The STA instruction stores the 8 -bit accumulator value at the memory address specified by the operand. If this address corresponds to a memorymapped port, then the byte is sent to the peripheral. The LDA command reverses the operation. It can be used to input a byte from a port. The MOV M,C instruction can be used to transfer a byte from the C register to the memory location designated by the HL register pair. The STAX D command moves a byte from the accumulator to the memory location designated by the DE register pair. The SHLD instruction opens a new dimension. Since this operation transfers 16 bits of data from the HL register pair directly into two consecutive memory locations, two adjacent ports can be simultaneously serviced.

The typical video console is a serial device that uses distinct ports. However, memory-mapped controller boards are commerically available. In this case, an ordinary TV set is then used for the video screen. There are also disk-controller boards that use memory-mapped operations to communicate with the disk drives. It is interesting to note that the Motorola 6600 CPU performs all of its I/O by memory mapping. There are no separate input or output instructions for this CPU.

## DISTINCT DATA PORTS

Data ports may be designed to operate either in parallel or in serial fashion. Both the parallel and the serial I/O ports are connected to the computer through the system bus by a set of eight data lines. In addition, the parallel port is connected to the peripheral by another set of eight data lines. The serial port, by contrast, has only two data lines connecting it to the peripheral.

For some peripherals, such as a printer, data is transferred in only one direction. For others, such as the console and magnetic tape units, the peripheral is able to both send and receive data. In this latter case, there will be 16 data lines between the computer and the peripheral if a parallel port is used. Eight lines are used for sending data and eight are used for receiving data. The serial port, in contrast, will have three signal lines to the peripheral if there is two-way communication. One is for transmitting, one is for receiving, and the third is a common line for the other two.

There may be additional lines between the computer and the peripheral. One of these might indicate to the computer whether the terminal is operational. Another can be used to inform the terminal that the computer is ready. These extra lines are sometimes referred to as handshake lines.

The computer usually operates at a much higher speed than the peripherals. Consequently, there must be a mechanism for effectively slowing down the computer during I/O operations. For serial or parallel ports, this is typically accomplished by using two separate I/O ports for each peripheral device. One port is used for the data port and the other is used for the status port. Each of these two ports will have distinct addresses, one of the 256 values available to the 8080 or Z-80 CPU for this purpose. There are three
general methods of performing I/O through data ports: looping, polling, and interrupting.

## LOOPING

Looping is the simplest method of performing I/O through separate ports, and it is the one that is most commonly employed in 8080 and Z-80 programs. The CPU performs output by sending a byte to the data port using the OUT instruction. The corresponding status port is then read with an IN instruction. One bit of the 8 -bit status port reflects the condition of the corresponding peripheral.

When the CPU places a byte in the data register, using the OUT command, the output status bit of the status register is set. This may actually result in a logical 1 or a logical zero, depending on the port design. When the peripheral utilizes the byte that was placed into the data register, the output status bit of the status register is reset. These changes in the status bit are automatically handled by the I/O interface hardware. However, the programmer must include in the software the appropriate routines for monitoring the status bits.

As an example of the looping method, consider the following subroutine:

| COUT: | IN | 10 H | ¢ CHECK STATUS |
| :---: | :---: | :---: | :---: |
|  | ANI | 2 | ¢ SELECT BIT |
|  | JZ | COUT | ONOT READY |
|  | MOV | A, C | gGET EYTE |
|  | OUT | 11H | -SEND |
|  | RET |  | 9 DONE |

This routine could be used to send a byte of data to the system console. The first instruction of the listing causes the CPU to read the 8 -bit status port which has the address of 10 hex. The second instruction performs a masking AND operation to select the write-ready bit, bit 1. Remember that a logical AND with zero and anything else gives a result of zero. However, a logical AND with unity and a second logical value, gives the result of that second value.

Suppose that the output status is indicated by a logical 1 of bit 1, where bit 0 is the least-significant bit of the register. Then, a logical AND with the value in the status register and with the number 2 will result in a logical 1 if the peripheral is ready. If the device is not ready, however, the result is a logical 0.

AND | 01010111 | status | 01010101 |
| :---: | :---: | :---: |
| 00000010 | $=2$ | 00000010 |
| 00000000 |  | 00000010 |
| reads |  |  |

Thus, the logical AND with the value of 2 in the status register gives a result of zero if bit 1 (the second bit) is 0 . Otherwise, a nonzero result is obtained.

The third instruction in the looping example is a conditional jump. If the peripheral is not ready, the JZ instruction will cause the computer to loop repeatedly through the first three lines until the peripheral is ready for another byte. At this point, the write-ready bit, bit 1, will be a logical 1. Then the logical AND operation, the second instruction of the subroutine, produces the nonzero value of 2 . The MOV instruction following the conditional jump will then be executed. The byte to be outputted is moved to the accumulator, and then sent to data port 11 hex by use of the OUT command.

When the byte to be output is actually sent to the data port, the writeready flag is reset to a logical zero. The output routine may be immediately reentered for outputting another byte, but now the peripheral is not ready. Looping will occur again through the first three instructions of the output routine since the write-ready flag has been reset to zero.

The CPU clock may be operating at 2 or 4 MHz . This rate is thousands of times faster than the speed of a typical printer. Consequently, if the looping method is used, the CPU will be spending over 99 percent of its time simply looping through the first three lines of the output subroutine. The computer will be spinning its wheels, so to speak, waiting on the peripheral.

Because the CPU is operating so much faster than the peripherals, it can, in principle, service many peripherals simultaneously. A very simple but useful implementation of this idea is found on the $\mathrm{CP} / \mathrm{M}^{*}$ operating system. In the $\mathrm{CP} / \mathrm{M}$ system,* console output is normally sent only to the console. This terminal is typically a high-speed video device. But if the user types a Control-P, then the list device is also turned on. Console output will now appear simultaneously at both the console and the line printer.

This technique can be easily observed if the console video accepts data much faster than the line printer. Normally, as data is sent only to the console, it appears rapidly on the video screen. But when the list device is turned on, the output appears much more slowly. The reason for the slowdown is that both peripherals are operating at the speed of the slower one, in this case the printer.

A subroutine for accomplishing such a dual output might look like this.

| LOUT: | IN | LSTAT | ЯLIST STATUS |
| :---: | :---: | :---: | :---: |
|  | ANI | 2 | وOUTPUT MASK |
|  | $J Z$ | LOUT | floop UNTIL READY |
|  | MOU | Ag C | fGET THE BYTE |
|  | OUT | lnata | وSENI TO LIST |
|  | OUT | cinata | \%ANLI CONSOLE |
|  | RET |  | $\triangle$ ITONE |

[^0]This routine is not the one that is actually used in the CP/M system since, with our routine, the console will always display everything that is sent to the printer. This feature does not increase printing time as long as the console operates faster than the printer. Notice that there is no need to check the console status register. The output rate is set at the speed of the printer, and so the console, which operates so much faster, will always be ready if the printer is ready.

## POLLING

One way to improve the performance, or throughput, of a CPU is with a technique known as polling. In this method, the CPU sends a byte to each of several different peripherals. Each peripheral operates at its full speed. Polling is more efficient than the looping method, and has been incorporated into several commercial 8080 software products. One product is a multiuser BASIC which can service up to four separate consoles. Each user can independently perform calculations using the same BASIC interpreter.

Another product that uses the polling technique is known as a spooler. The looping method is typically utilized for all output. In this case, all other activities must be halted while the printer is working. With a spooler program, however, things are different. When this program is incorporated into the system, the user can perform other tasks using the system console while a disk file is being printed.

In the polling method, the I/O routines are somewhat different from the corresponding routines of the looping method. The output-ready flag of the status register is checked periodically as with the looping method. But if the status flag indicates that the device is not ready, the CPU returns to perform some other task. Thus, the CPU does not waste time looping around the first three instructions of the input or output routine. A typical output routine using the polling method might look like tihis.


While the polling method is a great improvement over the looping method, there are still problems. For example, a decision must be made as to how often each status register will be polled. An even better method is to use hardware interrupts.

## HARDWARE INTERRUPTS

The 8080 and Z-80 microprocessors incorporate a hardware interrupt system. This feature allows an external device, such as the system console or printer,
to interrupt the current task of the processor. When the CPU is interrupted, it suspends its current task, and calls on one of several memory locations set aside for this purpose. The CPU services the request of the interrupting peripheral, then it returns to its previous task.

In this method, the CPU does not have to be programmed to check the peripherals on a regular basis as with the method of polling; nor does it have to waste time in a loop. Instead, the peripheral interrupts the processor when it needs service. If several peripherals are able to interrupt the CPU, then there must be a method for prioritizing the requests. This ordering is accomplished through a vectored interrupt system. For example, if a lower-priority device has interrupted the CPU for service, this phase can also be interrupted by a peripheral with a higher priority. On the other hand, a device with a lower priority cannot interrupt a higher-priority service, but must wait its turn.

Usually, the highest-priority interrupt will be assigned to updating the system clock. If the computer misses a beat, then the time will be incorrect. The next lower priority could be assigned to disk transfer. The printer could have a low priority since it is a relatively slow device, and it won't matter if it must slow down every so often.

Suppose that the printer is operated by interrupts rather than by looping or polling. The computer sends a byte to the printer, then continues with another task. When the current byte has actually been printed, the printer interrupts the CPU for another byte. In the time between the printing of two bytes, the CPU can perform many other tasks.

The console keyboard is another peripheral that can be readily serviced by an interrupt system. In this case, each time the user presses a key, the CPU is interrupted from its current task. Of course, if the CPU is currently servicing a higher-priority interrupt, then the console keyboard request will have to wait.

Both the 8080 and the Z-80 allocate eight addresses that can be used for the interrupt service routines. These addresses can be called by the eight, one-byte RST instructions.

| Z-80 | 8080 | Instruction code |  | Call |
| :---: | :---: | :---: | :---: | :---: |
| mnemonic | mnemonic | hex | binary | address |
| RST 00H | RST 0 | C7 | 11000111 | 00 H |
| RST 08H | RST 1 | CF | 11001111 | 08H |
| RST 10 H | RST 2 | D7 | 11010111 | 10H |
| RST 18H | RST 3 | DF | 11011111 | 18H |
| RST 20 H | RST 4 | E7 | 11100111 | 20 H |
| RST 28H | RST 5 | EF | 11101111 | 28 H |
| RST 30H | RST 6 | F7 | 11110111 | 30 H |
| RST 38H | RST 7 | FF | 11111111 | 38 H |

These instructions can be used as one-byte subroutine calls. As an example, suppose that the CPU executes an RST 5 instruction which corresponds to the instruction code EF hex. A subroutine call is then made to the corresponding address of 28 hex. The return address is pushed onto the stack,
just as for a regular subroutine call. Subsequent execution of a return instruction will cause the program flow to return to the instruction immediately following the RST 5 instruction.

Hardware interrupts operate by emulating the software RST call. When an interrupt occurs, the CPU automatically disables the interrupt flip-flop, thus further interrupts are prevented. Then a subroutine call is made to the corresponding call address. This is done by jamming the desired RST code onto the data bus. The simplest implementation is to use a single interrupting device and the RST 7 instruction. (A normal interrupt always performs an RST 7.) The interrupting peripheral momentarily changes the state of the interrupt-request bus line. For the $\mathrm{S}-100$ bus, this would require that bus line 73 be pulled to a zero-voltage state from the usual 5 -volt level. The CPU responds by automatically calling memory address 38 hex. The programmer will have previously placed the service routine at this location. The service routine will conclude with a command to re-enable the interrupt flip-flop. Then a return instruction will be executed.

The trouble with this simple approach is that the RST 7 call to location 38 hex interferes with system debuggers because they also use this address. Consequently, another interrupt level is more suitable. Unfortunately, a single interrupt system always calls the RST 7 location. One solution to this problem is to use a vectored interrupt board. A vectored interrupt board allows the user to select up to eight separate interrupt levels corresponding to the RST 0 to 7 instructions. The disadvantage of this approach is the cost, since a vectored interrupt board may sell for several hundred dollars.

However, there is a low-cost solution. If only one interrupt level is required, a single hardware interrupt can be converted from an RST 7 to some other level such as an RST 5 by using only two logic gates. The circuit shown in Figure 4.1 will make the needed translation. The output of the two-input NAND gate IC-1 goes low when both of the input lines are high. One of these inputs is SINTA, line 96 on the S-100 bus. It is a CPU status signal that indicates acknowledgment of the interrupt request. The other input is PDBIN, bus line 78. This signal indicates that the data bus is in the input mode.


Figure 4.1. Circuit to convert an 8080 interrupt to an RST 5.
When the output of IC-1 goes low, it turns on the three-state buffer IC-2. This pulls the data-input bus line DI4 low. Since the remaining seven lines of the data-in bus are high, the CPU will see the value of

Notice that this is the bit pattern for the RST 5 instruction. The result is that the CPU executes an RST 5 instruction, by calling address 28 hex. The interrupt service routine, or a jump to it, is placed at this address.

## AN INTERRUPT-DRIVEN KEYBOARD

We have seen that a printer operates considerably slower than a CPU. The console keyboard is even slower than the printer, especially if the operator is not an expert typist. Conversion to an interrupt-driven keyboard will considerably increase the effectiveness of a computer.

Characters entered on an interrupt-driven keyboard are temporarily stored in a memory buffer area. Each time a key is pressed on the console, the CPU is interrupted from its current task. The new byte is read and placed into the keyboard buffer. The computer then returns to its prior task. When the computer needs console input, it gets it from the input buffer, rather than from the console itself.

An interface program, utilizing a keyboard-interrupt approach, is shown in Listing 4.1. This program provides the necessary routines for interfacing the Lifeboart version of CP/M to a North Star disk system.* The portions of the program which specifically utilize the interrupt routines begin with a row of asterisks and end with a row of semicolons.

| Computer <br> pointer <br> F400 | Computer <br> count <br> F402 | Keyboard <br> count <br> F403 | Keyboard <br> pointer <br> F404 | Buffer <br> F406 |
| :---: | :---: | :---: | :---: | :---: |

Figure 4.2. The input buffer and pointers.
The layout of the memory buffer with its pointers is shown in Figure 4.2. The buffer area is arbitrarily chosen to start at the address of F400 hex. The location can be anywhere above the CP/M operating system. There is only one keyboard buffer, but there are two sets of pointers: one for the CPU and one for the keyboard. Two counters are also utilized; one shows how many characters have been entered from the keyboard and the other shows how many have been read by the computer. Since both sets of pointers grow larger, they need to be reset periodically. The two pointers are compared after each carriage return. If they are the same, then they are both reset to the beginning of the buffer.

Suppose that this interface program is incorporated into your system. $\mathrm{CP} / \mathrm{M}$ might be printing something on the console video screen when a key on the console is pressed. A hardware interrupt will occur, causing the computer to stop its task and call address 28 hex (RST 5). A jump instruction at address 28 hex will transfer control to subroutine KEYBD. The keyboard

[^1]Listins 4.1. Interrupt driven keyboard.

|  | TITLE 'Interrupt CF/M BIOS' |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |
|  | \% (Fiut todas's date here) |  |  |  |
|  | ; LIFEBOAT UERSION WITH OFTION FOR |  |  |  |
|  | \% EITHER SINGLE OR ROURLE RENSITY |  |  |  |
|  |  |  |  |  |
|  | \% TERMINAL MEUICES SUFFORTEI: |  |  |  |
|  | \% |  |  |  |
|  | ¢ CONSO | OLE | 10 HEX | CON: |
|  | - LIST. |  | 12 HEX | LST: |
|  | - FHONE | MOLEM | 14 HEX | FUN: |
|  | ; |  |  |  |
| $0000=$ | FALSE | ERU | 0 |  |
| FFFF = | TRUE | EQU | NOT FAL. | SE |
|  | ) ${ }^{\text {t }}$ ( |  |  |  |
| FFFF = | HOUBLE | EQU | TRUE | ¢ IOURLE IENSITY |
| FFFF $=$ | ${ }_{\text {i }}{ }^{\text {MTRM }}$ | EQU | TRUE | GINTEFF UEFSION |
|  |  |  |  |  |
|  |  | IF | nourle |  |
| $0036=$ | MSIZE | EQU | 54 | © IECIMAL K゙ |
| $11600=$ | BIOS | EQU | MSIZE*1 | 1024-200H |
| 1800 $=$ | USEF: | ERU | BIOS+50 | OOH |
| $4900=$ | OFFSET | ERU | $1 \mathrm{FOOH}-\mathrm{EIOS}$ |  |
|  |  | ELSE | ¢SINGLE DENSITY |  |
|  | MSIZE | EQU | 56 |  |
|  | USER | ERU MSIZE*1024-700H | MSIZE*1024-700H |  |
|  |  |  |  |  |
| $0003=$ | IOEYTE | EQU | 3 | \$ I/0 SETUF' |
| $0000=$ | CR | EQU | OLH | OCARRIAGE RET |
| 000A $=$ | LF | EQU | OAH | OLINEFEED |
| OOOC $=$ | FFEED | EQU | 12 | ¢FORMFEEI |
| $0003=$ | CTRC | EQU | 3 |  |
| $0004=$ | CTRA | EQU | 4 | ¢mp. EMF'TY BUFFER |
| $0011=$ | CTRQ | EQU | 17 | \% ${ }^{\text {OR, SG, SCROLL }}$ |
| $0013=$ | $\begin{aligned} & \text { CTRS } \\ & \hline \end{aligned}$ | EQU | 19 | \% ${ }^{\text {g }}$, FREEZE SCROLL |
|  |  | IF | nOURLE |  |
|  | ¢ F'ATCH | Late |  |  |
| [5B1 | ORG | 8IOS-100H+OR1H |  |  |
|  |  | ELSE |  |  |
|  | ORG | USER-60OH O AFH |  |  |
|  |  | ENIIF |  |  |
| 15S12E4465 |  | LB | '。Jan 2 | $28.80{ }^{\circ}$ \%PATCH IUATE |
|  | $\hat{\text { ¢ }}$ |  |  |  |
| IIBOO | ORG | USER |  |  |
| $0010=$ | CSTAT | EQU | 1 OH | ¢CONSOLE STATUS |
| $0011=$ | CIIATA | EQU | CSTAT+1 | 1 CONSOLE MATA |
| $0001=$ | CIMSK | EQU | 1 | ¢INFUT MASK |
| $0002=$ | COMSK | EQU | 2 | gOUTFUT MASK |
| $0012=$ | LSTAT | EQU | 12 H | ilist status |
| $0013=$ | LIIATA | EQU | LSTAT+1 | 1 ilIST InATA |
| $0001=$ | LIMSK | EQU | 1 | ¡INFUT MASK |
| $0002=$ | LOMSK | EQU | 2 | \#OUTFUT MASK |
| $0000=$ | LNULL | EQU | 0 | iLIST NULLS |






| LIBFE | Cu9EIB |  | CALL | RSETF' |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LICO1 | उEOK | CINS: | MUI | A, CR | ORESTOFE CR |
| nco3 | E1 | CINA: | FOF | H |  |
| nco4 | FE |  | EI |  | 9FEALIY FOR MOFE |
| acos | C9 |  | FET |  |  |
|  |  |  ELSE |  |  |  gNO INTEFFUFTS |
|  |  |  |  |  |  |  |
|  |  | $\hat{\text { p }}$ |  |  |  |
|  |  | CINS: | IN | CSTAT | \%CHECK STATUS |
|  |  |  | ANI | CIMSK |  |
|  |  |  | $J Z$ | CIN2 |  |
|  |  |  | IN | cmata |  |
|  |  |  | ANI | 7FH | GMASK FARITY |
|  |  |  | FET |  |  |
|  |  |  | ENTIF |  | 9 INTRM |
|  |  | ¢ |  |  |  |
|  |  | ; CONSOLE INFUT ค, |  | FFiOM LIST |  |
| nicob | 1812 | LIN: | IN | LSTAT |  |
| nCo8 | E601 |  | ANI | LIMSK |  |
| IICOA | CAOGINC |  | JZ | LTN |  |
| HICOL | DE13 |  | IN | LIIATA |  |
| IICOF | E67F |  | ANI | 7FH |  |
| UC11 | C9 |  | RET |  |  |
|  |  | \% |  |  |  |
|  |  | ; CONSOLE OUTFUT |  |  |  |
| UC12 | 3 AO 300 | CONOUT: | LDA | IOEYTE | ¢ WHERE? |
| 4 Cl 15 | E603 |  | ANI | 3 |  |
| LC17 | 187 |  | ORA | A |  |
| LIC18 | E22EMC |  | JFO | LIST |  |
|  |  | ¢ |  |  |  |
| LCIE | W810 | CONW: | IN | CSTAT | \% CHECK STATUS |
| DCiII | E602 |  | ANI | COMSK゙ |  |
| LC $1 F$ | CA1BLIC |  | $J Z$ | CONW |  |
| Luce2 | 79 |  | MOV | As C | gGET BYTE |
| LIC23 | 11311 |  | OUT | chata | ASENI IT |
| LIC25 | C9 |  | FET |  |  |
|  |  | \% |  |  |  |
|  |  | $\hat{\hat{p}}$ ¢ LIST OUTFUT |  |  |  |
| LIC26 | 3 AO 300 | LOUT: | LIIA | IOBYTE |  |
| IIC29 | E640 |  | ANI | 40 H | $\hat{y}$ BIT 6 |
| nces | C21BDC |  | JNZ | CONW | ¢CONSOLE OUT |
|  |  | ; |  |  |  |
| HC2E | 1 BL 12 | LIST: | IN | LSTAT | ¢CHECK STATUS |
| DC30 | E602 |  | ANI | L.OMSK |  |
| IIC32 | CASELIC |  | $J Z$ | LIST |  |
| DC35 | 79 |  | MOV | $A, C$ | \% GET BYTE |
| L1C36 | 11313 |  | OUT | LIATA | ¢SENIIT |
|  |  | ¢ |  |  |  |
|  |  |  | IF | LNULL $>0$ |  |
|  |  | ¢ |  |  |  |
|  |  | $\hat{\dagger}$ NULLS | FOF LIST | LIEVICE |  |
|  |  | $\hat{9}$ |  |  |  |



| nc74 | DE14 | MIN: | IN | MSTAT | ¢CHECK STATUS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| nc76 | E640 |  | ANI | MIMSK |  |
| DC78 | CA74IIC |  | JZ | MIN |  |
| nC7E | DE15 |  | IN | MLATA | 9GET EYTE |
| nc7a | E67F |  | ANI | TFH | GMASK FARITY |
| LCOF | C9 |  | RET |  |  |
|  |  | ¢ |  |  |  |
| [1080 | 31322 n |  | DE | ' 1-28-80' | ' ¢VERSION |
|  |  | \% |  |  |  |
| nC88 |  |  | ENA |  |  |

ssmbol table

| 00C5 | ACONT | OOC. 4 | aliata | 00 C 7 | BCONT | OOC6 | BDATA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1600 | BIOS | F400 | EUFFER | F406 | EUFF | F 402 | CCNT |
| 0011 | cmata | 0001 | CIMSK | LIELC | CIN3 | $\mathrm{ruco3}$ | CIN4 |
| LuCO1 | CINS | 0002 | Com 5 K | Lentis | CONIN | ncis | CONOUT |
| LIEAE | CONST | LIC1E | CONW | F400 | CFNTR: | OOON | CR |
| 0010 | cstat | 0003 | CTEC | 0004 | CTFEI | 0011 | CTFQ |
| 0013 | CTES | FFFF | IIOUBLE | 0000 | FALSE | OOOC | FFEEI |
| nc38 | FOFM | W815 | INIT | FFFF | INTFIM | 0003 | TOEYTE |
| F403 | KCNT | 10892 | KEY2 | LuE7F | KEEY | 1186C | KEY4 |
| 1891 | KEY5 | 14895 | KEYG | LB5E | NEYEII | F404 | KFNTR |
| 0013 | linata | 0005 | LEV | OOOA | LF | 0001 | LIMSK |
| IICO6 | LIN | LECE | LISST | HC2E | LIST | 0000 | LNULL |
| 0002 | LOMSK゙ | IUC26 | LOUT | nc3F | LSK゙IF' | 0012 | lstat |
| 0015 | minata | 0040 | MIMSK | ICC74 | MIN | InCSE | moncr |
| 0080 | MOMSK | WC69 | MOUT | 0036 | MSIZE | 0014 | MSTAT |
| 4900 | OFFSET | LIC48 | FUNCH | HECs | QUIT | DB9E | RSETF |
| UEOO | STAFT | 0095 | Stof' | FFFF | TRUE | 10800 | USER |

entry is read with an IN instruction. The byte is then placed into the keyboard buffer and the buffer pointer and buffer count are both incremented. The interrupt flip-flop is enabled with an EI instruction, then the computer returns to its previous task.

When the CPU needs another byte, it gets it from the keyboard buffer in memory, rather than from the keyboard itself. The instructions starting at subroutine CONIN perform this step. The separate buffer pointer and buffer count, maintained for the CPU, are both incremented.

The interrupt-driven keyboard can be utilized with most of the CP/M systems programs. For example, if a BASIC interpreter has been loaded and a source program has been entered, then the source program can first be listed, then executed by typing the following two lines.

```
LIST
RUN
```

The second command can be given immediately following the first, even though the first task has not been completed. The second command will not be displayed on the console, however, until the completion of the first task. Therefore, the operator must type carefully.

## SCROLL CONTROL AND TASK ABORTION

Data can appear (scroll) too rapidly on a high-speed video screen. With the usual CP/M arrangement, the user can type a Control-S to freeze the video display. Typing any other character will cause scrolling to resume. The interrupt-driven routine given in Listing 4.1 incorporates its own scroll control. Typing a Control-S freezes the screen, just as with the usual CP/M setup. However, scrolling can only be resumed by typing a Control-Q. The two commands, Control-S and Control-Q, are treated distinctly; they are not placed into the input buffer, but are acted upon immediately.
$\mathrm{CP} / \mathrm{M}$ tasks are normally aborted by typing any keyboard character. On the other hand, a Control-C is required in Microsoft BASIC, and a Control-E is used by Xitan BASIC for aborting the current task. This protocol has been altered so that characters can be entered into the keyboard buffer during a scroll operation. Nevertheless, it may be desirable to abort a task.

If no characters have been typed ahead, that is, if the computer is executing the latest command, then a Control-C command will abort the current operation. Alternatively, if there are characters waiting in the consoleinput buffer, then these must be flushed out by typing a Control-D. At this point, a Control-C can be typed to abort the task. This arrangement will work with most programs, including Microsoft BASIC and Tarbell BASIC. If you use Xitan BASIC, then you must change the abort command character in the interface routine from a Control-C to a Control-E.

An additional alteration is necessary for the Word-Master text editor. First of all, Word-Master buffers the keyboard buffer using software routines. Consequently, a hardware-interrupt system is unnecessary. Secondly, WordMaster uses Control-C and Control-D for system commands. Control-C is used to display the next screen and Control-D is used to move the cursor to the next word. If you want to use hardware interrupts with Word-Master, you must change the Control-C and Control-D commands in either the interface routine or in Word-Master.

## DATA TRANSMISSION BY TELEPHONE

The process of transmitting information between a peripheral and the computer may be simple or it may be complex. If the system console is wired into the computer, or if the computer itself is built into the console, then the integrity of the transmitted data is not likely to be much of a problem. It may be, however, that the console is connected to the computer through a telephone line. The computer may be located across town or across the country. In any case, connection through a telephone line complicates things.

In a typical telephone arrangement, the data is sent from the console by modulating an acoustical carrier for transmission over the telephone line. The conversion is performed by an electronic device called a modem (the name is an abbreviation for MODulator-DEModulator). Two modems are required, one at each end of the telephone line. One converts the transmitted
signal to telephone frequencies, the other converts the signal back to the original data.

The modem may also have an acoustical coupler. This allows a standard telephone headset to be pressed into two rubber-lined openings in the modem, making a direct connection between the modem and the telephone line unnecessary.

There will usually be two data carrier signals at different frequencies. This allows simultaneous two-way, or full duplex, operation. The computer can transmit data to the console on one carrier while the console is transmitting data to the computer on the other carrier.

A microcomputer can produce a more effective link between a console and a large main-frame computer, especially if a relatively slow modem is utilized. A program can be developed using the microcomputer's editor, then the resulting file can be automatically transmitted to the larger computer. A subroutine that can be used to link a microcomputer to a large computer is given in Listing 4.2. This routine can be readily incorporated into the system monitor introduced in Chapter 6.



## PARITY CHECKING

Parity checking provides a method of monitoring the integrity of data transmission. While there are several different schemes for digitally encoding the common characters, the ASCII method is frequently used for microcomputers. The ASCII code, shown in Appendix A, requires only seven bits for each character. Since each byte of data contains eight bits, there is one bit available for use as a check bit.

Consider the 7-bit pattern for the ASCII characters 2 and 3.
ASCII 20110010
ASCII 30110011
The value of 2 is encoded with four logical zero bits and three logical 1 bits. The value of 3 is encoded with three logical zero bits and four logical 1 bits. A parity check can be obtained by including an additional bit on the left (high-order) end.

There are two common methods of generating the parity bit. One encoding method is called even parity. In this case, a leading zero bit is added if there are an even number of logical ones among the other seven bits. On the other hand, the parity bit would be a logical 1 if there are an odd number of logical ones among the other seven bits. With even parity coding, the ASCII characters 2 and 3 would look like this.
$2 \quad 10110010$
300110011
Now the 8 -bit representation of both the 2 and the 3 contains an even number of logical ones (and an even number of logical zeros).

An alternate approach is called odd parity. In this case, the operation is simply the inverse of even parity. The logic of the parity bit is chosen so that the resulting bit pattern contains an odd number of logical ones. Either even or odd parity encoding will provide a check on the integrity of the data transmission.

Suppose that during transmission of the character 2 , the rightmost bit became inverted. The console sent the even-parity bit pattern

10110010
but the computer received the bit pattern
10110011

A parity check, performed at the computer, would be able to detect the fact that there was an error.

A typical console-input routine might look like this.

| CONIN: | IN | CMASK | ¢ CHECK STATUS |
| :---: | :---: | :---: | :---: |
|  | ANI | CIMSK | ©MASK FOF INFUT |
|  | JZ | CONIN | ¢LOOF UNTIL READY |
|  | IN | cdata | $\hat{\text { GET THE DATA }}$ |
|  | ANI | 7FH | © REMOUE FARITY |
|  | RET |  |  |

The next to the last instruction in this subroutine performs a logical AND with 7 F hex. This step is used to remove the high-order bit of the byte since it is not needed for ASCII data. Instead of ignoring this eighth bit, we could use it as a parity check. An input routine to perform a check for parity looks like the following list.

```
\begin{tabular}{lll} 
CONIN: & IN & CMASK \\
& ANI & CHECK STATUS \\
& CIMSK & OMASK FOR INFUT \\
& IZ & CONIN \\
IN & OLOOP UNTIL REAIY \\
& CMATA & OGET THE MATA \\
ORA & A & OSET PARITY FLAG \\
JFO & PERROR & AFARITY ERROR \\
ANI & 7FH & OREMOUE FARITY
\end{tabular}
    RET
%
* PARITY-ERROR MESSAGE
&
PERROR * * *
```

This routine is essentially the same as the one given immediately before, but after the data register has been read by the computer, the parity of the byte is determined.

The ORA A instruction performs a logical OR of the accumulator with itself. A logical OR of any byte with itself will not change the byte. However, it does affect the status flags in this case. After the OR operation, the parity flag will be set according to the parity of the accumulator. If the parity is found to be odd, then an error is present. The JPO instruction causes a jump to the parity-error routine in this case. However, if the parity is found to be even, then the byte in the accumulator does not contain a parity error.

Notice that a parity check will not detect an even number of bit errors in a byte. There may be two, four, or six errors, and the parity check will not detect an error. This is not likely to be a practical problem, however, since the likelihood of two errors is much less than the likelihood of single errors.

ASCII computer terminals usually have the ability to automatically transmit an eighth parity bit with the data. Furthermore, there will typically be a user-selectable switch for choosing either even or odd parity. There may also be the additional choices of always resetting or always setting the parity bit. The input routine can check for odd parity if the JPO instruction is changed to a JPE instruction.

There are much more sophisticated methods of checking for transmission errors. One of these is the checksum approach discussed in Chapter 9. With this method, the transmitted data are added together. At regular intervals, the sum, or its complement, is transmitted along with the data. When the data are decoded, the data are added up again and compared to the checksum.

The Hamming error-correction code is even better than the checksum method. It not only detects errors, but can also correct them. In the end, however, it is wise to find out why errors occur, and to take the appropriate action to correct the problem. A dirty tape head, for example, can produce errors. Cleaning the head is better than relying on an error-correction scheme.

## CHAPTER FIVE

## Macros

Sophisticated assemblers incorporate a macro processor. A macro is used to define a set of instructions which are associated with the macro name. Then whenever the macro name appears in the source program, the assembler substitutes the corresponding instructions. This is called a macro expansion.

Suppose that we want to interchange the contents of two memory locations with the following instructions.

| LITA | FIRST | gGET FIRST EYTE |
| :---: | :---: | :---: |
| PUSH | FSW | ¢SAVE |
| LIDA | SECOND | gGET SECOND |
| STA | FIRST | ¢PUT INTO FIRST |
| FOP | FSW | ¢GET FIRST |
| STA | second | ¢FUT INTO SECOND |

This set of instructions can be defined in a macro called SWAP.

| SWAF | MACKO LDA <br> PUSH | FIRST PSW | $\begin{aligned} & \text { QSWAF } \\ & \text { iGET } \\ & \text { iSAUE } \end{aligned}$ | FIRST AND FIRST BYTE | SECOND |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | L.DA | SECONA | ¢GET | SECOND | , |
|  | STA | FIRST | ifUT | INTO FIRST |  |
|  | POF | PSW | \% GET | FIRST |  |
|  | STA | SECOND | ;PUT | INTO SECONL |  |
|  | ENAM |  |  |  |  |

The macro definition is placed near the top of the assembler source program. The first line defines the macro name; the last line terminates the definition. The name SWAP can now be used like an operation code. it is placed in the source program whenever the corresponding instructions are needed. When the assembler encounters the name SWAP, it substitutes the desired
instructions. The final binary code generated by the assembler is the same as it would be if the instructions had originally been entered into the source program.

Each time the macro name SWAP appears in the source program, the same set of instructions will be generated and the same two memory locations will be interchanged. The SWAP macro becomes more versatile if the memory locations can be changed. If the names of the memory locations are placed on the first line of the macro definition, they become dummy variables.

| SWAF | MACRO | FIRST, | SECONI |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | LIIA | FIRST | 9GET | 15 T | EYTE |
|  | PUSH | FSW | ¢SAVE |  |  |
|  | LDA | SECONA | SGET | 2ND |  |
|  | STA | FIRST | ¢PUT | INTO | 15 T |
|  | POP | PSW | AGET | 1 ST |  |
|  | STA | SECONA | ¢PUT | INTO | 2 ND |
|  | ENIM |  |  |  |  |

The actual parameters in the macro call are substituted for the dummy parameters at assembly time. The macro call

```
SWAF HIGH, LOW
```

generates the assembly language instructions

| 1.10 | HIGH | f GET | $15 T$ | gite |
| :---: | :---: | :---: | :---: | :---: |
| PUSH | FSW | \% SAVE |  |  |
| LDA | LOW | \% GET | 2ND |  |
| STA | HIGH | \&PUT | INTO | 15 T |
| POF | PSW | \% GET | 151 |  |
| STA | LOW | \%PUT | INTO | 2 NH |

The statement

SWAF LEFT, RIGHT
will produce the instructions

| LDA | LEFT | GGET 1ST EYTE |
| :---: | :---: | :---: |
| PUSH | PSW | ¢SAUE |
| LDA | RIGHT | ¢GET 2ND |
| STA | LEFT | \&PUT INTO 15T |
| FOP | FSW | ¢GET $15 T$ |
| STA | RIGHT | ©PUT INTO 2ND |

The structure of macros can be much more complicated than the above examples. One macro can be nested inside another.

| OUTER | MACRO |  |  |
| :---: | :---: | :---: | :---: |
| INNER | IF MACRO | FAST |  |
|  | - |  |  |
|  | endm |  | OINNER |
|  | ENUIF |  | \#FAST |
|  | ENDM |  | ¢ DUTER |

Conditional assembly directives can be used to create different versions. Comments in the macro definition which begin with a single semicolon are reproduced in the macro expansion along with the op codes. But if the comments are preceded by two consecutive semicolons, then they will appear only in the macro definition, not in the macro expansion.

## GENERATING THREE OUTPUT ROUTINES WITH ONE MACRO

A subroutine can be used whenever a set of instructions is needed at several places in a program. But there are times when a similar but different group of instructions is needed. A subroutine cannot be used in this case. Consider the three 8080 output routines that follow. The first sends a byte to the console, the second sends a byte to the list device, and the third sends a byte to the phone modem.

COT: | IN | CSTAT |  |
| :--- | :--- | :--- |
|  | ANI | COMSK |
|  | JZ | COT |
|  | MOU | AッC |
|  | OUT | CMATA |
|  | RET |  |
| LOT: |  |  |
|  | IN | LSTAT |
|  | ANI | LOMSK |
|  | MZ | LOT |
|  | MOU | A,C |
|  | OUT | LDATA |
|  | RET |  |
| MOT: |  |  |
|  | IN | MSTAT |
|  | ANI | MOMSK |
|  | JNZ | MOT |
|  | MOU | ADC |
|  | OUT | MDATA |
|  | RET |  |

The structure of these three routines is very similar. Each begins by reading the appropriate status register. Then a logical AND is performed to select the output-ready bit. Looping occurs until the peripheral is ready. The byte is moved from the C register into the accumulator and sent to the appropriate peripheral. Finally, a return instruction is executed.

These three routines are slightly different, hence they cannot be replaced by a single subroutine. However, since they have similar structure they can be generated with a macro. The macro definition looks like this.

| OUTPUT ?S80T: | MACRO <br> IN | $\begin{aligned} & \text { TS:TZ } \\ & \text { PS\&STAT } \end{aligned}$ | OUUTPUT ROUTINES <br> ЯCHECK STATUS |
| :---: | :---: | :---: | :---: |
|  | ANI | TS90MSK | ЯMASK FOR OUTPUT |
|  | J\&PZ | ?S\&0T | ONDT READY |
|  | MOV | A, C | AGET EYTE |
|  | OUT | PS\&DATA | OSENII IT |
|  | RET |  |  |
|  | ENDM |  |  |

It would appear near the beginning of the source program. The macro name chosen is OUTPUT and the two dummy arguments are ?S and ?Z. Dummy arguments can have the same form as any other identifier. A question mark was chosen as the first character so that the dummy arguments would be easier to find in the macro definition. You must be careful not to use register names such as $\mathrm{A}, \mathrm{B}, \mathrm{H}$, or L for dummy arguments if these register names also appear in the macro.

Each of the three output routines is generated by a one-line macro call.

|  | QuTFUT | Coz | ACONSOLE OUTFUT |
| :---: | :---: | :---: | :---: |
| \% |  |  |  |
|  | QUTPUT | $L \triangleright Z$ | OLIST OUTFUT |
| \% |  |  |  |
|  | OUTPUT | M, NZ | ¢MODEM OUTPUT |

Each line includes the appropriate parameters. At assembly time, the real arguments replace the dummy arguments of the macro. The ampersand character ( $\&$ ) is a concatenation operator. It separates a dummy argument from additional text. The macro processor substitutes the real parameter for the dummy argument, then joins it to the rest of the text. By this means the expression ?S\&OT becomes LOT if the real argument is the letter L.

Macro assemblers may give the user three options for the assembly listing:

1. Show the macro call, the generated source line, and the resultant hex code.
2. Show the macro call and the hex code.
3. Show only the macro call.

If option 1 is chosen, then the above three macro calls to OUTPUT will produce the following.

|  | QUTFUT PS\&0T: | MACRO <br> IN <br> ANI <br> J\&?Z <br> MOU <br> OUT <br> RET <br> ENLIM | ?S.?Z <br> PS\&STAT <br> PS\&OMSK <br> PS\&OT <br> AgC <br> PS\&DATA | gOUTPUT ROUTINES <br> CHECK STATUS <br> ;MASK FOR OUTPUT <br> 引NOT READY <br> gGET BYTE <br> gSENA IT |
| :---: | :---: | :---: | :---: | :---: |
|  | \% |  |  |  |
|  |  | OUTPUT | C.z | ¢ CONSOLE OUTPUT |
| $4000+11810$ | COT: | IN | CSTAT | \$CHECK STATUS |
| $4002+E 602$ |  | ANI | COMSK | IMASK FOR OUTFUT |
| $4004+C A 0040$ |  | JZ | COT | jNOT READY |
| $4007+79$ |  | MOV | A, C | FGET BYTE |
| $4008+10311$ |  | OUT | chata | 9SEND IT |
| $400 \mathrm{AtC9}$ |  | RET |  |  |
|  | و |  |  |  |
|  |  | OUTPUT | L, Z | ILIST OUTFUT |
| $400 \mathrm{~B}+\mathrm{DE12}$ | LOT: | IN | LSTAT | - ChECK Status |
| 400 $0+$ E602 |  | ANI | LOMSK | ¢MASK FOR OUTFUT |
| 400F +CAOE40 |  | JZ | LOT | ¢NOT READY |
| $4012+79$ |  | MOV | A, C | gGET EYTE |
| $4013+10313$ |  | OUT | ldata | gSENA IT |
| $4015+c 9$ |  | RET |  |  |
|  | \% |  |  |  |
|  |  | QUTPUT | MoNZ | gMONEM OUTPUT |
| $4016+10814$ | MOT: | IN | MSTAT | ¢CHECK STATUS |
| $4018+E 680$ |  | ANI | MOMSK | OMASK FOR OUTFUT |
| $401 \mathrm{AlC21640}$ |  | JNZ | MOT | ANDT REALIY |
| $4010+79$ |  | MOU | A9C | GGET EYTE |
| $4015+11315$ |  | OUT | MMATA | OSEND IT |
| $4020+69$ |  | RET |  |  |

The first argument in the macro, ?S, is replaced by the actual argument. This is the letter C in the first call, the letter L in the second call, and the letter M in the third call. The second argument is used to select a JZ or JNZ instruction for the third line of the macro expansion.

Some assemblers automatically remove the ampersand symbol from the resultant assembly listing. Others leave the symbol in place. In this latter case, the first line of the first routine would look like this.

CgOT: IN C\&STAT 今CHECK STATUS
But this is a matter of style. The actual machine code generated is the same in either case.

## GENERATING Z-80 INSTRUCTIONS WITH AN 8080 ASSEMBLER

If you have a Z-80 CPU but an 8080 macro assembler, such as the Digital Research MAC, you can run all of the 8080 programs just as they are given in this book. You can also do the Z-80 programs by using macros to generate the Z-80 instructions. For some of the instructions, the regular Zilog mnemonic can be used. For other instructions a slightly different format is
necessary. Consider, for example, the Z-80 instruction that performs a two's complement on the accumulator. The Zilog mnemonic for this operation is NEG. A Z-80 assembler converts this mnemonic into the two hex bytes ED 44. With an 8080 macro assembler you can use the same mnemonic. Define the macro

```
NEG MACRO TWO'S COMFLEMENT
    DB OEINH: A4H
    ENDM
```

Then, the macro call

## NEG

is placed in the source program when the Z-80 NEG instruction is needed. The 8080 macro assembler will insert the desired hex bytes ED 44 at this point.

As another example, consider the Z-80 relative-jump instruction. This instruction can be implemented with a macro that uses the assembler's program counter, a dollar sign. The macro definition looks like this.

JR AIIDR 解ELATIUE JUMF
IIB 18 H , ADMR-\$-1 ENDM

The dummy parameter ADDR is the destination address of the jump. The macro call

## JR ERROR

will generate the correct Z-80 code. The first byte will be 18 hex. The second byte will be the required displacement for the jump.

The Z-80 instruction, DJNZ, can be generated in a similar way. This instruction decrements the B register and jumps relative to the address of the argument if the zero flag is not set. The macro definition is

| DJNZ | MACRO | ADIRR |
| :--- | :--- | :--- |
|  | DB | $10 H y$ ADDR- $\$-1$ |
|  | ENDM |  |

and the macro call looks like

## DJNZ LOOF'

This approach will work with most macro assemblers. There may be a problem, however, with the interpretation of the dollar sign. This symbol usually refers to the address of the beginning of the current instruction. But for some assemblers, it is interpreted as the address of the following instruction.

If your assembler uses the latter interpretation, you will have to change the macro accordingly. If in doubt, check the user manual.

Some Z-80 mnemonics are not compatible with the macro format. For example, the Z-80 instruction

PUSH IX
cannot be generated with a macro called
PUSH MACRO REG
since PUSH is a regular 8080 mnemonic. One possibility is to name the macro PUSHIX instead.

| PUSHIX MACRO |  |
| :--- | :--- |
|  | DB |
|  | ENDM ONDH,OESH |

Similar problems occur with the commands POP IX, ADD IX,BC, SUB (IX+dis), and SET. A format that is different from the Z-80 mnemonic must be chosen in each of these cases.

The Digital Research macro assembler has an added bonus. Frequentlyused macros can be placed into a separate macro library and given the file extension of LIB. In fact, this assembler is supplied with a macro library called Z80.LIB that will generate all of the Z-80 instructions. The statement

MACLIB 280
is placed near the beginning of the regular source program. The assembler will then look in the file Z80.LIB for the required macros.

## EMULATING Z-80 INSTRUCTIONS WITH AN 8080 CPU

The Z-80 CPU can execute many powerful instructions that are not available to the 8080. Some of these useful instructions are difficult to implement on an 8080 , while others are simply combinations of regular 8080 instructions. The NEG instruction is one of the easiest to implement. The macro definition is

|  | MACEO |  | ¢8080 TWO'S COMPLEMENT |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | CMA |  | و刀1'5 | COMFLEMENT |  |
| NEG | INR | A | 9\%2'5 | COMPLEMENT |  |

Now, whenever a two's complement is needed, the macro call
is placed into the program．The assembler generates the required 8080 mnemonics

```
CMA
INR A
```

Another useful Z－80 operation is the arithmetic shift．This operation shifts all bits of a register one position to the left．The high－order bit is moved into carry，that is，the carry flag is set to a 1 if bit 7 was originally a value of 1 ．The carry flag is reset to zero if bit 7 was zero．A value of zero is placed into the low－order bit（bit zero）．

The 8080 instruction ADD A，which adds the value in the accumulator to itself，performs the arithmetic shift left．But for the 8080，this is the only register which can perform the shift．The Z－80 has an additional instruction which allows this operation to be performed on any of the general－purpose， 8 －bit registers or on the memory byte referenced by HL，IX，or IY．

The following macro will generate a set of 8080 instructions for the arithmetic shift left operation．


The byte is first moved to the accumulator．The next step is to add the accumulator to itself．This doubling operation performs the needed shift into carry．Then the result is returned to the original register．The value in register C can be doubled by inserting the macro call

## SLA C

This macro must be used with caution，since the accumulator will be changed during use．But the byte originally in the accumulator cannot be saved with a PUSH PSW instruction．The problem is that the subsequent POP PSW command will overlay the flag register，so that the carry result of the shift will be lost．One solution is to save the accumulator in memory．

| SLA | MACRO STA | REG SAVE | ЯSHIFT LEFT ARITH引力 $\hat{9}$ SAVE A |
| :---: | :---: | :---: | :---: |
|  | MOU | A）REG | ¢ि¢GET BYTE |
|  | ADI | A | $\hat{\text { ¢ SHIFT LEFT }}$ |
|  | MOV | REG：A | G ¢PUT EACK |
|  | LDA | SAVE | 今िRESTORE A |
|  | ENDM |  |  |

## THE REPEAT MACROS

There are times when several lines of identical or nearly identical lines of code are needed. Three repeat macros, REPT, IRP, and IRPC are provided for this purpose. The repeat macros differ from the regular macros in that they are placed directly into the source program where they are needed. The macro definition is the macro call. In the simplest form, an instruction or group of instructions can be replicated. The expression

```
REPT A
RAR
ENDM
```

will generate the four lines

```
RAR
```

RAR
RAR
RAR

By using the SET directive, this operation can become more versatile. The SET instruction is like an EQU except that the value can be redefined. The lines

| ADDR | SET | 8000 H |
| :--- | :--- | :--- |
|  | KEFT | 4 |
| ALIDR | SET | ADMR +3 |
|  | LIW | ADLUR |
|  | ENDM |  |

will generate the code corresponding to

| DW | 8003 H |
| :--- | :--- |
| DW | 8006 H |
| DW | 8009 H |
| DW | 800 CH |

Such a series could refer to jump vectors that are spaced three bytes apart.
The repeat macro, combined with the conditional-assembly directive, can generate the required number of nulls after a carriage-return, line-feed pair. This will give the printer time to return to the left margin. Some printers need no nulls, whereas others may need as many as six or seven. The source code could be

```
%
* OUTPUT TO l.IST DEVICE
;
LOUT: IN LSTAT
    ANI LOMSK
    JZ LOUT
    MOU ADC GGET IIATA
    OUT LDATA SSEND BYTE
```

|  | IF | NULLS | 0 |
| :---: | :---: | :---: | :---: |
|  | ANI | 7FH | ©REMOVE PARITY |
|  | CPI | CR | © CARRIAGE RETURN? |
|  | RNZ |  | ; NO |
|  | MUI | C.O | ¢GET A NULL |
| ; |  |  |  |
|  | REPT | NULLS | ¢ HOW MANY? |
|  | CALL | LOUT | SEND NULL |
|  | ENDM |  | ¢REPEAT MACRO |
|  | ENDIF |  | \% NULLS |
| j |  |  |  |

The first part is a typical output subroutine. A call is made with the byte in register C. When the output device is ready, the byte is moved from the C register to the accumulator. It is then sent to the printer. If no nulls are required, then the passage from

```
    IF NULLS>0
to
```

ENDIF
is not assembled. On the other hand, if nulls are required, then this passage is assembled. If four nulls are needed, then the assembler will generate four lines of

## CALL LOUT 戶SEND NULL

The list output routine calls itself to produce the required nulls. The identifier called NULLS must be previously set to the necessary number of nulls.

There are two other repeat macros called IRP and IRPC. A set of onecharacter message routines can be generated by using the indefinite repeat macro IRPC. This example will introduce something called a programming trick. Some people think that it is a horrible example of programming. Others think it is very clever. Its purpose is to save two bytes of instruction each time it is used. In addition, less branching is required.

Suppose that we need five different message routines that each produce a single character. The instructions might look like

| CHARC: | MUI | $A^{\prime} C^{\prime}$ |
| :---: | :---: | :---: |
|  | JMP | OUTT |
| CHARM: | MUI | A, 'M' |
|  | JMP | OUTT |
| CHARR: | MUI | A ' $\mathrm{R}^{\prime}$ |
|  | JMP | OUTT |
| CHAR?: | MUI | Ag'p' |
|  | JMF' | OUTT |
| CHAR\%: | MUI | A, '\$' |
|  | JMF | OUTT |
|  | < | rout |

If the $B$ and $C$ registers are not in use, we can shorten the above passage by replacing each line containing the instruction JMP OUTT with a line of DB1.

| CHARC: | MUI | Ag' ${ }^{\prime}$ |
| :---: | :---: | :---: |
|  | 10B | 1 |
| CHARM: | MUI | A9'M' |
|  | DE | 1 |
| CHARR: | MUI | $A^{\prime}{ }^{\prime} R^{\prime}$ |
|  | DR | 1 |
| CHAR?: | MUI | Ay'?' |
|  | 1 B | 1 |
| CHAR \& ค. | MUI | A. ${ }^{\text {\% }}$ |
| OUTT: |  |  |

Let's see how this works. Suppose that a branch is made to the label CHARC. The accumulator is loaded with an ASCII letter C. The next byte, a DB 1, looks like the start of an LXI B instruction. The following two bytes, corresponding to the MVI A,' $\mathrm{M}^{\prime}$ instruction, will be interpreted as the argument for the LXI instruction. That is, they will be considered as data. The same will hold for the other occurrences of DB 1. By this means, we have effectively shortened the code. We no longer need the JMP statements. Caution: a disassembler is not likely to interpret this passage correctly. It looks like there are labels pointing into the middle of the LXI instructions. Notice that the second version has subroutine OUTT positioned directly under the CHAR\$ routine, so that no JMP instruction is needed at this point.

The second version can be easily generated with the IRPC macro. Only five lines are needed in the source program.

|  | IRPC | X, CMPR? |  |
| :---: | :---: | :---: | :---: |
|  | D8 | 1 | PFAKE LXI B |
| CHAR号: | MUI |  |  |
|  | ENDM |  |  |

The five different message routines are all generated with this single macro. One replication is made for each character of the second argument to IRPC.

## PRINTING STRINGS WITH MACROS

Suppose that we want to send messages to the console from various points of a program. We could write a subroutine called SENDM for this purpose.

| SENDM: | LIAAX | 0 | \#GET CHAR |
| :---: | :---: | :---: | :---: |
|  | ORA | A | ZERO? |
|  | RZ |  | ¢YES |
|  | INX | 0 | FPOINTER |
|  | MOV | $C, A$ |  |
|  | CALL | OUTT | SENT |
|  | JMP | SENDM | A NEXT |

The address of the message is loaded into the DE register and subroutine SENDM is called.

```
LXI D,MESSI
CALL SENDM
```

Subroutine SENDM prints a message by sending each character to the output subroutine OUTT. When a binary zero, used to indicate the end of the message, is found, SENDM returns to the calling program.

We can simplify the sending of messages by using a macro called PRINT. At each point we write

```
FRINT <CHECKSUM ERROR`
PRINT <END OF FILE>
PRINT <OUTPUT TO LISTP>
```

The macro called PRINT will generate the message given in the argument. The message is enclosed in angle brackets because the blanks are part of the argument.

If subroutine SENDM were placed into the macro body, then one copy of SENDM would be inserted for each occurrence of the PRINT statement. But we don't need more than one copy of SENDM. On the other hand, if we don't include SENDM in the macro, there may not be any copies at all. What we need is a mechanism for inserting one, and only one, copy of SENDM regardless of how many times we give the PRINT command.

The solution is to write a double macro-one nested inside the other. Both macros will be given the same name. Subroutine SENDM will be part of the outer macro which will be expanded only once. The layout looks like this.

| PRINT | MACRO | <messase> | SOUTER MACRO |  |
| :---: | :---: | :---: | :---: | :---: |
|  | [define | SENDM] |  |  |
|  | MACRO | <messase> | GINNER | MACRO |
| PRINT | [send m |  |  |  |
|  | ENDM |  | NER MAC | RO |
|  | ENDM |  | TEF MAC | Ro |

The source program in Listing 5.1 demonstrates this technique. The outer macro PRINT has the argument ?TEXT, used for the first call to the macro. Subroutine SENDM is generated at this time. Additional macro calls to PRINT utilize the inner macro which has the argument ?TEXT2. Subroutine SENDM is not generated on these subsequent calls.

```
Listins 5.1. Source listins for a macro
    demonstration frosram.
%
FRINT MACRO TTEXT
    LOCAL AROUNA
#
#
; SUBROUTINE TO SEND A STRING TO
; THE CONSOLE. BINARY ZERO AT STRING END.
; IIE IS STRING FOINTER.
%
SENIM: LIIAX I% OGET CHAR
    OFA A \hat{ZERO?}
    FZ FYES
    INX & FPOINTEF
    MOU CyA
    CALL OUTT SSENT
    JMF SENLM SNEXT
&
AROUND:
&
& RELIEFINE THE MACRO
g
FRINT MACRO ?TEXT2
    LOCAL MESGyCONT
&
    FUSH II ASAUE M,E
    LXI H.MESG GFOINT
    CALL SENIM
    FOF II EFESTORE
    JMF CONT SSKIF MESSAGE
#
MESG:
    MB CFgLF,'&?TEXT2',O
#
CONT: ENDM FINNER MACRO
    FFINT <?TEXT`
    ENIMM gOUTER MACRO
;
CSTAT EQU 10H fCONSOLE STATUS
CIATA EQU CSTATH1 क्CONSOLE MATA
CF EQU 13 FCAFRIAGE RETUFN
LF EQU 10 flINE FEEN
g
ORG 100H
START:
    FRINT <CHECKSUM ERROR.>
#
    FRINT <ENO OF FILE.`
    FRINT <OUTFUT TO LIST?S
    JMF O ORETURN TO CF/M
#
; SENLI CHARACTER IN C TO THE CONSOLE
```

| OUTT: | IN | CSTAT |
| :--- | :--- | :--- |
|  | ANI | 2 |
|  | JZ | OUTT |
|  | MOU | A,C |
|  | OUT | CLATA |
|  | RET |  |
|  |  |  |
|  | ENI |  |

Subroutine SENDM is coded into the main flow of the program, that is, it is an inline routine. It is therefore necessary to jump around SENDM. Additionally, there must be a branch around each of the messages, since they too are coded inline. Labels for the required branches are uniquely generated in the macro by declaring the corresponding labels as LOCAL. The resulting assembly listing is given in Listing 5.2. The assembler places plus symbols between the address and the generated code of the assembly listing to designate those lines that were generated by macros. Thus, lines that contain plus symbols were not present in the original source listing.

```
Listins 5.2. Assembls listiris for a macro
    demonstration frosram.
    %
    FRINT MACRO ?TEXT
        LOCAL AROUNA
    #
        JMF AROUNDI FSENIM
    S SURFOUTINE TO SENA A STFING TO
    * THE CONSOLE GINAFY ZERO AT STRING ENDI.
    * D,E IS STRING POINTER.
    #
    SENDM: LIIAX II OGET CHAFI
        ORA A SZERO?
        RZ \hat{y YES}
        INX II FFOINTEF
        MOU C,A
        CALL OUTT \hat{SENT}
        JMF SENIIM SNEXT
    \hat{b}
    AFOUND:
    %
    REDEFINE THE MACFO
    \hat{p}
    FRINT MACRO PTEXYZ
        LOCAL MESG,CONT
    #
        FUSH II OSAVE HgE
        LXI IIMESG \hat{FOINT}
        CALL SENLM
        FOF II FRESTORE
        JMP CONT \SK゙IF MESSAGE
    琣
    MESG:
        MB CF,LF,'&TREXT2',0
\begin{tabular}{|c|c|c|c|c|}
\hline & CONT: & ENIMM FRINT ENDM & ¢PTEXT. & \begin{tabular}{l}
tinner macro \\
jOUTER MACRO
\end{tabular} \\
\hline & ; & & & \\
\hline \(0010=\) & cstat & EQU & 10 H & - Console status \\
\hline \(0011=\) & clata & EQU & cstatti & console lata \\
\hline 00011 \(=\) & CF: & EQU & 13 & ¢CARRIAGE RETURN \\
\hline OOOA \(=\) & \[
{\underset{i}{\hat{j}}}_{\text {LF }}
\] & EQu & 10 & oline feen \\
\hline \multirow[t]{2}{*}{0100} & ORG & 100 H & & \\
\hline & START: & & & \\
\hline \multicolumn{2}{|l|}{\multirow[b]{2}{*}{O100+C30E01}} & PRINT & \multicolumn{2}{|l|}{CHECKSUM ERROR.>} \\
\hline & & JMF' & ? \(0^{0} 0001\) & gSENIM \\
\hline \(0103+1\) A & SENIM: & lunax & \(\square\) & gGET CHAF \\
\hline \multicolumn{2}{|l|}{0104+87} & ORA & A & ; ZERO? \\
\hline \multicolumn{2}{|l|}{\(0105+c 8\)} & kZ & & \#yEs \\
\hline \multicolumn{2}{|l|}{\(0106+13\)} & INX & 0 & ¢POINTER \\
\hline \multicolumn{2}{|l|}{0107+4F} & MOV & C, A & \\
\hline \multicolumn{2}{|l|}{\(0108+C 16501\)} & CALL & OUTT & \#SENT \\
\hline \multicolumn{2}{|l|}{\(010 \mathrm{BtC30301}\)} & JMF & SENDM & SNEXT \\
\hline \multicolumn{2}{|l|}{010Et15} & FUSH & & SAVE D,E \\
\hline \multicolumn{2}{|l|}{010F+111901} & LXI & 1, 9 ? 90002 & AFOINT \\
\hline \multicolumn{2}{|l|}{0112+CD0301} & CALL & SENUM & \\
\hline \multicolumn{2}{|l|}{\(0115+111\)} & FOF & \(\square\) & \% RESTORE \\
\hline \multicolumn{2}{|l|}{0116+C32B01} & JMP & ? 90003 & ¢SKIF MESSAGE \\
\hline \multicolumn{2}{|l|}{\(0119+0\) NOA434845} & D8 & CR,LF, 'CH & HECKSUM EFROR.'yO \\
\hline \multicolumn{5}{|l|}{\%} \\
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{0128+105}} & FRINT & SEND OF F & FILE. \({ }^{\text {c }}\) \\
\hline & & FUSH & & ¢SAUE D,E \\
\hline \multicolumn{2}{|l|}{\(012 \mathrm{C}+113601\)} & LXI & 10? 9 ?0004 & 9POINT \\
\hline \multicolumn{2}{|l|}{012F+CD0301} & CALL & SENDM & \\
\hline \multicolumn{2}{|l|}{\(0132+111\)} & FOF & 10 & ;RESTORE \\
\hline \multicolumn{2}{|l|}{\(0133+C 34501\)} & JMF' & ? 20005 & GSKIF MESSAGE \\
\hline \multicolumn{2}{|l|}{0136tOLOAASAEAA} & HE & CR,LF,'EN & ND OF FILE.',O \\
\hline \multicolumn{2}{|l|}{*} & & & \\
\hline & & FRINT & <OUTFUT & TO LIST? \\
\hline \multicolumn{2}{|l|}{\(0145+05\)} & PUSH & [ & ¢SAVE D,E \\
\hline \multicolumn{2}{|l|}{\(0146+115001\)} & LXI &  & ¢FOINT \\
\hline \multicolumn{2}{|l|}{\(0149+\) C10301} & CALL & SENDM & \\
\hline \multicolumn{2}{|l|}{\(014 \mathrm{Ct} 1{ }^{\text {d }}\)} & POF & 1 & \%RESTORE \\
\hline \multicolumn{2}{|l|}{\(01451+\mathrm{C} 36201\)} & JMP & ? 20007 & OSKIF MESSAGE \\
\hline \multicolumn{2}{|l|}{0150+010A4F5554} & ng & CFiolfy' & UTFUT TO LIST?\%o \\
\hline \multicolumn{2}{|l|}{0162 C30000} & JMF & \(\bigcirc\) & GRETURN TO CF/M \\
\hline & \% & & & \\
\hline & ; SENI & \multicolumn{3}{|l|}{character in c to the console} \\
\hline & & & & \\
\hline 0165 D810 & OUTT: & IN & cstat & \\
\hline 0167 E602 & & ANI & 2 & \\
\hline 0169 CA6501 & & JZ & OUTT & \\
\hline 016 C 79 & & mov & A, C & \\
\hline 016010311 & & OUT & cmata & \\
\hline 016F C9 & & RET & & \\
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{0170 )}} & & & \\
\hline & & ND & & \\
\hline
\end{tabular}

If you are familiar with the operation of your assembler, type up the demonstration program and try it out. Branch to the beginning and three messages will appear at the console.
```

Checksu\# error
Eno of fille
Output to list?

```

Assembler operation will be considered in the next chapter.
By constructing increasingly complicated macros, it is possible to develop some of the structure that is characteristic of higher-level languages such as Pascal. The common loop constructions
```

    REPEAT
    . . .
    UNTIL <condition true>
and

```
```

LOOF

```
LOOF
EXITIF <condition true>
EXITIF <condition true>
**.
**.
ENDLOOF
```

ENDLOOF

```
can be realized with macros called REPEAT, UNTIL, and so on. The arguments to UNTIL and EXITIF will consist of three terms. The first and third will be numeric values. The middle term will represent a logical operation such as EQUALS or LESS THAN. The spelling of the logical operators in this case will have to be unusual, since the normal spellings

EQ
LT
GE
are already utilized by the macro assembler. Macros for all of the common structures are available commercially. Also, source programs for structured macros of this type may be given in the instruction manual for your macro assembler.

\section*{CHAPTER SIX}

\section*{Development of a System Monitor}

The best way to learn assembly language programming is to actually do it. Consequently, in this chapter you will develop a small but very powerful utility program called a monitor. There are many useful things that can be done with the monitor. There is a command to examine memory and another to change it. Other commands deal with memory blocks. These allow you to move a block from one location to another. Some of the features will duplicate those found in other programs, but other features, such as a search routine and a memory test routine, will be unique.

You will not program the entire monitor at one time. Instead, you will start with just the bare essentials. You will check the monitor after each major change to ensure that the new features have been added correctly. With this so-called top-down method, any error that develops is likely to be found in the most recently added instructions. As new features are incorporated, the monitor will increase in size until it reaches 1 K bytes. This is a size that can be easily programmed into a single ROM. The monitor will then be immediately available as soon as the computer is turned on.

An editor and an assembler are required for the development of the monitor. In addition, a debugger will be helpful if you have problems along the way. Each phase of the development will require the same sequence of steps.
1. Generate an assembly language source file with the editor.
2. Assemble the source program to produce an object file.
3. Compare the hex code from your assembly listing to the listing given in this chapter.
4. Load the object program into memory.
5. Branch to the monitor and try it out.

The assembly listings given in this chapter are written with 8080 mnemonics. You can use an 8080 assembler for these programs whether you have an 8080 or a Z-80 CPU. The resulting code will run on both an 8080 and a Z-80 CPU. If you have only a Z-80 assembler, you will have to change the mnemonics. The cross-reference between the 8080 and Z-80 mnemonics, given in Appendix G, can be used to find the corresponding instructions. Alternately, you can define the 8080 mnemonics as macros.

\section*{PROGRAM DEVELOPMENT DETAILS}

This section describes the details of program development. Skip to the next section if you are familiar with the operation of your editor and assembler. An editor is needed to create and alter the assembly language source file. If you have \(\mathrm{CP} / \mathrm{M}\), you will have an editor called ED. Other editors, such as ED-80, EDIT80, and Word-Master, are separately available.

The session begins by giving the name of the editor and the name of the source program. The following discussion assumes that you have CP/M. If you have some other operating system, the approach will be similar, but the details may differ. Put the CP/M system diskette in drive \(A\) and a working diskette in drive \(B\) if you have more than one drive. Go to drive \(B\) with the command
\(A>B:\)
The response will be
B.)

Type the name of the editor followed by the name of the monitor source. program. The command line might look like this.
```

B.A:ED MON1.ASM

```
for the first version. The digit 1 in the filename refers to the version number. The file type is ASM for the Digital Research assemblers ASM and MAC. The file type should be chosen as MAC, however, if the Microsoft assembler is used.

As you type the source program, be careful to include only the instructions and the comments shown in Listing 6.1A. Do not type the resulting hex code that is also given at the beginning of each line. For example, the line that defines the parameter TOP, on the first page of the listing, should be typed as
TOF EQU 24 MEMORY TOP, K BYTES
rather than as:
\(0018=\) TOP EQU 24 MEMORY TOF, K BYTES
Type a Control-I or tab to automatically generate the blank spaces between symbols.

Most of the assembly language symbols have five or fewer characters. This is acceptable to many assemblers. However, if your assembler only allows names to have a maximum of five characters, then several symbols will have to be shortened. The TITLE directive, on the first line, is another potential problem. The CP/M version is shown. The apostrophes should be removed if the Microsoft assembler is utilized. If the TITLE directive is not available on your assembler, place a semicolon at the beginning of this first line to convert it to a comment.

\section*{VERSION 1: THE INPUT AND OUTPUT ROUTINES}

Refer to Listing 6.1A. This version will contain only the input and output routines. Generate an assembler source file with the system editor. The following variables will have to be tailored to your particular system.
\begin{tabular}{ll} 
TOP & (top of usable memory, decimal K) \\
HOME & (where to return when done) \\
CSTAT & (console input status address) \\
CDATA & (console input data address) \\
CSTATO & (console output status address) \\
CDATAO & (console output data address) \\
INMSK & (input-ready mask) \\
OMSK & (output-ready mask) \\
BACKUP & (console backspace character)
\end{tabular}

Normally, CSTATO will be the same as CSTAT, and CDATAO will be the same as CDATA. But if your console input address is different from your console output address, then each can be separately defined. Furthermore, the address of CDATA will typically have a value one larger or smaller than that of CSTAT.

Listins 6.1A. The Desinnins of a system monitor.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & ```
TITLE
#
* (Fut
;
``` & \[
\begin{aligned}
& \text { '8080 } 5: \\
& \text { today's }
\end{aligned}
\] & \begin{tabular}{l}
sstem mon \\
date here
\end{tabular} & \begin{tabular}{l}
itorg ver \(1^{\prime}\) \\
e)
\end{tabular} \\
\hline 0018 & \(=\) & TOF' & EQU & 24 & 9MEMORY TOF', \(K\) R \\
\hline 5800 & \(=\) & ORGIN & EQU & (TOF-2) \({ }^{\text {\% }}\) & W1024 OPROGRAM \\
\hline 5800 & & \[
\begin{aligned}
& \text { ORG } \\
& ?
\end{aligned}
\] & ORGIN & & \\
\hline 0000 & \(=\) & HOME & EQU & 0 & 9ABOFT (UER 1-2) \\
\hline & & HOME & ERU & DRGIN & \% ABORT ALMEESS \\
\hline 0031 & \(=\) & VEFS & ERU & '1' & \%UEFSION NUMEER \\
\hline 57A0 & \(=\) & STACK & EQU & \multicolumn{2}{|l|}{ORGIN-60H} \\
\hline 0010 & \(=\) & CSTAT & ERU & 10 H & SCONSOLE STATUS \\
\hline 0011 & \(=\) & CHATA & EQU & CSTAT+1 & ¢CONSOLE LIATA \\
\hline 0010 & \(=\) & CSTATO & EQU & cstat & ¢CON OUT STATUS \\
\hline 0011 & \(=\) & cratad & ERU & CsTATO+1 & 1 jout Inata \\
\hline 0001 & \(=\) & INMSK & ERU & 1 & ¢INFUT MASK \\
\hline 0002 & \(=\) & OMSK & ERU & 2 & GOUTFUT MASK \\
\hline 57A0 & \(=\) & FORTN & EQU & STACK & 33 EYTES I/0 \\
\hline 57 A 3 & \(=\) & IBUFF' & EQU & STACK +3 & GBUFFEF FOINTER \\
\hline 57 A5 & \(=\) & IRUFC & EQU & IBUFF+2 & ©EUFFER COUNT \\
\hline 57A6 & \(=\) & IBUFF & ERU & IBUFF+3 & SINFUT EUFFEF \\
\hline 0008 & \(=\) & CTRH & EQU & 8 & \% M EACKSFACE \\
\hline 0009 & \(=\) & TAB & EQU & 9 & \(i^{m} \mathrm{I}\) \\
\hline 0011 & \(=\) & CTRQ & EQU & 17 & \(\bigcirc \mathrm{m}\) \\
\hline 0013 & \(=\) & CTRS & ERU & 19 & 9 s \\
\hline 0018 & \(=\) & CTEX & ERU & 24 & ¢"X, ABORT \\
\hline 0008 & \(=\) & BACKUF & EQU & CTEH & - BACKUF CHAF \\
\hline 007F & \(=\) & DEL & ERU & 127 & ; FUEOUT \\
\hline 001 B & \(=\) & ESC & ERU & 27 & - ESCAFE \\
\hline 0057 & \(=\) & AF'OS & EQU & \multicolumn{2}{|l|}{(39-10') ANI OFFH} \\
\hline 000n & \(=\) & CR & ERU & 13 & GCAKRIAGE RET \\
\hline OOOA & \(=\) & L.F & EQU & 10 & SLINE: FEEI \\
\hline OONB & \(=\) & INC & EQU & OLEH & AIN DF COLIE \\
\hline 00113 & \(=\) & OUTC & ERU & On3 \({ }^{\text {O }}\) & SOUT OF COLIE \\
\hline 00c9 & \(=\) & \begin{tabular}{l}
RETC \\
名 \\
START:
\end{tabular} & ERU & OCSH & SFET OF CORE \\
\hline 5800 & C34A58 & START: & JMF' & COLII & - COLII START \\
\hline 5803 & C35358 & \begin{tabular}{l}
RESTRT: ; \\
- CONSOL \\
;
\end{tabular} & \begin{tabular}{l}
JMF \\
LE INFUT
\end{tabular} & WAFM
FOUTINE & \% WARM START \\
\hline 5806 & C01658 & INFUTT: & CALL & INSTAT & OCHECK STATUS \\
\hline 5809 & CA0658 & & JZ & INFUTT & SNOT FEALIY *** \\
\hline 580C & [H11 & INFUT2: & IN & clata & gGET EYTE \\
\hline 580 E & E67F & & ANI & HEL & \\
\hline 5810 & FE18 & & CFI & CTRX & ¢AEORT? \\
\hline 5812 & CA0000 & & JZ & HOME & ¢ YES \\
\hline 5815 & & \multicolumn{4}{|c|}{RET} \\
\hline & & \[
\begin{aligned}
& \hat{j} \\
& \hat{i} \\
& \hat{g}
\end{aligned} \text { GET }
\] & ONSOLE-IA & NFUT STAT & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|}
\hline 5816 & L1810 & \multirow[t]{3}{*}{INSTAT:} & IN & \multicolumn{2}{|l|}{CSTAT} \\
\hline 5818 & E601 & & ANI & INMSK & \\
\hline 581A & C9 & & \multicolumn{3}{|l|}{RET} \\
\hline & & \multicolumn{4}{|l|}{\multirow[t]{2}{*}{\% CONSOLE OUTFUT FOUTINE}} \\
\hline & & & & & \\
\hline & & \% & & & \\
\hline 5818 & \(F 5\) & OUTT: & FUSH & FSW & \\
\hline 581 C & C11658 & OUT2: & CALL & INSTAT & ¢ INFUT? \\
\hline \(581 F\) & CA3558 & & JZ & OUTA & ¢NO *** \\
\hline 5822 & CnOC58 & & CAll & INFUT2 & ¢GET INFUT \\
\hline 5825 & FE13 & & CFI & CTRS & OFREEZE? \\
\hline \multirow[t]{3}{*}{5827} & C21058 & & JNZ & oure & iNO \\
\hline & & \multicolumn{4}{|l|}{; JNZ} \\
\hline & & \multicolumn{2}{|l|}{; FFEEZE OUTFUT U :} & \multicolumn{2}{|l|}{UNTIL Ma OR \({ }^{\text {" }}\) X} \\
\hline 582A & C10658 & OUT3: & CALL. & INFUTT & GINFUT? \\
\hline 582 L & FE11 & & CFI & CTRQ & ¢RESUME? \\
\hline 582 F & C22A58 & & JNZ & OUT3 & ¢ NO \\
\hline \multirow[t]{2}{*}{5832} & c31058 & & JMF & OUT2 & \\
\hline & & \multicolumn{4}{|l|}{\% \({ }^{\text {\% }}\)} \\
\hline 5835 & \(\underline{1210}\) & \multirow[t]{6}{*}{OUT4:} & IN & cstato & 9 CHECK STATUS \\
\hline 5837 & E602 & & ANI & OMSK & \\
\hline 5839 & CA1C58 & & \(J Z\) & OUT2 & ¢NOT REALIY *** \\
\hline 5836 & F1 & & POF & FSW & \\
\hline 58311 & 11311 & & OUT & criatao & YSENII IATA \\
\hline \multirow[t]{2}{*}{\(583 F\)} & C9 & & RET & & \\
\hline & & \multicolumn{4}{|l|}{وे} \\
\hline 5840 & OLIOA & \multirow[t]{4}{*}{SIGNDN:} & H2] & \multicolumn{2}{|l|}{CFiglF} \\
\hline 5842 & 205665 & & L1B & \multicolumn{2}{|l|}{, Ver} \\
\hline 5847 & 3100 & & DW & \multicolumn{2}{|l|}{UEES} \\
\hline \multirow[t]{3}{*}{5849} & 00 & & [1E & 0 & \\
\hline & & \multicolumn{4}{|l|}{\(\hat{\text { p }}\)} \\
\hline & & \multicolumn{4}{|l|}{© CONTINUATION OF COLII START )} \\
\hline 584 A & 314057 & \multirow[t]{3}{*}{COLII:} & LXI & \multicolumn{2}{|l|}{SF.STACK} \\
\hline 5840 & 114058 & & LXI & \multirow[t]{3}{*}{D, SIGNON
SENLIM} & gMESSAGE \\
\hline \multirow[t]{3}{*}{5850} & CDE258 & & CALL & & ¢SENII IT \\
\hline & & \multicolumn{3}{|l|}{\(\hat{\mathrm{y}}\)} & \\
\hline & & \multicolumn{4}{|l|}{- WAKM-STAFT ENTRY \%} \\
\hline 5853 & 215358 & WARM: & LXI & H: WARM & وFETURN HERE \\
\hline 5856 & E5 & & FUSH & H & \\
\hline 5857 & CHB658 & & CALL & CRLLF & ONEW LINE \\
\hline 585A & C17758 & & CALL & INF:L & f CONSOLE LINE \\
\hline 5854 & craccss & & CALL & GETCH & GGET CHAR \\
\hline 5860 & FE44 & & CFI & ' L', & ¢ LIUMF- \\
\hline \multirow[t]{2}{*}{5862} & CA5358 & & JZ & WARM & \% (UEF 1) \\
\hline & & \multirow[t]{3}{*}{\%} & \(J 2\) & DUMF & ¢HEX/ASCII (2) \\
\hline 5865 & FE43 & & CFI & 'C' & - CALL \\
\hline \multirow[t]{2}{*}{5867} & CAS358 & & JZ & WARM & \% (VEF 1-2) \\
\hline & & \multirow[t]{3}{*}{\%} & JZ & CALLS & ¢SUBROUTINE (3) \\
\hline 586 A & FE47 & & CFI & 'G' & ¢ GO \\
\hline \multirow[t]{2}{*}{586 C} & CAS358 & & JZ & WARM & \% (UER 1-2) \\
\hline & & \multirow[t]{3}{*}{\%} & JZ & GO & \% SOMEWHEFE (3) \\
\hline \multirow[t]{3}{*}{\[
\begin{aligned}
& 586 F \\
& 5871
\end{aligned}
\]} & FEAC & & CFI & 'L' & \(\hat{\text { i }}\) LOAI \\
\hline & CA5358 & & JZ & WAFM & ' (VER 1-3) \\
\hline & & \% & \(J Z\) & LOALI & - INTO MEMORY (4) \\
\hline 5874 & c35358 & & JMF & WAFIM & ¢TEY AGAIN \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline 5877 & 3E3E \\
\hline 5879 & Cп1B58 \\
\hline 587 C & 214657 \\
\hline 587 F & 22 A 357 \\
\hline 5882 & OEOO \\
\hline 5884 & CH0658 \\
\hline 5887 & FE20 \\
\hline 5889 & DAA858 \\
\hline 588 C & FE7F \\
\hline 588 E & CACO58 \\
\hline 5891 & FE5B \\
\hline 5893 & LA9858 \\
\hline 5896 & E6SF \\
\hline 5898 & 77 \\
\hline 5899 & 3E20 \\
\hline 589 E & E9 \\
\hline 589 C & CA8458 \\
\hline 589F & \(7 E\) \\
\hline 58AO & 23 \\
\hline \(58 \mathrm{A1}\) & OC \\
\hline 58 F 2 & CD1858 \\
\hline 5845 & C38458 \\
\hline
\end{tabular}
\(58 A 8\) FEO
58AA CACO58 58ALI FEOI \(58 A F\) C28458
\(\begin{array}{ll}58 \mathrm{E} 2 & 79 \\ 58 \mathrm{~B} & 32 \mathrm{~A} 57\end{array}\)
\(58 B 6\) 3EOD
\(58 B 8\) CD1B58
58BE 3EOA
58 BL C31858
58C0 79
58С1 B7
58 C 2 CA845B
\(58 C 5\) 2E
58C6 OD
\(58 C 7\) 3EO8
58 C 9 C 3 A 258
```

INFUT A LINE FROM CONSOLE ANLI FUT IT

```
INFUT A LINE FROM CONSOLE ANLI FUT IT
* INTO THE EUFFER. CARRIAGE RETURN ENDS
* INTO THE EUFFER. CARRIAGE RETURN ENDS
f THE LINE. FUBOUT OF "H COFRECTS LAST
f THE LINE. FUBOUT OF "H COFRECTS LAST
& LAST ENTKY. CONTFOL-X FESTAFTS LINE.
& LAST ENTKY. CONTFOL-X FESTAFTS LINE.
% OTHER CONTROL CHARACTERSS ARE IGNOREN
% OTHER CONTROL CHARACTERSS ARE IGNOREN
%
%
INFLN: MUI Ay'`, \hat{FFROMFT}
INFLN: MUI Ay'`, \hat{FFROMFT}
    CALL OUTT
    CALL OUTT
INFL2: LXI HyIBUFF क्GUFFER ALLR
INFL2: LXI HyIBUFF क्GUFFER ALLR
    SHLII TRUFF $SAVE FOINTEF
    SHLII TRUFF $SAVE FOINTEF
    MUI C,O कCOUNT
    MUI C,O कCOUNT
INFLI: CALL INFUTT \hat{FCONSOLE CHAF}
INFLI: CALL INFUTT \hat{FCONSOLE CHAF}
    CFII , , %CONTFOL?
    CFII , , %CONTFOL?
    JC INFLC \hat{YES}
    JC INFLC \hat{YES}
    CFI DEL GIELETE
    CFI DEL GIELETE
    JZ INFLE \hat{YES}
    JZ INFLE \hat{YES}
    CFI 'Z'+1 SUFFER CASE?
    CFI 'Z'+1 SUFFER CASE?
    JC INFLZ3 औYES
    JC INFLZ3 औYES
    ANI SFH \MAKE UFFEF
    ANI SFH \MAKE UFFEF
            MOU MOA OINTO EUFFEF
            MOU MOA OINTO EUFFEF
            MUI A,32 FEUFFEF SIZE
            MUI A,32 FEUFFEF SIZE
            CMF C FFULL?
            CMF C FFULL?
            JZ INFLI GYESy LOOF
            JZ INFLI GYESy LOOF
            MOU AgM जGET CHAR
            MOU AgM जGET CHAR
            INX H \hat{ INCF FOINTEF}
            INX H \hat{ INCF FOINTEF}
            INF: C \hat{AND COUNT}
            INF: C \hat{AND COUNT}
INFLE: CALL OUTT 
INFLE: CALL OUTT 
INFLE: CALL OUTT 隹 SHOW CHAR
INFLE: CALL OUTT 隹 SHOW CHAR
\hat{p}
\hat{p}
FFFOCESS CONTFOL CHARACTER
FFFOCESS CONTFOL CHARACTER
\hat{y}
\hat{y}
INFLC: CFI CTRH %M?
INFLC: CFI CTRH %M?
    JZ INFLR \emptysetYES
    JZ INFLR \emptysetYES
    CFI CK GKETUFN?
    CFI CK GKETUFN?
            JNZ INFLII {NO, IGNORE
            JNZ INFLII {NO, IGNORE
%
%
% ENII OF INFUT LINE
% ENII OF INFUT LINE
\hat{%}
\hat{%}
            MOV AяC \hat{gCOUNT}
            MOV AяC \hat{gCOUNT}
            STA IBUFC \hat{SAVE}
            STA IBUFC \hat{SAVE}
\hat{\}
\hat{\}
CARFIAGE-FETURN, LINE-FEEI FOUTINE
CARFIAGE-FETURN, LINE-FEEI FOUTINE
%
%
CFLF: MUI A,CR
CFLF: MUI A,CR
            CALL OUTT क्SENL CF
            CALL OUTT क्SENL CF
            MUI A,LF
            MUI A,LF
            JMF: OUTT क्SENI LF
            JMF: OUTT क्SENI LF
%
%
; IELETE FRIOR CHARACTER IF ANY
; IELETE FRIOR CHARACTER IF ANY
\hat{0}
\hat{0}
INPLE: MOU A,C OCHAR COUNT
INPLE: MOU A,C OCHAR COUNT
            ORA A EZERO?
            ORA A EZERO?
            JZ INFLI #YES
            JZ INFLI #YES
            DCX H #BACK FOINTEF
            DCX H #BACK FOINTEF
            LCF C FANI COUNT
            LCF C FANI COUNT
            MUI AgEACK゙UF ;CHAFACTEF
            MUI AgEACK゙UF ;CHAFACTEF
            JMF INFLLE OSEND
            JMF INFLLE OSEND
                    \hat{y}
                    \hat{y}
                    ; GET A CHAFACTER FFOM CONSOLE EUFFEE
                    ; GET A CHAFACTER FFOM CONSOLE EUFFEE
                    ; SET CAFRY IF EMFTY
```

                    ; SET CAFRY IF EMFTY
    ```
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & \% & & & \\
\hline 58CC & E5 & \multirow[t]{9}{*}{GETCH:} & FUSH & H & ¢SAUE REGS \\
\hline 58 CLI & 2 AA 357 & & LHLII & IEUFF & \(\hat{\text { g GET FOINTER }}\) \\
\hline 5810 & 3AAS57 & & LIIA & IEUFC & - ANI COUNT \\
\hline 58013 & 11601 & & SUI & 1 & GHECR WITH CARRY \\
\hline 58115 & IIAE058 & & JC & getc4 & gNO MORE CHAF' \\
\hline 5808 & 324557 & & STA & IBUFC & ¢SAVE NEW COUNT \\
\hline 5818 & 7E & & MOV & A, M & GGET CHARACTER \\
\hline 58DC & 23 & & INX & H & ¢ INCK FOINTEF \\
\hline 5800 & \(22 A 357\) & & SHLD & IBUFF & ¢ AND SAVE \\
\hline \multirow[t]{6}{*}{\begin{tabular}{l}
58EO \\
58E1
\end{tabular}} & \multirow[t]{6}{*}{\[
\begin{aligned}
& \mathrm{E} 1 \\
& \mathrm{C} 9
\end{aligned}
\]} & \multirow[t]{2}{*}{GETCA:} & FOP & \multirow[t]{2}{*}{H} & \multirow[t]{2}{*}{¢RESTORE REGS} \\
\hline & & & RET & & \\
\hline & & \multicolumn{3}{|l|}{\multirow[b]{2}{*}{- SENI ASCII MESSAGE U}} & \\
\hline & & & & & IL RINARY ZERO \\
\hline & & \multicolumn{4}{|l|}{\(\hat{\prime}\) IS FOUND. POINTEF IS H.E} \\
\hline & & \multicolumn{4}{|l|}{¢} \\
\hline 58 E 2 & 1 A & \multirow[t]{6}{*}{SENDM:} & LINAX & 11 & g GET EYTE \\
\hline 58 ES & E7 & & OFA & A & ¢ ZERO? \\
\hline 58EA & C8 & & RZ & & ¢YES, LIONE \\
\hline 58ES & C11858 & & CALL & DUTT & وSENI IT \\
\hline \(58 E 8\) & 13 & & INX & 11 & OFOINTER \\
\hline \multirow[t]{2}{*}{\(58 E 9\)} & \multirow[t]{2}{*}{C3E258} & & JMF & SENLIM & g NEXT \\
\hline & & \multirow[t]{2}{*}{¢} & & & \\
\hline 58 CC & & & ENI & & \\
\hline
\end{tabular}

If you don't know the addresses of the console status and data registers and you are using the CP/M operating system, there is another approach you can take. You can use the I/O routines in the CP/M BIOS. The disadvantage of this approach is that \(\mathrm{CP} / \mathrm{M}\) must always be in place whenever the monitor is used. The BIOS entry address is given at memory address 1. The console status, input and output addresses are obtained by adding, respectively, 3, 6, and 9 to this address. The following I/O routines in Listing 6.1B can be substituted for the subroutines in Listing 6.1A starting with the label INPUTT and ending with the label OUT2. If this version is utilized, the addresses in the following sections will not agree with your assembly listings.
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{} & \& CONSOL & E INFUT & ROUTINE & USING CFF/M EIOS \\
\hline & & INFUTT: & & & \\
\hline 5806 & E5 & INPUT2: & FUSH & H & ¢SAUE FEGISTERS \\
\hline 5807 & D5 & & FUSH & 11 & \\
\hline 5808 & C5 & & FUSH & B & \\
\hline 5809 & 211558 & & LXI & H9INS & - RETURN ALIIRESS \\
\hline 580C & E5 & & FUSH & H & ¢FUT ON STACK \\
\hline 5801 & 2 AO 100 & & LHLII & 1 & ¢ BIOS WARM START \\
\hline 5810 & 110600 & & LXI & 11.6 & ¢OFFSET TO INFUT \\
\hline 5813 & 19 & & IIAL & II & ¢f ALM IN \\
\hline 5814 & E9 & & FCHL & & ¢CALL BIOS \\
\hline 5815 & C1 & IN5: & F'OF & \(\mathbb{E}\) & ¢RESTORE REGISTERS \\
\hline 5816 & 11 & & FOP & II & \\
\hline 5817 & E1 & & FOP & H & \\
\hline 5818 & FE18 & & CFII & CTRX & 9ABOKT? \\
\hline 581A & CA0058 & & JZ & START & ¢YES \\
\hline 5811 & c9 & & FET & & \\
\hline
\end{tabular}


Some of the constants such as PORTN will not be used at this time. However, their inclusion now will simplify things later. There are four occurrences of the dummy instruction
following the label WARM. Each is followed by an instruction that will be needed later. These latter instructions are preceded by a semicolon so that they will be treated as comments by the assembler.

There are some other matters that may need to be considered. One has to do with the sense of the input and output ready flags. There are three conditional jump instructions based on console-ready flags that display a logical 1 (active high) when ready. If your flags are inverted, that is, they present a logic zero when ready, then the three JZ commands must be changed to JNZ commands. These lines, indicated by three stars in the listing below, should be changed to
\begin{tabular}{|c|c|c|c|}
\hline \multirow[t]{2}{*}{INPUTT:} & CALL & INSTAT & gCMECK status \\
\hline & JNZ & INPUTT & \%NOT READY 脳* \\
\hline \multirow[t]{2}{*}{OUT2:} & CALL' & INSTAT & AINPUT? \\
\hline & JNZ & DUTA & 9 NO *** \\
\hline \multirow[t]{3}{*}{OUTA:} & IN** & cstat & ACHECK STATUS \\
\hline & ANI & OMSK & \\
\hline & JNZ & OUT2 & ¢NOT READY *** \\
\hline
\end{tabular}

The routine that corrects keyboard errors is programmed for a video console. If you have a console printer instead, change the backspace character to a slash.
```

BACKLUF EQU '/' ACORRECTION

```

This will print a slash when an error is corrected. Otherwise the printer will back up during error correction, overstriking the old character with the new. You may also need to add some nulls after each carriage return. The problem here will be evidenced by missing characters at the beginning of each line. The solution is to place additional instructions in the subroutine called CRLF. Replace the last statement in this routine with the following.


The rest of the program can be copied directly as it is. The abort command is a control-X. Initially, the abort address of HOME will be needed to leave the new monitor and return to your regular system. We will change this in version 3 when we will add a routine for branching to any memory address.

If you have a TRS-80 Model I, you won't have a control key. Therefore, you will have to change several of the commands shown in the listing. The original commands follow.
```

CTRH (Control-H)
TAB (Control-I)
CTKQ (Control-Q)
CTRS (Coritral-S)
CTRX (Coritrol-X)
DEL (IEL/RUB)
ESC (EscaFe)

```

After you have finished typing the program, exit from the editor and assemble the source program with the assembler. The command line might be
```

B>A:ASM MON1

```
or
```

E>A:MAC MON1

```
for the Digital Research assemblers. These two assemblers will produce two files.
```

MON1.ASM (assembly iistiris)
MON1.HEX (hem cade)

```

In addition, MAC will produce a symbol table
```

MON1.SYM (sumbol table)

```

Inspect the hex code given in the assembly listing to see that it matches the corresponding instructions given in this chapter. These 8080 listings have all been generated with the Digital Research assembler MAC. This assembler displays the hex code for 16 -bit operands in the usual reverse order. The low-order byte appears first followed by the high-order byte. Thus:
```

CN1E58 means CALL 581B and
C38458 means JMP 5884

```

By contrast, the assembly listing produced by the Microsoft assembler reverses the usual order of the two bytes. The high-order byte is given first; this is followed by the low-order byte. In this case, the listing
```

CD 581B means CALL 581E and
C3 5884 means JMF 5884

```

The next step is to load the hex program into memory using the debugger. The \(\mathrm{CP} / \mathrm{M}\) command would be
```

B`A:IDT MON1.HEX or
B.>A:SID MON1.HEX

```

Now branch to the beginning of the monitor using the debugger G command.
65800
The first thing that the monitor will do is display the version number on the first line and a prompt symbol of \(>\) underneath it.

Try out this first version by typing a series of letters and numbers. Each character that is typed should appear (echo) on the console. Try the correction keys. Typing either a control-H (backspace) or the RUB/DEL key should back up the cursor on a video terminal. Type a carriage return. The prompt symbol should appear at the beginning of the next line. If all of the features are working properly, type a control-X to return to your regular system. If something appears to be wrong, carefully compare your assembly listing with the one given in Listing 6.1A. Don't proceed to the next version until the current one is working.

\section*{VERSION 2: A MEMORY DISPLAY}

A provision for exarnining the contents of memory will now be added. This routine is called a memory dump, or dump for short; it displays the contents of memory in both hex and ASCII notation. The dump feature is initiated with a command of D followed by the address limits in hexadecimal. For example, the statement
```

\$1100 18F

```
will dump memory from address 100 to 18 F hex. The first address (100 in this case) must immediately follow the letter D. A space is typed and then the second address ( 18 F in this case) is entered. Leading zeros are unnecessary.

Each line will display 16 memory locations. The hexadecimal address of the first location will appear at the beginning of the line. Then the hexadecimal representation of the contents will follow, two characters per byte. These are arranged in four groups of four bytes. The ASCII representations of the data will be given at the end of the line if printable. Otherwise, a period is given. A dump of the first line of the monitor might look like this.
```

    2D5800 580F (your command)
    5800 C35C58C3 65S8CD16 58CA0658 DB11E67F .\X.eX.,X..X....

```

Use your system editor to make the necessary alterations and additions to version 1. First, change the version number at the beginning of the program.
```

UERS EQU '2' GUERSION NUMBER

```

Next, locate the instruction

\section*{JZ DUMF}
that follows the label WARM. Remove the semicolon at the beginning of this line. Also delete the line just before it that jumps to WARM. The region should now look like this.
\begin{tabular}{lll} 
CALL & GETCH & \\
CFI & 'LI & IDUMP? \\
JZ & DUMP & \\
\(\cdot\) & \(\bullet:\) &
\end{tabular}

The remaining instructions, shown in Listing 6.2, will be placed at the end of version 1, just preceding the END statement. It might be easier to delete the END statement, type in the new code, and then add a new END statement. The END statement is usually optional, anyway. One of the subroutines (READHL) will translate the dump limits from ASCII-encoded hexadecimal into binary. One routine gets both the start and the stop address (using READHL) then checks to see that the second address is larger than the first. If the second address is smaller than the first, then the task will be aborted. Subroutine OUTHEX will convert the binary data already in memory into ASCII-coded hex for output to the console. Subroutine TSTOP is used to determine when to terminate the dump process. Finally, an error routine (ERROR) will be needed in case an invalid character is entered by the user.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & ( RUMFF & MEMCIFY & IN HEXALIE & CIMAL AND ASCII \\
\hline & & ¢ & & & \\
\hline 58EC & C12059 & LIUMF: & CALL & RIMHLDE & \% RANGE \\
\hline 58 EF & C18359 & IUMP2: & CALL & CRHL. & GNEW LINE \\
\hline 5852 & 4E & DUMF:3: & MOU & C.M & AGET RYTE \\
\hline \(58 F 3\) & c口9359 & & CALL & OUTHX & APRINT \\
\hline \(58 F 6\) & 23 & & INX & H & APOINTER \\
\hline \(58 F 7\) & 71 & & MOV & A, L & \\
\hline \(58 \mathrm{F8}\) & EGOF & & ANI & OFH & ALINE END? \\
\hline 58FA & CA0559 & & JZ. & RUMF4 & \#YES. ASCII \\
\hline 58FD & E603 & & ANI & 3 & YSFACE \\
\hline 58 FF & CC8E59 & & CZ & OUTSF & \% 4 BYTES \\
\hline 5902 & C3F258 & & JMF & LUMF3 & SNEXT HEX \\
\hline 5905 & CLAES 5 & LUMP4: & CALL. & OUTSF & \\
\hline 5908 & LS & & FUSH & 1 l & \\
\hline 5909 & 11FOFF & & LXI & \(\mathrm{My}-10 \mathrm{H}\) & ¢RESET LINE \\
\hline 5900 & 19 & & DAII & If & \\
\hline 5901 & 11 & & POF & 0 & \\
\hline 590 E & Cu1059 & DUMFS: & CALLI. & PASCI & PASCII RUMF \\
\hline 5911 & CMA759 & & CALL & TSTOF & S DONE? \\
\hline 5914 & 711 & & MOU & Agl & iNO \\
\hline 5915 & ESOF & & ANI & OFH & 'LINE END? \\
\hline 5917 & C20E59 & & JNZ & LUMPE & \& NO \\
\hline 591A & C3EF58 & & JMP & LUMF'2 & \\
\hline
\end{tabular}


\begin{tabular}{|c|c|c|c|c|}
\hline & \% & & & \\
\hline 594723 & \multirow[t]{8}{*}{TSTOF:} & INX & H & \\
\hline 59A8 7B & & MOV & A, E & \\
\hline 594995 & & SUE & \(L\) & ; E-L \\
\hline 59AA 7A & & MOV & A 9 II & \\
\hline 59AB 9C & & SEB & H & ) II - H \\
\hline 59AC 10 & & RNC & & gNOT DONE \\
\hline 59ALI E1 & & POP & H & ¢RAISE STACK \\
\hline S9AE C9 & & RET & & \\
\hline & \% & & & \\
\hline 5981 & & END & & \\
\hline
\end{tabular}

Type up the new instructions, then, after you leave the editor, rename the new file. The CP/M command will be

REN MON2.ASM=MON1,ASM
Rename the backup file to its original name.

\section*{REN MON1.ASM=MON1.BAK}

Assemble version 2 and load it into memory. Start it up by branching to the address of START. Again, the version number should be printed, and the prompt symbol should appear. Test the new feature by dumping a portion of the monitor.
```

305800 585F

```

Be sure to type a carriage return at the end of the line. Input errors can be corrected by typing a backspace or DEL. Check to see that the hex code displayed on the screen matches the assembly listing code. Most of the ASCII representation will be meaningless. But the section from 5842 to 585A hex will read

\section*{Ver 2}

Now test the scroll-freeze commands. Dump a large section of memory.
```

200 1000

```

Type a control-S as the data are being displayed on the console. The console screen should freeze. Now type a control-Q. The screen should again resume displaying the data. The commands of Control-S and control-Q will alternately freeze and resume the scrolling.

Try the routine that checks for proper dump limits by typing a larger address first, then a smaller address.

As a result of this improper input, a question mark should be printed. Then the prompt will appear on a new line. If everything is all right, return to your regular system by entering a control-X.

If version 2 does not perform satisfactorily, compare the hex code in your assembly listing with the values given in Listing 6.2 for the new code. Correct any errors, reassemble the program, and try it again.

\section*{VERSION 3: A CALL AND GO ROUTINE}

Now that both hex-to-binary and binary-to-hex routines are available, we can easily include new features. A CALL routine and a GO routine will be added in version 3 . These routines will allow you to branch to any address in memory. The GO command will be useful for testing subroutines. For this latter command, the monitor warm-start address (WARM) is on the stack when the call is made. A subroutine can be called with the \(\mathbf{C}\) command. The execution of an RET instruction at the end of the subroutine will cause a return to the monitor.

First, change the version number to 3 . Then find the instructions corresponding to the C and G commands after the label WARM. Remove the semicolons from the beginning of the lines that branch to CALLS and GO. Delete the prior lines that jump to WARM. The program should now look like
\begin{tabular}{lll} 
CPI & 'C' & PCALLT \\
\(J Z\) & CALLS & \\
\(C P I\) & \(G G\) & BGOP \\
\(J Z\) & \(G O\) &
\end{tabular}

The remaining lines of code (and some comments) are placed at the end of the source program just prior to the END statement. They are given in Listing 6.3.
```

Listins 6.3. A CALL and a GO routine.
% ROUTINE TO GO ANYWHERE IN MEMORY
; ALIDRESS OF WARM IS ON STACK,SO A
SIMFLE FET WILL RETURN TO THIS MONITOF
\hat{p}
59AF E1 GO: FOP H FRAISE STACK
59RO CL4459 CALLS: CALL READHL FGET ALHRESS
5983 E9

```

PCHL
END

Another importart change should be made at this time. Since we can now branch to any place in memory with the GO command, we can change the abort command, control-X. Redefine HOME near the beginning of the source program so that an abort command of control-X will restart the monitor.

HOME EQU ORGIN AEORT AHMRESS
This line was originally entered as a comment. Remove the semicolon at the beginning of the line and delete the previous line.

Assemble the new version and load it into memory. Branch to the monitor and try the dump routine as before. Try the CALL feature by calling the monitor itself.
\(2 C 5800\)
The cold-start message should appear. Now use the GO routine to return to your main system. If the GO address is zero, then no argument need follow the G command.
```

\$0

```

\section*{VERSION 4: A MEMORY-LOAD ROUTINE}

In version 2 we added a routine that could be used to inspect any memory location. A routine which can be used to change memory will now be added. Change the version number to 4 . Locate the instruction
```

\& IZ LOAI

```
following WARM. Remove the semicolon at the beginning of the line. Delete the original JZ WARM on the prior line. The program should now look like
```

CPI 'L'
JZ LOAD

```

Add the load routines shown in Listing 6.4 to the end of the source program.
```

Listins 6.4. A memors-load routine.
; LOAD HEX OR ASCII CHAR INTO MEMORY
; FROM CONSOLE. CHECK TO SEE IF
乡 THE dATA ACTUALLY GOT THERE
; APOSTROFHE FRECEELIS ASCII CHAR
; CARRIAGE RETURN PASSES OUER LOCATION
;
59E4 c04459
59B7 C118659
59\&A CH11559
59EN CN8E59
59C0 4E
59C1 CH8R59
59C4 E5
59C5 CD7C58
59C8 CD4459
59CE4}4
LOAD: CALL
REAIIHL FANMRESS
LOAD2: CALL OUTHL ;FRINT IT
CALLL OUTSP
MOU C,M SORIG RYTE
CALL OUTHEX yHEX
FUSH H GSAUE FNTR
CALL INFLZ IINFUT
CALL READHL ; BYTE
MOV
E%L % TO B

```


Assemble version 4 and compare the assembly listing of the new part to Listing 6.4. Load the new program and branch to the beginning. Recheck the dump command by examining the new code for the load routine
```

2D59B4 59EB

```

Now try the load command. Great care must be taken when typing the load address. This command will actually change the contents of memory, including the monitor itself.

Type the letter \(L\), the hexadecimal address, and a carriage return. The response will be the address that was typed and the current contents of that memory location. The data are represented two ways: in ASCII and in hex. If the ASCII value is not a printable character, it is rendered as a period.

The displayed location can now be changed by typing the new value and a carriage return. The data can be entered in several ways. It can be in the form of one or two hex characters. If more than two characters are entered, only the last two are actually used. This allows you to correct an error by continuing to type. Errors can also be corrected with the backspace or the DEL/RUB key. A single ASCII character can be entered into memory by preceding it with an apostrophe.

As each new value and a carriage return is typed, the next address and the present data value will appear. In this way, a machine-language routine can be entered from the console. Of course, using an assembler is a more efficient way to generate a long program. But our load routine will be useful for making simple changes or for writing short routines.

The load command is terminated by typing a control-X (if you redefined HOME as ORGIN back in version 3). It is also terminated if you enter a nonhex character. Control then returns to the monitor. If the load command is used to revise existing code, another feature is useful. A carriage return is given without entering any data. The memory pointer then skips over the current location and the corresponding value is not changed.

After each revised byte is entered into memory, the monitor checks to see that the new value is correct. If an attempt is made to write into protected, nonexistent, or defective memory, the load process is terminated and a question mark is printed.

Try the load routine by entering the following five bytes into a convenient location such as 4000 hex.

3E \(7 \mathrm{DZ} \times \mathrm{KC9}\)
This sequence corresponds to the assembly language program
\begin{tabular}{lll}
\(3 E 07\) & MUI & Ag7 \\
13XX & OUT & \(X X\) \\
C9 & RET &
\end{tabular}

The value of XX is the console-data address (CDATA in the source program). Check the code with the dump command.

1140004004
Now use the CALL command to execute the routine
\(C 4000\)
The console bell should sound and control will return to the command level of our monitor.

\section*{VERSION 5: USEFUL ENTRY POINTS}

Changes to the first four versions were made for the most part by adding new instructions to the end of the existing program. For versions 5, 6, and 7, we are going to start the process over to some extent by inserting some new instructions in the middle of the existing program.

At the beginning of the monitor there are two jump instructions.
```

JMP COLD
JMP WARM

```

Entry points such as these are sometimes called vectors. The first jump to COLD is the initial, cold-start entry point into the monitor. Stack initialization and printing of the sign-on message occur at this time. But other
housekeeping chores, such as interface initialization, could be performed in this section. The second vector causes a jump to WARM, a restart entry point that does not alter the stack pointer.

We will now insert some additional vectors after these first two. The additional jumps will provide fixed entry points to useful subroutines in the monitor. These routines can then be easily called by other programs outside the monitor. Since these jump instructions are all at the beginning of the monitor, their addresses won't change when the monitor is altered. Furthermore, new vectors can be added to the end of the group without affecting those already present.

Place the five jump instructions shown in Listing 6.5 at the beginning of the monitor just after the first two (START and RESTRT).
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline & & \multicolumn{5}{|l|}{* UECTORS TO USEFUL ROUTINES} \\
\hline 5806 & C32A58 & COUT: & JMF & OUTT & g DUTFUT & C CHAR \\
\hline 5809 & C31558 & CIN: & JMF & INPUTT & g INPUT & CHAR \\
\hline 580 C & C30058 & INLN: & JMF & INPLN & © INPUT & LINE \\
\hline 580 F & C32559 & GCHAR: & JMF & GETCH & gGET CH & HAR \\
\hline 5812 & C3EC59 & OUTH: & \(\operatorname{JMF}\) & OUTHX & gBIN TO & HEX \\
\hline
\end{tabular}

Reassemble the monitor, load it into memory, and try the DUMP, LOAD, and GO routines again to be sure that they still work. Now, when separate, external routines are written, they need not contain subroutines for console input, output, conversion of binary to hex, and so on.

A character can be displayed on the console by calling COUT with the character in the accumulator. A single console character is obtained by calling CIN. The byte is returned in the accumulator.

An entire line of characters can be easily obtained by calling the lineinput entry INLN. As each character is typed, it is automatically printed on the console. The error-correction commands are available at this time. The backspace and DEL/RUB keys can be used to delete the previously typed character. A line is normally terminated with a carriage return. After the console-input buffer has been filled by a call to INLN, the GCHAR address can be called.

A character is returned in the accumulator for each call to GCHAR. When the input buffer has been exhausted, the carry flag is set. Typing a control- X will abort a routine and return control to the monitor. Therefore, it is not necessary to include an abort routine in separate, external programs.

The fifth new entry point will perform a conversion from binary to ASCII-coded hexadecimal. This will allow display of individual memory locations or any of the CPU registers. The byte to be converted is placed in the \(C\) register and the address of OUTH is called. The accumulator is also used by the conversion routine in this case, so it may be necessary to save the accumulator's original contents on the stack by using a PUSH instruction.

Use the monitor to write the following short routine. This program will demontrate the new vectors.
\begin{tabular}{lll}
\(3 E 07\) & MUI & Ag7 \\
\(C 30658\) & JMF & COUT
\end{tabular}

This program, which is similar to the one written in the last section, can be placed almost anywhere in memory. This time, however, there is no need to worry about the output device address since the monitor takes care of this. Branch to the routine by giving the monitor command of C and the address
```

2C4000

```

The monitor output routine will ring the console bell, then cause a return to the address WARM.

The monitor now contains a bare minimum of features. The DUMP, LOAD, GO, and CALL routines can be used to write and inspect simple routines. The several vectors located at the beginning of the monitor, allow easy access to useful subroutines within. These vectors will greatly simplify the task of writing and debugging simple routines.

At this point, you may wish to go on to Chapter 8 and try some of the routines discussed there. Otherwise, continue in this chapter as we add more features to the monitor. The new features will include memory fill and zero, memory search, ASCII load and dump, input from and output through any port, a memory test, byte replacement, and memory comparison.

\section*{VERSION 6: AUTOMATIC MEMORY SIZE}

A routine that will automatically find the top of usable memory will be added for version 6 . The routine is executed each time a cold or warm start is performed. The first byte of memory in each page of 256 bytes of memory is checked, starting with page zero. The byte in memory is moved to the accumulator, complemented, then written back to the same memory location. The result is compared to the accumulator to see if it is the same. If so, then the byte in the accumulator is complemented back to the original byte and it is written back into memory. This effectively restores the original byte.

Each page of memory is checked in this way until the monitor stack area is encountered or until defective, missing, or protected memory is found. The hexadecimal value of this top page is printed just preceding the monitor greater-than prompt ( \(>\) ). For example, if the monitor starts at 5800 hex and the stack is located at 57 A 0 , then the prompt will appear as

This routine provides a regular, continuous check on the memory size. It does not check all of the memory, but only the first byte of each 256 bytes of the page. Nevertheless, this check may point up potential problems. A more complete memory test program will be added in version 15 .


Insert the new instructions shown in Listing 6.6 right after the PUSH H instruction that follows the label WARM.
```

WARM: LXI H,WARM \&RET TO
PUSH H \hat{ HERE}
(add new code here)

```

If your assembler does not have the shift-right operation SHR, then just code the high half of the stack address. The second line in Listing 6.6 might look like this instead.
```

MUI E.57H

```

Assemble the new version. Check the assembly listing to see that the new additions are correct. Then try out version 6.

The symbol table at this point follows.
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline OOF7 & APOS & 0008 & BACKUP & 5980 & calls & 0011 & cdata \\
\hline 0011 & cdatao & 59E5 & CHEKM & 584 A & cola & 0001 & CR \\
\hline 5983 & CRHL & 5886 & CRLF & 0010 & cstat & 0010 & cstato \\
\hline 0008 & CTEH & 0011 & CTRA & 0013 & CTRS & 0018 & CTEX \\
\hline 007F & nEl. & 58EC & LIUMP & S8EF & LuMP2 & 58 F 2. & DUMP3 \\
\hline 5905 & DUMPA & 590 E & numps & 5978 & ERROR & 001 B & ESC \\
\hline 58 E 0 & GETC4 & 58CC & getch & S9AF & G0 & 599C & HEX1 \\
\hline 5938 & HHLDE & 0000 & HOME & 5745 & IBUFC & 5746 & IBUFF \\
\hline 5743 & IBUFF & OOLE & INC & 0001 & INMSK & 587 C . & INFL2 \\
\hline 5898 & INFLS & 58 CO & INFLB & 5848 & INFFLC & 5842 & INFLE \\
\hline 5884 & INPLI & 5877 & INFLN & 580 C & INFUT2 & 5806 & INPUTT \\
\hline 5816 & INSTAT & 000A & LF & 5984 & LOAII & 5987 & LOALIS \\
\hline 5910A & LOALB & 59117 & LOAIIA & 59 LE & LOAD6 & 596 B & NIB \\
\hline 0002 & OMSK & 5800 & ORGIN & 581 C & OUT2 & 582 A & OUT3 \\
\hline 5835 & OUTA & 0003 & OUTC & 5988 & OUTHEX & 5986 & OUTHL \\
\hline 5993 & OUTHX & 598A & OUTLL & 598 E & OUTSF & 581 B & OUTT \\
\hline 5928 & FASC? & 592A & PASC3 & 59110 & PASCI & 5740 & FORTN \\
\hline 5949 & RDHL 2 & 595E & RDHL 4 & 5968 & RIOHLS & 5930 & FIUHLD2 \\
\hline 592 L & ROMLDE & 5944 & READHL & 5803 & RESTRT & 00C9 & RETC \\
\hline 58 E 2 & SENLM & 5840 & SIGNON & 5740 & Stack & 5800 & START \\
\hline 0009 & TAB & 0018 & TOF & 59A7 & TSTOF- & 0031 & VEFS \\
\hline 5853 & WARM & & & & & & \\
\hline
\end{tabular}

\section*{VERSION 7: COMMAND-BRANCH TABLE}

Before incorporating additional features into the monitor, we should make a fundamental change in the command processor routine. This routine interprets the initial character of the command line. The routine looks for commands beginning with the letter D, C, G, or L. Five bytes of instruction are needed for each one of these commands. For example, the LOAD routine uses the instructions
CFI 'L'

12 LOAD

Since there are 26 letters of the alphabet, there will eventually be 26 times 5 , or 130 bytes needed if 26 different commands are incorporated. This approach is satisfactory for a short table, but there is a better approach when there are many entries.

An alternate method is to use a command branch table. This method only requires two bytes per table entry plus 23 bytes of decoding instructions. The disadvantage of this method is that all 26 table entries will have to be allocated, even if only a few are needed. Thus, there may be a lot of unallocated table entries.

Delete the 13 lines of program immediately following the command of CALL GETCH, just after the label MSIZE.


The new code that will be added is given in Listing 6．7．Notice that there are 26 table entries．Each line corresponds to one letter of the alphabet．At this time，most of the entries refer to the error routine called ERROR．This is because we have not yet incorporated many features．As new features are added to the monitor，these error references will be replaced by the desired subroutine names．
```

Listins 6.7. Command-branch table.
f MAIN COMMAND FROCESSOR
5885 11641
5887 DAL1459
588A FE1A
588C D21459
588F 87
5890 219C58
5893 1600
5895 5F
596 19
5897 5E
5898 23
589956
589A EB
589B E9
%

| SUI | ＇${ }^{\prime}$＇ | －CONUERT OFFGET |
| :---: | :---: | :---: |
| JC | ERROR | ¢＜$<$ A |
| CFI | ＇ ＇$^{\prime}$－＇$A^{\prime}+$ | 1 |
| JNC | ERROR | ；$>\mathrm{Z}$ |
| ADID | A | © DOUBLE |
| LXI | H，TABLE | ©START |
| MUI | H0\％ |  |
| MOU | EgA | G OFFSET |
| DAD | II | SARLI TO TARLE |
| MOV | EgM | ILOW EYTE |
| INX | H |  |
| MOU | H．M | ¢HIGH EYTE |
| XCHG |  | OINTO HsL |
| PCHL |  | ЯGO THERE |

5890-1459
589C D459
58A0 095A
58A2 4559
58A4 10459
58A6 [1459
58A8 085A
COMMANI TABLE
%
58AA D459
58AC D459
S8AE [459
58B0 D459
58B2 0D5A
58E4 1459
5886 [1459
5888 10459
58BA 10459
58BC D459
58BE D459
58C0 11459
58C2 D459
58C4 10459
58C6 D459
58C8 14459
58CA D459
58CC D459
TABLE:

| ERROR | ¢A， | ASCII |
| :---: | :---: | :---: |
| ERROR | \％ $\mathrm{B}^{\text {c }}$ |  |
| CALLS | ¢ C | Call subr |
| DUMP | ；Di | DUMF |
| ERROR | \％E |  |
| ERROR | 嚕， | FILL |
| G0 | \％G。 | G0 |
| ERROR | it ${ }^{\text {a }}$ | hex math |
| ERROR | 仕， | FORT INPUT |
| ERROR | －J | MEMORY TEST |
| ERROR | \％ |  |
| LOAD | iL． | load |
| ERROR | 9 m | MOVE |
| ERROR | ON |  |
| ERROR | \％0， | PORT OUTPUT |
| ERROR | \％ F |  |
| ERROR | ¢0 |  |
| ERROR | 限， | REFLACE |
| ERROR | ¢S． | SEARCH |
| ERROR | ¢T |  |
| ERROR | －U |  |
| ERROR | iv， | UERIFY MEM |
| ERROR | iw |  |
| ERROR | ； X ， | Stack Pointer |
| ERROR | \％Y |  |
| ERROR | ； 2 ， | ZERO |

```

Generate the new version, assemble it, and compare the resulting assembly listing to the one given in Listing 6.7. Try out version 7. It should behave exactly like version 6 . It will be a bit longer than version 6 at this stage, but it will not grow as rapidly as we add new features. In the remainder of this chapter, we will add the new subroutines to the end of source program. The label for the subroutine will be placed in the appropriate place of the command branch table.

\section*{VERSION 8: DISPLAY THE STACK POINTER}

By adding seven bytes of new code, we will be able to examine our monitor's stack pointer. This will alert us to a possible problem with the monitor itself. We may find, for example, that as we use the monitor, the stack tends to grow up or down in memory, rather than remain in the same place. This is undesirable and indicates that we are not properly lowering or raising the stack somewhere in the program. For example, subroutine TSTOP increments the pointer then checks to see if the current task should be terminated. If so, the stack is raised with a POP instruction. Then a return instruction skips one level of subroutines, so that control returns to the address of WARM.

Change the version number to 8 . Also change the entry in the command table that corresponds to the command of X . This is the third from the last entry. Delete the word ERROR and replace it with the word REGS.

DW REGS \(\quad X\), STK POINTER
Then go to the end of the source program. We will make a minor change in subroutine CHECKM, the last subroutine in the monitor. Then the new instructions will be added. Delete the END statement and the instruction just prior to the END statement.

JMP ERROR GBAD
Then add the new instructions as shown in Listing 6.8.


Reassemble the monitor and try it out. First give the X command (with no argument). Make a note of the value given for the stack pointer. Now, try other monitor features such as the dump and load commands. After each of these commands, give the X command to see that the stack pointer remains in the same place.

Try the separate routine that rings the console bell. This routine, which was written for version 4 , may have to be rewritten if it was destroyed by the assembler or the editor. Again, check that the stack pointer is still in the same place. When you are convinced that everything is all right, continue to the next version.

\section*{VERSION 9: ZERO AND FILL ROUTINES}

In version 4, we added a routine that could be used to change individual memory locations, one at a time. We will now add a routine which will allow us to fill a portion of memory with a constant value. A separate command for zeroing memory is also added for convenience, even though this operation could be performed with the FILL command.

Change the version number to 9 , then alter the two command table entries that correspond to the F (fill) and Z (zero) commands.
\begin{tabular}{|c|c|c|}
\hline nW & FILL & QF. MEMORY \\
\hline nw & ZERO & \%Z. MEMORY \\
\hline
\end{tabular}

Add the new code shown in Listing 6.9 to the end of the program.



Assemble the program, load it into memory, and try it out. First, display a portion of memory.
```

>D4OOO 4OAF

```

Then, zero out a part of this region.
```

>24000 403F

```

Display the region again to be sure that the zero routine is working. Now fill a portion of the previously zeroed memory with A5 hex bytes.
```

>F4001 401E A5

```

Again, dump this region of memory to ensure that the fill routine is working.
```

>D4000 404F

```

Finally, check the ASCII fill command by filling with a \(\$\) symbol.
```

>F4020 402F '\$

```

As with the load command, ASCII input is preceded by an apostrophe.

\section*{VERSION 10: A BLOCK-MOVE ROUTINE}

The next routine to be added will allow us to move a block data from one memory location to another. This is actually a duplication routine, since the original memory block will remain unchanged. As each byte is moved to the new location, a check is made to ensure that it actually got there.

First, change the version number to 10 . Then add the new lines to the end of the source program. Change the branch table entry corresponding to the command of M.
```

DW MOVE iM, MEMORY

```

Insert the instructions given in Listing 6.10 to the end of the source program. Assemble the monitor and try it out.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & : MDUE & A BLOCK & OF MEMORY & H:L-D,E TO B,C \\
\hline 5493 & CD7C5A & MOUE: & CALL & HLDEBC & -3 ADMR \\
\hline 5496 & CMA05A & MOUDN: & CALL & MOVIN & GMOVE/CHECK \\
\hline 5 A99 & cdoosa & & CALL & TSTOF & S MONE? \\
\hline 5A9C & 03 & & INX & \(\mathbb{B}\) & iNO \\
\hline 5A9D & C3965A & & JMF' & MOUMN & \\
\hline & & \(\stackrel{\text { ¢ }}{ }\) & & & \\
\hline 5AAO & 7E & MOUIN: & MOU & AgM & ¢EYTE \\
\hline \(5 A A 1\) & 02 & & STAX & B & SNEW LOCATION \\
\hline \(5 A A 2\) & OA & & LDAX & B & ACHECK \\
\hline SAA3 & BE & & CMP & M & gIS IT THERE? \\
\hline 5AA4 & C8 & & RZ & & GYES \\
\hline 5AA5 & 60 & & MOV & HeB & OERROR \\
\hline SAAG & 69 & & MOV & L, C & gINTO HOL \\
\hline 5 5A7 & C3425A & & MPP & ERRF & SSHOW BAL \\
\hline
\end{tabular}

The move command requires three addresses. These are the start and stop address of the source block and the start address of the destination block. For example,
\(3 M 5800\) 58FF 4000
will move the first page of the monitor ( 5800 to 58 FF hex) down to the address range 4000 to 40 FF hex.

The move routine is designed to move data downward. Thus the first byte of a block can be deleted by moving the remainder of the program downward by one byte. The command
>M103 1000100
moves the memory block in the address range 103 through 1000 down three bytes to the memory range 100 through FFD hex. On the other hand, a block move in the upward direction must be done carefully.

If the new block does not overlap the old, then there is no problem. But if there is an overlap, then the upward move will destroy some of the data. One possible solution to this problem is to first move the block downward until it is clear of the new upper block. Then move the block up to the desired location. Another possibility is to move the upper half of the block first, then move the lower half.

The best solution is to have a more sophisticated move routine. This routine should first determine whether the move is to be upward or downward. If the movement is downward, then the move commences with the lower part of the block (as with the present program). But if the move is upward, then it should begin with the upper end of the block. The memory pointers should now move downward in memory. With this approach, the original data will be unaltered. This additional feature is more easily coded with the Z-80 block-move routines than with the 8080 instructions.

We have not incorporated the upward-move feature at this time. In developing a system monitor, there must be a tradeoff between features and space. A minimum of idiot-proofing is necessary. But, if we want to have a monitor that will fit into 1 K bytes of ROM , we will have to make some compromises.

Notice that this move routine moves a byte from the source location into the destination location. It then reads the byte back from the new location to see that it actually got there. If an attempt is made to move data into read-only memory, protected memory, or defective memory, the process will be terminated. The address of the location will be printed following the letter B (for "bad").

If we want to retain this memory-checking feature, we will not be able to use the \(\mathrm{Z}-80\) block-move routines. The problem is that the \(\mathrm{Z}-80\) routines perform an automatic pointer increment after each byte is moved. If a memory check is desired, then the destination pointer will have to be backed up after each byte is moved. This will allow the newly moved byte to be checked. Finally, the pointer will have to be incremented again.

\section*{VERSION 11: A SEARCH ROUTINE}

Sometimes it is necessary to find a particular data byte or address in memory. Or perhaps all occurrences of a data byte or an address within a memory block are needed. For version 11, we will add a hex search routine. Change the version number and the branch table entry for the letter S.

DW SEARCH 今S, MEMORY
Add the new instructions as given in Listing 6.11.

\begin{tabular}{|c|c|c|c|c|c|}
\hline 5AAF & DAB85A & \multirow{12}{*}{SEAR3:} & JC & SEAR3 & \% ONLY ONE \\
\hline \(5 A B 2\) & E5 & & PUSH & H & \\
\hline 5 AB 3 & ca9059 & & CALL & FEALIML & OND BYTE \\
\hline 5AB6 & 45 & & MOV & R\%L & SINTO C \\
\hline 5 AB 7 & E1 & & FOF & H & \\
\hline 5 AB8 & 7E & & MOV & A, M & gGET BYTE \\
\hline 5 AB9 & H9 & & CMF & C & ¢ MATCH? \\
\hline 5ABA & C2CF5A & & JNZ & SEAF4 & ONO \\
\hline 5 ABD & 23 & & INX & H & © YES \\
\hline 5ABE & 78 & & MOV & A) \({ }^{\text {P }}\) & ¢ONLY 1? \\
\hline 5 ABF & FEOD & & CFI & CF & \\
\hline \multirow[t]{3}{*}{5 AC 1} & \multirow[t]{3}{*}{CAC95A} & & JZ & SEAR S & iYES \\
\hline & & \% & & & \\
\hline & & ; FOUNA \% & FIRST & MATCH, CH & CK FOR SECONI \\
\hline 5AC4 & 7E & & MOV & A, M & ENEXT EYTE \\
\hline \(5 A C 5\) & - 88 & & CMF & \(\underline{B}\) & ¢MATCH? \\
\hline \multirow[t]{2}{*}{5 SAC 6} & C2CF5A & & JNZ & SEAR4 & ONO \\
\hline & & \(\hat{\theta}\) & & & \\
\hline 5 AC9 & 2B & SEAR5: & ncx & H & §A MATCH \\
\hline 5ACA & C5 & & PUSH & E & \\
\hline SACB & concs & & CALL & CRHL & SSHOW AHLK \\
\hline 5 SCE & Cl & & FOFP & B & \\
\hline 5 ACF & CD005A & SEAR4: & CALL & TSTOF & STONE? \\
\hline 5 A02 & C3B85A & & JMF' & SEAR3 & SNO \\
\hline
\end{tabular}

Our new feature will display the address of every occurrence of one or two chosen bytes. For example, the command
```

>S100 4FF OII

```
will print the address of each occurrence of a carriage return (OD hex) over the memory block 100 to 4 FF hex. The alternate command
```

>SO FFFF 3E 10

```
includes two search bytes. This command will look for the byte 3 E followed by the byte 10 over the entire 64 K -byte memory range. These two bytes might represent the 8080 instruction MVI A,10 or perhaps the address 103E hex.

Notice that if two search bytes are given in the command, they must be separated by a space. If the command is incorrectly given without the space between the bytes, the search will only include the second byte. For example, the command
```

>50 FFFF 3E10

```
will be interpreted as a search for the byte 10 hex . This occurs because only the last two characters of the field are used.

\section*{VERSION 12: ASCII LOAD, SEARCH, AND DISPLAY}

At this time, the monitor is hex oriented, but it is capable of limited ASCII operations. For example, the DUMP routine gives both the hex and the ASCII representation of the data. The load and fill commands will accept ASCII characters when preceded by an apostrophe. In version 12 , we will add three new ASCII commands: ASCII load, ASCII dump, and ASCII search. A continuous series of ASCII characters (a string), including a carriage return, line feed, tab, and so on, can be entered directly into memory. A straight ASCII dump will render an ASCII portion of memory in its natural form. And we will be able to search the memory for one or two ASCII characters. If the command line begins with the letter A, a branch will occur to a second command processor. The letter following the A will cause a jump to the desired task of dump, load, or search.

Change the version number to 12 and the command table entry for the letter A.

DW ASCII AA IUUMP: LOAD
Type the code from Listing 6.12; assemble the new version and start it up.
Listins 6.12. ASCII loady searchy and display.
\begin{tabular}{|c|c|}
\hline SADS & cid2559 \\
\hline SAD8 & FE44 \\
\hline SADA & CA045B \\
\hline SADD & FES3 \\
\hline 5ADF & CA2CSE \\
\hline \(5 A E 2\) & FE4C \\
\hline 5 SEA & C210459 \\
\hline
\end{tabular}
5 SE 7 CO9D59
SAEA CDMF59
SAEN CD1558
5AFO CR2A58
SAF3 47
SAFA CDBESA
5AF7 23
\(5 A F 8710\)
5AF9 E67F
\(5 A F B\) C2ED5A
5AFE CROCSO
SEO1 C3EDSA
```

\& ASCII SUE-COMMANIN FRDCESSOR

```
& ASCII SUE-COMMANIN FRDCESSOR
g
g
ASCII: CALL GETCH #NEXT CHAR
ASCII: CALL GETCH #NEXT CHAR
    CPI 'I'' #DISPLAY
    CPI 'I'' #DISPLAY
            JZ ALIUMF 'S' OSEARCH
            JZ ALIUMF 'S' OSEARCH
            CFI ASCS OSEARCH
            CFI ASCS OSEARCH
            CFI 'L' 
            CFI 'L' 
            JNZ ERROR
            JNZ ERROR
#
#
# JNZ ERROR 
# JNZ ERROR 
# JNZ ERROR 
# JNZ ERROR 
;
;
#PRINT IT
#PRINT IT
ALOD2: CALL INFUTT #NEXT CHAR
ALOD2: CALL INFUTT #NEXT CHAR
CALL OUTT OFRINT IT
CALL OUTT OFRINT IT
MOU E,A क्SAVE
MOU E,A क्SAVE
CALL CHEKM SINTO MEMORY
CALL CHEKM SINTO MEMORY
INX H OPOINTER
INX H OPOINTER
MOV AgL FIN
MOV AgL FIN
ANI 7FH FLINE END?
ANI 7FH FLINE END?
JNZ ALOH2 iNO
JNZ ALOH2 iNO
CALLL CFHL ONEWLINE
CALLL CFHL ONEWLINE
f
f
# MISPLAY MEMORY IN STRAIGHT ASCII.
# MISPLAY MEMORY IN STRAIGHT ASCII.
; KEEF CARRIAGE RETURN, LINE FEED, CHANGE
; KEEF CARRIAGE RETURN, LINE FEED, CHANGE
% TAB TO SFACE, REMOVE OTHER CONTROL CHAR.
% TAB TO SFACE, REMOVE OTHER CONTROL CHAR.
\hat{g}
```

\hat{g}

```
\begin{tabular}{|c|c|c|c|c|c|}
\hline 5B04 & cn8659 & ADUMF： & CALL & RDHLIDE & QRANGE \\
\hline 5B07 & 7E & \multirow[t]{12}{*}{ALMFE：} & MOV & A PM & PGET BYTE \\
\hline 5808 & FETF & & CFI & DEL & OHIGH BIT ON？ \\
\hline SBOA & 12265B & & JNC & ALIMF4 & ¢ YES \\
\hline 5 EOLI & FE20 & & CFI & ， & ©CONTROL？ \\
\hline 5 BOF & D2235B & & JNC & ALIMP3 & \＄NO \\
\hline 5 B 12 & FEOD & & CFI & CR & ACARR RET？ \\
\hline 5814 & CA235B & & JZ & ALIMP3 & ¢YES \({ }^{\text {O }}\) OK \\
\hline 5 SH 17 & FEOA & & CFI & LF & PLINE FEEL？ \\
\hline 5819 & CA235B & & \(\checkmark \mathrm{L}\) & ALMPP3 & ¢YES．OK \\
\hline \(5 \mathrm{B1C}\) & FE09 & & CPI & TAE & \\
\hline 5B1E & C22658 & & JNZ & ALMP4 4 & OSK゙IP OTHER \\
\hline 5821 & 3E20 & & MUI & \(A^{\prime \prime}\) & OSFACE FOR TAR \\
\hline 5823 & C口2A58 & Almap3： & CALL & OUTT & ¢SENH \\
\hline 5826 & C1005A & ALIMF4： & CALL & TSTOF & PDONE？ \\
\hline \multirow[t]{4}{*}{5829} & \multirow[t]{4}{*}{C3075B} & & JMP & ALIMP2 & ¢NO \\
\hline & & \multicolumn{4}{|l|}{\multirow[t]{3}{*}{\begin{tabular}{l}
－SEARCH FOR 1 OR 2 ASCII CHARACTERS \\
－NO SPACE BETWEEN ASCII CHARS \\
；FORMAT：START STOF 1 OR 2 ASCII CHAR
\end{tabular}}} \\
\hline & & & & & \\
\hline & & & & & \\
\hline 582C & C18659 & ASCS： & CALL & FDMLIME & SRANGE \\
\hline 5B2F & ca2559 & & CALL & GETCH & ЯFIEST CHAR \\
\hline 5832 & 4F & & MOU & C．A & \\
\hline 5833 & cロ2559 & & CALL & GETCH & Q 2ND DR CARR FET \\
\hline 5836 & DAADSA & & JC & SEAR2 & pONLY DNE CHAR \\
\hline 5839 & 47 & & MOV & BgA & ¢ 2NI \\
\hline 5B3A & C3E85A & & JMP & SEAR3 & \\
\hline
\end{tabular}

Dump a section of memory with the regular hex dump command．Then enter a line of ASCII characters using the new ASCII load command．
```

>AL4000 <carriase returri
4000 This is a test of the new <cr><<l>
ASCII load routine. <cr><<lP>

```

All of these characters will be deposited directly into memory，including the carriage returns and line feeds．Type a control－X to abort the task．Inspect the new addition first with the hex dump
```

>14000 404F

```
then inspect it with the new ASCII dump：

\section*{\(>A D 4000\) 404F}

Notice the difference．The ASCII dump renders the data as it was originally typed．

A carriage－return line－feed pair will cause a real carriage－return line－feed pair to be sent to the console．Tab characters are not expanded but are ren－ dered as blanks（in line with our goal of reducing the monitor size）．All other control characters are ignored．

\section*{VERSION 13: INPUT AND OUTPUT TO ANY PORT}

The load routines added in versions 4 and 12 allow us to change individual memory locations. And the dump routines added in versions 2 and 12 allow us to inspect individual memory locations. For version 13 , we will add a routine to read any I/O port and another to send a byte to any I/O port. This feature will allow us to initialize and test I/O ports.

The 8080 and Z-80 microprocessors can address 256 separate, 8-bit input/output ports. These ports are used for communicating with the console, list, and tape devices. In addition, if there is a front panel, the switches are usually assigned to a separate data port. Also, some disk-controller boards use several I/O ports for communication with the CPU.

It is more difficult to implement these I/O features on an 8080 CPU than on a Z-80. The reason is that the 8080 I/O instructions require the port address to be placed in memory immediately following the IN or OUT command
\begin{tabular}{llll}
\(D B\) & 10 & \(I N\) & \(10 H\) \\
103 & 11 & \(O U T\) & \(11 H\)
\end{tabular}

By comparison, the Z-80 can execute I/O instructions with the device address located in the C register. Nevertheless, we will implement the input and output instructions, at this time, using only 8080 code.

The plan is to write the IN or OUT instruction in memory, write the port number in the next byte, then write a RET instruction in the third position. A call to the address of PORTN will then produce the desired effect. The routine that writes these bytes in the stack area is called PUTIO. Since we are developing a monitor that can be placed in ROM, we will have to perform the actual I/O instructions outside of the regular monitor code area. Three bytes of memory just above the stack were previously set aside for this purpose. They start with the address PORTN.

A fourth routine is also needed. Subroutine BITS is used to convert the binary data read from the selected port into ASCII-coded binary characters. An IN command then prints on the console the port data in both hex and binary. For example, the command

SIFF
will give the front-panel switch setting in both hex and binary notation.

F8 11110000
The BITS routine can be coded more efficiently if a Z-80 CPU is available. This is because the Z-80 can shift data in the general-purpose registers, as well as in the accumulator. This is discussed in Chapter 7.

Change the version number to 13 and alter the branch table entries for the letters I and O.
\begin{tabular}{lll} 
DW & IPORT & II PORT INFUT \\
DW
\end{tabular}

Add the new routines to the end of the source code. Assemble version 13 and try it out.
```

Listins 6.13. Input and output to ans port.

```








```

    * FRINT L FEGISTER IN EINARY (808O UER)
    % FRINT L REGISTER IN GINARY (8OBO UER)
    \hat{9}
    5B4A 0608 BITS: MUI B,8 %8 EITS
l
l
l
l
l
l
l
l
l

```





```

    BIT2: MOU A,L
    ADI A 戶SHIFT LEFT
    MOU L.A
    MUI A,'O'/2 \hat{HALF OF O}
    ADC A {HOUBLE+CARRY
    CALL OUTT &FFINT BIT
        HICR B
        JNZ EITS ;8 TIMES
    RET
    \hat{0}
    ; OUTFUT EYTE FROM PORT (8O8O UERSION)
    ; FORMAT IS: O,FORT,BYTE
    5B5A CN91159
OFORT: CALL REALHL FFORT
SESD 4D
5B5D 4D
5B61 3ED3
OFORT: CALLL REALHL FFORT
CALL READHL. \#DATA
MUI A,OUTC SOUT OFCOLE

* EMULATE Z8O INP AND OUTF FOR }808
5R63 32AO57 FUTIO: STA FORTN FIN OR OUT COLIE
5B66 79
5B67 32A157
MOU ADC FFORT NUMEER
STA POFTNH1
5B6A 3EC9

```

```

5B6C 32A257
STA FORTN+2
5B6F7D
MOU
A\rhoL. कOUTPUT BYTE
5H7O C3AO57
JMF
PORTN GEXECUTE

```

If you have a set of front panel switches, give the command
```

>IFF

```
and see if the bit pattern matches the actual switch setting. Next, try to ring your console bell by sending a binary 7 .

\section*{20117}

The value of 11 should be changed to your console data port address if it is different.

Modern serial and parallel ports need to be initialized before use. These initialization routines could be placed in the monitor cold-start routines. Initialization can also be performed with the new monitor output command. A Motorola 6850 serial port can be initialized for one stop bit with the two commands
```

>010 3 <reset>
>010 15 <met>

```
where 10 is the address of the status/control port.

\section*{VERSION 14: HEXADECIMAL ARITHMETIC}

A routine for obtaining the sum and difference of two hexadecimal numbers will now be added. Change the version number to 14 . Change the branch table corresponding to the entry H .
```

IW HMATH :H, HEX MATH

```

Place the remaining new lines at the end as usual.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & HEXAI & ECIMAL & MATH, SUM & AND MIFFERENCE \\
\hline 5873 & cr9159 & HMATH: & CALL & HHL IIE & \$TWO NUMEERS \\
\hline 5876 & ES & & PUSH & H & ¢SAUE HiL \\
\hline 5877 & 19 & & DAII & D & © SUM \\
\hline 5878 & CuIDF59 & & CALL & OUTHL & ¢FRINT IT \\
\hline 587B & E1 & & POF & H & \\
\hline 5B7C & 711 & & MOV & Agl & \\
\hline 58711 & 93 & & SUE & E & ; LOW BYTES \\
\hline 5B7E & 6F & & MOU & \(L, A\) & \\
\hline SE7F & 7C & & MOU & A, H & \\
\hline \(5 \mathrm{B8O}\) & 9A & & SBE & D & \\
\hline 5881 & 67 & & MOV & H, A & FHIGH BYTES \\
\hline 5882 & C31.1559 & & JMP & QUTHL & gnIFFERENCE \\
\hline
\end{tabular}

The new feature is executed by typing the letter H and the hex numbers. The response is the sum and the difference.
```

>H8000 4000
C000 4000

```

\section*{VERSION 15: MEMORY-TEST PROGRAM}

Back in version 6, we installed an automatic memory-size routine. This addition performs a memory check of sorts by testing the first byte of each page. In version 15 , we will add a more complete memory-test program. Change the version number and the branch table entry for the letter J (justification):
```

DW JUST iJ. MEMORY TEST

```

Then, type in the new lines as shown in Listing 6.15.


Assemble the program, load it into memory, and try it out. The memory range from zero to 58 FF hex is tested with the command

3105800
This is a continuing test. The given range is tested over and over until aborted with a control-X command. This memory-test program is not very sophisticated. The routine will not find unusual problems in flakey, dynamic memories. It will, however, locate those regions with no memory, protected memory, and grossly defective memory. The address of each bad location is printed in hex, then the bit pattern follows. ASCII ones are shown for the bad bits and ASCII zeros are given for the good bits.

The test program gets the original memory byte, complements it, and puts it back. It then complements it a second time and restores the original byte. Thus, the original memory is left intact. The only caution here is that the stack area should not be tested.

Much more sophisticated memory test programs are needed for difficult memory errors. Of course, such programs will require a lot of memory, and so would not fit into a compact system monitor. One feature of such a program is to provide a delay between the time the test byte is placed into memory and the time that the byte is checked. One disadvantage of a more powerful memory-test program is that it does not protect the original memory contents.

\section*{VERSION 16: REPLACE ONE BYTE WITH ANOTHER}

In version 11 we added a memory-search routine. This feature gives us the ability to find every occurrence of a particular byte. A companion feature added in version 16 allows us to change every occurrence of a particular byte to a different byte. Change the version number and the branch table corresponding to the letter R.
```

DN REPL कR, REPLACE

```

Add the new lines shown in listing 6.16 to the end of the program.
```

Listins b.16. Replace one hex bste with another.
REPLACE HEX GYTE WITH ANOTHER
OUER GIUEN RANGE
FOFMAT IS: START, STOF: ORIG, NEW
و
5BR4 CR7C5A REFL: CALL HLDEEC FRANGE, 1ST EYTE
5BE7 LIALI459
5BRA 41
SBBE ES
JC ERROR gNO SNI
ME ERROR SNO SNR

```
\begin{tabular}{|c|c|c|c|c|c|}
\hline 5 EBC & cı9159 & & CALL & READHL. & \% 2NI BYTE \\
\hline 5 BEF & 411 & & MOV & C. L & ¢INTO C \\
\hline 5 BCO & E1 & & POF & H & \\
\hline 5 EC 1 & 7E & REFL2: & MOV & A M M & ¢FETCH BYTE \\
\hline 5 BC 2 & B8 & & CMF & E & ЯA MATCH? \\
\hline 5 BC 3 & c2ccsa & & JNZ & REPL3 & ¢NO \\
\hline \(58 C 6\) & 71 & & MOV & \(\mathrm{M}, \mathrm{C}\) & QSUBSTITUTE \\
\hline 5 EC 7 & 79 & & MOV & A 9 C & \\
\hline \(5 \mathrm{BC8}\) & BE & & CMF' & M & S SAME? \\
\hline 5 BC 9 & C2435A & & JNZ & EFFEB & ¢NO. BALI \\
\hline 5 BCC & CLOOSA & FEFPL3: & CALL & TSTOP & GHONE? \\
\hline 5 BCF & C3C15B & & JMF' & FEFPL & \\
\hline
\end{tabular}

Assemble version 16 and try it out. Move three lines of the monitor's code to a lower place using the M command.
\(3 M 5800\) 582F 4000
Dump these three lines of memory with the D command.
```

>104000 402F

```

Change every occurrence of the byte C3 found in those lines to a 40 hex using the command
```

>R4000 402F C3 40

```

Notice that a space must separate the two bytes C3 and 40 . Now, dump this portion of memory with the command
```

>\$4000 402F

```

The new byte is an ASCII "at" sign (@), therefore it will show up clearly on the ASCII portion of the dump.

The replace routine can be useful for relocating a short executable program. Suppose that a routine is programmed for execution at 3000 hex. It can be moved to 4000 hex with the block-move command
```

2M3000 3FFF 4000

```

However, the program will not run at the new location if there are absolute jumps present. The high byte of each jump address will have to be changed from 30 to 40 in this case. The search routine can be used to find all occurrences of 30 hex in the program.
```

>54000 4FFF 30

```

Then the replace command can be given to convert each 30 hex into a 40 hex.

Another use for the replace command is to convert an assembly language source file from one format to another. For example, the CP/M format requires a line feed to follow a carriage return. But another assembler may generate lines in which only the carriage return is placed at the end of each line. In this case, the original file can be loaded into memory. Then, all of the carriage returns (OD hex) can be replaced with an ASCII character such as a \# symbol (23 hex).
```

\$R100 38FF OD 23

```

After the file is altered with the monitor, it can be saved on a disk. The final step can be performed with the system editor. The global replace command of this editor can be used to replace every occurrence of the \# sign with a carriage-return/line-feed pair. With the Word-Master editor, the command would be

\section*{}

The first step required the monitor because the system editors cannot be directed to globally change a carriage return to something else. The carriage-return/line-feed pair must be treated as a unit.

\section*{VERSION 17: COMPARE TWO BLOCKS OF MEMORY}

This last addition to our system monitor will fill out the size to just under 1 K bytes. The new routine will allow us to compare two blocks of memory. If discrepancies are found, the address and the contents of the appropriate location in both blocks will be shown. Change the version number and the branch table corresponding to the letter \(R\).
```

DW VERM \hat{V}

```

Add the new lines shown in Listing 6.17.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & \multicolumn{4}{|l|}{```
& GIUE RANGE OF 1ST BLOCK
; ANII START OF SECOND
#
```} \\
\hline \(5 \mathrm{BD2}\) & CD7C5A & UERM: & CALL & HLIMEBC & ¢ 3 ALIMRESSES \\
\hline SEDS & \(O A\) & UERM2: & LIIAX & B & ¢FETCH BYTE \\
\hline 58106 & BE & & CMF & M & ¢SAME AS DTHER? \\
\hline 5807 & CAF358 & & JZ & UERM3 & ¢YES \\
\hline 5 BLAA & ES & & FUSH & H & GMIFFERENT \\
\hline SEDE & C5 & & PUSH & E & \\
\hline 58 nc & cunc59 & & CALL & CRHL & FPRINT 1ST FOINTER \\
\hline 58 DF & 4E & & MOU & C,M & ¢FIRST EYTE \\
\hline 5 EEO & CIE459 & & CALL & OUTHEX & FPRINT IT \\
\hline 5 EE 3 & 3E3A & & MUI & Ag':' & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline 5BES & C12A58 \\
\hline SEE8 & E1 \\
\hline 58E9 & CanF59 \\
\hline 5BEC & 4E \\
\hline 5BED & CDEC59 \\
\hline 5BFO & 4D \\
\hline 5 BF 1 & 44 \\
\hline 5 BF 2 & E1 \\
\hline 5 SF 3 & CD005A \\
\hline 5BF6 & 03 \\
\hline 5 BF 7 & C3D558 \\
\hline
\end{tabular}
\begin{tabular}{ll} 
CALL & OUTT \\
FOF & H \\
CALL & OUTHL \\
MOU & CYM \\
CALL & OUTHX \\
MOU & C,L \\
MOU & BوH \\
FOF & H \\
CALL & TSTOP \\
INX & B \\
IMP & UERM2
\end{tabular}

\author{
AB, C TO HoL \\ GSECOND POINTER \\ و 2 NH EYTE \\ IPRINT IT \\ 今RESTORE C \\ 今, ANM B \\ PAND HOL - LODNE? \\ ©2NI FOINTER
}

The symbol table should now look like this.
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline 5807 & ALIMP2 & 5 B 23 & ADMF3 & 5826 & ALmp4 & 5804 & ARUMP \\
\hline SAED & ALOD2 & OOF7 & AFOS & 5 Alis & Ascil & 582C & ASCS \\
\hline 0008 & backup & \(5 \mathrm{B4C}\) & EIT2 & SB4A & BITS & 5 S09 & CALLS \\
\hline 0011 & cdata & 0011 & cdatao & 5 Sa E & CHEKM & 5809 & C.IN \\
\hline 5858 & colir & 5806 & COUT & 000] & CR & 59 DC & CRHL \\
\hline 590 F & CRLF & 0010 & cstat & 0010 & cstato & 0008 & CTRH \\
\hline 0011 & CTRQ & 0013 & CTRS & 0018 & CTRX & 007 F & DEL \\
\hline 5945 & nump & 5948 & DUMP2 & 594 B & nump3 & 595 E & DUMP4 \\
\hline 5967 & DUMF5 & 5 S45 & ERR2 & 5 S43 & ERRE & 59104 & ERROR \\
\hline 5 A42 & ERRF & 0018 & ESC & 5 S5D & FILL & 5466 & FILL2 \\
\hline 5A6C & FILL3 & 5A75 & FILL4 & 580F & gChar & 5939 & GETC4 \\
\hline 5925 & GETCH & 5 S08 & G0 & 5975 & HEX1 & 5991 & HHLIDE \\
\hline 5A7C & HLIEEBC & 5ABA & HLDECK & 5 E 73 & HMATH & 57 A5 & IBUFC \\
\hline 57A6 & IEUFF & 57A3 & IBUFF & OODE & INC & 580C & INLN \\
\hline 0001 & INMSK & 5805 & INPL2 & 58 F 1 & INPL3 & 5919 & INPLE \\
\hline 5901 & INFLC & 58 FE & INFLE & 58 nL & INFLI & 5800 & INPLN \\
\hline 581 E & INPUT2 & 5815 & INFUTT & 5825 & INSTAT & 5830 & IPORT \\
\hline 5BAS & JERR & 5885 & Just & 5889 & JUST2 & 5892 & Just3 \\
\hline OOOA & LF. & 5AOD & LOAD & 5A10 & Load2 & 5 A33 & loaliz \\
\hline 5A30 & Loalia & 54.37 & Loadi & 5 A96 & Mound & 5 A93 & move \\
\hline 5AAO & MOUIN & 5878 & msize & 59C4 & NIR & 586A & NFAGE \\
\hline 0002 & OMSK & 5E5A & OPORT & 5800 & ORGIN & 582 B & OUT2 \\
\hline 5839 & 0UT3 & 5844 & OUT4 & 0003 & OUTC & 5812 & OUTH \\
\hline 59E4 & OUTHEX & 590F & OUTHL & 59EC & OUTHX & \(59 E 3\) & OUTLL \\
\hline \(59 E 7\) & outsf & 582A & OUTT & 5981 & FASC2 & 5983 & FASC3 \\
\hline 5976 & PASCI & 57AO & FORTN & 5863 & futio & 59A2 & RIDHL 2 \\
\hline 5987 & RLIHL4 & 59 Cl & RDHLS & 5989 & RDHLI2 & 5986 & RDHLDE \\
\hline 5991 & REEADHL & 5A4E & REGS & \(5 \mathrm{EB4} 4\) & REFL & 5 BC 1 & REFL2 \\
\hline 5 BCC & REFL 3 & 5803 & RESTRT & 00c9 & RETC & 5AAD & SEAR2 \\
\hline \(5 A B 8\) & SEAR3 & SACF & SEAR4 & 5AC9 & SEARS & \(5 A A A\) & SEARCH \\
\hline 593 B & SENDM & 584 F & SIGNON & 57A0 & STACK & 5800 & Start \\
\hline 0009 & tab & 589 C & table & 0018 & TOF & 5 A 00 & TSTOP \\
\hline \(5 \mathrm{BL2}\) & UERM & 58 SD & VERM2 & 5BF3 & VERM3 & 3731 & VERS \\
\hline 5861 & WARM & 5 A55 & zero & & & & \\
\hline
\end{tabular}

Try the new addition by first moving a copy of the monitor down to a lower memory location.
```

\M5800 5BFF 4800

```

Then verify that the two copies are the same.
```

>V5800 5BFF 4800

```

Of course this step is not necessary, since there is a verification step included in the block-move routine. Change one byte in the new location so that there will be a difference.
```

>L4820
4820 - XX 0 <zero location 4820%
. . . Ax <quit>

```

Then, give the verification command again.
```

>V5800 5BFF 4800

```

Because you changed one byte of the copy, there should be an indication of error.

This compare routine completes the 1K 8080 system monitor. We have incorporated many useful features into a minimum of space. We have carefully distinguished program code from data code so that the monitor can be placed into ROM or PROM.

\section*{AUTOMATIC EXECU'IION OF THE MONITOR}

If you program the monitor into ROM, it will be ready to use each time the computer is turned on. On the other hand, you may want to copy it from disk into memory each time it is needed. We have been loading the monitor with the system debugger each time it is needed. But it is easier to include a short loader program at the beginning of the monitor. Then you can execute the monitor just by typing its name.

A suitable loader program is given in Listing 6.18. Type the program into your editor. There are two locations that need to be matched to your monitor; these are the addresses of START and FINAL. START must correspond to the first address of your monitor. The address FINAL is the last address of the monitor.

\begin{tabular}{|c|c|c|c|c|}
\hline 010C & C20000 & JNZ & 0 & \$NO, QUIT \\
\hline 010 F & 23 & INX & H & © INCREMENT \\
\hline 0110 & 03 & INX & E & \% POINTERS \\
\hline 0111 & 7B & MOV & A, E & S DONE? \\
\hline 0112 & 95 & SUB & \(L\) & \\
\hline 0113 & 7A & MOV & A \(\quad\) II & \\
\hline 0114 & 9 C & SBE & H & \\
\hline 0115 & 120901 & JNC & LOOP & OKEEF GOING \\
\hline 0118 & c30058 & JMP & START & ¢ LIONE \\
\hline & & & & \\
\hline O11B & & ENIf & & \\
\hline
\end{tabular}

Assemble the loader program, then load it into memory with the debugger SID or DDT.

\section*{A DDAT MOVE.MEX}

Next, place a copy of the monitor into memory starting at address 120 hex. If the monitor is already in memory, a copy can be generated with the monitor itself. DDT or SID can also be used for this task. The command is
```

M5800 5BFF 120

```

If the monitor resides on disk as a hex file, it can be loaded with the debugger after you calculate the offset. The offset is necessary since hex files are normally loaded at the operating address, but we want to put it somewhere else.

The required offset should be given in the assembly listing of the loader program as the value of the equate OFFST. If your assembler doesn't print such values, then use the debugger to calculate the value.
```

H120 5800 <startins value of monitor>
5920 A920
<sum> <dipference.

```

Give the commands
```

IMON17.HEX
R<offset>

```
so that the monitor will be loaded starting at address 120 hex.
Return to the CP/M system

GO
<so to zero.
and save the combination
ASAVE 5 MONITOR.COM

From now on, all you have to do is type the command

\section*{A. MONITOR}
and the monitor will automatically start up.
What actually happens is that the combination of the monitor and the loader program is first copied into memory at 100 hex. The move program relocates the monitor from address 120 hex to its proper place. Then control is transferred to the monitor. As each byte is moved to the new location, it is checked to see that it actually got there. If not, the process is terminated and control returns to CP/M.

This short loader can be placed on the front of any program that must be relocated. Only the first two instructions may have to be changed to reflect the proper starting and ending addresses.

In the next chapter, we will convert our monitor to Z-80 code. The Z-80 version will be smaller so that we can incorporate a few additional features and still be able to fit the program into 1 K of ROM. The features in the next chapter can be incorporated in the 8080 version, but they will take so much space that the monitor will no longer fit into 1 K bytes.

\section*{CHAPTER SEVEN}

\section*{A Z-80 System Monitor}

The system monitor developed in Chapter 6 contains many features. Since the size is less than 1,024 bytes, it will easily fit into a 1 K PROM, such as the 2708 EPROM. It can then be ready for use as soon as the computer is turned on. But, in this case, it may be necessary to include a routine to initialize the peripheral ports, such as those that handle the console and printer. In addition, you might want to send output to a printer as well as to the video console. If these two features are added to the monitor, the size will increase beyond 1 K bytes and it will not fit into a single 1 K PROM.

One way to add these new features without increasing the monitor's size is to remove some of the original routines. Another way, if you have a Z-80 CPU, is to convert some of the instructions to the more compact Z-80 equivalent operations. The latter approach will be followed in this chapter. Listing 7.1 gives the final version with all changes discussed in this chapter. The symbol table at the end can be used to find the routines of interest.
```

Listins 7.1 The Z-80 version of the sustem monitor.
TITLE Z-80 SYSTEM MONITOF
\#
(Mate soes nere)
\hat{j}
FOUR SECTIONS HAVE BEEN REMOUED:
UERS EQU ... (1 LINE)
SIGNON: *.. (A LINES)
LXI D,SIGNON (2 LINES)
SENDM: ... (G LINES)
; ONE SECTION HAS BEEN AMMEN:
LIST OUFUT ROUTINES
\#
O018 TOF EQU 24 GMEMORY TOF, K RYTES
5800
OFGIN EQU (TOF-2)* 1024 OFROGRAM START

```



\section*{587A 20 F.8 \\ 587C 11 \\ \(58711 \quad 19\)}

587E \(3157 A 0\)
\begin{tabular}{lll}
5881 & BE & 03 \\
5883 & H3 & 10 \\
5885 & 103 & 12 \\
5887 & \(3 E\) & 15 \\
5889 & H3 & 10 \\
\(588 E\) & 103 & 12 \\
5880 & AF & \\
\(588 E\) & 32 & \(57 A 0\)
\end{tabular}

5891215891
5894 ES
5895210000
\(5898 \quad 06 \quad 57\)
589A 7E
589 E 2 F
589C 77
5891 BE
589E \(20 \quad 05\)
58 AO 2 F
58A1 77
58 A 224
58A3 10 F5
\(58 A 54 C\)
\(58 A G\) CD 5935
\(58 A 9\) CI 59F8
58AC CD 58F■
58AF CI 5949
\(58 \mathrm{B2}\) 116 41
58B4 IIA 59EO
58 E 7 FE 1A
\(58 \mathrm{~A} 9 \mathrm{D2} 59 \mathrm{E} 0\)
58RC 87
588 n 2158 Cg
58 CO 1600
58 C 25 F
58C3 19
```

JR NZ,OUTCR gOUTER LOOF

```
JR NZ,OUTCR gOUTER LOOF
FOF IIE {RESTORE
FOF IIE {RESTORE
        RET
        RET
    & CONTINUATION OF COLII START
    & CONTINUATION OF COLII START
&
&
COLID: LD SF.STACK
COLID: LD SF.STACK
    INITIALIZE I/O FORTS
    INITIALIZE I/O FORTS
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
```

LLI (l)

```


```

LLI (l)

```
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
LLI (l)
```

LLI (l)

```


```

LLI (l)

```
LLI (l)
& IISFLAY HIGH BYTE OF MEMORY TOF.
& IISFLAY HIGH BYTE OF MEMORY TOF.
    #
    #
LLI HL,O FFAGE ZERO
LLI HL,O FFAGE ZERO
LII B,HIGH STACK %GTOF HERE
LII B,HIGH STACK %GTOF HERE
NFAGE: LD Ag(HL) कGET BYTE
NFAGE: LD Ag(HL) कGET BYTE
CFL %COMPLEMENT
CFL %COMPLEMENT
LII (HL),A \hat{FPUT IT BACK}
LII (HL),A \hat{FPUT IT BACK}
CF (HL) ;SAME?
CF (HL) ;SAME?
JR NZ,MSIZE $NO, MEM TOF'
JR NZ,MSIZE $NO, MEM TOF'
                                    #ORIG EYTE
                                    #ORIG EYTE
II (HL.),A 引RESTORE IT
II (HL.),A 引RESTORE IT
INC H &NEXT PAGE
INC H &NEXT PAGE
HINZ NFAGE {KEEF GOING
HINZ NFAGE {KEEF GOING
MSIZE: LD C,H jMEM TOF
MSIZE: LD C,H jMEM TOF
CALL CRLF \hat{NEW LINE}
CALL CRLF \hat{NEW LINE}
CALL DUTHX कFRINT MEM SIZE
CALL DUTHX कFRINT MEM SIZE
CALL INFLN ;CONSOLE LINE
CALL INFLN ;CONSOLE LINE
CALL GETCH \hat{FIRST CHAR}
CALL GETCH \hat{FIRST CHAR}
\hat{p}
\hat{p}
% MAIN COMMAND FROCESSOR
```

% MAIN COMMAND FROCESSOR

```


```

JF C,ERFROR \hat{ < A}

```
JF C,ERFROR \hat{ < A}
CF' 'Z'-'A'+1
CF' 'Z'-'A'+1
JF' NC,ERROR & > Z
JF' NC,ERROR & > Z
ALII A,A कMOUBLE
ALII A,A कMOUBLE
LII HL,TAELE #START
LII HL,TAELE #START
LII H,O
LII H,O
LII E,A tOFFSET
LII E,A tOFFSET
AND HL,ME fADM TO TABLE
```

AND HL,ME fADM TO TABLE

```
\begin{tabular}{ll}
\(58 C 4\) & \(5 E\) \\
\(58 C 5\) & 23 \\
\(58 C 6\) & 56 \\
\(58 C 7\) & \(E B\) \\
\(58 C 8\) & \(E 9\)
\end{tabular}
\begin{tabular}{|c|c|}
\hline C8 & 5 Sal \\
\hline 58CI & 5A15 \\
\hline S8CF & 595E \\
\hline 5801 & 59E0 \\
\hline 5803 & 5A64 \\
\hline 58105 & SA14 \\
\hline 58117 & 5E51 \\
\hline 5809 & 5 E 31 \\
\hline 58DE & 5860 \\
\hline 58 nm & 59E0 \\
\hline 58DF & 5A19 \\
\hline 58 EL & 5A97 \\
\hline 58 E 3 & 59E0 \\
\hline 58 ES & \(5 \mathrm{B47}\) \\
\hline 58 E 7 & 59E0 \\
\hline 58 E 9 & 59E0 \\
\hline S8ER & 5B8C \\
\hline 58ED & SaAd \\
\hline S8EF & 59E0 \\
\hline \(58 F 1\) & 59E0 \\
\hline 58 F 3 & 5bab \\
\hline 58F5 & 59E0 \\
\hline 58F7 & 5A56 \\
\hline 5879 & 59E0 \\
\hline & \\
\hline
\end{tabular}

58C9 5AD3
59E0
58CF 595E
5801 59E0

581175851
58195631
58DE 5B60
580 LI 5 EO
5A19
58E3 59E0
\(58 \mathrm{E} 5 \mathrm{5B47}\)
58E7 59E0
58ER SBBC
SBED SAAL
-
\(58 F 3\) 5RAE
8FS S9E0
58F9 59E0
58FB 5A5II




\begin{tabular}{lll}
\(59 F 8\) & 79 \\
\(59 F 9\) & \(1 F\) \\
\(59 F A\) & \(1 F\) \\
\(59 F B\) & \(1 F\) \\
\(59 F C\) & \(1 F\) & \\
\(59 F D\) & \(C D\) & \(5 A O 1\) \\
\(5 A O O\) & 79 & \\
\(5 A O 1\) & \(E 6\) & \(0 F\) \\
\(5 A 03\) & \(C 6\) & 90 \\
\(5 A O 5\) & 27 & \\
\(5 A 06\) & \(C E\) & 40 \\
\(5 A O 8\) & 27 & \\
\(5 A O 9\) & \(C 3\) & 5835
\end{tabular}

5AOC 23
5AOL 7E
5AOE 95
SAOF 7A
5A10 9C
\(5 A 11\) 10
5A12 E1
5A13 C9
\begin{tabular}{lll}
\(5 A 14\) & \(E 1\) & \\
\(5 A 15\) & \(C D\) & \(59 A E\) \\
\(5 A 18\) & \(E 9\) &
\end{tabular}
\begin{tabular}{|c|c|c|c|}
\hline OUTHX: & LII & As C & \\
\hline & RFA & & irotate \\
\hline & RRA & & ; FOUR \\
\hline & RFiA & & - EITS To \\
\hline & RRA & & * RIGHT \\
\hline & CALL & HEX1 & GUPPER CHAR \\
\hline & LLI & A, C & FLOWER CHAR \\
\hline HEX1: & ANLI & OFH & - TAKE 4 BITS \\
\hline & ADD & A.90H & \\
\hline & DAA & & GMAA TRICK \\
\hline & ALIC & \(\mathrm{A}, 40 \mathrm{H}\) & \\
\hline & LIAA & & \\
\hline & JF' & OUTT & \\
\hline ; & & & \\
\hline ¢ CHECK & FOR EN & , HoL MI & NUS [1, E \\
\hline ) INCRE & MENT H & & \\
\hline \% & & & \\
\hline TSTOF: & INC & HL & \\
\hline & LII & A, E & \\
\hline & SUB & & ; E-L \\
\hline & LII & A, II & \\
\hline & SEC & ApH & \% \(\mathrm{II}-\mathrm{H}\) \\
\hline & RET & NC & SNOT IONE \\
\hline & FOF & HL. & ORAISE STACK \\
\hline & RET & & \\
\hline ; & & & \\
\hline \% ROUTI & NE TO & ANYWHER & E IN MEMORY \\
\hline ¢ FOR C & ALL ENTR & Y, ADDRE & SS OF WARM \\
\hline \(\stackrel{\text { ¢ }}{ }\) IS ON & STACK, & SO A SIM & FLE RET \\
\hline \% WILLL & FETURN & 0 THIS M & ONITOR \\
\hline \(\stackrel{\square}{0}\) & & & \\
\hline G0: & POP & HL & ЯRATSE STACK \\
\hline CALLS: & CALL & REALHL & GGET ADLRESS \\
\hline & JF' & (HL) & ¢GO THERE \\
\hline \% & & & \\
\hline - LOAII & HEX OR & SCII CHA & R INTO MEMORY \\
\hline \% FROM & CONSOLE & CHECK T & 0 SEE IF \\
\hline \(\hat{\text { \% }}\) THE MA & ATA ACT & ALLY GOT & THERE \\
\hline ; AFOSTR & ROFHE P & ECEEROS A & SCII CHAR \\
\hline ; CARRI & AGE FIET & PASSES & OUER LOCATION \\
\hline \% & & & \\
\hline LOAD: & CALL & REAMHL & \% AMMRESS \\
\hline LOALI2: & CALL & OUTHL. & FFRINT IT \\
\hline & CALL & FASCI & ¢ASCII \\
\hline & CALL & OUTSP & \\
\hline & L.II & Co (HL) & 今ORIG BYTE \\
\hline & CALL & OUTHEX & g HEX \\
\hline & FUSH & HL & - SAVE PNTR \\
\hline & CALL & INPL 2 & ¢ INFUT \\
\hline & CAll & REALHL & 9 BYTE \\
\hline & LII & B,L & ¢ 70 B \\
\hline & POP & HL & \\
\hline & CF & APOS & \\
\hline & JR & Z.LOAIIG & QASCII INPUT \\
\hline & LII & A, C & ¢HOW MANY? \\
\hline & OR & A & - NONE? \\
\hline & JR & Z.LOALS & ¢YES \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline 5A3A & CD & \(5 A 46\) & LOALI4: & CALL & CHEKM & \multirow[t]{2}{*}{- INTO MEMORY „POINTER} \\
\hline 5A3II & 23 & & LOAII3: & INC & HL. & \\
\hline \multirow[t]{4}{*}{SA3E} & \multirow[t]{4}{*}{18} & \multirow[t]{4}{*}{Lic} & & JR & \multicolumn{2}{|l|}{LOAD2} \\
\hline & & & \multicolumn{4}{|l|}{t} \\
\hline & & & \multicolumn{4}{|l|}{¢ LOAI ASCII CHARACTEF} \\
\hline & & & \multicolumn{4}{|l|}{¢} \\
\hline 5 A 40 & Ca & 5949 & LOALI6: & CALL & GETCH & \\
\hline 5 A43 & 47 & & & LII & ByA & \\
\hline \multirow[t]{5}{*}{5 A44} & 18 & F4 & & JFi & LOADI & \\
\hline & & & \multicolumn{4}{|l|}{\%} \\
\hline & & & \multicolumn{4}{|l|}{A COFY BYTE FROM E TO MEMORY} \\
\hline & & & \multicolumn{4}{|l|}{\multirow[t]{2}{*}{\(\hat{\dot{g}}\) ¢ ANI SEE THAT IT GOT THERE}} \\
\hline & & & & & & \\
\hline 5 S46 & 70 & & \multirow[t]{4}{*}{CHEKM:} & LII & \multicolumn{2}{|l|}{(HL), B OPUT IN MEM} \\
\hline 5 A47 & 7E & & & LII & A) (HL) & gGET BACK \\
\hline 5 A48 & H8 & & & CF' & B & ¢SAME? \\
\hline \(5 A 49\) & C8 & & & RET & Z & ©OK \\
\hline \(5 A 4 A\) & F1 & & ERRF: & FOF & AF- & ¢RAISE STACK \\
\hline \(5 A 4 B\) & 3E & 42 & ERRE: & LIL & \(A{ }^{\prime} B^{\prime}\) & ¢ BAII \\
\hline \(5 A 411\) & CII & 5835 & & CALL & OUTT & \\
\hline \(5 A 50\) & CI & 5973 & & CALL & OUTSP & \\
\hline \multirow[t]{3}{*}{5 S53} & \multirow[t]{3}{*}{C3} & \multirow[t]{3}{*}{S9EE} & & JF & OUTHL & APOINTER \\
\hline & & & \multicolumn{2}{|l|}{\(\hat{\theta}\)} & & \\
\hline & & & \multicolumn{2}{|l|}{```
; gisplay gtack
%
```} & FOINTER & REGTSTER \\
\hline 5 556 & 21 & 0000 & \multirow[t]{3}{*}{REGS:} & LII & HL, 0 & \\
\hline 5459 & 39 & & & AIIS & HL, SP & \\
\hline \multirow[t]{4}{*}{\(545 A\)} & \multirow[t]{4}{*}{C3} & \multirow[t]{4}{*}{59EB} & & JP & OUTHL & \\
\hline & & & \multicolumn{4}{|l|}{\multirow[t]{3}{*}{\% ZERO A PORTION OF MEMORY}} \\
\hline & & & & & & \\
\hline & & & & & & \\
\hline \(5 A 51\) & CII & 5999 & \multirow[t]{3}{*}{ZERO:} & CALL & RIMHLIEE & \multirow[t]{3}{*}{¢ FIANGE} \\
\hline 5460 & 06 & 00 & & LII & B: 0 & \\
\hline \multirow[t]{4}{*}{5462} & \multirow[t]{4}{*}{18} & \multirow[t]{4}{*}{08} & & JFi & FILL2 & \\
\hline & & & \multicolumn{4}{|l|}{\multirow[t]{2}{*}{, FILL A FORTION OF MEMORY}} \\
\hline & & & & & & \\
\hline & & & \multicolumn{4}{|l|}{} \\
\hline \(5 A 64\) & CHI & 5 A 80 & \multirow[t]{4}{*}{FILL:} & CALL & HLIEEBC & ¢RANGE, BYTE \\
\hline 5467 & FE & F7 & & CF & APOS & ¢AFOSTROFHE? \\
\hline 5469 & 28 & \multirow[t]{3}{*}{OF} & & JR & Z,FILL4 & ¢YES. ASCII \\
\hline 5 A 6 B & 41 & & & Lu & \(\mathrm{E}, \mathrm{C}\) & \\
\hline \(5 A 6 C\) & 7 C & & \multirow[t]{3}{*}{FILL2:} & LII & AsH & \#FILL BYTE \\
\hline \(5 A 6 I 1\) & FE & 57 & & CP & HIGH STA & ACK ¢TOO FAR? \\
\hline 5 A 6 F & 12 & 59E0 & & JP' & NC, ERROR & \% YYES \\
\hline \(5 A 72\) & CII & \(5 A 46\) & \multirow[t]{3}{*}{FILL3:} & CALL & CHEKM & ¢PUT, CHECK \\
\hline 5 A75 & CII & \(5 A O C\) & & CALL & TSTOF & PDONE? \\
\hline \multirow[t]{2}{*}{5 A 78} & \multirow[t]{2}{*}{18} & \multirow[t]{2}{*}{F2} & & JR & FILL? & ¢NEXT \\
\hline & & & \multicolumn{4}{|l|}{¢} \\
\hline \(5 A 7 A\) & CD & 5949 & FILL4: & CALL & GETCH & \#ASCII CHAR \\
\hline \(5 A 70\) & 47 & & & LII & B, \({ }^{\text {A }}\) & \\
\hline \multirow[t]{3}{*}{SA7E} & \multirow[t]{3}{*}{18} & \multirow[t]{3}{*}{\(F 2\)} & & JR & FILL3 & \\
\hline & & & \multicolumn{4}{|l|}{} \\
\hline & & & ; GET & HgL IIgE Al & NH: ByC & \\
\hline 5480 & CII & \(5 A 8 E\) & HLDEBC: & : CALL & HLIEECK & FFANGE \\
\hline 5483 & IIA & 59E0 & & JF' & C, ERROR & ONO EYTE \\
\hline 5486 & E5 & & & FUSH & HL. & \\
\hline
\end{tabular}
\begin{tabular}{ll}
\(5 A 87\) & \(C \cap\) \\
\(5 A 8 A E\) \\
\(5 A B A\) & 44 \\
\(5 A B B\) & \(4 \cap\) \\
\(5 A B C\) & \(E 1\) \\
\(5 A B D\) & \(C 9\)
\end{tabular}
\(5 A 97\) CL 5 A80
5A9A CL 5AA3
5A9II CI 5AOC
\(5 A A O \quad 03\)
SAA1 18 F7
5AA3 7E
5AA4 O2
\(5 A A 5\) OA
SAAG BE
5AA7 C8
5AAB 60
SAA9 69
\(5 A A A\) C3 5A4A
5AAL CI 5A8O
SAEO OG OLI
5AB2 3806
5AB4 E5
5AB5 CN 59AE
SAB8 45
5AR9 E1
SABA 7E
SAEB B9
5ABC 2010
\(5 A B E 23\)
SABF 78
SACO FE OLI
5AC2 2804
5AC4 7E
5AC5 B8
\(5 A C 620 \quad 06\)


\begin{tabular}{|c|c|c|}
\hline LI & Ag (HL) & gNEXT BYTE \\
\hline CF & B & \#MATCH? \\
\hline JFi & NZ, SEARA & 9 NO \\
\hline
\end{tabular}
```

                                    CALLL FEALIHL S}3FLD INFU
    ```
                                    CALLL FEALIHL S}3FLD INFU
LII B,H कMOVE TO
LII B,H कMOVE TO
                                    LII C,L & BoC
                                    LII C,L & BoC
POF HL
POF HL
FEET
FEET
;
;
& GET 2 AMDRESSES, CHECK THAT
& GET 2 AMDRESSES, CHECK THAT
* ammitional data is included
* ammitional data is included
%
%
% MOUE A HLOCK OF MEMORY H.L-HgE TO B,C
% MOUE A HLOCK OF MEMORY H.L-HgE TO B,C
g
g
OF
OF
    M B,C
    M B,C
\hat{p}
\hat{p}
{ SEARCH FOR 1 OR 2 BYTES OVER THE
{ SEARCH FOR 1 OR 2 BYTES OVER THE
; FIANGE H,L LI,E EYTES AFE IN B,C
; FIANGE H,L LI,E EYTES AFE IN B,C
& B HAS CAFFFIAGE RETURN IF ONLIY ONE BYTE
& B HAS CAFFFIAGE RETURN IF ONLIY ONE BYTE
\hat{y}FUT SFACE BTWEEN BYTES IF TWO
\hat{y}FUT SFACE BTWEEN BYTES IF TWO
; FORMAT: START STOP BYTEX BYTE2
; FORMAT: START STOP BYTEX BYTE2
;
;
SEARCH: CALL HLDEBC FRANGE, 1ST BYTE
SEARCH: CALL HLDEBC FRANGE, 1ST BYTE
SEAF2: LII B,CR OSET FOR 1 BYTE
SEAF2: LII B,CR OSET FOR 1 BYTE
    JR COSEARZ ;ONLY ONE
    JR COSEARZ ;ONLY ONE
    FUSH HL
    FUSH HL
    CALL FEADHL % SNN EYTE
    CALL FEADHL % SNN EYTE
    LII ByL SINTO C
    LII ByL SINTO C
    FOF HL
    FOF HL
SEAR3: LIH Ag(HL) #GET BYTE
SEAR3: LIH Ag(HL) #GET BYTE
CF C EMATCH?
CF C EMATCH?
JR NZ.SEAR4 INO
JR NZ.SEAR4 INO
INC HL OYES
INC HL OYES
LII A,B FONLY 1?
LII A,B FONLY 1?
CP CF
CP CF
Z,SEARS \hat{YES}
Z,SEARS \hat{YES}
\hat{0}
\hat{0}
% FOUND FIRST MATCHO CHECK FOR SECOND
% FOUND FIRST MATCHO CHECK FOR SECOND
%
```

%

```
5ABE CL 59A3
\(5 A 91\) IIA 59EO
\(5 A 94\) C3 599C



\begin{tabular}{|c|c|c|}
\hline 5BB1 & CI & 59E8 \\
\hline \(5 \mathrm{EB4} 4\) & 4E & \\
\hline 5 BES & CII & 5970 \\
\hline 5 BEP & 3E & 3A \\
\hline 5 BBA & CII & 5835 \\
\hline 5 EBLI & E1 & \\
\hline 5 EBE & CH & 59EE \\
\hline 5 ECL & 4E & \\
\hline SEC2 & CD & 5978 \\
\hline \(5 \mathrm{BC5}\) & 41. & \\
\hline 58C6 & 44 & \\
\hline 5 BC 7 & E1 & \\
\hline \(5 \mathrm{BC8}\) & CII & \(5 A O C\) \\
\hline 5 ECB & 03 & \\
\hline 5RCC & 18 & III \\
\hline
\end{tabular}
\(5 \mathrm{BB1}\) Cम 59E8
5BE4 4E
5BE5 CL 59FO
\(5 B E 8\) 3E 3A
5BBA CI 5835
SERLI EL
5 EBE CH 59EB
\(5 \mathrm{EBC1} 4 \mathrm{E}\)
5ECS CD 59F8
5BC5 41
5RC6 44
5BC7 E1
\(5 B C 8\) CI SAOC
5 ECC 18 M

Sumbols:
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline AIMF'2 & 5 EO 01 & AIMP3 3 & 5 F 18 & ALMPA & 5 EAB & AIIUMF & 5 AFE \\
\hline AL.OH2 & 5AE9 & AFOS & FFF7 & ASCII & SAD3 & ASCS & 5820 \\
\hline BACK゙UF' & 0008 & BIT2 & 5H3C & BITS & 5B3A & CALLS & 5 A 15 \\
\hline chata & 0011 & CHEKM & \(5 A 46\) & CIN & 5809 & COLI & 587E \\
\hline COUT & 5806 & CR & 00011 & CRHL & 59E8 & CRLF & 5935 \\
\hline CSTAT & 0010 & CTEH & 0008 & CTRF* & 0010 & CTRQ & 0011 \\
\hline CTRS & 0013 & CTRX & 0018 & UEL & 007F & RUMF. & 595E \\
\hline LUMF2 & 5961 & nump 3 & 5964 & LUMPF4 & 5975 & LIUMPS & 597E \\
\hline ERFEE & 5A4B & ERFROR & 59E0 & ERFP' & \(5 A 4 A\) & FILL. & \(5 A 64\) \\
\hline FILL2 & 5 A 6 C & FILL3 & 5 S 72 & FILL. 4 & SA7A & GCHAF & 580 F \\
\hline GETC4 & 595 C & GETCH & 5949 & GO & \(5 A 14\) & HEX1 & \(5 A 01\) \\
\hline HHLIEE & 59A3 & HLIEEC & 5 A 80 & HLLDECK & SABE & HMATH & 5851 \\
\hline I RUFC & 5745 & IBUFF & 57 Ab & IEUFF' & 5743 & INLN & 580 C \\
\hline INMSK & 0001 & INPL2 & 5902 & INFLL 3 & 591 E & INFLE & 593 F \\
\hline INPLC & 5929 & INFLE & 5924 & INFLI & 590A & INPL & 58 FII \\
\hline INFUTS & 581A & INFUTT & 5815 & INSTAT & 5827 & IFORT & 5 B 31 \\
\hline JERF & 5B7E & JUST & \(5 \mathrm{B60}\) & JUST2 & 5864 & Just3 & \(5 \mathrm{B6} 11\) \\
\hline lidata & 0013 & LF & OOOA & LOAII & 5 S19 & LOALI2 & 5A1C \\
\hline LDAD3 & 5A3 & LOALI 4 & 5 A 3 A & LOALIG & \(5 A 40\) & L.OMSK゙ & 0002 \\
\hline LOUT & 585 B & l.stat & 0012 & MOUIN & 5A9A & MOVE & 5497 \\
\hline MOUIN & \(5 A A 3\) & MSIZE & 5845 & NIE & 59110 & NNULS & 0004 \\
\hline NFAGE & 589A & OMSK & 0002 & OFORT & 5847 & ORGIN & 5800 \\
\hline OUT2 & 583 C & OUT3 & 5848 & OUT4 & 5851 & OUTCE: & 5874 \\
\hline OUTCF2 & 5876 & OUTH & 5812 & OUTHEX & 5970 & OUTHL & 59 EB \\
\hline OUTHX & 5978 & OUTLL & 59EF & OUTSF & 5953 & OUTT & 5835 \\
\hline F'ASC2 & 5994 & FASC3 & 5996 & FASCI & 598E & FORTN & 57 AO \\
\hline FLIHLIL & 5983 & FIDHL 4 & 5905 & RHHLS & 59 Ca & RLHLIS & 599 C \\
\hline RIMHLIEE & 5999 & REALIHL & 59AE & FEGS & 5456 & REFL & \(5 \mathrm{B8C}\) \\
\hline REFL? & 5899 & FEFL3 & 5 BA 3 & RESTRT & 5803 & SEAR2 & 5 SAO \\
\hline SEAR3 & \(5 A B A\) & SEARA & SACE & SEAKS & 5 CL 8 & SEARCH & SAAII \\
\hline SETLST & 582 C & STACK & 57 AO & STAFT & 5800 & TAB & 0009 \\
\hline TABLE & \(58 \mathrm{C9}\) & TOP & 0018 & TSTOF & \(5 A O C\) & UERM & 5EAB \\
\hline UEFM2 & \(5 B A B\) & UEFIM & \(58 C 8\) & WARM & 5891 & ZERO & \(5 A 511\) \\
\hline
\end{tabular}

\section*{CONVERSION OF THE MONITOR TO Z-80 MNEMONICS}

If you used 8080 mnemonics to program the monitor in Chapter 6, you can now convert it to Z-80 mnemonics. The form of the mnemonics depends on the type of assembler you have. The Microsoft assembler accepts both the Intel 8080 and the Zilog Z-80 mnemonics. Since most other assemblers use only one or the other, you may need a second assembler.

The Digital Research assembler MAC requires the 8080 mnemonics, but it can generate Z-80 code with an accompanying macro library. The Xitan assembler utilizes 8080 mnemonics for the common set of 8080-type instructions and Zilog-like instructions for the others.

First, make a working copy of the monitor using PIP, a CP/M utility routine.

PIF MONZ.ASM=MON17.ASM[V]
If you are using MAC or the Xitan assembler, skip to the next section. Otherwise, use the system editor to make the necessary changes to the new file. The conversion can be easily performed with the global substitute command of the Word-Master or the CP/M editor. For example, the 8080 mnemonic

\section*{MOV AgM}
can be changed to the equivalent Z-80 mnemonic
LD \(A_{0}(H L)\)
with the command
*SMOUくtab>ADM\&LD<tab>A9 (HL) कOTT
The \(\$\) symbols indicate that the escape key is pressed. The "tab" refers to the ASCII tab key, a control-I. You may find the cross-reference list for 8080 and Z-80 mnemonics, given in Appendix G, helpful in the conversion process.

After changing the monitor to Z-80 mnemonics, assemble it and carefully check the assembly listing to see that the hex code is correct. The Z-80 version at this time should generate the same hex code as the 8080 version. A further check can be made with the monitor's V command. Load the binary code into memory with an offset. A command of
```

HDT
IMONZ.HEX
RFOOO

```
will load the new version 4 K bytes below the regular monitor position. Branch to the monitor prepared in the last chapter. Then compare its code to the new version using the verify command. If there is a discrepancy, find the error and correct it. When you are convinced that the Z-80 version produces the same code as the 8080 version, you can begin the alterations to reduce the monitor's size.

\section*{REDUCING THE MONITOR SIZE}

In this section you will reduce the monitor size by converting many of the 3-byte absolute jump instructions into 2 -byte relative jump instructions. This change will make room for additional features. There are five types of jumps to be changed.
```

absolute
MSMME

```
relative
jumF
JR \(\quad X\)
\(J R \quad Z, X\)
\(J R \quad N Z g X\)
\(J R \quad C g X\)
\(J R \quad N C ; X\)
```

condition
unconditional
zero
not zero
carrs
not carry

```

Not all of the absolute jumps can be converted in this way since the relative jumps are limited to a distance of about 126 bytes.

Another way to obtain more space is to move some of the subroutines to more advantageous locations. This will allow a few more absolute jumps to be converted into relative jumps. For example, several routines contain a jump to the routine ERROR. These can be placed together in a group. Then the ERROR routine can be moved into the middle of the group.

Another change will free up three more bytes. Notice that subroutine OUTSP ends with the instruction
```

JP OUTT

```

If this subroutine were located directly ahead of subroutine OUTT, then the jump instruction would not be necessary. Actually, this type of change has already been used extensively in our monitor. Subroutines CRHL, OUTHL, OUTHEX, and OUTSP are all directly related. They initially could have been programmed (using Z-80 mnemonics) as
```

CRHL: CALL CRLF
CALL OUTHL
RET
%
OUTHL: LDD COH
CALL OUTHX
OUTLL: LD COL
CALL OUTHEX
RET
\
OUTHEX: CALL OUTHX
CALL OUTSP
RET

# 

OUTSP: LDD A,',
CALL OUTT
RET

```

The CALL/RET combination at the end of each routine can be replaced by a JP instruction. Then, since the calling program is located directly above the called program, the jump instruction becomes unnecessary. Thus, four bytes are saved in each of the first three routines. Furthermore, if this entire block of four subroutines were located just prior to subroutine OUTT, we could eliminate the final JP OUTT instruction and save three more bytes.

While this kind of subroutine rearrangement can be used to make the overall program smaller, there is a penalty. The readability is reduced. We have traded comprehension for space. This may not, in general, be a worthwhile tradeoff for assembly-language programming. Such programs are more difficult to understand than those written in a high-level language such as Pascal or BASIC. Furthermore, assembly-language programs are typically much shorter than they would be if written in a higher-level language. But if packing a maximum number of features into a 1 K PROM is your goal, then this technique may be worth it.

\section*{GETTING MORE FREE SPACE}

The two instructions
\begin{tabular}{ll}
meC & B \\
JP & \(\mathrm{NZ}, \mathrm{X}\)
\end{tabular}
which generate four bytes of code appear in two places. Replace them with the 2-byte instruction

IUJNZ \(X\)
One location is just prior to the label MSIZE (address 58A5 in Listing 7.1) and the other is in subroutine BITS (5B3A). This change will free four more bytes.

The 16 -bit subtraction routine in HMATH (5B51) has been improved. The sequence of instructions
\begin{tabular}{|c|c|}
\hline LII & AgL \\
\hline SUB & A, E \\
\hline LD & L; A \\
\hline LD & AyH \\
\hline SBC & A, II \\
\hline LD & H, A \\
\hline
\end{tabular}
is replaced by the shorter, double-precision subtraction:
```

OR A greset carry
SEC HLgDE ysubtract

```

Three more bytes are freed by this change.

Since the Z-80 contains a set of instructions for direct rotation of data in the general CPU registers, we can simplify subroutine BITS. In the 8080 version, the three instructions
\begin{tabular}{ll}
\(\operatorname{MOV}\) & \(A, L\) \\
AMD & \(A\) \\
\(\operatorname{MOU}\) & \(L, A\)
\end{tabular}
are used to move the data from a general register to the accumulator, perform the shift, then move it back. The 2 -byte, Z-80 arithmetic shift left instruction

SLA L
performs the shift directly in the L register.
The 8080 can output a byte only from the accumulator, and can input a byte only to the accumulator. Furthermore, the address of the peripheral must be located in memory immediately following the first byte of the input or output instruction.

The port-input routine IPORT and the port-output routine OPORT in the system monitor utilized subroutine PUTIO. This routine writes the desired IN or OUT instruction in memory, the requested port address and then a return instruction. There is a \(\mathrm{Z}-80\) instruction that can perform I/O from any register. The address of the peripheral is located in register C in this case. Since the port address does not have to be located in memory, subroutine PUTIO can be eliminated. The resulting Z-80 code is 19 bytes shorter than the 8080 version. See Listing 7.1 for the new versions of IPORT (5B31) and OPORT (5B47).

Since you are nearly finished with the development of the monitor program, you can gain some more space by removing the routines that print the version number. There are four areas involved. First, delete the line near the beginning that identifies the version number.

\section*{VERS EQU '17'}

Second, remove four lines starting with the label SIGNON. Third, delete the two lines starting on the line after the label COLD.
```

LIN INE,SIGNON
CALL SENAM

```

Fourth, remove the entire subroutine SENDM, but keep a copy of it in case you want to incorporate it in another program.

\section*{PERIPHERAL PORT INITIALIZATION}

There are two schools of thought on peripheral port initialization. One approach is to initialize ports only on a cold start or a warm start. The other
way is to initialize a port each time it is used. The method you use depends on the integrity of your system.

The approach taken in this chapter initializes ports only on a cold start. The instructions are placed just after the label COLD. In anticipation of adding a printer-output routine, we include the initialization for two separate peripherals.

Ports which need initialization utilize a control register for this purpose. The address of the control register is the same as the status register. A CPU IN instruction reads the status register, while a CPU OUT instruction to the same address writes into the control register. A typical initialization procedure requires two OUT instructions. The first is used to reset the port; the second is used to set the desired options. The values shown in the listing correspond to a Motorola 6850 ACIA serial port set for eight data bits, one stop bit, and no interrupts.
\begin{tabular}{|c|c|c|c|}
\hline Lu & \multicolumn{3}{|l|}{A 3} \\
\hline OUT & (CSTAT), A & \% & RESET \\
\hline LII & A. 15 H & & \\
\hline our & (CSTAT):A & ¢ & SET F \\
\hline
\end{tabular}

\section*{PRINTER OUTPUT ROUTINES}

Up to this point, we have been writing programs for output to a console video screen. We output an ASCII backspace character for error correction so that the cursor will actually back up on the screen. We also included a pair of scroll commands: control-S to freeze the display and control-Q to resume the scrolling.

Sometimes, however, we want computer output we can look at after the computer has been shut off. A printer or list device is what we need for this purpose. We will not want to use the printer as a main console, though, because it is too slow.

For sophisticated operating systems like CP/M, the software for the list device is wholly separate. For example, we can divert a disk file to the printer and none of the system commands will appear on the listing.

Our approach will be a little different. The video console will always display all output whether the printer is on or not. Of course, when the printer is engaged, the console speed will be reduced to that of the printer. We will both enable and disable the printer with a control-P command, just as in \(\mathrm{CP} / \mathrm{M}\). We refer to the control-P command as a list toggle: the same command turns it on or off. The output includes the echoing of the commands typed in from the console keyboard.

Both the input and output routines will have to be changed if you want to incorporate the printer routines. In addition, two new subroutines will be added. First, add two new lines to the input routine; they will look for a control-P from the console keyboard. If a control-P is found, the program
will branch to a new subroutine called SETLST. The two new lines appear in subroutine INPUTT (5815).
\begin{tabular}{lll} 
CP & CTRP & OAP \\
JR & Z.SETLST \(\operatorname{HLIST}\)
\end{tabular}

Subroutine SETLST (582C), containing 4 lines of code, is added just after subroutine INSTAT.
\begin{tabular}{|c|c|c|c|}
\hline SETLST: & LI & A, (FORTN) & - CHECK Flag \\
\hline & CFL & & 今 INVERT \\
\hline & LII & (FORTN), A & ¢SAVE \\
\hline & JR & INFUTT & ¢NEXT BYTE \\
\hline
\end{tabular}

This routine complements the printer flag (PORTN) when a control-P is typed. The output routine uses this flag to determine whether to send output to the printer. Notice that in Chapter 6, the identifier PORTN was used to set up the port number for the I and O commands. This feature is not needed for the Z-80 version, so we can use the location for the printer flag instead.

The third new section is placed in the output routine OUTT (5835).
\begin{tabular}{lll} 
LD & Ag(FORTN) & WHERE? \\
OR & A \\
JR LOUT & \#ERO? \\
& NZIST OUTFUT
\end{tabular}

This part checks the flag PORTN to see if output is to be sent to the printer.
The fourth routine is LOUT (585B); it follows OUT4. This routine sends output to both the console and the printer. It first checks the status port for the printer. When the output bit indicates ready, a byte is sent to the printer. Since the console video screen operates so much faster than the printer, there is no need to check the console-ready flag. The byte is therefore also sent directly to the console by the next instruction. The output appears simultaneously at both devices.

\section*{DELAY AFTER A CARRIAGE RETURN}

Video screens operate with electron beams that move very fast. Mechanical printers, on the other hand, are much slower. For some printers, the time it takes to execute a carriage return is so great that the first few characters of the next line may be lost. The solution is to have the computer do something else for a little while after it sends a carriage return.

One method of slowing down the computer is to arrange for it to send binary zeros, called nulls, after each carriage return or carriage-return/linefeed pair. One routine for accomplishing this is as follows.
\begin{tabular}{|c|c|c|c|}
\hline CRLF: & LII & A CR & ¢ CARRIAGE RET \\
\hline & CALL & OUTT & - SEND \\
\hline & LII & A, LF & ALINE FEEI \\
\hline & CALL & OUTT & 9 SENI \\
\hline & XOR & A & gGET A NULL \\
\hline & CALL & OUTT & ¢SENIT IT \\
\hline & CALL & OUTT & ¢A SECONI ONE \\
\hline & CALL & OUTT & A A THIRD \\
\hline & \(J F \cdot\) & OUTT & \$THE FOURTH \\
\hline
\end{tabular}

But this approach may cause trouble if the printer circuits attempt to interpret the null characters.

A different approach is taken with the list-output routine, LOUT, shown in Listing 7.1. After each carriage return is sent, the computer starts executing a double loop. The inner loop is executed 250 times. The outer loop is set according to the equivalent number of nulls that are needed. No nulls are actually sent, though, in this case.

The disadvantage of this method is that the resultant delay time is a function of the computer speed. A Z-80 running at 4 MHz would require approximately twice the number of loops as would a \(2-\mathrm{MHz}\) Z- 80 . Thus, the loop-initialization values may have to be adjusted to the particular computer.

Be careful to tailor the port-initialization routines to your system or remove them if they are not needed. The time delay in the list-output routine should also be removed if it is not needed. If you are not sure whether a delay is necessary, then leave it in, at least for the first version. Then use the memory load command of the monitor itself to reduce the delay values on the two loops. When you reduce the delay time to too small a value, then you will notice that some of the characters are missing from the beginning of some of the lines.

A sample loop-change session could look like this.
```

215870 587F
5870 COD51678 1EFA1D20 1520....
L5873
5873 < 78 3C
5873 - 1E AX (to quit)

```

The first command line is used to display the memory region containing the loop constants. Then the outer loop value of 78 hex is changed to 3 C hex which is half the value. As long as you change the timing-loop values with the printer disengaged, no problem should occur. After each change in the timing loops, re-engage the printer with a control-P. Display several lines on the printer by giving the D command. Check to see if any of the first few characters of each line are missing. If everything is all right, then again reduce the loop constant until characters are lost. (Be sure to disengage the printer between each change.)

\section*{CHAPTER EIGHT}

\section*{Number-Base Conversion}

This chapter deals with assembly language routines that can be used to convert data from one form to another. The first part deals with the conversion of a sequence of ASCII characters called a string into a binary number. The second part reverses the procedure; binary numbers are converted into ASCII strings. The characters in each string represent digits in one of the common bases \(2,8,10\), or 16 . The corresponding binary number may be 4 bits, 8 bits, or 16 bits in size.

All of the programs in this chapter are designed to run with the system monitor developed in Chapters 6 and 7. Some of the monitor's input and output facilities are needed. These include the console input buffer which supplies the characters, the binary-to-hexadecimal conversion routine which will print the answer in hexadecimal, and the console output routine needed for the error message.

The monitor error-correction features are available during input. Pressing the DEL (or RUB) key or the backspace (control-H) key will delete the previously typed character and remove it from the console video screen. If the list routines have been incorporated into the monitor, the printer can be turned on by typing a control-P. When you have finished with each routine, you can return to the monitor simply by typing a control-X.

\section*{THE ASCII CODE}

When a key is pressed on a computer terminal, a unique signal is sent to the computer. There are several, very different ways of electronically encoding this signal. ASCII, which stands for American Standard Code for Information Interchange, is the most commonly used code. Appendix A gives the 128 ASCII characters with the corresponding values expressed in decimal, hexadecimal, octal, and binary. EBCDIC, which is used by IBM, is another coding technique.

The ASCII table can be divided into four parts. Part 1 of the table contains the nonprinting control characters. Part 2 contains most of the special characters such as \(\$, \%\), and \#, and the digits \(0-9\). The uppercase letters are found in part 3 , and the lowercase letters are found in part 4.

Computer terminals typically have a keyboard that looks like a typewriter. There is a shift key to change from lowercase letters to uppercase letters. In addition to the shift key, there will usually be a control key. This key will give the letter keys a third meaning. Thus the user can enter a lowercase letter A, an uppercase letter A (a shift A), or a control-A. The bit patterns are:

> 1100001 lowercase A
> 1000001 uppercase A
> 0000001 control-A

It can be seen from the pattern that the shift key resets bit 5 while the control key resets both bits 5 and 6.

Some of the commonly used control functions such as the carriage return (control-M), line feed (control-J), the horizontal tab (control-I), and the backspace (control-H) may have their own separate keys.

All console input to the computer will be in the form of ASCII characters. The console will send eight data bits for each character. But the ASCII code contains only seven bits per character. Consequently, the eighth, high-order bit is not needed. The user will need to have routines for converting strings of ASCII characters into the ultimate numbers that will reside in memory. For example, if the operator enters the string

3014
from the console, the computer would actually receive the bit patterns
\begin{tabular}{lll}
011 & 0111 & (ASCII 3) \\
011 & 0000 & (ASCII 0) \\
011 & 0001 & (ASCII 1) \\
011 & 0100 & (ASCII 4)
\end{tabular}

The next step is to convert the string into a 16 -bit number. The conversion scheme that is chosen depends on whether the string represents a decimal number, an octal number, or a hexadecimal number.

Additionally, a check is made to ensure that each character in the string is within the proper range. For example, octal numbers must contain only the digits zero through 7. The digits 8 and 9 , the letters A through Z , and the other characters are not used. Finally, we may need a special character, called a delimiter, to indicate the end of a string. We will use a space or a carriage return for this purpose. Thus the string of characters
will be interpreted as two separate numbers since a space appears in the middle.

The ASCII string may need to be converted into a 4 -bit nibble, an 8 -bit byte destined for a CPU register, or a 16 -bit word meant for a double register. Furthermore, the format may be either free entry or fixed entry. The choice is a matter of personal taste. With free entry, leading zeros are not needed. The entries

0004
004
04
4
are all interpreted as the same number. An additional feature is that you can recover from an error by retyping the entry on the same line. Suppose that the 4 -digit number 1035 is desired but 1045 was typed by mistake. The correct value can be immediately typed without a space.

10351045
If two 4 -digit numbers are needed, they must be separated by a delimiter.
10451055
With the fixed-entry format, the required number of digits, including leading zeros, must be entered. But since an end-of-string indicator is not needed, two numbers can be run together. The fixed-entry expression

10451055
will be interpreted as two separate numbers.

\section*{CONVERSION OF ASCII-ENCODED BINARY CHARACTERS TO AN 8-BIT BINARY NUMBER IN REGISTER C}

One of the simplest base-conversion routines is the ASCII-to-binary program. This program takes a string of ASCII-encoded ones and zeros from the console input buffer and produces an 8 -bit binary number in register \(C\). The hexadecimal equivalent of the number is printed on the console. If the operator types the string

10101100
the keyboard actually transmits the following sequence.

0110001
0110000
0110001
0110000
0110001
0110001
0110000
0110000
The conversion routine will take this combination, convert it to the binary number

10101100
and place it into the C register.
Type the routine shown in Listing 8.1 Set the assembly location somewhere below the monitor's stack and include the address of the monitor using the EQU directive. The monitor I/O routines are defined relative to the monitor's address.
```

L.stins 8.1. ASCIImencoded binars to bimars in C.
\& THIS FROGRAM IS DESIGNEN TO OFERATE

# WITH THE SYSTEM MONITOR AT 5800 HEX.

JAN 29, 80
ORG 5000H

# 

5800= MONTT EQU 5800H
5806 = OUTT EQU MONIT+6
580C = INFLN EQU MONIT\&OCH
580F = GETCH EQU MONIT+OFH
5812 = OUTHX EQU MONIT+12H
5000 3EOD
5002 CH0658
5005 3EOA
5007 C010658
500A CHOC58
5000 CH1E50
5010 CD1258
5013 3E20
5015 CNO658
;
STAFT: MUI AgODH \hat{OCAFFF RET}
CALL OUTT
MUI AgOAH कLINE FEEI
CALL OUTT
CALL INFLN कGET A LINE
CALL BBIN SCONUEFT
CALL OUTHX \hat{yEX VALUE}
MUI
Ag',
CALL OUTT
THE NEXT INSTRUCTION IS NEEREEI WHEN
THE FOUTINE IN LISTING 8.9 IS AFPENAEI
; CALL ETTS gBIN TO ASCII
JMFF START yNEXT UALUE
SURROUTINE TO CONUERT UF TO 8 AGCII-
ENCODELI BINARY CHAFIACTEFS INTO AN
8-BIT BINARY NUMBER IN C
\hat{y}

```
\begin{tabular}{|c|c|c|c|c|c|}
\hline 501 F & ES & BBIN: & FUSH & H & ¢SAUE FEGS \\
\hline 501 C & 210000 & & LXI & H:O & ¢CLEAR \\
\hline 501 F & CDOF58 & BBIN2: & CALL & GETCH & -GET CHAR \\
\hline 5022 & LIABASO & & JC & BEIN3 & GLINE ENI \\
\hline 5025 & 11630 & & SUI & '0' & ¢CONU TO E \\
\hline 5027 & IIA3550 & & JC & BEINA & ¢ ¢ 0 \\
\hline 502 A & FEO2 & & CFI & 2 & \\
\hline 502C & 123150 & & JNC & ERROR & ¢ \(\quad 1\) \\
\hline 502 F & 29 & & IIAII & H & © SHIFT LEF \\
\hline 5030 & B5 & & ORA & L. & ¢ AHM NEW C \\
\hline 5031 & 6F & & MOV & L. 9 A & \\
\hline 5032 & C31F50 & & JMF' & BEINS & ONEXT \\
\hline & & CHECK & \multicolumn{3}{|l|}{FOR BLANK AT END} \\
\hline 5035 & FEFO & EBINA: & CFI & (' \({ }^{\prime}\) & ) AND OFFH \\
\hline 5037 & C23150 & & JNZ & ERROR & ¢ NOT BLANK \\
\hline 503 A & 411 & EBIN3: & MOU & C, L & ¢8 BITS TO \\
\hline 503 B & E1 & & FOF & H & ¢RESTORE \\
\hline 5030 & C9 & & \multicolumn{3}{|l|}{RET} \\
\hline & & FRINT & \multicolumn{3}{|l|}{? ON IMFROFEF INFUT} \\
\hline 5031 & C1 & ERROR: & FOF & E & ¢FAISE STA \\
\hline 503 E & C1. & & FOF & E & \\
\hline 503 F & 3E3F & & MUI & Ag'? \({ }^{\prime}\) & \\
\hline 5041 & C10658 & & CALL & OUTT & \\
\hline 5044 & C30050 & & JMF' & STAFT & §TRY AGAIN \\
\hline
\end{tabular}

Assemble the program and load it into memory; start it up by branching to the beginning of the program, the address of START. The monitor prompt symbol of \(>\) will appear on the console. Test the routine by entering the following binary numbers. Be sure to add a carriage return to the end of each line.
```

>0 (you type this)
00 (prosram responds with this)
>1
01
>10
02 (binary 10 is heरadecimal 2)
211
03
201
O5 (binary 101 is hexadecimal 5)
>1111
OF
211110000
FO
210101010
AA

```

Of course, only ASCII zeros and ones are acceptable binary characters. Leading zeros are not necessary. If more than eight characters are entered, only the last eight are used. A question mark will be printed if a nonbinary
character is typed. Typing errors can be corrected with a backspace or DEL keys.

The program consists of three parts. The first and third parts will be common to other conversion programs in this chapter. The first part calls the monitor to obtain data from the console. The last part converts the data to the hexadecimal equivalent and prints it on the console if valid. If the entry is invalid, a question mark is printed.

The conversion routine occupies the middle portion of the program. It works as follows: Since HL is used as a working register, the original contents are first saved on the stack. While this step is not necessary in this case, it may be needed in a real application. The HL register is then zeroed.

As each new character is obtained from the input buffer, it is converted from ASCII to binary by subtracting 30 hex, the value of the ASCII zero. An ASCII zero, which has a value 30 hex, becomes a binary zero. Similarly, an ASCII 1, which has a value of 31 hex, becomes a binary 1.
```

0110000 ASCII zero
011 0000 Subtract ASCII zero
0000000 binary zero
0110001 ASCII 1
0110000 subtract ASCII zero
0000001 binars 1

```

A check is made at this point to ensure that an invalid character has not been typed. Only three characters are acceptable: An ASCII zero, an ASCII 1 , and a space. If the carry flag is set after the subtraction of an ASCII zero, then the input value was neither a zero nor a 1 . But it might be a space character. A jump is made to subroutine BBIN4 in this case. This routine determines whether the current character is a space or some other character. A space is the normal end-of-string character (delimiter); other characters are not.

Each character is also checked to see that it is not greater than an ASCII 1. In either case, if any character in the string is found to be other than an ASCII zero or 1 , then the subroutine is terminated with a jump to the error routine. At this point, the stack is raised with a POP instruction, and control returns to START at the top of the program.

If the input value is a zero or 1 , the procedure continues. The current value in the HL register is multiplied by two, the binary number base. This arithmetic shift left is accomplished by adding the HL register to itself with the double-precision add DAD H. An alternate method would be to place the sum in the accumulator. In this case the multiplication is performed with an ADD A instruction. But then the intermediate sum would have to be saved in another register while the new character was checked.

The new character, which is now a binary zero or 1 in the accumulator, is added to the value in HL. The addition of the 8 -bit accumulator to the 16 -bit HL register generally requires several steps.
1. Add \(L\) to A.
2. Move sum in A to L.
3. Increment H if carry is set.

But in this particular case, the carry flag will never be set. Consequently, a simpler method of addition can be used. The one chosen for this application is to perform a logical OR operation with the \(L\) register and the accumulator.

\section*{CONVERSION OF ASCII DECIMAL CHARACTERS TO A BINARY NUMBER}

We frequently find it useful to input computer data in the form of decimal numbers. We may then need a program to convert ASCII-encoded decimal numbers into binary form. The program given in Listing 8.2 will perform this task for us.



This new program uses our monitor for some of the necessary subroutines, just like the ASCII binary-to-binary program given in the previous section. Assemble the program, load it into memory, and branch to START. Again, the monitor prompt symbol \(>\) will appear. Try this routine by entering the following decimal numbers. Remember to type a carriage return at the end of each line.
```

>0 (you tywe this)
0000 (computer ressonse)
>
0001
10 (decimal 10)
OA (sives OA hex)
>16
OOOF
84
0100
>1024
O400
865545
FFFF
>65547
0002

```

If the input consists of valid decimal characters, then the response will be the corresponding hexadecimal value. If an invalid character is typed, a question mark is printed as an error message and the program is restarted.

Since this routine generates a 16 -bit binary number, the largest possible value is one less than 2 to the power 16. This is equivalent to a decimal number of 65,545 . If a larger number than this is entered, the excess over 65,545 is lost. Thus, an input of 65547 will give a value of 0002 . Remember that the monitor error-correction features and the control-P list toggle are available.

The algorithm is similar to the one in the previous section. The HL register pair is initially zeroed. The incoming character is converted from ASCII to binary, then checked to see that it is in the range 0-9. The current value is multiplied by 10 (the number base) prior to adding in the new character. The multiplication is accomplished with the double-register add instructions as follows.
```

MOU D,H (duFlicate H in D)
MOU E|L (duFlicate E in L.)
MAD H (double initial value)
DAll H (quadruple it)
DAII D (5 times initial value)
LIALI H (double, makiris 10 times
the initial value)

```

The total is first duplicated in the DE register. Two double-precision DAD H operations multiply the original value by 4 . Adding in the original value with the DAD D makes it 5. A final DAD H produces the desired multiplication by 10 .

If only an 8-bit binary number is needed, then the multiplication can be performed in the accumulator rather than in the HL register. This will free the HL register for some other use, such as a memory pointer. The 8 -bit version is given in Listing 8.3

\begin{tabular}{|c|c|c|c|c|c|}
\hline 500A & cnocs8 & & CALL & INFLL & ¢GET A LINE \\
\hline 5000 & C11650 & & CALL & DEIN & \% DEC TO BIN \\
\hline 5010 & Cu1258 & & CALL & OUTHX & \%HEX \\
\hline \multirow[t]{3}{*}{. 5013} & C30050 & & JMF' & Start & \\
\hline & & \[
\hat{y} \text { CONUER }
\] & T ASC & I I- Decimal & TO 8-BIT BINARY \\
\hline & & ; & & & \\
\hline 5016 & OEOO & DEIN: & MUI & C.O & acleafi c \\
\hline 5018 & CLOF58 & LBIN2: & Call & GETCH & gGET CHAFi \\
\hline 501 B & L8 & & Fic & & tLINE ENI \\
\hline 501 C & 1630 & & suI & '0' & ;CONU TO BINARY \\
\hline 501 E & 11.3250 & & JC & DEINA & ¢ < 0 \\
\hline 5021 & FEOA & & crid & 10 & \\
\hline 5023 & 123850 & & JNC & ERROR & \% \(>10\) \\
\hline 5026 & 57 & & MOU & II, A & gSAUE NEW \\
\hline 5027 & 79 & & mov & A, C & ¢Sum \\
\hline 5028 & 87 & & Alic & A & ¢TIMES 2 \\
\hline 5029 & 4F & & MOV & C.A & 9SAUE \\
\hline 502A & 87 & & ADS & A & ¢TIMES 4 \\
\hline 502 B & 87 & & AIID & A & -TIMES 8 \\
\hline 502 C & 81 & & Alli & c & -TIMES 10 \\
\hline \(502 \square\) & 82 & & Ang & 1. & ¢ COMBINE \\
\hline 502 E & 4F & & MOV & C.A & gSave in c. \\
\hline \multirow[t]{3}{*}{502 F} & c31950 & & JMF' & HEIN2 & INEXT \\
\hline & & ; & & & \\
\hline & & ; CHECK & FOR A & LANK AT ENI & \\
\hline 5032 & FEFO & UEINA: & CPI & ('...'0 & \(0^{\prime}\) ) AND OFFH \\
\hline 5034 & C23850 & & JNZ & ERROR & \#NOT BLANK \\
\hline \multirow[t]{2}{*}{5037} & C9 & & FET & & \\
\hline & & ; FRINT & ? 0 N & IMPROPER I & INFUT \\
\hline 5038 & F1 & ERROR: & Fof & FSW & \% RESTORE \\
\hline 5039 & 3E3F & & MUI & A, 'p' & \\
\hline 5038 & cn0658 & & CALL & OUTT & \\
\hline 503E & c30050 & & JMP & START & GTEY AGAIN \\
\hline 5041 & & ; & ENA & & \\
\hline
\end{tabular}

\section*{CONVERSION OF ASCII HEXADECIMAL CHARACTERS TO A 16-BIT BINARY NUMBER IN HL}

The development of a routine to convert a string of ASCII-encoded hexadecimal characters into a 16 -bit binary number will now be considered. This is the routine most frequently used in a system monitor. In fact, this was one of the first routines to be incorporated into our system monitor. Somewhere along the way there will have to be a multiplication by 16 , since this is the base of the hexadecimal number. The multiplication can be easily performed by shifting the results left by four bits. Shifting left one bit is equivalent to multiplying by 2 . Consequently, shifting by two bits performs a multiplication by 4 .

For the binary routine we considered first, only the characters 1 and zero were valid. In the decimal routine that followed, the range of valid
input was zero to 9 . The hexadecimal routine we will now consider is complicated by the fact that both the digits \(0-9\) and the letters A-F are valid.

Two separate algorithms will be considered; one produces an 8 -bit result, the other gives a 16 -bit result. The program given in Listing 8.4 is similar to the previous ones. It will convert a string of ASCII-encoded hex characters into a 16 -bit binary number in the \(\mathrm{H}, \mathrm{L}\) register pair. The doubleprecision add, DAD H , is used four times to perform the multiplication by 16 .



Each ASCII character is converted to binary in subroutine NIB. This routine subtracts an ASCII zero, then checks to see that the character is valid. If it was originally in the range of an ASCII zero to ASCII 9, it will now be converted to the binary number \(0-9\). If a hex character A-F was entered, it will be converted to binary form by the additional subtraction of 7. Of course, nonhex characters will produce the error message of a question mark.

Assemble the program, load it into memory, and start it up. Type the following series of hex numbers.
```

\$1
0001
>10
0010
A
OOOA
PFFFF
FFFF
>12345
2345 (only 1ast A characters used)

```

As with the other programs, leading zeros are not needed. If more than four characters are input, only the last four are used. Return to the monitor with a control-X.

\section*{CONVERSION OF TWO ASCII HEXADECIMAL CHARACTERS TO AN 8-BIT BINARY NUMBER IN REGISTER C}

In the previous section, HL was used to convert hex characters into a binary number. But, if the HL register pair is needed as a memory pointer, then the accumulator can be used for this conversion. In this case, however, only an 8 -bit binary number is produced. Listing 8.5 gives this version. Since the routine uses a fixed format, exactly two characters must be typed. This means that leading zeros must be entered.



The multiplication by 16 is performed in the accumulator by using four ADD A instructions. The ADD A instruction is equivalent to an arithmetic shift left. Data is moved from the lower four bits to the upper four, and fills the lower bits with zero.

Assemble the program shown in the listing, load it into memory, and try it out. Remember, for this version, exactly two hex characters must be entered.
```

>01
O1
210
10
>OA
OA
>12
1 2

```

If everything is all right, return to the monitor with a control-X.

\section*{CONVERSION OF ASCII OCTAL CHARACTERS TO A 16-BIT BINARY NUMBER IN REGISTER HL}

We did not use octal operations in the system monitor developed in Chapter 6 , yet they can be very useful in trying to understand 8080 assembly language instructions. From the 8080 instruction set in Appendix D, it can be seen that the registers are assigned values as shown in the following table.
\begin{tabular}{cl} 
register & \multicolumn{1}{c}{ value } \\
0 & B \\
1 & C \\
2 & D \\
3 & E \\
4 & H \\
5 & L \\
6 & memory \\
7 & A
\end{tabular}

Thus the register-move operations are obvious from the octal representation, but not from the hex or decimal form.
\begin{tabular}{ccccc} 
octal & hex & decimal & oferation \\
101 & 41 & 65 & MOU B,C \\
123 & 53 & 83 & MOU M,E \\
167 & 77 & 119 & MOU M,A
\end{tabular}

While octal numbers appear to be better than hexadecimal for expressing the 8080 operation codes, they leave something to be desired as memory pointers. The problem is that 16 -bit addresses must be considered as two 8 -bit bytes. But octal numbers represent groupings of three bits, and 8 is not evenly divisible by 3 . An address of FFFF hex is equivalent to 177777 octal. But if this address is stored in two consecutive bytes, each byte will contain FF hex or 377 octal. This peculiarity of octal has given rise to the expression "crazy octal." A value of FFFF hex is \(377: 377\) crazy octal.
\begin{tabular}{rrl} 
hex & octal & crazy octal \\
FF & 377 & \(000: 377\) \\
FFF & 7777 & \(017: 377\) \\
FFFF & 77777 & \(177: 377\) \\
FFFF & 177777 & \(377: 377\)
\end{tabular}

Assemble the program, load it into memory, and try it out. The octal numbers input to this routine can be in the range of 0 to 177777. Try various octal numbers.
```

>0
0000
>10
0008
>20
0010
2177
007F
277
OOFF
>400
0100
>123456
A72E
>200000 (too bis)
0000

```

\begin{tabular}{|c|c|c|c|}
\hline ¢ FRINT & \(?\) ON & IMFRROFEF & INFUT \\
\hline \multicolumn{4}{|l|}{;} \\
\hline ERROR: & POF & H & 乡FiAISE STACK \\
\hline & FOF & H & \\
\hline & MUI & Ay' \({ }^{\prime}\) & \\
\hline & CALL & QUTT & \\
\hline & JMF' & STAKT & gTRY AGAIN \\
\hline
\end{tabular}

This routine will convert a string of ASCII-encoded octal characters into a 16 -bit binary number in the HL register pair. The current value in the HL register pair is multiplied by 8 (the number base) by performing three DAD H instructions. The new byte is converted from ASCII to binary by subtracting an ASCII zero. It is checked at this time to ensure that it is in the proper octal range of 0 to 7 . The addition of the new digit to the present value is more complicated than it was for the binary or hex routines. The problem is that there can be a carry out from the low-order byte. For this reason, the new byte is placed into the DE register pair, then combined with the value in HL by using the double-precision DAD D instruction.

\section*{CONVERSION OF THREE ASCII OCTAL CHARACTERS TO AN 8-BIT BINARY NUMBER IN REGISTER C}

The routine given in Listing 8.7 will convert exactly three ASCII-encoded octal characters into an 8 -bit octal number in register C . The routine is programmed for fixed-format input; therefore, exactly three characters must be given. Assemble the program, load it into memory, and start it up. Type in the following octal numbers, including the leading zeros.
```

200
OO
210
08
>020
10
2177
7F
>377
FF

```

Since the largest 8 -bit number is 255 decimal or 377 octal, the first digit must be in the range \(0-3\). The remaining two digits must be in the range \(0-7\). A check is made to ensure that the characters are in the proper range. The first ASCII character in the input string is converted to binary by subtracting an ASCII zero. The result is multiplied by 8 with three ADD A instructions and the result is saved in the C register. The next character is converted to binary and added to the first with the ORA C instruction. The new sum is multiplied by 8 again with three ADD A instructions, then saved in the C register. Finally, the third character is converted to binary and added in. The final result is moved to the C register.

Listins 8.7. ASCII octal 8-bit bimary in C.


\begin{tabular}{|c|c|c|c|c|c|}
\hline 5040 & FE08 & & CFI & 8 & \\
\hline 5042 & 124650 & & JNC & ERFE & STOO LAFGE \\
\hline 5045 & c9 & & RET & & \\
\hline & & FRINT & ? ON & IMFRKOPEF & TNFUT \\
\hline 5046 & C1 & ERR2: & FOF & B & ¢FATSE STACK \\
\hline 5047 & C1 & ERROR: & POF' & B & \\
\hline 5048 & 3E3F & & MUI & Ag'?' & \\
\hline 504 A & c[10658 & & CALL & OUTT & \\
\hline 5041 & c30050 & & JMF' & START & ¢TRY AGAIN \\
\hline
\end{tabular}

\section*{CONVERSION OF TWO ASCII BCD DIGITS TO AN 8-BIT BINARY NUMBER IN REGISTER C}

The binary coded decimal (BCD) notation was introduced in Chapter 2. This method of encoding is less efficient than the binary notation. It takes more memory space to encode numbers, and mathematical operations can be considerably slower. The BCD notation, however, has two advantages. One is that conversion from decimal to BCD is simpler than conversion from decimal to binary. The second advantage is freedom from round-off error.

The conversion routine given in Listing 8.8 accepts exactly two ASCIIencoded decimal digits and converts them into an 8-bit BCD number in the C register. The routine can be repeatedly called to convert numbers with more than two characters.
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{4}{*}{}} & \multicolumn{2}{|l|}{\begin{tabular}{l}
; THIS FROGRAM IS \\
; WITH THE SYSTEM
\end{tabular}} & \multicolumn{3}{|l|}{\begin{tabular}{l}
5 DESIGNED TO DFERATE \\
M MONITOR AT 5800 HEX
\end{tabular}} \\
\hline & &  & & \multicolumn{3}{|l|}{M MONITOR AT 5800 HEX} \\
\hline & & \multicolumn{5}{|l|}{\% JAN 13, 80} \\
\hline & & \multicolumn{5}{|l|}{㐫} \\
\hline 5000 & & ORG & \multicolumn{4}{|l|}{\multirow[t]{2}{*}{5000 H}} \\
\hline & & \$ & & & & \\
\hline 5800 & \(=\) & MONIT & EQU & \multicolumn{3}{|l|}{5800 H} \\
\hline 5806 & \(=\) & OUTT & EQU & \multicolumn{3}{|l|}{MONITt6} \\
\hline 580 C & \(=\) & INFLN & EQU & \multicolumn{3}{|l|}{MONITHOCH} \\
\hline 580 F & \(=\) & GETCH & EQU & \multicolumn{3}{|l|}{MONITHOFH} \\
\hline 5812 & \(=\) & OUTHX & EQU & \multicolumn{3}{|l|}{\multirow[t]{2}{*}{MONIT+12H}} \\
\hline & & \% & & & & \\
\hline 5000 & 3EOL & \multirow[t]{5}{*}{STAFT:} & MUI & AgOLIH & ¢CAFEF & RET \\
\hline 5002 & c00658 & & CALL & OUTT & & \\
\hline 5005 & 3EOA & & MUI & \(A, O A H\) & - LINE & FEEI \\
\hline 5007 & CH0658 & & CALL. & OUTT & & \\
\hline 500 A & cnocs 8 & & CALL & INFLN & ¢GET A & A LINE \\
\hline 5001 & ca2050 & \multirow[t]{6}{*}{FIDHLS:} & CALL & HEX2 & - LEFT & CHAF \\
\hline 5010 & 87 & & Allil & A & STIMES & \\
\hline 5011 & 87 & & AlII & A & -TIMES & \\
\hline 5012 & 87 & & Alum & A & TTIMES & \\
\hline 5013 & 87 & & Allo & A & TTIMES & 16 \\
\hline 5014 & 4F & & MOV & \(C, A\) & ¢GAVE & \\
\hline
\end{tabular}


With the BCD notation, there is a \(2: 1\) correspondence between the number of BCD digits and the necessary number of bytes. Or, put another way, two decimal digits are stored in each byte. This arrangement is sometimes called packed decimal. The right decimal digit is encoded in the loworder four bits and the left digit is encoded into the high-order four bits.
\begin{tabular}{lll}
38 & 0011 & 1000 \\
27 & 0010 & 0111 \\
59 & 0101 & 1001
\end{tabular}

BCD encoding involves essentially the same steps as does the hex-to-binary routine, except that only the characters 0 through 9 are allowed. The bit patterns corresponding to the hexadecimal numbers A through F are not allowed.

\section*{CONVERSION OF AN 8-BIT BINARY NUMBER IN C TO A STRING OF EIGHT ASCII BINARY CHARACTERS}

In the first part of this chapter we developed programs to convert strings of ASCII-encoded characters into binary numbers. The programs in the following sections will perform the reverse operation. Binary numbers will be converted into strings of ASCII-encoded characters. Furthermore, we will combine the new routines with those already developed so that they may be more easily tested.

The program shown in Listing 8.9 can be used to convert an 8 -bit binary number in register C into eight ASCII-encoded binary characters. The resulting characters are sent to the console in this case, but they could be
placed into sequential memory locations instead. This routine is incorporated into the system monitor developed in Chapters 6 and 7.


Make a duplicate copy of the source program shown in Listing 8.1. This routine was used to convert ASCII-encoded binary characters into an 8-bit binary number in C. Remove the semicolon from the instruction that reads

\section*{\(\therefore\) CALL EITS \(\quad\) BIN TO ASCII}

Also delete the END directive if you used one. Add the lines given in Listing 8.9 to the end of the program.

The new routine works in the following way. Register B is initialized with the value of 8 , the number of bits to be generated. Register C begins with the original binary byte. The bits of this byte are shifted to the left one at a time into the carry flag. The carry flag is then added to an ASCII zero to produce a 0 or a 1 at the console. For the 8080 version, the byte is moved to the accumulator, shifted left with an add instruction, then returned to register C.

If the current high-order bit is a zero, then the carry flag is reset and a zero is printed. If the current high-order bit is a 1 , then the carry flag is set and a 1 is printed. The count in the B register is decremented after each character is printed. When the count reaches zero, the process is terminated.

Notice that the addition of the carry flag to the ASCII zero could have been accomplished with the instructions
```

MUI A,'O'
ACI 0

```

However, this will require four bytes. The code we will use, which is not so obvious, requires only three bytes.
```

MVI A,'0'/2
ADC A

```

If you have a Z-80 CPU, this routine can be simplified and shortened by three bytes. Performing the rotation directly in the \(C\) register reduces the program by one byte. Two additional bytes are gained by using the decrement B, jump-not-zero operation. Now the accumulator can be zeroed with an exclusive-or operation and the carry can be added directly to an ASCII zero.
\begin{tabular}{|c|c|c|c|}
\hline BITS: & LII & B,8 & ¢ 8 BITS \\
\hline \multirow[t]{6}{*}{BIT2:} & XOR & A & QZERO A \\
\hline & SLA & \(L\) & ¢SHIFT L LEFT \\
\hline & ADC & \(\mathrm{Ag}^{\prime} \mathrm{O}^{\prime}\) & \# AMM CARRY TO O \\
\hline & CALL & OUTT & ¢SEND \\
\hline & D.JNZ & BIT2 & ¢ 8 TIMES \\
\hline & RET & & \\
\hline
\end{tabular}

Assemble the combined program, load it into memory, and start it up. Be sure that the monitor is in place at the address of MONIT. The new binary-to-ASCII binary routine has been added in addition to the original binary to ASCII hex in the system monitor (OUTHX). Consequently, each number will now be rendered in both hex and binary. Type in the following binary numbers.
```

>0 (sou type this)
00 00000000 (both hes and binary are siven)
>1
0 1 0 0 0 0 0 0 0 1
\$101
05 00000101
\$10101010
AA 10101010
>11110000
FO 11110000

```

Remember that the error-correction features of the monitor are available. If you inadvertently type a control-X, you will end up in the monitor itself. You can return from the monitor to the new program, however, by typing
```

65000

```
if this is where you assembled the new routine.

\section*{CONVERSION OF AN 8-BIT BINARY NUMBER INTO THREE ASCII DECIMAL CHARACTERS}

An 8-bit binary number can be converted into a string of ASCII-encoded decimal characters by repeated subtraction of powers of 10 , the number base. The corresponding decimal number will lie in the range of zero to 255 . The value of 100 (decimal) is repeatedly subtracted from the original binary number until the result becomes negative. One less than the number of subtractions is the number of hundreds in the decimal form. The result, which in this case can only be 0,1 , or 2 , is added to the value of an ASCII zero, then sent to the console.

As an example of the 100s subtraction, consider the number 137.
\[
\begin{array}{r}
137 \\
\frac{-100}{37} \\
\text { (one subtraction) } \\
\frac{-100}{\text { (negative number) }} \text { (too many) }
\end{array}
\]

Since there was one subtraction of 100 before the number became negative, the number is in the range 100 to 199.

The value of the last 100 is added back to make the number positive again. Then the value of 10 is repeatedly subtracted from the new value until a negative result is again obtained. The number of tens in the decimal form is one smaller than the number of subtractions. This count is added to an ASCII zero and sent to the console for the middle digit. The value of ten is added back to the remainder. This adjusted remainder is then added to an ASCII zero to produce the units digit. It too is sent to the console.

Continuing with the example:
\begin{tabular}{ll} 
(negative number) \\
+100 & (add back last 100) \\
\(\frac{37}{-10}\) & (first subtraction) \\
\hline 27 & \\
\(\frac{-10}{17}\) & (2nd subtraction) \\
\(-\frac{10}{7}\) & (3rd subtraction) \\
\(\frac{-10}{}\) & (too many) \\
(negative number) \\
+10 & (add back last 10) \\
\hline 7 & (units)
\end{tabular}

Since there were three subtractions of 10 before the remainder became negative, the middle digit is a 3 . Finally, the rigkt digit is 7 , the remainder after the last subtraction of 10 .

Lisiting 8.10 gives the instructions for the conversion of an 8 -bit binary number in register H. Register D initially contains the value of 100 (decimal) that is to be repeatedly subtracted from the number in H . As soon as the result of the subtraction becomes negative, the last 100 is added back, and the value in D is changed to a 10 by subtraction of 90 . Register C is used to count the number of subtractions. It is initialized with the value of one less than an ASCII zero to simplify the conversion.
```

Listins 8.10. Birary in A to ASCII Secimal.

```
















































There is an additional feature added to this routine: leading-zero suppression. Leading zeros are typically suppressed when a number is expressed
in decimal form. On the other hand, leading zeros are commonly left in place for binary, octal, and hexadecimal numbers. Thus, we write
\[
1
\]

2
18
197
207
for decimal numbers, but
\[
\begin{aligned}
00001111 & \text { (binary) } \\
040 & \text { (octal) } \\
0 \text { FE3 } & \text { (hexadecimal) }
\end{aligned}
\]
for the others.
One reason for keeping leading zeros is to make it easier to distinguish octal or hex numbers from decimal numbers. With this convention, the number 0137 would be interpreted as an octal or hex value rather than a decimal number. The suppression of leading zeros is not a difficult task, but it does require some additional code. It is not sufficient to merely remove all zeros, for then the number 0307 becomes 37.

One technique is to utilize a zero-suppression flag which is initially reset. Zeros are omitted as long as the flag remains reset. Then the flag is set when the first nonzero character is encountered. Subsequent zeros are not removed since the flag is set.

The necessary zero-suppression code has been included in the routine shown in Listing 8.10. Register E is used for the flag; it is initially reset. Then each character is checked with a CPI ' 1 ' instruction to see if it is an ASCII zero. If the value is not a zero, it is printed and the flag is set to FF hex. On the other hand, if the digit is a zero, the flag is checked. If it is found to be reset, the zero is not printed. Only three decimal characters can be produced from the original byte; consequently, just the first two need to be checked. If the value of the byte is zero, a single ASCII zero is printed.

The B, C, D, and E registers are utilized in the operations. Consequently, the original values are initially saved on the stack, then restored at the conclusion of the routine.

Duplicate the program shown in Listing 8.4, the ASCII-hex to binary routine. Keep one of the copies as a backup, then rename the other one HEXDEC.ASM. Remove the semicolon at the beginning of the line

\section*{; CALL DECB}
and remove the END directive at the end of the program. Add the lines given in Listing 8.10. Assemble the combination program, load it into memory, and start it up by branching to the address of START. We have coupled the 16 -bit hex input program with the 8 -bit decimal output program. Consequently, only the high-order byte will be converted to decimal. This is the
byte in the H register. Try the combined program with the following hex numbers.
```

>0
0000 0
>1
0001 0
\$100
0 1 0 0 1
AOO
OAOO 10 (hex A is decimal 10)
>1000
1000 16 (10 hex is 16 decimal)
\triangleFFFF
FFFF 255 (FF hex is 255 decimal)

```

This binary-to-decimal routine can be very useful at the CP/M systems level. Suppose that you want to save a program that starts at 100 hex and runs to 2736 hex. If the decimal routine is incorporated into a hexadecimal math routine of the system monitor, you have only to type
```

2H2800 100 (command)
2900270039 (response)

```

The response of 39 is the decimal number of 256 -byte blocks to be saved. Then you can give the CP/M command

A SAVE 39 FILENAME.EXT

\section*{CONVERSION OF A 16-BIT BINARY NUMBER INTO FIVE ASCII DECIMAL CHARACTERS}

In the previous section, we developed a routine to convert an 8 -bit binary number into three ASCII-encoded decimal characters. We will now write a routine for converting a 16 -bit binary number in HL into 5 ASCII-encoded decimal characters. This double-precision decimal number will range from zero to 65,535.

Duplicate the decimal-to-16-bit binary program in Listing 8.2. Remove the semicolon from the line
```


# CALL TBIN

```
and the END directive if you used one. Add the program shown in Listing 8.11 to the end.

Listins 8.11 Einary in HL to ASCII decimal.
```

* THIS FROGRAM IS DESIGNED TO RUN WITH
; THE SYSTEM MONITOR ANM WITH THE
    * FFROGRAM SHOWN IN L.ISTING 8.2
FER 22,79
FRINT BINARY NUMEER IN H:L AS ASCII
HECIMAL HIGITS. LEALING ZEFO SUFFRESSED.
%
BINII: MUI E:O \hat{LEADING O FLAG}
LXI IM-10000 %2'S COMFLL
CALL SURTR \$10 THOUS
LXI IV.-1000
CALL SUBTF \&THOUS
LXI IM-100
LXI LI,-100
LXI LI,-10
MOU AyL AMI ASCIIESAS
MDU AyL ANI ASSCIIESAS
IMF OUTT FUNITS
\&}\mathrm{ SUBTRACT FOWER OF TEN ANI COUNT
\hat{0}
SUBTF: MUI Cy'O'-1 gASCII COUNT
SUBT2: INR C
DALI I ADIN NEG NUMEEF
JC SUBT2 SKEEF GOTNG
%


# ONE TOO MANY, ALILI ONE EACK

| MOV | A 01 | OCOMFLEMENT |
| :---: | :---: | :---: |
| CMA |  | ) DIE |
| MOU | 10, A |  |
| MOU | A,E |  |
| CMA |  |  |
| MOU | EgA |  |
| INX | D | SAND |
| IIALI | D | ¢AMLI BACK |
| MOV | A, C | AGET COUNT |

%
; CHECK FOR ZERO
CFI '1' tLESS THAN 1?
JNC NZERO INO
MOV AgB 献HECK O FLAG
ORAA A \hat{SET?}
MOU A,C कRESTOFE
FZ \#SKIF LEADING O
JMF OUTT SINTEFIOR ZERO
\
; SET FLAG FOF NON-ZERO CHARACTER
5091 O6FF NZERO: MUI B,OFFH $\$$ SET O FLAG
JMF OUTT \&FRINT IT
END

```
5075 OE2F
5077 OC
507819
5079 凹A7750
507 C 7 A
507 D 2 F
507E 57
\(507 F 7 B\)
50802 F
5081 5F
508213
508319
508479
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 508 \mathrm{C} & \mathrm{CB} \\ 508 E & \mathrm{C} 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 508 \mathrm{C} & \mathrm{CB} \\ 508 E & \mathrm{C} 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 5080 & C 8 \\ 508 E & C 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 508 \mathrm{C} & \mathrm{CB} \\ 508 E & \mathrm{C} 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 508 \mathrm{C} & \mathrm{CB} \\ 508 E & \mathrm{C} 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 1229150 \\ 508 A & 78 \\ 508 B & 87 \\ 508 C & 79 \\ 5080 & C 8 \\ 508 E & C 30658\end{array}\)
\(\begin{array}{ll}5085 & \mathrm{FE} 31 \\ 5087 & 129150 \\ 508 \mathrm{~A} & 78 \\ 508 \mathrm{~B} & \mathrm{B7} \\ 508 \mathrm{C} & 79 \\ 508 \mathrm{C} & \mathrm{C8} \\ 508 \mathrm{E} & \mathrm{C} 30658\end{array}\)
\(\begin{array}{ll}5055 & 0600 \\ 5057 & 11 \text { FOLI }\end{array}\)
\(\begin{array}{ll}5057 & 11 F 0108 \\ 505 A & \text { Cп7550 }\end{array}\)
505 D 1118 FC
\(5060 \quad \mathrm{C} 17550\)
5063119 CFF
5066 C117550
506911 FGFF
506 C C117550
506 F 7 D
\(5070 \quad \mathrm{C} 630\)
5072 C30658
5093 C30658
5096

This 16 -bit version is similar to the 8 -bit version of the previous section. This time we start with the subtraction of the decimal value 10,000 instead of 100 . The number of subtractions is counted as before. When the result becomes negative, the last 10,000 is added back. The number of subtractions that was performed is the desired digit for the ten-thousandths position.

Since the 8080 CPU does not incorporate a 16 -bit subtraction operation, the subtraction is obtained by adding the corresponding two's complement
```

LXI Mg-10000

*     - "
- . .
MAD ID

```

The carry flag will be set for each addition (subtraction) except the last. The carry flag is then reset for the operation corresponding to the result becoming negative. The JC instruction in subroutine SUBTR causes the computer to loop the correct number of times. Suppose, for example, that the binary number in HL corresponds to the decimal number 32,128 . This is the equivalent of the hexadecimal value 7D80. The two's complement of 10,000 is D8F0 hex. The sum of these two is
\begin{tabular}{cc} 
decimal & hexadecimal \\
32.128 & 7 m80 \\
-10.000 & +10850 \\
-22.128 & 5670
\end{tabular}

Thus the addition of 7D80 and D8F0 hex is equivalent to subtracting 10,000 from 32,128 .

The last subtraction that causes the result to become negative has to be undone. This could be accomplished by adding 10,000 . However, the addition is accomplished in subroutine SUBTR which is also used to add back the \(1,000,100\), and 10 for the equivalent steps of each decade. Therefore, we won't know, in general, which value to add. The solution is to obtain the necessary value from the two's complement of the two's complement for the current value. This two's complement is first obtained by complementing both the D and the E register to produce the one's complement. Then the DE register pair is incremented. Subroutine SUBTR is first called with DE set to \(-10,000\), then to \(-1,000,-100\), and -10 . At this point, the units digit is contained in the \(L\) register.

This double-precision routine also incorporates instructions for suppressing leading zeros. The approach is similar to the one used in the previous section except that the \(H\) register is used for the zero flag.

Assemble the combination program, load it into memory, and start it up. Enter the following decimal numbers. The response will include both the hexadecimal and the decimal values of the input number.
```

>0
0000 0
>
0 0 0 1 1
>100
0064100
>1024
0400 1024
>65535
FFFF}6553

```

At this point you may want to incorporate decimal numbers into the system monitor. When we incorporated an ASCII-input feature into the monitor we used the apostrophe to indicate this fact. It is customary to precede decimal numbers by a number sign. For example, the following input would indicate decimal input.

2H昔1024 200

\section*{CONVERSION OF AN 8-BIT BINARY NUMBER INTO TWO ASCII HEXADECIMAL CHARACTERS}

The conversion of an 8-bit binary byte into two ASCII-encoded hexadecimal characters is an interesting exercise. The high-order four bits are represented by one hex character, and the low-order four bits are represented by the other hex character. Since the upper character is printed first, the upper four bits are rotated down to the lower position. These new lower four bits are converted to ASCII to produce the first character. Then the original loworder four bits are converted to ASCII to get the second character.

The nibble conversion appears to be straightforward. The upper four bits are zeroed by performing a masking AND with the value of 0 F hex. The lower four bits are then converted to ASCII by the addition of an ASCII 0. If the result is in the range \(0-9\), then the conversion is complete. Otherwise, a binary 7 is added to the result, converting it to an ASCII-encoded letter of A through F .

To see why this conversion works, look at the ASCII table in Appendix A. The ASCII number 9 has a decimal value of 57 . The ASCII letter A has a decimal value of 65 . But the hexadecimal value of \(A\) follows the value of 9 . Therefore, we need to add 7 to any valid hex number larger than 9 to convert it into the appropriate ASCII letter A through F.

The program shown in Listing 8.12 will convert an 8 -bit binary number in the C register into two ASCII characters and send them to the console. Duplicate the program in Listing 8.5. Remove the external reference to subroutine OUTHX near the beginning.

\section*{OUTHX EQU MONIT+12H}

Our new program will perform the same function. Also remove the final END directive if you used one. Copy the lines from Listing 8.12 on the end of the program. Assemble the combined program, load it into memory, and
start it up. Our monitor will still have to be in memory since we will need the I/O routines. This current version, Listing 8.12 , with the built-in binary-to-hex routine, should respond exactly the same as the earlier version, Listing 8.5. The only difference is that we are converting binary to hex within the program rather than using a routine in the monitor.


The algorithm used to convert the binary nibble to a hex character clearly demonstrates the technique. But there is a more efficient method for CPUs such as the 8080 and Z-80 that incorporate the decimal adjust accumulator (DAA) instruction. Change the second, third, fourth, and fifth lines of subroutine HEX1 so the subroutine looks like
\begin{tabular}{|c|c|c|c|}
\hline HEX1: & ANI & OFH & (same) \\
\hline & All I & 9OH & (new) \\
\hline & DAA & & (rew) \\
\hline & ACI & 4 OH & (new) \\
\hline & IAA & & ( Hew) \\
\hline & JMP & OUTT & (same) \\
\hline
\end{tabular}

Conversion of a 16 -bit binary value into four hex characters is obtained by calling the 8 -bit routine twice. For example, the HL register pair can be printed with the following routine.
\begin{tabular}{|c|c|c|}
\hline OUTHL: & MOU & \(\mathrm{C}, \mathrm{H}\) \\
\hline & call & OUTHX \\
\hline & MOU & \(\mathrm{C}, \mathrm{L}\) \\
\hline & CALL & OUTHX \\
\hline
\end{tabular}

Conversion of a binary number to a string of ASCII-encoded BCD characters does not require a special routine. It is performed simply by calling the binary-to-hex routine OUTHX.

\section*{CONVERSION OF A 16-BIT BINARY NUMBER INTO SIX ASCII OCTAL CHARACTERS}

A 16-bit binary number in the HL register pair can be converted into six ASCII-encoded octal characters by repeatedly shifting the double register to the left. We make use of the double-register add instruction DAD H. This instruction adds the register pair HL to itself. The operation is equivalent to a double-precision arithmetic shift left. All 16 bits are shifted left and a zero is moved into the lowest order bit. The carry flag is set if the original highestorder bit was a logical one. The carry bit is reset otherwise.

The routine is shown in Listing 8.13. As the bits of the double register are shifted out the high end, they are converted to the corresponding octal number in the accumulator. The largest 16 -bit octal number is 177777; consequently, the first octal character (starting from the left) can only be a zero or a one. The remaining five characters can range from zero through 7. They are obtained from groups of three bits.
```

Listins 8.13 Biramy in HL to ASCII octal.
\# THIS FROGRAM IS DESIGNED TO RUN WITH
5052 E5
5053 C5
5054 0605
5 0 5 6 ~ A F
505729
5058 CE3O
505A CN0658
5051 3E06
505F 29
5060 17
506129
5062 17
5063 29
5064 17
5065 C00658
5068 05
5069 C25450
506C C1
5060 E1
506E C9
506F

```

The first step shown in Listing 8.13 saves the HL and BC registers on the stack. This operation may not always be necessary. The XRA operation is used to zero the accumulator. It must be performed before the DAD H instruction since it resets the carry flag. The DAD instruction will set the carry flag if the high-order bit was a 1 , or reset the flag if the high-order bit was a zero. The carry flag is then added to an ASCII zero and sent to the console.

The remaining five digits are generated in a loop starting at label OCT2. Register B is preloaded with the value of 5 to count the remaining digits. We need to transfer the current three high-order bits from the H register into the accumulator. This is accomplished by three DAD H instructions. After each one, the carry flag will reflect the state of the most recent high-order bit of H. After each DAD instruction, we perform a rotate accumulator instruction. This moves the carry bit into the low-order bit of A. After three such operations, the three low-order bits of the accumulator will contain the proper octal bit pattern for the appropriate character. But they are in binary form and we need to convert them to ASCII for printing.

The bit pattern for the ASCII zero is 0110000 . Notice that it contains zeros in the lower four bit positions. At the beginning of the OCT2 loop we preloaded the accumulator with a binary 6 which has a bit pattern of 000 0110. At the conclusion of the OCT2 loop, the three rotations will convert this binary 6 into a 60 octal which is equivalent to an ASCII zero. This effectively converts the three lower-order bits, shifted in from the carry flag, into ASCII-encoded octal.

The Z-80 version can be a little shorter if the instruction
DJNZ OCT2
is used in place of
DCR B
JNZ OCT2

\section*{CONVERSION OF AN 8-BIT BINARY NUMBER INTO THREE ASCII OCTAL CHARACTERS}

In the previous section we derived a subroutine for the conversion of a 16 -bit binary number into ASCII characters. The conversion of an 8-bit binary number to octal will be considered here. We could use the H,L double register, as previously, to perform the necessary shifts. However, if the H,L register is needed for something else, such as a pointer to memory, then another method would be better.

The routine shown in Listing 8.14 performs the needed rotations in the accumulator. The original binary byte is in the C register. The byte is moved to the accumulator and two left circular rotate instructions are performed. This effectively moves the two high-order bits down to the two low-order
positions. It is equivalent to performing six right circular rotations. The remaining bits are zeroed with a logical AND 3 step. The ubiquitous ASCII zero is added, and the result is sent to the console.

The middle character is obtained by rotating the original byte to the right. A logical AND 7 isolates these low-order bits. The ASCII zero is added and the byte is sent to the console. The original byte is retrieved a third time. Now the three bits of the third character are properly positioned. Hence no rotation is needed. The masking AND operation is still needed, however. Finally, the ASCII zero is added prior to printing.

Type the program shown in Listing 8.14. Add the new program to the end of the octal-to-binary program shown in Listing 8.7. Assemble the combination, load it into memory, and branch to the beginning. Remember that the input requires exactly three octal characters. If less than three are used, an error message of a question mark will be printed. If more than three characters are typed, only the first three will be used.
```

Listins 8.14. 8-bit bimary in C to ASCII
% THIS FFOGFAM IS NESIGNED TO RUN WITH
; THE SYSTEM MONITOF ANI WITH THE
* FROGRAM SHOWN IN LISTING 8.7
JAN 22. 80
* ROUTINE TO OUTFUT AN 8-BIT BINAFIY
; VALUE AS THREE OCTAL CHARACTEFS
505379 OCT: MOU A,C GGET IT
5054 07
5055 07
5056 E603
5058 C06550
505B79
505C OF
505I OF
505E OF
505F C06350
506279
5063 E607
5065 C630
5067 C30658
506A

```


\section*{CONVERSION OF A 16-BIT BINARY NUMBER TO SPLIT OCTAL}

Some of the 8080 and Z-80 instructions can have either 8 -bit or 16 -bit operands. Typical 8-bit operations for the 8080 are
```

MUI Ag10
AIII 3
ANI 7

```

The 16 -bit operations include
\begin{tabular}{ll} 
CALL & 100 H \\
JMP & 5005 H \\
LXI & \(\mathrm{H}, 0\)
\end{tabular}

But the 8 -bit architecture of microcomputers means that 16 -bit operands are stored as two consecutive bytes. Each byte can be represented as two hexadecimal characters. And the entire 16 -bit value can be represented by a combination of all four of these hex characters. For example, the 16 bits

1111000010101010
can be represented with the hex characters
FOAA
Alternately, the left byte can be represented by an F0 hex, and the right byte can be expressed as AA hex. There is no problem here since each hex character represents four bits, and both 8 and 16 are evenly divisible by 4 .

Octal representation is more complex. In this case, each octal character represents three bits (or sometimes two). Since neither 8 nor 16 is evenly divisible by 3 , a problem can occur. Consider the 16 -bit value

1111010011101010
It can be represented in the octal notation as
172352

This is the result that the program in Listing 8.13 would produce at the system console. The problem is that the 16 bits are actually stored in two adjacent 8 -bit locations. If the bit pattern is grouped into 8 -bit bytes, it looks like this.
\[
\begin{array}{llllll}
11 & 110 & 100 & 11 & 101 & 010
\end{array}
\]

In this arrangement, the two corresponding octal bytes are represented as
364352
The result, which has been termed split octal or crazy octal, looks very different from the corresponding 16 -bit octal value of 172352 . The two octal bytes of split-octal notation are sometimes separated by a colon to distinguish the representation from the regular 16-bit octal.

The split-octal notation can be readily implemented, as shown in Listing 8.15. This program is adapted from the 8 -bit octal-to-binary and binary-to-octal routines given in Listings 8.7 and 8.14. The first part takes two separate octal bytes and converts them to an 8 -bit binary number. The second part converts the binary byte into two octal bytes. Each split-octal number is entered from the console as two groups of three characters. A space or colon can be used to separate the two parts.


\begin{tabular}{|c|c|c|c|c|c|}
\hline 5081 & 79 & & MOV & A \(\quad \mathrm{C}\) & \%RIGHT EITS \\
\hline 5082 & E607 & OCT2: & ANI & 7 & ¢3 EITS \\
\hline 5084 & C630 & 0CT3: & AlII & '0' & \%ASCII BIAS \\
\hline 5086 & c30658 & & JMF' & outt & ¢FRINT \\
\hline & & ; & & & \\
\hline 5089 & & & END & & \\
\hline
\end{tabular}

The input number is converted into a 16 -bit binary number in the \(\mathrm{D}, \mathrm{E}\) register pair by calling the 8 -bit routine twice. The hex value is printed out as usual, then the split-octal version. A colon in the middle separates the two halves.

Assemble the program and try it out.
```

\$177 377 (a space sefarator)
7FFF 177:377
>100:200 (a colon sefarator)
4080 100:200

```

This completes the base-conversion routines. At this point, you may want to incorporate some of these routines into your system monitor.

\section*{CHAPTER NINE}

\section*{Paper Tape and}

\section*{Magnetic Tape Routines}

It is possible to encode complete programs, such as a BASIC interpreter, into ROM so that calculations, such as the square root of 19 , can be performed as soon as the computer is turned on. But more complicated problems will require a source program. If the source program is used frequently, then it would be inconvenient to reenter the source program each time it is needed. One way to avoid this reentry problem is to save the source program somehow and then reload it into the computer when it is needed.

But BASIC is not the only computer language. Some tasks are more easily performed with other languages, such as Pascal or APL. Assembly language is useful for systems programming. A full text editor program has more features than the most complex BASIC interpreter. Thus, it is better not to have the BASIC interpreter in ROM. Instead, a small monitor program, such as the one developed in Chapter 6, can be placed in ROM. We can use this small monitor to load larger programs from an external medium.

The floppy disk is a convenient medium for saving and reloading programs. The cost, however, is greater than other storage media such as paper tape or magnetic tape. Even if a floppy-disk system is utilized for program storage, it might be wise to make backup copies on magnetic or paper tape.

The simplest storage method is to utilize the paper tape accessory available on some Teletype machines. With this approach, a separate computer I/O port is unnecessary. Furthermore, paper tapes can be read directly on the Teletype, without using a computer. The disadvantage of this method is that the transfer rate is low, since the Teletype operates at only ten characters per second.

A more complicated, but faster, method utilizes an ordinary magnetic tape machine designed for home recording. In this case a separate I/O port will usually be necessary, but the advantage is that the recording rate is higher than for paper tape. Common data transfer rates range from 30 to over 120 characters per second.

The frequency response of audio tape recorders is limited to a maximum of 10 to 20 kHz . But since the computer operates at 2 or 4 MHz , the signals from the computer cannot be directly copied onto tape.

One solution is to convert the computer's digital signals into sine waves that can be easily recorded. A digital-to-analog (D/A) circuit is used for this purpose. When the recorded program is subsequently played back into the computer, a separate analog-to-digital (A/D) circuit reverses the process. It converts the signal from a sine wave back into the digital form. The D/A and A/D circuits are combined on a printed circuit board with the usual parallel-to-serial converter for the I/O port.

\section*{THE CHECKSUM METHOD}

Two separate tape-handling routines are given in this chapter; both may be used with paper tape or magnetic tape. They are both suitable for storing binary object programs, ASCII-encoded source programs, or just a set of numbers. The information is stored in a file consisting of a sequence of records. Each record contains a checksum that is used to detect errors.

Errors can be introduced at several places in the tape-recording and playback process. The proximity of AC power cords to audio signal lines can change the transmitted signal. Oxide layers may fall off the tape, or there may be a defective spot on the recording surface. If the recording and playback heads are dirty, they can incorrectly render the signal. The A/D conversion step, when the tape is played back, can also give rise to errors.

In addition to the data, each record stored on the tape contains the record length, the memory address of the record, and a checksum byte. The checksum byte is obtained by adding all of the data bytes in the record. When the tape is read back, the computer sums up the data and compares the result to the checksum value written on the tape at the end of the record. A discrepancy indicates an error.

Since an 8 -bit checksum is used in both programs, there are 256 possible combinations. Any single load error in the record will be discovered by this method. In principle, it is possible that two errors in the same record will combine to produce the expected checksum value. In practice, however, this is not likely to be a problem. Double errors occur much less frequently than single errrors. Furthermore, in a well-tuned system, single errors should be infrequent. They are most likely to be caused by low-quality tape, a dirty head, or a mistuned A/D converter circuit. Buy the best tape you can and clean the heads often. A routine that can be used for aligning the A/D circuit is incorporated in the second tape routine given later in this chapter.

\section*{AN ASCII-HEX TAPE PROGRAM}

The tape program given in Listing 9.1 is based on an ASCII-encoded hexadecimal format. It can be used to produce paper tapes or magnetic tapes of
computer programs. It can even produce a tape of itself. The program is self-contained and assembled to run at 100 hex. No outside routines are required. An additional feature of this program is that it can punch readable labels on the leader of a paper tape. (Of course, this feature is not very useful for magnetic tape recordings.) The label routine is discussed in the next section of this chapter.

\begin{tabular}{|c|c|c|c|c|c|}
\hline 010F & F5 & \multirow[t]{2}{*}{\begin{tabular}{l}
OUTT： \\
OUTW：
\end{tabular}} & PUSH & \multicolumn{2}{|l|}{FSW} \\
\hline 0110 & 1810 & & IN & \multicolumn{2}{|l|}{CSTAT} \\
\hline 0112 & E602 & & ANI & \multicolumn{2}{|l|}{COMSK} \\
\hline 0114 & CA1001 & & JZ & \multicolumn{2}{|l|}{OUTW} \\
\hline 0117 & F1 & & FOF＇ & \multicolumn{2}{|l|}{FSW} \\
\hline 0118 & 11311 & & OUT & \multicolumn{2}{|l|}{CIIATA} \\
\hline \multirow[t]{4}{*}{011A} & C 9 & & FET & & \\
\hline & & －OUTP & T HoL & \multicolumn{2}{|l|}{CONSOLE} \\
\hline & & ；16－B & r BIN & \multicolumn{2}{|l|}{TO HEX} \\
\hline & & \multicolumn{2}{|l|}{\％} & \multirow[t]{2}{*}{} & \\
\hline 0118 & 4 C & OUTHL： & MOV & & ¢FETCH H \\
\hline 011 C & c02001 & & CALL & OUTHX & 伊RINT IT \\
\hline \multirow[t]{5}{*}{011 F} & 4 L & & MOV & CgL & ¢FETCA Ly FRINT \\
\hline & & \multicolumn{4}{|l|}{\％} \\
\hline & & \multicolumn{4}{|l|}{－CONUERT A BINARY NUMBER TO TWO} \\
\hline & & \multicolumn{3}{|l|}{；HEX CHARACTERS．AND} & EINT THEM \\
\hline & & \multirow[t]{2}{*}{OUTHX：} & & & \\
\hline 0120 & 79 & & MOV & \multicolumn{2}{|l|}{As C} \\
\hline 0121 & \(1 F\) & & RAR & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{\％ROTATE}} \\
\hline 0122 & IF & \multicolumn{2}{|r|}{RAR} & & \\
\hline 0123 & IF & \multicolumn{2}{|r|}{RAR} & \multirow[b]{3}{*}{HEX1} & ¢ CHAFACTEF \\
\hline 0124 & 1 F & \multicolumn{2}{|r|}{RAR} & & ¢ TO LOWEF \\
\hline 0125 & CD2901 & & CALL & & GOUTPUT UPFEF \\
\hline \multirow[t]{5}{*}{0128} & 79 & & MOV & A，C & ¢OUTFUT LOWER \\
\hline & & \multicolumn{3}{|r|}{MoV A．C} & \\
\hline & & \multicolumn{4}{|l|}{人 DUTPUT A MEX CHARACTER} \\
\hline & & \multicolumn{4}{|l|}{－FROM LOWER FOUR EITS} \\
\hline & & \multicolumn{3}{|l|}{} & \\
\hline 0129 & E60F & \multirow[t]{2}{*}{HEX 1：} & ANI & OFH & ¢TAKE 4 BITS \\
\hline 012B & C690 & & ADI & 144 & \\
\hline 012 n & 27 & & DAA & & GMAA TKICK \\
\hline 012E & CE40 & & ACI & 64 & \\
\hline 0130 & 27 & & LIA & & OONCE AGAIN \\
\hline 0131 & C30FO1 & & JMF＇ & \multicolumn{2}{|l|}{OUTT} \\
\hline & & \multicolumn{4}{|l|}{\(\hat{p}\)} \\
\hline & & \multicolumn{2}{|l|}{－CONUEFT ASC} & CHAR゙ACTER & R FFOM CONSOLE \\
\hline & & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{\(\stackrel{\text { ¢ }}{\text { ¢ }}\) ，EINARY}} & ITS & \\
\hline & & & & & \\
\hline 0134 & 11630 & \multirow[t]{2}{*}{NIE：} & SUI & \({ }^{\prime} 0^{\prime}\) & \％ASCII BIAS \\
\hline 0136 & 128 & & FC & \multicolumn{2}{|l|}{碞 \({ }^{\circ}\)} \\
\hline 0137 & FE17 & & CFI & \multicolumn{2}{|l|}{\({ }^{\prime} \mathrm{F}^{\prime}-{ }^{\prime} 0^{\prime}+1\)} \\
\hline 0139 & 3F & & CMC & \multicolumn{2}{|r|}{SINUEFT} \\
\hline 013A & D8 & & RC & & SERFIOR \({ }^{\text {S }}\) ，F＇ \\
\hline 013B & FEOA & & CPI & 10 & \\
\hline 0131 & \(3 F\) & & CMC & & GINUERT \\
\hline 013E & 10 & & RNC & & ONUMBER IS 0－9 \\
\hline 013F & 1607 & & SUI & ＇\(A^{\prime}\)－－＇\({ }^{\text {c }}\) & \\
\hline 0141 & FEOA & & CFI & 10 & \\
\hline 0143 & c9 & & RET & & SCHARACTER IS A－F \\
\hline & & \multicolumn{3}{|l|}{¢} & \\
\hline & & －INPU & HoL F & －CONSO & \\
\hline 0144 & 115 & REAIIHL & FUSH & 4 & \\
\hline 0145 & C5 & & FUSH & E & \\
\hline 0146 & 210000 & & LXI & HoO & जSTAFT WITH O \\
\hline 0149 & C10402 & RLIML2： & CALL & GETCH & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|}
\hline 014C & 19A6801 & & JC & FDHLS & ¢ END OF LINE \\
\hline 014 F & C13401 & & CALL & NIB & ¢CONUERT TO BINARY \\
\hline 0152 & DA5E01 & & JC & RDHL 4 & ONOT HEX \\
\hline 0155 & 29 & & IUAD & H & 916-BIT \\
\hline 0156 & 29 & & IAD & H & \% SHIFT LEFT \\
\hline 0157 & 29 & & Dall & H & \\
\hline 0158 & 29 & & OAII & H & \\
\hline 0159 & B5 & & OKA & L & SCOMEINE NEW \\
\hline 015A & 6F & & MOU & \(L\), \(A\) & \\
\hline \multirow[t]{5}{*}{0158} & \multirow[t]{5}{*}{C34901} & & JMF' & Finhle & GNEXT \\
\hline & & \% & & & \\
\hline & & ¢ CHECK & FOR & MA OR BL & ANK \\
\hline & & \(\stackrel{A}{\text { a }}\) AT & D OF & RESS & \\
\hline & & ¢ & & & \\
\hline 015E & FEFC & RDHL 4: & CPI & '9'..- \(0^{\prime}\) & ¢COMMA? \\
\hline 0160 & CA6801 & & JZ & FIDHL 5 & GYES. OK \\
\hline 0163 & FEFO & & CPI & , - - \({ }^{\prime}\) & ¢BLANK? \\
\hline 0165 & C26801 & & JNZ & EFROR & g NO \\
\hline 0168 & C1 & KMHLS 5 & POF & E & \\
\hline 0169 & 11 & & FOF & 1 & \\
\hline \multirow[t]{2}{*}{016A} & \multirow[t]{2}{*}{C9} & & RET & & \\
\hline & & ¢ & & & \\
\hline 0168 & 3E3F & ERROR: & MUI & Ag'?' & SIMPROFEF INPUT \\
\hline 01611 & CMOFO1 & & CALL & OUTT & \\
\hline \multirow[t]{5}{*}{0170} & \multirow[t]{5}{*}{c30001} & & JMP & START & gTELL HOW AGAIN \\
\hline & & \% & & & \\
\hline & & \% SEND & CHRACT & \(S\) FOINTE & TO EY M, E \\
\hline & & ¢ UNTIL & A BIN & \(Y\) ZERO I & FOUNA \\
\hline & & \% & & & \\
\hline 0173 & 1 A & SENDM: & LIDAX & 11 & FNEXT RYTE \\
\hline 0174 & E7 & & ORA & A & ¢SEE IF ZERO \\
\hline 0175 & C8 & & RZ & & 9LIONE \\
\hline 0176 & CnOFO1 & & CALL & OUTT & \\
\hline 0179 & 13 & & INX & 1 & \\
\hline \multirow[t]{2}{*}{017A} & c37301 & & JMF' & SENIM & \\
\hline & & \% & & & \\
\hline 01711 & 312106 & CONTIN: & LXI & SF'gTAC & * \\
\hline 0180 & 118603 & & LXI & IISSIGN & ¢MESSAGE \\
\hline \multirow[t]{2}{*}{0183} & ca7301 & & CALL & SENIMM & ¢SEND IT \\
\hline & & \% & & & \\
\hline 0186 & 312106 & RSTRT: & LXI & SFPSTAC & \\
\hline 0189 & CDACO1 & & CALL & INFLN & gGET A LINE \\
\hline 018C & CDO402 & & CALL & GETCH & ¢INFUT THE TASK \\
\hline 018 F & FES7 & & CFI & 'W' & \% LUMF' \\
\hline 0191 & CA1A02 & & JZ & F'IUMF & \\
\hline 0194 & FE52 & & CFI & 'R'。 & GREALI NO AUTOSTART \\
\hline 0196 & CAE602 & & JZ & Ploan & \\
\hline 0199 & FE45 & & CFI & 'E' & iloan ana execute \\
\hline 019E & CAE602 & & J2. & Floali & \\
\hline O19E & FES6 & & CFI & 'V' & GUEFIFY \\
\hline 0140 & CAE602 & & JZ & Floan & \\
\hline OLA3 & FE47 & & CFI & 'G' & \$GO SOMEWHEFE \\
\hline O1AS & C26801 & & JNZ & ERROR & \\
\hline
\end{tabular}


```

021A CD4401
021D [AAGBO1
0220 EB
0221 CD4401
O224 EE
0225 13
0226 E5
0227 cm4401
O22A E3
022B C108502
O22E CD8404
0204 ES
0205 2A2106
0208 3A2306
020B 10601
O20n DA1802
0210 322306
0213 7E
021423
0215 222106
0218 Ei
0219 C9

| 02 | CD |
| :---: | :---: |
| 0210 | $\square A 6 B 01$ |
| 0220 | EP |
| 0221 | CDA401 |
| 0224 | EE |
| 0225 | 13 |
| 0226 | ES |
| 0227 | cm4401 |
| 022A | E3 |
| 022B | C08502 |
| O22E | CD8404 |

\hat{q}
01F5 C3OFO1
01F879
01F9 B7
OIFA CABCOI
O1FD 2B
OIFE OLI
01FF 3E08
0201 C3DAO1

| IF | NNULS 3 | O ASSEMEILE |  |
| :---: | :---: | :---: | :---: |
| CALL | OUTT |  |  |
| XRA | A | ¢GET A | NULL |
| REPT | NNULS-1 |  |  |
| CALL | OUTT |  |  |
| ENDM |  |  |  |
| ENOIF |  | ¢ NULLS |  |

JMF
OUTT
DELETE ANY FRIOR CHAFACTER
g
INPLE: MOU A,C SHCHAF COUNT
ORA A OZEFO?
JZ INFLI GYES
IOCX H \&BACK POINTER
DCF C GAND COUNT
MUI A,CTRH क्BACK CURSOR

```

```

\hat{g}
obTAIN A ChARACTER FROM THE CONSOLE

# BUFFER. SET CARRY IF EMFTY.

\&
GETCH: PUSH H GSAVE REGS
LHLD IBUFF FGET FOINTER
GETC2: IDA IEUFC FGET COUNT
SUI 1 SHECR WITH CARRY
IC GETC4 \hat{NO CHARACTERS}
STA IEUFC FEFLACE COUNT
MOU A,M GGET CHARACTER
GETC3: INX H OINCR FOINTER
SHLII IBUFF OFEFLACE FOINTER
POF H ORESTORE FEEGS
RET \CARRY IF NO CHAR

```

```

\
\& FUNCH A FAFER TAFE
g
FTUMF: CALL FEADHL \#START ALIDRESS
JC ERROR \&TOO FEW FARAM
XCHG
CALL FEAIHL ASTOF ALIDRESS
XCHG
INX D
PUSH H
CALLL FEALHLL yAUTOSTART AIIDR
XTHL \&FUT ON STACK
CALL LEADF 夕FUNCH LEADEF
CALL LABEL \#FUNCH LABEL
%
S START NEW RECORI, ZERO THE CHECKSUM
g PUNCH CR, LF, 2 NULLS ANI COLON
\#
0231 COMOO2 NEWREC: CALL FCFLF \&CR, LFg NULLS
\hat{0}
; FINL THE RECORD LENGTH

```
\begin{tabular}{|c|c|}
\hline 0234 & 7B \\
\hline 0235 & 95 \\
\hline 0236 & 4F \\
\hline 0237 & 7A \\
\hline 0238 & 9C \\
\hline 0239 & 47 \\
\hline 023A & DA6B01 \\
\hline 023 D & 3E10 \\
\hline 023 F & \(\mathrm{C} 24 \mathrm{CO2}\) \\
\hline 0242 & B9 \\
\hline 0243 & DA4C02 \\
\hline 0246 & 78 \\
\hline 0247 & B1 \\
\hline 0248 & CA6802 \\
\hline 024B & 79 \\
\hline 024C & 4F \\
\hline 02411 & 0600 \\
\hline 024F & C19502 \\
\hline 0252 & C119002 \\
\hline 0255 & AF \\
\hline 0256 & C19502 \\
\hline 0259 & 7E \\
\hline 025A & C119502 \\
\hline 02511 & 23 \\
\hline 025E & OD \\
\hline 025F & C25902 \\
\hline 0262 & CD6703 \\
\hline 0265 & C33102 \\
\hline
\end{tabular}

0268 AF
026947
026A CD9502
026 DEL
026 E CD9002
0271 7C
0272 B5
0273 3E00
0275 CA7902
0278 3C
0279 C109502
027 C C116703
027F CD8502
0282 C38601

0285 AF
0286063 C
0288 CDB8O2
028 B 05
028 C C28802
028F C9

```

0 2 9 0 ~ 7 C ~ C
0291 C119502
0294 7II
0295 F5
029680
029747
0298 F1
0 2 9 9 ~ F 5 ~ 5
029A 1F
029B 1F
029C 1F
02910 1F
O29E CNA2O2
02A1 F1

| $02 A 2$ | $E 60 F$ |
| :--- | :--- |
| $02 A 4$ | $C 690$ |
| $02 A 6$ | 27 |
| $02 A 7$ | CE40 |
| $02 A 9$ | 27 |
| $02 A A$ | C3B802 |

02AII CDC4O2
0280 11630
O2B2 FEOA
02B4 D8
02B5 11607
02B7 C9
02R8 F5
0289 14BO6
O2BB E680
0280 C28902
02C0 F1
02C1 10307
02C3 c9
02C4 11806
02C6 E601
02C8 C2C472
02CB 10807
02CII E67F
O2CF C9

```
```

% FUNCH THE H%L REGISTER FAIR
\$IT

```
```

PUNHL: MOU AyH FFETCH H

```
PUNHL: MOU AyH FFETCH H
CALL FNHEX \hat{FUNCH IT}
CALL FNHEX \hat{FUNCH IT}
MOU AgL \hat{GET L, PUNCH}
MOU AgL \hat{GET L, PUNCH}
\hat{g}
\hat{g}
\hat{g}
C CONUEFTT A BINAFY NUMEER TO TWO HEX
C CONUEFTT A BINAFY NUMEER TO TWO HEX
C CONUEFTT A BINAFY NUMEER TO TWO HEX
; CHARACTERS, PUNCH THEM, AMD TO CHECKSUM
; CHARACTERS, PUNCH THEM, AMD TO CHECKSUM
; CHARACTERS, PUNCH THEM, AMD TO CHECKSUM
%
%
%
FNHEX: FUSH FSW GSAVE ON STACK
FNHEX: FUSH FSW GSAVE ON STACK
FNHEX: FUSH FSW GSAVE ON STACK
    ADN E FADN TO CHECKSUM.
    ADN E FADN TO CHECKSUM.
    ADN E FADN TO CHECKSUM.
    MOU E,A ;SAUE IT IN E
    MOU E,A ;SAUE IT IN E
    MOU E,A ;SAUE IT IN E
    POF FOSW IRETRIEVE BYTE
    POF FOSW IRETRIEVE BYTE
    POF FOSW IRETRIEVE BYTE
    PUSH FSW
    PUSH FSW
    PUSH FSW
    RAR GROTATE UPFER
    RAR GROTATE UPFER
    RAR GROTATE UPFER
    RAR #FOTATE UFFER
    RAR #FOTATE UFFER
    RAR #FOTATE UFFER
    FAR {TO LOWER
    FAR {TO LOWER
    FAR {TO LOWER
    RAR FHEX1 \hat{M OLEFT CHARACTER}
    RAR FHEX1 \hat{M OLEFT CHARACTER}
    RAR FHEX1 \hat{M OLEFT CHARACTER}
    FOF FOSW ORIGHT CHARACTEF
    FOF FOSW ORIGHT CHARACTEF
    FOF FOSW ORIGHT CHARACTEF
\hat{g}
\hat{g}
* FUNCH A HEX CHAFACTEF FROM
* FUNCH A HEX CHAFACTEF FROM
; LOWER FOUR EITS
; LOWER FOUR EITS
{
{
PHEX1: ANI OFH {MASK UPFER 4 BITS
PHEX1: ANI OFH {MASK UPFER 4 BITS
ALII 144
ALII 144
IDAA
IDAA
ACI 64
ACI 64
IIAA
IIAA
    JMF FOUT
    JMF FOUT
\hat{y}}\mathrm{ INFUT A HEX CHARACTER FROM TAPE
\hat{y}}\mathrm{ INFUT A HEX CHARACTER FROM TAPE
%
%
HEX: CALL FIN
HEX: CALL FIN
SUI 'O'
SUI 'O'
CPI 10
CPI 10
KC \hat{0Mg}
KC \hat{0Mg}
SUI 7 A-F
SUI 7 A-F
FET
FET
&
&
& OUTPUT A BYTE TO THE FUNCH
& OUTPUT A BYTE TO THE FUNCH
#
#
POUT: FUSH FSW
POUT: FUSH FSW
FOUTW: IN PSTAT
FOUTW: IN PSTAT
ANI POMSK
ANI POMSK
JNZ POUTW
JNZ POUTW
POF FOSW
POF FOSW
OUT FMATA
OUT FMATA
RET
RET
&
&
A INPUT A BYTE FROM PAPER TAPE
A INPUT A BYTE FROM PAPER TAPE
#
#
FIN: IN FSTAT
FIN: IN FSTAT
    ANI PIMSK
    ANI PIMSK
    JNZ FIN
    JNZ FIN
    IN FLIATA
    IN FLIATA
    ANI 7FH osTRIF FARITY
    ANI 7FH osTRIF FARITY
RET
```

RET

```
\begin{tabular}{|c|c|}
\hline 02100 & 3EOD \\
\hline 0202 & CuB802 \\
\hline 0205 & 3EOA \\
\hline 0207 & CDB802 \\
\hline O2DA & AF \\
\hline 02ab & CaB802 \\
\hline O2DE & CuB802 \\
\hline O2E1 & 3E3A \\
\hline O2E3 & C3B802 \\
\hline
\end{tabular}
```

02E6 320006
02E9 3E11
O2EB CDB8O2
O2EE CIM401
02F1 220106

```
O2F4 CDCAO2
\(02 F 7\) FE3A
\(02 F 9\) C2F402
\(02 F C 0600\)
\(02 F E\) CO3303
0301 B7
\(0302 \mathrm{CA4A03}\)
0305 4F
0306 CO2PO3
0309 EB
O30A 2A0106
03011 19
O3OE CH3303
03115 F
0312 3A0006
0315 FE56
031778
0318 CA1CO3
031 B 77
031 C RE
\(0310 \mathrm{C27603}\)
032023
0321 OD
0322 C2OEO3
0325 C1261103
0328 C3F402
032 B CLI 3303
O32E 67
032 F CD3303
0332 6F
```

; FUNCH CR, LF, NULLS ANI COLON
;
PCRLF: MUI A,CR
CALL FOUT
MUI A,LF
CALL FOUT
XRA A
CALL FOUT ;TWO NULLS
CALL FOUT
MUI A,':' ACOLON
JMF FOUT

```

```

% ENTRY FOR LOAI, EXECUTE AND VERIFY
PLOAD: STA TASK
MUI A.17 ATAPE READER ON
CALL FOUT
CALL READIHL yOFFSET
SHLI OFSET 戶SAVE IT
; process the fecoril mealingg on input
;
HEAI: CALL PIN \#INPUT FROM TAFE
CPI '!' \#COLON?
JNZ HEAII iNO, TRY AGAIN
MUI B.O tZERO THE CHECKSUM
CALL FHEX {RECORD LENGTH
ORA A y IS IT ZERO?
SZ ENDFL gYES` DONE
MOU C:A tSAVE REC. LEN.
CALL TAFEHL कGET H/L
XCHG ;ADDR TO D,E
LHLD OFSET igET OFFSET
DAD ■ %ANI
CALl frhex ofmFut mata gyte
MOU E:A \#SAVE BYTE
LDA TASK gGET TASK
CPI 'U' 今
MOU A,E कMOVE BACK
JZ SKIP \hat{JUMF IF VERIFYING}
MOU MgA fDATA TO MEMORY
SKIF: CMP M FCHECK MEMORY
JNZ MERROR ABAD MEMORY
INX H DINCREMENT FOINTER
ICR C ODECR RECORD LEN
JNZ LOOF \#NOT YET ZERO
CALL CHECK pPROCESS CHECKSUM
JMP HEAD 戶START NEXT RECORD
; INPUT H,L AND RECORD TYPE FROM TAPE
|
TAPEHL: CALL FHEX tREAD H
MOV HIA FHEX SREAIIL
CALL PHEX iREAIIL
MOU LyA gREAD RECORII TYFE
\hat{j}

* CONUERT 2 CHAR FROM TAPE TO DNE BINAFY
; WORD, STORE IN A AND ADII TO CHECKSUM

```


\begin{tabular}{|c|c|c|c|c|c|c|}
\hline OAEF & CDB502 LABL2: & CALL & \multicolumn{4}{|l|}{LEAIR} \\
\hline OAC2 & 01 & POP & 1 & & & \\
\hline OAC3 & E1 & POP & H & & & \\
\hline 0.84 & C9 & RET & & & & \\
\hline \multicolumn{7}{|c|}{\%} \\
\hline 0405 & 0000000000 TAEL: & DB & O\% 0, & 09000 & ; & SPACE \\
\hline OACA & OOOOCFCFOO & D8 & O. 0. & 207,207:0 & ¢ & ExCl. \\
\hline OACF & 0007000700 & D8 & 0, 7, & \(0,7,0\) & \% & : \\
\hline 04104 & 2EFESBFE28 & DB & 40, 254 & ,40, 254,40 & ¢ & 每 \\
\hline 04109 & 48895188972 & DB & 70, 137 & ,255,137,114 & , & \$ \\
\hline OADE & 462610 CBCA & 108 & 70, 38, & 16,2009196 & * & \% \\
\hline O4E3 & 6C92ACAOAO & 08 & 108,146 & ,172.64, 160 & ) & 8 \\
\hline 04 E 8 & 0004030300 & DB & 0,4 & ,3, 3, 0 & \$ & , \\
\hline OAEII & \(003 C 428100\) & 10 B & 0, 60, & 66.129 .0 & ; & ( \\
\hline \(04 F 2\) & \(0081423 C 00\) & DE & 0, 129, & ,66, 60, 0 & \% & ) \\
\hline 0457 & 8850F85088 & LE & 136,80, & 248,80, 136 & \% & 家 \\
\hline O4FC & 08087E0808 & 1 B & 8, 8, & 126,8, 8 & \% & \(t\) \\
\hline 0501 & 0080703000 & DB & 09128 & ,112.48, 0 & ) & , \\
\hline 0506 & 0808080808 & L18 & 8, 8, & 8, 8, 8 & \(\dagger\) & - \\
\hline O508 & 00 COCOOOOO & D8 & 0, 192. & 192,0, 0 & \% & - \\
\hline 0510 & 4020100804 & WE & 64, 32, & 16, 8, 4 & ¢ & 1 \\
\hline 0515 & 7EA189857E & DB & 126,161. & ,137.133.126 & \% & 0 \\
\hline OS1A & 8482FF8080 & DB & 1329130 & ,255,128.128 & * & 1 \\
\hline 0515 & C2A1918986 & L18 & 194.161. & ,145,137,134 & \% & 2 \\
\hline 0524 & 4289898976 & D8 & 66,137 & ,137,137.118 & ¢ & 3 \\
\hline 0529 & OCOA89FF88 & HB & 12, 10. & ,137,255,136 & * & 4 \\
\hline 052E & 6789898971 & PB & 103.137 & ,137.137,113 & ; & 5 \\
\hline 0533 & \(7 E 89898972\) & DB & 126,137. & ,137,137,114 & ) & 6 \\
\hline 0538 & 0101F90503 & UR & 1.19 & 249,5, 3 & - & 7 \\
\hline 0530 & 7689898976 & D* & 118.137 & ,137,137,118 & * & 8 \\
\hline 0542 & 468989897E & 0 B & \(70,137\). & ,137,137,126 & ) & 9 \\
\hline 0547 & 00118180000 & IR & 0, 216 & ,216,0, 0 & ¢ & : \\
\hline 054 C & 0080763600 & DB & 0, 128. & ,118,54,0 & ¢ & ) \\
\hline 0551 & 1028448200 & 118 & 16. 40, & 68, 130,0 & \$ & \(<\) \\
\hline 0556 & 2828282828 & HE & 40, 40, & 40, 40, 40 & ; & \(=\) \\
\hline 055B & 8244281000 & pB & 130,68, & \(40,16,0\) & \% & > \\
\hline 0560 & 0601490906 & HE & \(691 \%\) & 185.986 & \(\hat{\text { ¢ }}\) & ? \\
\hline 0565 & 7E8191910E & DB & 126.129. & .157.145.14 & ; & \\
\hline 056A & FE090909FE & DB & 254,9\% & 9, 9, 254 & \% & A \\
\hline 056F & 81FF898976 & LIE & 129.255. & ,137,1370118 & \% & B \\
\hline 0574 & 7E81818142 & \(\square B\) & 126.129. & ,129,129, 66 & ) & C \\
\hline 0579 & 81FF81817E & DE & 129.255. & ,129,129,126 & ; & \(\square\) \\
\hline 057E & FF89898989 & D8 & 255,137. & ,137,137.137 & ) & \(E\) \\
\hline 0583 & FF09090901 & dB & 255.9. & 9.9 .1 & ; & \(F\) \\
\hline 0588 & 7E81919172 & 14B & 126,129. & ,145,145,114 & ) & G \\
\hline 0580 & FF080808FF & 118 & 255.8. & 8, 8, 255 & , & H \\
\hline 0592 & 0081 FF 8100 & DB & 0. 129, & ,255,129.0 & * & I \\
\hline 0597 & 6080817F01 & DB & 96, 128. & ,129,127.1 & \% & J \\
\hline 059C & FF081422C1 & 188 & 255,8, & 20, 34, 193 & \% & \(K\) \\
\hline 05A1 & FF80808080 & 108 & 255,128, & ,128,128,128 & ; & \(L\) \\
\hline \(05 A 6\) & FF020C02FF & IB & 255.2. 1 & 12, 2, 255 & , & M \\
\hline OSAB & FF023C40FF & D8 & 255.2, 6 & 60, 64, 255 & ; & \(N\) \\
\hline 0580 & FF818181FF & DB & 255,129, & ,129,129,255 & ) & 0 \\
\hline 0585 & 0509090906 & DB & 5. 9\% & 9, 9\% 6 & \(\hat{\dagger}\) & F \\
\hline OSBA & 7E81A1418E & 188 & 126.129, & ,161,65, 190 & ; & Q \\
\hline 05BF & FF19294986 & D8 & 255.259 & 41, 73, 134 & , & \(R\) \\
\hline 05C4 & 4689898972 & DB & 70. 137, & , 137,137,114 & \% & 5 \\
\hline 05c9 & 0101FF0101 & DE & 1. 10, & 255,1, 1 & ¢ & T \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline OSCE & 7F8080807F & & DB & 127.128. & 128,128,127 & \% U \\
\hline 05D3 & OF30CO300F & & DB & 15, 48, & 192,48, 15 & \% U \\
\hline 0518 & 7F8070807F & & 188 & 127.128. & 112.128 .127 & W \\
\hline 0510 & C3241824C3 & & DE & 195.36. & 24, 36, 195 & , X \\
\hline 05E2 & 0304F80403 & & NB & 3. 4, & 248,4 , 3 & ¢ \(Y\) \\
\hline 0SE7 & C1A1918987 & & [B & 193.1610 & 145,137.135 & \% Z \\
\hline 05EC & OOFF818181 & & D8 & 0, 255. & 129.129,129 & - [ \\
\hline 0571 & 0408102040 & & 118 & \(4 \% 80\) & 16, 32, 64 & 1 \\
\hline 05F6 & 818181FF00 & & DB & 129.129 & 129,255,0 & 7 \\
\hline 05FB & OC0201020C & & DB & 12, 29 & 1, 2, 12 & \% \\
\hline 0600 & & TASK: & ns & 1 & GSAUE IT & \\
\hline 0601 & 0000 & OFSET: & DW & 0 & GLOAD OFFSET & \\
\hline 0603 & & & DS & 30 & ¢STACK SPACE & \\
\hline & & STACK: & & & & \\
\hline 0621 & & IRUFP: & 05 & 2 & g BUFFER POIN & NTER \\
\hline 0623 & & IBUFC: & IS & 1 & ABUFFER COUN & \\
\hline 0624 & & IBUFF: & DS & 20 & - INFUT BUFFE & \\
\hline 0638 & & & ENI & & & \\
\hline
\end{tabular}

Sumbols:
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline 0011 & cdata & 03611 & CHECK & 0001 & CIMSK & 0002 & COMSK \\
\hline 0171 & CONTIN & 000 n & CR & OLEE & CRLF & 0010 & cstat \\
\hline 0367 & CSUM & 0008 & CTRH & 007F & LEL & 0279 & DON2 \\
\hline 0268 & LONE & 0344 & ENDFL & 016E & ERROR & 0208 & GETC2 \\
\hline 0214 & getc3 & 0218 & getca & 0204 & GETCH & 0254 & HEAM \\
\hline 0129 & HEX1 & O2AD & HEX & 0623 & IEUFC & 0624 & IBUFF \\
\hline 0621 & IBUFP & 0184 & INPL2 & 01100 & INFL 3 & 01F8 & INFLE \\
\hline Q1E0 & INPLC & 01114 & INPLE & O1BC & INPLI & O1AC & INPLN \\
\hline 0103 & INPUTT & O1AE & JPCHL & 0484 & LABEL & 048F & LABL 1 \\
\hline 04 BF & LABL2 & 0285 & LEALIR & OOOA & L.F & O46B & LMESG \\
\hline O30E & LOOF & 0376 & MEFRROR & 024C & NEW2 & 0231 & NEWREC \\
\hline 04AF & NEXTC & 0134 & NIE & 0288 & NLDF & 0000 & NNULS \\
\hline 0601 & OFSET & 011E & OUTHL & 0120 & OUTHX & 010F & OUTT \\
\hline 0110 & OUTW & 02 DO & PCRLF & 0007 & FIdata & 021A & Flump \\
\hline 02A2 & PHEX1 & 0333 & PHEX & 0001 & PIMSK & 02 C 4 & FIN \\
\hline 02E6 & PLOALI & 0259 & PMEM & 0295 & PNHEX & 0080 & FOMSK \\
\hline 02B8 & FOUT & 0289 & POUTW & 0006 & FSTAT & 0290 & PUNHL \\
\hline 0149 & RDHL 2 & 015E & RDHL 4 & 0168 & REHLS & 0144 & REAIOHL \\
\hline 0010 & RLEN & 0186 & RSTRT & 0173 & SENDM & 0386 & SIGN \\
\hline 031 C & SKIP & 0621 & STACK & 01.00 & START & 0405 & TABL. \\
\hline 032B & TAFEHL & 0600 & TASK & 0362 & TOFF & & \\
\hline
\end{tabular}

This program generates tapes with a modified Intel format. A typical record is shown in Figure 9.1.


Figure 9.1. The hex tape format.
In this example, the record length is 10 hex, the address is 100 hex, the record type is 00 , the first data byte is C3, the last data byte is F5 hex, and the checksum is FF hex. This is the format used by the \(\mathrm{CP} / \mathrm{M}\) assemblers ASM and MAC to generate HEX files.

Each record starts with a colon and is followed by the hex-encoded data. Since the data are encoded in ASCII, two bytes on the tape are needed to represent each original byte. Two hex characters, representing the record length, follow the header character. This hex value gives the actual number of data bytes contained in the record. It does not include the other characters in the record which designate the record address, the record type, and the checksum. A zero value for the record length is used for the last record to indicate the end of the file.

The record address, the address of the first byte in the record, comes next. This address is encoded into four hex characters, high-order byte first. The next item is the record type; it consists of two characters and can be 00 or 01 . The value is usually 00 , however; 01 is used for the end-of-file record for autostart tapes.

The data from memory are encoded next. Two bytes on the tape represent each data byte. The checksum byte is the last item in the record. It is formed by taking the two's complement of the sum of all the previous bytes in the record (in binary form). A carriage return, line feed, and optional nulls follow the checksum.

When the hex tape is loaded into the computer, the bytes within each record including the checksum are added together. The checksum byte is formed from the two's complement of the original sum. Since the sum of a number and its two's complement is zero, the total at this point should be zero. A nonzero result indicates an error.

The last record in the file has a record length of zero. This end-of-file record can indicate an autostart address in place of the usual record address. The computer can branch to this autostart address after the program is loaded. The record type in this case is 01 -the end-of-file record.

Since the tape is written with an ASCII-encoded format, it is easy to read. Listing 9.2 shows the first part of the monitor made with the monitor itself.

> Listins 9.2 A hen dump of the besimoins of the monitor.
> :10010000C37NO1DB10EGO1CAOKO1OB11EG7FC9FSFF :10011000DB10E602CA1001F1H311C94CCD200141OOC :10012000791F1F1F1FCD290179E60FC69027CE4OEA :1001300027C30F011630N8FE173F R8FEOA3FLIOD6CE

The disadvantage of this format is that the tape takes twice as long to make and twice as long to read as a corresponding binary tape. A BASIC interpreter that loads in 20 minutes from a binary format would take 40 minutes to load from hex format.

You may want to reassemble the hex tape routine for some other memory location, or you may want to incorporate it into your system monitor. But wait until you've learned about the binary tape monitor shown later in this chapter before you do.

Type in the hex program, assemble it, and start it up by branching to the beginning. A list of commands will be printed as a guide to operation.

Hex paper-tape program:
\begin{tabular}{ll}
E & load and execute \\
G & go to address given \\
R & read tape into memory (with optional offset) \\
V & verify tape against memory \\
W & write and label paper tape (with optional autostart)
\end{tabular}

Console input is buffered just as it is in our system monitor. In fact, you will notice that many of the monitor I/O routines have been duplicated in this tape program. To create a tape, type the letter \(W\) (for write), the start address, and an optional autostart address. Finish the line with a carriage return. Typing errors can be corrected as usual with a DEL or backspace key. When the statement "Enter leader message" appears, either type the characters that you want on the tape leader, or just type a carriage return to skip the title.

After the tape has been made, it should be verified. Type the letter V and a carriage return. If you have a Teletype with an automatic tape reader, the computer can turn it on at the beginning and turn it off at the end. This is accomplished by sending a control-Q at the beginning and a control-S at the end. Each entry on the tape will be compared to the corresponding value in memory. If a checksum or verify error is detected, the process will be terminated. The appropriate error message and the address of the error will appear. In the case of a checksum error, the address is not meaningful.

A tape can be loaded into memory by typing the letter \(R\) (for read) and the optional offset value. This offset is added to the record address, after the record address has been added into the checksum. An offset of 1000 hex will
load a program 4 K bytes higher than the regular address. An offset of F000 hex will load the program 4 K bytes lower. If you want, the computer will branch to the autostart address after the tape has been loaded; simply type an \(E\) (for execute) rather than an \(R\).

If a leader message has been punched on the tape, it is not necessary to position the tape past this message. The loader routine is looking for a colon to indicate the start of a record. But the colon symbol will never appear in the label itself. There is a GO command so that you can easily leave the tape program. Type the letter G (GO) and the address.

\section*{A TAPE-LABELING ROUTINE}

The assembly language instructions that punch readable labels on paper tape begin at LABEL and continue on down to TABL. The data used by this portion starts at TABL and goes down to TASK. The characters that are available include the complete set of ASCII characters from the blank ( 20 hex) through the underline ( 5 F hex). The uppercase letters are included but the lowercase letters are not. One line of data in the source program is used for each character punched on the tape. The characters can be identified by the comment at the end of the line. The lines of data are arranged in sequence corresponding to the ASCII character set. The characters punched on the tape are generated in a five-by-eight matrix, with a row of blanks between the characters.

When the label subroutine is called, it first prints a message requesting input. In response, the user enters one line of characters and concludes the line with a carriage return. The message is then punched on the tape. Each ASCII character is obtained from the console input buffer as needed. The ASCII character is converted to binary by subtraction of an ASCII blank. The result is then used as a pointer to find the corresponding entry in the table. This is done by multiplying the binary value by 5 and adding it to the table address. The next five bytes of the table are then sent to the punch. The complete set of characters is shown in Figure 9.2.


Figure 9.2. The set of letters and numbers produced by HEXMON.

The label subroutine with its necessary I/O routines can be removed from the tape program and used separately. It can be placed into high memory and called by another program such as a BASIC interpreter.

\section*{A BINARY TAPE MONITOR}

The hexadecimal program given in the previous section is useful for paper tape. But a binary tape routine is much more suitable for magnetic tape. With a magnetic tape format, the tape cannot be visually inspected. Therefore, there is no advantage in coding the data in hexadecimal format.

Files are organized into records just as they are with the hex program. Each record starts with a record header, then continues with the record length, the address, the data, and the checksum. But the binary format is a bit different. As shown in Figure 9.3, there are three types of records: a header record, a data record, and an end-of-file record. The first record in the file is the file-header record. It begins with a 55 -hex character. An optional filename appears next. The record header ends with a carriagereturn character.
\begin{tabular}{l|l|l|l|l|l|}
\hline & \multicolumn{1}{c|}{ Header Record } & 55 H & \multicolumn{2}{|c|}{ Filename } & \multicolumn{2}{c|}{ Carriage Return } \\
\hline & \\
Data Record & 3 CH & Rec. Len. & Addr. & Data & Checksum \\
\hline & & \\
EOF Record & 74 H & \multicolumn{5}{|c|}{ Autostart Addr. } & Checksum \\
\hline
\end{tabular}

Figure 9.3. Three different record types are used with the binary tape format: A header record, one or more data records, and an end-of-file record.

The data record follows the header record. It starts with a 3C-hex header byte, a record-length byte, and two bytes giving the record address. The record address is written with the low-order byte first. The data bytes appear next, and then the checksum concludes the record.

With this format, the checksum byte consists of the sum of the data record bytes rather than the two's complement of the sum as used with the hex format. This checksum includes the record address and the data bytes, but it does not include the record length. The record length is not needed, since an incorrectly read record length will point to an incorrect byte that is to be used for the checksum.

The end-of-file record is four bytes long. It begins with a 74 -hex character. It is followed by the autostart address, written as low byte, high byte. The fourth byte in this record is the checksum of the two-byte autostart address.

The routine given in Listing 9.3 is not a complete program. It is meant to be added to the end of the system monitor developed in Chapter 6. The

I/O and conversion routines of the monitor are used whenever possible. If you want to use it as a stand-alone program, you will have to include the necessary I/O routines. The addition of the tape program to the monitor will increase its size to one-and-a-half K bytes.

Add the new instructions to the end of the monitor, then change the monitor command-branch table for the letter T (tape)

DW TAPE \(\hat{T}\)
so that a command line starting with the letter T will cause a branch to the new tape routines.
\begin{tabular}{|c|c|c|c|c|c|}
\hline & & \multicolumn{4}{|l|}{- LOCATIONS IN THE STACK AREA ;} \\
\hline 5706 & \(=\) & FBUF & EQU & IBUFF+32 & ifilename ruff \\
\hline 57E6 & \(=\) & OFSET & EQU & FEUF +20 H & OLDAD OFFSET \\
\hline 57E8 & \(=\) & TASK゙ & EQU & OFSET+2 & \\
\hline 57E9 & \(=\) & LFLAG \% & EQU & TASK゙+1 & OLOAD-ERROR FLAG \\
\hline 0055 & \(=\) & SEYTE & EQU & 55 H & gSYNC EYTE \\
\hline 003 C & \(=\) & RHEAII & EQU & 3 CH & ORECORIL HEALER \\
\hline 0074 & \(=\) & EOF & EQU & 74 H & ¢END OF FILE \\
\hline 0006 & \(=\) & PSTAT & EQU & 6 & PPUNCH STATUS \\
\hline 0007 & \(=\) & Pdata & ERU & FSTAT+1 & ¢PUNCH TATA \\
\hline 0001 & \(=\) & PIMSK & ERU & 1 & ¢ INFUT MASK \\
\hline 0080 & \(=\) & ```
FOMSK
#
#
``` & EQU & 8 OH & ¢OUTFUT MASK \\
\hline 5 BFA & 210000 & TAPE: & LXI & \(\mathrm{H}, \mathrm{O}\) & \\
\hline 5 BFI & \(22 E 657\) & & SHLII & OFSET & ¢ ZERO OFFSET \\
\hline \multirow[t]{2}{*}{5 COO} & cn2559 & & CALL & GETCH & ¢COMMANA \\
\hline & & \[
\hat{y} \text { TAFE }
\] & COMMANII & FROCESSOR & \\
\hline 5 CO 3 & FE45 & & CFI & 'E' & \\
\hline 5 COS & CAM25C & & \(J Z\) & Tloadi & ¢ LOAII ANI EXEC \\
\hline \(5 \mathrm{Co8}\) & FEAC & & CFI & 'L' & \\
\hline \(5 C O A\) & CAL25C & & JZ & tloali & itoali \\
\hline SCOD & FEAD & & CFI & 'M' & \\
\hline Scof & CA80511 & & \(\downarrow \mathrm{Z}\) & TMAKE & ¢MAKE TEST TAFE \\
\hline 5 C 12 & FEAF & & CFI I & '0' & \\
\hline 5 C 14 & CACASC & & \(J Z\) & OFFST & GOFFSET LOAN \\
\hline 5C17 & FE54 & & CFI & 'T' & \\
\hline 5 C 19 & CA9A5II & & JZ & TTEST & ;TAPE TEST \\
\hline 5 C 1 C & FES6 & & CPI & 'V' & \\
\hline 5C1E & CAD25C & & JZ & TLOAD & ЭUERIFY TAFE/MEM \\
\hline 5 C 21 & FE44 & & CFI & ' \(\mathrm{II}^{\prime}\) & ¢DUMP TO TAFE \\
\hline 5 C 23 & C210459 & & JNZ & ERROR & \\
\hline
\end{tabular}

\begin{tabular}{|c|c|}
\hline 5 C 29 & Cn8 \\
\hline 5C2A & CD9 \\
\hline 5 C 2 D & E3 \\
\hline 5C2E & CD \\
\hline \(5 C 31\) & 3E55 \\
\hline 5033 & C \\
\hline \(5 \mathrm{5C36}\) & Cn255 \\
\hline \(5 C 39\) & DA425 \\
\hline 5c3C & C10935 \\
\hline 5C3F & C3365 \\
\hline 5 C 42 & 3EOD \\
\hline 5 C 44 & C1935 \\
\hline 5 C 47 & 3E3C \\
\hline 5 C 49 & C119 \\
\hline 5c4C & 7B \\
\hline 5 C 4 I & 95 \\
\hline \(5 C 4 E\) & 3 C \\
\hline 5C4F & 4F \\
\hline 5 C 50 & CD9 \\
\hline \(5 \mathrm{C5} 3\) & 7D \\
\hline \(5 \mathrm{C54}\) & C119 \\
\hline 5 C 57 & 45 \\
\hline \(5 C 58\) & 70 \\
\hline 5 C 59 & CD9 \\
\hline \(5 \mathrm{5C5}\) & 7E \\
\hline 5 CSD & CD935 \\
\hline \(5 C 60\) & OD \\
\hline \(5 C 61\) & CA6 \\
\hline 5 C 64 & 23 \\
\hline 5 C 65 & C35C5 \\
\hline
\end{tabular}

5 C 6878
5069 C19350
5 CbC 7 C
5C6D BA
5C6E CA755C
\(5 C 7123\)
5C72 C3475C
今
; ENII OF FILE
\(\begin{array}{ll}5 C 75 & 3 E 74 \\ 5077 & C 109350\end{array}\)
5C77 CD935C
5C7A E1
5C7B 7D
5C7C C1935C
5C7F 45
\(5 C 807 C\)
\(5 \mathrm{C81}\) CD935C
5 C84 78
\(5 \mathrm{C85} \mathrm{C} 1935 \mathrm{C}\)

\begin{tabular}{|c|c|c|c|c|c|}
\hline SCBC & 3 E11 & \multirow[t]{2}{*}{FINA:} & MUI & A CTRQ & \({ }^{m} \mathrm{~m} \mathrm{Q}\) \\
\hline SCBE & ca975c & & CALL & POUT & ¢TURN ON FEADER \\
\hline \(5 \mathrm{CC1}\) & cab25c & \multirow[t]{4}{*}{FINS:} & CALL & FIN & gGET EYYTE \\
\hline 5 SC 4 & FES5 & & CFI & SRYTE & SSYNC EYTE? \\
\hline 5CC6 & C2C15C & & JNZ & PINS & ONO, TRY AGAIN \\
\hline \multirow[t]{3}{*}{5CC9} & \multirow[t]{3}{*}{C9} & & \multirow[t]{2}{*}{RET} & & \\
\hline & & \multicolumn{3}{|l|}{,} & \\
\hline & & \multicolumn{4}{|l|}{¢ LOAL A TAPE WITH 16-EIT OFFEST} \\
\hline 5CCA & 57 & OFFST: & MOV & IIPA & - SAve TASk \\
\hline 5CCB & c091159 & & CALL & FEADHL & ¢GET OFFSET \\
\hline \(5 C C E\) & \(22 E 657\) & & SHLD & OFSET & ¢SAVE IT \\
\hline \multirow[t]{3}{*}{5cn1} & \multirow[t]{3}{*}{7 A} & \multirow[t]{2}{*}{} & MOV & A 0 II & SRESTORE TASK \\
\hline & & & & & \\
\hline & & LOAII & \multicolumn{3}{|l|}{UERIFY BINARY TAPE} \\
\hline \(5 \mathrm{CO2}\) & 32 E 857 & \multirow[t]{4}{*}{TLOAI:} & STA & TASK & - SAVE COMMAND \\
\hline 5 COS & \(21 C 657\) & & LXI & H,FBUF & OFILENAME EUFFER \\
\hline \(5 \mathrm{Cn8}\) & AF & & XRA & A & YGET A ZERO \\
\hline 5 Cn 9 & \(32 E 957\) & & STA & LFLAG & ¢RESET FLAG \\
\hline SCDC & C02559 & \multirow[t]{5}{*}{TLM1:} & CALL & GETCH & OREAII FILENAME \\
\hline SCDF & DAE75C & & JC & TLDS & OENL OF FTLENAME \\
\hline \(5 C E 2\) & 77 & & MOV & M, A & ¢FUT IN FBUF \\
\hline \(5 C E 3\) & 23 & & INX & H & \\
\hline SCEA & C3nc5c & & JMF' & TLII 1 & ONEXT CHARACTER \\
\hline 5 CE7 & 3EOL & \multirow[t]{8}{*}{TLILS:} & MUI & A,CF & \\
\hline 5CE9 & 324657 & & STA & IBUFF & \\
\hline \(5 C E C\) & cascsc & & CALL & FINA & SFIND HEADER \\
\hline SCEF & 210657 & & LXI & HeFbuF & OFILENAME BUFFEF \\
\hline \(5 C F 2\) & 7E & & MOV & AgM & 915T CHARACTER \\
\hline \(5 C F 3\) & FEOL & & CFI I & CR & \\
\hline \(5 C F 5\) & CA1CSn & & JZ. & TLO & SNO FILEMAME \\
\hline \multirow[t]{3}{*}{\(5 C F 8\)} & \multirow[t]{3}{*}{11 A657} & & LXI & Ing IBUFF & A INFUT EUFFEF \\
\hline & & & \multicolumn{2}{|l|}{LXI} & \\
\hline & & INFUT & FILENAM & ME FROM T & APEg FUT IN IBUF \\
\hline 5 CFB & cras 35 C & \multirow[t]{8}{*}{TLD2:} & CALL & TINA & GBYTE FROM TAFE \\
\hline SCFE & 12 & & Stax & 11 & ¢FUT IN IEUFF \\
\hline \(5 C F F\) & 13 & & INX & 11 & \\
\hline 5000 & FEOD & & CFI & CR & \\
\hline 51002 & CA12511 & & \(J Z\) & TLIT4 & GNO FILENEME \\
\hline 5005 & BE & & CMF & M & OCOMF FILENAMES \\
\hline 51006 & 23 & & INX & H & \\
\hline \multirow[t]{5}{*}{5107} & \multirow[t]{5}{*}{CAFBSC} & & JZ. & TLD2 & gNEXT CHAFACTER \\
\hline & & \multicolumn{3}{|l|}{;} & \\
\hline & & \% FILENA & AME ENT & EREI FROM & CONSOLE \\
\hline & & - LOESN & 'T MATC & H NAME ON & TAFE \\
\hline & & ; & & & \\
\hline SIOA & 3E46 & & MUI & Ay 'F' & \(\hat{\text { SET ERFROR FLAG }}\) \\
\hline 5 LHOC & \(32 E 957\) & & STA & LFLAG & \\
\hline 5nof & C3FB5C & & JMP & TLIL2 & \\
\hline 5112 & AF & TLD4: & XRA & A & \\
\hline 5013 & 18 & & DCX & II & \\
\hline 5014 & 12 & & STAX & 1 & \\
\hline 5015 & 3 AE957 & & LIMA & lflag & ¢CHECK FLAG \\
\hline 5018 & B7 & & ORA & A & ¢ ZERO? \\
\hline 5119 & cecosn & & JNZ & FNERF & ¢FILENAME ERROR \\
\hline
\end{tabular}


\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline 5 BO & ADMP2 & 5823 & AIMP3 & 5 H 26 & ALIMP4 & 5804 & ADUMF \\
\hline SAEI & ALOM2 & FFF7 & AFOS & SADS & ASCII & \(5 \mathrm{B2C}\) & ASCS \\
\hline 0008 & BACKUF & SB4C & EITE & SE4A & BITS & 5 S09 & CALLS \\
\hline 0011 & chata & 0011 & chatao & \(5 A 3 E\) & CHEKM & 5809 & CIN \\
\hline 5858 & coldi & 5806 & COUT & 000 LI & CR & 59110 & CRHL \\
\hline 590 F & CFLLF & 5458 & CSERK & 0010 & cstat & 0010 & cstato \\
\hline 0008 & CTRH & 0011 & CTRQ & 0013 & CTRS & 0018 & CTRX \\
\hline 007F & LEL & 5945 & IULMF' & 5948 & DUMP2 & 5948 & DUMP3 \\
\hline \(595 E\) & nump 4 & 5967 & LUMPS & 50189 & EMESS & 0074 & EOF \\
\hline 5 A45 & ERF2? & 5443 & EFRE & 59104 & ERROR & 5 A 42 & ERRP \\
\hline 0018 & ESC & 51060 & EXEC & 5706 & FBUF & 54511 & FILL \\
\hline 5466 & FILL2 & 5 A 6 C & FILL3 & 5 A75 & FILLA & 50CO & FNEFR \\
\hline 580 F & GCHAR & 5939 & getca & 5925 & GETCH & 5 AOP & G0 \\
\hline 5955 & HEX1 & 5991 & HHLLIE & 5 A 7 C & HLDEBC & SABA & HL पECK \\
\hline 5873 & HMATH & 5745 & IBUFC & 5746 & IBUFF & 5743 & I BUFF \\
\hline 0088 & INC & 580 C & INLN & 0001 & INMSK & 5805 & INPL 2 \\
\hline 58 F 1 & INPL3 & 5919 & INFLCB & 5901 & INPLC & 58 FB & INPLE \\
\hline 58 nD & INPLI & 58110 & INFLN & 581 B & INFUT2 & 5815 & INFUTT \\
\hline 5825 & INSTAT & \(5 \mathrm{B3H}\) & IFORT & 5845 & JERR & 5885 & JUST \\
\hline 5889 & JUST2 & 5892 & JUST3 & \(5 \mathrm{C88}\) & LEADR & OOOA & LF \\
\hline 57 59 & LFLAG & 5 AOD & LOAII & 5 A 10 & LOAD2 & 5 A33 & LOADI3 \\
\hline 5 A30 & LOAIIA & 5 A37 & LOALIG & 5496 & MOUNON & 5493 & MOVE \\
\hline \(5 A A O\) & MOUIN & 5878 & MSIZE & 59 CA & NIE & \(5 \mathrm{C8B}\) & NLIIR \\
\hline 586 A & NFAGE & SCCA & OFFST & 57E6 & OFSET & 0002 & OMSK \\
\hline 585A & OPORT & 5800 & ORGIN & 582 B & OUT2 & 5839 & OUT3 \\
\hline 5844 & OUTA & 0013 & OUTC & 5812 & OUTH & \(59 E 4\) & OUTHEX \\
\hline 597f & OUTHL & S9EC & OLTTHX & \(59 E 3\) & OUTLL & \(59 E 7\) & OUTSF \\
\hline 582A & OUTT & 5981 & FASC2 & 5983 & FASC3 & 5976 & PASCI \\
\hline \(51.7 F\) & FCHLT & 5 C 47 & PLO & 5c5C & FDi & 5 C 68 & FH2 \\
\hline 5075 & PD3 & \(5 \mathrm{C4} 2\) & FIA & 0007 & Fliata & SLAE & PERROR \\
\hline 0001 & FIMSK & 5CB2 & FIN & 5 CBC & PINA & SCC1 & FINS \\
\hline 5 ME4 & POFF & 0080 & FOMSK & 57A0 & FORTN & \(5 \mathrm{C97}\) & FOUT \\
\hline \(5 \mathrm{C98}\) & POUTW & 0006 & FSTAT & 5863 & PUTIO & 59A2 & FDHL2 \\
\hline 5987 & RDHLL 4 & 59 Cl & ROMLS & 5989 & KIHHLD2 & 5986 & FIIHLDE \\
\hline 5990 & FEADHL & SAAE & FEGS & \(58 B 4\) & REFL & 5 BC 1 & REFL2 \\
\hline 5 BCC & FEEFL3 & 5803 & RESTRT & 00C9 & RETC & 003C & FHEAL \\
\hline 0055 & SBYTE & SAAII & SEAR2 & \(5 \mathrm{AB8}\) & SEAFB & SACF & SEAR 4 \\
\hline \(5 \mathrm{AC9}\) & SEARS & 5 AAA & SEARCH & 593 E & SENAM & 584 F & SIGNON \\
\hline 5194A & SKIF. & 57 AO & STACK & 5800 & STAFT & 0009 & TAB \\
\hline 589 C & TABLE & 5BFA & TAFE & 57 E 8 & TASK & \(5 C 36\) & TLMF \\
\hline SCAJ & TINA & 5110 & TLO & 51I3E & TLI & 5 cac & TLID \\
\hline SCFE & TLD2 & \(5 \mathrm{H12}\) & TLII4 & SCE7 & TLILS & \(5 \mathrm{Co2}\) & Tloan \\
\hline 51183 & TMAK2 & 51180 & TMAKE & 0018 & TOF & 5 C 93 & TOUT \\
\hline 5 A 00 & TSTOF & 51198 & TTEST & 5199E & Trestz & \(5 \mathrm{ED2}\) & UERM \\
\hline \(5 \mathrm{ELH5}\) & UERM2 & \(58 F 3\) & VERM3 & 3831 & UERS & 5861 & WARM \\
\hline
\end{tabular}

There are seven tape commands that can be given. The appropriate command letter must immediately follow the letter T. The first thing that should be done is to make a test tape. In fact, the test pattern should be recorded onto the beginning of each tape you own. Give the command

STM
(tape make), and start recording. The computer will send a sequence of bytes, each being one larger than the previous one. When the maximum value of FF hex has been sent, the next byte will be a zero. Record the pattern for 15 to 30 seconds. Type a control-X to end the procedure.

The integrity of the whole tape-recording system can now be tested. Rewind the test section of the tape and play it back. Type a command of

\section*{\(>T T\)}
(tape test). The computer will read a byte from the tape, increment the value, then read another byte. If the two values don't agree, then a letter C will be printed on the console. The process will then be repeated until you terminate it.

If the two values do agree, then the computer will increment the first byte again, read another byte, and compare the two. This process will be repeated over and over. Each byte on the tape will be compared to see that it is exactly one larger than the previous byte. If you can go through a onehour cassette recording without a single error, then you have a reliable system.

You may have an adjustment on the A/D converter circuit that allows you to set the frequency of the phase-locked loop (PPL). The MITS audio cassette boards have this feature. Make a test tape at least 10 minutes long, then play it back. Adjust the PPL frequency until a stream of Cs appear on the console; then adjust the PPL frequency in the opposite direction. The Cs should not print. Continue adjusting the PPL in the opposite direction again until the Cs appear again. You have now bracketed the usable range of the PPL. Set the PPL adjustment halfway between these two extremes.

There are some other tests you can make while the test tape is playing. Try moving both the audio cables and the AC line cords around to see if certain positions will cause an error. You can also try tapping the tape recorder, the computer case, the boards in the computer, and so on to see how delicate the system is. Pretty soon you will know if you have a reliable tape storage system. Remember to run the test tape at least once a week.

To save data from the computer's memory, including the tape program itself, type
```

>TD<start> <stof> <autostart> <Pilename>

```

After the D (for dump), give the start address, the stop address, the required autostart address, and an optional filename. A filename is important on
magnetic tape to ensure that you are loading the right program. The autostart address can be the system monitor address. CP/M programs can be saved on tape using the original filename. Load the program into memory with DDT, SID, or the program FETCH given in the next chapter. Branch to the tape program and give the command
```

TT1100 9AF 100 TAFE.ASM

```

The filename can include the decimal point and the file type.
Each time a new tape is made, it should be verified with the command
```

\TV<filename>

```

A tape can be loaded into memory, at its normal position by typing
```

\TL<<ilename>

```

At the conclusion of the load, the autostart address is printed on the console then control returns to the monitor. If an incorrect filename is entered, the load operation is aborted and the actual filename on the tape is printed on the console.

During the load operation, all printable characters are displayed on the console. If your console is a printer rather than a video console, you will have to remove this feature to prevent the computer from falling behind. In this case, take out the following three lines from subroutine POUTW.
```

CFI
RC
OUT CNATA

```

It is not necessary to verify the load step because of the checksum feature. If the load step was completed, then the tape was correctly read into memory.

The E command can be used instead of the L command for loading data. In this case the computer will branch to the autostart address at the completion of the load. A BASIC interpreter could be saved with the autostart address set to the BASIC start address. BASIC will then automatically start up at the completion of the E load command. The O command is used to load a tape at an offset from its regular address.

While this binary format is designed for magnetic tape systems, it can be used for paper tape as well. If a tape is punched on a Teletype machine, there will be a strange sound. The reason is that binary, rather than ASCII characters, are being punched. The printout will also be meaningless. But when the resulting tape is read back, the operation is quiet, since the inputted characters are not echoed back on the Teletype.

\section*{CHAPTER TEN}

\section*{Linking Programs to the CP/M Operating System}

The system monitor we developed in Chapters 6 and 7 allows us to communicate with the computer through the console. But this program only provides the bare minimum of operations such as memory display, block move, hex addition and subtraction, and so on. Computers are capable of performing more complicated tasks such as decimal arithmetic, keeping business records, formatting text, and game playing. Computer languages, such as FORTRAN, COBOL, and Pascal, make these tasks easier. These languages will operate on programs (called source programs) that are written by the user.

As an example, a BASIC interpreter, which may be as large as 24 K bytes, needs a user's source program for direction. An assembler needs a source file to generate the desired machine code. And, of course, a formatting program needs a work file to produce a finished file.

Because programs to perform these common tasks are so large, an efficient method of loading them into memory is needed. In addition, the output generated by these programs needs to be stored somewhere. Magnetic tape can be used for this purpose, but it tends to be slow. The floppy disk currently is a better medium. It is relatively inexpensive, and the recording medium, the diskette, can be removed. This means that backup copies can be easily generated. In addition, programs can be readily exchanged between users.

We wrote our system monitor to transfer data between the console and the computer proper. Likewise, we need a disk-operating system (DOS) to effect an orderly transfer of information between the disk and the computer. Several different floppy disk systems are available for the 8080 and the Z-80. The disk-operating system that is provided with the disk drives may be relatively primitive, or it may be very elaborate.

A very popular DOS available today for the 8080 and Z-80 is called CP/M. CP/M was initially developed for the \(8080 \mathrm{~S}-100\) buss and the 8 -inch
soft-sectored floppy disk. It is now available for most of the other configurations, including the 5 -inch floppies and the Winchester hard disk. Versions are supplied for computers that don't have an S-100 buss, such as the TRS-80.
\(\mathrm{CP} / \mathrm{M}\) is a software system that must be interfaced to each different computer configuration through a set of software interface routines. Once the interfacing is accomplished, the computer programs that run with \(\mathrm{CP} / \mathrm{M}\) become system independent.

The operating system integrates all of the common tasks. Before CP/M came along, each assembler and BASIC interpreter had to incorporate its own text editor. The user could then write and correct the source program with the built-in editor. But with the CP/M operating system, the editing can be performed separately from program execution. An independent system editor is used to create an ASCII source file. Then a processor program such as BASIC, FORTRAN, Pascal, an assembler, or a text-output formatter can be directed to utilize the source file. The results can be stored in a separate ASCII file on the disk.

It is possible to generate an assembly-language program with the system editor, then assemble it as we did when we developed the system monitor in Chapters 6 and 7. In this case we had to tailor the console input and output routines to the host computer. In particular, we included in the program the address of the console status and data ports, and the read-ready and writeready status bits. The sense of the status flags was selected with a JZ command corresponding to an active-high flag. As a result of this approach, our system monitor is not portable. The monitor runs on your system, but it might not run on someone else's unless the I/O details are changed.

We approached a solution to this problem in Chapter 8, where we wrote some base-conversion routines. We did not have to write the I/O subroutines into each program because we utilized the ones in the monitor.

When we wrote the monitor, we placed five jump vectors at the beginning. These provided an easy access to the commonly used routines. While this technique greatly simplifies things, it has the disadvantage that three bytes must be set aside for each different entry point. Also, the programmer must keep track of which entry is used for which task.

A better approach is to have only a single entry address for all operations. When this special address is called by an external program, the values in the CPU registers indicate the desired operation and provide the data. The CP/M operating system utilizes this approach. All of the systems operations are performed by calling memory address 5 . Up to 37 different operations can be performed in this way. Operations 1 through 11 allow interaction with the four logical peripherals named CONSOLE, LIST, PUNCH, and READER. They are summarized in Table 10.1. Operation 12 allows a program to determine the current \(\mathrm{CP} / \mathrm{M}\) version. The remaining function numbers are used for disk operations such as reading, writing, and head positioning.

The desired operation is selected by placing the proper function number into register C. Sixteen-bit data are transferred in the DE register.

Eight-bit data are transferred in Register E or the accumulator. For example, the console input status can be determined by placing the function number of 11 (decimal) in the C register, and calling address 5.
```

MUI C.11
CALL
5

```

Table 10.1. \(\quad \mathrm{CP} / \mathrm{M} \mathrm{I/O}\) operations. The function number is placed into register C. Single bytes are in register E. Double bytes are in the D, E register pair.
\begin{tabular}{|c|c|c|c|}
\hline Function number (in C) & Operation & Value sent & Value returned \\
\hline 1 & read CONSOLE & & char in A \\
\hline 2 & write CONSOLE & char in E & \\
\hline 3 & read READER & & char in A \\
\hline 4 & write PUNCH & char in E & \\
\hline 5 & write LIST & char in E & \\
\hline 6 & direct console I/O & \[
\begin{aligned}
& \text { FF (input; } \\
& \text { char (output) }
\end{aligned}
\] & char/stat in A \\
\hline 7 & get I/O byte & & IOBYTE in A \\
\hline 8 & set I/O byte & IOBY'TE in E & \\
\hline 9 & print CONSOLE buffer & buffer address in D, E & \\
\hline 10 & read CONSOLE buffer & buffer address in D, E & characters in buffer: \\
\hline 11 & CONSOLE status & & \[
\begin{aligned}
& 0=\text { not ready } \\
& \mathrm{FF}=\text { ready }
\end{aligned}
\] \\
\hline
\end{tabular}

On return, the accumulator and register E contain the value of FF hex if the console is ready for input, or a zero if not. The byte in the console data register can then be read by calling address 5 with the value of 1 in register C. The byte that is read will be returned in the accumulator.

\section*{CP/M MEMORY ORGANIZATION}

When \(\mathrm{CP} / \mathrm{M}\) is in operation, the main memory is divided into several regions. In order of decreasing memory, they are:
1. Basic Input/Output System (BIOS)
2. Basic Disk-Operating System (BDOS)
3. Console-Command Processor (CCP)
4. Transient-Program Area (TPA)
5. System parameter area

If the BIOS is especially tailored to a particular system, then it is called the customized BIOS or CBIOS. The BIOS and BDOS regions are collectively known as the Full Disk-Operating System (FDOS). The memory layout is shown in Figure 10.1.


Figure 10.1 A memory map for \(\mathrm{CP} / \mathrm{M}\).
BIOS contains the tailor-made routines for operation of all the peripheral devices such as the console, printer, disk drives, phone modem, and tape drives. BDOS has the hardware-independent routines for the disk operating system. The CCP handles the console commands. It contains the built-in routines such as DIR, LIST, and ERA. Separate programs such as PIP, DDT, and user-written programs execute in the TPA.

The lowest memory area contains several different items. The first is a warm-boot entry to BIOS. The first few entries are:
\begin{tabular}{lll}
\multicolumn{1}{c}{ Address } & \multicolumn{1}{c}{ Action } & \multicolumn{1}{c}{ Purpose } \\
\hline 0 & JMP BIOS +3 & warm start entry \\
3 & IOBYTE & peripheral assignment \\
4 & disk & current drive number \\
5 & JMP BDOS +6 & peripheral control \\
5 C hex & FCB & command-line argument
\end{tabular}

\section*{CHANGING THE PERIPHERAL ASSIGNMENT}

CP/M can interact with four logical peripheral devices. These are termed:
CON: console
LST: list (printer)
PUN: punch
RDR: (tape) reader
Each of these four logical devices can be assigned to four different physical devices. The 16 different possible combinations can all be encoded into the IOBYTE located at memory address 3 . The colon is part of the name; it is used when referring to peripheral devices. Disk filenames, on the other hand, are written without the colon.

The actual mapping of the logical devices into the desired physical devices must be accomplished in BIOS. Since there are so many different possibilities, it is not likely that the system supplied by your dealer will have
the IOBYTE features fully implemented. The CP/M logical console is probably mapped into your video terminal and the logical list device will be mapped into your printer. But the punch and reader might be mapped into your video terminal.

Even if you have only two peripherals, it may be useful to set up the IOBYTE feature. For example, suppose that you have both a video terminal and a printer such as a Decwriter or Teletype that has its own keyboard. Then either peripheral can be used for the console input and either can be used for the console output. The four physical console arrangements could correspond to:
\begin{tabular}{cll} 
IOBYTE & Input & \multicolumn{1}{c}{ Output } \\
\hline 0 & video & video (default) \\
1 & video & printer \\
2 & printer & printer \\
3 & printer & video
\end{tabular}

Your customized BIOS (CBIOS) will set the default combination on a cold start. But any user program can change the IOBYTE to a new configuration. Also, the CP/M programs STAT and DDT can be used to alter the IOBYTE. The instructions in CBIOS will sample the IOBYTE and act accordingly.

Suppose that the IOBYTE is set to zero, and you load a BASIC interpreter. You develop a program that sends information to the console. The program will include statements like
```

FRINT I, X(I), Y(I)

```

The resulting output appears on the console video screen. After the program is debugged, you would like a hard-copy output of the program results. This is easily done if you have incorporated the IOBYTE feature. You can change the IOBYTE with the POKE command in the BASIC interpreter.
```

FOKE 3, 1

```
FUN

The POKE command will change the IOBYTE at address 3 from a zero to a 1. Console output will now appear at the printer when the BASIC program is run. Of course, console input has not changed; it still comes from the video terminal. At the conclusion of the run, the IOBYTE can be restored with another POKE command.

POKE 3, 0
As another example, suppose that you have a Teletype for your list device and it has a paper tape reader and punch. You can easily make BASIC
tapes and reload them using the IOBYTE features. POKE the IOBYTE to a value of 1 for punching a source tape. This will map the Teletype output into the logical console output. Give the BASIC commands

NULL 3
LIST
to make a tape of the source program.
Later, you can reload the tape into BASIC by setting the IOBYTE to a value of 3 .
```

PONE 3,3

```

Just put the tape into the reader and turn it on. With this configuration, the Teletype keyboard and tape reader perform the console input. But the video screen is used for console output. After the tape has been read, give the command
```

FOKE 3, O

```
from the Teletype keyboard to return to the console keyboard.

\section*{INCORPORATING THE IOBYTE INTO YOUR CBIOS}

You will have to reassemble your CBIOS if you want to incorporate the IOBYTE feature. A sample CBIOS that uses the IOBYTE is given in Listing 5.1. This version additionally features such things as an interrupt-driven keyboard and connection to a telephone modem.

At the beginning of BIOS there are seven jump vectors that are used by other parts of \(\mathrm{CP} / \mathrm{M}\).
\begin{tabular}{lll} 
JMF & INIT & ofnitialization \\
JMF & CONST & iconsole status \\
JMF & CONIN & pconsole infut \\
JMF & CONOUT & gconsole outfut \\
JMF & LOUT & glist outfut \\
JMF & FUNCH & \(\hat{i}\) Funch \\
JMF & REALIF & ireader
\end{tabular}

Because of these fixed entry points, BIOS can be altered without having to alter any other part of CP/M. There are four regions of BIOS that need to be changed if the IOBYTE feature is incorporated into console routines. These are the routines for initialization, console status, console input, and console output. We have to set the IOBYTE to the default value in the initialization section of BIOS. Then, at the beginning of the three console routines, we have to read the IOBYTE at address 3 , and branch to the appropriate subroutine.

In accordance with the step-by-step approach to programming we used in Chapter 6, we will not make all the changes at one time. The first alteration will be to the initialization and output routines.

\section*{Incorporating the IOBYTE into Output Routines}

First locate the initialization region of BIOS. This area is referenced by the first jump instruction at the beginning of BIOS. Add the following instructions somewhere in the initialization routine.
\begin{tabular}{lll} 
MUI & A.O & sset a zero \\
STA & 3 & SET IOBYTE
\end{tabular}

The safest places to put them are at the very beginning of the initialization section or at the end, just before the RET instruction. We could, of course, use an XRA A instruction rather than the MVI A, 0 instruction shown above. This would reduce the size of BIOS by one byte. But if we later wanted BIOS to initialize the IOBYTE to 3 we would have to reassemble BIOS. With the MVI instruction, we can easily change the argument of zero to a 3 by using the system debugger.

Refer to the label START at the beginning of Listing 4.1 where there is a series of jump instructions.
\begin{tabular}{llll} 
& \(\bullet\) & \\
START: & & \\
& JMF & INIT & IINITIALIZATION \\
& JMP & CONST & OCONSOLE STATUS \\
& JMF & CONIN & ICONSOLE INPUT \\
& JMF & CONOUT & ICONSOLE OUTPUT
\end{tabular}

Locate the address of the console-output routine. This can be found from the fourth jump instruction, JMP CONOUT in this case. We will now alter the console-output routine so that it will read the IOBYTE at memory address 3 and act accordingly. The upper six bits, which refer to the list, punch, and reader, are reset by performing a masking AND with the value of 3 .
\begin{tabular}{|c|c|c|c|c|c|}
\hline XXXX & XX01 & or & XXXX & \(\times \times 10\) & Iobyte \\
\hline & 11 & & & 11 & ANII with \\
\hline 0000 & 0001 & or & 0000 & 0010 & goevte \\
\hline
\end{tabular}

The two low-order bits then determine whether output is sent to the console or to the printer. If the resulting value is a 1 or a 2 , then a branch is made to the printer-output routine. Otherwise, output goes to the video console. Printer output corresponds to the following IOBYTE bit patterns.


The other two possible IOBYTE patterns correspond to console output.
```

00000000=0 or 00000011=3

```

Notice that parity is odd for printer output but parity is even for console output. Thus the BIOS code at this point is programmed to jump to the list-output routine if parity is odd.
```


# 

% LOGICAL CONSOLE DUTFUT
\&
CONOUT: LDA IOEYTE OGET ASSIGNMENT
ANI 3 SMASK FOR CONSOLE
JFO LOUT \#LIST OUTPUT
g
; UINEO-OUTPUT ROUTINE
g
UIDEO:. . (existing routine)
%
\& LIST-OUTFUT ROUTINE
\&
LOUT: . . . (existins routine)

```

Assemble the new BIOS and try it out. We can use the system debugger DDT or SID to load the new CBIOS over the old one. The command is

\section*{A. ADT CEIOS.HEX}

One word of caution: Since the debugger uses the routines in CBIOS, there may be a problem. A safer way to put the new CBIOS into place is to first load it somewhere else.

Use the hex arithmetic command of DDT to calculate the offset. Suppose that BIOS is assembled for the address DB00 hex and you want to load it temporarily at 100 hex . Then the command

\section*{H100 10800}
will give both the sum and difference of the two addresses. The difference is what we need. Load CBIOS with the indicated offset
```

ICBIOS.HEX
R(offset)

```

DDT will indicate the location of the end of BIOS. The move command can now be used to put BIOS into its proper place.
```

M100 2FF [1800

```

The second address will be the present end of BIOS. The new BIOS is now in place. If the debugger no longer works, there may be an error in BIOS or there may have been an error in the move command.

If everything appears to be all right, try out the IOBYTE feature. Use the \(S\) (set) command of the debugger to change the IOBYTE at address 3 . Change the value of the IOBYTE from a zero to a 1.
```

53
0003 00 1 (type a 1)
0004 00 - (type a decimal foimt)

```

The (logical) console output should now appear at the printer instead of the console. Notice that this is different from typing a control-P when the IOBYTE has a value of zero. In fact, if a control-P is typed at this time, each typed character should be printed twice. Return the logical console output to the console by changing the IOBYTE back to zero using DDT.
```

53
0003 01 0 (tyfe a 0)
0004 00 (tyfe a decimal point)

```

Output should return to the console.
If everything appears to be all right, you are still not finished. You have a working copy of BIOS in memory; now you must get a copy onto the system tracks of the disk. Continue with this section if you want to write a permanent copy of the new BIOS onto the disk. Otherwise, go on to the second part of the alteration where you will add the IOBYTE feature to the console input routines. Then come back to this section to save the completed BIOS. If you have a Lifeboat version of \(\mathrm{CP} / \mathrm{M}\), you can easily copy the new version of BIOS to the disk. Just give the command

\section*{A. SAUEUSER}
and the new BIOS will be copied to the system disk.
Another method of getting the new CBIOS on the disk system tracks is to use SYSGEN. The current version of CPM is loaded into memory with the DDT command

\section*{A. \(\operatorname{HIIT}\) CFMXX.COM}
where XX refers to the memory size. Then move the working version of BIOS down to the proper SYSGEN position using the DDT move command. Alternately, the HEX file of CBIOS could be copied from disk into memory.

The SYSGEN location for BIOS should be given in your CP/M documentation. Perform a warm start with a control-C, and then give the command

\section*{A. SYSGEN}

Answer the first question about where to get the system by typing just a carriage return. The second question asks where to put the system. Give the appropriate drive name, A, B, etc. The new BIOS will now be copied to disk.

\section*{Incorporating the IOBYTE into Input Routines.}

We are now ready to implement the second part of the console IOBYTE feature. This will allow the logical console input to be obtained from either of two keyboards. One of these keyboards will be the video terminal; the other will be the printer. If you don't have a second keyboard, go on to the next section.

Locate the console status and the console input routines. These are found from the second and third entries of the jump table of BIOS. Your present console-input routine may be coded in one of two ways. One method is straight-forward. The input routine has a status check independent of the regular BIOS status routine.
```

;
; CONSOLE INFUT ROUTINE
\hat{p}
CONIN: IN CSTAT OGET STATUS
ANI CIMSK 夕MASK FOR INPUT
JZ CONIN \LOOF UNTIL FEANY
* . *

```

The other method uses the BIOS status routine.
```

g
; CONGOLE INPUT ROUTINE
g
CONIN: CALL CONST \&GET STATUS
JZ CONIN \hat{LOOF UNTIL REAIIY}

```

Although either method can be altered to include the IOBYTE feature, the former method will be demonstrated here. We will need two separate input routines. One is for the video screen and the other is for the printer or other keyboard. Our new console input routine might look like this.
```

%
; LOGICAL CONSOLE INPUT
f
CONIN: LDA IOBYTE gGET ASSIGNMENT
ANI 2 जMASK FOR LIST
JNZ LISTIN \hat{QLIST INFUT}

```
```

g
UIDEO INPUT
\&
UIMIN: IN CSTAT BGET STATUS
ANI CIMSK \MASK FOR INPUT
JZ UIDIN ILOOP UNTIL READY
IN CDATA ;GET IIATA
ANI 7FH \hat{MASK PARITY}
RET
%
INPUT FROM FRINTER
\hat{p}
LISTIN: IN LSTAT GGET STATUS
ANI LIMSK ЯMASK FOR INFUT
JZ LISTIN BLOOF UNTIL REAIIY
IN CLATA igET INATA
ANI TFH OMASK FARITY
RET

```

The third jump statement at the beginning of BIOS should branch to the label CONIN. The IOBYTE at memory address 3 is read. All bits but bit 1 (the second bit) are zeroed with the ANI 2 command. List input corresponds to an IOBYTE of 2 or 3 . The logical AND with 2 and either value will produce the result of 2 .
\begin{tabular}{rrrl}
00000010 & or & 00000011 & IORYTE \\
10 & & 10 & ANA with 2 \\
-00000010 & 0000 & 0010 & \(=2\)
\end{tabular}

The JNZ instruction will then cause a branch to the list-input routine. Otherwise, program flow will continue on to the console-input routine.

A similar construction can be used for the console status routine.
```

%
; LOGICAL CONSOLE-INPUT STATUS
;
CONST: LDA IOBYTE OGET ASSIGNMENT
ANI 2 OMASK FOR LIST
JNZ LISTST iLIST
\hat{g}
% INPUT FROM UILEEO
USTAT: IN CSTAT {CHECK STATUS
ANI CIMSK ЭMASK FOR INFUT
RZ %NO REALIY
MUI AgOFFH SSET FOR REAMY
RET
\hat{p}
{ INPUT FROM LIST
\hat{%}
LISTST: IN LSTAT OCHECK STATUS
ANI LIMSK \&MASK FOR INPUT
RZ INOT READY
MUI A,OFFH ASET FOR REALIY
RET

```

Assemble the new version of BIOS and try it out as we did in the previous section. Load the debugger, then use it to change the IOBYTE at address 3. First, change the IOBYTE to a value of 3 . This will assign the logical console input to the printer (or other alternate keyboard) and logical console output to the video screen. As soon as you make the change, all further input must come from the printer. Use the debugger to change the IOBYTE to a value of 2 . Now logical console input must come from the printer, and logical console output will appear at the printer. Finally, change the IOBYTE back to the value of zero. Console input and output should both go through the video terminal.

\section*{USING STAT TO CHANGE THE IOBYTE}

The CP/M program called STAT can be used to symbolically change the IOBYTE. STAT can also be used to determine the current value of the IOBYTE. Each of the four logical devices CON: (console), RDR: (reader), PUN: (punch), and LST: (list) can be assigned to four different physical devices.
\begin{tabular}{llllc} 
Logical device & \multicolumn{4}{c}{ Physical device } \\
& & 1 & 2 & 3 \\
\hline CON: console & TTY: & CRT: & BAT: & UC1: \\
RDR: reader & TTY: & PTP: & UR1: & UR2: \\
PUN: punch & TTY: & PTP: & UP1: & UP2: \\
LST: list & TTY: & CRT: & LPT: & UL1:
\end{tabular}

The first column represents the four logical peripherals. The remaining entries on each line represent the four physical devices. You can easily change these names in STAT to something more descriptive. Load STAT into memory with the debugger.
```

DIT STAT.COM

```

Then dump the first few lines.
```

D100 16F

```

You will see the names of the logical peripherals and the physical peripherals encoded in ASCII. You can now change any of the names to something else. You might want to choose the names

CRT:
LST:
LPT:
LCR:
for the four console devices. These four names correspond to the IOBYTE values of 0 through 3 . After you change the names with the debugger, return to CP/M and save the altered STAT. If the IOBYTE is currently set to zero and you type the command

\section*{ADSTAT CON:=LST:}

STAT will change the IOBYTE to a value of 1 and console output will appear at the printer. The IOBYTE can be set back to zero with the command

\section*{A \(\triangle\) STAT CON: \(=\) CRT:}

If you have other peripherals, such as a phone modem, these can also be incorporated into IOBYTE. The logical punch can then be sent to the modem, the printer, or the console. A disk file can be sent over the phone modem with the command

\section*{ASTAT FUN:=B:CPMIO.ASM}
where CPMIO.ASM is a disk file on drive B. As you can see, there is room for a lot of imagination.

\section*{A ROUTINE TO GO ANYWHERE IN MEMORY}

The assembly language program shown in Listing 10.1 can be used to branch to any location in memory. Executable programs in CP/M are usually designed to be run starting at address 100 hex, since this is where programs are loaded by CP/M. There are times, however, when it is desirable to assemble a program for operation at some other location. The system monitor developed in Chapter 6 is one such program. If this monitor is to be located in ROM, then it must be placed above the \(\mathrm{CP} / \mathrm{M}\) operating system. A location of F000 hex would be ideal. But there is no easy way to get to the monitor from the \(\mathrm{CP} / \mathrm{M}\) system. If the GO routine is located on disk drive \(A\), then we have only to give the \(\mathrm{CP} / \mathrm{M}\) command
\[
A>G 0 \quad F 000
\]
and a branch will occur to the address F000 hex.
The GO program demonstrates several of the I/O features available with \(\mathrm{CP} / \mathrm{M}\). The branch address given as an argument on the above command line is read from a region of memory called the file-control block (FCB). The address of the FCB is 5C hex but the ASCII-encoded address starts at 5D hex. The input address, F000 in this example, is a valid hexadecimal number; it is to be converted from ASCII into a 16 -bit binary number. The result is placed into the CPU program counter so that the computer will branch to the desired address. The address format is free-form, and leading zeros are

\begin{tabular}{|c|c|c|c|c|c|}
\hline & & ```
; BLANK
; ELSE
%
``` & AT END AN ERROF & OF LINE & IS OK \\
\hline 0138 & FEFO & RDHL 4： & CPI & ，＇－\({ }^{\prime}\) & \\
\hline 013 A & C8 & \multicolumn{4}{|c|}{FZ} \\
\hline & & \multicolumn{4}{|l|}{；Improfer argument．try again \％} \\
\hline O13B & 117501 & ERFOR： & LXI & M，MESG & OPOINT TO MESSAGE \\
\hline O13E & C45901 & & CALL & FRINT & \％SENI IT \\
\hline 0141 & 119001 & & LXI & LI，RBUFM & SINPUT BUFFER \\
\hline 0144 & CH5E01 & & CALL & READE & igET A LINE \\
\hline 0147 & 1600 & & MUI & 1． 0 & \\
\hline 0149 & 3A9E01 & & LIA & REUFL & \％BUFFER LENGTH \\
\hline 014C & 5F & & MOV & EgA & \\
\hline 014 D & 219F01 & & LXI & HoREUF & \\
\hline 0150 & 19 & & LAD & \(\square\) & OFAST EUFFER \\
\hline 0151 & 3620 & & MUI & M\％＇， & ¢PUT IN ELANK \\
\hline 0153 & \(219 \mathrm{FO1}\) & & LXI & HsREUF & \\
\hline \multirow[t]{3}{*}{0156} & C30901 & & JMP＇ & AGAIN & ATRY AGAIN \\
\hline & & 令 & & & \\
\hline & & ；PRINT & \multicolumn{3}{|l|}{CHARACTERS UNTIL \＄IS FOUNA} \\
\hline 0159 & 0E09 & PRINT： & MUI & C．PBUF & \＃SET FOR FREINT \\
\hline \multirow[t]{3}{*}{0158} & C30500 & & JMF & BLOS & \\
\hline & & 名 & & & \\
\hline & & INPUT & A LINE & FFOM CONS & SOLE \\
\hline \multirow[t]{4}{*}{\[
\begin{aligned}
& 015 E \\
& 0160
\end{aligned}
\]} & OEOA & \multirow[t]{2}{*}{REALIE：} & MUI & CyRDBUF & OREAL INFUT BUFFER \\
\hline & C30500 & & \multirow[t]{2}{*}{JMP} & \multirow[t]{2}{*}{BROS} & \\
\hline & & ； & & & \\
\hline & & ；GET A & \multicolumn{2}{|l|}{CHARACTER FFIOM T} & THE INPUT BUFFER \\
\hline 0163 & E5 & GETCH： & FUSH & H & \\
\hline 0164 & 2A9801 & & LHLD & REUFF & \％GET PQINTEF \\
\hline 0167 & 7E & & MOV & A，M & PGET NEXT CHAR \\
\hline 0168 & 23 & & INX & H & S INCREMENT FOINTEF \\
\hline 0169 & 229801 & & SHL & REUFF & SSAUE FOINTER \\
\hline 016C & FE61 & & CFI & ＇ \(\mathbf{z}^{\prime}+7\) & ¢ \(1 P F E E\) CASE？ \\
\hline O16E & DA7301 & & JC & getce & pNO \\
\hline 0171 & EG5F & & ANI & SFH & FMAKE UPPER CASE \\
\hline 0173 & E1 & GETC2： & POF & H & \\
\hline \multirow[t]{2}{*}{0174} & C9 & & RET & & \\
\hline & & \multicolumn{4}{|l|}{MESG：} \\
\hline 0175 & 4745206572 & & UB & ＇GO error & or．Iriput \({ }^{\text {che }}\) \\
\hline 0185 & 7468652061 & & DE & ＇the add & dress asair．＇ \\
\hline \multirow[t]{2}{*}{0197} & ODOA2A24 & & LIB & \multirow[t]{2}{*}{CFigF\％＇种} & ＊＊＇ \\
\hline & & \multicolumn{2}{|l|}{\(\hat{0}\)} & & \\
\hline 0198 & 9501 & REUFF： & ［1W & REUF & ABUFFER POINTER \\
\hline 0190 & OA & REUFM： & HE & 10 & SMAX SIZE \\
\hline O19E & & RBUFL： & IIS & 1 & ¢ACTUAL SIZE \\
\hline 019F & & \begin{tabular}{l}
RBUF： \\
\％
\end{tabular} & 105 & 1 & A INPUT RUFFER \\
\hline Q1AO & & & END & & \\
\hline
\end{tabular}
unnecessary. If more than four characters are entered, only the last four are used. Thus, all of the following are valid.
\begin{tabular}{ll}
0 & F000 \\
900 & PF800 \\
6000 &
\end{tabular}

If no argument is given to the GO command, or if an invalid hexadecimal address is entered, then an error message is printed. This step uses the console string-output feature, selected with the function code of 9 in register C. The DE register pair is loaded with a pointer to the string location in memory. A dollar sign ( \(\$\) ) is used to indicate the end of the string. In subroutine SENDM of Chapter 6, a binary zero is used for this purpose since it requires less code.

The user can retype the desired address after the error message has been printed. This time, however, the program reads the input string data in a different way. The console string-input operation is selected by loading the C register with the function number of 10 . If the new string is a valid hex number, it is converted to a 16 -bit binary number. The computer then jumps to this address. If the input is still invalid, the error routine is repeated again.

During the input operation, the usual \(\mathrm{CP} / \mathrm{M}\) commands are available for error correction. For example, the most recently typed character can be deleted by pressing the DEL key. A control-R will reprint the current line in its corrected form. A control-U cancels the entire line so that it can be retyped. If Version 2 of \(\mathrm{CP} / \mathrm{M}\) is being used, then the backspace character, control-H, can also be used for correcting errors. Finally, a control-C can be entered to abort the entire program. This returns control to the \(\mathrm{CP} / \mathrm{M}\) operating system.

Enter the GO program in Listing 10.1. Assemble it and try it out. GO is a universal program; it will work on any system. If you have a monitor located in memory, use GO to branch to it; if not, you can still try out the GO program. Type just the command of GO without an argument. An error message should be printed. Type some characters, then delete some of them with the DEL key. The deleted characters will be printed a second time. Reprint the line with a control-R to see the correct version. Finally return to CP/M by giving the address of zero.

\section*{GO 0}

A control-C can also be used to return to CP/M.

\section*{A LIST ROUTINE WITH DATE AND TIME}

In Chapter 7 we developed a monitor routine for sending data to a separate list device. When this routine is activated with a control-P command, the output appears at both the console and the printer. \(\mathrm{CP} / \mathrm{M}\) has a similar
arrangement. A control-P command will activate the list device, too. Output is then sent to both the console and the printer.

But the console and list routines are entirely separate in \(\mathrm{CP} / \mathrm{M}\). Output can therefore be sent specifically to the list device and it will not appear on the console. In CP/M I/O operations, a function number of 2 corresponds to console output, and a function number of 5 corresponds to list output. If memory address 5 is called with a value of 2 in the C register, then the byte in the \(E\) register will be displayed on the system console. On the other hand, if a function number of 5 is placed in the \(C\) register, then the byte in register E will appear on the list device. The byte in the E register can be sent to the punch by loading a function number of 4 into the \(C\) register.

This complexity may seem unnecessary, since the list device can be turned on by typing a control-P. If the command

\section*{A〉TYPE 氏filename>}
were given, then the file would be sent to both the console and the printer. The disadvantage of this method is that the TYPE command line will appear on the printer output. Also, when the listing is finished, the new prompt of \(\mathrm{A}>\) will be printed on the listing.

The CP/M utility program PIP can be used to send a disk file specifically to the list device. The command is
```

A.FIF LST:=\&ilename>[T8]

```

The argument T8, embedded in brackets, will expand the ASCII tab character to 8 -column fields. PIP, however, does not automatically eject a new page when a form feed is encountered.

The LIST program in Listing 10.2 can be used to send an ASCII disk file to the printer, too. It will automatically expand the ASCII tab character. Furthermore, when a form-feed character is encountered, LIST will add the correct number of lines to the end of the page. At the end of the disk file, additional line feeds are issued to finish the page. This will ensure that the printer will start the next task on a new page. If the file contains an odd number of pages, then an extra blank page is added to the end. Without this feature you will have to refold about half of the output.

If your computer keeps track of the date and time, LIST can print current values at the top of the first page. The name of the disk file is also printed on this line.

LIST is a very small program, requiring only 1 K bytes of memory. It was derived from the program called DUMP in the CP/M Interface Guide. LIST bears only a passing resemblance to DUMP, however. DUMP is designed to convert binary files to ASCII-hex characters and display them on the console. LIST, on the other hand, prints ASCII files directly with no conversion. Since the CP/M BDOS is used for all I/O and disk operations, LIST will operate with all standard CP/M systems.

```

0110210000
0113016000
0116 OA
0117 FE20
0119 CA4001
011C FE46
011E CA3CO1
0121 FE50
0123 CA3601
0126 11630

```
```

012854
012951
012A 29
012B29
012C 19
012D 29
O12E 5F
012F 1600
013119
013203
0133 c31601

```
0136320904
0139 C33F01
013 C 3211804
\(013 F \mathrm{AF}\)
014022 LAO 4
0143 CDE302
0146 3E80
0148 32DEO4
\(014 \mathrm{E} 32 \mathrm{D3} 04\)
OIAE 2ALIAOA
0151 7C
\(0152 \mathrm{B5}\)
0153 CAG401
0156 ES
\(0157 \mathrm{CD4302}\)
015A E1
O15B FEOM
0150 C 25601
01602 E
0161 C 35101
0164 AF
0165321504
0168 CD4302
016 BE 5
;
HOW MANY LINES TO SKIF BEFORE STARTING? ;
\begin{tabular}{|c|c|c|c|}
\hline \multirow{4}{*}{SKIF゙2:} & LXI & \(\mathrm{H}, \mathrm{O}\) & \\
\hline & LXI & B, 6INH & Q 3RD ARGUMENT \\
\hline & LIIAX & B & GET CHARACTER \\
\hline & CFI & , ' & ¢BLANK AT END \\
\hline & JZ & SKIF3 & GDONE \\
\hline & CFI & 'F' & ONEED FORM FEEIIS? \\
\hline & \(J Z\) & FORM & gYES \\
\hline & CPI & 'F' & 9EXTRA FAGE? \\
\hline & JZ & NOFAGE & ¢ NO \\
\hline & SUI & '0' & ¢FEMOUE ASCII BIAS \\
\hline
\end{tabular}
\(\hat{\text {; }}\) CONUERT ASCII LECIMAL TO BINARY IN H;L
i
\begin{tabular}{|c|c|c|c|}
\hline & MOV & DOH & ¢ IUFLICATE \\
\hline & MOU & E, & कH\%L IN M\%E \\
\hline & LIAD & H & OTIMES 2 \\
\hline & LIAD & H & ¢TIMES 4 \\
\hline & DAD & 0 & OTIMES 5 \\
\hline & LIAD & H & ¢TIMES 10 \\
\hline & MOV & E,A & \\
\hline & MUI & D.0 & \\
\hline & IIAII & 1 & ¢AMLI NEW BYTE \\
\hline & INX & B & ¢INCR FOINTER \\
\hline & JMF' & SKIF2 & gNEXT \\
\hline \multicolumn{4}{|l|}{\(\hat{9}\)} \\
\hline NOPAGE: & STA & FFLAG & gNO EXTRA FAGE \\
\hline & JMF & ZERO & \\
\hline \multicolumn{4}{|l|}{¢} \\
\hline FOKM: & STA & FFLAG & SSET FOR FORM FEELS \\
\hline ZERO: & XFA & A & ¢RESET COUNT \\
\hline SKIF'3: & SHLII & SKIFB & ¢SAUE EINARY CNT \\
\hline \multicolumn{4}{|l|}{\multirow[t]{2}{*}{\(\hat{\text { 今 }}\), REAL AS MUCH AS POSGTELE INTO MEMORY}} \\
\hline & & & \\
\hline
\end{tabular}
\begin{tabular}{lll} 
CALL & SETUF & ISET UF INFUT FILE \\
MUI & A \(8 O H\) & \\
STA & IBF & ©SET FOINTER TO \(8 O H\)
\end{tabular}
            STA TIME O ASET \(1 S T\) FASS
!

MAING:
LHLD SKIP ЯHOW MANY LINES?
AgH
\(\mathrm{L} \quad \hat{\mathrm{H}} \mathrm{L}=\mathrm{O}=\mathrm{P}\) MAINS SNO SKIF
MAIN7: FUSH H
CALL GNB ONEXT EYTE
FOF H
CPI CR
JNZ MAIN7 \(\quad\) LOOK FOF CR
IICX H OLIECR COUNT
JMP MAING
;
MAINS: XRA A
STA FULL ifESET FLAG
MAIN2: CALL GNB \(\hat{G E T}\) A BYTE
\begin{tabular}{|c|c|}
\hline 016 C & 2 ADCO 4 \\
\hline 016F & 77 \\
\hline 0170 & 23 \\
\hline 0171 & 22 nc 4 \\
\hline 0174 & 47 \\
\hline 0175 & 3EFF \\
\hline 0177 & BD \\
\hline 0178 & C28B01 \\
\hline 017E & 300700 \\
\hline 017E & 1160A \\
\hline 0180 & BC \\
\hline 0181 & 1028E01 \\
\hline 0184 & 3E1A \\
\hline 0186 & 77 \\
\hline 0187 & \(32 \times 504\) \\
\hline 018A & 47 \\
\hline 0188 & 78 \\
\hline 018C & E1 \\
\hline 018 I & FEIA \\
\hline 018F & C26801 \\
\hline
\end{tabular}
0192 2ADCOA
01952 B
0196 3E1A
0198 BE
\(0199 \mathrm{CAA101}\)
019 C 23
019 D
\(019 E\)
22 ACOA
\(01 A 1\) CA7CO2

\begin{tabular}{|c|c|c|}
\hline CALL & Clock & GGET TIME \\
\hline LILA & FFLAG & ¢FORMFEEIS? \\
\hline ORA & A & \\
\hline CNZ & TWOLN & ¢ YES \\
\hline CALL & GETB & GGET EYTE \\
\hline CPI & FORMFII & AFORMFEEI \\
\hline JNZ & GLOF2 & ¢ NO \\
\hline CALL & TWOLN & ¢SENH 2 LF \\
\hline CALL & GETB & gGET NEXT EYTE \\
\hline MOV & ByA & ¢SAUE EYTE \\
\hline CALL & TABO & \%PRINT EYTE \\
\hline MOV & \(A, B\) & tGET BYTE AGAIN \\
\hline CFII & LF & \%ENLI OF LINE? \\
\hline JNZ & GLOOF & ¢ NO \\
\hline LIMA & LCOUNT & ¢GET COUNT \\
\hline INF & A & \$INCREMENT IT \\
\hline STA & LCOUNT & ¢SAVE IT \\
\hline CPI & LMAX & ¢TOO MANY? \\
\hline CNC & NPAGE & GYES, FEESET \\
\hline LDA & FFLAG & AFORM FEEDS? \\
\hline
\end{tabular}


```

0268 E1
0269 E67F
026B FE1A
0261 C0
026E F1
026F 3ALI504
0272 B7
0273 CA8E02
0276 C口7C02
0279 c36401
027C E5
0270210005
0280 220C04
0283 E1
0284 C9
0285 110204
0288 CD3EO2
028B C3AEO2
0294 3A11904
0297 B7
0298 C2AEO2
029B 3AD704
029E E601
O2AO CAAEO2
02A3 0642
O2A5 3EOA
02A7 CNO4O2
02AA 05
02AE C2A502
O2AE 2AE004
02B1 Fg
02B2 C9

```
```

%

```
%
FOP H
FOP H
ANI TFH \hat{STRIF FARITY}
ANI TFH \hat{STRIF FARITY}
CPI EOF
```

```
CPI EOF
```

```


```

```
LMA FULL \hat{FCHECK FLAG}
```

```
LMA FULL \hat{FCHECK FLAG}
ORA A OZERO?
ORA A OZERO?
JZ FINIS GYES, DONE
JZ FINIS GYES, DONE
CALL RESET FFOINTER
CALL RESET FFOINTER
JMF MAINS OGET MORE
JMF MAINS OGET MORE
\hat{g}
\hat{g}
; NORMAL END OF OF LISTING
; NORMAL END OF OF LISTING
#
#
FINIS: STA EOFFL ASET EOF FLAG
FINIS: STA EOFFL ASET EOF FLAG
%
%
    CALL FILL s
    CALL FILL s
AMD AN EXTRA FAGE IF THERE IS AN OMI NUMEER
AMD AN EXTRA FAGE IF THERE IS AN OMI NUMEER
& AND F FLAG IS NOT SET
& AND F FLAG IS NOT SET
    LDA FFLAG
    LDA FFLAG
ORA A SZERO?
ORA A SZERO?
JNZ AHOR2 \NNO
JNZ AHOR2 \NNO
LDA PAGES SHOW MANY?
LDA PAGES SHOW MANY?
ANI 1 sODI?
ANI 1 sODI?
JZ ABOR2 SNO
JZ ABOR2 SNO
j.
j.
; AMII blaNK fage to makE EUEN
; AMII blaNK fage to makE EUEN
%
%
* (CAN WE CALL FILL?)
* (CAN WE CALL FILL?)
    MUI BILMAX कLINES
    MUI BILMAX कLINES
EFAGE: MUI A,LF
EFAGE: MUI A,LF
EFAGE: MUI A,LF
EFAGE: MUI A,LF
    CALL FCHAR
    CALL FCHAR
    IICF B
    IICF B
    JNZ EPAGE
    JNZ EPAGE
\hat{0}
\hat{0}
ABOF2:
ABOF2:
ABOR3:
ABOR3:
\begin{tabular}{|c|c|c|}
\hline F'OP & H & \\
\hline ANI & 7FH & QSTRIF FARITY \\
\hline CPI & EOF & \\
\hline RNZ & & \\
\hline POF & FSW & ¢FAISE STACK \\
\hline LDA & FULL & ¢ CHECK FLAG \\
\hline ORA & A & © ZERO? \\
\hline JZ & FINIS & - YESY DONE \\
\hline CALL & RESET & FFOINTER \\
\hline JMF & MAINS & GGET MORE \\
\hline
\end{tabular}
```

```
\hat{p}
```

\hat{p}

```
\hat{p}
; FESET MEMORY FOINTER
; FESET MEMORY FOINTER
; FESET MEMORY FOINTER
%
%
%
RESET: FUSH H
RESET: FUSH H
RESET: FUSH H
LXI H,BUFFER
LXI H,BUFFER
LXI H,BUFFER
SHLD EUFFF
SHLD EUFFF
SHLD EUFFF
FOF H
FOF H
FOF H
RET
RET
RET
%
%
%
NONAME: LXI IMMES1 {POINT TO MESSAGE
NONAME: LXI IMMES1 {POINT TO MESSAGE
NONAME: LXI IMMES1 {POINT TO MESSAGE
FINI3: CALL FRINT
FINI3: CALL FRINT
FINI3: CALL FRINT
    JMF: ABOR2
    JMF: ABOR2
    JMF: ABOR2
```

    *T
    ```
    *T
```

    *T
    
# 

# 

    LHLII OLIISF SOLII STACK FOINTEF
    LHLII OLIISF SOLII STACK FOINTEF
    SPHL
    SPHL
    RET
    RET
    i
i
; SETUF FILE AND OFEN FOR INFUT

```
; SETUF FILE AND OFEN FOR INFUT
```

```
ll
O2BE FEFF
02BI CAC5O2
O2C0 AF
O2C1 327C00
02C4 C9
#
& CMECK FOR ERFORS
\ CFI 255
\hat{%}\mathrm{ OPEN IS OK}
%
ll
ll
ll
ll
ll
ll
ll
ll
\hat{g}
% REAO IISK FILE RECORD
O2DAES DISKR: FUSH H
O2NE 05
O2nc C5
024n 115C00
O2EO OE14
O2E2 CDOSOO
02E5 C1
O2E6 01
O2E7 E1
O2E8 E7
O2E9 C8
O2EA FEO1
02EC CAF502
O2EF 111104
O2F2 C3AEO2
02F5 2ANCO4
02F8 361A
02FA C3A101
XFIA A
STA FCBCR
FET
\hat{g}
` BAII OFEN
*
BALIOFN: LXI
                            MOV
                            CFI
JZ
LXI Hy'?$' SSET UF FOF FRINT
SHLII FCBRL \hat{USE INFUT FILENAME}
```



```
JMF FINI3 कQUIT
#
                    FUSH D
                    FUSH : B
                            LXI MyFCE
                    MUI C,FEALF
                                    CALL BLIOS
                                    FOF B
                    POF II
                    FOF H
                    ORA A 言HECK FOR ERRS
                            KZ
& MAY EE EOF
            CFI 1
            JZ FENII \EOF
            LXI HOMES2
                    JMF AROOFS
\hat{q}
FOUNA LISK EOF
;
FENI: LHLII BUFFF {GET FOINTER
                    MUI M,EOF \hat{FUT INIA}
                    JMF: MAINZ
                    ;
                    ; TAB COUNTER ROUTINE
                    JUMF HERE WITH BYTE IN E
```

| SETUF: | LXI | IIFFCB |
| :--- | :--- | :--- |
|  | MUI | CyOFENF |
|  | CALL | BNOS |


| 0283 | $115 C 00$ |
| :--- | :--- |
| 0286 | OEOF |
| 0288 | CNO |



| 0358 | 3 E 20 | BLANK: | MUI | A, |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 035A | C30402 |  | JMP | PCHAF | OSENI IT |
|  |  | ; |  |  |  |
| 0351 | DEC4 | CLOCK: | IN | ADATA | ; EOARI FRESENT? |
| 035 F | FEFF |  | CFI | OFFH |  |
| 0361 | C8 |  | RZ |  | ¢ NO |
| 0362 | 3AD304 |  | LDA | TIMEZ | FPASS? |
| 0365 | B7 |  | ORA | A | ¢ ZERO? |
| 0366 | C8 |  | RZ |  | \%NOT 15T |
| 0367 | AF |  | XRA | A |  |
| 0368 | 321304 |  | STA | TIME2 | \#SET 15T |
| 036E | 21 DEO3 |  | LXI | HyMON |  |
| 036E | CDA703 |  | CALL | LATE | ¢GET IT |
| 0371 | $21 E D 03$ |  | LXI | H. HOUF |  |
| 0374 | Cncoo3 |  | CALL | TIME |  |
| 0377 | 2111703 |  | LXI | H, FIAATE | ¢FOINT LAATE/TIME |
| 037A | clusa03 |  | CALL | SENH |  |
| 037 I | AF |  | XRA | A | jGET A ZERO |
| 037E | 326900 |  | STA | FCB+13 | SNAME ENI |
| 0381 | 2151000 |  | LXI | H,FCEFN | jNAME START |
| 0384 | CDBA03 |  | CALL | SENI | ¢ SHOW |
| 0387 | $21 F F 03$ |  | LXI | HySCRLF |  |
|  |  | \% |  |  |  |
|  |  | - SENH | MESSAGE | To LIST |  |
| 038A | 7E | SEND: | MOV | A, M | gGET BYTE |
| O388 | B7 |  | OFA | A | ; ZERO AT ENI |
| 038C | C8 |  | RZ |  | GIIONE |
| 03818 | CDO402 |  | CALL | FCHAR | 'SEND CHARACTER |
| 0390 | 23 |  | INX | H | ¢ INCREMENT FQINTER |
| 0391 | C38A03 |  | JMF' | SEND |  |
|  |  |  |  |  |  |
|  |  | ; REAII $\hat{y}$ | A MTGIT |  |  |
| 0394 | 7A | FuIGIT: | MOV | A, II | ¢SELECT DIGIT |
| 0395 | ロ3C4 |  | out | aliata |  |
| 0397 | DEC4 |  | IN | Aliata | \#RESET INTERRUFT |
| 0399 | 18C5 | LUWAIT: | IN | ACONT | ¢LIGIT PRESENT? |
| 0398 | E680 |  | ANI | 80 H |  |
| 0391 | CA9903 |  | JZ | LIWAIT | glode UNTIL FEADY |
| 03 AO | neca |  | IN | aliata | ; REAL A MIGIT |
| 03A2 | E60F |  | ANI | OFH | ¢MASK |
| 03 A4 | F630 |  | ORI | 3 OH | ¢CONUEFT TO ASCII |
| O3AG | C9 |  | FET |  |  |
|  |  | \% |  |  |  |
|  |  | FREAL-DATE ROUTINE |  |  |  |
| 03 A 7 | AF | IIATE: | XF'A | A | ¢DATE IIISFLAY MODE |
| 03 A8 | $113 C 6$ |  | OUT | Emata |  |
| OJAA | 4F |  | MOV | $C, A$ | jTHIS IS LATE |
|  |  | \% |  |  |  |
|  |  | ; REAL | FOUR AIG | ITS |  |
| O3AE | 1600 | REALI4: | MUI | [1.0 | \% SELECT FIRST nIGIT |
| OBAD | C19403 | Rll4: | CALL | RUIGIT | - melar one digit scan |
| 03 EO | cacnoz |  | CALL | RSIIG | YREAI \& STORE UIGIT |
| $03 \mathrm{B3}$ | 7 A |  | MOV | $\mathrm{A}, \mathrm{II}$ |  |
| 03 B 4 | FE20 |  | CPI | 2 OH | 9TWO DIGITS DONE? |


| 0386 | c2baO3 |  | JNZ | SKIF | SSKIF A Flace |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0389 | 23 |  | INX | H | 引SkIF : OR / |
| 03BA | FE40 | SKIF: | CPI | 4 OH |  |
| 038C | c2anoz |  | JNZ | RII4 | gget another migit |
| 038 F | C9 |  | FET |  |  |
|  |  | $\hat{\mathrm{g}} \text { READ }$ | TIME \& | FEAII ANO | Store migit |
| 03 CO | $3 E 40$ | TIME: | MUI | A. 40 H | ¢time disflay mone |
| 03 C 2 | 13C6 |  | ou' | bIata |  |
| 03 C 4 | OEO1 |  | mul | C. 1 | this is TIME |
| $03 \mathrm{C6}$ | cdaboz |  | CALL | FEADA | \%GET 4 IIGITS |
| $03 \mathrm{C9}$ | 23 |  | INX | H | ¢SKIF COLON |
| 03CA | cucnoz |  | CALL | RSuIG |  |
| 03 CD | C199403 | FSDIG: | CALL | RIIgit |  |
| 03 n 0 | 77 |  | mov | M, A | ¢STORE BYTE |
| 0301 | 23 |  | INX | H | ;INCR FOINTER |
| 0312 | 7A |  | MOU | A. ${ }^{\text {I }}$ |  |
| 0303 | C610 |  | Alli | 10 H |  |
| 0305 | 57 |  | MOU | 1, A |  |
| 0306 | C9 |  | RET |  |  |

$\stackrel{\rightharpoonup}{9}$
©STORAGE AREA
$\hat{\text { g }}$
FLATE:


|  | و |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | \% | STACK | AREA |  |
| O4E0 | OLISF: | U15 | 2 | ¢OLI STACK |
| OAE2 |  | 115 | 30 | ¢ STACK SFACE |
|  | STACK: |  |  | 9NEW STACK |
| 0500 | BUFFER: ; | $\underline{1} 5$ | 1 | GMEMORY BUFFER |
| 0501 |  | ENII |  |  |

LIST can be executed by the command

```
A\LIST <filename> <oftional arsument>
```

The CP/M system copies LIST into memory at 100 hex and branches to it. The first step is to save the incoming stack pointer and set up a new one. The clock routine is executed next. The routine shown in Listing 10.2 is written for a Computime R clock board, but the program can be altered to accommodate other methods of timekeeping. The first step of the clock routine is to see if there is a clock board in the computer. One of the clock ports, at address ADATA, is read. If there is no port at this I/O address, the computer will read a value of FF hex. This will harmlessly terminate the subroutine with a return instruction.

If a clock board is present, then the first line of the printer output will appear in the form

Mate 06/15/80 Time 13:18:33 FILE: ©filename
The next step is to see if one of the three optional arguments was given after the filename. These arguments are:

| F | (add form feeds) |
| :--- | :--- |
| P | (no extra page at end) |
| decimal number | (skip lines at beginning) |

The letter F is used to insert form feeds every 58 lines of the listing. The command looks like this.

```
ANLIST SORT,FAS F
```

This feature is useful for listing BASIC, FORTRAN, Pascal, or assemblylanguage source programs. If this argument is selected, the proper number of line feeds is generated as the end of the page is approached. This step causes the printer to skip over the fold in the paper. Also, any form feeds that are encountered are ignored.

If the letter $P$ is given for the argument, then no extra blank page is generated at the end. This argument can be used to save paper when several one-page files are printed.

Another possible argument to LIST is a decimal number. In this case, the argument tells how many lines of the file are to be skipped. For example, the command

## ALIST LINFIT.FOR 500

will skip the first 500 lines and start the listing with line 501 . Use this option if you want to print the last part of a long file but don't want to wait for the first part to be printed.

At this point, the disk directory is searched for the requested filename. This filename is retrieved from the file-control block at address 5C hex. If the requested filename can't be found in the directory, then the filename is printed on the console along with a question mark. LIST is then aborted. If no filename was entered, an error message stating this fact appears on the console. LIST is aborted in this case also. LIST could have been programmed to handle input errors the way that the GO routine does. Then, instead of aborting, LIST would ask for the filename to be entered again. The addition of this feature is left as an exercise for the reader.

If the filename exists in the directory, then the requested disk file is read. The proper number of lines are skipped over if the second argument of the command line was a valid decimal number. At this point, the disk file is read into memory. The FDOS address located at address 7 is checked to see how much memory is available. The entire file will be copied into memory if there is room. A check is made to see if the disk end-of-file character is encountered before the available memory is filled.

In either case, the date and time of day are printed first. Then the data in memory are printed. The first character is ignored if it is an ASCII form feed. This will prevent a page eject immediately after the date and time. The ASCII tab character is properly expanded by the routine TABO. The number of lines is counted. When a form-feed character is encountered, the proper number of line feeds is issued to fill out the page. If the F argument was given, the form feeds will be automatically issued.

LIST can be aborted at any time during the printing by pressing any console key. The console is checked for this after each carriage return. The CP/M program DUMP is set up a little differently. The disk data are read into a 128-byte buffer, rather than into the memory area above 100 hex. Using a small buffer has the advantage that programs can be stored in memory during the DUMP operation and they will not be erased. But, in return, there is a lot of disk activity. The disk must be accessed every 128 bytes.

## COPY A DISK FILE INTO MEMORY

If you have programmed one of the tape routines given in Chapter 8, then you can make backup copies of your disk files. But you have to first copy the disk file into memory. The copy step can be performed with the debugger DDT or SID.

## 

This command loads the debugger at address 100 hex and branches to it. The debugger relocates itself into high memory, then copies the requested disk file into memory starting at 100 hex. The address of the end of the disk file in memory is printed in hexadecimal. This address can be used in conjunction with the memory map given in Appendix B to determine the number of 256 -byte blocks in the file. For example, if DDT gives a value of 13 AF , then the disk file occupies 19 (decimal) blocks of 256 bytes.

When the file has been copied into memory, the G command in the debugger can be used to branch to the tape routine. Then the SAVE command can be given to make a copy on tape. The process can be reversed by loading the file into memory from tape. Branch to address zero to restart CP/M. Finally, give the SAVE command

## A>SAVE $X X$ <filenamè

where XX is the decimal number of 256 -byte blocks to be saved.
This procedure can be simplified by using the FETCH program given in Listing 10.3. FETCH uses CP/M for all I/O and disk operations, so it should work with all standard CP/M systems. There are, however, 2 items that need to be customized. Fetch is initially loaded into memory at 100 hex. It then automatically relocates itself to higher memory. The relocation address is chosen to be F400 hex in Listing 10.3. You may have to change it to some other address if this region is not available. The address is defined by the label ORIGIN in the source program. After FETCH copies the requested disk file into memory, it branches to your tape routine. This address, defined by the label MONIT, is chosen to be F000 hex in Listing 10.3 MONIT should be changed to your tape address.

```
Listins 10.3. Cofs a disk file into memors.
    % (date soes here)
    \hat{g}
    TITLE 'Cofy a disk file into memors,'
    g
    # THIS FROGRAM RELOCATES ITSELF TO HIGH MEMORY THEN
    & COFIES A IISK FILE TO MEMORY STARTING AT 100 HEX.
    ; ASCII ANI COM FILES ARE CORRECTLY HANDLED.
    ; GIUE A THIRD ARGUMENT OF E FOR OTHER BINARY FILES.
    ; A 1A EOF CHARACTER IS FUT AT THE ENI ASCII FILES.
    ; THE LAST AMMRESS ANO MECIMAL BLOCK SIZE ARE GIUEN.
    ; FINALLY A JUMF IS MADE TO THE AIDRESS OF MONIT.
    % QUITS IF NO REAII-WFITE MEMORY AT NEW LOCATION
FOOO = MONIT EQU OFOOOH %GO HERE WHEN DONE
F400 = ORIGIN EQU OF4OOH GFELOCATE FETCH HERE
0100= BUFFEF EQU 100H #START MEMORY ELFFER
0005 = EMOS EQU 5
```








One of the advantages of FETCH is that it is considerably smaller than DDT or SID. In addition, the decimal number of blocks to be saved and the last address of the program are given. FETCH is executed just like the debugger.

## A)FETCH fileriames. <extensions

The CP/M system loads FETCH at 100 hex and then branches to it. The instructions at the beginning of FETCH are used to relocate the rest of the program into a preselected memory area. A jump is then made to the relocated FETCH.

FETCH loads the selected disk file into memory starting at 100 hex. An ASCII file is copied up to the 1A end-of-file mark. Typical extension names include the following.

| ASM | (assembly language) |
| :--- | :--- |
| PAS | (Pascal) |
| FOR | (FORTRAN) |
| BAS | (BASIC) |
| HEX | (hex-encoded binary) |
| TEX | (text formatter) |
| LIB | (library) |
| MAC | (assembly language) |

Executable binary files will have a file extension of COM; the entire file will be copied in this case. If a nonexecutable binary file is loaded, an additional argument of $B$ (for binary) must be given.

FETCH SORT.REL B
Examples of executable binary files are

REL (relocatable)
INT (intermediate)
Relocatable files generated by the Microsoft assembler, and the FORTRAN, COBOL, and BASIC compiler are of this type. Intermediate files are produced by CBASIC.

After the disk file is loaded, FETCH prints two numbers. One number is the memory address of the end of the file expressed in hex. The other number is the size of the file. The number of 256 -byte blocks is printed, in decimal.

Type up the program given in the listing. Assemble it and load it into memory with the debugger
A) LILT FETCH.HEX

The debugger will load the move routine, the first part of FETCH, into memory at 100 hex. The main part of the program, however, will be loaded at the address of ORIGIN, 0F400 hex in this case. Use the debugger to move the main part of FETCH back down to the beginning of the user area.

```
MF400 FSFF 12A
```

Now, return to the CP/M system with a control-C and save the combination of the move program and the main part of FETCH.

## A.SAVE 2 FETCH.COM

FETCH is now ready for use.

## Appendixes

Appendix A The ASCII Character Set ..... 253
Appendix B A 64K Memory Map ..... 255
Appendix C The 8080 Instruction Set (Alphabetic) ..... 258
Appendix D The 8080 Instruction Set (Numeric) ..... 261
Appendix E The Z-80 Instruction Set (Alphabetic) ..... 264
Appendix F The Z-80 Instruction Set (Numeric) ..... 272
Appendix G Cross-Reference of 8080 and Z-80 Instructions ..... 280
Appendix H Details of the Z-80 and 8080 Instruction Set ..... 283
Appendix I Abbreviations and Acronyms ..... 311
Appendix J Undocumented Z-80 Instructions ..... 313

## APPENDIX A

## The ASCII Character Set

The ASCII character set is listed in numerical order with the corresponding decimal, hexadecimal, and octal values. The control characters are indicated with a caret ( $\wedge$ ). For example, the horizontal tab (HT) is formed with a control-I.

| NUL | 0 | 00 | 000 | -1 | Null | 0 | 64 | 40 | 100 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SOH | 1 | 01 | 001 | " $A$ | Start of headins | A | 65 | 41 | 101 |
| STX | 2 | 02 | 002 | ${ }^{\circ} \mathrm{B}$ | Start of text | B | 66 | 42 | 102 |
| ETX | 3 | 03 | 003 | ${ }^{m} \mathrm{C}$ | Erid of text | C | 67 | 43 | 103 |
| EOT | 4 | 04 | 004 | - 1 | Erad of tranismission | 0 | 68 | 44 | 104 |
| ENQ | 5 | 05 | 005 | ${ }^{\text {a }}$ E | Ericuiry | E | 69 | 45 | 105 |
| ACK | 6 | 06 | 006 | mF | Acknowledse | F | 70 | 46 | 106 |
| BEL | 7 | 07 | 007 | -G | Bel1 | G | 71 | 47 | 107 |
| BS | 8 | 08 | 010 | - | Backspace | H | 72 | 48 | 110 |
| HT | 9 | 09 | 011 | $\cdots$ | Horizorital tab | 1 | 73 | 49 | 111 |
| LF | 10 | OA | 012 | -J | Line feed | $J$ | 74 | 4A | 112 |
| UT | 11 | OB | 013 | -K | Vertical tab | $K$ | 75 | 4B | 113 |
| FF | 12 | OC | 014 | mL | Form feed | L | 76 | 4C | 114 |
| CR | 13 | OD | 015 | m | Carriase return | M | 77 | 4 II | 115 |
| S0 | 14 | OE | 016 | -N | Shift out | N | 78 | $4 E$ | 116 |
| SI | 15 | OF | 017 | $\cdots$ | Shift in | 0 | 79 | 4F | 117 |
| DLE | 16 | 10 | 020 | 'F' | Lata link escafe | F | 80 | 50 | 120 |
| DCI | 17 | 11 | 021 | -a | Levice control 1 | 0 | 81 | 51 | 121 |
| DC2 | 18 | 12 | 022 | -R | Device control 2 | $R$ | 82 | 52 | 122 |
| DC3 | 19 | 13 | 023 | -5 | llevice control 3 | 5 | 83 | 53 | 123 |
| DC4 | 20 | 14 | 024 | T | Device coritrol 4 | $T$ | 84 | 54 | 124 |
| NAK | 21 | 15 | 025 | -u | Nesative ackrowledse | U | 85 | 55 | 125 |
| SYN | 22 | 16 | 026 | - $V$ | Surichronous idle | $v$ | 86 | 56 | 126 |
| ETB | 23 | 17 | 027 | -W | Erid transmission block. | W | 87 | 57 | 127 |
| CAN | 24 | 18 |  |  | $==$ |  | 8 |  | 130 |
| EM | 25 | 19 | 031 | my | Erid of medi | Y | 88 | 58 | 131 |
| SUB | 26 | 1 A | 032 | $\cdots$ | Substitute | Z | 90 | 5 A | 132 |
| ESC | 27 | 1 B | 033 | ${ }^{\text {m }}$ | Escafe | [ | 91 | 5 B | 133 |
| FS | 28 | 1 C | 034 | - | File sefarator | 1 | 92 | 5 C | 134 |
| GS | 29 | 1 II | 035 | $\left.{ }^{m}\right]$ | Grous sefarator | ] | 93 | 51 | 135 |
| RS | 30 | 1E | 036 | ] | Record sefarator | m | 94 | SE | 136 |
| US | 31 | 1 F | 037 | m- | Uriit sefarator | - | 95 | 5 F | 137 |


| SP | 32 | 20 | 040 | Sface |
| :---: | :---: | :---: | :---: | :---: |
| . | 33 | 21 | 041 |  |
| $\cdots$ | 34 | 22 | 042 |  |
| * | 35 | 23 | 043 |  |
| \$ | 36 | 24 | 044 |  |
| \% | 37 | 25 | 045 |  |
| 8 | 38 | 26 | 046 |  |
| , | 39 | 27 | 047 |  |
| $($ | 40 | 28 | 050 |  |
| ) | 41 | 29 | 051 |  |
| * | 42 | 2A | 052 |  |
| + | 43 | 2B | 053 |  |
| , | 44 | 2 C | 054 |  |
| - | 45 | 20 | 055 |  |
| - | 46 | 2 E | 056 |  |
| 1 | 47 | 2 F | 057 |  |
| 0 | 48 | 30 | 060 |  |
| 1 | 49 | 31 | 061 |  |
| 2 | 50 | 32 | 062 |  |
| 3 | 51 | 33 | 063 |  |
| 4 | 52 | 34 | 064 |  |
| 5 | 53 | 35 | 065 |  |
| 6 | 54 | 36 | 066 |  |
| 7 | 55 | 37 | 067 |  |
| 8 | 56 | 38 | 070 |  |
| 9 | 57 | 39 | 071 |  |
| : | 58 | 3A | 072 |  |
| \% | 59 | 38 | 073 |  |
| $<$ | 60 | 3 C | 074 |  |
| $=$ | 61 | 3 I | 075 |  |
| 3 | 62 | 3 E | 076 |  |
| ? | 63 | 3 F | 077 |  |


| , | 96 | 60 | 140 |  |
| :---: | :---: | :---: | :---: | :---: |
| 3 | 97 | 61 | 141 |  |
| $b$ | 98 | 62 | 142 |  |
| $c$ | 99 | 63 | 143 |  |
| $d$ | 100 | 64 | 144 |  |
| e | 101 | 65 | 145 |  |
| $f$ | 102 | 66 | 146 |  |
| 5 | 103 | 67 | 147 |  |
| h | 104 | 68 | 150 |  |
| i | 105 | 69 | 151 |  |
| $j$ | 106 | 6A | 152 |  |
| k. | 107 | 6 B | 153 |  |
| 1 | 108 | 6C | 154 |  |
| $m$ | 109 | 610 | 155 |  |
| $n$ | 110 | 6E | 156 |  |
| 0 | 111 | $6 F$ | 157 |  |
| $F$ | 112 | 70 | 160 |  |
| $a$ | 113 | 71 | 161 |  |
| $r$ | 114 | 72 | 162 |  |
| 5 | 115 | 73 | 163 |  |
| $t$ | 116 | 74 | 164 |  |
| $u$ | 117 | 75 | 165 |  |
| $v$ | 118 | 76 | 166 |  |
| $\omega$ | 119 | 77 | 167 |  |
| $x$ | 120 | 78 | 170 |  |
| צ | 121 | 79 | 171 |  |
| $z$ | 122 | 7 A | 172 |  |
| \{ | 123 | 7 B | 173 |  |
| : | 124 | 7 C | 174 |  |
| 3 | 125 | 7 B | 175 |  |
| $\sim$ | 126 | 7E | 176 |  |
| DEL. | 127 | 7F | 177 | Melete |

## APPENDIX B

## A 64K Memory Map

The 8080 and Z-80 microprocessors can directly address 64 K bytes of memory. The memory area is mapped out in the chart that follows. Each entry represents a 256 -byte block. The high-order byte of the address is given in hex then in octal. For example, the first entry of the second column is:
$20 \quad 040 \quad 32$
This represents an address range of 2000 to 2 FFF hex, or 040-000 to 040777 octal. The third column gives the decimal number of 1 K blocks. The fourth column is the decimal number of 256 -byte blocks starting at the address 100 hex. As an example, suppose that a CP/M program runs from 100 hex to 3035 hex. The 30 hex entry in the table shows that the program contains 48 decimal blocks of 256 -byte size. The program can be saved with the CP/M command:
A) SAVE 48 filename

As another example, if you have two, 16 K memory boards starting at address zero, then your top of memory is located at address 7FFF hex.

Hex Oct K Bl Hex Oct K Bl Hex Oct K Bl Hex Oct K Bl

| 000000 | 20 | 040 | 32 | 40 | 100 | 64 | 60 | 140 | 96 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 01001 | 21 | 041 | 33 | 41 | 101 | 65 |  | 141 | 97 |
| 02002 2 | 22 | 042 | 34 | 42 | 102 | 66 |  | 142 | 98 |
| 0300313 | 23 | 043 | 935 | 43 | 10317 | 67 | 63 | 14325 | 99 |
| 04004 | 24 | 044 | 36 | 44 | 104 | 68 | 64 | 144 | 100 |
| 050055 | 25 | 045 | 37 | 45 | 105 | 69 | 65 | 145 | 101 |
| 06006 | 26 | 046 | 38 | 46 | 106 | 70 | 66 | 146 | 102 |
| 0700727 | 27 | 047 | 1039 | 47 | 10718 | 71 | 67 | 14726 | 103 |
| 08010 | 28 | 050 | 40 | 48 | 110 | 72 | 68 | 150 | 104 |
| 09011 | 29 | 051 | 41 | 49 | 111 | 73 | 69 | 151 | 105 |
| OA 01210 | 2A | 052 | 42 | 4A | 112 | 74 | 6 6 | 152 | 106 |
| OF 013311 | 2 B | 053 | 1143 | 48 | 11319 | 75 | 68 | 15327 | 107 |
| OC 01412 | 2 C | 054 | 44 | 4 C | 114 | 76 | 6 C | 154 | 08 |
| OD 01513 | 20 | 055 | 45 | 4 D | 115 | 77 | 61 | 155 | 109 |
| OE 01614 | 2 E | 056 | 46 | 4 E | 116 | 78 | 6 E | 156 | 110 |
| OF 017415 | $2 F$ | 057 | 1247 | 45 | 11720 | 79 | 6 F | 15728 | 111 |
| $10020 \quad 16$ | 30 | 060 | 48 | 50 | 120 | 80 | 70 | 160 | 112 |
| $11021 \quad 17$ | 31 | 061 | 49 | 51 | 121 | 81 | 71 | 161 | 113 |
| 1202218 | 32 | 062 | 50 | 52 | 122 | 82 | 72 | 162 | 114 |
| 13023519 | 33 | 063 | 1351 | 53 | 12321 | 8.3 | 73 | 16329 | 115 |
| $14024 \quad 20$ | 34 | 064 | 52 | 54 | 124 | 84 | 74 |  | 116 |
| $15025 \quad 21$ | 35 | 065 | 53 | 55 | 125 | 85 | 75 | 165 | 117 |
| $16 \quad 026 \quad 22$ | 36 | 066 | 54 | 56 | 126 | 86 |  | 166 | 118 |
| 17027623 | 37 | 067 | 1455 | 57 | 12722 | 87 | 77 | 16730 | 119 |
| $18 \quad 030 \quad 24$ | 38 | 070 | 56 |  |  |  |  |  |  |
| $19031 \quad 25$ | 39 | 071 | 57 | 59 | 131 | $89$ |  |  |  |
| 1 A 032 l | 3 A | 072 | 58 | 5 A | 132 | 90 | 7 A | 172 | 122 |
| 18033727 | 3 B | 073 | 1559 | 5 E | 13323 | 91 | 7 B | 17331 | 123 |
| $\begin{array}{ll}\text { 10 } & =3 \\ 10 & =34\end{array}$ | 3C | 074 | 60 | 5 C | 134 | 92 |  |  | 124 |
| 1 l 035129 | 31 | 075 | 61 | 50 | 135 | 93 |  |  | 125 |
| $1 E 03630$ | 3E | 076 | 62 | 5 E | 136 | 94 |  |  | 126 |
| $1 F \begin{array}{llll}15 & 3 & 8 & 31\end{array}$ | 3 F | 077 | 1663 | 5 F | 13724 | 95 | 7 F | 17732 | 127 |

Hex Oct K Bl Hex Oct K B1 Hex Dct K Bl Hex Oct K Bl


## APPENDIX C The 8080 Instruction Set (Alphabetic)

The 8080 instruction set is listed alphabetically with the corresponding hexadecimal code. The following representations apply.
$\begin{array}{cc}\text { nn } & 8 \text {-bit argument } \\ \text { nnnn } & 16 \text {-bit argument }\end{array}$

| Hex |  | Mnemonic |  |
| :--- | :--- | :--- | :--- |
| CE | nn | ACI | nn |
| 8F |  | ADC | A |
| 88 |  | ADC | B |
| 89 |  | ADC | C |
| 8A |  | ADC | D |
| 8B |  | ADC | E |
| 8C |  | ADC | H |
| 8D |  | ADC | L |
| 8E |  | ADC | M |
| 87 |  | ADD | A |
| 80 |  | ADD | B |
| 81 |  | ADD | C |
| 82 |  | ADD | D |
| 83 |  | ADD | E |
| 84 |  | ADD | H |
| 85 |  | ADD | L |
| 86 |  | ADD | M |
| C6 | nn | ADI | nn |
| A7 |  | ANA | A |
| A0 |  | ANA | B |
| A1 |  | ANA | C |
| A2 |  | ANA | D |
| A3 |  | ANA | E |
| A4 |  | ANA | H |
| A5 |  | ANA | L |
| A6 |  | ANA | M |
| E6 | nn | ANI | nn |
| CD | nnnn | CALL | nnnn |
| DC | nnnn | CC | nnnn |
| FC | nnnn | CM | nnnn |


| Hex |  | Mnemonic |  |
| :---: | :---: | :---: | :---: |
| 2 F |  | CMA |  |
| 3 F |  | CMC |  |
| BF |  | CMP | A |
| B8 |  | CMP | B |
| B9 |  | CMP | C |
| BA |  | CMP | D |
| BB |  | CMP | E |
| BC |  | CMP | H |
| BD |  | CMP | L |
| BE |  | CMP | M |
| D4 | nnnn | CNC | nnnn |
| C4 | nnnn | CNZ | nnnn |
| F4 | nnnn | CP | nnnn |
| EC | nnnn | CPE | nnnn |
| FE | nn | CPI | nn |
| E4 | nnnn | CPO | nnnn |
| CC | nnnn | CZ | nnnn |
| 27 |  | DAA |  |
| 09 |  | DAD | B |
| 19 |  | DAD | D |
| 29 |  | DAD | H |
| 39 |  | DAD | SP |
| 3D |  | DCR | A |
| 05 |  | DCR | B |
| 0D |  | DCR | C |
| 15 |  | DCR | D |
| 1D |  | DCR | E |
| 25 |  | DCR | H |
| 2 D |  | DCR | L |
| 35 |  | DCR | M |


| Hex |  | Mnemonic |  |
| :---: | :---: | :---: | :---: |
| 0B |  | DCX | B |
| 1B |  | DCX | D |
| 2B |  | DCX | H |
| 3B |  | DCX | SP |
| F3 |  | DI |  |
| FB |  | EI |  |
| 76 |  | HLT |  |
| DB | nn | IN | nn |
| 3 C |  | INR | A |
| 04 |  | INR | B |
| 0C |  | INR | C |
| 14 |  | INR | D |
| 1 C |  | INR | E |
| 24 |  | INR | H |
| 2 C |  | INR | L |
| 34 |  | INR | M |
| 03 |  | INX | B |
| 13 |  | INX | D |
| 23 |  | INX | H |
| 33 |  | INX | SP |
| DA | nnnn | JC | nnnn |
| FA | nnnn | JM | nnnn |
| C3 | nnnn | JMP | nnnn |
| D2 | nnnn | JNC | nnnn |
| C2 | nnnn | JNZ | nnnn |
| F2 | nnnn | JP | nnnn |
| EA | nnnn | JPE | nnnn |
| E2 | nnnn | JPO | nnnn |
| CA | nnnn | JZ | nnnn |
| 3A | nnnn | LDA | nnnn |
| 0A |  | LDAX | B |
| 1A |  | LDAX | D |
| 2A | nnnn | LHLD | nnnn |
| 01 | nnnn | LXI | B, nnnn |
| 11 | nnnn | LXI | D, nnnn |
| 21 | nnnn | LXI | H, nnnn |
| 31 | nnnn | LXI | SP, nnnn |
| 7F |  | MOV | A,A |
| 78 |  | MOV | A,B |
| 79 |  | MOV | A,C |
| 7A |  | MOV | A,D |
| 7B |  | MOV | A,E |
| 7C |  | MOV | A, H |
| 7D |  | MOV | A,L |
| 7 E |  | MOV | A,M |
| 47 |  | MOV | B,A |
| 40 |  | MOV | B,B |
| 41 |  | MOV | B,C |
| 42 |  | MOV | B,D |


| Hex | Mnemonic |  |
| :---: | :---: | :---: |
| 43 | MOV | B,E |
| 44 | MOV | B,H |
| 45 | MOV | B,L |
| 46 | MOV | B,M |
| 4 F | MOV | C,A |
| 48 | MOV | C,B |
| 49 | MOV | C, C |
| 4 A | MOV | C,D |
| 4B | MOV | C,E |
| 4C | MOV | C,H |
| 4D | MOV | C,L |
| 4E | MOV | C,M |
| 57 | MOV | D,A |
| 50 | MOV | D,B |
| 51 | MOV | D,C |
| 52 | MOV | D,D |
| 53 | MOV | D,E |
| 54 | MOV | D, H |
| 55 | MOV | D,L |
| 56 | MOV | D,M |
| 5 F | MOV | E,A |
| 58 | MOV | E,B |
| 59 | MOV | E,C |
| 5A | MOV | E,D |
| 5B | MOV | E,E |
| 5C | MOV | E,H |
| 5D | MOV | E,L |
| 5 E | MOV | E,M |
| 67 | MOV | H,A |
| 60 | MOV | H,B |
| 61 | MOV | H,C |
| 62 | MOV | H,D |
| 63 | MOV | H,E |
| 64 | MOV | H, H |
| 65 | MOV | H,L |
| 66 | MOV | H,M |
| 6 F | MOV | L,A |
| 68 | MOV | L,B |
| 69 | MOV | L, C |
| 6A | MOV | L, D |
| 6B | MOV | L, E |
| 6C | MOV | L, H |
| 6D | MOV | L, L |
| 6 E | MOV | L,M |
| 77 | MOV | M,A |
| 70 | MOV | M,B |
| 71 | MOV | M,C |
| 72 | MOV | M,D |
| 73 | MOV | M,E |




## APPENDIX D

## The 8080 Instruction Set (Numeric)

The 8080 instruction set is listed alphabetically with the corresponding hexadecimal code. The following representations apply.

$$
\begin{array}{ll}
\mathrm{nn} & 8 \text {-bit argument } \\
\text { nnnn } & 16 \text {-bit argument }
\end{array}
$$

| Hex |  | Mnemonic | Hex |  | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00 |  | NOP | 1E | nn | MVI | E, nn |
| 01 | nnnn | LXI B, nnnn | 1 F |  | RAR |  |
| 02 |  | STAX B | 20 |  | (not | ed) |
| 03 |  | INX B | 21 | nnnn | LXI | H, nnnn |
| 04 |  | INR B | 22 | nnnn | SHLD | nnnn |
| 05 |  | DCR B | 23 |  | INX | H |
| 06 | nn | MVI B, nn | 24 |  | INR | H |
| 07 |  | RLC | 25 |  | DCR | H |
| 08 |  | (not used) | 26 | nn | MVI | $\mathrm{H}, \mathrm{nn}$ |
| 09 |  | DAD B | 27 |  | DAA |  |
| 0A |  | LDAX B | 28 |  | (not u | ed) |
| 0B |  | DCX B | 29 |  | DAD | H |
| 0 C |  | INR C | 2A | nnnn | LHLD | nnnn |
| 0D |  | DCR C | 2B |  | DCX | H |
| 0E | nn | MVI C, nn | 2C |  | INR | L |
| 0 F |  | RRC | 2D |  | DCR | L |
| 10 |  | (not used) | 2 E | nn | MVI | $\mathrm{L}, \mathrm{nn}$ |
| 11 | nnnn | LXI D, nnnn | 2 F |  | CMA |  |
| 12 |  | STAX D | 30 |  | ( not u | ed) |
| 13 |  | INX D | 31 | nnnn | LXI | $\mathrm{SP}, \mathrm{nnnn}$ |
| 14 |  | INR D | 32 | nnnn | STA | nnnn |
| 15 |  | DCR D | 33 |  | INX | SP |
| 16 | nn | MVI D, nn | 34 |  | INR | M |
| 17 |  | RAL | 35 |  | DCR | M |
| 18 |  | (not used) | 36 | nn | MVI | $\mathrm{M}, \mathrm{nn}$ |
| 19 |  | DAD D | 37 |  | STC |  |
| 1A |  | LDAX D | 38 |  | (not u | ed) |
| 1B |  | DCX D | 39 |  | DAD | SP |
| 1 C |  | INR E | 3A | nnnn | LDA | nnnn |
| 1D |  | DCR E | 3B |  | DCX | SP |


| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3 C | INR | A | 6D | MOV | L, L |
| 3D | DCR | A | 6E | MOV | L,M |
| 3 E nn | MVI | A, nn | 6 F | MOV | L,A |
| 3F | CMC |  | 70 | MOV | M,B |
| 40 | MOV | B,B | 71 | MOV | M, C |
| 41 | MOV | B, C | 72 | MOV | M,D |
| 42 | MOV | B,D | 73 | MOV | M, E |
| 43 | MOV | B,E | 74 | MOV | M, H |
| 44 | MOV | B, H | 75 | MOV | M, L |
| 45 | MOV | B,L | 76 | HLT |  |
| 46 | MOV | B,M | 77 | MOV | M,A |
| 47 | MOV | B,A | 78 | MOV | A, B |
| 48 | MOV | C,B | 79 | MOV | A, C |
| 49 | MOV | C, C | 7A | MOV | A,D |
| 4 A | MOV | C,D | 7B | MOV | A, E |
| 4B | MOV | C,E | 7C | MOV | A, H |
| 4 C | MOV | C, H | 7 D | MOV | A,L |
| 4D | MOV | C,L | 7E | MOV | A,M |
| 4 E | MOV | C,M | 7 F | MOV | A, A |
| 4F | MOV | C,A | 80 | ADD | B |
| 50 | MOV | D,B | 81 | ADD | C |
| 51 | MOV | D, C | 82 | ADD | D |
| 52 | MOV | D,D | 83 | ADD | E |
| 53 | MOV | D,E | 84 | ADD | H |
| 54 | MOV | D, H | 85 | ADD | L |
| 55 | MOV | D,L | 86 | ADD | M |
| 56 | MOV | D,M | 87 | ADD | A |
| 57 | MOV | D,A | 88 | ADC | B |
| 58 | MOV | E,B | 89 | ADC | C |
| 59 | MOV | E,C | 8A | ADC | D |
| 5A | MOV | E,D | 8B | ADC | E |
| 5B | MOV | E,E | 8C | ADC | H |
| 5 C | MOV | E,H | 8D | ADC | L |
| 5D | MOV | E,L | 8E | ADC | M |
| 5 E | MOV | E,M | 8F | ADC | A |
| 5 F | MOV | E,A | 90 | SUB | B |
| 60 | MOV | H,B | 91 | SUB | C |
| 61 | MOV | H,C | 92 | SUB | D |
| 62 | MOV | H,D | 93 | SUB | E |
| 63 | MOV | H, E | 94 | SUB | H |
| 64 | MOV | H, H | 95 | SUB | L |
| 65 | MOV | H,L | 96 | SUB | M |
| 66 | MOV | H, M | 97 | SUB | A |
| 67 | MOV | H,A | 98 | SBB | B |
| 68 | MOV | L, B | 99 | SBB | C |
| 69 | MOV | L, C | 9A | SBB | D |
| 6A | MOV | L, D | 9B | SBB | E |
| 6B | MOV | L, E | 9 C | SBB | H |
| 6C | MOV | L, H | 9D | SBB | L |


| Hex | Mnemonic | Hex | Mnemonic |
| :---: | :---: | :---: | :---: |
| 9E | SBB M | CF | RST 1 |
| 9 F | SBB A | D0 | RNC |
| A0 | ANA B | D1 | POP D |
| A1 | ANA C | D2 nnnn | JNC nnnn |
| A2 | ANA D | D3 nn | OUT nn |
| A3 | ANA E | D4 nnnn | CNC nnnn |
| A4 | ANA H | D5 | PUSH D |
| A5 | ANA L | D6 nn | SUI nn |
| A6 | ANA M | D7 | RST |
| A7 | ANA A | D8 | RC |
| A8 | XRA B | D9 | (not used) |
| A9 | XRA C | DA nnnn | JC nnnn |
| AA | XRA D | DB nn | IN nn |
| AB | XRA E | DC nnnn | CC nnnn |
| AC | XRA H | DD | (not used) |
| AD | XRA L | DE nn | SBI nn |
| AE | XRA M | DF | RST |
| AF | XRA A | E0 | RPO |
| B0 | ORA B | E1 | POP H |
| B1 | ORA C | E2 nnnn | JPO nnnn |
| B2 | ORA D | E3 | XTHL |
| B3 | ORA E | E4 nnnn | CPO nnnn |
| B4 | ORA H | E5 | PUSH H |
| B5 | ORA L | E6 nn | ANI $n$ n |
| B6 | ORA M | E7 | RST 4 |
| B7 | ORA A | E8 | RPE |
| B8 | CMP B | E9 | PCHL |
| B9 | CMP C | EA nnnn | JPE nnnn |
| BA | CMP D | EB | XCHG |
| BB | CMP E | EC nnnn | CPE nnnn |
| BC | CMP H | ED | (not used) |
| BD | CMP L | EE nn | XRI nn |
| BE | CMP M | EF | RST |
| BF | CMP A | F0 | RP |
| C0 | RNZ | F1 | POP PSW |
| C1 | POP B | F2 nnnn | JP nnnn |
| C2 nnnn | JNZ nnnn | F3 | DI |
| C3 nnnn | JMP nnnn | F4 nnnn | CP nnnn |
| C4 nnnn | CNZ nnnn | F5 | PUSH PSW |
| C5 | PUSH B | F6 nn | ORI nn |
| C6 nn | ADI nn | F7 | RST 6 |
| C7 | RST 0 | F8 | RM |
| C8 | RZ | F9 | SPHL |
| C9 | RET | FA nnnn | JM nnnn |
| CA nnnn | JZ nnnn | FB | EI |
| CB | (not used) | FC nnnn | CM nnnn |
| CC nnnn | CZ nnnn | FD | (not used) |
| CD nnnn | CALL nnnn | FE nn | CPI nn |
| CE nn | ACI nn | FF | RST 7 |

## APPENDIX E

## The Z-80 Instruction Set

## (Alphabetic)

The Zilog Z-80 instruction set is listed alphabetically with the corresponding hexadecimal values. The following representations apply.

| nn | 8 -bit arguments |
| :--- | :--- |
| nnnn | 16 -bit arguments |
| dd | 8 -bit signed displacement |
| $*$ | instructions common to the 8080 |


| Hex | Mnemonic |  |  | Hex |  | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 8E | * | ADC | A,(HL) | 19 | * | ADD | HL, DE |
| DD 8Edd |  | ADC | A,(IX+dd) | 29 | * | ADD | HL,HL |
| FD 8Edd |  | ADC | A,(IY+dd) | 39 | * | ADD | HL,SP |
| 8F | * | ADC | A, A | DD 09 |  | ADD | IX,BC |
| 88 | * | ADC | A,B | DD 19 |  | ADD | IX,DE |
| 89 | * | ADC | A, C | DD 29 |  | ADD | IX,IX |
| 8A | * | ADC | A,D | DD 39 |  | ADD | IX,SP |
| 8B | * | ADC | A, E | FD 09 |  | ADD | IY,BC |
| 8C | * | ADC | A, H | FD 19 |  | ADD | IY,DE |
| 8D | * | ADC | A,L | FD 29 |  | ADD | IY,IY |
| CE nn | * | ADC | A, nn | FD 39 |  | ADD | IY,SP |
| ED 4A |  | ADC | HL,BC | A6 | * | AND | (HL) |
| ED 5A |  | ADC | HL,DE | DD A6dd |  | AND | (IX+dd) |
| ED 6A |  | ADC | HL,HL | FD A6dd |  | AND | (IY+dd) |
| ED 7A |  | ADC | HL,SP | A7 | * | AND | A |
| 86 | * | ADD | A,(HL) | A0 | * | AND | B |
| DD 86dd |  | ADD | A,(IX+dd) | A1 | * | AND | C |
| FD 86dd |  | ADD | A,(IY+dd) | A2 | * | AND | D |
| 87 | * | ADD | A,A | A3 | * | AND | E |
| 80 | * | ADD | A,B | A4 | * | AND | H |
| 81 | * | ADD | A, C | A5 | * | AND | L |
| 82 | * | ADD | A, D | E6 nn | * | AND | nn |
| 83 | * | ADD | A, E | CB 46 |  | BIT | 0,(HL) |
| 84 | * | ADD | A, H | DD CBdd46 |  | BIT | 0,(IX+dd) |
| 85 | * | ADD | A,L | FD CBdd46 |  | BIT | 0, (IY+dd) |
| C6 nn | * | ADD | A, nn | CB 47 |  | BIT | 0,A |
| 09 | * | ADD | HL,BC | CB 40 |  | BIT | 0,B |



|  | Hex | Mnemonic |  |  | Hex |  | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A1 |  | CPI |  | 13 | * | INC | DE |
|  | B1 |  | CPIR |  | 1C | * | INC | E |
| 2 F |  | * | CPL |  | 24 | * | INC | H |
| 27 |  | * | DAA |  | 23 | * | INC | HL |
| 35 |  | * | DEC | (HL) | DD 23 |  | INC | IX |
|  | 35 dd |  | DEC | (IX+dd) | FD 23 |  | INC | IY |
| FD | 35 dd |  | DEC | (IY+dd) | 2 C | * | INC | L |
| 3D |  | * | DEC | A | 33 | * | INC | SP |
| 05 |  | * | DEC | B | ED AA |  | IND |  |
| 0B |  | * | DEC | BC | ED BA |  | INDR |  |
| 0D |  | * | DEC | C | ED A2 |  | INI |  |
| 15 |  | * | DEC | D | ED B2 |  | INIR |  |
| 1B |  | * | DEC | DE | E9 | * | JP | (HL) |
| 1D |  | * | DEC | E | DD E9 |  | JP | (IX) |
| 25 |  | * | DEC | H | FD E9 |  | JP | (IY) |
| 2B |  | * | DEC | HL | DA nnnn | * | JP | C, nnnn |
|  | 2B |  | DEC | IX | FA nnnn | * | JP | M, nnnn |
|  | 2B |  | DEC | IY | D2 nnnn | * | JP | NC, nnnn |
| 2D |  | * | DEC | L | C3 nnnn | * | JP | nnnn |
| 3B |  | * | DEC | SP | C2 nnnn | * | JP | NZ, nnnn |
| F3 |  | * | DI |  | F2 nnnn | * | JP | $\mathrm{P}, \mathrm{nnnn}$ |
|  | dd |  | DJNZ | dd | EA nnnn | * | JP | PE, nnnn |
| FB |  | * | EI |  | E2 nnnn | * | JP | PO, nnnn |
| E3 |  | * | EX | (SP),HL | CA nnnn | * | JP | Z, nnnn |
|  |  |  | EX | (SP),IX | 38 dd |  | JR | C, dd |
|  | E3 |  | EX | (SP), IY | 18 dd |  | JR | dd |
| 08 |  |  | EX | AF, $\mathrm{AF}^{\text {' }}$ | 30 dd |  | JR | NC, dd |
| EB |  | * | EX | DE,HL | 20 dd |  | JR | NZ, dd |
| D9 |  |  | EXX |  | 28 dd |  | JR | Z, dd |
| 76 |  | * | HALT |  | 02 | * | LD | (BC), A |
|  | 46 |  | IM | 0 | 12 | * | LD | (DE), A |
|  | 56 |  | IM | 1 | 77 | * | LD | (HL), A |
|  | 5E |  | IM | 2 | 70 | * | LD | (HL), B |
| ED | 78 |  | IN | A,(C) | 71 | * | LD | (HL), C |
|  | nn | * | IN | $\mathrm{A},(\mathrm{nn})$ | 72 | * | LD | (HL), D |
|  | 40 |  | IN | B,(C) | 73 | * | LD | (HL), E |
|  | 48 |  | IN | C,(C) | 74 | * | LD | (HL), H |
|  | 50 |  | IN | D,(C) | 75 | * | LD | (HL), L |
|  | 58 |  | IN | E,(C) | 36 nn | * | LD | (HL), nn |
| ED | 60 |  | IN | H,(C) | DD 77dd |  | LD | (IX+dd), A |
| ED | 68 |  | IN | L,(C) | DD 70dd |  | LD | (IX+dd), B |
| 34 |  | * | INC | (HL) | DD 71dd |  | LD | (IX+dd), C |
|  | 34dd |  | INC | (IX+dd) | DD 72dd |  | LD | (IX+dd), D |
| FD | 34dd |  | INC | (IY+dd) | DD 73dd |  | LD | (IX+dd), E |
| 3 C |  | * | INC | A | DD 74dd |  | LD | (IX+dd), H |
| 04 |  | * | INC | B | DD 75dd |  | LD | (IX+dd), L |
| 03 |  | * | INC | BC | DD 36ddnn |  | LD | (IX+dd), nn |
| 0 C |  | * | INC | C | FD 77dd |  | LD | (IY+dd), A |
| 14 |  | * | INC | D | FD 70dd |  | LD | (IY+dd),B |



| Hex | Mnemonic |  |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 6 F | * | LD | L,A | F5 | * PUSH | AF |
| 68 | * | LD | L,B | C5 | * PUSH | BC |
| 69 | * | LD | L, C | D5 | * PUSH | DE |
| 6A | * | LD | L, D | E5 | * PUSH | HL |
| 6B | * | LD | L, E | DD E5 | PUSH | IX |
| 6C | * | LD | L,H | FD E5 | PUSH | IY |
| 6D | * | LD | L, L | CB 86 | RES | 0,(HL) |
| 2 E nn | * | LD | L, nn | DD CBdd86 | RES | 0,(IX+dd) |
| ED 4F |  | LD | R,A | FD CBdd86 | RES | 0,(IY+dd) |
| ED 7Bnnnn |  | LD | SP, (nnnn) | CB 87 | RES | 0,A |
| F9 | * | LD | SP,HL | CB 80 | RES | 0,B |
| DD F9 |  | LD | SP,IX | CB 81 | RES | 0,C |
| FD F9 |  | LD | SP,IY | CB 82 | RES | 0,D |
| 31 nnnn | * | LD | SP, nnnn | CB 83 | RES | 0,E |
| ED A8 |  | LDD |  | CB 84 | RES | 0,H |
| ED B8 |  | LDDR |  | CB 85 | RES | 0,L |
| ED A0 |  | LDI |  | CB 8E | RES | 1,(HL) |
| ED B0 |  | LDIR |  | DD CBdd8E | RES | 1,(IX+dd) |
| ED 44 |  | NEG |  | FD CBdd8E | RES | 1,(IY+dd) |
| 00 | * | NOP |  | CB 8F | RES | 1,A |
| B6 | * | OR | (HL) | CB 88 | RES | 1,B |
| DD B6dd |  | OR | (IX + dd) | CB 89 | RES | 1,C |
| FD B6dd |  | OR | (IY + dd) | CB 8A | RES | 1,D |
| B7 | * | OR | A | CB 8B | RES | 1,E |
| B0 | * | OR | B | CB 8C | RES | 1,H |
| B1 | * | OR | C | CB 8D | RES | 1,L |
| B2 | * | OR | D | CB 96 | RES | 2,(HL) |
| B3 | * | OR | E | DD CBdd96 | RES | 2,(IX+dd) |
| B4 | * | OR | H | FD CBdd96 | RES | 2,(IY+dd) |
| B5 | * | OR | L | CB 97 | RES | 2,A |
| F6 nn | * | OR | nn | CB 90 | RES | 2,B |
| ED BB |  | OTDR |  | CB 91 | RES | 2,C |
| ED B3 |  | OTIR |  | CB 92 | RES | 2,D |
| ED 79 |  | OUT | (C), A | CB 93 | RES | 2,E |
| ED 41 |  | OUT | (C), B | CB 94 | RES | 2,H |
| ED 49 |  | OUT | (C), C | CB 95 | RES | 2,L |
| ED 51 |  | OUT | (C), D | CB 9E | RES | 3,(HL) |
| ED 59 |  | OUT | (C), E | DD CBdd9E | RES | 3,(IX+dd) |
| ED 61 |  | OUT | (C), H | FD CBdd9E | RES | 3,(IY+dd) |
| ED 69 |  | OUT | (C), L | CB 9F | RES | 3,A |
| D3 nn | * | OUT | (nn), A | CB 98 | RES | 3,B |
| ED AB |  | OUTD |  | CB 99 | RES | 3,C |
| ED A3 |  | OUTI |  | CB 9A | RES | 3,D |
| F1 | * | POP | AF | CB 9B | RES | 3,E |
| C1 | * | POP | BC | CB 9C | RES | 3,H |
| D1 | * | POP | DE | CB 9D | RES | 3,L |
| E1 | * | POP | HL | CB A6 | RES | 4,(HL) |
| DD E1 |  | POP | IX | DD CBddA6 | RES | 4,(IX+dd) |
| FD E1 |  | POP | IY | FD CBddA6 | RES | 4,(IY+dd) |


| Hex | Mnemonic |  |  | Hex | Mnemonic |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CB A7 |  | RES | 4,A | DD CBdd16 |  | RL | (IX + dd) |
| CB A0 |  | RES | 4,B | FD CBdd16 |  | RL | (IY + dd) |
| CB A1 |  | RES | 4,C | CB 17 |  | RL | A |
| CB A2 |  | RES | 4,D | CB 10 |  | RL | B |
| CB A3 |  | RES | 4,E | CB 11 |  | RL | C |
| CB A4 |  | RES | 4, H | CB 12 |  | RL | D |
| CB A5 |  | RES | 4,L | CB 13 |  | RL | E |
| CB AE |  | RES | 5,(HL) | CB 14 |  | RL | H |
| DD CBddAE |  | RES | 5,(IX+dd) | CB 15 |  | RL | L |
| FD CBddAE |  | RES | 5,(IY+dd) | 17 | * | RLA |  |
| CB AF |  | RES | 5,A | CB 06 |  | RLC | (HL) |
| CB A8 |  | RES | 5,B | DD CBdd06 |  | RLC | (IX +dd ) |
| CB A9 |  | RES | 5,C | FD CBdd06 |  | RLC | (IY+dd) |
| CB AA |  | RES | 5,D | CB 07 |  | RLC | A |
| CB AB |  | RES | 5,E | CB 00 |  | RLC | B |
| CB AC |  | RES | 5, H | CB 01 |  | RLC | C |
| CB AD |  | RES | 5, L | CB 02 |  | RLC | D |
| CB B6 |  | RES | 6,(HL) | CB 03 |  | RLC | E |
| DD CBddB6 |  | RES | 6,(IX + dd) | CB 04 |  | RLC | H |
| FD CBddB6 |  | RES | 6,(IY+dd) | CB 05 |  | RLC | L |
| CB B7 |  | RES | 6,A | 07 | * | RLCA |  |
| CB B0 |  | RES | 6,B | ED 6F |  | RLD |  |
| CB B1 |  | RES | 6,C | CB 1E |  | RR | (HL) |
| CB B2 |  | RES | 6,D | DD CBdd1E |  | RR | (IX+dd) |
| CB B3 |  | RES | 6,E | FD CBdd1E |  | RR | (IY+dd) |
| CB B4 |  | RES | 6, H | CB 1F |  | RR | A |
| CB B5 |  | RES | 6,L | CB 18 |  | RR | B |
| CB BE |  | RES | 7,(HL) | CB 19 |  | RR | C |
| DD CBddBE |  | RES | 7,(IX+dd) | CB 1A |  | RR | D |
| FD CBddBE |  | RES | 7,(IY+dd) | CB 1B |  | RR | E |
| CB BF |  | RES | 7,A | CB 1C |  | RR | H |
| CB B8 |  | RES | 7,B | CB 1D |  | RR | L |
| CB B9 |  | RES | 7,C | 1F | * | RRA |  |
| CB BA |  | RES | 7,D | CB 0E |  | RRC | (HL) |
| CB BB |  | RES | 7,E | DD CBdd0E |  | RRC | (IX + dd) |
| CB BC |  | RES | 7,H | FD CBdd0E |  | RRC | (IY+dd) |
| CB BD |  | RES | 7,L | CB 0F |  | RRC | A |
| C9 | * | RET |  | CB 08 |  | RRC | B |
| D8 | * | RET | C | CB 09 |  | RRC | C |
| F8 | * | RET | M | CB 0A |  | RRC | D |
| D0 | * | RET | NC | CB OB |  | RRC | E |
| C0 | * | RET | NZ | CB 0C |  | RRC | H |
| F0 | * | RET | P | CB 0D |  | RRC | L |
| E8 | * | RET | PE | OF | * | RRCA |  |
| E0 | * | RET | PO | ED 67 |  | RRD |  |
| C8 | * | RET | Z | C7 | * | RST | 0 |
| ED 4D |  | RETI |  | CF | * | RST | 8 |
| ED 45 |  | RETN |  | D7 | * | RST | 10 H |
| CB 16 |  | RL | (HL) | DF | * | RST | 18H |


| Hex | Mnemonic |  |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| E7 | * | RST | 20 H | CB D5 | SET | 2,L |
| EF | * | RST | 28H | CB DE | SET | 3,(HL) |
| F7 | * | RST | 30 H | DD CBddDE | SET | 3,(IX + dd) |
| FF | * | RST | 38 H | FD CBddDE | SET | 3,(IY+dd) |
| 9E | * | SBC | A,(HL) | CB DF | SET | 3,A |
| DD 9Edd |  | SBC | A,(IX + dd) | CB D8 | SET | 3, B |
| FD 9Edd |  | SBC | A,(IY + dd) | CB D9 | SET | 3,C |
| 9 F | * | SBC | A,A | CB DA | SET | 3,D |
| 98 | * | SBC | A,B | CB DB | SET | 3,E |
| 99 | * | SBC | A,C | CB DC | SET | 3,H |
| 9A | * | SBC | A,D | CB DD | SET | 3,L |
| 9B | * | SBC | A,E | CB E6 | SET | 4,(HL) |
| 9 C | * | SBC | A, H | DD CBddE6 | SET | 4,(IX + dd) |
| 9D | * | SBC | A,L | FD CBddE6 | SET | 4,(IY+dd) |
| DE nn | * | SBC | A, nn | CB E7 | SET | 4,A |
| ED 42 |  | SBC | HL, BC | CB E0 | SET | 4,B |
| ED 52 |  | SBC | HL, DE | CB E1 | SET | 4,C |
| ED 62 |  | SBC | HL, HL | CB E2 | SET | 4,D |
| ED 72 |  | SBC | HL,SP | CB E3 | SET | 4,E |
| 37 | * | SCF |  | CB E4 | SET | 4, H |
| CB C6 |  | SET | 0,(HL) | CB E5 | SET | 4,L |
| DD CBddC6 |  | SET | 0,(IX+dd) | CB EE | SET | 5,(HL) |
| FD CBddC6 |  | SET | $0,(\mathrm{IY}+\mathrm{dd})$ | DD CBddEE | SET | $5,(\mathrm{IX}+\mathrm{dd})$ |
| CB C7 |  | SET | 0,A | FD CBddEE | SET | $5,(\mathrm{IY}+\mathrm{dd}$ ) |
| CB C0 |  | SET | 0,B | CB EF | SET | 5,A |
| CB C1 |  | SET | 0,C | CB E8 | SET | 5,B |
| CB C2 |  | SET | 0,D | CB E9 | SET | 5,C |
| CB C3 |  | SET | 0,E | CB EA | SET | 5,D |
| CB C4 |  | SET | 0, H | CB EB | SET | 5,E |
| CB C5 |  | SET | 0,L | CB EC | SET | 5,H |
| CB CE |  | SET | 1,(HL) | CB ED | SET | 5,L |
| DD CBddCE |  | SET | 1,(IX+dd) | CB F6 | SET | 6,(HL) |
| FD CBddCE |  | SET | 1,(IY+dd) | DD CBddF6 | SET | 6,(IX+dd) |
| CB CF |  | SET | 1,A | FD CBddF6 | SET | 6,(IY + dd) |
| CB C8 |  | SET | 1,B | CB F7 | SET | 6,A |
| CB C9 |  | SET | 1,C | CB F0 | SET | 6,B |
| CB CA |  | SET | 1,D | CB F1 | SET | 6,C |
| CB CB |  | SET | 1,E | CB F2 | SET | 6,D |
| CB CC |  | SET | 1,H | CB F3 | SET | 6,E |
| CB CD |  | SET | 1,L | CB F4 | SET | 6,H |
| CB D6 |  | SET | 2,(HL) | CB F5 | SET | 6,L |
| DD CBddD6 |  | SET | 2,(IX+dd) | CB FE | SET | 7,(HL) |
| FD CBddD6 |  | SET | 2,(IY+dd) | DD CBddFE | SET | 7,(IX + dd) |
| CB D7 |  | SET | 2,A | FD CBddFE | SET | 7,(IY+dd) |
| CB D0 |  | SET | 2,B | CB FF | SET | 7,A |
| CB D1 |  | SET | 2,C | CB F8 | SET | 7,B |
| CB D2 |  | SET | 2,D | CB F9 | SET | 7,C |
| CB D3 |  | SET | 2,E | CB FA | SET | 7,D |
| CB D4 |  | SET | 2,H | CB FB | SET | 7,E |



## APPENDIX F

## The Z-80 Instruction Set (Numeric)

The Zilog Z-80 instruction set is listed numerically with the corresponding hexadecimal values. The following representations apply.

| nn | 8 -bit argument |
| :--- | :--- |
| nnnn | 16 -bit argument |
| dd | 8 -bit signed displacement |
| * | instructions common to the 8080 |


|  | Hex | Mnemonic |  |  | Hex |  |  | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00 |  | * | NOP |  | 1 C |  |  | INC | E |
| 01 | nnnn | * | LD | BC, nnnn | 1D |  | * | DEC | E |
| 02 |  | * | LD | (BC), A | 1 E | nn |  |  | E, nn |
| 03 |  | * | INC | BC | 1 F |  |  | RRA |  |
| 04 |  | * | INC | B |  | dd |  | JR | NZ, dd |
| 05 |  | * | DEC | B | 21 | nnnn |  | LD | HL, nnnn |
| 06 | nn | * | LD | B, nn | 22 | nnnn | * | LD | (nnnn),HL |
| 07 |  |  | RLCA |  | 23 |  |  | INC | HL |
| 08 |  |  | EX | AF, AF ${ }^{\prime}$ | 24 |  | * | INC | H |
| 09 |  |  | ADD | HL,BC | 25 |  | * | DEC | H |
| 0A |  |  | LD | A, (BC) | 26 | nn | * |  | H, nn |
| 0B |  |  | DEC | BC | 27 |  | * | DAA |  |
| 0 C |  |  | INC | C |  | dd |  | JR | Z, dd |
| 0D |  |  | DEC | C | 29 |  |  | ADD | HL,HL |
| 0E | n |  | LD | C, nn | 2A | nnnn | * | LD | HL, (nnnn) |
| 0 F |  |  | RRCA |  | 2B |  | * | DEC | HL |
| 10 | dd |  | DJNZ | dd | 2C |  |  | INC | L |
| 11 | nnnn |  | LD | DE, nnnn | 2D |  | * | DEC | L |
| 12 |  |  | LD | (DE), A | 2E | nn | * |  | L, nn |
| 13 |  |  |  | DE | 2 F |  | * | CPL |  |
| 14 |  |  |  | D | 30 | dd |  | JR | NC, dd |
| 15 |  |  | DEC | D |  | nnnn | * | LD | SP, nnnn |
| 16 | nn |  | LD | D, nn | 32 | nnnn | * | LD | (nnnn), A |
| 17 |  |  | RLA |  | 33 |  |  | INC | SP |
|  | dd |  | JR | dd | 34 |  | * | INC | (HL) |
| 19 |  |  | ADD | HL,DE | 35 |  | * | DEC | (HL) |
| 1A |  |  | LD | A,(DE) | 36 |  | * |  | (HL), nn |
| 1B |  |  | DEC | DE | 37 |  | * | SCF |  |


| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 38 dd | JR | C, dd | 69 | * LD | L,C |
| 39 | * ADD | HL,SP | 6A | * LD | L, D |
| 3 A nnnn | * LD | A, (nnnn) | 6B | * LD | L, E |
| 3B | * DEC | SP | 6C | * LD | L, H |
| 3 C | INC | A | 6 D | * LD | L,L |
| 3D | * DEC | A | 6 E | * LD | L,(HL) |
| 3 E nn | * LD | A, nn | 6 F | * LD | L,A |
| 3 F | * CCF |  | 70 | * LD | (HL), B |
| 40 | * LD | B,B | 71 | * LD | (HL), C |
| 41 | * LD | B,C | 72 | * LD | (HL), D |
| 42 | * LD | B,D | 73 | * LD | (HL), E |
| 43 | * LD | B,E | 74 | * LD | (HL), H |
| 44 | * LD | B,H | 75 | * LD | (HL), L |
| 45 | * LD | B,L | 76 | * HALT |  |
| 46 | * LD | B,(HL) | 77 | * LD | (HL), A |
| 47 | * LD | B,A | 78 | * LD | A,B |
| 48 | * LD | C,B | 79 | * LD | A, C |
| 49 | * LD | C,C | 7 A | * LD | A,D |
| 4A | * LD | C,D | 7B | * LD | A, E |
| 4B | * LD | C,E | 7 C | * LD | A, H |
| 4 C | * LD | C,H | 7 D | * LD | A,L |
| 4D | * LD | C,L | 7 E | * LD | A,(HL) |
| 4 E | * LD | C,(HL) | 7 F | * LD | A,A |
| 4 F | * LD | C,A | 80 | * ADD | A, B |
| 50 | * LD | D,B | 81 | * ADD | A, C |
| 51 | * LD | D, C | 82 | * ADD | A,D |
| 52 | * LD | D,D | 83 | * ADD | A,E |
| 53 | * LD | D, E | 84 | * ADD | A, H |
| 54 | * LD | D,H | 85 | * ADD | A,L |
| 55 | * LD | D,L | 86 | * ADD | A,(HL) |
| 56 | * LD | D,(HL) | 87 | * ADD | A,A |
| 57 58 | * LD | D,A | 88 | * ADC | A,B |
| 58 | * LD | E,B | 89 | * ADC | A, C |
| 59 | * LD | E,C | 8A | * ADC | A,D |
| 5 A | * LD | E,D | 8B | * ADC | A,E |
| 5B | * LD | E,E | 8 C | * ADC | A, H |
| 5 C | * LD | E,H | 8D | * ADC | A,L |
| 5D | * LD | E,L | 8E | * ADC | $\mathrm{A},(\mathrm{HL})$ |
| 5 E | * LD | E,(HL) | 8 F | * ADC | A,A |
| 5 F | * LD | E,A | 90 | * SUB | B |
| 60 | * LD | H,B | 91 | * SUB | C |
| 61 | * LD | H, C | 92 | * SUB | D |
| 62 | * LD | H,D | 93 | * SUB | E |
| 63 | * LD | H,E | 94 | * SUB | H |
| 64 | * LD | H, H | 95 | * SUB | L |
| 65 | * LD | H,L | 96 | * SUB | (HL) |
| 66 | * LD | H,(HL) | 97 | * SUB | A |
| 67 | * LD | H,A | 98 | * SBC | A,B |
| 68 | * LD | L,B | 99 | * SBC | A, C |



| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CB 39 | SRL | C | CB 6A | BIT | 5,D |
| CB 3A | SRL | D | CB 6B | BIT | 5,E |
| CB 3B | SRL | E | CB 6C | BIT | 5,H |
| CB 3C | SRL | H | CB 6D | BIT | 5,L |
| CB 3D | SRL | L | CB 6E | BIT | 5,(HL) |
| CB 3E | SRL | (HL) | CB 6F | BIT | 5,A |
| CB 3F | SRL | A | CB 70 | BIT | 6,B |
| CB 40 | BIT | 0,B | CB 71 | BIT | 6,C |
| CB 41 | BIT | 0,C | CB 72 | BIT | 6,D |
| CB 42 | BIT | 0,D | CB 73 | BIT | 6,E |
| CB 43 | BIT | 0,E | CB 74 | BIT | 6,H |
| CB 44 | BIT | 0,H | CB 75 | BIT | 6,L |
| CB 45 | BIT | 0L | CB 76 | BIT | 6,(HL) |
| CB 46 | BIT | 0,(HL) | CB 77 | BIT | 6,A |
| CB 47 | BIT | 0,A | CB 78 | BIT | 7,B |
| CB 48 | BIT | 1,B | CB 79 | BIT | 7,C |
| CB 49 | BIT | 1,C | CB 7A | BIT | 7,D |
| CB 4A | BIT | 1,D | CB 7B | BIT | 7,E |
| CB 4B | BIT | 1,E | CB 7C | BIT | 7,H |
| CB 4C | BIT | 1,H | CB 7D | BIT | 7,L |
| CB 4D | BIT | 1,L | CB 7E | BIT | 7,(HL) |
| CB 4E | BIT | 1,(HL) | CB 7F | BIT | 7,A |
| CB 4F | BIT | 1,A | CB 80 | RES | 0,B |
| CB 50 | BIT | 2,B | CB 81 | RES | 0, C |
| CB 51 | BIT | 2,C | CB 82 | RES | 0,D |
| CB 52 | BIT | 2,D | CB 83 | RES | 0,E |
| CB 53 | BIT | 2,E | CB 84 | RES | 0,H |
| CB 54 | BIT | 2,H | CB 85 | RES | 0,L |
| CB 55 | BIT | 2,L | CB 86 | RES | 0,(HL) |
| CB 56 | BIT | 2,(HL) | CB 87 | RES | 0,A |
| CB 57 | BIT | 2,A | CB 88 | RES | 1,B |
| CB 58 | BIT | 3,B | CB 89 | RES | 1,C |
| CB 59 | BIT | 3,C | CB 8A | RES | 1,D |
| CB 5A | BIT | 3,D | CB 8B | RES | 1,E |
| CB 5B | BIT | 3,E | CB 8C | RES | 1,H |
| CB 5C | BIT | 3,H | CB 8D | RES | 1,L |
| CB 5D | BIT | 3,L | CB 8E | RES | 1,(HL) |
| CB 5E | BIT | 3,(HL) | CB 8 F | RES | 1,A |
| CB 5F | BIT | 3,A | CB 90 | RES | 2,B |
| CB 60 | BIT | 4,B | CB 91 | RES | 2,C |
| CB 61 | BIT | 4,C | CB 92 | RES | 2,D |
| CB 62 | BIT | 4,D | CB 93 | RES | 2,E |
| CB 63 | BIT | 4,E | CB 94 | RES | 2,H |
| CB 64 | BIT | 4,H | CB 95 | RES | 2,L |
| CB 65 | BIT | 4,L | CB 96 | RES | 2,(HL) |
| CB 66 | BIT | 4,(HL) | CB 97 | RES | 2,A |
| CB 67 | BIT | 4,A | CB 98 | RES | 3,B |
| CB 68 | BIT | 5,B | CB 99 | RES | 3,C |
| CB 69 | BIT | 5,C | CB 9A | RES | 3,D |


| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CB 9B | RES | 3,E | CB CC | SET | 1,H |
| CB 9C | RES | 3,H | CB CD | SET | 1,L |
| CB 9D | RES | 3,L | CB CE | SET | 1,(HL) |
| CB 9E | RES | 3,(HL) | CB CF | SET | 1,A |
| CB 9F | RES | 3,A | CB D0 | SET | 2,B |
| CB A0 | RES | 4,B | CB D1 | SET | 2,C |
| CB A1 | RES | 4,C | CB D2 | SET | 2,D |
| CB A2 | RES | 4,D | CB D3 | SET | 2,E |
| CB A3 | RES | 4,E | CB D4 | SET | 2,H |
| CB A4 | RES | 4,H | CB D5 | SET | 2,L |
| CB A5 | RES | 4,L | CB D6 | SET | 2,(HL) |
| CB A6 | RES | 4,(HL) | CB D7 | SET | 2,A |
| CB A7 | RES | 4,A | CB D8 | SET | 3,B |
| CB A8 | RES | 5,B | CB D9 | SET | 3,C |
| CB A9 | RES | 5,C | CB DA | SET | 3,D |
| CB AA | RES | 5,D | CB DB | SET | 3,E |
| CB AB | RES | 5,E | CB DC | SET | 3,H |
| CB AC | RES | 5,H | CB DD | SET | 3,L |
| CB AD | RES | 5,L | CB DE | SET | 3,(HL) |
| CB AE | RES | 5,(HL) | CB DF | SET | 3,A |
| CB AF | RES | 5,A | CB E0 | SET | 4,B |
| CB B0 | RES | 6,B | CB E1 | SET | 4,C |
| CB B1 | RES | 6,C | CB E2 | SET | 4,D |
| CB B2 | RES | 6,D | CB E3 | SET | 4,E |
| CB B3 | RES | 6,E | CB E4 | SET | 4,H |
| CB B4 | RES | 6,H | CB E5 | SET | 4,L |
| CB B5 | RES | 6,L | CB E6 | SET | 4,(HL) |
| CB B6 | RES | 6,(HL) | CB E7 | SET | 4,A |
| CB B7 | RES | 6,A | CB E8 | SET | 5,B |
| CB B8 | RES | 7,B | CB E9 | SET | 5,C |
| CB B9 | RES | 7,C | CB EA | SET | 5,D |
| CB BA | RES | 7,D | CB EB | SET | 5,E |
| CB BB | RES | 7,E | CB EC | SET | 5,H |
| CB BC | RES | 7,H | CB ED | SET | 5,L |
| CB BD | RES | 7,L | CB EE | SET | 5,(HL) |
| CB BE | RES | 7,(HL) | CB EF | SET | 5,A |
| CB BF | RES | 7,A | CB F0 | SET | 6,B |
| CB C0 | SET | 0,B | CB F1 | SET | 6,C |
| CB C1 | SET | 0,C | CB F2 | SET | 6,D |
| CB C2 | SET | 0,D | CB F3 | SET | 6,E |
| CB C3 | SET | 0,E | CB F4 | SET | 6,H |
| CB C4 | SET | 0,H | CB F5 | SET | 6,L |
| CB C5 | SET | 0,L | CB F6 | SET | 6,(HL) |
| CB C6 | SET | 0,(HL) | CB F7 | SET | 6,A |
| CB C7 | SET | 0,A | CB F8 | SET | 7,B |
| CB C8 | SET | 1,B | CB F9 | SET | 7,C |
| CB C9 | SET | 1,C | CB FA | SET | 7,D |
| CB CA | SET | 1,D | CB FB | SET | 7,E |
| CB CB | SET | 1,E | CB FC | SET | 7,H |


| Hex | Mnemonic |  |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CB FD |  | SET | 7,L | DD 9Edd | SBC | A,(IX+dd) |
| CB FE |  | SET | 7,(HL) | DD A6dd | AND | (IX+dd) |
| CB FF |  | SET | 7,A | DD AEdd | XOR | (IX + dd) |
| CC nnnn | * | CALL | Z, nnnn | DD B6dd | OR | (IX + dd) |
| CD nnnn | * | CALL | nnnn | DD BEdd | CP | (IX+dd) |
| CE nn | * | ADC | A, nn | DD CBdd06 | RLC | (IX + dd) |
| CF | * | RST | 8 | DD CBdd0E | RRC | (IX + dd) |
| D0 | * | RET | NC | DD CBdd16 | RL | (IX + dd) |
| D1 | * | POP | DE | DD CBdd1E | RR | (IX + dd) |
| D2 nnnn | * | JP | NC, nnnn | DD CBdd26 | SLA | (IX + dd) |
| D3 nn | * | OUT | (nn), A | DD CBdd2E | SRA | (IX + dd) |
| D4 nnnn | * | CALL | NC, nnnn | DD CBdd3E | SRL | (IX + dd) |
| D5 | * | PUSH | DE | DD CBdd46 | BIT | $0,(\mathrm{IX}+\mathrm{dd})$ |
| D6 nn | * | SUB | nn | DD CBdd4E | BIT | 1,(IX+dd) |
| D7 | * | RST | 10 H | DD CBdd56 | BIT | 2,(IX+dd) |
| D8 | * | RET | C | DD CBdd5E | BIT | 3,(IX+dd) |
| D9 |  | EXX |  | DD CBdd66 | BIT | 4,(IX+dd) |
| DA nnnn | * | JP | C, nnnn | DD CBdd6E | BIT | 5,(IX+dd) |
| DB nn | * | IN | A, (nn) | DD CBdd76 | BIT | 6,(IX + dd) |
| DC nnnn | * | CALL | C, nnnn | DD CBdd7E | BIT | 7,(IX+dd) |
| DD 09 |  | ADD | IX,BC | DD CBdd86 | RES | 0,(IX + dd) |
| DD 19 |  | ADD | IX,DE | DD CBdd8E | RES | 1,(IX+dd) |
| DD 21 nnnn |  | LD | IX, nnnn | DD CBdd96 | RES | 2,(IX+dd) |
| DD 22 nnnn |  | LD | (nnnn), IX | DD CBdd9E | RES | 3,(IX+dd) |
| DD 23 |  | INC | IX | DD CBddA6 | RES | 4,(IX+dd) |
| DD 29 |  | ADD | IX,IX | DD CBddAE | RES | 5,(IX+dd) |
| DD 2Annnn |  | LD | IX, (nnnn) | DD CBddB6 | RES | 6,(IX+dd) |
| DD 2B |  | DEC | IX | DD CBddBE | RES | 7,(IX+dd) |
| DD 34dd |  | INC | (IX + dd) | DD CBddC6 | SET | 0,(IX+dd) |
| DD 35dd |  | DEC | (IX+dd) | DD CBddCE | SET | 1,(IX+dd) |
| DD 36ddnn |  | LD | (IX +dd ), nn | DD CBddD6 | SET | 2,(IX+dd) |
| DD 39 |  | ADD | IX,SP | DD CBddDE | SET | 3,(IX+dd) |
| DD 46dd |  | LD | B,(IX+dd) | DD CBddE6 | SET | 4,(IX+dd) |
| DD 4Edd |  | LD | C,(IX+dd) | DD CBddEE | SET | 5,(IX+dd) |
| DD 56dd |  | LD | D,(IX + dd) | DD CBddF6 | SET | 6,(IX+dd) |
| DD 5Edd |  | LD | E, (IX + dd) | DD CBddFE | SET | 7,(IX+dd) |
| DD 66dd |  | LD | H,(IX + dd) | DD E1 | POP | IX |
| DD 6Edd |  | LD | L, (IX + dd) | DD E3 | EX | (SP),IX |
| DD 70dd |  | LD | (IX+dd), B | DD E5 | PUSH | IX |
| DD 71dd |  | LD | (IX+dd), C | DD E9 | JP | (IX) |
| DD 72dd |  | LD | (IX+dd), D | DD F9 | LD | SP,IX |
| DD 73dd |  | LD | (IX+dd), E | DE nn | * SBC | A, nn |
| DD 74dd |  | LD | (IX + dd), H | DF | * RST | 18 H |
| DD 75dd |  | LD | (IX+dd), L | E0 | * RET | PO |
| DD 77dd |  | LD | (IX+dd), A | E1 | * POP | HL |
| DD 7Edd |  | LD | A,(IX + dd) | E2 nnnn | * JP | PO, nnnn |
| DD 86dd |  | ADD | A, (IX + dd) | E3 | * EX | (SP), HL |
| DD 8Edd |  | ADC | A, (IX + dd) | E4 nnnn | * CALL | PO, nnnn |
| DD 96dd |  | SUB | (IX + dd) | E5 | * PUSH | HL |


| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| E6 nn | * AND | nn | ED A2 | INI |  |
| E7 | * RST | 20 H | ED A3 | OUTI |  |
| E8 | RET | PE | ED A8 | LDD |  |
| E9 | * JP | (HL) | ED A9 | CPD |  |
| EA nnnn | * JP | PE, nnnn | ED AA | IND |  |
| EB | EX | DE,HL | ED AB | OUTD |  |
| EC nnnn | CALL | PE, nnnn | ED B0 | LDIR |  |
| ED 40 | IN | B,(C) | ED B1 | CPIR |  |
| ED 41 | OUT | (C), B | ED B2 | INIR |  |
| ED 42 | SBC | HL, BC | ED B3 | OTIR |  |
| ED 43nnnn | LD | (nnnn), BC | ED B8 | LDDR |  |
| ED 44 | NEG |  | ED B9 | CPDR |  |
| ED 45 | RETN |  | ED BA | INDR |  |
| ED 46 | IM | 0 | ED BB | OTDR |  |
| ED 47 | LD | I,A | EE nn | * XOR | N |
| ED 48 | IN | C,(C) | EF | * RST | 28 H |
| ED 49 | OUT | (C), C | F0 | * RET | P |
| ED 4A | ADC | HL, BC | F1 | * POP | AF |
| ED 4Bnnnn | LD | BC, (nnnn) | F2 nnnn | * JP | $\mathrm{P}, \mathrm{nnnn}$ |
| ED 4D | RETI |  | F3 | * DI |  |
| ED 4F | LD | R,A | F4 nnnn | * CALL | P, nnnn |
| ED 50 | IN | D,(C) | F5 | * PUSH | AF |
| ED 51 | OUT | (C), D | F6 nn | * OR | nn |
| ED 52 | SBC | HL, DE | F7 | * RST | 30 H |
| ED 53 nnnn | LD | (nnnn), DE | F8 | * RET | M |
| ED 56 | IM | 1 | F9 | * LD | SP,HL |
| ED 57 | LD | A,I | FA nnnn | * JP | $\mathrm{M}, \mathrm{nnnn}$ |
| ED 58 | IN | E,(C) | FB | * EI |  |
| ED 59 | OUT | (C), E | FC nnnn | * CALL | M, nnnn |
| ED 5A | ADC | HL, DE | FD 09 | ADD | IY, BC |
| ED 5Bnnnn | LD | DE, (nnnn) | FD 19 | ADD | IY,DE |
| ED 5E | IM | 2 | FD 21nnnn | LD | IY, nnnn |
| ED 5F | LD | A,R | FD 22 nnnn | LD | (nnnn),IY |
| ED 60 | IN | H,(C) | FD 23 | INC | IY |
| ED 61 | OUT | (C), H | FD 29 | ADD | IY,IY |
| ED 62 | SBC | HL,HL | FD 2 Annnn | LD | IY, (nnnn) |
| ED 67 | RRD |  | FD 2B | DEC | IY |
| ED 68 | IN | L,(C) | FD 34dd | INC | (IY+dd) |
| ED 69 | OUT | (C), L | FD 35dd | DEC | (IY+dd) |
| ED 6A | ADC | HL,HL | FD 36ddnn | LD | (IY +dd ), nn |
| ED 6F | RLD |  | FD 39 | ADD | IY,SP |
| ED 72 | SBC | HL,SP | FD 46dd | LD | B,(IY+dd) |
| ED 73nnnn | LD | (nnnn), SP | FD 4Edd | LD | C,(IY+dd) |
| ED 78 | IN | A,(C) | FD 56dd | LD | D,(IY+dd) |
| ED 79 | OUT | (C), A | FD 5Edd | LD | E,(IY+dd) |
| ED 7A | ADC | HL, SP | FD 66dd | LD | H,(IY+dd) |
| ED 7Bnnnn | LD | SP, (nnnn) | FD 6Edd | LD | L,(IY+dd) |
| ED A0 | LDI |  | FD 70dd | LD | (IY+dd), B |
| ED A1 | CPI |  | FD 71dd | LD | (IY+dd), C |


| Hex | Mnemonic |  | Hex | Mnemonic |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| FD 72dd | LD | (IY+dd), D | FD CBdd6E | BIT | 5,(IY+dd) |
| FD 73dd | LD | (IY+dd), E | FD CBdd76 | BIT | 6,(IY+dd) |
| FD 74dd | LD | (IY+dd), H | FD CBdd7E | BIT | 7,(IY+dd) |
| FD 75dd | LD | (IY + dd), L | FD CBdd86 | RES | 0,(IY+dd) |
| FD 77dd | LD | (IY+dd), A | FD CBdd8E | RES | 1,(IY+dd) |
| FD 7Edd | LD | A,(IY+dd) | FD CBdd96 | RES | 2,(IY+dd) |
| FD 86dd | ADD | A,(IY+dd) | FD CBdd9E | RES | 3,(IY+dd) |
| FD 8Edd | ADC | A,(IY+dd) | FD CBddA6 | RES | 4,(IY+dd) |
| FD 96dd | SUB | (IY+dd) | FD CBddAE | RES | 5,(IY+dd) |
| FD 9Edd | SBC | A,(IY+dd) | FD CBddB6 | RES | 6,(IY+dd) |
| FD A6dd | AND | (IY+dd) | FD CBddBE | RES | 7,(IY+dd) |
| FD AEdd | XOR | (IY+dd) | FD CBddC6 | SET | 0,(IY+dd) |
| FD B6dd | OR | (IY+dd) | FD CBddCE | SET | 1,(IY+dd) |
| FD BEdd | CP | (IY+dd) | FD CBddD6 | SET | 2,(IY+dd) |
| FD CBdd06 | RLC | (IY+dd) | FD CBddDE | SET | 3,(IY+dd) |
| FD CBdd0E | RRC | (IY+dd) | FD CBddE6 | SET | 4,(IY+dd) |
| FD CBdd16 | RL | (IY+dd) | FD CBddEE | SET | 5,(IY+dd) |
| FD CBdd1E | RR | (IY+dd) | FD CBddF6 | SET | 6,(IY+dd) |
| FD CBdd26 | SLA | (IY+dd) | FD CBddFE | SET | 7,(IY+dd) |
| FD CBdd2E | SRA | (IY+dd) | FD E1 | POP | IY |
| FD CBdd3E | SRL | (IY+dd) | FD E3 | EX | (SP),IY |
| FD CBdd46 | BIT | 0,(IY+dd) | FD E5 | PUSH | IY |
| FD CBdd4E | BIT | 1,(IY+dd) | FD E9 | JP | (IY) |
| FD CBdd56 | BIT | 2,(IY+dd) | FD F9 | LD | SP,IY |
| FD CBdd5E | BIT | 3,(IY+dd) | FE nn | * CP | nn |
| FD CBdd66 | BIT | 4,(IY+dd) | FF | * RST | 38 H |

## APPENDIX G <br> Cross-Reference of 8080 and Z-80 Instructions

The instructions are listed in alphabetic order according to the 8080 mnemonic. The following representations are used.

| N | 8 -bit constant |
| :--- | :--- |
| NN | 16 -bit constant |

R single register
RR double register

- range of values expressed as one character
-     - range of values expressed as two characters

| 8080 <br> code |  | HEX <br> code | Z-80 <br> code |  |
| :--- | :--- | :---: | :--- | :--- |
| ACI | N | CE | ADC | A,N |
| ADC | M | 8 E | ADC | A,(HL) |
| ADC | $R$ | $8-$ | ADC | A,R |
| ADD | M | 86 | ADD | A,(HL) |
| ADD | R | $8-$ | ADD | A,R |
| ADI | N | C6 | ADD | A,N |
| ANA | M | A6 | AND | (HL) |
| ANA | R | A- | AND | R |
| ANI | N | E6 | AND | N |
| CALL | NN | CD | CALL | NN |
| CC | NN | DC | CALL | C,NN |
| CM | NN | FC | CALL | M,NN |
| CMA |  | $2 F$ | CPL |  |
| CMC |  | $3 F$ | CCF |  |
| CMP | M | BE | CP | (HL) |
| CMP | R | B- | CP | R |
| CNC | NN | D4 | CALL | NC,NN |
| CNZ | NN | C4 | CALL | NZ,NN |
| CP | NN | F4 | CALL | P,NN |
| CPE | NN | EC | CALL | PE,NN |
| CPI | N | FE | CP | N |
| CPO | NN | E4 | CALL | PO,NN |
| CZ | NN | CC | CALL | Z,NN |


| $\begin{aligned} & 8080 \\ & \text { code } \end{aligned}$ |  | HEX <br> code | $\begin{aligned} & \mathrm{Z}-80 \\ & \text { code } \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: |
| DAA |  | 27 | DAA |  |
| DAD | B | 09 | ADD | HL,BC |
| DAD | D | 19 | ADD | HL, DE |
| DAD | H | 29 | ADD | HL,HL |
| DAD | SP | 39 | ADD | HL,SP |
| DCR | M | 35 | DEC | (HL) |
| DCR | R | -- | DEC | R |
| DCX | B | 0B | DEC | BC |
| DCX | D | 1B | DEC | DE |
| DCX | H | 2B | DEC | HL |
| DCX | SP | 3B | DEC | SP |
| DI |  | F3 | DI |  |
| EI |  | FB | EI |  |
| HLT |  | 76 | HALT |  |
| IN | N | DB | IN | A,(N) |
| INR | M | 34 | INC | (HL) |
| INR | R | -- | INC | R |
| INX | B | 03 | INC | BC |
| INX | D | 13 | INC | DE |
| INX | H | 23 | INC | HL |
| INX | SP | 33 | INC | SP |
| JC | NN | DA | JP | C,NN |
| JM | NN | FA | JP | M,NN |
| JMP | NN | C3 | JP | NN |
| JNC | NN | D2 | JP | NC,NN |
| JNZ | NN | C2 | JP | NZ,NN |
| JP | NN | F2 | JP | P,NN |
| JPE | NN | EA | JP | PE,NN |
| JPO | NN | E2 | JP | PO,NN |
| JZ | NN | CA | JP | Z,NN |
| LDA | NN | 3A | LD | A,(NN) |
| LDAX | B | 0A | LD | A,(BC) |
| LDAX | D | 26 | LD | A,(DE) |
| LHLD | NN | 2A | LD | HL,(NN) |
| LXI | B,NN | 01 | LD | BC,NN |
| LXI | D,NN | 11 | LD | DE,NN |
| LXI | H,NN | 21 | LD | HL,NN |
| LXI | SP,NN | 31 | LD | SP,NN |
| MOV | M,R | -- | LD | (HL), R |
| MOV | R,M | -- | LD | R,(HL) |
| MOV | R,R2 | -- | LD | R,R2 |
| MVI | M,N | 36 | LD | (HL),N |
| MVI | R,N | -- | LD | R,N |
| NOP |  | 00 | NOP |  |
| ORA | M | B6 | OR | (HL) |
| ORA | R | B- | OR | R |
| ORI | N | F6 | OR | N |
| OUT | N | D3 | OUT | (N), A |


| $\begin{aligned} & 8080 \\ & \text { code } \end{aligned}$ |  | HEX <br> code | $\begin{aligned} & \mathrm{Z}-80 \\ & \text { code } \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: |
| PCHL |  | E9 | JP | (HL) |
| POP | B | C1 | POP | BC |
| POP | D | D1 | POP | DE |
| POP | H | E1 | POP | HL |
| POP | PSW | F1 | POP | AF |
| PUSH | B | C5 | PUSH | BC |
| PUSH | D | D5 | PUSH | DE |
| PUSH | H | E5 | PUSH | HL |
| PUSH | PSW | F5 | PUSH | AF |
| RAL |  | 17 | RLA |  |
| RAR |  | 1F | RRA |  |
| RC |  | D8 | RET | C |
| RET |  | C9 | RET |  |
| RLC |  | 07 | RLCA |  |
| RM |  | F8 | RET | M |
| RNC |  | D0 | RET | NC |
| RNZ |  | C0 | RET | NZ |
| RP |  | F0 | RET | P |
| RPE |  | E8 | RET | PE |
| RPO |  | E0 | RET | PO |
| RRC |  | 15 | RRCA |  |
| RST | 0 | C7 | RST | 0 |
| RST | 1 | CF | RST | 8 |
| RST | 2 | D7 | RST | 10 H |
| RST | 3 | DF | RST | 18H |
| RST | 4 | E7 | RST | 20 H |
| RST | 5 | EF | RST | 28 H |
| RST | 6 | F7 | RST | 30 H |
| RST | 7 | FF | RST | 38H |
| RZ |  | C8 | RET | Z |
| SBB | M | 9E | SBC | A,(HL) |
| SBB | R | 9- | SBC | A,R |
| SBI | N | DE | SBC | A,N |
| SHLD | NN | 22 | LD | (NN),HL |
| SPHL |  | F9 | LD | SP,HL |
| STA | NN | 32 | LD | (NN), A |
| STAX | B | 02 | LD | (BC), A |
| STAX | D | 12 | LD | (DE), A |
| STC |  | 37 | SCF |  |
| SUB | M | 96 | SUB | (HL) |
| SUB | R | 9- | SUB | R |
| SUI | N | D6 | SUB | N |
| XCHG |  | EB | EX | DE,HL |
| XRA | M | AE | XOR | (HL) |
| XRA | R | A- | XOR | R |
| XRI | N | EE | XOR | N |
| XTHL |  | E3 | EX | (SP),HL |

## APPENDIX H <br> Details of the Z-80 and 8080 Instruction Set

A summary of the Z-80 and 8080 instruction set is given in this appendix.* The instructions are listed alphabetically by the official Zilog mnemonic. If there is a corresponding 8080 instruction, the Intel mnemonic is shown in angle brackets; if not, "no 8080 " is shown in the angle brackets. The Z-80 mnemonics are listed in numeric order in Appendix F. The Z-80 equivalent of an 8080 mnemonic can be found from the cross-reference given in Appendix G.

The letters A, B, C, D, E, H, I, L, IX, IY, R, and SP are used for the standard Z-80 register names. In addition, the symbols BC, DE, and HL are used for the register pairs. The following symbols are used for general arguments.

| r, r2 | 8-bit CPU register |
| :--- | :--- |
| dd | 8-bit signed displacement |
| nn | general 8-bit constant |
| nnnn | 16 -bit constant |

The flag bits are represented by:

| C | carry |
| :--- | :--- |
| H | half carry |
| N | add/subtract |
| P/O | parity/overflow |
| S | sign |
| Z | zero |

Pointers to memory or input or output addresses are enclosed in parentheses.

[^2]ADC Ay (HL) <ADC M)
Add the memory byte pointed to by the HL register pair to the accumulator and the carry flag. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

```
ALIC A, (IXtdd) <no 8080>
ADC Ay(IYtdd) धno 8080>
```

Add the memory byte referenced by the sum of the specified index register and the displacement to the accumulator and the carry flag. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

ADC Agr < ADC $\quad$ ?
Add the value in register $r$ to the accumulator and the carry flag. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z,
Flags reset: N

ADC Agrini <ACI riris
Add the constant given in the second operand to the accumulator and the carry flag. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

| ADC | $H L, B C$ | <no 8080$\rangle$ |
| :--- | :--- | :--- |
| ADC | $H L, H E$ | <no 8080$\rangle$ |
| ADC | $H L, H L$ | rno 8080$\rangle$ |
| ALIC | $H L, S F$ | rio 8080$\rangle$ |

Add the indicated double register to the HL register and the carry flag. The result is placed in HL.

Flags affected: C, H, O, S, Z,
Flag reset: N

ADD Ay (HL) SADIN M>
Add the memory byte pointed to by the HL pair to the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

```
ADII A,(IX+dd) <no 8080)
ADD Ag(IY+dd) <no 8080>
```

Add the memory byte pointed to by the sum of the specified index register and the displacement to the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

ADD Apr <ADI r>
Add the value in register $r$ to the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag reset: N

ADD Agrin <ADI nn>
Add the immediate byte (the second operand) to the accumulator. The result is placed in A.

Flags affected: C, H, O, S, Z
Flag reset: N

| ADD | HL, ECC | $<D_{A D}$ | 8) |
| :---: | :---: | :---: | :---: |
| AIDD | HL, DE | <DAI | I1) |
| ADD | HL.9HL. | <nAI | H |
| ADD | HL. SP | <IALI |  |

Add the specified double register to the HL pair. The result is placed in HL. This is a double-precision addition. The carry flag is set if an overflow occurs. The instruction ADD HL,HL performs a 16 -bit arithmetic shift left, effectively doubling the value in HL. The ADD HL,SP instruction can be used with the 8080 CPU to save an incoming stack pointer:

| LXI | H,0 |
| :--- | :--- |
| DAD | SP |
| SHLD | nnnn |

Flags affected: C, H, O, S, Z
Flag reset: N

| AIID | IX, BC | <no 8080> |
| :---: | :---: | :---: |
| ALIS | IX, DE | <no 8000. |
| ADID | IX, IX | <no 8080> |
| ALII | IX,SF' | <no 8080) |
| ADD | IY, BC | <no 8080> |
| ADD | IY,DE | <no 8080> |
| ALID | IY,IY | <no 8080> |
| ADD | IY, SF | <no 8080> |

Add the indicated double register to the specified index register. The result is placed in the index register. The HL register pair does not participate in this group of instructions. Notice that there is no equivalent series of ADC instructions.

Flags affected: C, O, S, Z
Flag reset: N

ANH (HL) $\because A N A$ M.
Perform a logical AND with the accumulator and the memory location pointed to by the HL register pair. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, N
Flag set: H

| AND | $(I X+d d)$ | $<n o ~ 8080\rangle$ |
| :--- | :--- | :--- |
| AND | $(I Y+d d)$ | nno 8080$\rangle$ |

Perform a logical AND with the accumulator and the memory byte referenced by the sum of the index register and displacement. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, N
Flag set: H
AND $r$ SANA $r$ >

Perform a logical AND with the accumulator and register $r$. The result is placed in the accumulator. An instruction AND A is an effective way to test the parity, sign, and zero flags.

Flags affected: P, S, Z
Flags reset: C, N
Flag set: H

AND nI $\angle A N I$ nis
Perform a logical AND with the accumulator and the constant given in the argument. The result is placed in the accumulator. This instruction can be used to selectively reset bits of the accumulator. For example, the instruction AND 7FH will reset bit 7.

Flags affected: P, S, Z
Flags reset: C, N
Flag set: H

| BIT | $b y(H L)$ | nio 8080$\rangle$ |
| :--- | :--- | :--- |
| BIT | $b y(I X+d \sigma)$ | no 8080$\rangle$ |
| BIT | $b y(I Y+d \sigma)$ | rio 8080$\rangle$ |

Test bit b of the memory byte referenced by the second operand. Bit b can range from zero through 7 . The zero flag is set if the referenced bit is a logical 1 ; otherwise, it is reset. Thus, the zero flag becomes the complement of the selected bit.

Flag affected: Z
Flag set: H
Flag reset: N

BIT ber rio 8080:
Test bit $b$ of register $r$, where $b$ can range from zero through 7 . The zero flag is set if the referenced bit is a logical 1. It is reset otherwise.

Flag affected: Z
Flag set: H
Flag reset: N

CALL rororore ©CALL rorirori>
Unconditional subroutine call to address nnnn. The address of the following instruction is pushed onto the stack.

Flags affected: none

| CALL | Conriror | $<\mathrm{CC}$ | normers |
| :---: | :---: | :---: | :---: |
| CALL | Megonnei | cM | nerinis) |
| CALL | NC y morron | CNC | nomiri> |
| CAll | NZ eronerin | $\triangle \mathrm{CNZ}$ | rimbris: |
| CALLIL | Peporina | $<C F$ | rimines |
| CALL | FEgronirin | $\triangle C F E$ | niminas: |
| CALL | FOg rinoro | CFO | rinnori. |
| CALL | Zennorn | $\therefore \mathrm{CZ}$ | nirinris |

Conditional subroutine call to address nnnn. The address of the following instruction is pushed onto the stack. The conditions are:

| C | carry flag set | (carry) |
| :--- | :--- | :--- |
| M | sign flag set | (minus) |
| NC | carry flag reset | (not carry) |
| NZ | zero flag reset | (not zero) |
| P | sign flag reset | (plus) |
| PE | parity flag set | (parity even) |
| PO | parity flag reset | (parity odd) |
| Z | zero flag set | (zero) |

```
CCF
\(<\) CMC >
```

Complement the carry flag. This instruction can be given after a SCF command to reset the carry flag.

Flag affected: C
Flag reset: N

CF (HL) CMF M.
Compare the byte in memory pointed to by the HL pair to the accumulator (an implied operand). The zero flag is set if the accumulator is equal to the operand. The carry flag is set if the accumulator is smaller than the operand.

Flags affected: C, H, O, S, Z
Flag set: N

| CF | $(I X+d d)$ | <no 8080) |
| :--- | :--- | :--- |
| CF | $(I Y+d \alpha)$ | no 8080 |

Compare the memory location referenced by the sum of the index register and displacement to the accumulator which is an implied operand. The zero flag is set if the accumulator is equal to the operand. The carry flag is set if the accumulator is smaller than the operand.

Flags affected: C, H, O, S, Z
Flag set: N

CF $r$ CMF $r$
Compare register $r$ to the accumulator, which is an implied operand. The zero flag is set if the accumulator is equal to the operand. The carry flag is set if the accumulator is smaller than the operand.

Flags affected: C, H, O, S, Z
Flag set: N

CF rin $\langle C F I$ rin>
Compare the constant given in the operand to the accumulator, which is an implied operand. The zero flag is set if the accumulator is equal to the operand. The carry flag is set if the accumulator is smaller than the operand.

Flags affected: C, H, O, S, Z
Flag set: N

```
CFU <no 8080>
CPUR <no 8080>
CFI <no 8080>
CPIR <no 8080>
```

Compare the memory byte pointed to by HL to the accumulator. Decrement HL (if D) or increment HL (if I). Decrement the byte count in the BC register. Repeat the operation for CPDR and CPIR until a match is found or until the BC register pair has been decremented to zero. The zero flag is set if a match is found. The parity flag is set if BC is decremented to zero.

Flags affected: H, S
Flags set: $\mathrm{N}, \mathrm{Z}$ if $\mathrm{A}=(\mathrm{HL}), \mathrm{P}$ if $\mathrm{BC}=0$

CPL $\langle C M A>$
Complement the accumulator. This instruction performs a one's complement on the accumulator. (Compare to the instruction NEG.)

Flags set: H, N

DAA $<$ MAA $>$
Decimal adjust the accumulator. This instruction is used after each addition with BCD numbers. The Z-80 performs this operation properly for both addition and subtraction. The 8080, however, gives an incorrect result for subtraction.

Flags affected: O, S, Z, C, H
$\overline{\text { DEC }}$ (HL) $\angle \mathrm{LLCR}$ M

Decrement the memory byte pointed to by the HL register pair.
Flags affected: H, O, S, Z
Flag set: N
Flag not affected: C

| DEC | $(I X+d d)$ | no $8080 \%$ |
| :--- | :--- | :--- |
| DEC | $(I Y+d d)$ | no 8080$\rangle$ |

Decrement the memory byte pointed to by the sum of the index register and the displacement.

Flags affected: H, O, S, Z
Flag set: N
Flag not affected: C

```
DEC r <LICR r>
```

Decrement the register r. Don't try to decrement a register past zero while executing a JP NC loop. The carry flag is not affected by this operation.

Flags affected: H, O, S, Z
Flag set: N
Flag not affected: C

| IEC | BC | $\operatorname{mcx}$ | B) |
| :---: | :---: | :---: | :---: |
| DEC | UE | macx | 1) |
| DEC | HL | 4 mcx | H |
| DEC | SP | mcx | SF' |

Decrement the indicated double register. Don't try to decrement a double register to zero in a JP NZ loop. It won't work since this operation does not affect any of the PSW flags. Instead, move one byte of the double register into the accumulator and perform a logical OR with the other byte.

| LD | A,C |
| :--- | :--- |
| OR | B |
| JR | NZ,nnnn |

Flags affected: none!!!!

| DEC | IX | no 8080. |
| :--- | :--- | :--- |
| DEC | IY | no 8080. |

Decrement the index register.
Flags affected: none

DI < MI >
Disable maskable interrupt request.

IJNZ dd «no 8080>
Decrement register $B$ and jump relative to displacement dd if $B$ register is not zero.

Flags affected: none
$E I<E I>$
Enable maskable interrupt request.

Exchange the byte at the stack pointer with register L. Exchange the byte at the stack pointer +1 with register $H$.

Flags affected: none

| EX | (SF'), IX | <no 8080\% |
| :---: | :---: | :---: |
| EX | (SF), IY | <no 8080) |

Exchange the 16 bits referenced by the stack pointer with the specified index register.

Flags affected: none

```
EX AFgAF, <no 8080>
```

Exchange the accumulator and flag register with the alternate set.
Flags affected: all

```
EX DEgHL < XCHG >
```

Exchange the double registers DE and HL.
Flags affected: none

EXX <no 8080>
Exchange BC, DE, and HL with the alternate set.
Flags affected: none

HALT
$\langle$ HLT >
Suspend operation of the CPU until a reset or interrupt occurs. Dynamic memory refresh continues during a halt.
$\qquad$

| IM | 0 | $<n o 8080\rangle$ |
| :--- | :--- | :--- |
| IM | 1 | $<n o 8080\rangle$ |
| IM | 2 | $<n o 8080\rangle$ |

Sets interrupt mode 0,1 , or 2 . Interrupt mode 0 is automatically selected when a Z-80 reset occurs. The result is the same as the 8080 interrupt response. Interrupt mode 1 performs an RST 38 H instruction. Interrupt mode 2 provides for many interrupt locations.

IN $\quad \mathrm{rg}(\mathrm{C})$ (no 8080)
${ }^{9}$ Input a byte from the port address in register C to register r .
Flags affected: P, S, Z
Flags reset: H, N

IN Ag(nn) <IN nin)
Input a byte from the port address nn to the accumulator.
Flags affected: none

INC (HL) $\leq I N R \quad M>$
Increment the memory byte pointed to by the HL pair.
Flags affected: H, O, S, Z
Flag set: N
Flag not affected. C!!!!

```
INC (IX+dd) <no 8080>
INC (IY+dd) <no 8080>
```

Increment the memory byte pointed to by the sum of the index register and the displacement.

Flags affected: H, O, S, Z
Flag set: N
Flag not affected: C!!!

INC $r$ <INR $r>$
Increment the 8 -bit register r. Don't try to increment a register past zero while executing a JP NC loop. It won't work because the carry flag is unaffected by this instruction.

Flags affected: H, O, S, Z
Flag set: N
Flag not affected: C!!!

| INC | $B C$ | $\angle I N X$ | $B\rangle$ |
| :--- | :--- | :--- | :--- |
| INC | $D E$ | $\angle I N X$ | $D\rangle$ |
| $I N C$ | $H L$ | INX | $H\rangle$ |
| INC | $S P$ | $\angle I N X$ | $S F\rangle$ |

Increment the specified double register.
Flags affected: none!!!!

| INC | IX | no 8080 - |
| :--- | :--- | :--- |
| INC | IY | no 8080 . |

Increment the specified index register.
Flags affected: none

| IND | no $8080 \%$ |
| :--- | :--- |
| INAR | no $8080 \%$ |
| INI | no $8080 \%$ |
| INIR | no $8080 \%$ |

Input a byte from the port address in register $C$ to the memory byte pointed to by HL. Decrement register B. The HL register is incremented (if I) or decremented (if D). For INDR and INIR the process is repeated until the 8-bit register B becomes zero.

Flag affected: Z (if B=0)
Flag set: N

JF (HL) < PCHL >
Copy the HL register pair into the program counter; then retrieve the next instruction from the address referenced by HL. This instruction causes a jump to the address referenced by HL.

Flags affected: none

| JF | $(I X)$ | (no 8080> |
| :--- | :--- | :--- |
| JF | $(I Y)$ | sno $8080>$ |

Copy the contents of the specified index register into the program counter; then retrieve the next instruction from the address referenced by IX or IY.

Flags affected: none
$\qquad$
JP nnnn <JMP nnnor.>
Unconditional jump to address nnnn.
Flags affected: none

| JF | Comrimin | $<\mathrm{JC}$ | nnon) |
| :---: | :---: | :---: | :---: |
| JF | Manninn | <JM | nnnnis |
| JF | NCinnmin | <JNC | nrinios |
| JF | NZgnnimi | <JJZ | ninimi |
| JP | Perinmorn | <JF' | nnins |
| JP | PEgnnon | <JPE | nnins: |
| JF' | Pognnmin | <JPO | nnini. |
| JP | Zannan | < JZ | nnni |

Conditional jump to address nnnn where:

| C | means carry flag set | (carry) |
| :--- | :--- | :--- |
| M | means sign flag set | (minus) |
| NC | means carry flag reset | (not carry) |
| NZ | means zero flag reset | (not zero) |
| P | means sign flag reset | (plus) |
| PE | means parity flag set | (parity even) |
| PO | means parity flag reset | (parity odd) |
| Z | means zero flag set | (zero) |

JR do sno 8080)
Unconditional relative jump with a signed displacement $n n$. The jump is limited to 129 bytes forward and 126 bytes backward in memory.

Flags affected: none

| JR | C.gd | <no 8080> |
| :---: | :---: | :---: |
| JR | NCrids | <no 8080) |
| JR | NZ.dd | <no 8080) |
| JR | Zodd | <no 8080> |

Conditional relative jump to address nn where:

| C | means carry flag set | (carry) |
| :--- | :--- | :--- |
| NC | means carry flag reset | (not carry) |
| NZ | means zero flag reset | (not zero) |
| Z | means zero flag set | (zero) |


| LII | (BC) $A$ | $<\mathrm{STAX}$ |
| :---: | :---: | :---: |
| La | (DE), $A$ | $\because S T A X$ |

Move the byte in the accumulator to the memory byte referenced by the specified register pair.

```
LD (HL)OP <MOV Mor>
```

Move the byte in register $r$ to the memory byte pointed to by the HL pair.

```
LD (HL),nn <MUI Monn>
```

Move the immediate byte nn into the memory byte referenced by the HL pair.

| LD | ( $1 \times+d d$ ) ${ }^{\text {r }}$ | <no 8080> |
| :---: | :---: | :---: |
| LD | ( IX $\mathrm{C}+\mathrm{dd}$ ) m n | <no 8080\% |
| LD | (IY+dd)er | <no 8080> |
| LD | ( IY+dd) n nn | no |

Move the byte in register r or the immediate byte nn into the memory byte referenced by the sum of the index register plus the displacement. These instructions can be used to load relocatable binary code.

```
LD (nmmri),A <STA nomri>
```

Store the accumulator in the memory location referenced by nnnn.


Store the low-order byte ( C or E ) of the specified double register at the memory location nnnn. Store the high-order byte (B or D) at nnnn +1 .

```
LD (noririn)OHL <SHLII rirION`
```

Store register L at the memory address nnnn. Store register H at the address $n n n n+1$.

| 10 | (nnoni) , IX | <no 8080> |
| :---: | :---: | :---: |
| LD | (rinori) ${ }^{\text {I }}$ I | <no 8080> |
| L0 | (nnom) , SP | uno 8080. |

Store the low-order byte of the specified register IX, IY, or SP at the location nnnn. Store the high-order byte at nnnn +1 . The instruction LD (nnnn), SP can be used to temporarily save an incoming stack pointer. It can later be restored by a LD SP,(nnnn) operation.

| $L D$ | $A y(B C)$ | $\operatorname{LDAX}$ | $B\rangle$ |
| :--- | :--- | :--- | :--- |
| $L D$ | $A y(D E)$ | $\operatorname{LDAX}$ | $D>$ |

Move the memory byte referenced by the specified register pair BC or DE into the accumulator.

```
LD A.I <no BO80.
```

Load the accumulator from the interrupt-vector register. The parity flag reflects the state of the interrupt-enable flip-flop.

Flags affected: S, Z, P
Flags reset: H, N

LD A,R 《no 8080>
Load the accumulator from the memory-refresh register. The parity flag reflects the state of the interrupt-enable flip-flop. This is an easy way to obtain a fairly decent random number.

Flags affected: S, Z, P
Flags reset: H, N

```
LII I.A <no 8080>
```

Copy the accumulator into the interrupt-vector register.
Flags affected: none

LD R.A <no 8080>
Copy the accumular into memory-refresh register.
Flags affected: none

```
LIN ry(HL) <MOU r.M>
```

Move the byte in the memory location pointed to by the HL register pair into register r.

```
Ln ry(IX+d\sigma) <no 8080>
LD ry(IYtod) <no 8080>
```

Move the byte at the memory location referenced by the sum of the index register and the displacement into register $r$.
LD rir2 <mov rirz>

Move the byte from register r 2 to r .

LD rinn <MUI rinn>
Load register r with the 8 -bit data byte nn .

LD Ag (romin) <LDA riorn>
Load the accumulator from the memory byte referenced by the 16 -bit pointer nnnn.

| LD | BC, (ronnm) | <no 8080) |
| :---: | :---: | :---: |
| Lil | DEy (rinini) | <no 8080. |

Load the low-order byte ( C or E ) from the location referenced by the 16 -bit pointer nnnn. Load the high-order byte (B or D) from nnnn +1 .

```
LD HL.(mnrm) <LHLD nronri)
```

Load register $L$ from the address referenced by the 16 -bit value nnnn. Load register H from the address $n n n n+1$.

| 4 LI | BCennonn | $<\operatorname{LXI}$ | Benrinnis |
| :---: | :---: | :---: | :---: |
| LII | DEgnnorn | <LXI | Denminno |
| LIN | HL enorna | $<L X I$ | Henrorins |
| LII | SFermorin | $<\mathrm{LXI}$ | SPanmmis |
| LII | IX, minini | no | 8080.) |
| LD | IYgninni | <no | 8080) |

Load the specified double register with the 16 -bit constant nnnn. Be careful not to confuse LD HL,(nnnn) with LD HL,nnnn.

| LII | IX ( ${ }^{\text {rinnris }}$ ) | <no 8080) |
| :---: | :---: | :---: |
| 1.10 | IVg (nninn) | <no 8080> |
| LII | SPM (nnmo) | <rio 8080> |

Load the low byte of IX, IY, or SP from the memory location nnnn. Load the high byte from nnnn +1 . The LD SP,(nnnn) instruction can be used to retrieve a previously saved stack pointer.

| LI | SPOHL | < SFHL > |
| :---: | :---: | :---: |
| L.ID | SP, IX | <no 8080) |
| LD | SPPIY | <no 8080) |

Load the stack pointer from the specified 16 -bit register. The SPHL instruction can be used to retrieve a previously saved stack pointer when the 8080 CPU is used.
LHLD nnnn
SPHL

| LDI | <no 8080 ${ }^{\text {¢ }}$ |
| :---: | :---: |
| LDPR | <ino 8080> |
| LDI | <no 8080) |
| LTIR | <no 8080> |

Move the byte referenced by the HL pair into the location pointed to by the DE register pair. Decrement the 16 -bit byte counter in BC. Increment (if I) or decrement (if D) both HL and DE. Repeat the operation for LDDR and LDIR until the BC register has been decremented to zero.

NEG
《no 8080>
This instruction performs a two's complement on the accumulator. It effectively subtracts the accumulator from zero. To perform this task on an 8080, use a CMA command followed by an INR A command.

Flags affected: all

NOP
$<$ NOF >
No operation is performed by the CPU.
Flags affected: none

OR (HL) $\langle O R A$ M>
Perform a logical OR with the accumulator and the byte referenced by HL. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, H, N

| $O R$ | $(I X+d d)$ | <no 8080> |
| :--- | :--- | :--- |
| $O R$ | $(I Y+d d)$ | <no 8080 $\rangle$ |

Perform a logical OR with the accumulator and the byte referenced by the specified index register plus the displacement. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, H, N

```
OR r <ORA r>
```

Perform a logical OR with the accumulator and the register $r$. The result is placed in the accumulator. An instruction of OR A is an efficient way to test the parity, sign, and zero flags.

Flags affected: P, S, Z
Flags reset: C, H, N

OF NT $S O R I$ riris
Perform a logical OR with the accumulator and the byte nn . The result is placed in the accumulator. This instruction can be used to set individual bits of the accumulator. For example, OR 20 H will set bit 5 to a logical 1.

Flags affected: P, S, Z
Flags reset: C, H, N

```
OTDR <no 8080>
```

Output a byte from the memory location pointed to by the HL pair. The port address is contained in register C. Register B is decremented. The HL register pair is incremented (if I) or decremented (if D). The process is repeated until register $B$ has become zero.

Flags set: N, Z

OUT (C) \&r sno 8080)
Output the byte in register $r$ to the port address contained in register C.
Flags affected: none
$\qquad$
OUT (rin),A <OUT nri.
Output the byte in the accumulator to the port address $n n$.
Flags affected: none

|  |  |
| :---: | :---: |
| OUTD | <no 8080> |
| OUTI | <no 8080 $>$ |

Output a byte from the memory location pointed to by the HL pair. The port address is contained in register C. Register B is decremented. The HL register pair is incremented (if I) or decremented (if D).

Flag affected: Z
Flag set: N


Move the byte at the memory location referenced by the stack pointer into the flag register (PSW), and increment the stack pointer. Then move the byte at the location referenced by the new stack-pointer value into the accumulator and increment the stack pointer a second time.

Flags affected: all

| FOF | BC | FOF | B |
| :--- | :--- | :--- | :--- |
| FOF | DE | FOF | D |
| FOF | HL | FOF | $H\rangle$ |

Copy two bytes of memory into the appropriate double register as follows. The memory byte referenced by the stack pointer is moved into the loworder byte ( $\mathrm{C}, \mathrm{E}$, or L ), then the stack pointer is incremented. The memory byte referenced by the new stack pointer is then moved into the high-order byte ( $\mathrm{B}, \mathrm{D}$, or H ). The stack pointer is incremented a second time.

Flags affected: none

|  |  |  |
| :--- | :--- | :--- |
| FOF | IX | 亿no 8080> |
| FOF | IY | no 8080. |

Copy the top of the stack into the specified index register. Increment the stack pointer twice.

Flags affected: none

PUSH AF <FUSH FSW.
Store the accumulator and flag register in memory as follows. The stack pointer is decremented, then the value in the accumulator is moved to the memory byte referenced by the stack pointer. The stack pointer is decremented a second time. The flag register is copied to the byte at the memory address referenced by the current stack-pointer position.

Flags affected: none

| FUSH | BC | FUSH | B) |
| :--- | :--- | :--- | :--- |
| FUSH | IE | FUUSH | ID |
| FUSH | HL | \&FUSH | H) |

Store the referenced double register in memory as follows. The stack pointer is decremented, then the byte in the specified high-order register $\mathrm{B}, \mathrm{D}$, or H is copied to the memory location referenced by the stack pointer. The stack pointer is decremented a second time. The byte in the low-order position C, E , or L is moved to the byte referenced by the current value of the stack pointer.

Flags affected: none

| PUSH | IX | 亿no 8080〉 |
| :--- | :--- | :--- |
| FUSH | IY | no 8080＞ |

The indicated index register is copied to the top of the stack．The stack pointer is decremented twice．

Flags affected：none

| RES | $b,(H L)$ | ＜no 8080＞ |
| :--- | :--- | :--- |
| RES | $b,(I X+\sigma d)$ | 亿no 8080＞ |
| RES | $b,(I Y+\sigma d)$ | 亿no 8080＞ |

Reset bit b of the memory byte referenced by the second operand．Bit b can range from zero through 7.

Flag reset： N
Other flags affected：none

RES ber＜no 8080＞
Reset bit b of register $r$ to a value of zero．Bit b can range from zero through 7.
Flag reset：N
Other flags affected：none

RET＜RET＞
Return from a subroutine．The top of the stack is moved into the program counter．The stack pointer is incremented twice．

| RET | $C$ | $<R C\rangle$ |
| :--- | :--- | :--- |
| RET | $M$ | $<R M\rangle$ |
| RET | NC | $<R N C\rangle$ |
| RET | $N Z$ | $<R N Z\rangle$ |
| RET | P | $\langle R F\rangle$ |
| RET | PE | $<R P E\rangle$ |
| RET | $F O$ | $<R P D\rangle$ |
| RET | $Z$ | $<R Z\rangle$ |

Conditional return from a subroutine．If the condition is met，the top of the stack is moved into the program counter．The stack pointer is incre－ mented twice．

| C | means carry flag set | （carry） |
| :--- | :--- | :--- |
| M | means sign flag set | （minus） |
| NC | means carry flag reset | （not carry） |
| NZ | means zero flag reset | （not zero） |
| P | means sign flag reset | （plus） |
| PE | means parity flag set | （parity even） |
| PO | means parity flag reset | （parity odd） |
| Z | means zero flag set | （zero） |

```
RETI <no 8080>
```

Return from maskable interrupt.

```
RETN <no 8080>
```

Return from nonmaskable interrupt.

The following RL and RLA instructions rotate bits to the left through carry.


RL (HL) <no 8080):
The memory byte referenced by the HL pair is rotated left through carry. The carry flag moves into bit zero. Bit 7 moves to the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

| FiL | $(I X+d \alpha)$ | (no 8080) |
| :--- | :--- | :--- |
| RLL | $(I Y+d \alpha)$ | no 8080 ) |

The memory byte referenced by the sum of the index register and the displacement is rotated left through carry. The carry flag moves into bit zero. Bit 7 moves to the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

FiL $r$ <no 8080>
The byte in register $r$ is rotated left through carry. The carry flag moves into bit zero. Bit 7 moves to the carry flag. Note: the instruction RL A performs the same task that the separate instruction RLA does, but the former takes twice as long as the latter.

Flags affected: C, P, S, Z
Flags reset: H, N

$$
\text { RLA }<\text { RAL }>
$$

The byte in the accumulator is rotated left through carry. The carry flag moves to bit zero. Bit 7 of the accumulator moves to the carry flag.

Flag affected: C
Flags reset: H, N

The following RLC and RLCA instructions rotate bits to the left.


The byte referenced by the HL pair is rotated left circularly. Bit 7 moves to both the zero bit and to the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

| FLLC | $(I X+d d)$ | (no 8080) |
| :--- | :--- | :--- |
| RLC | $(I Y+d d)$ | no 8080 ) |

The byte referenced by the specified index register plus the displacement is rotated left circularly. Bit 7 moves to both bit zero and the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

RLC r <no 8080>
The byte in register $r$ is rotated left circularly. Bit 7 moves to both bit zero and the carry flag. Note: RLC A performs the same task that another instruction RLCA does, but the former instruction takes twice as long as the latter.

Flags affected: C, P, S, Z
Flags reset: H, N

RLCA < RLC >
The accumulator is rotated left circularly. Bit 7 moves to both bit zero and the carry flag.

Flag affected: C
Flags reset: H, N

RLLI
《no 8080)
A 4 -bit rotation over 12 bits. The low 4 bits of A move to the low 4 bits of the memory location referenced by the HL pair. The original low 4 bits of
memory move to the high 4 bits. The original high 4 bits move to the low 4 bits of A. This instruction is used for BCD operations.

Flags affected: P, S, Z
Flags reset: H, N


The following $R R$ and $R R A$ instructions rotate bits to the right through carry.


RR (HL) <no 8080>
The memory byte pointed to by the HL pair is rotated right through carry. Carry moves to bit 7. Bit zero moves to the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

| $R R$ | $(I X+d d)$ | no 8080$\rangle$ |
| :--- | :--- | :--- |
| $R R$ | $(I Y+d d)$ | no 8080 |

The memory byte pointed to by the specified index register plus the offset is rotated right through carry. The carry flag moves to bit 7 . Bit zero moves to the carry flag.

Flags affected: C, P, S, Z
Flags reset: H, N

FR $r$
©no 8080)
The byte in register $r$ is rotated right through carry. Carry moves to bit 7. Bit zero moves to the carry flag. Note: RR A performs the same task that another instruction RRA does, but the former instruction takes twice as long as the latter.

Flags affected: C, P, S, Z
Flags reset: H, N

RRA < RAR >
The accumulator is rotated right through carry. The carry flag moves to bit 7. Bit zero moves to the carry flag.

Flag affected: C Flags reset: H, N

The following RRC and RRCA instructions rotate bits to the right.


RRC (HL) <no 8080>
The memory byte pointed to by the HL pair is rotated right circularly. Bit zero moves to both the carry flag and bit 7 .

Flags affected: C, P, S, Z
Flags reset: H, N

| RRC | (IXtod) | nno 8080$\rangle$ |
| :--- | :--- | :--- |
| RRC | (IYtod) | ino 8080 . |

The memory byte pointed to by the index register plus the offset is rotated right circularly. Bit zero moves to both the carry flag and bit 7 .

Flags affected: C, P, S, Z
Flags reset: H, N

FRFC $r$ no 8080>
The byte in register $r$ is rotated right circularly. Bit zero moves to both the carry flag and bit 7. Note: RRC A performs the same task that another instruction RRCA does, but the former instruction takes twice as long as the latter.

Flags affected: C, P, S, Z
Flags reset: H, N

FRCA < RRC >
The accumulator is rotated right circularly. Bit zero moves to both the carry flag and bit 7.

Flag affected: C
Flags reset: H, N

RRD <no 8080)
A 4-bit rotation over 12 bits. The low 4 bits of $A$ move to the high 4 bits of the memory location referenced by the HL pair. The original high 4 bits of memory move to the low 4 bits. The original low 4 bits move to the low 4 bits of A . This instruction is used for BCD operations.

Flags affected: P, S, Z
Flags reset: $\mathrm{H}, \mathrm{N}$


| RST $00 H$ | $<R S T$ | $0\rangle$ |
| :--- | :--- | :--- |
| RST O8H | $\langle R S T$ | $1\rangle$ |
| RST $10 H$ | $\langle R S T$ | $2\rangle$ |
| RST $18 H$ | $<R S T$ | $3\rangle$ |
| RST 20H | $\langle R S T$ | $4\rangle$ |
| RST $28 H$ | $<R S T$ | $5\rangle$ |
| RST $30 H$ | $<R S T$ | $6\rangle$ |
| RST $38 H$ | <RST 7$\rangle$ |  |

These restart instructions generate one-byte subroutine calls to address given in the Z-80 operand.

SBC $A,(H L) \because S E B \quad M>$
Subtract the carry flag and the memory byte pointed to by the HL pair from the accumulator. The result is placed in the accumulator. Some $\mathrm{Z}-80$ assemblers allow the 8080 mnemonic of SBB to be used as an alternate Z-80 mnemonic for this instruction.

Flags affected: C, H, O, S, Z
Flag set: N

| SEC | Ag $(I X+d d)$ | sno 8080 ) |
| :--- | :--- | :--- |
| SEC | Ag $(I Y+d d)$ | no 8080) |

Subtract the carry flag and the memory byte pointed to by the sum of the index register and displacement from the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag set: N

SBC Apr <SBB r>
Subtract the carry flag and the specified CPU register from the accumulator. The result is placed in the accumulator. Some Z-80 assemblers allow the 8080 mnemonic of SBB to be used as an alternate Z-80 mnemonic for this instruction.

Flags affected: C, H, O, S, Z
Flag set: N

SBC A,nn <SBI nn>
Subtract the immediate byte (the second operand) and the carry flag from the accumulator. The result is placed in the accumulator. Some Z-80 assemblers allow the 8080 mnemonic of SBB to be used as an alternate Z-80 mnemonic for this instruction.

Flags affected: C, H, O, S, Z
Flag set: N

| SBC | HL, BC | <no | $8080 \%$ |
| :---: | :---: | :---: | :---: |
| SRC | HL, DE | <no | 8080) |
| SBC | HL, HL | <no | 8080> |
| SEC | HL, SP | <no | 8080) |

Subtract the specified CPU double register and the carry flag from the HL register pair. The result is placed in HL. You may need to reset the carry flag with an OR A operation before using these instructions.

Flags affected: C, H, O, S, Z
Flag set: N

SCF < STC $>$
Set the carry flag. There is no equivalent reset command. However, the carry flag can be reset with the XOR A instruction, or with the pair of instructions SCF and CCF.

Bit set: C
Bits reset: H, N

| SET | $b,(H L)$ | no 8080$\rangle$ |
| :--- | :--- | :--- |
| SET | $b,(I X+d d)$ | no 8080$\rangle$ |
| SET | $b,(I Y+d d)$ | no $8080>$ |

Set bit b of the memory byte referenced by the second operand. Bit b can range from zero through 7 .

Flag reset: N
Other flags affected: none

```
SET byr <no 8080.>
```

Set bit $b$ of register $r$. Bit $b$ can range from zero through 7.
Flag reset: N
Other flags affected: none

The following SLA instructions shift bits to the left.


Perform an arithmetic shift left on the memory byte pointed to by the HL pair. Bit 7 is moved to the carry flag. A zero is moved into bit zero. This operation doubles the original value.

Bits affected: C, P, S, Z
Bits reset: H, N

| SLA | $(I X+d d)$ | rno 8080) |
| :--- | :--- | :--- |
| SLA | $(I Y+d d)$ | no 8080$\rangle$ |

Perform an arithmetic shift left on the memory byte pointed to by the index register plus the displacement. Bit 7 is moved to the carry flag. A zero is moved into bit zero. This operation doubles the original value.

Bits affected: C, P, S, Z
Bits reset: H, N

```
SLA <r00 8080>
```

Perform an arithmetic shift left on register $r$. Bit 7 is moved to the carry flag. A zero is moved into bit zero. This operation doubles the original value. Note: SLA A performs the same task that another instruction ADD A,A does, but the former instruction takes twice as long as the latter.

Bits affected: C, P, S, Z
Bits reset: H, N

The following SRA instructions shift bits to the right.


SRA (HL) <no 8080>
Perform an arithmetic shift right on the memory byte pointed to by the HL pair. Bit zero moves to the carry flag. Bit 7 is duplicated in bit 6.

Bits affected: C, P, S, Z
Bits reset: H, N

| SFiA | $(I X+d d)$ | <no 8080> |
| :--- | :--- | :--- |
| SRA | $(I Y+d d)$ | ®no 8080〉 |

Perform an arithmetic shift right on the byte pointed to by the index register plus the displacement. Bit zero moves to carry and bit 7 is duplicated into bit 6.

Bits affected: C, P, S, Z
Bits reset: H, N

SFA $r$ no 8080.
Perform an arithmetic shift right on register $r$. Bit zero moves to carry and bit 7 is duplicated into bit 6. The operation effectively halves the register value. The carry flag represents the remainder. The carry flag is set if the original number was odd.

Bits affected: C, P, S, Z
Bits reset: H, N

The following SRL instructions shift bits to the right.


SRL (HL) 《no 8080>
Perform a logical shift right on the byte pointed to by the HL register pair. A zero bit is moved into bit 7. Bit zero moves to the carry flag.

Bits affected: C, P, Z
Bits reset: H, N, S

| SRL | (IX+dd) | $\because$ no 8080) |
| :---: | :---: | :---: |
| SRL | ( IY+dd) | $<\mathrm{no} 8080$ |

Perform a logical shift right on the byte pointed to by the index register plus the displacement. A zero bit is moved into bit 7. Bit zero moves to the carry flag.

Bits affected: C, P, Z
Bits reset: H, N, S

SRL $r$ <no 8080 >
Perform a logical shift right on register r. A zero bit is moved into bit 7. Bit zero moves to the carry flag.

Bits affected: C, P, S, Z
Bits reset: H, N

SUB (HL) <SUB M>
Subtract the memory byte referenced by the HL pair from the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag set: N

| SUB | (IX+dd) | rno 8080$\rangle$ |
| :--- | :--- | :--- |
| SUB | (IYtdd) | no 8080$\rangle$ |

Subtract the memory byte referenced by the index register plus the displacement from the value in the accumulator. The result is placed in A.

Flags affected: C, H, O, S, Z
Flag set: N

SUB $r$ SUE r>
Subtract the specified CPU register from the accumulator. The result is placed in the accumulator. Notice that Z-80 SUB mnemonic has only one operand, whereas there are two operands in the corresponding 8-bit ADC, ADD, and SBC mnemonics. The destination operand for all four of these instructions is always the accumulator. Consequently, the first operand is optional with some assemblers.

Flags affected: C, H, O, S, Z
Flag set: N

SUB nn «SUI rins
Subtract the immediate byte nn from the accumulator. The result is placed in the accumulator.

Flags affected: C, H, O, S, Z
Flag set: N

XOR (HL) <XRA M)
Perform a logical exclusive OR with the accumulator and the byte referenced by the HL pair. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, H, N

| $\times 0 R$ | $(I X+d d)$ | (no 8080) |
| :--- | :--- | :--- |
| XOR | $(I Y+d d)$ | nno 8080 |

Perform a logical exclusive OR with the accumulator and the byte referenced by the sum of specified index register and the displacement. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, H, N

```
XOR <XRA r>
```

Perform a logical exclusive OR with the accumulator and register $r$. The result is placed in the accumulator. The XOR A instruction is an efficient way to zero the accumulator, although all the flags are then reset. XOR A is also used to reset the carry flag.

Flags affected: P, S, Z
Flags reset: C, H, N


Perform a logical exclusive OR with the accumulator and the byte $n n$. The result is placed in the accumulator.

Flags affected: P, S, Z
Flags reset: C, H, N

## APPENDIX I

## Abbreviations and Acronyms

| A/D | Analogue to Digital |
| :--- | :--- |
| APL | A Programming Language |
| ASCII | American Standard Code for Information Interchange |
| BCD | Binary-Coded Decimal |
| BDOS | Basic Disk-Operating System (CP/M) |
| BIOS | Basic Input/Output System (CP/M) |
| Bit | BInary digiT |
| BJT | Bipolar Junction Transistor |
| CBIOS | Customized Bios (CP/M) |
| CCD | Charge-Coupled Device |
| CCP | Console Command Processor (CP/M) |
| CMOS | Complementary Metal-Oxide Semiconductor |
| COBOL | COmmon Business-Oriented Language |
| CP/M | Control Program for Microcomputers |
| CPU | Central Processing Unit |
| CRC | Cyclical-Redundancy Check |
| CRT | Cathode Ray Tube |
| CTS | Clear To Send |
| D/A | Digital to Analogue |
| DCD | Data-Carrier Detect |
| DDT | Dynamic Debugging Tool (CP/M) |
| DMA | Direct Memory Access |
| DOS | Disk-Operating System |
| ECL | Emitter-Coupled Logic |
| EOF | End Of File |
| EPROM | Erasable PROM |
| FCB | File Control Block (CP/M) |
| FDOS | Full DOS (CP/M) |
| FET | Field-Effect Transistor |
| FIFO | First-In, First-Out |
| FORTRAN | FORmula TRANslation |
| Hz | Hertz (cycles per second) |
| IC | Integrated Circuit |
| IGFET | Insulated-Gate FET |


| IIL | Integrated Injection Logic |
| :--- | :--- |
| I/O | Input/Output |
| JFET | Junction FET |
| LCD | Liquid Crystal Display |
| LED | Light-Emitting Diode |
| LIFO | Last-In, First-Out |
| LSB | Least-Significant Bit (or Byte) |
| LSI | Large-Scale Integration |
| MHz | Megahertz (million Hz) |
| MODEM | MODulator/DEModulator |
| MOS | Metal-Oxide Semiconductor |
| MOSFET | MOS FET |
| MSB | Most Significant Bit (or Byte) |
| NAND | Not AND |
| NOR | Not OR |
| OP AMP | OPerational AMPlifier |
| PIP | Peripheral Interchange Program (CP/M) |
| PPL | Phase-Locked Loop |
| PROM | Programmable ROM |
| PSW | Program-Status Word |
| R/W | Read/Write |
| RAM | Random-Access Memory |
| ROM | Read-Only Memory |
| RTS | Request To Send |
| SCR | Silicon-Controlled Rectifier |
| SID | Symbolic Instruction Debugger (CP/M) |
| TPA | Transient Program Area (CP/M) |
| TTL | Transistor-Transistor Logic |
| TTY | Teletype |
| UART | Universal Asynchronous Receiver/Transmitter |
| UJT | UniJunction Transistor |
| XOR | Exclusive OR |

## APPENDIX J

## Undocumented Z-80 Instructions

The Z-80 CPU contains two 16-bit index registers called IX and IY. All of the official Zilog instructions which refer to IX and IY are 16-bit operations. For example, the IX register can be assigned the constant value 1234 with the LD instruction

```
LII IX,1234H
```

And the contents of the IY register can be saved on the stack with a PUSH operation.

FUSH IY
A perusal of the numerically ordered Z-80 instructions, given in Appendix F, reveals that sequences beginning with the byte DD hex refer to operations involving the IX register. Similarly, the byte FD hex signifies an IY operation.

In addition to the 16 -bit operations, there are many 8 -bit operations that can be performed with the Z-80 index registers. These instructions are not shown in Appendix F because they have not been officially documented by Zilog. All of these 8 -bit IX and IY instructions follow the same pattern. The first byte of the IX operation codes is DD hex and the first byte of the IY operation codes is FD hex. The remaining byte of the instruction is a regular Z-80 operation which refers to the H or L register. But, in this case, H now refers to the high 8 bits of the index register and $L$ refers to the low 8 bits.

As an example, consider the Z-80 instruction:

```
LII H,B
```

which moves the byte in register $B$ into the $H$ register. If this operation code is preceded by a DD hex byte, then the B register is moved into the high 8 bits of the IX register. An assembler that incorporated these undocumented instructions might generate the following source code.

| 60 | LD | $\mathrm{H}, \mathrm{B}$ | ¢MOVE | B TO | H |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1206 | LD | XH, B | ¢MOVE | B T0 | HIGH IX |
| [106E | LD | XL, E | ¢MOUE | E TO | LOW IX |
| F167 | LII | YH, $A$ | ¢MOUE | A TO | HIGH IY |
| F1169 | LD | YL, C | fMOVE | C TO | LOW IY |

But, except for Allen Ashley's PDS assembler, these XH, XL, YH, and YL symbols have not actually been incorporated into Z-80 assemblers. The undocumented instructions encompass all of the 8-bit LD op codes involving the H and L registers. These include the register-to-register moves

where $r$ is one of the general-purpose registers $A, B, C, D$, and $E$. The instructions

| Lin | $\mathrm{L}, \mathrm{H}$ |
| :--- | :--- |
| LD | and |

are also included. In this case the H and L refer respectively to the high 8 bits and the low 8 bits of the same index register. Thus, the instruction

```
LIIL.H
```

preceded by a DD byte will move the high 8 bits of the IX register into the low 8 bits. The regular H and L registers cannot be operands for these moves. Move-immediate instructions are not included in the new instructions. Furthermore, 8 -bit transfers cannot be made from one index register to the other.

Many of the other 8-bit register operations can be utilized in this way. In addition to the above LD instructions, these include the following.

| ADC | A.H | ALIC | AgL |
| :---: | :---: | :---: | :---: |
| ADID | $\mathrm{A}, \mathrm{H}$ | AnII | Ag L |
| AND | H | ANII | L |
| CF | H | CF | L. |
| IEC | H | DEC | $L$ |
| INC | H | INC | L |
| OR | H | OR | L. |
| SBC | $\mathrm{A}, \mathrm{H}$ | SRC | Ag L |
| SUB | H | SUB | L |
| XOR | H | XOF | L |

The rotations and shifts, the bit manipulations that set, reset and test, and the input and output operations are not included.

All of these undocumented operations can be produced with a regular Z-80 assembler. One method is to generate the initial DD or FD hex with the DEFB directive. Then, the corresponding regular Z-80 instruction follows. For example, the following two lines will generate the instruction needed to move the accumulator into the high half of IX.

```
INEFE ODDH \hat{SET FFOF IX}
LI H.A yMOUE A TO XH
```

Alternately, a macro can be used. The definition could be

| LDX | MACRO | REG1, REG2 |
| :--- | :--- | :--- |
|  | DEFB | ODDH |
|  | LD | REG1,REG2 |
|  | ENDM |  |

Then the macro call
LIIX H,A
will generate the desired code.

## Index

Accumulator, 3
Acoustical coupler, 65
Acronyms, 311
Active high, 93
Analog-to-digital, 188
Arithmetic shift, 76, 155, 180, 307
ASCII, 20, 66, 150
character set, 253
Assembler, 2, 86
Autostart tape, 201
Base conversion, 150
BCD, 19, 168
Binary, 17
Binary coded decimal, 19, 168
BIOS (CP/M), 91, 216
Block move, 13, 111, 297
Branch table, 107
Buffered input, 55
Bus, 1
Carry flag, 5, 10
Checksum, 68, 188
Clock routine, 241
Code, operation, 1
Cold start, 103
Compare 7, 123
Complement, 21
Concatination, 72
Conditional branch, 12, 287, 293
Control character, 93, 99, 100
Conversion, number base, 150
CP/M, 51, 86, 91, 123, 175, 201, 214
CPU, 1
Crazy octal, 164,182
Cross reference
8080 to Z-80, 280
Z-80 to 8080, 283
DAA, 179
Data port, 49
Data ready, 91
Debugger, 94
Decimal adjust accumulator, 179
Decrement, 8, 10

Delay, after carriage return, 148
Delimiter, 151
De Morgan's theorem, 28
Digital-to-analog, 188
Directive, 87
DOS, 214
Double precision arithmetic, 22,180
Double register, 3, 10, 13
Doubling, 15, 155, 307
Dummy variable, 70
Dump, memory, 95
Echo, 95
Editor, 86, 143
Exclusive OR, 26
FCB (CP/M), 226, 242
File control block, 226, 242
Filename, 204
Fixed entry, 152
Flags, 3, 6, 10
I/O, 50, 71, 93
Free entry, 152
Full duplex, 65
Function number (CP/M), 216
Gates, 21
GO program, 226
Halving, 15
Handshake, 49
Hex arithmetic, 119
Hex format, 201
Hexadecimal numbers, 17
High-level language, 2, 214
Increment, 8, 10
Index register, 313
Input, 14, 48, 117, 146
Instruction set
alphabetic, 8080, 258
alphabetic, Z-80, 264
numeric, 8080, 261
numeric, Z-80, 272
details, 283

Intel hex format, 201
Interrupt-driven keyboard, 55
Interrupt register, 11
Interrupts, 52
IOBYTE (CP/M), 217, 220
Jump, relative, 12, 144
Label, 2
local, 82
Labels, readable, 203
Leading-zero suppression, 173
LIFO stack, 30
List routine, 229
Loader routine, 125
Logical AND, 23, 224
Logical devices, 215
Logical exclusive OR, 26
Logical operations, 7, 20
Logical OR, 23
Logical shift, 15
Looping, 50
Macros, 69, 143
Magnetic tape, 187
Masking AND, $25,50,178,220$
Memory allocation (CP/M), 217
Memory
map, 255
pointer, 2, 55, 113
test, 120
Memory-mapped port, 48
Mnemonic, 2
Modem, 64
Monitor, 85, 128
Movement of data, 111
Multiplication, 15, 157
NAND gate, 26
Nibble, 178
NOR gate, 26
Nulls, carriage return, $77,93,219$
Number-base conversion, 150
Object program, 2
Octal, 16, 163, 180
Offset, 202
One's complement, 21
Opcode, 1
Operand, 2
Operation code, 1
Output, 14, 48, 71, 117, 146, 215
Packed BCD, 19, 168
Page, memory, 105
Paper tape, 187
Parallel port, 49
Parity, 66
Passing data, 37, 39
Peripheral, 1, 14
port, 48, 117, 146
Physical devices, 218
PIP (CP/M), 143, 230
Pointer, $2,12,55$

Polling, 52
POP, 31
Port, I/O, 48, 117, 146
initialization, 146
Printer routine, 147
Program counter, 3, 11, 36
Program status word, 3,34
PSW, 3, 34
PUSH, 31
Register
flag, 3
memory, 5
refresh, 11
saving, 33
status, 2
Register pair, 3
Registers
8080, 3
Z-80, 11
Relative jump, 12, 144
Resetting a bit, 25
Rotation, 9
RST instruction, 53
Scroll, 64, 99
Searching, 113, 115
Serial port, 49
Setting a bit, 24
Shift, 14, 76, 155, 307
Signed number, 6, 15
Source program, 2, 214
Split octal, 164, 182
Spooling, 52
Stack, 30
automatic placement, 45
saving registers on, 33
setting up new, 40
storing data on, 31
Stack pointer, 31, 109
STAT (CP/M), 225
Status port, 49
String, 150
Subroutine call, 35, 287
Subtraction, 22, 177
Table, command branch, 107
Tape recording, 187
Tape, test, 212
Telephone modem, 64
Top-down method, 85
Truth table, 21
Two's complement, 21, 74, 75, 177, 201
Unconditional branch, 12
Undocumented Z-80 instructions, 313
Unsigned number, 6
Vectors, 103, 219
Vectored interrupt, 53
Warm start, 103
Z-80 instruction macros, 73
Z-80 registers, 11

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