ZENITH data systems

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DESKTOP COMPUTER SYSTEMS

Z-217-1 TECHNICAL MANUAL

Winchester Disk Drive Controller

Technical Manual
Z-100 Series Computers

595-3014-01

Z-217-1

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Zenith Data Systems Corporation
Saint Joseph, Michigan 49085

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Contents

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Introduction

The Z-217-1 Disk Drive Controller is a two-board pair which will allow owners of the Z-100 series computers to add and control up to two rigid 5-1/4-inch Winchester drives.

One of the two boards, the Data Separator, resides on the rigid Winchester drive. The second board, the controller, is located in any of the vacant S-100 connectors in the computer's card cage. A single, 34-conductor cable connects the two boards together. Another 34-conductor cable connects the main board to the disk drives (daisy chain). In addition, two other cables are used for data transmission to and from the Winchester drives. One cable is used per drive.

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Specifications

Drives Supported	Two Winchester disk drives, each up to 65 MB.
Drive Interface	Seagate™ standard interface.
Interface to Host	Via S-100 bus, with exception that +5V is not taken from the bus, but, rather furnished from an external source. Otherwise, compatible with IEEE standard 696.
Sector Size	Two sector sizes, 512 or 1024 bytes, with programmable interleave.
Buffering	Buffers all transfers to and from host via on-board multiple-sector buffer.
Data Transfers	All transfers made via TMA with programmable mode of transfer — burst or byte. Data transfer can be halted by host using PAUSE command. CONTINUE command resumes the transfer.
I/O Ports	Controller uses two I/O ports. Port address is set by PAL and is not user selectable.
Error Detection	Detects and corrects (if enabled) data errors. Reports logical errors. Reports drive errors and also issues a HOME command if the drive was not previously accessed.
Power Requirements	+5 volts, 2.5 amps maximum (controller board). +5 volts, 1.0 amps maximum (data separator). −5 volts or −12 to −16 volts (jumper selectable) 100 milliamps maximum (data separator).

The Zenith Data Systems Corporation reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

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Switch and Jumper Settings

Pictorial 1 illustrates the mother board of your Desktop Computer and the location of DIP switch S101 in particular. The illustration shows you the proper settings for autoboot upon power-up from the Winchester drive. Refer to your *Z-100 Series User's Manual*, Appendix I for more information regarding this switch and its settings.

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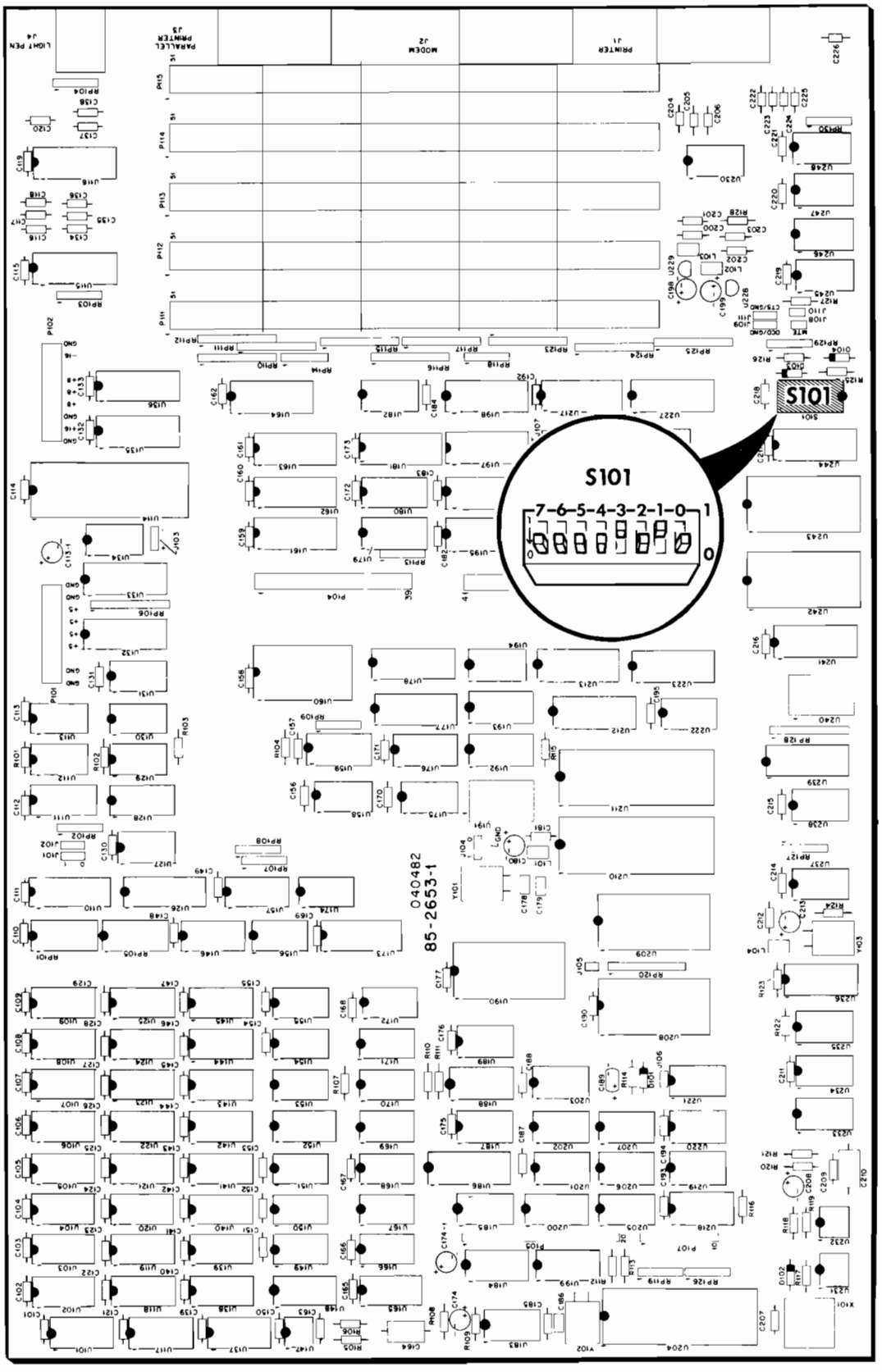
Switch and Jumper Settings



PICTORIAL 1

Z-100 Mother Board

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Switch and Jumper Settings

Controller Board Jumpers and Switches (Pictorial 2)

The following information applies to the jumpers and switches on your Z-217-1 Controller and Data Separator circuit boards. Each jumper position is described and the "standard" position for normal operation in a Z-100 Desktop Computer is identified. Refer to Pictorials 2 and 3 for the locations of each jumper and switch.

PROM — 2K position—for 2K ROM's.
1K position—for 1K ROM's (position for normal Z-100 operation).

FORMAT ENABLE — Jumper installed—Format enabled.
Jumper not installed—Format protected (position for normal Z-100 operation)

EXTENDED PORT ADDRESS (2 jumpers) — Left position—16-bit port addressing. Right position—8-bit port addressing (position for normal Z-100 operation).

VI* — Vector interrupt level—No jumpers installed (position for normal Z-100 operation). **NOTE:** You may find a jumper installed between pins 3 & 4 of the top row of jumpers. This is the storage location for the Format Enable jumper. Refer to Appendix B of your *Z-100 User's Manual Winchester Supplement.*

AP* — Arbitration Priority DIP Switches

Position no. 8 4 2 1
0 0 0 0—lowest priority (0)
1 0 0 0—middle priority (8) (setting used for normal Z-100 operation).
1 1 1 1—highest priority (15)

NOTE: Position 0 indicates a closed switch, position 1 indicates an open switch. Disregard the numbers on the switch. The numbers printed on the P.C. board are the switch weights.

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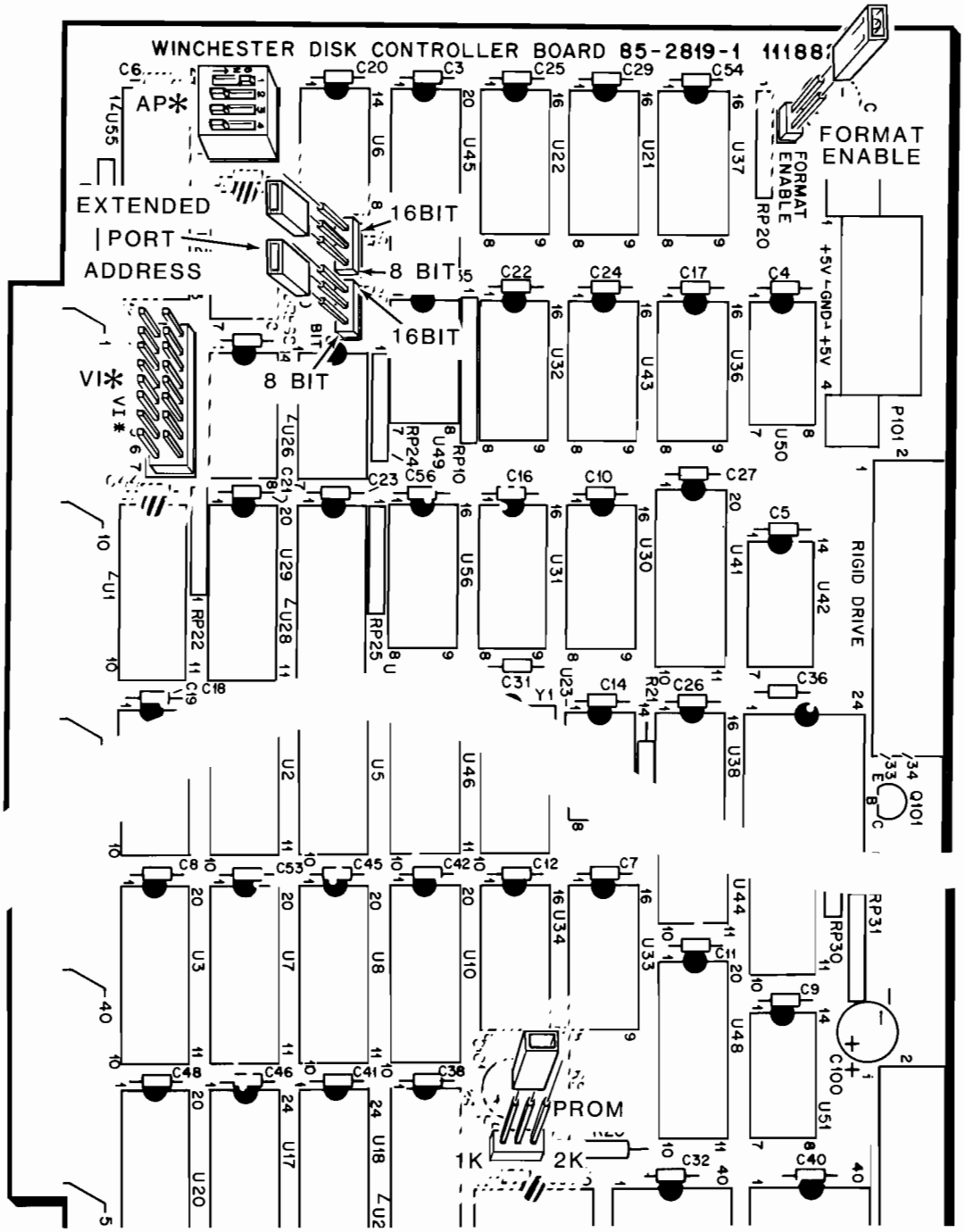
Switch and Jumper Settings



PICTORIAL 2

Controller Board Jumpers and Switches

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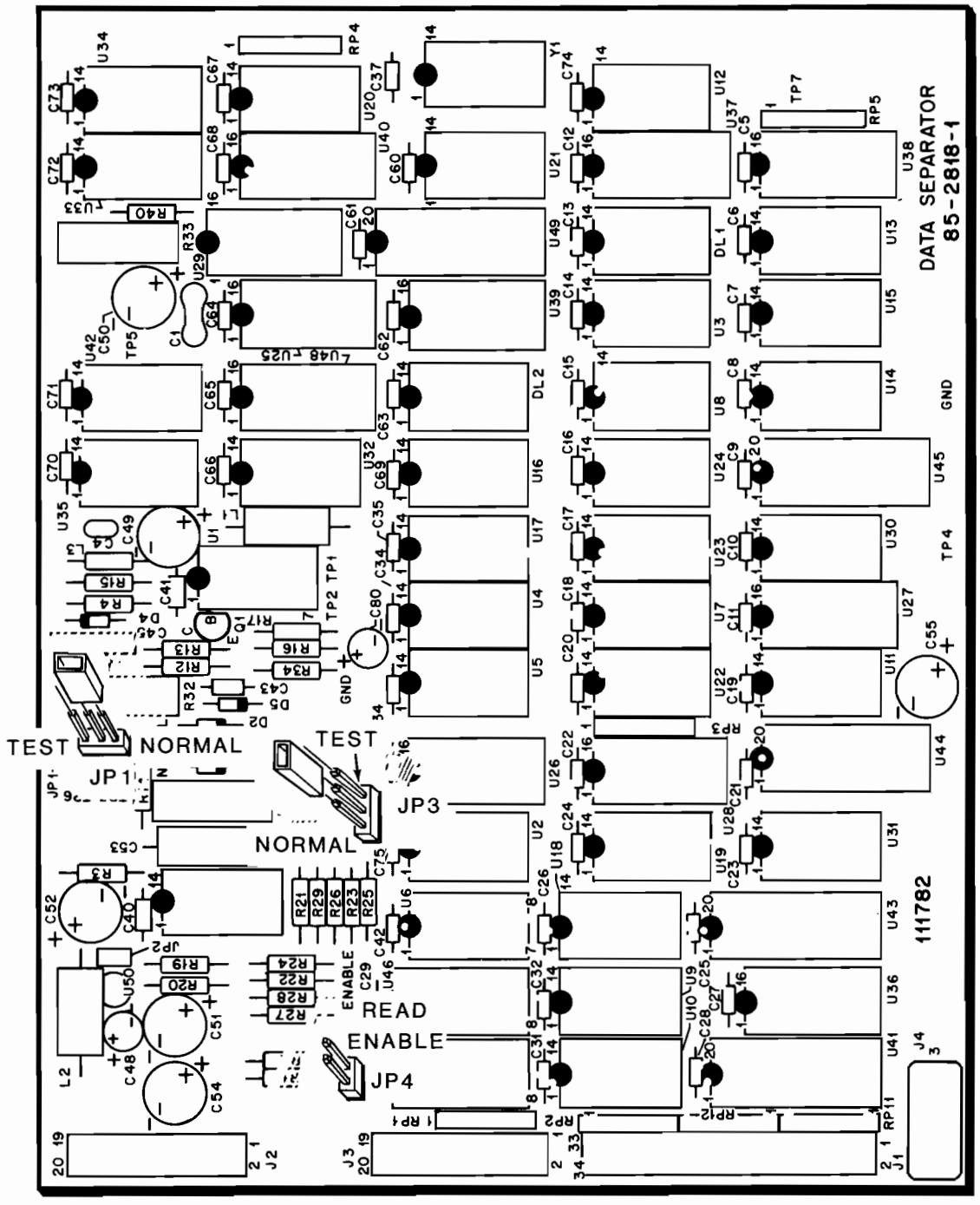
Switch and Jumper Settings



PICTORIAL 3

Data Separator Board Jumpers

Data Separator Board Jumpers (Pictorial 3)

JP1 Test—Calibration position for VCO.
Normal—Phase lock enabled (position for normal Z-100 operation).

JP3 Test—Calibration position for sending 625KHz to the 9602.
Normal—Routes READ data to the 9602 (position for normal Z-100 operation).

JP4 Read Enable—Jumper installed asserts READ gate (used for calibration)
Jumper not installed—normal read/write operation (position for normal Z-100 operation).

System Operation

Since your system has been changed by the introduction of the Z- 217 Winchester system, you will need a Winchester-compatible version of your operating system(s). Refer to your operating system manual(s) and the *Z-100 User's Manual Winchester Supplement* for additional setup and operating information.

Software Access

The following will provide you with information regarding Winchester disk software operations.

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Software Access

IEEE 696 (S-100) Interface

Slave Interface—The Z-217 uses two I/O (Input/Output) ports. The upper eight addresses are optionally used to decode the port address and must be at a logical "0" to access this board. The option can be disabled by moving the Extended Port Address jumpers to the 8-bit position.

The lower eight address lines are decoded for port addressing by a PAL. Eight vectored interrupts are used, any one of which can be addressed and used by the controller by moving the VI* jumper.

Master Interface—TMA (Temporary Master Access, previously referred to as DMA—direct memory access), performed by the Z-217, conforms to all IEEE-696 (S-100 bus) requirements. One wait state is automatically added during read cycles to allow it to work in the Z-100. The arbitration level (all sixteen priority levels are available) for the TMA is selected by the four AP* DIP switches. Twenty-four bit addresses are used for TMA across 64K memory boundaries.

Interrupt Handling—When INT* is asserted in the burst mode, the Z-217 is taken off the bus. Your interrupt service routine should check for a TMA in progress. If a TMA is in progress, you should first halt the TMA by sending a PAUSE command to the Z-217 before acknowledging the interrupt and servicing it. Once the interrupt has been serviced, your interrupt service routine should send a CONT command to the Z-217 so the TMA may be resumed.

In the byte mode, the PAUSE and CONT commands are still executed by the Z-217, but they are not needed unless software timing loops are being used or critical real-time processing is being performed. Also, the Z-217 will not arbitrate for the bus when INT* is asserted in the byte mode.

Command Philosophy

There are two levels of commands associated with the Z-217 controller.

First level commands are direct commands that are written directly into the controller's command register and executed immediately. They are used to call second level commands.

Second level commands are used for the primary communication mode between the controller and the operating system. They are placed in a memory buffer until fetched by the controller executing a first level (direct) command. The controller uses a TMA to transfer commands into its internal command buffer. Once a command has been completed, an interrupt is generated to notify the host processor and status is returned to the memory buffer via TMA.

Data Transfers

All data transfers take place via TMA; programmed input-output is not allowed. A 2K $\times$ 8 buffer on the controller board handles entire sectors of data at a time. When transferring from the disk to memory, the buffer is used to correct any errors detected by the ECC (Error Correction Code) before the data is transferred to system memory. When writing to the disk, the buffer is used to make an entire sector of data available for the disk.

The system can handle a minimum interleave of three to one.

Direct Access Registers

The Z-217 controller occupies two I/O ports (command and reset) in the system.

Writing to the command port places commands in the controller's command register. Reading this port yields the controller's hardware status.

Writing to the reset port causes the controller to execute a hardware reset. Reading this port is used for interrupt acknowledge and resets the interrupt latch and causes the status to be read.

Direct Mode Commands (First Level)

The controller responds to the following direct mode commands:

08	SETUP	Uses the following three bytes to specify the TMA address for commands (MSB is first, least significant last). You **must** use this command before the first EXECUTE command is sent to the controller.
10	EXECUTE	Causes the controller to fetch a command from the memory buffer.
18	PAUSE	Halts any TMA in progress until a CONT command is received.
20	CONT	Restarts any TMA that was stopped by a PAUSE command.

Control Block Commands (Second Level)

The controller responds to the following commands when they are the first byte in the control block of system memory.

Type 0

00	RECAL	Causes the selected drive to step outward one cylinder at a time until cylinder zero is reached. No data is transferred.
01	STATUS	Returns the status for the selected drive to the TMA address. The format of the status is shown on Page 21.

Type 1

10	WRITE	Writes the specified number of sectors (up to 256) from the TMA address to the specified drive. Error Correction Code is generated and written to the disk at this time also.
11	READ	Reads the specified number of sectors (up to 256) from the specified drive to the TMA address. Any errors detected by the ECC are corrected (if enabled).
13	SEEK	Positions the heads of the specified drive to the specified logical address.

Type 2

20	FORMAT	Formats the specified drive.
21	FORMAT TRACK	Formats only the specified track.
22	SET DRIVE	Sets drive parameters.

Type 3

30	WRITE ABS	Writes one sector using absolute addressing.
31	READ ABS	Reads one sector using absolute addressing.
33	SEEK ABS	Positions the heads of the specified drive to the specified cylinder.

Format of Commands

Type 0 and Type 1

	Byte	Bit 7 6 5 4 3 2 1 0	
	1	Command OP Code	
	2	Drive Select	MSB—Logical Sector No.
C	3	MB—Logical Sector No.	
O	4	LSB—Logical Sector No.	
M	5	Sector Count	
M	6	MSB—Data TMA Address	
A	7	MB—Data TMA Address	
N	8	LSB—Data TMA Address	
D	9	MSB—Next Command Address	
	10	MB—Next Command Address	
	11	LSB—Next Command Address	
	12	Flags	
	13	Error Code	
S	14	Drive Select	MSB—Logical Sector # of Error
T A T U S	15	MB—Logical Sector # of Error	
	16	LSB—Logical Sector # of Error	

MSB—Most Significant Byte; MB—Middle Byte; LSB—Least Significant Byte

Flag byte: Bit # If set

- 7 Interrupts enabled
- 6 Use burst mode TMA
- 5 Ignore PAUSE and CONT commands
- 4
- 3
- 2 Disable retries
- 1 Disable ECC
- 0 Chain next command immediately

NOTE: Only Type 0, 1, and 3 commands can be chained. Bytes 9, 10, and 11 are the starting address of the next command block to be executed. These three bytes must be valid or a new setup command must be issued before the next execute command. Also, this address must be valid if the chain flag (bit 0) is set.

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Software Access

Type 2

	Byte	Bit 7	6	5	4	3	2	1	0
	1	Command OP Code							
	2	Drive Select			N/A			Max Head No.	
C	3	Max Cylinder Number (MSB)							
O	4	Max Cylinder Number (LSB)							
M	5	Reduced Write Current (MSB)							
M	6	Reduced Write Current (LSB)							
A	7	Precomp Cylinder (MSB)							
N	8	Precomp Cylinder (LSB)							
D	9	Step Rate (LSB ± 20 μS)							
	10	ECC Span							
	11	N/A	*	N/A	Interleave Factor				
	12	Fill Character							
	13	Error Code							
S	14	Head # of Error				Sector # of Error			
T A T U S	15	Cylinder # of Error (MSB)							
	16	Cylinder # of Error (LSB)							

*Cell Size: 0 = 512 bytes/logical sector
1 = 1024 bytes/logical sector

MSB—Most Significant Byte; LSB—Least Significant Byte

Type 3

	Byte	Bit 7	6	5	4	3	2	1	0
	1	Command OP Code							
	2	Drive Select			N/A		Head Select		
C	3	Cylinder Number (MSB)							
O	4	Cylinder Number (LSB)							
M	5	N/A			Sector Number				
M	6	Data TMA Address (MSB)							
A	7	Data TMA Address (MB)							
N	8	Data TMA Address (LSB)							
D	9	Next Command Address (MSB)							
	10	Next Command Address (MB)							
	11	Next Command Address (LSB)							
	12	*	Flags						
	13	Error Code							
S	14	Head # of Error			Sector # of Error				
T A T U S	15	Cylinder # of Error (MSB)							
	16	Cylinder # of Error (LSB)							

* 0 = Disable Interrupts
  1 = Enable Interrupts

MSB—Most Significant Byte; MB—Middle Byte; LSB—Least Significant Byte

Format of Status Register

BIT	
7	Interrupt
6	Busy
5	Burst Mode
4	TMA in Progress
3	Error
2	Immediate Mode Error
1	Paused
0	Done

Format of Status Returned by 01 Command

Byte	Bit 7	6	5	4	3	2	1	0
1	Reserved				B3	B2	B1	B0
2	Maximum Cylinder No. (MSB)							
3	Maixmum Cylinder No. (LSB)							
4	Reduced Write Current Cylinder Number (MSB)							
5	Reduced Write Current Cylinder Number (LSB)							
6	Precomp Cylinder No. (MSB)							
7	Precomp Cylinder No. (LSB)							
8	Current Cylinder No. (MSB)							
9	Current Cylinder No. (LSB)							
10	Step Rate							
11	Span							
12	Interleave Factor							
13	Cell Size							
14	Maximum Head #							
15	Fill Character							
16	Reserved							

B0 = Drive Ready
B1 = Accessed
B2 = Seek Complete
B3 = Track 0

Step Rate = Value times 20 μS.

Cell Size 1 = 512 bytes/sector
2 = 1024 bytes/sector

Fill Character = The character used during format to fill the data fields.

MSB—Most Significant Byte; MB—Middle Byte; LSB—Least Significant Byte

NOTE: Bytes 8 and 9 will not be recognized unless Bit 1 of Byte 1 (B1) is set.

Error Codes

Type 0

00 No error
01 Drive not ready
02 No seek complete
03 No Track 0
04 No Index
05 No Drive Selected

Type 1

10 Header Address Mark not found
11 Seek error (bad cylinder number in header)
12 Sector number not found
13 ECC error in header
14 Data Address Mark not found
15 Non-correctable ECC error in data field
16 Correctable ECC error in data field
17 Write fault

Type 2

20 Illegal op code
21 Illegal disk address
22 Format protected
23 Write protected

Type 3

30 Miscellaneous error

Type 4

40 Error during diagnostic

Software Access Examples

The following information and examples present methods for accessing the Z-217-1 Winchester Controller and Disk Drive from assembly language routines. These examples assume that there is no BIOS support and the access of the Z-217-1 will not affect the BIOS.

The first step is to set up the controller with the memory location of its command buffer. This is the SETUP command discussed earlier.

NOTE: The Z217WCB in the following code is the Winchester Control Block that is described in a previous section of this manual.

```
PORT217         EQU     0AEH                    ; Z-217 port address
WICSETUP        EQU     08H                     ; SETUP command
WISBUSY         EQU     01000000B               ; Busy status bit
WISDONE         EQU     00000001B               ; Done status bit

        MOV     DX,PORT217                      ; Base port of 217
        MOV     AL,WICSETUP
        OUT     DX,AL                           ; Do a SETUP command
        MOV     CX,-1                           ; Loop count for BUSY
START1:
        IN      AL,DX                           ; Read status
        TEST    AL,WISBUSY                      ; Is he busy?
        JNZ     START2                          ; Yes, continue
        LOOP    START1

;       Timed out, no busy signal from z217

        MOV     DX,OFFSET NOZ217                ; Point to error message
        JMP     NEAR PTR ABORT                  ; Print error and exit

;       Found the controller, execute the remainder of the command

START2:
        MOV     BX,CS                           ; BX = segment
        XOR     CX,CX                           ; CX = zero

;       Make a 20 bit address

        SHL     BX,1                            ; Shifted 1 bit
        RCL     CX,1
        SHL     BX,1                            ; Shifted 2 bits
        RCL     CX,1
        SHL     BX,1                            ; Shifted 3 bits
        RCL     CX,1
        SHL     BX,1                            ; and shifted 4 bits
        RCL     CX,1
        ADD     BX,OFFSET Z217WCB               ; Add offset of 217 block
        ADC     CX,0                            ; Propagate carry
```

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Software Access Examples

```
;       20 bit address in CL:BX

        MOV     AL,CL                           ; AL = MSB
        OUT     DX,AL                           ; Send it to controller
        MOV     AL,BH
        OUT     DX,AL                           ; Next one
        MOV     AL,BL
        OUT     DX,AL                           ; And the last one
```

At this point, the Z-217-1 is ready to accept commands from the command buffer. The following code will tell the Z-217-1 which type of drive is installed in the system:

```
;       SI = address of drive type specifier

        MOV     SI,OFFSET TUSER
        CLD
        MOV     DI,OFFSET Z217WCB
        MOV     CX,12
        REP     MOVSB                           ; Move it in here too

;       Now execute the Set Drive Parameters command

        CALL    EXCCMD                          ; Execute the command
        OR      AL,AL                           ; AL = returned status

;       'ZR' flag clear if error executing command
```

The following routine executes the command in the command buffer. It then waits for the controller to inform it that the command has been executed.

```
EXCCMD:
        MOV     AL,BYTE PTR UNIT
        OR      BYTE PTR Z217WCB+1,AL           ; Determine unit number
        MOV     BYTE PTR Z217WCB+WI3ERR,-1      ; Indicate command not done
        MOV     DX,PORT217                      ; DX = command port
        MOV     AL,10H                          ; Exec command
        OUT     DX,AL                           ; Execute it
EXCCMD1:
        CMP     BYTE PTR Z217WCB+WI3ERR,-1      ; Done yet?
        JZ      EXCCMD1                         ; No, keep waiting
        MOV     AL,BYTE PTR Z217WCB+WI3ERR      ; AL = error code
        RET
```

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Software Access Examples

The following routines are simple sector read and write routines. Note that the only difference between read and write is the first byte in the command buffer: 11H for read, 10H for write.

```
;**     RDSEC - Read a sector
;
;       DX = ADDRESS OF DATA
;       CX = STARTING SECTOR NUMBER
;       BX = SECTOR COUNT
;
;       NOTE: 'CY' set if error (as opposed to WRTSEC issueing messages
;

RDSEC:
        MOV     BYTE PTR Z217WCB,11H            ; Set a READ command
        CALL    WRTSEC0                         ; do the I/O
        JNZ     RDSEC1                          ; If error
        RET                                     ; No errors
RDSEC1:
        STC                                     ; Error , set carry
        RET

;**     WRTSEC - Write a sector
;
;       DX = ADDRESS OF DATA
;       CX = STARTING SECTOR NUMBER
;       BX = SECTOR COUNT
;

WRTSEC:
        MOV     BYTE PTR Z217WCB,10H            ; Set a WRITE command
        CALL    WRTSEC0                         ; do the I/O
        JNZ     WRTSEC1                         ; If error
        RET                                     ; No errors
WRTSEC1:
        STC                                     ; Error, Set carry
        RET


;*     WRTSEC0 - Do read/write, no error detection
;

WRTSEC0:
        MOV     SI,OFFSET Z217WCB               ; SI points to command
        MOV     BYTE PTR [SI+1],0               ; Set drive/sector hi = 0
        XCHG    CH,CL                           ; Flip sector number
        MOV     WORD PTR [SI+2],CX              ; Sector number
        MOV     BYTE PTR [SI+4],BL              ; Sector count
        XOR     CX,CX
        MOV     BX,DX                           ; BX = address
        MOV     DX,CS
        SHL     DX,1                            ; Shift 1 bit
        RCL     CX,1
        SHL     DX,1                            ; Shift 2 bits
        RCL     CX,1
        SHL     DX,1                            ; Shift 3 bits
        RCL     CX,1
        SHL     DX,1                            ; Shift 4 bits
        RCL     CX,1
```

```
ADD     DX,BX                           ; DX:CX = 20 bit address
ADC     CX,0
MOV     BYTE PTR [SI+5],CL
MOV     BYTE PTR [SI+6],DH
MOV     BYTE PTR [SI+7],DL
MOV     BYTE PTR [SI+11],0              ; Zero the flags
CALL    NEAR PTR EXCCMD                 ; Do it
OR      AL,AL                           ; Status
RET
```

The following example is a table that can be used to set up for a ST-506 drive. In this example, WC is the reduced write-current cylinder number and PC is the precompensation starting cylinder number.

```
TUSER    DB     022H                    ; Setup command
TUSERMH  DB     0                       ; Max head number
TUSERMC  DB     1                       ; Max cyl hi
         DB     31H                     ; Max cyl lo
TUSERWC  DB     2                       ; Max wc hi
         DB     0                       ; Max wc lo
TUSERPC  DB     2                       ; Max pc hi
         DB     0                       ; Max pc lo
TUSERSR  DB     5                       ; Step rate
TUSERSM  DB     7FH                     ; ECC burst span mask
         DB     4                       ; Interleave
         DB     0E5H                    ; Fill character
```

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Theory of Operation

Refer to the block diagrams, Pictorials 4 and 5, and the schematic for the following discussion.

The Z-217 Disk Controller is a bit-slice processor-based Z-100 bus controller (Z-100 is defined as the bus used in the Z-100 system). It is used to access one or two 5-1/4-inch Winchester disks. The Z-217 Controller is made up of two boards, a controller board that resides in the Z-100 bus and a data separator board that is mounted on the drive.

The controller board contains the bit-slice processor and all the interface circuitry to connect it to the drive, the Z-100 and the data separator. Commands are issued by the host, received and interpreted by the controller board. The controller then issues control signals to the drive and data separator to perform the desired function. Command information and data are transferred to and from the controller by TMA (Temporary Master Access). The data separator board connects to the controller board and also to the data cable on the drive. Its function during a read is to take the serial MFM data coming off the drive and convert it to 8-bit parallel data; the write operation is just the opposite.

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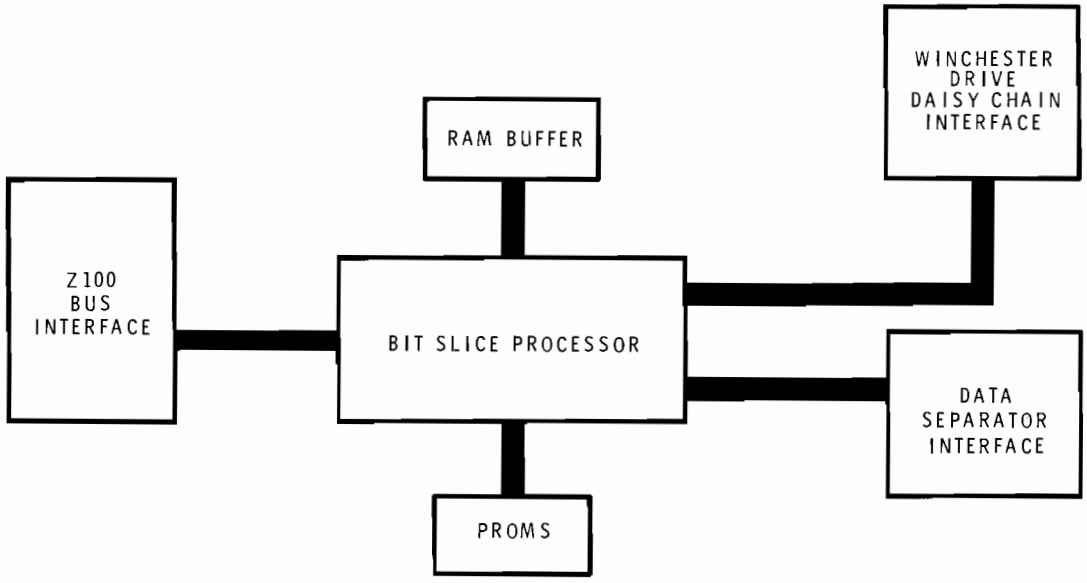
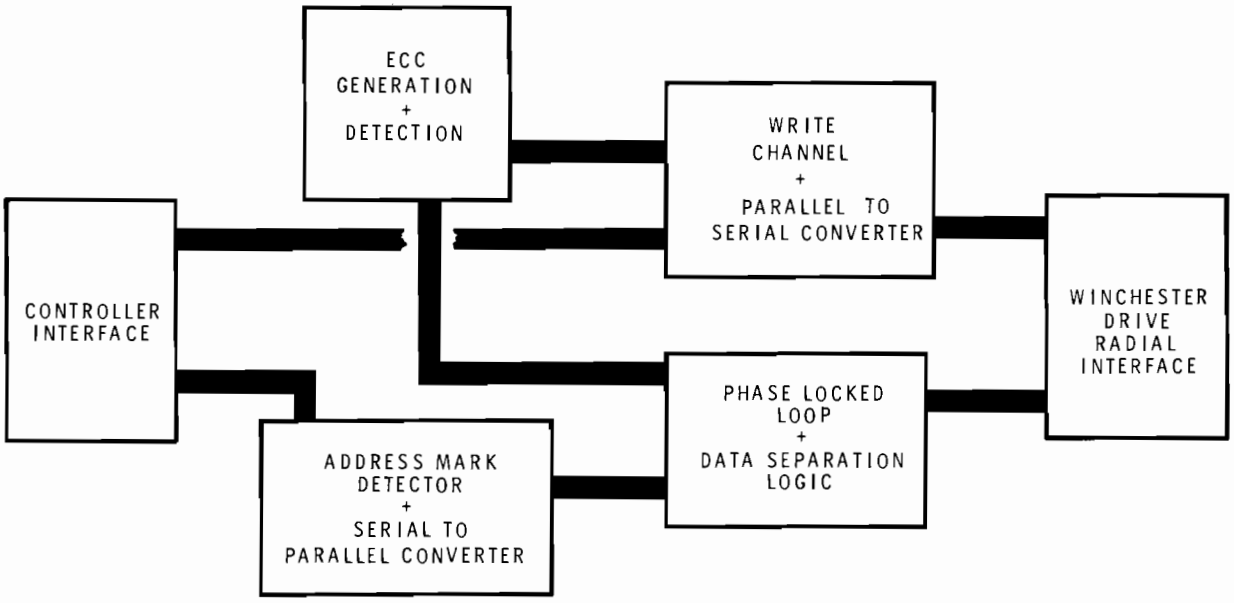
Theory of Operation



PICTORIAL 4

Z-217-1 Controller Board Block Diagram



PICTORIAL 5

Z-217-1 Data Separator Block Diagram

Circuit Description

The Controller Board

The Z-100 Bus Interface

The bus interface consists of all the devices that connect to the Z-100 bus. U1, U2, and U5 are the address latches used during a TMA to hold the address on the Z-100 bus. U4 and U7, the data latches, are used during a TMA transfer to hold the data on the bus. U4 is used during a memory write, and U7 is used during a memory read. All of these registers are connected to a common internal 8-bit data bus. Information loaded into these registers, except the data in register U7, is controlled by the bit-slice processor. U7 is clocked by the TMA circuit.

U46, a PAL, is used with U80 to decode the port address of the host. When J31 and J32 are set so $\overline{AD1}$ and $\overline{AD2}$ are pulled up, the board will respond to an 8-bit port address. When J31 and J32 are connected to pins 6 and 5 of U80, the board will respond to a 16-bit port address.

The board occupies two ports, AE hex and AF hex in the 8-bit mode, and 00AE hex and 00AF hex in the 16-bit mode. These ports are fixed by the PAL. The PAL must be reprogrammed to change the port address. The port AE hex is used to send direct mode commands and to read the status of the Controller. When the host executes an "out" to port AE hex, the PAL will issue a clock pulse from pin 16 that latches the value on the Z-100 data bus into U3, the Command Register. This pulse will also clock U26 (pin 3), setting the Q output high (pin 5). The second half of U26 is used to synchronize this output to the internal clock.

When the host executes an "in" from port AE hex, the PAL (U46) will issue a pulse (from pin 17) to U8 to enable its data onto the Z-100 bus. Information about the PAL and its programming are in the Semiconductor Information section of this Manual. U8 is the status register that can be used by the host to monitor the status of the controller. Data is written to the status register by the bit-slice processor from the internal bus. U23 is also clocked when the status register is loaded. If the high order bit of status is a one, U23 will be set and the Q output (pin 9) will go high. A low from U50 (pin 2) will then be driven onto one of the vectored interrupt lines of the Z-100 bus. The host may also execute an "in" from port AF hex to read the status. The same signal will result from pin 17 but $\overline{\text{IACK}}$ will also be activated, which will cause U23 to be cleared. This results in an interrupt acknowledge.

When the host executes an "out" to port AF hex, a hardware reset will result. $\overline{\text{PRIN}}$ (U46 pin 14) will be pulled low causing $\overline{\text{RESET}}$ (U24 pin 22) to go low. $\overline{\text{RESET}}$ can also result from the reset line on the Z-100 bus going low. All latches will return to a known state and the bit-slice processor will run through a reset program.

Internal Clock

The internal clock of the controller runs at 6 MHz. It is generated by Y1, a 12 MHz oscillator, then divided by two by U23. A two-phase 6 MHz clock is then available at U23 pins 5 and 6. Three gates of U47 are tied in series to provide a 6 nanosecond skew (typically). The bit-slice processor will run off the skewed clock.

The Program Control Unit

The program control section is the heart of the bit-slice processor. It includes the PROM's (U14-U19) which contain the program, an AMD2910 (U11) that controls program execution, and the condition code multiplexer (U21, U22, and U32) used for conditional program operations.

The PROM's used in the Z-217 are very fast "registered" bipolar PROM's. The register built into the PROM acts as a pipe line register, allowing the address to be changed while holding the data stable. The PROM's have an access time of about 15 to 20-nanoseconds.

Addresses to the PROM's are generated by the sequencer (U11). The sequencer will allow the program to advance, jump, and execute subroutine calls. This chip also has a built-in 12-bit loop counter. U11 is also connected to the internal data bus, allowing constants to enter from the PROM's through U10. These constants can either be used as jump addresses or loaded into the counter. The instruction lines to the sequencer come directly from the PROM outputs (data bits 33–36). J11 is a jumper to allow for future expansion of the PROM size from 1K to 2K.

U32, U21, and U22 form a 16-to-1 multiplexer. The output at U32 (pin 5) is the true or inverted value of the selected input. The input is selected by the micro code data bits 28–31. The output is true or inverted depending on the state of data bit 32 (high is inverted). The output of this condition code multiplexer is fed into U11 pin 14. The purpose of the condition codes are to allow conditional jumps and subroutine calls and returns. The inputs to this multiplexer are from various drive, data separator, and ALU status lines. J12 is also connected to an input of the multiplexer and serves as the format protect for the disk drives. If the jumper is not installed, the controller will not format a drive.

Arithmetic Logic Unit

The ALU section of the Controller uses two AMD2901 4-bit slices to form an 8-bit ALU. (U12 handles the four low-order bits, and U13 handles the four high-order bits.) U30 is a 6-bit latch used to latch status lines from the ALU slices. U30's clock is generated by data bit 8 of the micro code and the non-skewed clock through U24. This allows the status of the ALU's to be latched only when data bit 8 is set. The ALU chips contain 16 internal registers and are addressed by data bits 14–17 and 21–24. The internal bus is also connected to the input of the ALU's. This allows the logical operation to be performed by several different sources, internal registers or constants from internal bus or zero. U31 is a dual 4-to-1 multiplexer. It allows the ALU's to rotate and shift in several different modes: shift in a zero or one in both directions, shift in a previously latched carry in both directions, or rotate in both directions. These modes are controlled by data bits 9 and 10 of the micro code, and the direction is controlled by the instruction given to the ALU from data bits 11–13, 18–20, and 25–27.

Internal Bus Control

The sections of the controller board are tied together by a common 8-bit bus. The section U33 through U35 controls which element of the controller can drive the bus and which element on the bus receives the data. U35 is a 3-to-1 decoder. Its inputs are data bits 4–6, and control what output will go low. The outputs of U35 will go low and remain low for one clock cycle. These outputs will drive the output enables for the driving elements on the bus. U33 and U34 combine to make a 4-to-1 decoder. Its inputs come from data bits 0–3. They also control which output will go low. These outputs do not go low until the second half of the clock cycle, and remain low for only that half of the cycle. These outputs are used as clocks to latch the data off the bus.

Internal RAM Buffer

The data read from or written to the disk is stored in a 2K by 8-bit RAM. This RAM is addressed by U36–38. These are parallel loading 4-bit counters. The desired address is placed in the counters by the processor through the internal bus. The address can then be incremented by placing a 1 in data bit 7. This signal is combined with non-skewed clock by U47 (pin 7–9), and the output is then fed to the counters. U40 is a bidirectional 8-bit buffer so the RAM data can be put on the bus and vice versa.

Drive and Data Separator Interface

U41 and U43 are latches used to hold the levels of control lines going to the disk drive. These lines are buffered with open-collector buffers. The write gate going to the drive is driven by a special circuit. This line can not be pulled low during power up until the supply level gets above 4 volts (approx.). Also on power down, the line can not be driven if the voltage falls below 4 volts.

U44 is a bidirectional buffer used to pass data to and from the data separator. U48 is another latch to hold levels of control lines going to the data separator and to the TMAC (Temporary Master Access Control).

U45 synchronizes the asychronous signals from the data separator, the drive, and the TMAC to the internal clock. These signals are then fed to the condition code multiplexer. All signals coming from the drive and the data separator have receivers.

Temporary Master Access Control

This section of the controller controls the DMA transfers on the Z-100 bus. U28 and U29 are PALs programmed to perform data transfers on the Z-100 bus. When DMARUN and BYTRDY are asserted by the bit-slice processor, U28 will assert the IWANT signal, starting U25 and U55 (the arbitration logic) to determine bus control. The exact sequence and timing is outlined in the IEEE-696 (S-100) bus specification.

The dip switches permit you to select the DMA priority level desired for the controller. U27B is used to echo back a signal called $\overline{\text{TMACBUSY}}$ to the bit-slice processor. This signal tells the bit-slice that the TMAC is in the process of transferring a byte. U56 and U20 are buffers used to assert the status and control lines on the Z-100 bus. The TMAC issues a signal called $\overline{\text{ENASDBUF}}$ that is connected to the address buffers of section A. It causes the output enable to go low, so addresses are driven on to the bus. $\overline{\text{LDDATA}}$ is another signal issued by the TMAC to strobe data into the data buffer at the correct time during a read cycle. An interrupt at any time in the transfer cycle will cause the present cycle to complete and then to release bus control.

The Data Separator

The data separator card and its attendant circuitry are proprietary information and the property of Zenith Data Systems. For this reason, no circuit description, parts listing, or schematic diagram is furnished. However, you may refer to Pictorial 3, the Block Diagram of the Data Separator Card for general information as to its function within the Z-217-1 Controller.

Controller Board Connector

P1 – 100 Pin Bus Interface

1	N/U	26	PHOLDA	51	N/U	76	PSYNC
2	N/U	27	N/U	52	N/U	77	PWR*
3	XRDY	28	N/U	53	GND	78	PDBIN
4	VI0*	29	A5	54	N/U	79	A0
5	VI1*	30	A4	55	DMA0*	80	A1
6	VI2*	31	A3	56	DMA1*	81	A2
7	VI3*	32	A15	57	DMA2*	82	A6
8	VI4*	33	A12	58	SXTRO*	83	A7
9	VI5*	34	A9	59	A19	84	A8
10	VI6*	35	DO1	60	SIXTN*	85	A13
11	VI7*	36	DO0	61	A20	86	A14
12	N/U	37	A10	62	A21	87	A11
13	N/U	38	DO4	63	A22	88	DO2
14	DMA3*	39	DO5	64	A23	89	DO3
15	A18	40	DO6	65	N/U	90	DO7
16	A16	41	DI2	66	N/U	91	DI4
17	A17	42	DI3	67	N/U	92	DI5
18	SDSB*	43	DI7	68	N/U	93	DI6
19	CSDB*	44	SM1	69	N/U	94	DI1
20	GND	45	SOUT	70	GND	95	DI0
21	N/U	46	SINP	71	N/U	96	SINTA
22	ADSB*	47	SMEMR	72	RDY	97	SWO*
23	DODSB*	48	SHLTA	73	INT*	98	N/U
24	I	49	N/U	74	HOLD*	99	N/U
25	PSTVAL*	50	GND	75	RESET*	100	GND

N/U = Not Used

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In Case of Difficulty

The Z-217 Disk Controller and Data Separator are not considered to be user serviceable. If your controller or separator does not operate properly, first refer to the chart below. If the problem persists, return it to one of the repair centers listed in the documentation you received with the Z-100 Computer.

Problem	Possible Solution
Winchester does not boot.	1. Verify correct version of ROM. 2. Verify settings of DIP SW101. 3. Verify correct positioning of programming jumpers. 4. Check all cable connections. 5. Remove and reseat Controller board. 6. Review software. See *Z-100 User's Manual Winchester Supplement.*

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Replacement Parts

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION

Resistors

All resistors are 1/4 W, 5%, unless marked otherwise.

R1, 2, 4, 5, 21	6-102-12	1000 Ω
R3	6-101-12	100 Ω
R20	6-471-12	470 Ω
RP10	9-135	220 Ω resistor pack
RP20–RP25	9-124	4700 Ω resistor pack

Capacitors

All capacitors are 20%, unless marked otherwise.

C1–C57	21-786	0.1 μF ceramic
C100–C103	25-915	47 μF electrolytic

Switches

S1	60-667	DIP 2 pos. SPST

Miscellaneous

Y1	150-145	12 MHz crystal

Semiconductors

See "Semiconductor Identification."

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Semiconductor Identification

This section is divided into two parts. The "Component Number Index" relates circuit component numbers to Heath part numbers. The "Part Number Index" relates part numbers to manufacturers' part numbers, and provides lead configuration drawings for each part.

Component Number Index

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D1–D2	56-61
Q101	417-875
U1–U5	443-1031
U6	443-1084
U7, U8	443-1031
U9	Not used
U10	443-1096
U11	443-1091
U12, U13	443-1090
U14	444-155
U15	444-156
U16	444-157
U17	444-158
U18	444-159
U19	444-160
U20	443-1096
U21, U22	443-878
U23	443-900
U24	444-153
U25, U26, U27	443-1051
U28	444-151
U29	444-152
U30	443-879
U31	443-1087
U32	443-878
U33, U34	443-1075
U35	443-877
U36–U38	443-1094
U39	443-1079
U40	443-1097
U41	443-1098 or 443-805
U42	443-967
U43	443-879
U44	443-1097
U45	443-1098 or 443-805
U46	444-150
U47	443-1095
U48	443-1098 or 443-805
U49	443-1084
U50, U51	443-967
U52	443-872
U53	443-901
U54	443-1020
U55	444-154
U56	443-857
U57-U79	Not used
U80	443-1092

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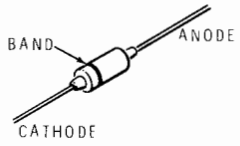
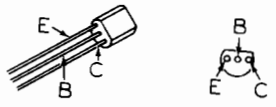
Semiconductor Identification

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
56-61	STB620	Diode	

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
417-875	2N3904	Transistor	

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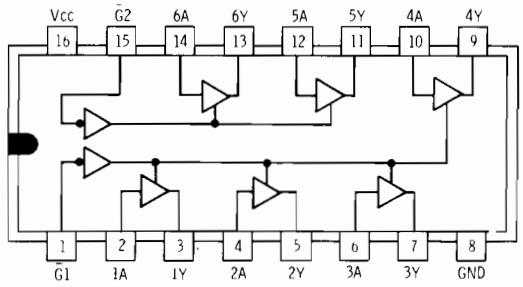
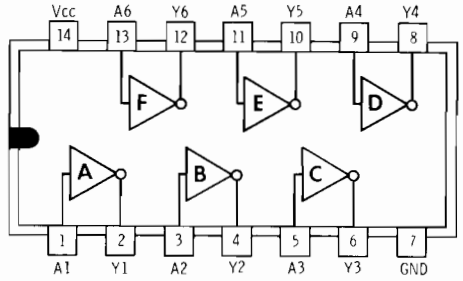
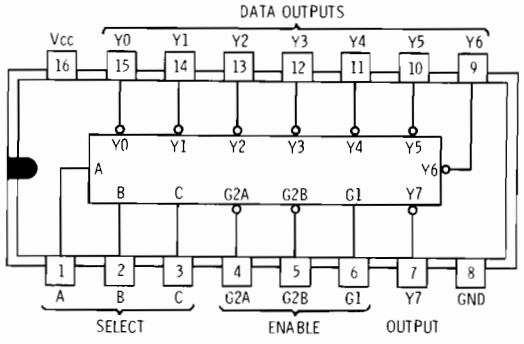
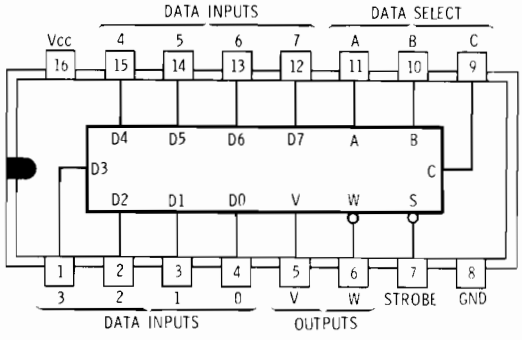
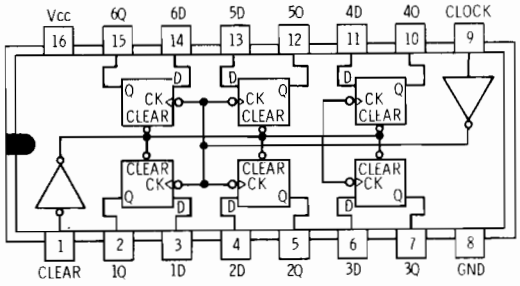
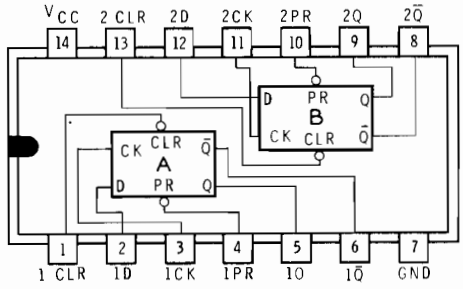
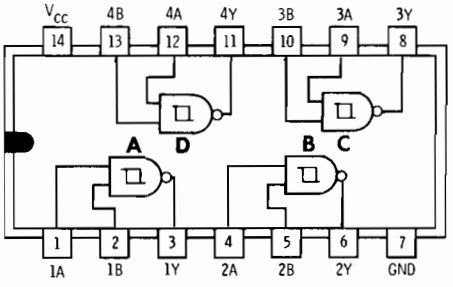
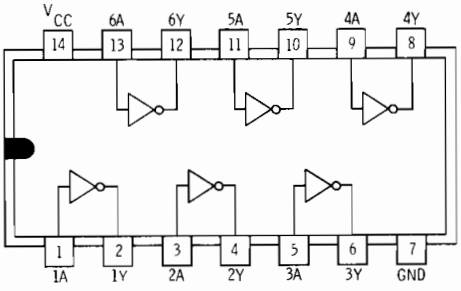
Semiconductor Identification

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-857	74LS367	Tri-state hex buffer	
443-872	74LS14	Hex inverting Schmidt trigger	
443-877	74LS138	3-line to 8-line decoder	
443-878	74LS151	8-input multiplexer (MUX)	

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-879	74LS174	D-type hex flip-flop	
443-900	74S74	Dual D flip-flop	
443-901	74S132	Quad, 2-input NAND Schmidt trigger	
443-967	7406	Open collector hex inverter/ driver	

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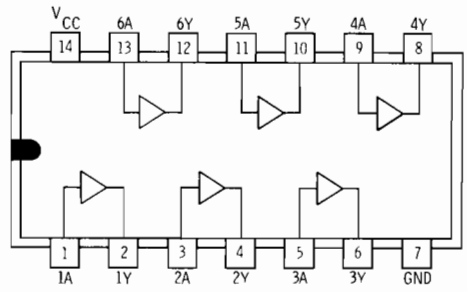
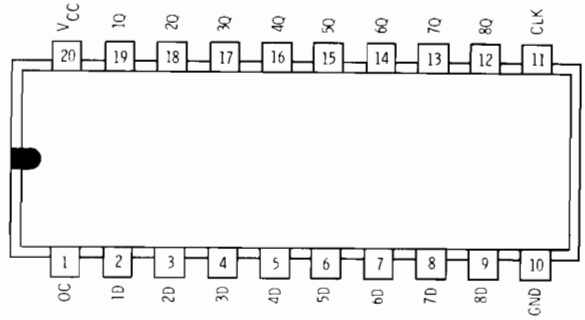
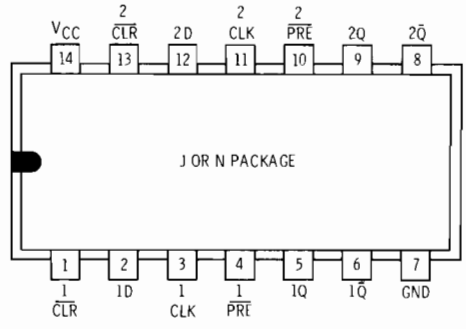
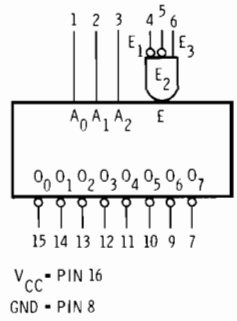
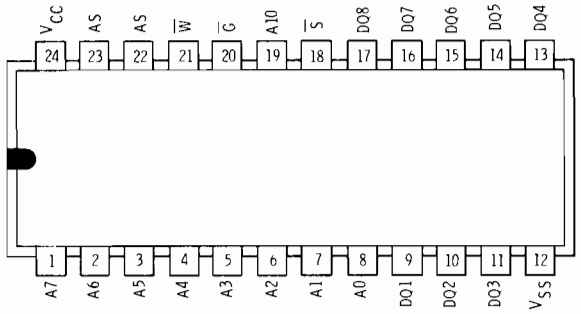
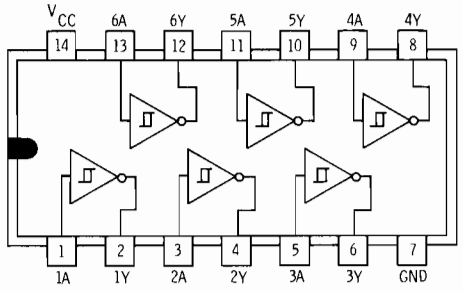
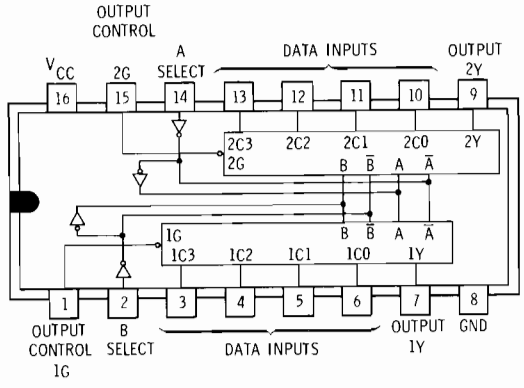
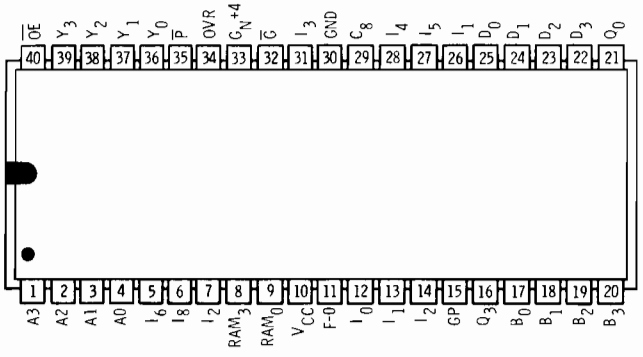
Semiconductor Identification

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1020	7407	Open collector hex buffer/ driver	
443-1031	74ALS574	3-gate octal D flip-flop	
443-1051	74ALS74	Dual D flip-flop	
443-1075	74F138	3-line to 8-line decoder	

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1079	TMS 4016	2K × 8 static RAM	
443-1084	74LS19	Hex inverting Schmidt trigger	
443-1087	74LS253	Dual 4-to-1 MUX	
443-1090	2901B	4-bit arithmetic logic unit (ALU)	

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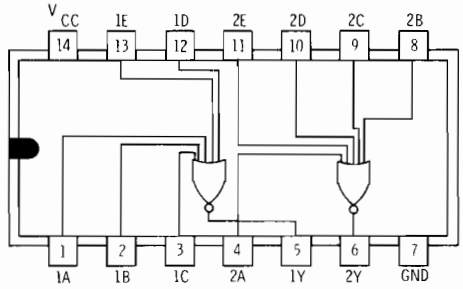
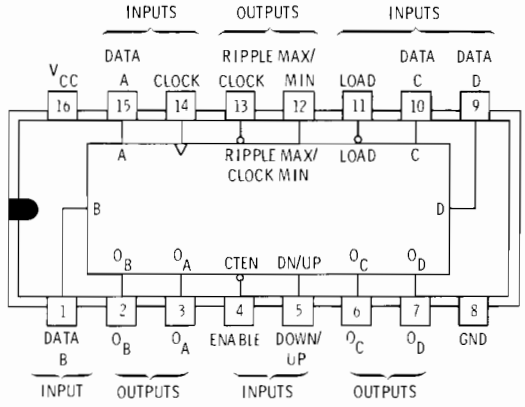
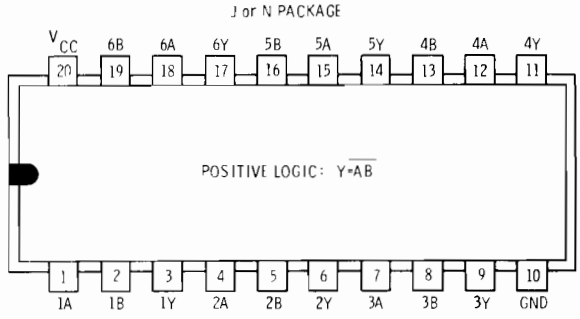
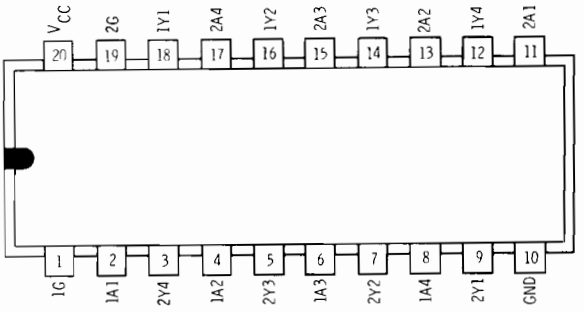
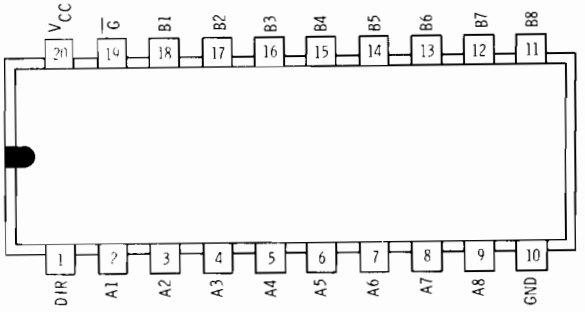
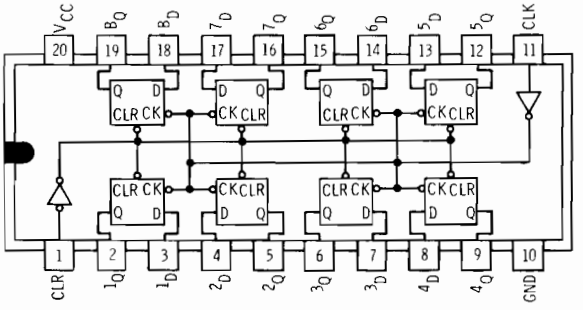
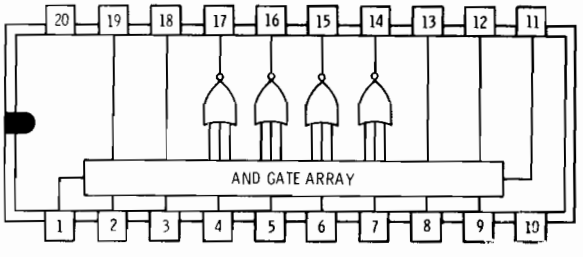
Semiconductor Identification

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1091	2910	Micro-program control	
443-1092	74LS260	Dual 5-input NOR gate	
443-1094	74LS191	Up/Down sync. counter	
443-1095	74AS804	Hex 2-input NAND driver	

Semiconductor Identification

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1096	74ALS244	3-state octal buffer	
443-1097	74ALS245	3-state octal transceiver	
443-1098 -or- 443-805	74ALS273 -or- 74LS273	Octal flip-flop	
444-150	See page following these charts.*	Address decoder	

*This component is available only from Zenith Data Systems or Heath Company.

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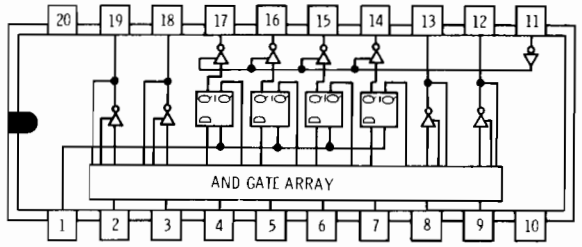
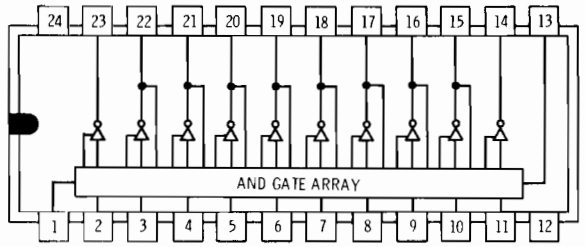
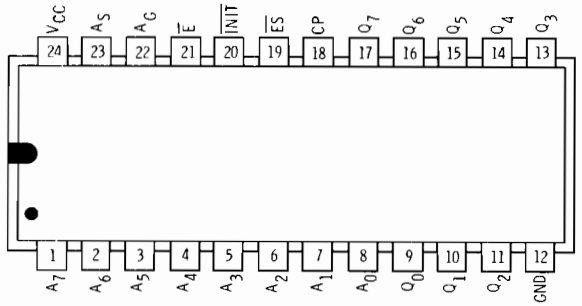
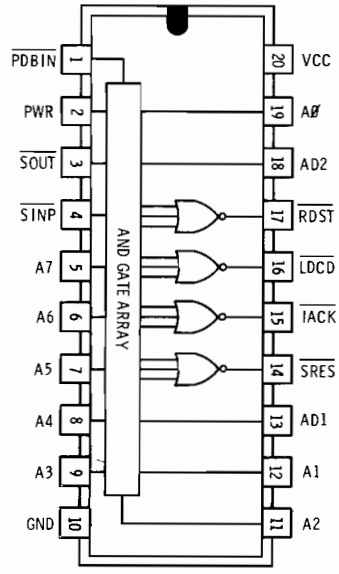
Semiconductor Identification

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
444-151-1	*	TMACA	
444-152-3	*	Array logic	
444-153	*	PAL	
444-154	*	Arbitrator	
444-155-2	*	Bits 0–7	
444-156-2	*	Bits 8–15	
444-157-2	*	Bits 16–23	
444-158-2	*	Bits 24–31	
444-159-2	*	Bits 32–39	
444-160-2	*	Bits 40–47	
444-9038	*	1K × 8 PROM	

*These components are available only from Zenith Data Systems or Heath Company

PAL Equations for 444-150



$\overline{SRES}$ = SOUT*PWR*AD1*AD2*A7*$\overline{A6}$*A5*$\overline{A4}$*A3*A2*A1*A0

$\overline{IACK}$ = SINP*PDBIN*AD1*AD2*A7*$\overline{A6}$*A5*$\overline{A4}$*A3*A2*A1*A0

$\overline{LDCD}$ = SOUT*PWR*AD1*AD2*A7*$\overline{A6}$*A5*$\overline{A4}$*A3*A2*A1

$\overline{RDST}$ = SINP*PDBIN*AD1*AD2*A7*$\overline{A6}$*A5*$\overline{A4}$*A3*A2*A1

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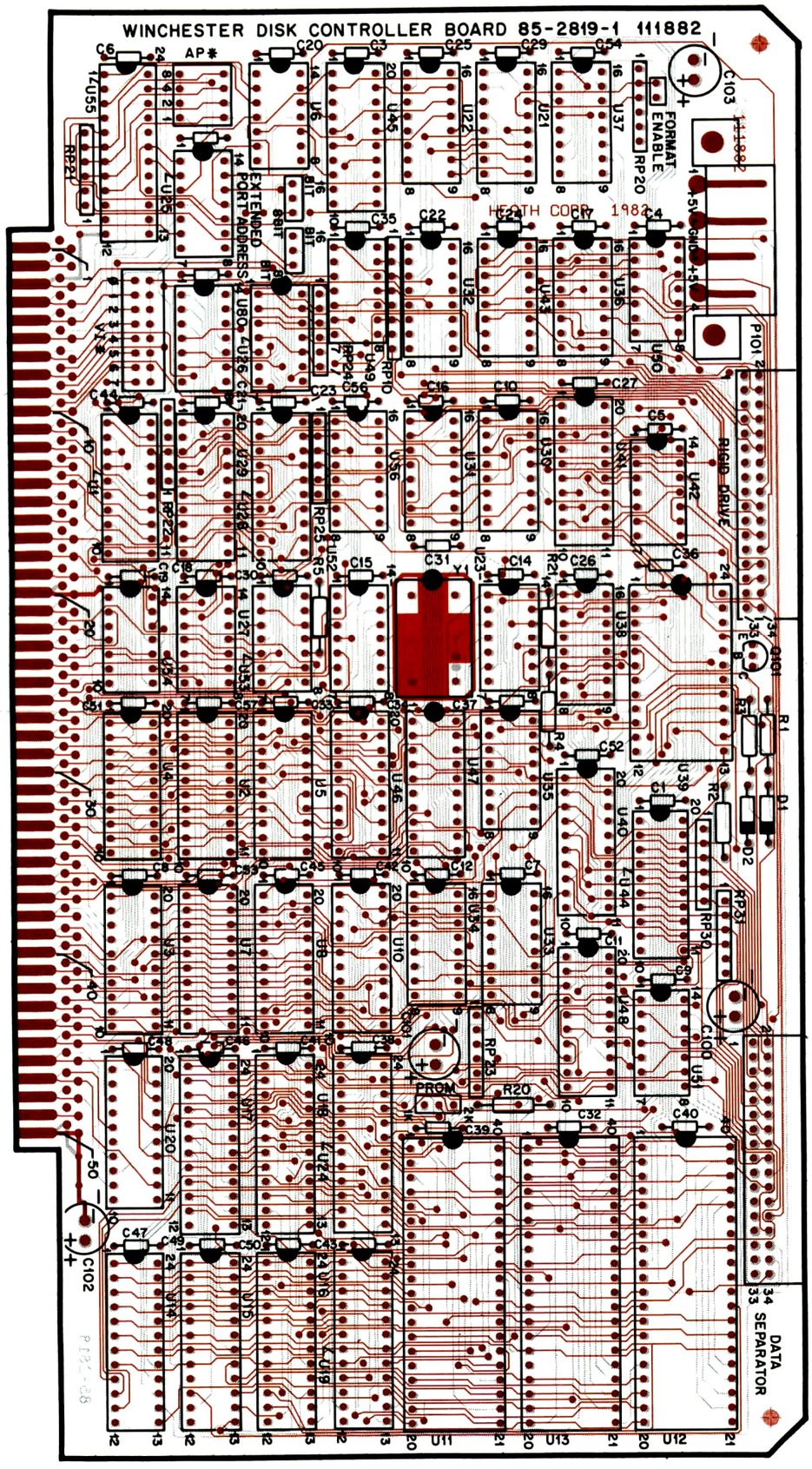
Circuit Board X-Ray View

NOTE: To find the PART NUMBER of a component:

A. Find the circuit component number (R111, C101, etc.) on the "X-Ray View" (fold-out from this page).

B. Locate this same number in the "Circuit Component Number" column of the "Replacement Parts List."

C. Adjacent to the circuit component number, you will find the PART NUMBER and DESCRIPTION.


WINCHESTER DISK CONTROLLER BOARD 85-2819-1 111882
HEATH CORP. 1982
FORMAT ENABLE
EXTENDED PORT ADDRESS
RIGID DRIVE
DATA SEPARATOR
PROM
AP*
P101
C103
C102
Y1