ZENITH data systems

THE QUALITY GOES IN BEFORE THE NAME GOES ON

DESKTOP COMPUTER SYSTEMS

Z-205 USER'S MANUAL

Desktop Computer

Z-205 RAM CARD USER'S MANUAL

ZENITH | data systems

TABLE OF CONTENTS

INTRODUCTION

The Z-205 Dynamic RAM (Random Access Memory) Card gives your Z-100 Computer an additional 256K of memory. You may give your system additional RAM, up to a total system memory of 768K, by adding additional Cards. This main board must contain 192K of RAM. This Card is supplied fully populated, and may be placed in any vacant card slot in your Computer.

You can configure the RAM in many ways with the switches located on the Card. This configuration capability is especially useful if you have to troubleshoot, or configure the added memory around or in support of existing memory.

All of the information you need to use the features of the Z-205 Dynamic RAM Card is contained within this Manual. Please read it carefully before attempting to use your Z-205 Dynamic RAM Card.

SPECIFICATIONS

Memory Size	262,144 bytes × 9 (1-parity) in four banks of 65,536.
Memory Chip Type	64K × 1 Dynamic RAM, 5 volt single supply.
Addressing	256K contiguous address locations, configurable on 64K boundaries within 1 of 16 1-megabyte blocks.
Parity	Byte parity for error detection.
Access Time	292 ns maximum using 200 ns RAM.
Width	256K × 8 + parity or 128K × 16 + byte parity. Automatic width selection via S-100 bus 16REQ/16ACK signals.
Wait States	0, 1, 2, or 3, user-selectable.
Bus Interface	S-100, proposed IEEE Standard 696.
Refresh	Transparent, onboard, independent of bus.
Power Requirements	8–11 volts DC at 1.2 A maximum.

DISASSEMBLY

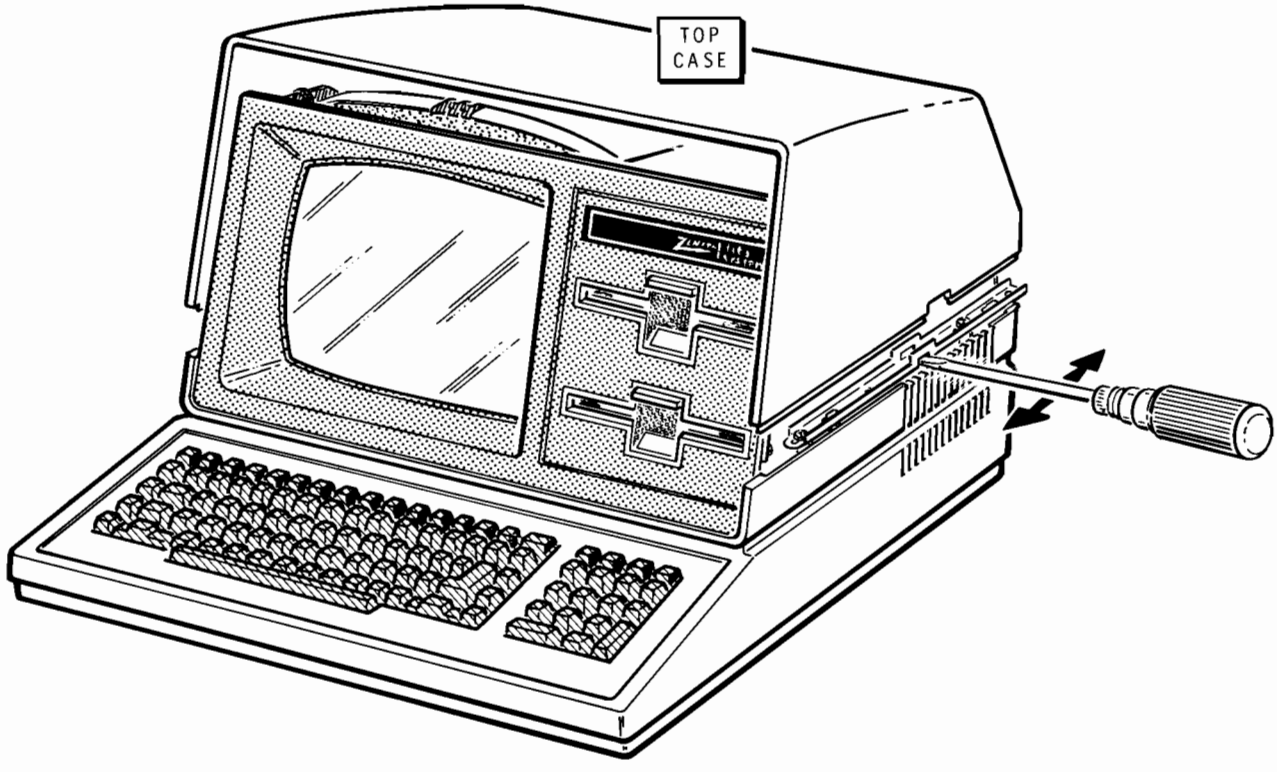
All-in-One Models

WARNING: When the line cord is connected to an AC outlet, hazardous voltages can be present inside your Computer.

☐ Unplug the line cord from the AC outlet.

☐ Refer to Pictorial 1. Using a small flat-blade screwdriver, move the metal slides all the way to the front and then 1/4" to the back as shown.

☐ Carefully lift the top case straight up and set it to one side.

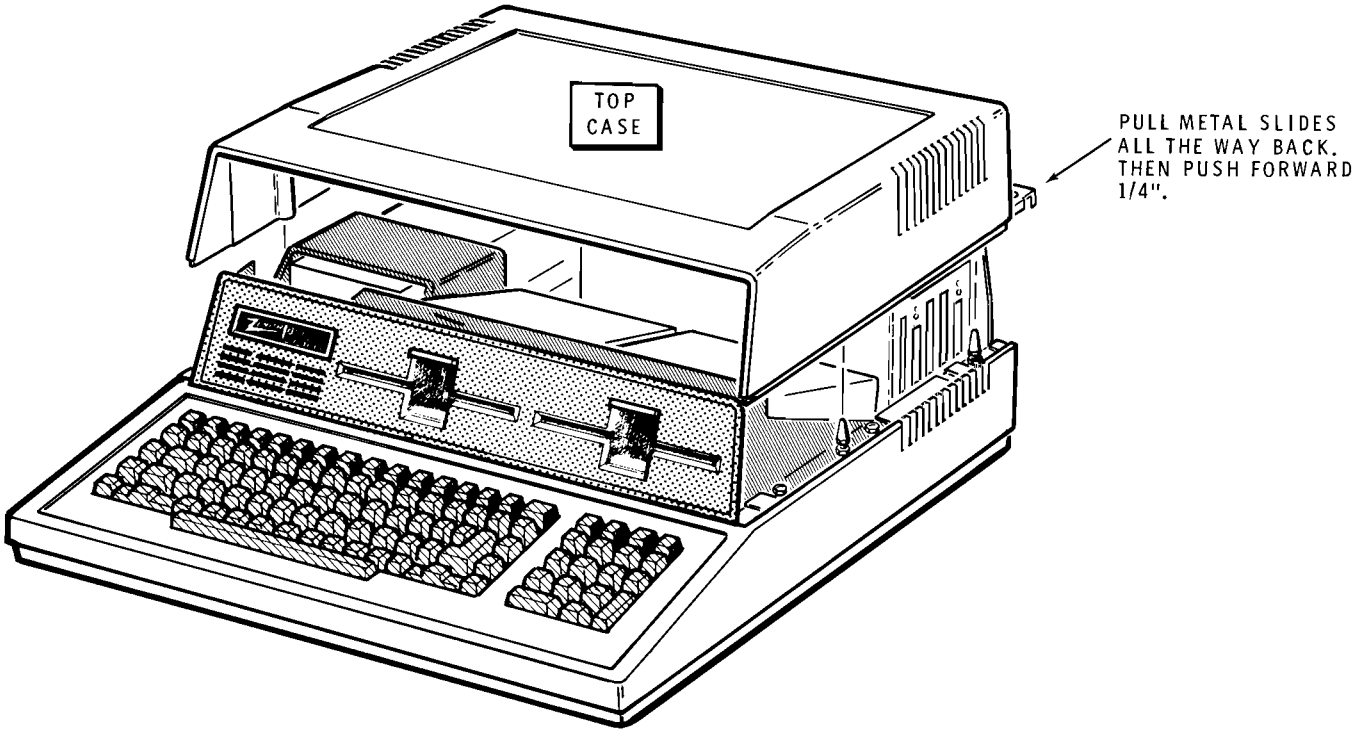


PICTORIAL 1

Low-Profile Models

WARNING: When the line cord is connected to an AC outlet, hazardous voltages can be present inside your Computer.

- ☐ Unplug the line cord from the AC outlet.
- ☐ Refer to Pictorial 2. Pull the metal slides all the way to the back, and then push 1/4" to the front as shown.
- ☐ Carefully lift the top case straight up and set it to one side.



PICTORIAL 2

CONFIGURATION

Typical Configuration

The following typical configuration instructions allow you to access the full 256K RAM on your Z-205 Card. Typical configuration data for H/Z-100 owners who use **more** than one Z-205 Card is found on Page 16. For special applications that require less than 256K RAM, or for system information for other than Zenith products, refer to the "Detailed Configuration Data" below.

NOTE: If you have more than one Card, repeat the following steps for each Card. Some of the jumpers and switches may already be in the correct position.

Refer to Pictorial 3 for the following steps.

- ☐ Position the Card as shown in the pictorial.
- ☐ Place a programming jumper on J6 (no wait states).
- ☐ Place programming jumpers on J7, pins 4 and 5, and on J7 pins 2 and 3 (normal operation and four banks).
- ☐ Set DIP (Dual In-line Pack) switch SW1 positions 0 and 1 to the OFF (0) position, and all others to the ON (1) position.
- ☐ Set DIP switch SW2 positions 0 and 1 to the ON (1) position, and all others to the OFF (0) position.

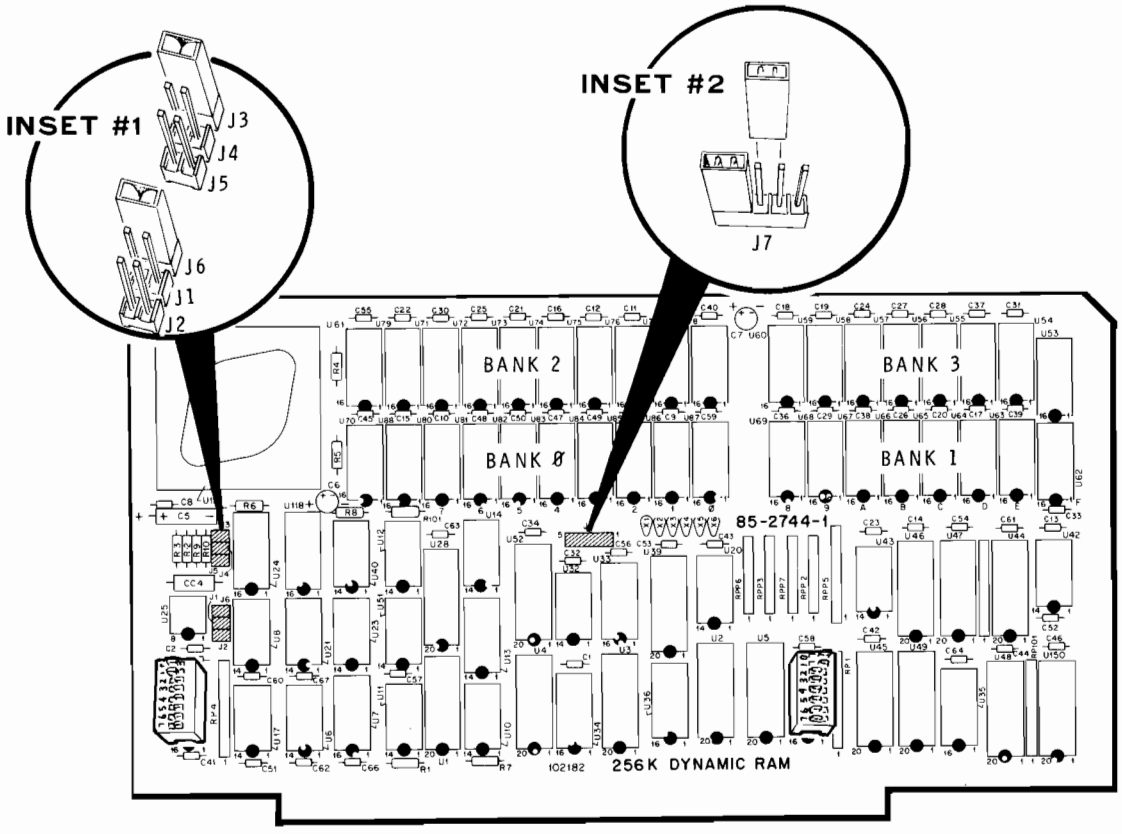
NOTE: We assume that your H/Z-100 has the full 192K RAM installed. If it only has 128K RAM and the Z-205 Card is configured to respond to addresses in the 20000 (Hex)-5FFFF (Hex) range, it is possible to damage the mother board's data bus buffers. This will result in either an inoperative system, memory expansion, or both.

This completes the basic configuration for a Z-205 Dynamic RAM Card. Repeat these steps for each Card. Then proceed to "Installation."

Detailed Configuration Data

The following information is furnished to allow purchasers of the Z-205 Dynamic RAM Card to configure the card for their non-Zenith Data System S-100 microcomputers, as well as for the Z-100 user who desires to make modifications or effect a customized configuration.

Refer to Pictorial 3 for the locations of the jumpers and switches.



Legend:

Bank 0	Used in 64K configuration.
Banks 0,1	Used in 128K configuration.
Banks 0,1,2,3	Used in 256K configuration.

NOTE: It is possible to select any configuration on the fully populated board.

PICTORIAL 3

CONFIGURATION

JUMPERS

J1 Open for 256K. Add programming jumper for 128K and 64K operation.

J2 Open for 256K and 128K. Add programming jumper for 64K operation.

J1	J2	COMMENTS
O	O	256K
I	O	128K
O	I	Not defined
I	I	64K

NOTE: I = Installed [programming jumper used]
O = Open [programming jumper **not** used]

J3 Add programming jumper for 3 wait states.

J4 Add programming jumper for 2 wait states.

J5 Add programming jumper for 1 wait state.

J6 Add programming jumper for 0 wait state.

NOTE: You may only select **one** of the above programming jumpers. Any attempt to select more than one jumper will result in damage to U24, and a system failure.

J7 Place programming jumpers on pins 2 & 3 and 4 & 5 for normal (8-bit or 16-bit) operation for use with 128K or 256K.
Place programming jumpers on pins 1 & 2 and 3 & 4 for 64K (8-bit only with 1 bank) operation.

CONFIGURATION

SWITCHES

DIP switches SW1 and SW2 are used for the following purposes:

SW1—The Z-205 Card uses one I/O port to control and monitor the parity error circuitry. SW1, an eight-position switch, permits you to select any one of 256 possible address locations as the I/O (input/output) port address. For example, to select the address 98[HEX], you would set SW1 as shown below. NOTE: ZDS/Heath Computers use port address 98 (Hex) for the first 192K–448K, and 99 (Hex) for the second 448K–704K.

POSITION	ADDRESS BIT	ON/OFF
0	A0	OFF
1	A1	OFF
2	A2	OFF
3	A3	ON
4	A4	ON
5	A5	OFF
6	A6	OFF
7	A7	ON

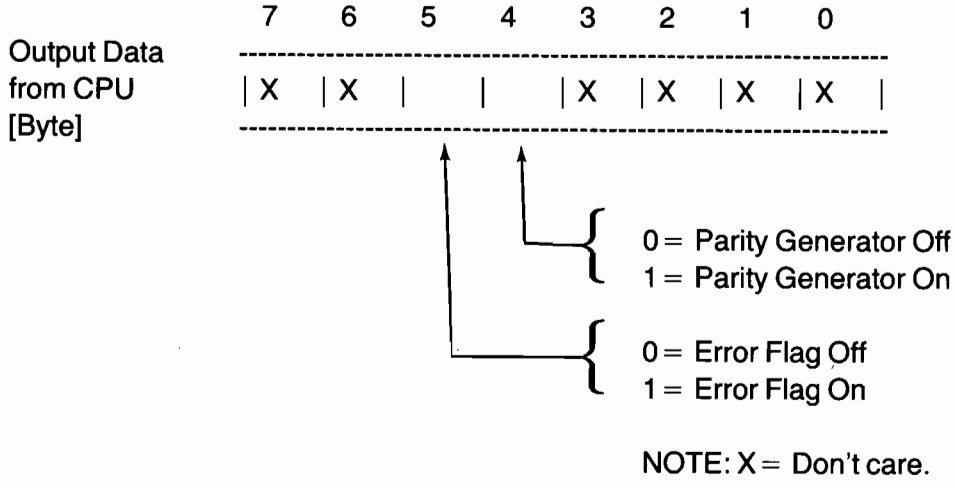
SW2—The Z-205 Card is addressed as a single (64K, 128K, or 256K) block of contiguous memory starting on a 64K boundary. The starting address is selected by SW2, an eight-position switch. To access the full 256K RAM, starting with address location 30000H (192K), SW2 would be set as follows:

POSITION	ADDRESS BIT	ON/OFF
0	A16	ON
1	A17	ON
2	A18	OFF
3	A19	OFF
4	A20	OFF
5	A21	OFF
6	A22	OFF
7	A23	OFF

CONFIGURATION

INPUT/OUTPUT PORT

A single I/O port is used for parity control and status monitoring. The following representations show you the input data from the memory board and what information being sent as output data from the CPU will look like. Both representations are of a data byte.



NOTE: X = Don't care.

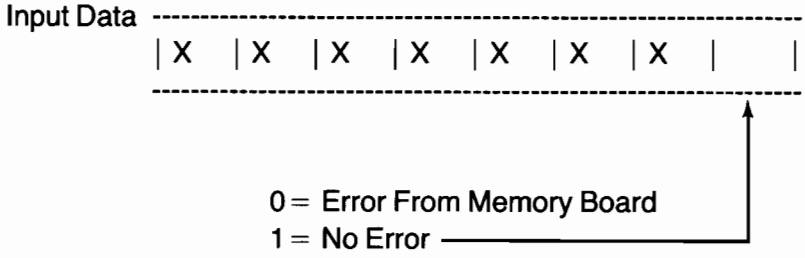
Parity Generator

The parity generator is an onboard circuit that writes a 1 into the parity RAM when the incoming byte has an even number of 1's. It writes a 0 into the parity RAM when the incoming byte has an odd number of 1's. You can disable this function by writing a data word with bit 4 set to 0, and outputting this byte to the I/O port.

Error Flag

The error flag is set by onboard circuitry when the parity detected during the read cycle is even (or incorrect). To clear an error flag: output XX01XXXX and then XX11XXXX to the I/O port selected by SW1.

NOTE: On power up, the parity generator and error flag circuits are disabled. Thus, you must enable these circuits by software commands. You may enable them by writing a 1 to bits 4 and 5 and outputting the byte to the I/O port.



NOTE: X = Don't care.

Parity Error from Memory Board

If a parity error happens, you can determine which memory board it occurred on by inputting from the I/O port and checking bit 0. If an error occurred, bit 0 will be set to 1; if not, bit 0 will be set to 0.

INSTALLATION

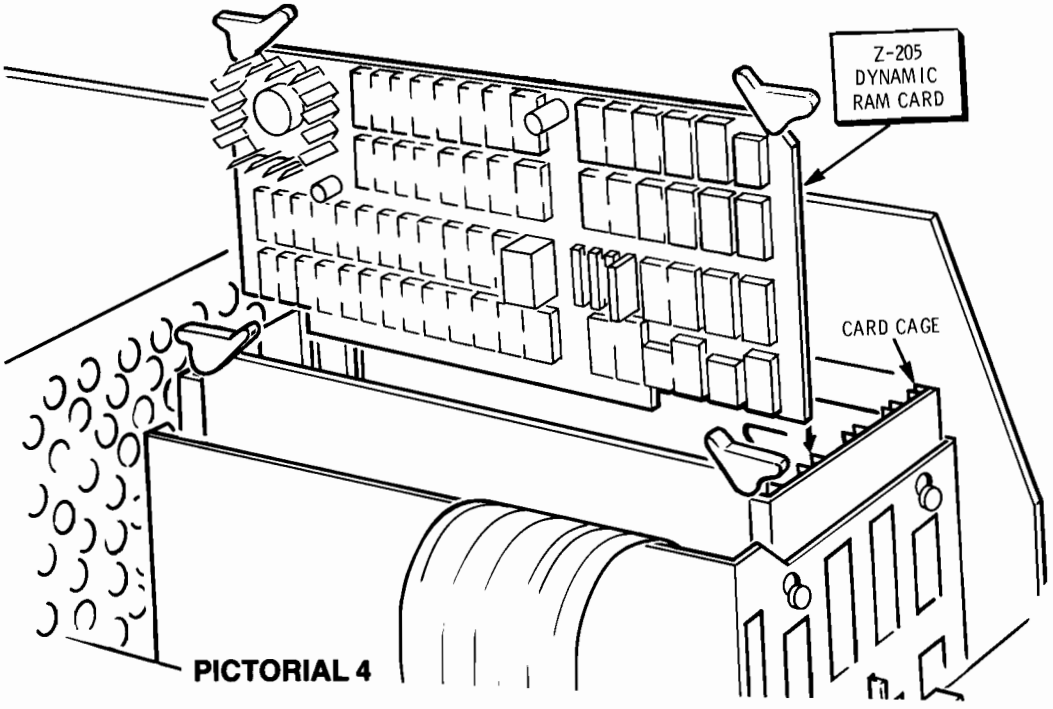
NOTES:
1. If you have more than one Z-205 Card, install only one of them at this time. You will install the others after you complete the "Initial Test."
2. Be sure the DIP switches (SW1 and SW2) and the programming jumpers are in the correct positions before you install the Card. See "Configuration," Page 11.
3. Disconnect the 8-inch floppy drive cable from your H/Z-207 board if it has been installed. Reconnect this cable **after** installing your Z-205 Card(s).

Refer to Pictorial 4 for the following steps.

☐ Select a vacant slot in the card cage assembly (we recommend slot 2).

☐ Insert the Z-205 Card with the components **facing you** into the vacant slot and seat it firmly by pushing straight down.

This completes the installation of your Z-205 Card.



PICTORIAL 4

INITIAL TESTS

Use the following procedure to test your newly installed Z-205 Dynamic RAM Card. If you have purchased more than one Card:

1. Test each Card separately.

2. After you complete the tests on the first Card, remove it from the card cage and install the second Card in its place.

3. Repeat the tests on this Card.

Be sure, on each Card, that the DIP switches (SW1 and SW2) and the programming jumpers are in the correct positions before you install the Card. See "Configuration," Page 11.

☐ Turn your Computer and monitor on.

☐ At the prompt, enter the following commands exactly as shown:

```
F
     [your Computer will reply]
FILL
FILL 3000:0-FFFF, 33 RETURN
FILL 4000:0-FFFF, 44 RETURN
FILL 5000:0-FFFF, 55 RETURN
FILL 6000:0-FFFF, 66 RETURN
```

Running the Test

☐ To display the last 128 Bytes in the first 64K block enter:
`DUMP 3000:FF90-000F` RETURN

☐ To display the last 128 Bytes in the next 64K block enter:
`DUMP 4000:FF90-000F` RETURN

☐ To display the last 128 Bytes in the next 64K block enter:
`DUMP 5000:FF90-000F` RETURN

☐ To display the last 128 Bytes in the last 64K block enter:
`DUMP 6000:FF90-000F` RETURN

☐ To exit this test sequence enter:
`Q` RETURN

This completes the Initial Test. Repeat these tests for each Card if you have more than one.

Perform the following steps only if you have more than one Z-205 Card for your system. If you have only one card, proceed to "Screen Display."

Final Configuration, Multi-Card

Second Card

☐ Set DIP switch SW2 positions 7, 4, 3, and 0 to the ON (1) position. Set all others to OFF (0).

Install your Z-205 Cards in the vacant slots in the card cage.

Screen Display

This completes the entry of the Initial Test. Pictorial 5 shows the display as the memory test is cycled*. Your screen display should resemble the display shown in Pictorial 5. If you experience any difficulties, refer to the "In Case of Difficulty" section of this Manual.

```
3000:FF90  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFA0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFB0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFC0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFD0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFE0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:FFF0  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333
3000:0000  33 33 33 33 33 33 33 33-33 33 33 33 33 33 33 33  3333333333333333

4000:FF90  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFA0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFB0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFC0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFD0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFE0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:FFF0  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD
4000:0000  44 44 44 44 44 44 44 44-44 44 44 44 44 44 44 44  DDDDDDDDDDDDDDDD

5000:FF90  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFA0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFB0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFC0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFD0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFE0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:FFF0  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU
5000:0000  55 55 55 55 55 55 55 55-55 55 55 55 55 55 55 55  UUUUUUUUUUUUUUUU

6000:FF90  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFA0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFB0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFC0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFD0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFE0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:FFF0  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
6000:0000  66 66 66 66 66 66 66 66-66 66 66 66 66 66 66 66  ffffffffffffffff
```

PICTORIAL 5

Proceed to "Re-Assembly."

*Only 25 lines of the display can be shown on the screen at one time.

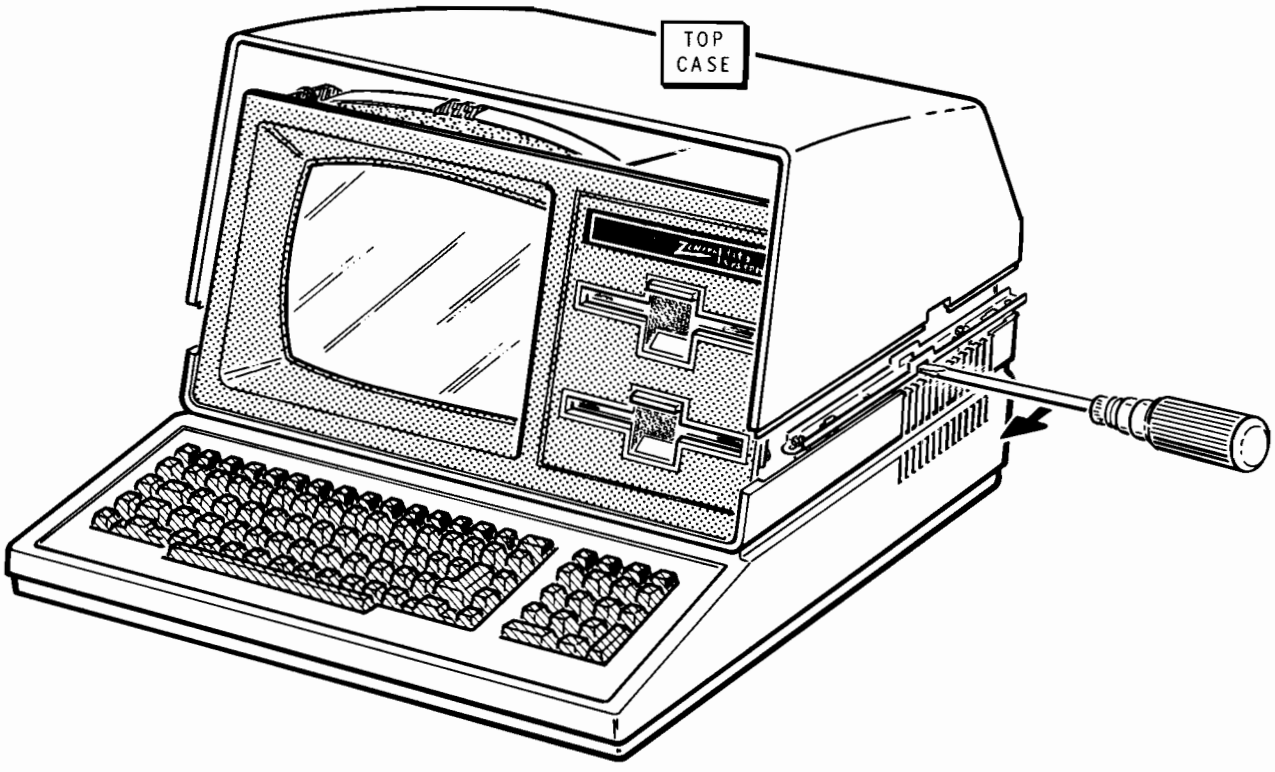
REASSEMBLY

All-in-One

☐ Reconnect your 8″ drive cable (if necessary).

☐ Refer to Pictorial 6. Replace the top case by bringing it straight down into its position and slide the latches all the way to the front.

This completes the reassembly of the All-in-One model.



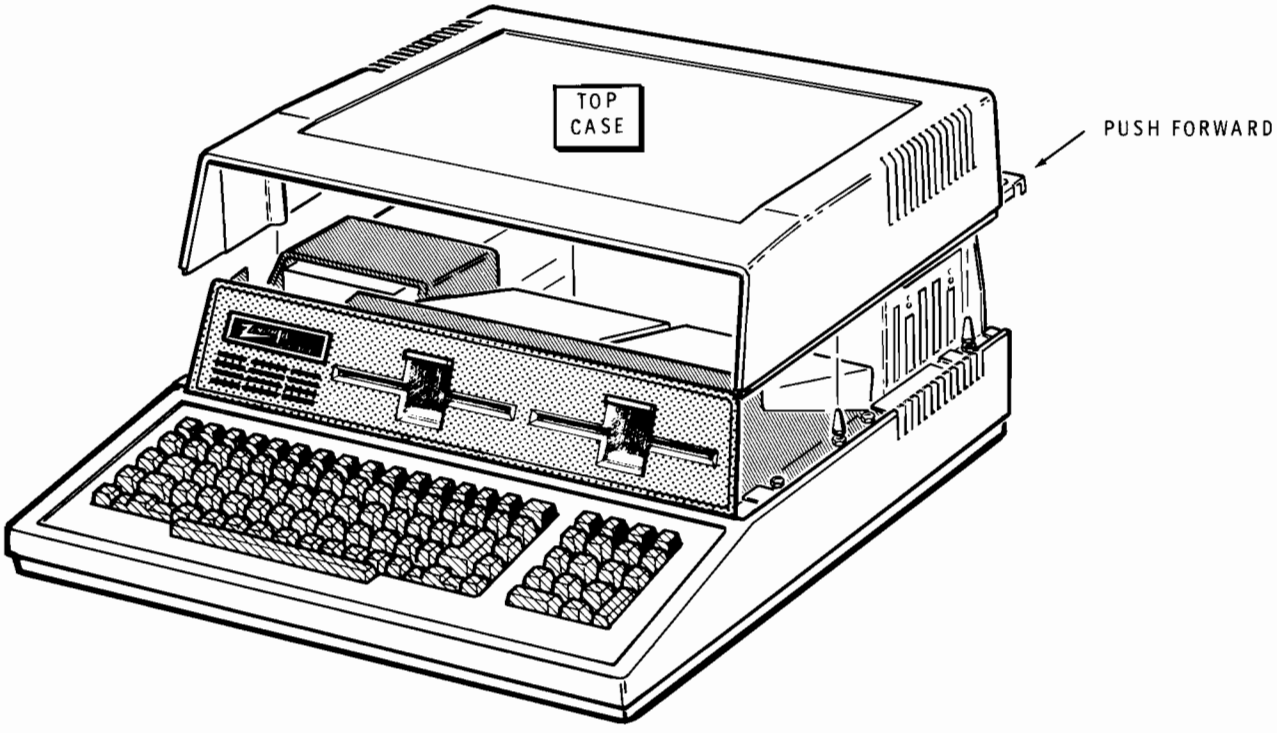
PICTORIAL 6

Low Profile

☐ Reconnect your 8" drive cable (if necessary).

☐ Refer to Pictorial 7. Replace the top case by bringing it straight down into its position. Push the latches all the way to the front.

This completes the reassembly of the Low-Profile model.



PICTORIAL 7

THEORY OF OPERATION

Refer to Pictorial 8, the Block Diagram, as you read the following description.

The Z-205 Dynamic RAM Card is divided into seven main sections.

The address bus buffers.
The address multiplexer (MUX).
The refresh circuit.
The system decode and control circuits.
Four banks of dynamic Random Access Memory (RAM).
The parity circuit.
The 8/16-bit data multiplexer circuit.

Address Bus Buffers

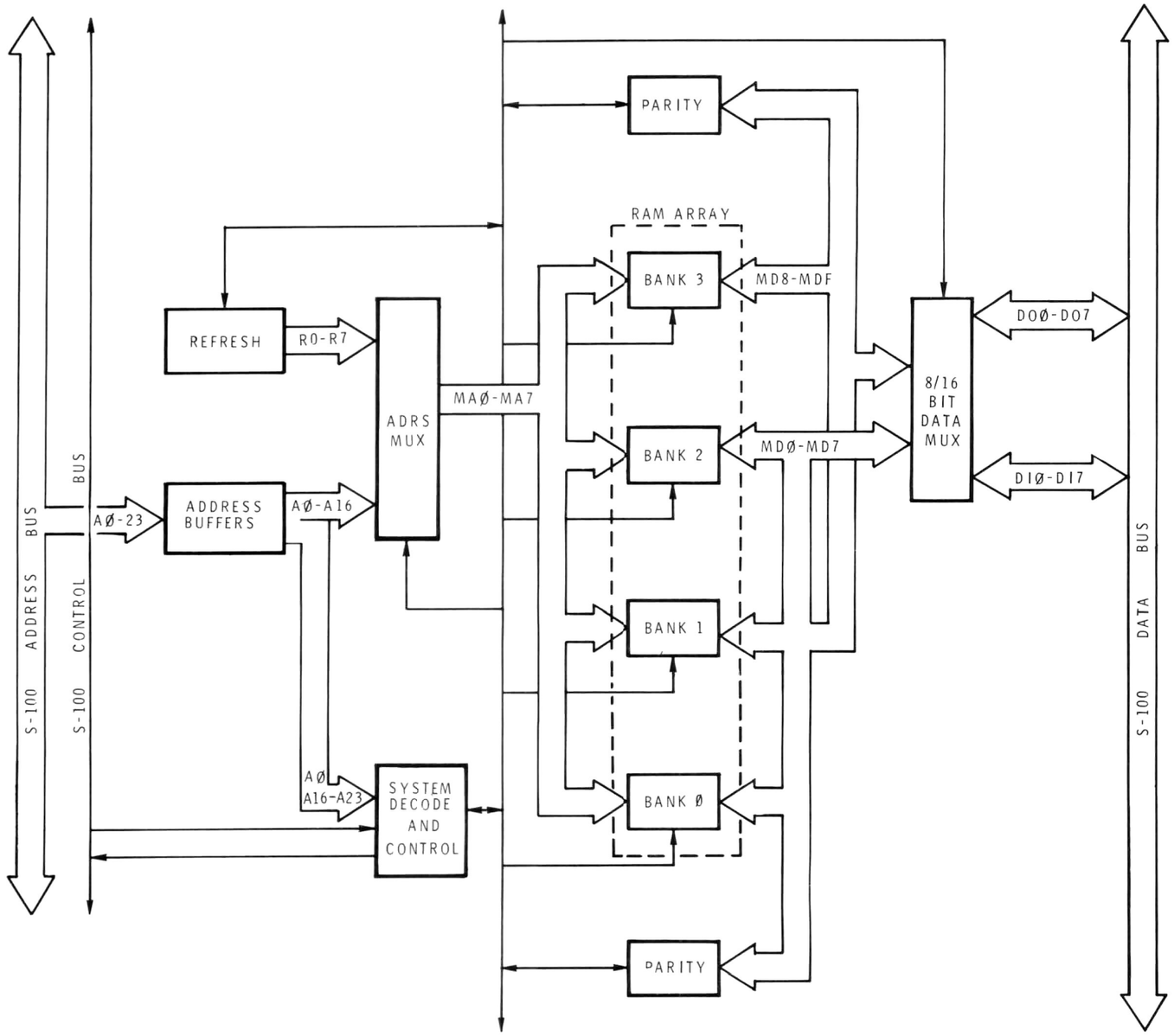
The address bus buffers are bus receivers for the S-100 address and control signals.

Address Multiplexer (MUX)

The address multiplexer circuit passes the eight bits of row address during the row address strobe (RAS) time, and then the eight bits of column address during the column address strobe (CAS) time. They also pass the eight-bit refresh address during memory refresh cycles.

Refresh Circuit

The refresh timer circuit periodically generates a high-going edge to start the refresh process. Flip-flops are used to synchronize the refresh pulses to the bus clock and start the refresh cycle. A programmable array logic (PAL™) contains the logic to handle contention problems between normal memory accesses and refresh cycles.



PICTORIAL 8
Block Diagram of the Z-205 Dynamic RAM Card

System Decode and Control

The system decode and control circuits contain all of the logic necessary to control normal memory accesses and I/O accesses, to perform address decoding, to generate memory array strobes, to select row and column addresses for the RAM array, to handle refresh contention, to handle parity errors, and to control the eight and 16-bit data transfers.

Random Access Memory Array

The dynamic random access memory array consists of four banks of eight 64K by one bit RAM chips. The four banks are capable of storing up to 262,144 (256K) bytes of data and program instructions. To populate the RAM array, all four banks are filled with RAM chips for 256K, or bank 0 and bank 1 are filled for 128K, or bank 0 is filled for 64K. The Card is supplied fully populated.

Parity Circuit

The parity circuit consists of two 9-bit parity generators/checkers and four parity RAMs identical to the 64K dynamic RAMs used in the memory array. Each parity generator/checker monitors an internal data bus coming from the memory array. The output of the parity generators drive the error detection circuitry in the system control portion of the board, passing parity bits to the RAMs for storage. The parity checkers test the parity bits from the parity RAMs along with the original data byte from the memory array to determine if an error has occurred.

THEORY OF OPERATION

8/16-bit Data Multiplexer

The 8/16-bit data multiplexer consists of buffers and transparent latches.

Two buffers and one latch are connected to the data output lines (DO0–DO7) from the S-100 bus. The two buffers provide a path from the data output lines to either of the internal data busses, while the latch provides a path from the even-bank (bank 0 and bank 2) data bus to DO0–DO7 during a 16-bit read.

Two latches and one buffer are connected to the data input lines (DI0–DI7) on the S-100 bus. The two latches couple data from either bank of the memory array to DI0–DI7. The buffer connects DI0–DI7 to the odd bank (bank 1 and bank 3) of the memory array during 16-bit memory writes.

Overview

Refer to the Schematic Diagram (fold-in) and the Block Diagram (Pictorial 8) for the following discussion.

The dynamic memory card consists of these seven major circuits:

- The memory array itself, which can be populated as a 256K, 128K, or 64K array, where K = 1024.
- The address multiplexer, used to convert the 16-bit address bus to the 8-bit address required by the dynamic random access memory (RAM).
- The board select circuitry, used to select the correct 256K, 128K, or 64K of memory within the 16M address space.
- Refresh circuits.
- Parity circuits.
- The 8/16-bit data bus which can read and write 8-bit words to an 8-bit bus master or 16-bit words to a 16-bit bus master (with 128K or 256K installed).
- The address bus buffers.

CIRCUIT DESCRIPTION

Dynamic RAM

The Z-205 Card uses 6665/M5K4164 64K × 1-bit dynamic RAMs for the memory array. There is one IC per bit position, so eight ICs make up 64 kilobytes. For the first 64K bank, U87 corresponds to memory data bit 0 (MD0), and U80 corresponds to MD7 (memory data bit 7).

Refer to Pictorial 3, Page 9 for the following.

When the Card is configured for 64K, one set of RAMs make up the 64K address space:

U87–U80 = First 64K bank (Bank 0)

When the Card is configured for 128K, two sets of RAMs make up the 128K address space:

U87–U80 = First 64K even addressed bytes (Bank 0)
U69–U62 = First 64K odd addressed bytes (Bank 1)

When the Card is configured for 256K (normal configuration as supplied), four sets of RAMs make up the 256K address space:

U87–U80 = First 64K even addressed bytes (Bank 0)
U69–U62 = First 64K odd addressed bytes (Bank 1)
U78–U71 = Second 64K even addressed bytes (Bank 2)
U60–U53 = Second 64K odd addressed bytes (Bank 3)

To read or write to memory, the address circuits select the correct RAM location by placing the lower eight bits of the address onto memory address bit 0 through 7 (MA0–MA7). One of the four row address strobe (RAS) lines 0–3 latches this address into the RAM bank. The upper 8-bits of the address is placed onto MA0–MA7. After waiting a short time for the lines to settle, the column address strobe (CAS) line latches the byte at MA0–MA7 into the RAM bank.

Address Multiplexer

The address multiplexers consist of U33–U36. These ICs couple address bits 1 through 8 to MA0–MA7 during the RAS (row address strobe) time. They next pass, address bits 9 through 16 during CAS (column address strobe) time. They also couple the 8-bit refresh address to MA0–MA7 during refresh time.

If the Card is configured for only 64K, address bit 16 is jumpered out at J7 and replaced with address bit 0, permitting the memory array to read and write to only one bank of RAM.

NORMAL ACCESS

During a normal access, when the CPU starts to access the memory and a refresh cycle is **not** occurring (RCYC = "0"), the address select line SEL is logic 1. This couples the A inputs of the multiplexers to the Z outputs at MA0–MA7. U39, the RAM strobe generator, outputs a RAS (row address strobe) signal to the appropriate bank, causing the RAMs to latch in the lower eight address bits.

Later in the timing cycle, delay line output TAP1 goes from low to high, causing SEL to go high. This, in turn, passes the signals at the B inputs to the Z outputs of the multiplexers. The upper eight address bits are placed into MA0–MA7.

Next, TAP2 goes high. This causes the CAS (column address strobe) lines from U39 to be asserted, latching the upper eight address bits into the RAMs.

CIRCUIT DESCRIPTION

REFRESH

During a refresh cycle, RCYC goes high and the 8-bit refresh address is placed onto MA0–MA7.

Later in the timing cycle, TAP1 goes high, causing all four RAS (row address strobe) lines to go active, which then latch the refresh address into the RAMs.

If a memory access is attempted during a refresh cycle, the refresh arbitration circuitry inserts a wait state until the refresh and the memory access is completed.

Address Decode for Board Selection and I/O

BOARD SELECT

The board select circuitry consists of an 8-section DIP switch (SW2), a quad exclusive OR gate (U6), a four bit full-adder (U7), and an 8-input NAND gate (U8). The upper four address bits (A20 through A23) are tested against the four most significant bits from DIP switch SW2. If A20 through A23 match SW2 bits 4 through 7, all outputs are high from the XOR (exclusive OR) gate, thus determining what 1M byte block is desired.

The decode sequence now depends on the state of address bits A16 through A19. These address bits are inverted and then fed into the adder along with bits 0 through 3 from SW2. The sum of the two sets of inputs then determines if the board is to be selected. For example, an address to be decoded is found by adding the inverse of address lines A19 through A16 to SW bits 3 through 0. If the result is x11xx (x means don't care), then the board is selected, assuming J1 and J2 are configured for 256K (both jumpers open). If 128K decoding is desired, the result of the above arithmetic must yield x11x, (J1 closed, J2 open). For 64K decoding, x1111 must result, with J1 **and** J2 closed. The example figures shown below explain how memory board addressing is determined:

Address Selection

Switch settings for DIP switch SW2

ADDRESS BIT	POSITION NUMBER
A23	7
A22	6
A21	5
A20	4
A19	3
A18	2
A17	1
A16	0

CIRCUIT DESCRIPTION

SWITCH SETTING				ADDRESSES (HEX)		
SW2 POSITION No.				MEMORY CONFIGURATION		
3	2	1	0	256K	128K	64K
0	0	0	0	X00000–X3FFFF	X00000–X1FFFF	X00000–X0FFFF
0	0	0	1	X10000–X4FFFF	X10000–X2FFFF	X10000–X1FFFF
0	0	1	0	X20000–X5FFFF	X20000–X3FFFF	X20000–X2FFFF
0	0	1	1	X30000–X6FFFF	X30000–X4FFFF	X30000–X3FFFF
0	1	0	0	X40000–X7FFFF	X40000–X5FFFF	X40000–X4FFFF
0	1	0	1	X50000–X8FFFF	X50000–X6FFFF	X50000–X5FFFF
0	1	1	0	X60000–X9FFFF	X60000–X7FFFF	X60000–X6FFFF
0	1	1	1	X70000–XAFFFF	X70000–X8FFFF	X70000–X7FFFF
1	0	0	0	X80000–XBFFFF	X80000–X9FFFF	X80000–X8FFFF
1	0	0	1	X90000–XCFFFF	X90000–XAFFFF	X90000–X9FFFF
1	0	1	0	XA0000–XDFFFF	XA0000–XBFFFF	XA0000–XAFFFF
1	0	1	1	XB0000–XEFFFF	XB0000–XCFFFF	XB0000–XBFFFF
1	1	0	0	XC0000–XFFFFF	XC0000–XDFFFF	XC0000–XCFFFF
* 1	1	0	1	XD0000–XFFFFF, X00000–X0FFFF	XD0000–XEFFFF	XD0000–XDFFFF
1	1	1	0	XE0000–XFFFFF, X00000–X1FFFF	XE0000–XFFFFF	XE0000–XEFFFF
1	1	1	1	XF0000–XFFFFF, X00000–X2FFFF	XF0000–XFFFFF, X00000–X0FFFF	XF0000–XFFFFF
JUMPER CONFIGURATION			J1	OPEN	CLOSED	CLOSED
			J2	OPEN	OPEN	CLOSED
			J7	2–3, 4–5	2–3, 4–5	1–2, 3–4

X = Determined by SW2 positions 7, 6, 5, 4 as shown:

SW2 POSITION No.				
7	6	5	4	X(HEX)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

*NOTE: Addresses selected near the "top" of a 1 M byte block wraparound.

Address Configuration Examples

Example 1

To configure your Z-205 Card for 64K operation at addresses 0B0000–0BFFFF (Hex):

☐ Place programming jumpers on J1 and J2.

☐ Place programming jumpers on J7 pins 1–2 and 3–4.

☐ Set SW2 positions 0, 1, and 3 to the ON (1) position. Set all other positions to OFF (0).

CIRCUIT DESCRIPTION

Example 2
To configure your Z-205 Card for 128K operation at addresses 280000–29FFFF (Hex):

- ☐ Place a programming jumper on J1.
- ☐ Remove the programming jumper from J2 (if necessary).
- ☐ Place programming jumpers on J7 pins 2–3 and 4–5.
- ☐ Set SW2 positions 3 and 5 to ON (1). Set all others to OFF (0).

Example 3
To configure your Z-205 Card for 256K operation at addresses CC0000–CFFFFF (Hex):

- ☐ Remove programming jumpers from J1 and J2 (if necessary).
- ☐ Place programming jumpers on J7 pins 2–3 and 4–5.
- ☐ Set SW2 positions 2, 3, 6, and 7 to ON (1). Set all others to OFF (0).

BOARD SELECT (Continued)

When a memory address corresponds to the address space of the memory board, the board select (BSEL) line goes active, thus permitting memory accesses.

A memory read cycle is performed in the following manner:

The memory address appears at the inputs to address bus buffers U1–U4. The address is then decoded as described previously and BSEL goes active high.

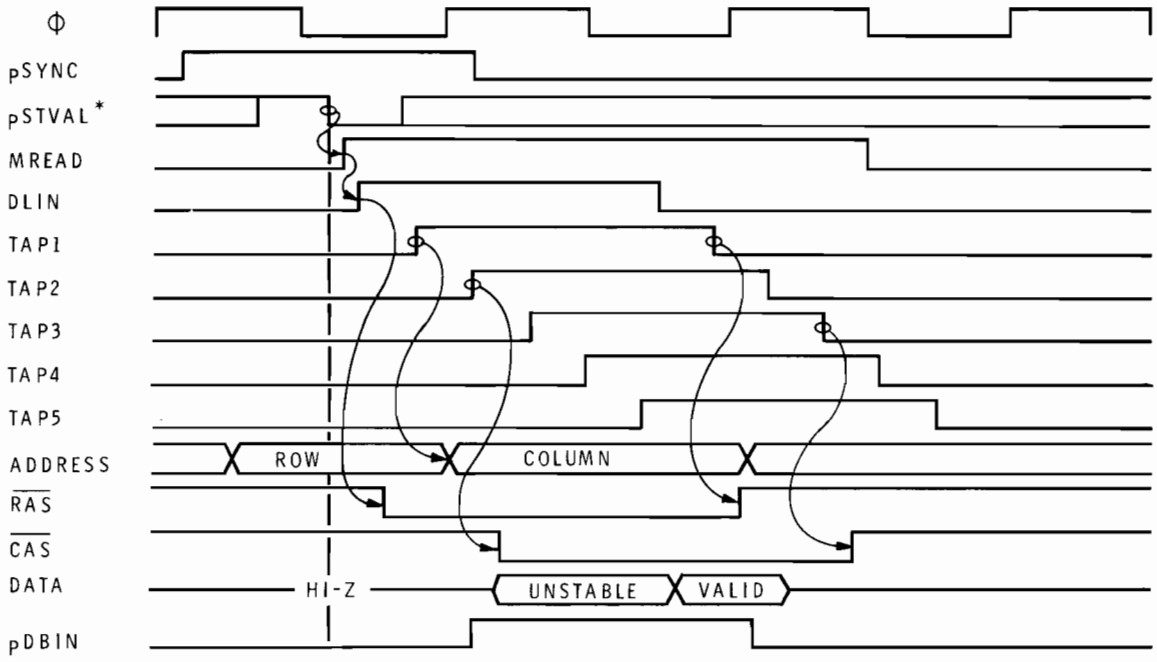
Status signal sMEMR indicates a memory read is to be performed. This signal is active high and appears at U10–11 along with BSEL at U10–10 to drive the read request (RDREQ) signal active high.

The bus cycle is started when pSTVAL* makes its high-to-low transition during pSYNC high. These signals appear at U10–1 and U10–13 respectively. The high-to-low transition of pSTVAL* clocks the cycle control flip-flop at U13–1 and U13–13. If RDEQ is high, then the output at U13–9 goes high after the transition of pSTVAL*, indicating the present bus cycle is for a memory read. At that time, MREAD goes high, then U12–3, then U40–3, the input to the delay line, (DLIN.) This signal, along with the outputs from the delay line, TAP1 through TAP4, is fed into the memory array strobe generator, U39. This PAL generates the appropriate RAS, SEL, and CAS signals to latch the address location into the RAM. RAS asserts when the delay line input (DLIN) and TAP1 are high. SEL asserts when TAP1 is high, and CAS asserts when TAP2 and TAP3 are high.

After CAS goes active, data from the RAM chips is stable at the data outputs after the access time delay. This data passes through one of the transparent latches at U47, U48, or U49 and is latched on the falling edge of the internally generated memory read (MREAD) signal. MREAD is returned to its inactive state by the clear memory cycle (CLRMCYC) pulse from U39–19. This signal is an active low pulse which is active when TAP1 goes low, but while TAP2 is still high. CLRMCYC is used to reset the cycle control flip-flop U13.

CIRCUIT DESCRIPTION

At this time, the data is present on the S-100 bus and is held valid until pDBIN goes inactive.



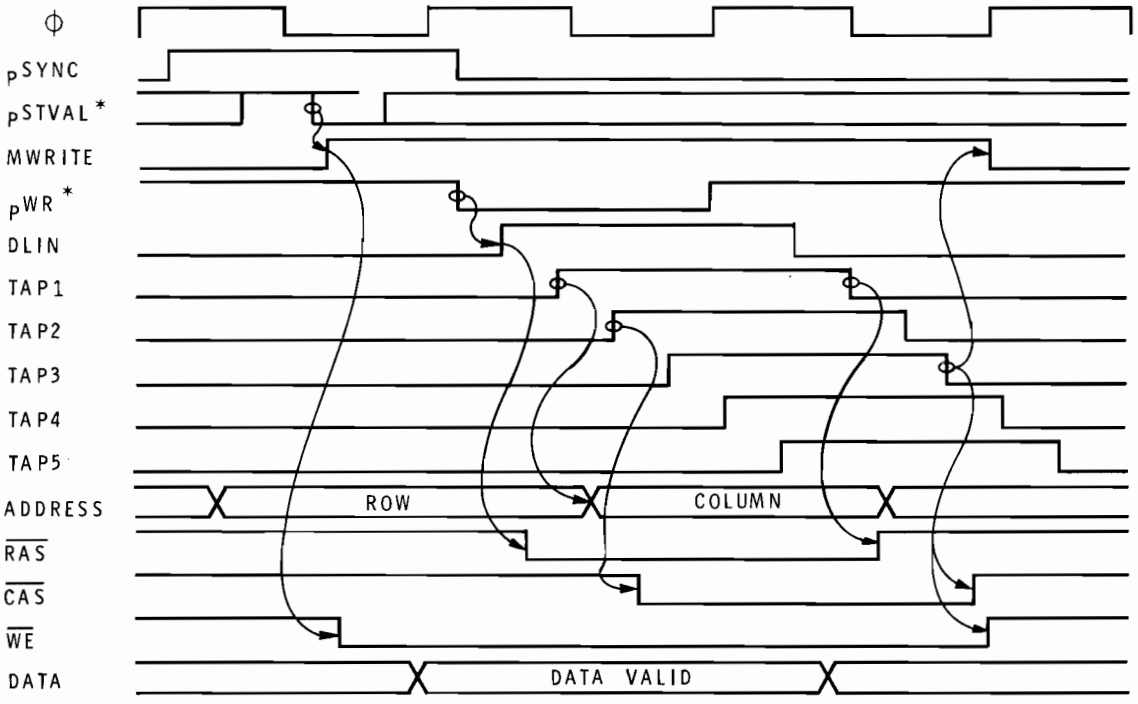
Read cycle timing in Z-100 systems.

PICTORIAL 10

CIRCUIT DESCRIPTION

The memory write cycle is similar to the memory read cycle with the exception that when pSTVAL* makes its transition and sets U13–5 high, the memory array is **not** accessed until pWR* goes active, indicating that data is valid on the bus and ready to be written.

When pWR* goes active, PWR makes a low-to-high transition, clocking U14–3 and initiating the write sequence.



Write cycle timing in Z-100 systems.

PICTORIAL 11

CIRCUIT DESCRIPTION

I/O SELECT

The I/O select circuitry consists of an eight-position DIP switch, SW1, and address comparator U5.

The positions on the DIP switch correspond to the eight least significant address lines. Address line A0 through A7 correspond to SW1 bits 0 through 7 respectively. Thus, you can select any one of 256 possible address locations as the I/O port address.

When an I/O instruction is issued by the CPU, address lines A0 through A7 are compared with the address selected by SW1 at U5. If an input instruction is being executed and if the addresses are the same, the output from U5 (DEVSEL) goes active low and the data appearing on data lines DO0–DO7 is written into U150.

If an output instruction is being executed and if the addresses are the same, the DEVSEL goes active low and the output from U118, pin 11 appears on data input line DI0.

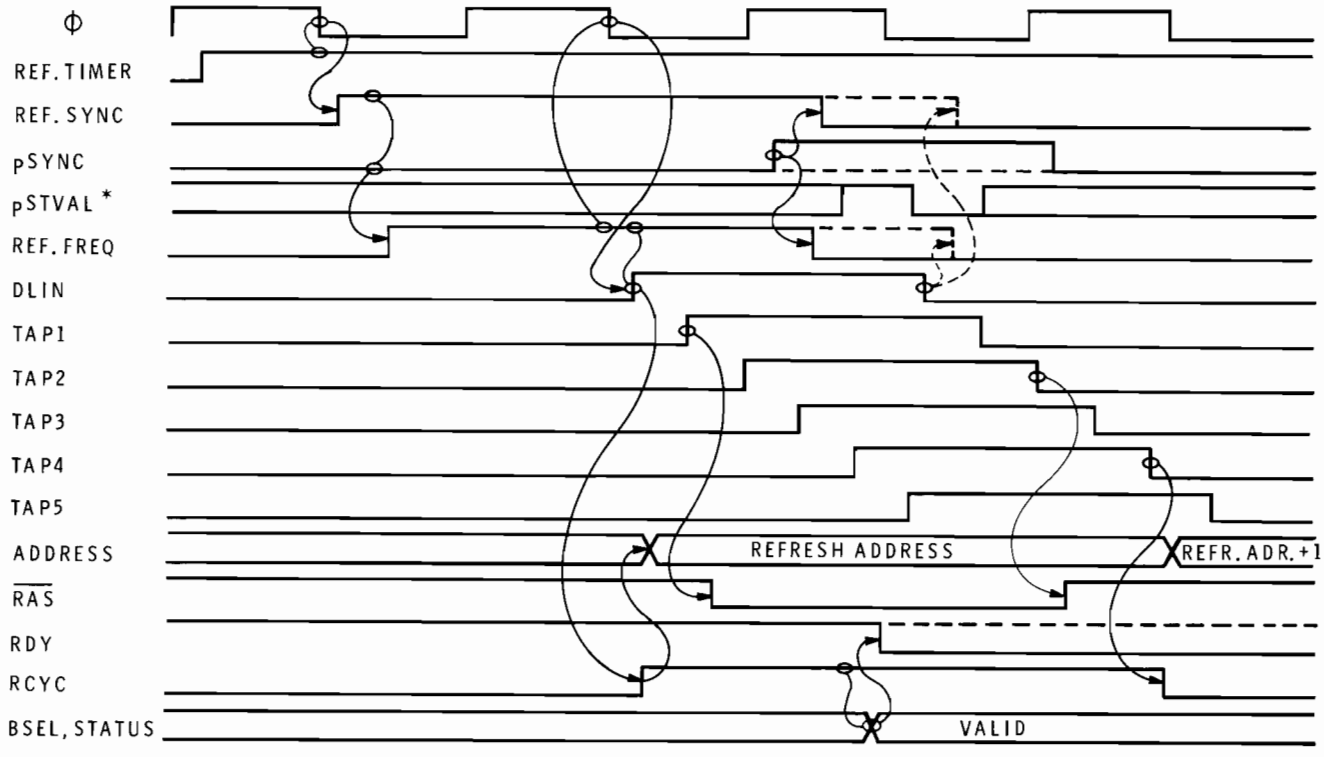
Refresh Circuits

The refresh circuits consist of a refresh clock U25, three flip-flops for synchronization and control (U23, U51, and U21), and a PAL, U28, for generating refresh request signals.

These circuits refresh the memory when the CPU is not accessing them. Sometimes a refresh is requested when the memory is being used. In this case, the refresh circuits contain arbitration logic to resolve any contentions which may arise during refresh.

CIRCUIT DESCRIPTION

Each row of the dynamic RAMs must be refreshed about every two milliseconds for 128-row devices, or about every four milliseconds for 256-row devices. Therefore, refresh clock U25 outputs a high signal every 15 microseconds to U23–3 to request a refresh. The signal is then synchronized with the falling edge of the phi clock from the bus at U51–5, and generates the refresh synchronization (REFSYNC) pulse.



Refresh cycle timing.

PICTORIAL 12

CIRCUIT DESCRIPTION

ARBITRATION

The REFSYNC signal is then tested against memory read and write signals, as well as the pSYNC signal, to insure that a refresh cycle will not begin at the same time a memory cycle starts. If the conditions allow a refresh to occur, REFREQ goes active and requests a refresh at U51–12. After the next falling edge of the phi clock from the bus, the output from U51–9 is passed to delay line U20–1 via U12–13, U12–2 and U40. When the input to the delay line goes high, U21 is clocked and the output identifies the present cycle as a refresh cycle. The input to delay line (DLIN) causes the address multiplexers to pass the refresh address to the RAM array. Then TAP1 causes the refresh address to be strobed into the memories with the RAS signal present in all four banks.

As we mentioned previously, a memory refresh cycle is inhibited during pSYNC active and when a read or write cycle is being performed. If MREAD, MWRITE, or PSYNC are active at U28–1, U28–2, or U28–4, respectively, REFREQ is held low and U51–9 stays low after the clocking edge of phi passes. In this way, a refresh cycle cannot start during a memory cycle or at the same time as a memory cycle.

If a refresh cycle is in progress and the board is accessed for a read or write, the RDY line is pulled low for the duration of the refresh cycle as well as during the read or write cycle until the memory access is completed. When the RDY line is allowed to return to the high state, data which has been read will be ready on the bus, or will have been written if a write cycle was initiated.

WAIT STATES DURING REFRESH

A refresh cycle begins with RCYC becoming active. U21–10 goes low, setting U21–9 high. If a read or write cycle is occurring, RDREQ or WRREQ are high at U12–5 or U12–4. This then sets SMCYC high which, in turn, causes U17–11, RDY, to go low, and the CPU will insert wait states until the RDY line returns high. The output from U21–9 is reset to its low state when MEMWAIT, whose logic equation is (MREAD + MWRITE), goes low and TAP5 returns to its inactive state, thereby clocking U21–11. This happens only at the end of a memory cycle, which assures that the data has been either read or written by the time RDY returns high.

When this board is used in systems with bus clocks in excess of 5 MHz or with fast fetch cycles, one or more wait states is required. A user-selectable wait state generator has been added to permit use of the Z-205 Card in these systems.

WAIT STATES DURING NORMAL ACCESS

One, two, or three wait states can be jump selected at J3, J4, or J5 respectively. The circuitry that performs this function consists of U24, the jumpers, and U17.

At the beginning of a bus cycle, PSYNC goes active. This resets the flip-flops inside U24, and the outputs at U24–6, U24–7, and U24–14 all go high. If the board is about to be accessed for a read or write, SMCYC at U17–10 goes high and the RDY signal goes low at U17–8. The Central Processor Unit (CPU) will then insert wait states into the bus cycle until a low level appears at U17–9. This will occur after phi clocks a low level to the selected output of U24.

CIRCUIT DESCRIPTION

Parity Circuit

The parity circuit consists of U42, U43, U61, U70, U79, and U88.

This circuit maintains the parity status for each byte in the 256K of RAM. If a memory location should not match its parity bit, the parity circuit sends an error signal to the CPU. Also, a bit is set in the status latch to indicate an error. The latch can be interrogated by I/O instructions to determine which board is at fault in multiboard systems.

U61, U70, U79, and U88 are 64K by 1 bit RAMs and store one bit of parity information for each address location of RAM. These RAMs are addressed by RAS and CAS in the same way as the other RAMs. However, the write enable lines are gated through U118, so that the parity RAMs can be written to independently, and the data transfers take place through U42 and U43 instead of the data bus. U42 and U43 are 9-bit odd parity generators and even parity checkers that process and maintain the parity status.

During a memory write, the data written into RAM is present at pins 8–13 and 1–2 of U42 and U43. Pin 14 of each parity RAM is at a high impedance state so U42–4 and U43–4 are at logic 1 through pull-up resistors R4 and R5 respectively.

The following truth table shows the levels of the odd and even outputs for the number of high inputs:

NUMBER OF INPUTS THAT ARE HIGH.	OUTPUTS EVEN	ODD
0, 2, 4, 6, 8 (even number)	H	L
1, 3, 5, 7, 9 (odd number)	L	H

So, if there is an odd number of high bits in the data byte, the logic 1 on U42–4 or U43–4 makes it even. U42–6 or U43–6 responds by going low and a logic zero is written into the addressed RAM location. Later, when that particular RAM location is read, the odd data byte is read along with the logic zero from the parity RAM and the total number of high bits still remains zero.

If there is an even number of data bits in the data byte, the logic 1 at U42–4 or U43–4 makes it odd. U42–2 or U43–6 respond, going low, and a logic 1 is coupled into the addressed RAM. Later, if that same memory location is read, the even data byte is read along with the logic 1 from the parity RAM and the total number of high bits is odd.

The parity circuit will only allow an odd number of high bits to be stored in a memory location. If an even number of high bits is read, an error has occurred.

The RAMs that store the parity bits can be enabled and disabled with the "no parity" (NOPAR) line. The NOPAR line at U118–2 is normally low. This can be brought up to high to force a parity error by disabling the parity RAM during a write sequence. Then, when the memory is read, an error will occur, provided that the byte that was written was of opposite parity to the stored parity RAM bit. You write a logic 0 to data bit D4 of the input port on the logic card to force the NOPAR line high. This feature is used to test the error-detection circuitry.

The even-parity outputs go to U12–9 and U12–10. These are coupled to U40–12. U40–13 is low except at the end of a read cycle, thus preventing a false error signal from being generated during a write or refresh cycle.

CIRCUIT DESCRIPTION

During a memory read, data output from the addressed RAMs are present at the inputs of U42 and or U43. The corresponding parity bits from U61, U70, U79, or U88 are placed on U43–4 or U42–4. If the bit pattern that was previously written into data RAM has not changed, the total number of logic 1 bits is always odd. Therefore, U42–5 and U43–5 remain low, which is the nonerror condition.

If, due to a chip failure, the bit count totals an even number, U43–5 or U42–5 go high. When the memory read cycle is nearly complete, the error enable (ERREN) line at U40–13 goes high, causing U23–11 to clock a high level out at U23–9, asserting the ERROR* line at U17–6. This generates an error interrupt to the CPU. When KILPAR is asserted low, U23 is cleared, preventing a parity error interrupt. To assert KILPAR, set data bit D5 to zero and output it to the I/O port on the Z-205 Memory Card.

Eight-bit and 16-bit Data Transfer Capability

The data bus buffers, U44–U49 and with data bus controllers U52, make up the data multiplexing network through which the CPU can access the RAM array in either the 8-bit bytes or the 16-bit words. The size and direction of the data transfer is controlled by a single chip, U52. This 8/16-bit data transfer controller responds to the conditions of address line A0, SIXTN*, pDBIN, and MWRITE, the on-board memory write signal. The read and write signals, pDBIN and MWRITE, identify the direction of data flow in or out of the RAM array, respectively. The status signal, SIXTN, determines if a 16-bit data transfer is desired, and A0 determines if an odd or even byte is to be read from or written to for 8-bit transfers. If A0 is low, the byte is considered even. If A0 is high, the byte is odd.

The following table shows how U52 enables U44 through U49:

MEMORY CYCLE TYPE	DATA BUFFER(S) ENABLED
Even byte read	U47
Even byte write	U45
Odd byte read	U48
Odd byte write	U44
Word read	U48, U49
Word write	U45, U46

The memory array is divided into two-odd banks and two-even banks. The memory board appears as either a 256K **byte** card when used in an 8-bit system, or as a 128K **word** card when used with a 16-bit system.

CIRCUIT DESCRIPTION

Data lines DO0–DO7 (DATA0–DATA7) are connected to the inputs of U44 and U45 so that 8-bit data can be written to either the odd or even bank. U45 also provides data passage to the even bank during a 16-bit write. During a 16-bit read, data from the even bank passes through U49 and onto data lines DATA0–DATA7 (DO0–DO7).

Data lines DI0–DI7 (DATA8–DATA15) are connected to the outputs from U47 and U48 so that 8-bit data can be read from either the odd or even bank. U48 also provides data passage from the even bank during a 16-bit read. During a 16-bit write, data from DATA8–DATA15 (DI0–DI7) passes through U46 and into the even bank.

NOTE: A Z-205 Card configured for 64K (1 bank only) should not be used in a system with only 16-bit data capability. The system must use the sXTRQ* (pin 58, S-100 Bus) line.

Address Line Buffers

The address bus buffers consist of two 74S240 inverting Schottky type buffers and two 74LS244 noninverting, low-power, Schottky type buffers. These devices act as bus receivers for the S-100 address and control signals.

IN CASE OF DIFFICULTY

The Z-205 Dyanmic RAM Card is considered to be too complex for user servicing. If your Card does not operate properly, first refer to the problem — resolution chart below. If the problem persists, return the Card to one of the repair centers listed in the documentation you received with your Z-100 Computer.

PROBLEM	RESOLUTION
System responds with parity or bus error.	1. Check switch SW1 for correct settings per the Configuration section of this manual.
System fails to operate.	1. Check J6 and J7 for proper programming jumper installation. 2. Check switches SW1, SW2 settings. 3. Ensure that the Card is fully seated in the card edge connector. 4. Inspect all IC packages for proper seating in sockets.
System fails Initial Test; Displays all "FF" in place of data shown as screen display. Display is other than expected.	1. Check switch settings to ensure proper configuration. Code "FF" display tells you that the bank under test is not addressed or not present. 2. Switch SW2, in wrong position, causing errors in display. Repeat Initial Test. 3. If problem persists, return your Z-205 Card to the nearest service center with a description of the problem, and the system it was used in.

REPLACEMENT PARTS LIST

Circuit Comp. No.	Part No.	Description
RESISTORS		
R1, R6–R8, R101	6-102-12	1000 ohms
R2, R3	6-682-12	6800 ohms
R4, R5, R9, R10	6-103-12	10 kohms
RP1, RP4, RP5, RP101, RP102	9-119	10 k R-pack
RP2, RP3, RP6, RP7	9-126	33 Ohm R-pack
CAPACITORS		
C1	21-769	0.01 μF
C2, C3	21-763	330 pF
C4	29-44	0.001 μF
C5	25-180	2.2 μF, 50 V
C6, C7	25-820	10 μF, 10 V
C8–C66	21-786	0.1 μF
MISCELLANEOUS		
U20	41-10	200 ns Delay line
INTEGRATED CIRCUITS		

See "Semiconductor Identification."

SEMICONDUCTOR IDENTIFICATION

This section is divided into two parts. The "Component Number Index" relates circuit component numbers to Heath part numbers. The "Part Number Index" relates part numbers to manufacturers' part numbers, as well as providing lead configuration drawings for each part.

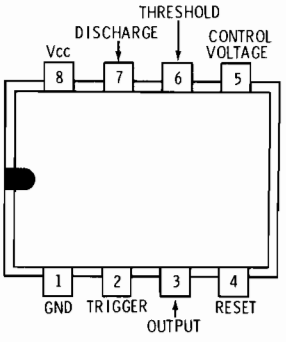
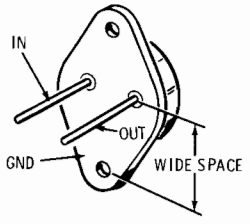
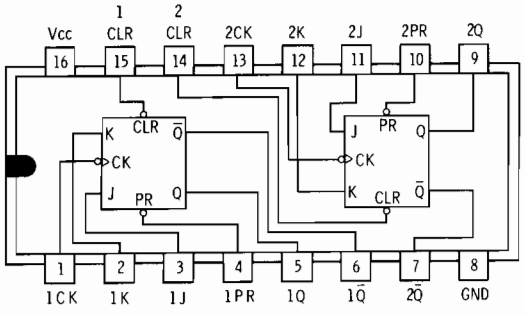
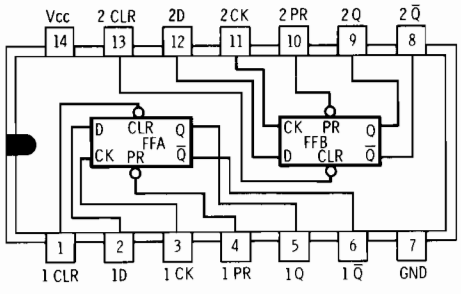
Component Number Index

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U1	443-753
U2, U3	443-791
U4	443-753
U5	443-971
U6	443-915
U7	443-855
U8	443-732
U9	not used
U10	443-1078
U11	443-755
U12	443-975
U13	443-42
U14	443-730
U15	442-702
U16	not used
U17	443-898
U18	not used
U19	not used
U20	41-10
U21	443-900
U22	not used
U23	443-730
U24	443-752
U25	442-53
U26	not used
U27	not used
U28	444-147

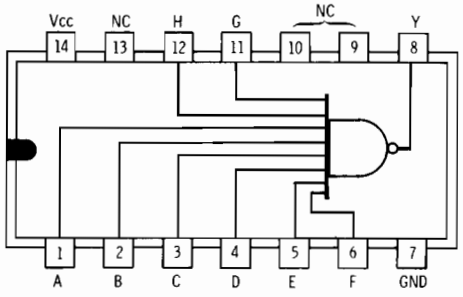
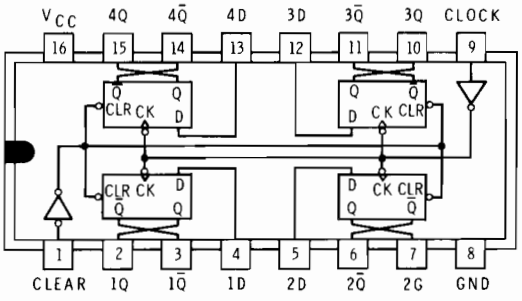
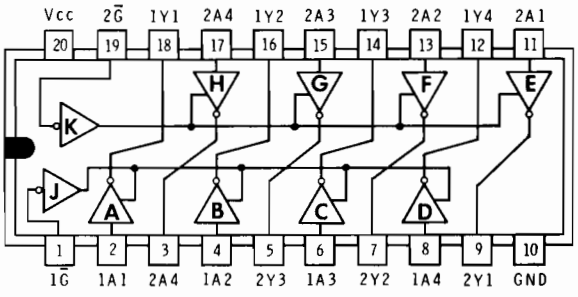
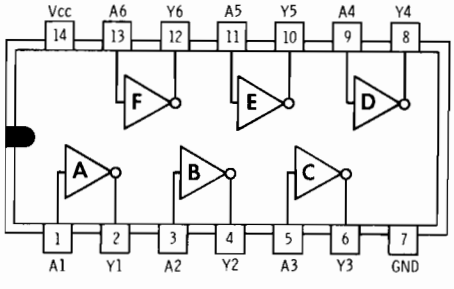
CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U29	not used
U30	not used
U31	not used
U32	443-973
U33–U36	443-1100
U37	not used
U38	not used
U39	444-144
U40	443-976
U41	not used
U42–U43	443-1001
U44–U46	443-791
U47–U49	443-1070
U50	not used
U51	443-730
U52	444-145
U53–U88	443-970
U89–U117	not used
U118	443-857
U119–U149	not used
U150	443-805

SEMICONDUCTOR IDENTIFICATION

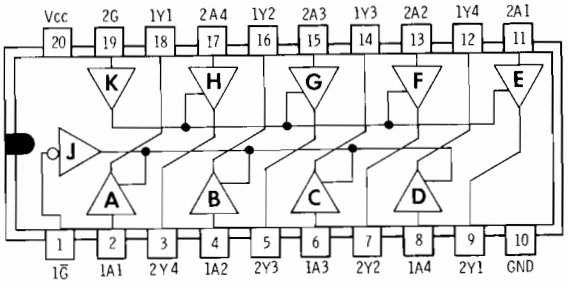
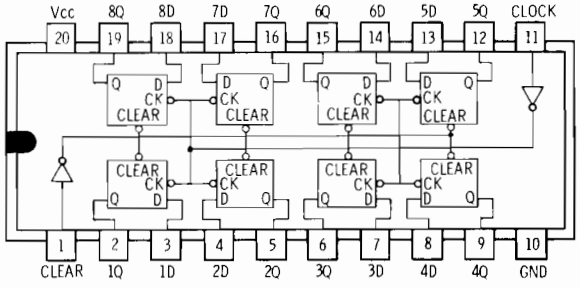
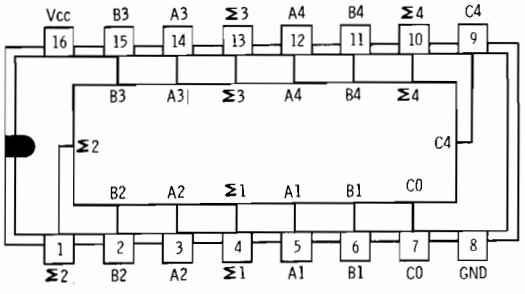
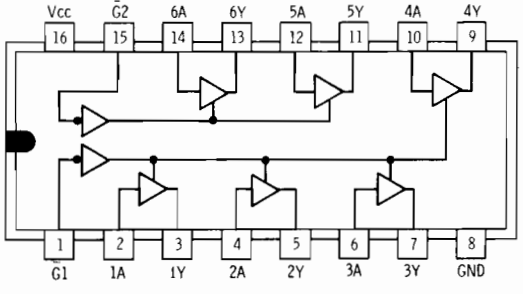
Part Number Index

Part Number	May Be Replaced With	Description	Identification
442-53	NE555	Timer	
442-702	LM323	Voltage regulator	
443-42	74S112	Dual J-K, negative trigger flip-flop	
443-730	74LS74	Dual D flip-flop	

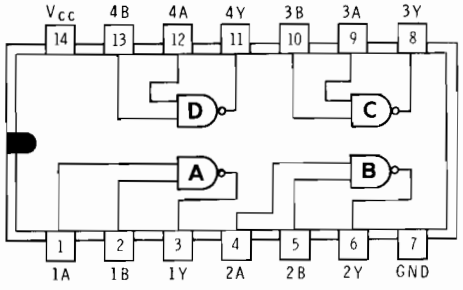
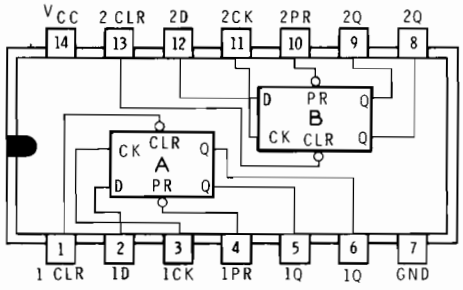
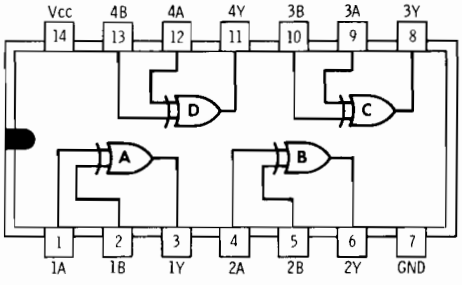
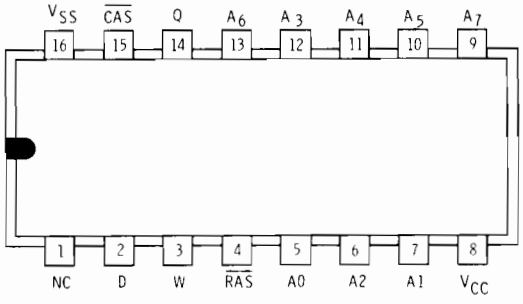
SEMICONDUCTOR IDENTIFICATION

Part Number	May Be Replaced With	Description	Identification
443-732	74LS30	8-input NAND	
443-752	74LS175	Quad D-type flip-flop	
443-753	74S240	Octal buffer 3-state outputs	
443-755	74LS04	Hex buffer	

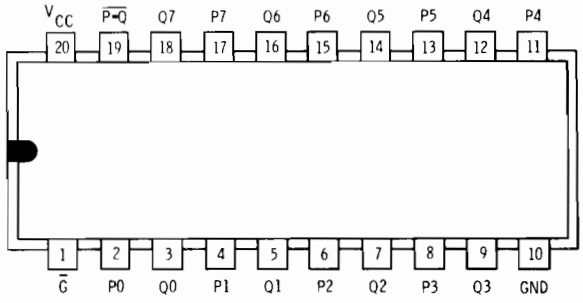
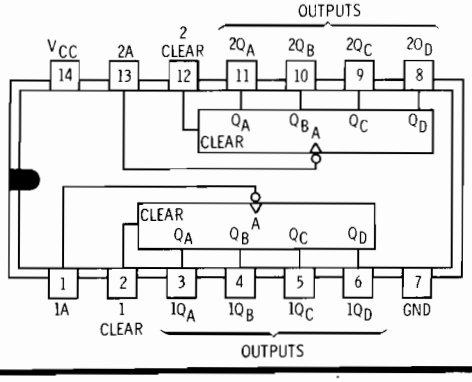
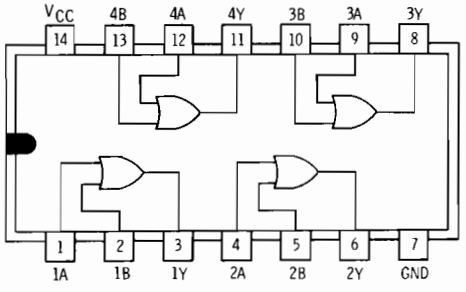
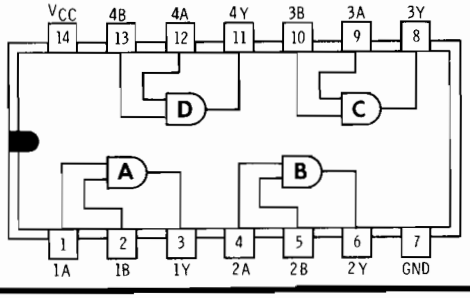
SEMICONDUCTOR IDENTIFICATION

Part Number	May Be Replaced With	Description	Identification
443-791	74LS244	Noninverting 3-state output octal buffers	
443-805	74LS273	Octal D flip-flop with clear	
443-855	74LS283	Adder	
443-857	74LS367A	Hex bus driver	

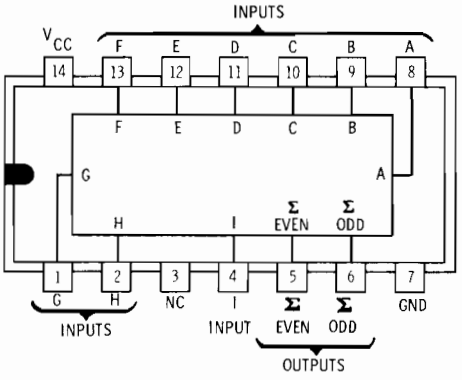
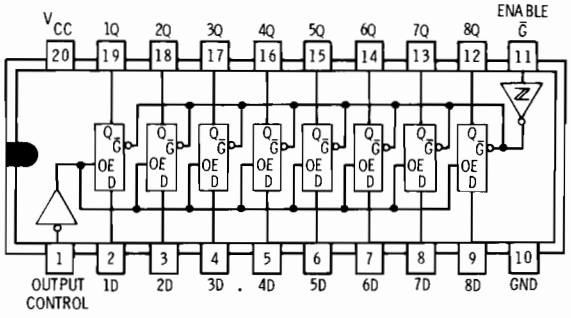
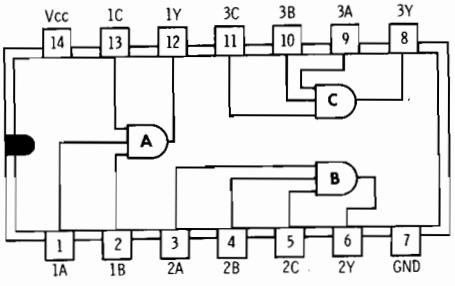
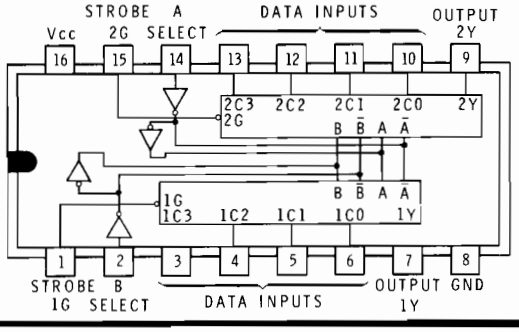
SEMICONDUCTOR IDENTIFICATION

Part Number	May Be Replaced With	Description	Identification
443-898	74S38	Quad 2-Input NAND Open Collector Buffer	
443-900	74S74	Dual D flip-flop	
443-915	74S86	Quad 2-input exclusive OR	
443-970	200ns 64K = 1DRAMs MCM6665 M5K4164	64K RAM	

SEMICONDUCTOR IDENTIFICATION

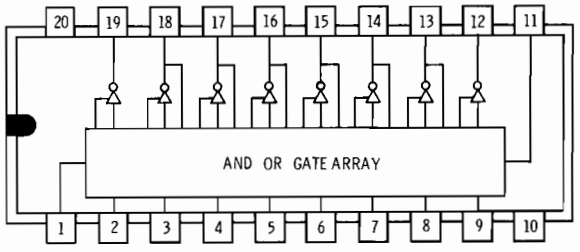
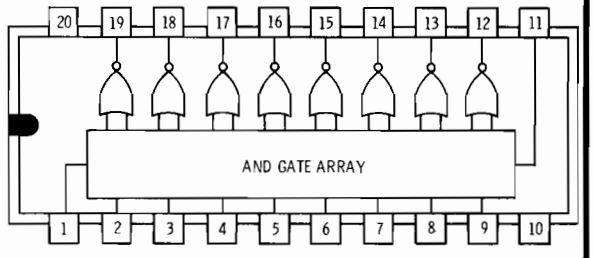
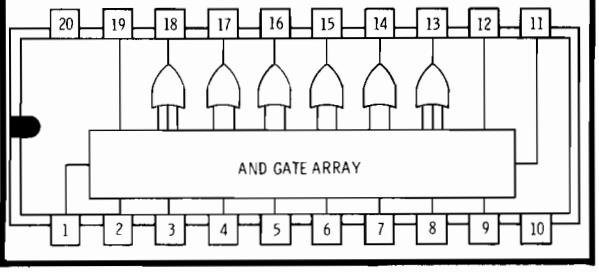
Part Number	May Be Replaced With	Description	Identification
443-971	25LS2521	8-Bit = TO comparator	
443-973	74LS393	Dual 4-bit binary/decade counter	
443-975	74S32	Quad 2-input Positive OR gate	
443-976	74S08	Quad 2-input Positive AND gate	

SEMICONDUCTOR IDENTIFICATION

Part Number	May Be Replaced With	Description	Identification
443-1001	74LS280	9-bit odd/even parity generator checker	
443-1070	74ALS573	Octal D-type transparent latch	
443-1078	74ALS11	Triple 3-input AND gate	
443-1100	74F153	Dual 4-input MUX	

SEMICONDUCTOR IDENTIFICATION

Integrated Circuits (Cont'd.)

Part Number	May Be Replaced With	Description	Identification
444-144	PAL 16L8* OR HAL 16L8	Programmable Array Logic	
444-145	PAL 10L8* OR HAL 10L8	Programmable Array Logic	
444-147	PAL 12L8* OR HAL 12L8	Programmable Array Logic	

*Available only from Heath/ZDS.

PAL Equations

PAL16L8
444-144
Z-205 MEMORY STROBE GENERATOR

DLIN TAP1 TAP2 TAP3 TAP4 /PA17 SIXTN PA0 RCYC GND
PHANTOM /CAS0 /CAS1 /RAS0 /RAS1 /RAS2 /RAS3 /SEL /CLRMCYC VCC

IF (VCC) /RAS3 = RCYC*TAP1 + /RCYC*PA17*PA0*DLIN + /RCYC*PA17*SIXTN*DLIN
+ RCYC*TAP2 + PA17*PA0*TAP1 + PA17*SIXTN*TAP1

IF (VCC) /RAS2 = RCYC*TAP1 + /RCYC*PA17*/PA0*DLIN + /RCYC*PA17*SIXTN*DLIN
+ RCYC*TAP2 + PA17*/PA0*TAP1 + PA17*SIXTN*TAP1

IF (VCC) /RAS1 = RCYC*TAP1 + /RCYC*/PA17*PA0*DLIN + /RCYC*/PA17*SIXTN*DLIN
+ RCYC*TAP2 + /PA17*PA0*TAP1 + /PA17*SIXTN*TAP1

IF (VCC) /RAS0 = RCYC*TAP1 + /RCYC*/PA17*/PA0*DLIN + /RCYC*/PA17*SIXTN*DLIN
+ RCYC*TAP2 + /PA17*/PA0*TAP1 + /PA17*SIXTN*TAP1

IF (VCC) /CAS1 = /RCYC*TAP2/PHANTOM + /RCYC*TAP3*/PHANTOM

IF (VCC) /CAS0 = /RCYC*TAP2/PHANTOM + /RCYC*TAP3*/PHANTOM

IF (VCC) /SEL = /RCYC*TAP1

IF (VCC) /CLRMCYC = /RCYC*TAP2*TAP3

SEMICONDUCTOR IDENTIFICATION

PAL Equations

PAL10L8
444-145
8/16 BIT CONTROL SIGNAL GENERATOR

PA0 SIXTN /PDBIN MWRITE PHANTOM BSEL RDREQ /SOUT /DEVSEL GND
/SINP DOUTLB DOUTHB LBDIN DINHB LBDOUT /INSEL /OUTSEL HBDIN VCC

HBDIN = PDBIN*/PHANDOM*SIXTN*BSEL*RDREQ + PDBIN*/PHANTOM*BSEL*RDREQ*/SIXTN*PA0

DINHB = MWRITE*SIXTN*/PHANTOM

LDBIN = PDBIN*RDREQ*BSEL*/PHANTOM*/SIXTN*/PA0

DOUTHB = MWRITE*/SIXTN*PA0*/PHANTOM

DOUTLB = MWRITE*SIXTN*/PHANTOM + MWRITE*/SIXTN*/PHANTOM*/PA0

LBDOUT = PDBIN*/PHANTOM*BSEL*RDREQ*SIXTN

/OUTSEL = SINP*PDBIN*DEVSEL

/INSEL = SOUT*DEVSEL

PAL Equations

PAL12H6
444-147
Z-205 MEMORY CYCLE CONTROLLER

MREAD MWRITE REFSYNC /PSYNC TAP1 TAP2 TAP3 TAP4 /DEVSEL GND
PWR /SOUT /CLRFSH REFREQ MEMWAIT /CLRCYC ERREN INPUT RCYC VCC

/CLRFSH = TAP1 + /TAP4 + /RCYC

REFREQ + REFSYNC*/PSYNC*/MREAD*/MWRITE + RCYC

/CLRCYC = TAP3 + /TAP4

ERREN = MREAD*/TAP2*TAP3

INPUT = DEVSEL*SOUT*PWR

MEMWAIT = MREAD + MWRITE

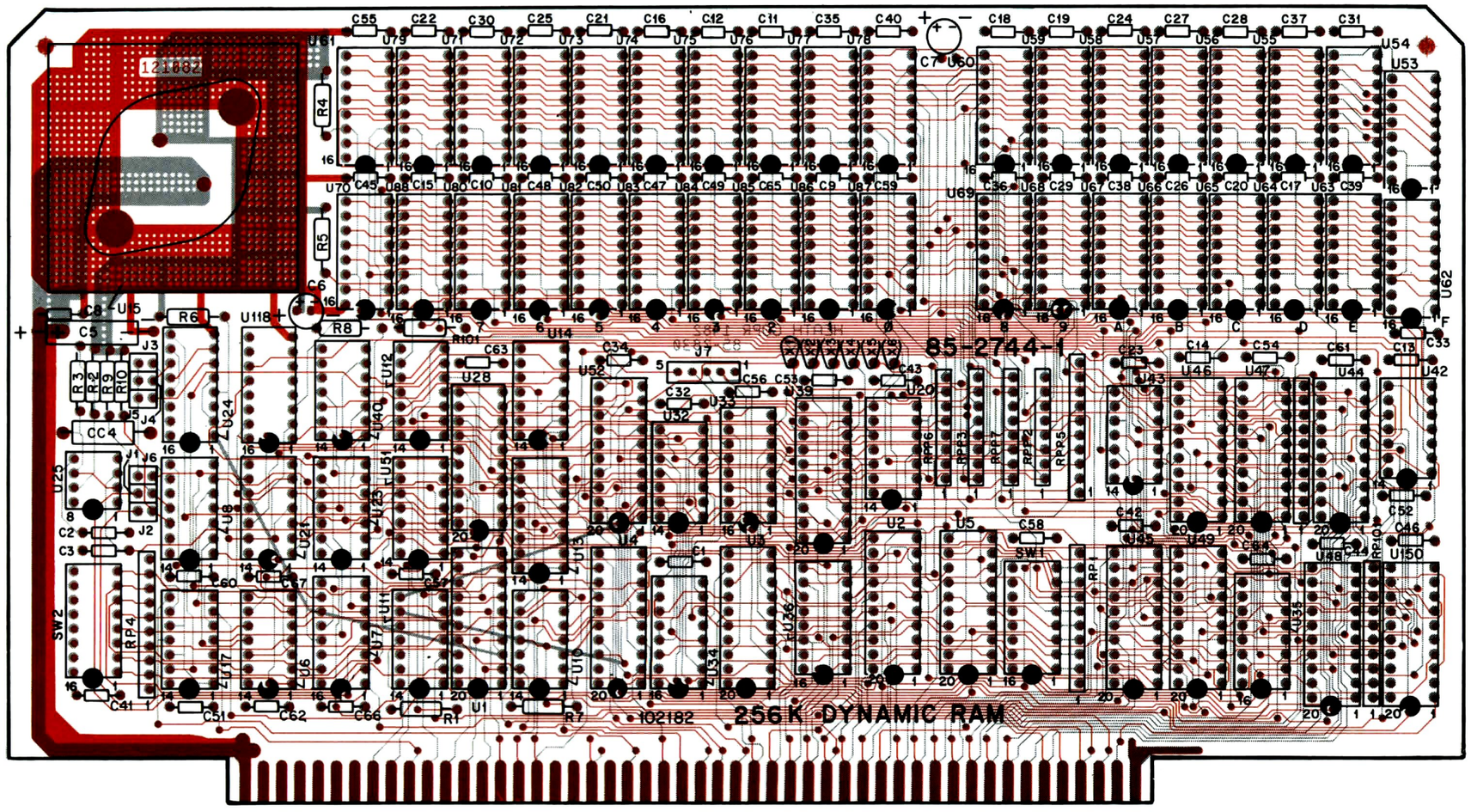
CIRCUIT BOARD X-RAY VIEW

NOTE: To find the PART NUMBER of a component:

A. Find the circuit component number (R111, C101, etc.) on the "X-Ray View" (fold-out from this Page).

B. Locate this same number in the "Circuit Component Number" column of the "Replacement Parts List".

C. Adjacent to the circuit component number, you will find the PART NUMBER and DESCRIPTION.



Circuit Board X-Ray View

APPENDIX A

S-100 Bus Pin Definitions

PIN NO.	SIGNAL/TYPE	ACTIVE LEVEL
1	+8 Volts (B)	
15	A18 (M)	H
16	A16 (M)	H
17	A17 (M)	H
20	GND (B) 0 Volts Line	
24	ϕ (B)	H
25	pSTVAL* (M)	L
29	A5 (M)	H
30	A4 (M)	H
31	A3 (M)	H
32	A15 (M)	H
33	A12 (M)	H
34	A9 (M)	H
35	DO1 (M)/DATA1 (M/S)	H
36	DO0 (M)/DATA0 (M/S)	H
37	A10 (M)	H
38	DO4 (M)/DATA4 (M/S)	H
39	DO5 (M)/DATA5 (M/S)	H
40	DO6 (M)/DATA6 (M/S)	H
41	DO12 (M)/DATA10 (M/S)	H
42	DO13 (M)/DATA11 (M/S)	H
43	DO17 (M)/DATA15 (M/S)	H
45	sOUT (M)	H
46	sINP (M)	H
47	sMEMR (M)	H
50	GND 0 Volts Line	

APPENDIX A

PIN NO.	SIGNAL/TYPE	ACTIVE LEVEL	
51	+8 Volts (B)		
58	sXTRQ*	L	
59	A19 (M)	H	
60	SIXTN* (S)	L	O.C.
61	A20 (M)	H	
62	A21 (M)	H	
63	A22 (M)	H	
64	A23 (M)	H	
67	PHANTOM* (M/S)	L	O.C.
70	GND (B) 0 Volts Line		
72	RDY (S)	H	O.C.
76	pSYNC (M)	H	
77	pWR* (M)	L	
78	pDBIN (M)	H	
79	A0 (M)	H	
80	A1 (M)	H	
81	A2 (M)	H	
82	A6 (M)	H	
83	A7 (M)	H	
84	A8 (M)	H	
85	A13 (M)	H	
86	A14 (M)	H	
87	A11 (M)	H	

APPENDIX A

PIN NO.	SIGNAL/TYPE	ACTIVE LEVEL	
88	DO2 (M)/DATA2 (M/S)	H	
89	DO3 (M)/DATA3 (M/S)	H	
90	DO7 (M)/DATA7 (M/S)	H	
91	D14 (M)/DATA12 (M/S)	H	
92	D15 (M)/DATA13 (M/S)	H	
93	D16 (M)/DATA14 (M/S)	H	
94	D11 (M)/DATA9 (M/S)	H	
95	D10 (M)/DATA8 (M/S)	H	
97	sWO* (M)	L	
98	ERROR* (S)	L	O.C.
99	POC* (B)	L	
100	GND (B) 0 Volts Line		

APPENDIX B

65 536 Bit Dynamic RAM

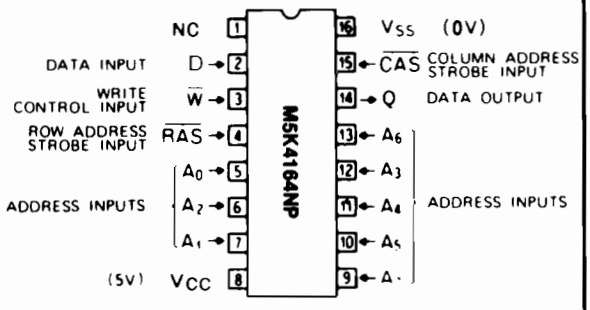
The following data sheet is reprinted with the permission of MITSUBISHI ELECTRIC COMPANY.

APPENDIX B

DESCRIPTION

This is a family of 65 536-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicongate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pints to the standard 16-pin package configuration and an increase in system densities. The M5K4164NP operates on a 5V power supply using the on-chip substrate bias generator.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FEATURES

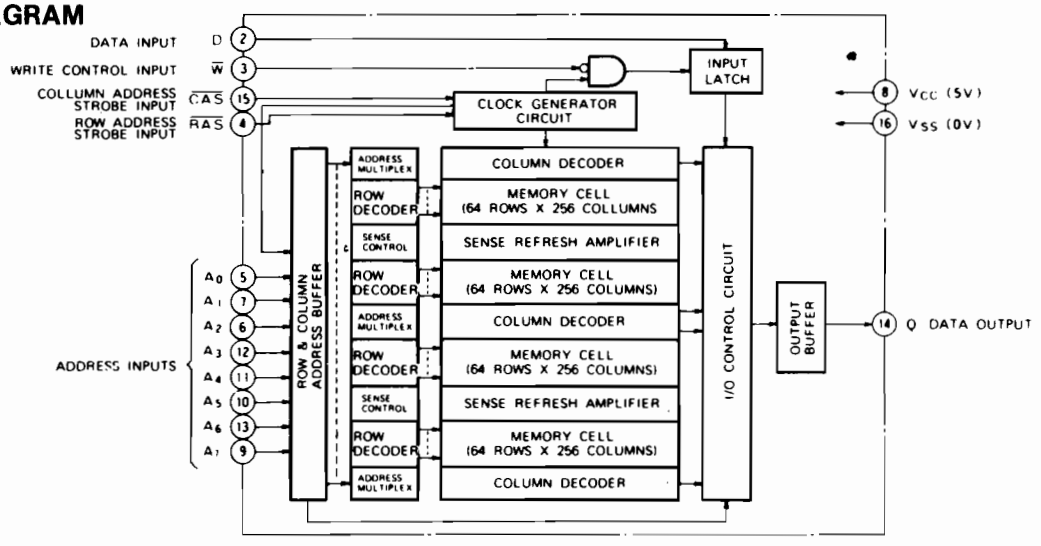
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K4164NP-15	150	260	200
M5K4164NP-20	200	330	170

- Standard 16-pin package
- Single 5V ± 10% supply
- Low standby power dissipation: 28.0mW (max)
- Low operating power dissipation: 275mW (max)
- Unlatched ouput enables two-dimensional chip selection and extended page boundary
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capaciatance and are directly TTL-compatible
- Output is three-stage and directly TTL-compatible
- 128 refresh cycles every 2ms (16K dynamic RAMs M5K4116P, S compatible)
- CAS controlled output allows hidden refresh.
- Output data can be held infinitely by $\overline{CAS}$.
- Interchangeable with intel's 2164 and Motorola's MCM 6665 in pin configuration.

APPLICATION

- Main memory unit for computers.

BLOCK DIAGRAM



APPENDIX B

FUNCTION

The M5K4164NP provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are show in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Page mode identical except refresh is NO
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	APD	DNC	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open

SUMMARY OF OPERATIONS

Addressing

To select one of the 65536 memory cells in the M5K4164NP the 16-bit address signal must be multiplexed into 8 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 8 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 8 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)}$ max ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transistons of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5K4164NP is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K4164NP, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2. Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

APPENDIX B

3. Two Method of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 256 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows ($A_0 \sim A_6$) of the M5K4164NP must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5K416NP are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "write-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the output in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Hidden Refresh

A features of the M5K4164NP is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5K4164NP is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K4164NP as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5K4164NP operates on a singel 5V power supply.

A wait of some 500*us* and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

APPENDIX B

ABSOLUTE MAXIMUM RATINGS

Symbol	Paramater	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1 ~ 7	V
V_I	Input voltage		−1 ~ 7	V
V_O	Output voltage		−1 ~ 7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta = 25°C	700	mW
Topr	Operating free-air temperature range		0 ~ 70	°C
Tstg	Storage temperature range		−65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = OV, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V \leq V_{OUT} \leq 5.5V$	−10		10	μA
I_I	Input current		$0V \leq V_{IN} \leq 6.5V$, All other pins = 0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5K4164NP-15	$\overline{RAS}$, $\overline{CAS}$ cycling			50	mA
		M5K4164NP-20	$t_{CR} = t_{CW}$ = min output open			45	mA
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS} = V_{IH}$ output open			4	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5K4164NP-15	$\overline{RAS}$ cycling $\overline{CAS} = V_{IH}$			40	mA
		M5K4164NP-20	$t_{C(\overline{REF})}$ = min, output open			35	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5K4164NP-15	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling			40	mA
		M5K4164NP-20	t_{CPG} = min, output open			35	mA
$C_{I(A)}$	Input capacitance, address inputs		$V_I = V_{SS}$ f = 1MHz V_I = 25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		$V_O = V_{SS}$, f = 1MHz, V_I = 25mVrms			7	pF

Note 2 Current flowing into an IC is positive, out is negative.

3 $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4 $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

APPENDIX B

TIMING REQUIREMENTS (For Read, Write, Read-Modify, Refresh , and Page-Mode Cycle)

(Ta = 0 ~ 70°C , V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted; See notes 5, 6 and 7)

Symbol	Parameter		Alternative Symbol	M5K4164NP-15 Limits Min	M5K4164NP-15 Limits Max	M5K4164NP-20 Limits Min	M5K4164NP-20 Limits Max	Unit
t_{CRF}	Refresh cycle time		t_{REF}		2		2	ms
$t_{W(RASH)}$	$\overline{RAS}$ high pulse width		t_{RP}	100		120		ns
$t_{W(RASL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	150	10000	200	10000	ns
$t_{W(CASL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	75	∞	100	∞	ns
$t_{W(CASH)}$	$\overline{CAS}$ high pulse width	(Note 8)	t_{CPN}	35		40		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$		t_{CSH}	150		200		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$		t_{RSH}	75		100		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$	(Note 9)	t_{RCD}	25	75	30	100	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$		t_{ASR}	0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$		t_{ASC}	−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$		t_{RAH}	20		25		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$		t_{CAH}	25		35		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$		t_{AR}	95		120		ns
t_{THL} t_{TLH}	Transition time		t_T	3	35	3	50	ns

Note 5 An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.

6 The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.

7 Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.

8 Except for page-mode.

9 Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.

$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C , V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Read Cycle

Symbol	Parameter		Alternative Symbol	M5K4164NP-15 Limits Min	M5K4164NP-15 Limits Max	M5K4164NP-20 Limits Min	M5K4164NP-20 Limits Max	Unit
t_{CR}	Read cycle time		t_{RC}	260		330		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$	(Note 10)	t_{RCH}	0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$	(Note 10)	t_{RRH}	20		25		ns
$t_{dis(CAS)}$	Output disable time	(Note 11)	t_{OFF}	0	40	0	50	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 12)	t_{CAC}		75		100	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 13)	t_{RAC}		150		200	ns

Note 10 Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.

Note 11 $t_{dis(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}

Note 12 This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max. Test conditions , Load = 2T TL, C_L = 100pF

Note 13 This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions ; Load = 2T TL, C_L = 100pF

Write Cycle

Symbol	Parameter		Alternative Symbol	M5K4164NP-15 Limits Min	M5K4164NP-15 Limits Max	M5K4164NP-20 Limits Min	M5K4164NP-20 Limits Max	Unit
t_{CW}	Write cycle time		t_{RC}	260		330		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$	(Note 16)	t_{WCS}	− 10		− 10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$		t_{WCH}	45		55		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$		t_{WCR}	95		120		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	45		55		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	45		55		ns
$t_{W(W)}$	Write pulse width		t_{WP}	45		55		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$		t_{DS}	0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$		t_{DH}	45		55		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$		t_{DHR}	95		120		ns

APPENDIX B

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	M5K4164NP-15 Limits		M5K4164NP-20 Limits		Unit
				Min	Max	Min	Max	
t_{CRW}	Read-write cycle time	(Note 14)	t_{RWC}	295		370		ns
t_{CRMW}	Read-modify-write cycle time	(Note 15)	t_{RMWC}	310		390		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	45		55		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	45		55		ns
$t_{w(W)}$	Write pulse width		t_{WP}	45		55		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write	(Note 16)	t_{RWD}	120		150		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write	(Note 16)	t_{CWD}	60		80		ns
$t_{su(D-W)}$	Data-in set-up time before write		t_{DS}	0		0		ns
$t_{h(W-D)}$	Data-in hold time after write		t_{DH}	45		55		ns
$t_{dis(CAS)}$	Output disable time		t_{OFF}	0	40	0	50	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 12)	t_{CAC}		75		100	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 13)	t_{RAC}		150		200	ns

Note 14: $t_{CRW}min = t_{d(RAS-CAS)}max + t_{d(CAS-W)}min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH}(t_{THL})$

15: $t_{CRMW}min$ is defined as $t_{CRMW}min = t_{a(RAS)}max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH}(t_{THL})$

16: $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geq t_{su(W-CAS)}min$, an early-write cycle is performed, and the data output keeps the high-impedance state

When $t_{d(RAS-W)} \geq t_{d(RAS-W)}min$, and $t_{d(CAS-W)} \geq t_{su(W-CAS)}min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

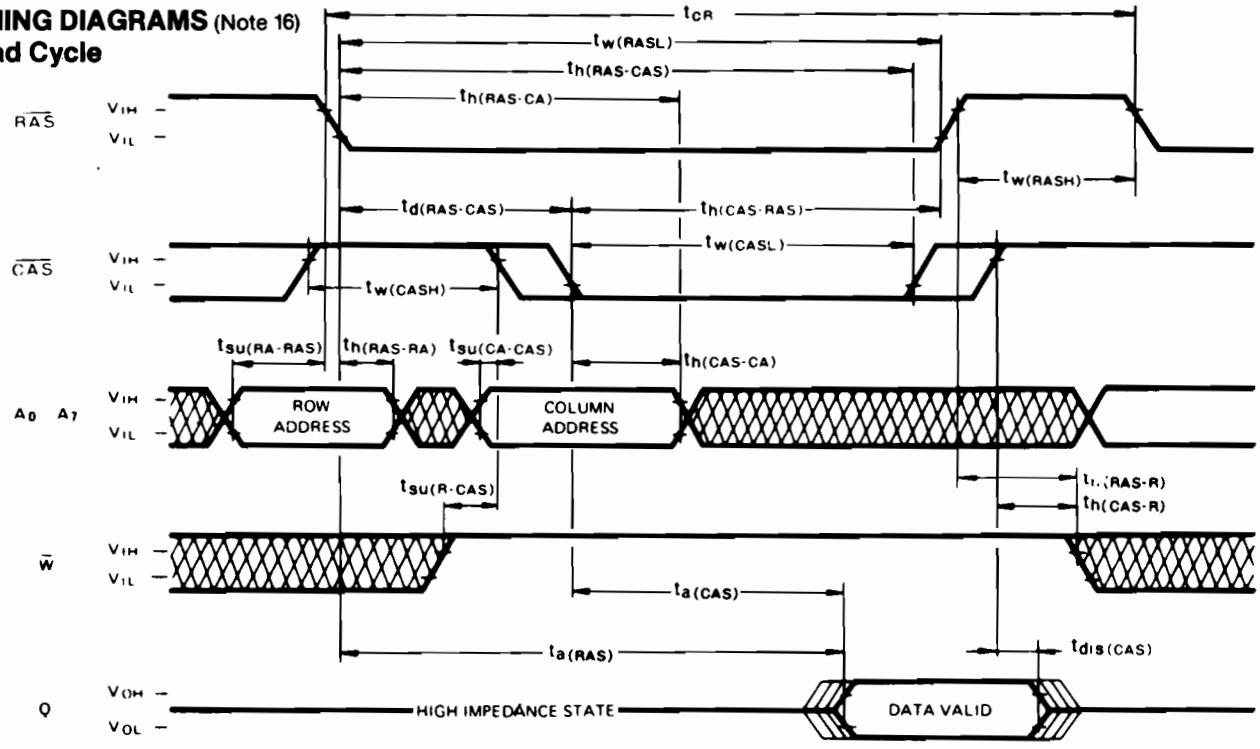
Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	M5K4164NP-15 Limits		M5K4164NP-20 Limits		Unit
			Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	145		190		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	60		80		ns

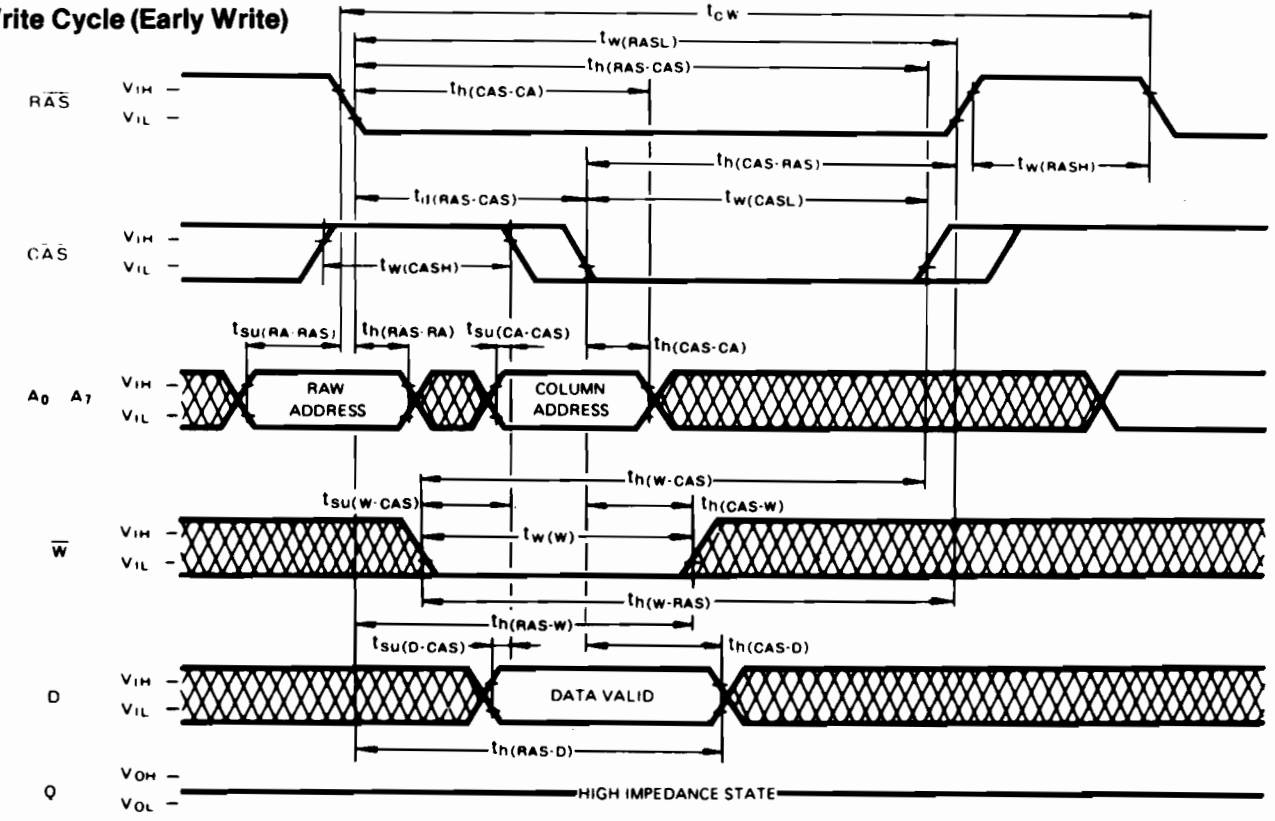
APPENDIX B

TIMING DIAGRAMS (Note 16)

Read Cycle

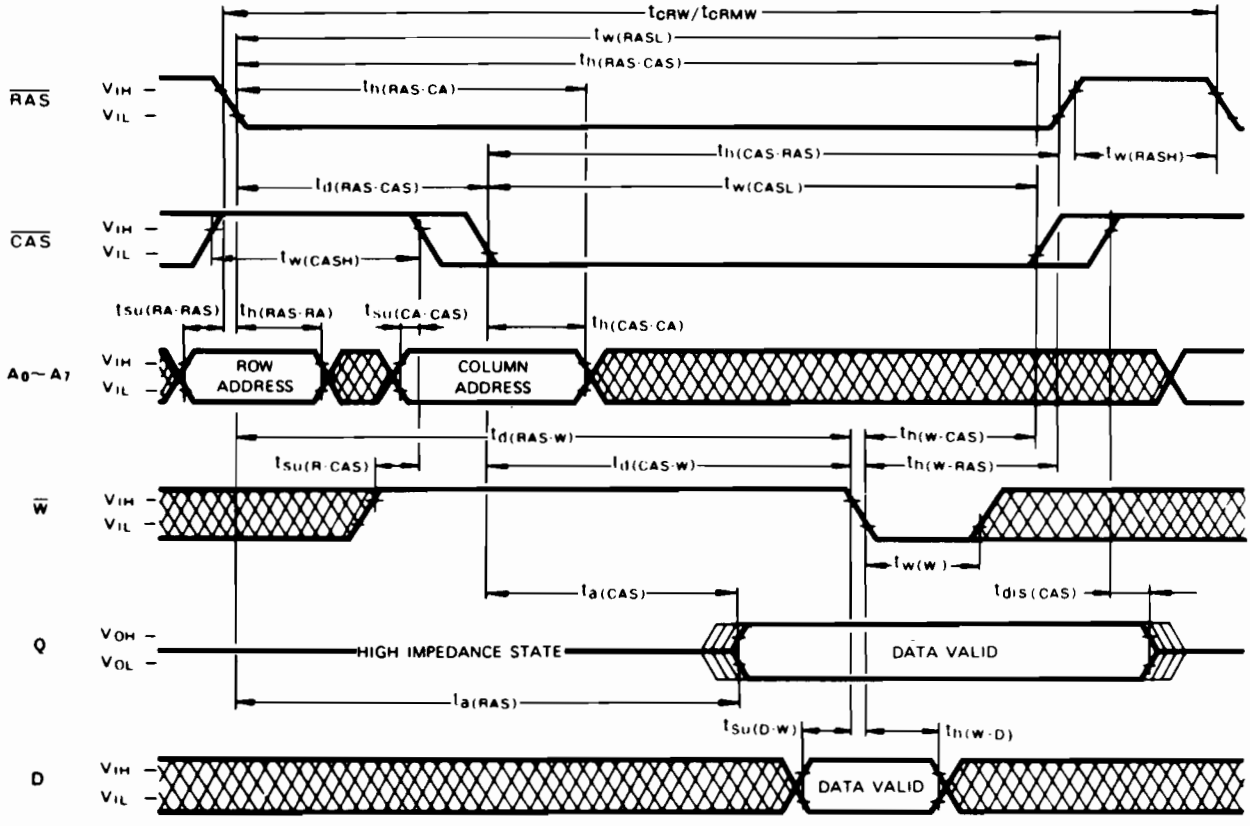


Write Cycle (Early Write)

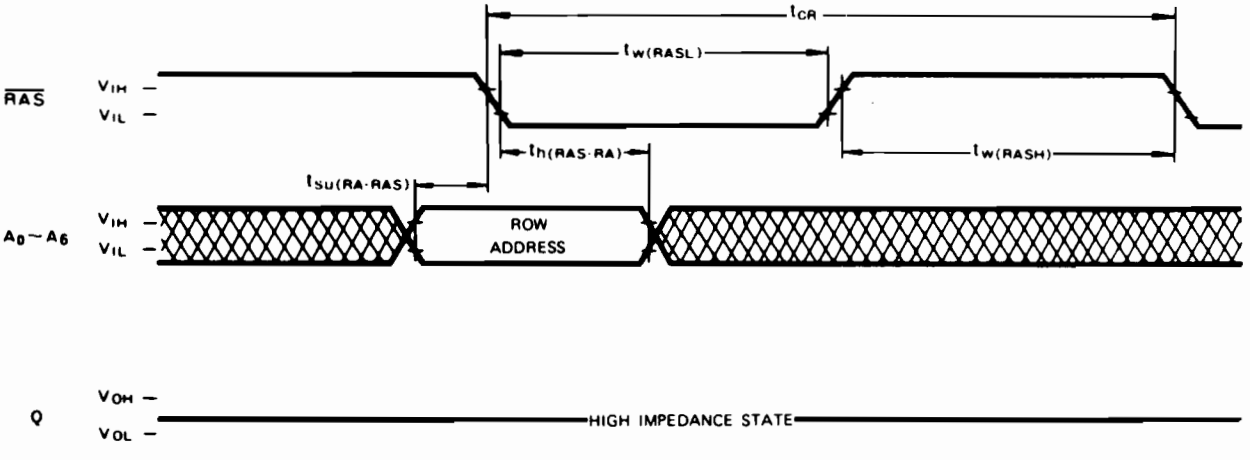


APPENDIX B

Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 17)



Note 16

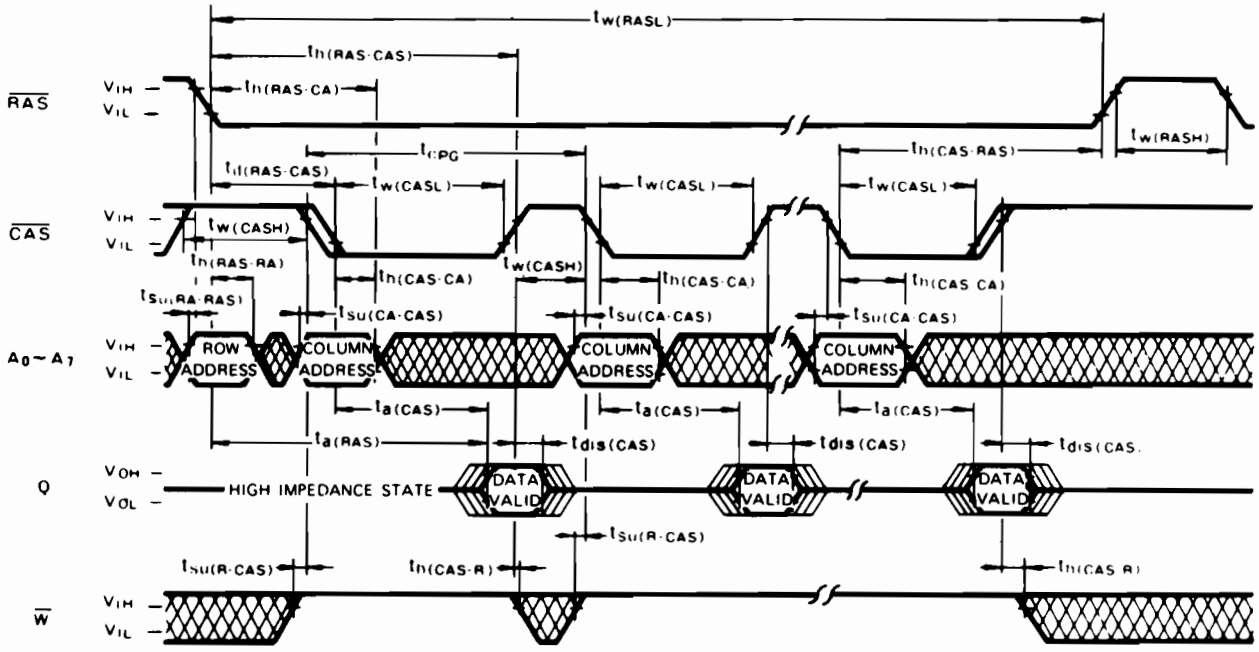
Indicates the don't care input

The center-line indicates the high-impedance state

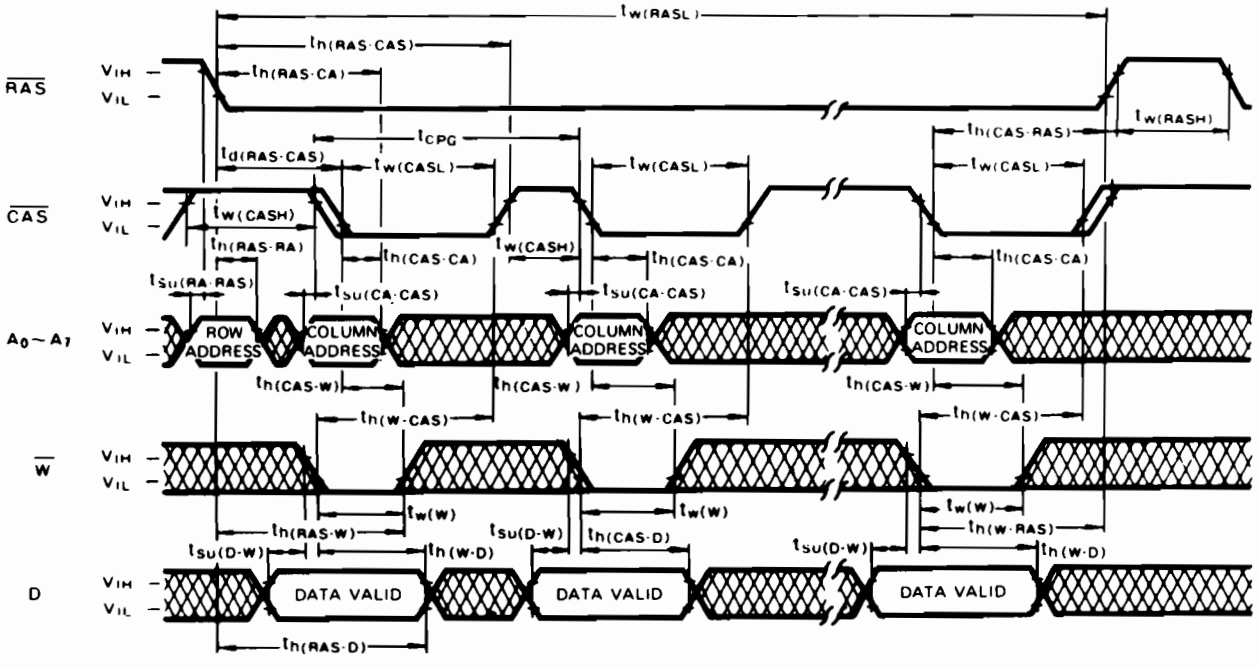
Note 17. $\overline{CAS} = V_{IH}$, $\overline{W}$, A_7, D = don't care.

APPENDIX B

Page-Mode Read Cycle

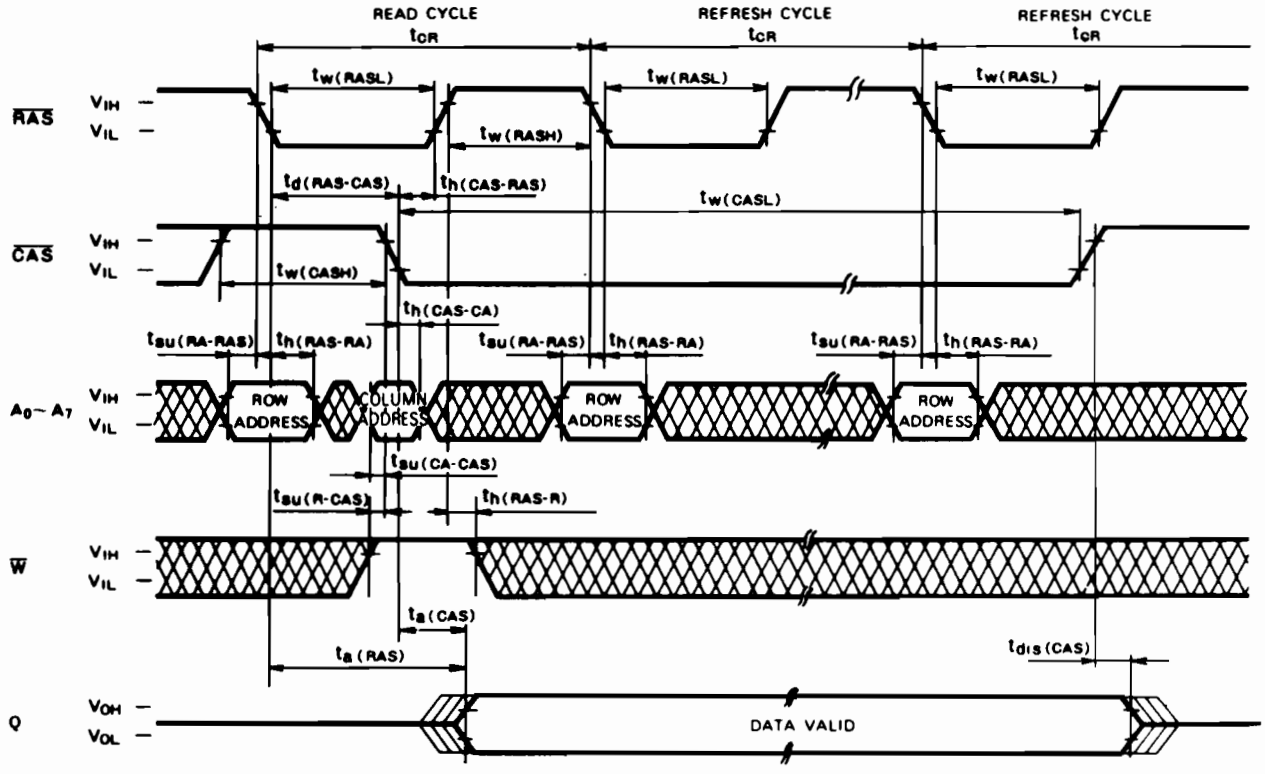


Page-Mode Write Cycle



APPENDIX B

Hidden Refresh Cycle (Note 17)



YOUR ZENITH DATA SYSTEMS COMPUTER HARDWARE PRODUCTS

90 DAY LIMITED WARRANTY

Welcome to the ZENITH DATA SYSTEMS family. We believe that you have purchased one of the finest computer products available. Please read this carefully. It is a Limited Warranty as defined in the U. S. Consumer Product Warranty and Federal Trade Commission Improvement Act. This warranty gives you specific legal rights, and you may also have other rights that vary from State to State within the U. S. A.

ZENITH DATA SYSTEMS (ZDS) RESPONSIBILITY

SERVICE LABOR – For a period of 90 days from the effective warranty date, ZDS will pay for service labor by a ZDS-approved service station when needed as a result of defective workmanship and material in ZDS computer hardware products.

PARTS – New or rebuilt replacements for factory-defective parts will be supplied for 90 days from the effective warranty date. Replacement parts are warranted for the remaining portion of the original warranty period.

NOT COVERED – The above warranty does not extend to installation and adjustment at User's location, nor to any computer hardware products which does not bear a serial number, or which has been subjected to misuse, abuse, neglect, accident, improper installation application, or alteration including, but not limited to electrical, mechanical, or cosmetic (including removal of ZDS nameplates, logos, trademarks, or identification, or the attachment of any non-ZDS nameplate, logo, trademark or identification), without the expressed written authority of ZDS, or subjected to negligence in use, storage, transportation or handling.

APPLICABILITY OF WARRANTY – This warranty covers only ZENITH DATA SYSTEMS computer hardware products and is not extended to other computer hardware products or components that customer uses in conjunction with our products. This Warranty does not cover computer software products nor damage to computer hardware products caused by computer software products. This Warranty applies only to the first end-user of the ZENITH DATA SYSTEMS computer hardware product who becomes such either by purchase at retail or by lease. This Warranty is not assignable.

DAMAGES — UNDER NO CIRCUMSTANCES SHALL ZDS BE LIABLE IN ANY WAY TO THE USER FOR INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING BUT LIMITED TO, ANY LOSS OF BUSINESS OR PROFITS, WHETHER OR NOT FORSEEABLE AND WHETHER OR NOT BASED ON BREACH OF WARRANTY, CONTRACT, OR NEGLIGENCE IN CONNECTION WITH THE SALE OF SUCH COMPUTER HARDWARE PRODUCTS. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

OWNERS RESPONSIBILITY

EFFECTIVE WARRANTY DATE - Warranty begins on the date of purchase at retail by, or leased to, the first end user, as the case may be. For your convenience, keep the dealer's dated bill of sale or invoice as evidence of the sale. The proof of purchase must be provided when Warranty service is requested.

OPERATING MANUAL – Read Your Operating Manual Carefully so that you will understand the operation of your computer hardware products.

OWNER'S REGISTRATION – Please fill out your Owner Registration card and return it by mail to ZDS.

WARRANTY SERVICE – For Warranty service, contact your ZDS dealer, HEATHKIT ELECTRONIC CENTER, or any ZDS approved service station. Parts and service labor that are ZDS's responsibility under this warranty will be provided. Other service is at the User's expense. If you have any problem in obtaining satisfactory warranty service, write to:

Customer Services
ZENITH DATA SYSTEMS, CORPORATION
1000 Milwaukee Ave.
Glenview, Il 60025

(See reverse side for other Service Information)

YOUR ZENITH DATA SYSTEMS COMPUTER HARDWARE PRODUCTS

90 DAY LIMITED WARRANTY

Welcome to the ZENITH DATA SYSTEMS family. We believe that you have purchased one of the finest computer products available. Please read this carefully. It is a Limited Warranty as defined in the U.S. Consumer Product Warranty and Federal Trade Commission Improvement Act. This warranty gives you specific legal rights, and you may also have other rights that vary from State to State within the U.S.A.

ZENITH DATA SYSTEMS (ZDS) RESPONSIBILITY

SERVICE LABOR — For a period of 90 days from the effective warranty date, ZDS will pay for service labor by a ZDS-approved service station when needed as a result of defective workmanship and material in ZDS computer hardware products.

PARTS — New or rebuilt replacements for factory-defective parts will be supplied for 90 days from the effective warranty date. Replacement parts are warranted for the remaining portion of the original warranty period.

NOT COVERED — The above warranty does not extend to installation and adjustment at User's location, nor to any computer hardware product which does not bear a serial number, or which has been subjected to misuse, abuse, neglect, accident, improper installation application, or alteration including, but not limited to electrical, mechanical, or cosmetic (including removal of ZDS nameplates, logos, trademarks, or identification, or the attachment of any non-ZDS nameplate, logo, trademark, or identification), without the expressed written authority of ZDS, or subjected to negligence in use, storage, transportation or handling.

APPLICABILITY OF WARRANTY — This warranty covers only ZENITH DATA SYSTEMS computer hardware products and is not extended to other computer hardware products or components that customer uses in conjunction with our products. This warranty does not cover computer software products nor damage to computer hardware products caused by computer software products. This warranty applies only to the first end user of the ZENITH DATA SYSTEMS computer hardware product who becomes such either by purchase at retail or by lease. This warranty is not assignable.

DAMAGES — UNDER NO CIRCUMSTANCES SHALL ZDS BE LIABLE IN ANY WAY TO THE USER FOR INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING BUT NOT LIMITED TO, ANY LOSS OF BUSINESS OR PROFITS, WHETHER OR NOT FORESEEABLE AND WHETHER OR NOT BASED ON BREACH OF WARRANTY, CONTRACT, OR NEGLIGENCE IN CONNECTION WITH THE SALE OF SUCH COMPUTER HARDWARE PRODUCTS. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

OWNERS RESPONSIBILITY

EFFECTIVE WARRANTY DATE — Warranty begins on the date of purchase at retail by, or leased to, the first end user, as the case may be. For your convenience, keep the dealer's dated bill of sale or invoice as evidence of the sale. The proof of purchase must be provided when warranty service is requested.

OPERATING MANUAL — Read Your Operating Manual Carefully so that you will understand the operation of your computer hardware products.

OWNER'S REGISTRATION — Please fill out your Owner Registration card and return it by mail to ZDS.

WARRANTY SERVICE — For warranty service, contact your ZDS dealer, HEATHKIT ELECTRONIC CENTER, or any ZDS approved service station. Parts and service labor that are ZDS's responsibility under this warranty will be provided. Other service is at the User's expense. If you have any problem in obtaining satisfactory warranty service, write to:

Customer Services
ZENITH DATA SYSTEMS, CORPORATION
1000 Milwaukee Ave.
Glenview, IL 60025