# SERVICE MANUAL

# Xebec Winchester System

## Z-100 PC Series Computers

**NOTE:** If you must change controllers (from Western Digital to Xebec or vice versa), the Winchester disk **must** be reinitialized. This means that you will have to run PREP and PART and reformat the partitions your customer will use.

To prevent loss of the customer's data on the Winchester disk, perform the BACKUP procedure for the customer's operating system. If a controller card failure has occurred, replace the card with another card of the same part number. After the Winchester disk has been prepared, partitioned, and formatted, use RESTORE to replace the customer's files on the Winchester disk.

585-136

860-122

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

# Record of Field Service Bulletins

| SERVICE BULLETIN NUMBER | DATE OF ISSUE | CHANGED PAGE(S) | PURPOSE OF SERVICE BULLETIN | INITIALS |
|---|---|---|---|---|
| | | | | |



**Zenith Data Systems Corporation**
**St. Joseph, Michigan 49085**

# Contents



# Figures



# Tables

Chapter 1

# Introduction

This manual provides information on the Xebec Winchester system. The OEM manual for the Xebec Winchester controller card is included. **DO NOT** attempt repair on the Winchester drive.

Chapter 2

# Installation and Configuration

## Introduction

This chapter provides the information necessary to configure, install, test, and prepare the Xebec Winchester option.

**NOTE:** If you must change controllers (from Western Digital to Xebec or vice versa), the Winchester disk **must** be reinitialized. This means that you will have to run PREP and PART and reformat the partitions your customer will use.

To prevent loss of the customer's data on the Winchester disk, perform the BACKUP procedure for the customer's operating system. If a controller card failure has occurred, replace the card with another card of the same part number. After the Winchester disk has been prepared, partitioned, and formatted, use RESTORE to replace the customer's files on the Winchester disk.

**NOTE**: The Xebec Winchester controller card can be identified from the exterior by an X on the bracket.

# Xebec Winchester Controller Card Configuration

Refer to Figure 2.1 for the jumper block locations of the Xebec Winchester controller card.

The Xebec Winchester controller card has three jumper blocks.

- I/O ADDR (input/output address);
- ROM ADD ( ROM addressing ) and PD (BIOS ROM disable);
- OPTION.

## I/O ADDR

The I/O ADDR jumper block selects the command port address for drive 0. Factory configuration is configured at I/O address 320 hexadecimal (refer to Figure 2.1). If a second controller is installed, the I/O address of controller 1 is configured at I/O address 322 hexadecimal. Refer to Table 2.1 for a complete list of available addressing.

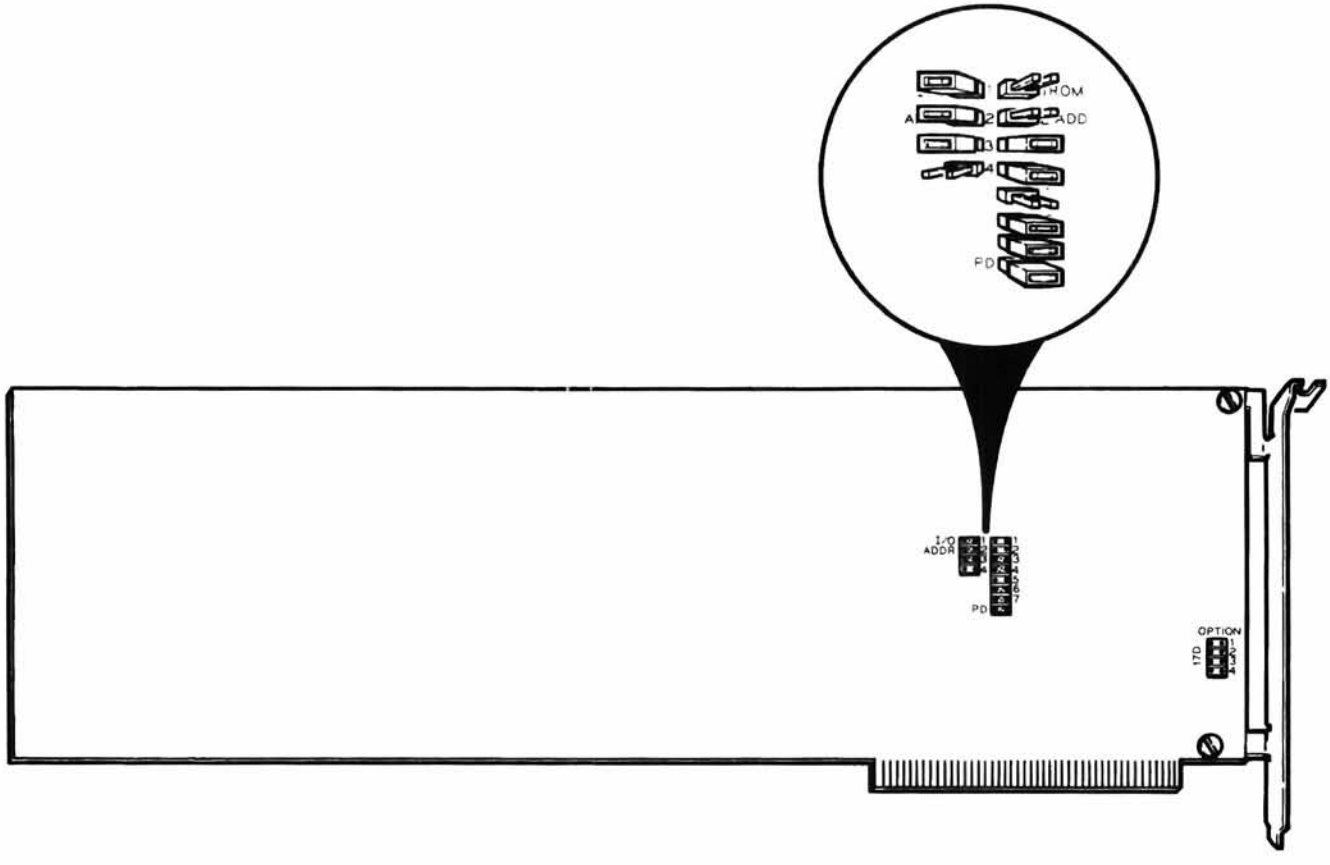



**Figure 2.1. Xebec Jumper Block Locations and Factory Configuration**

**Table 2.1. I/O ADDR Selection**

| HEXADECIMAL BASE ADDRESS | I/O ADDR LINES (J = JUMPERED, O = OPEN) 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 300 | J | J | J | J |
| 304 | O | J | J | J |
| 308 | J | O | J | J |
| 30C | O | O | J | J |
| 310 | J | J | O | J |
| 314 | O | J | O | J |
| 318 | J | O | O | J |
| 31C | O | O | O | J |
| 320 | J | J | J | O |
| 324 | O | J | J | O |
| 328 | J | O | J | O |
| 32C | O | O | J | O |
| 330 | J | J | O | O |
| 334 | O | J | O | O |
| 338 | J | O | O | O |
| 33C | O | O | O | O |

# ROM ADD (ROM Addressing) and PD (BIOS ROM Disable)

The ROM ADD jumper block selects the memory hexadecimal address from 00000 through XXFFF. Factory configuration is configured at address C8000 hexadecimal (refer to Figure 2.1). If a bit-mapped video graphics card (Z-319) is installed, the memory address is configured at memory address F4000 hexadecimal (refer to Figure 2.2). Refer to Table 2.2 for a complete list of available memory addressing

The PD jumper enables the BIOS ROM. If more than one controller is used in a system, one of the controllers must have the BIOS ROM disabled (PD jumper removed).

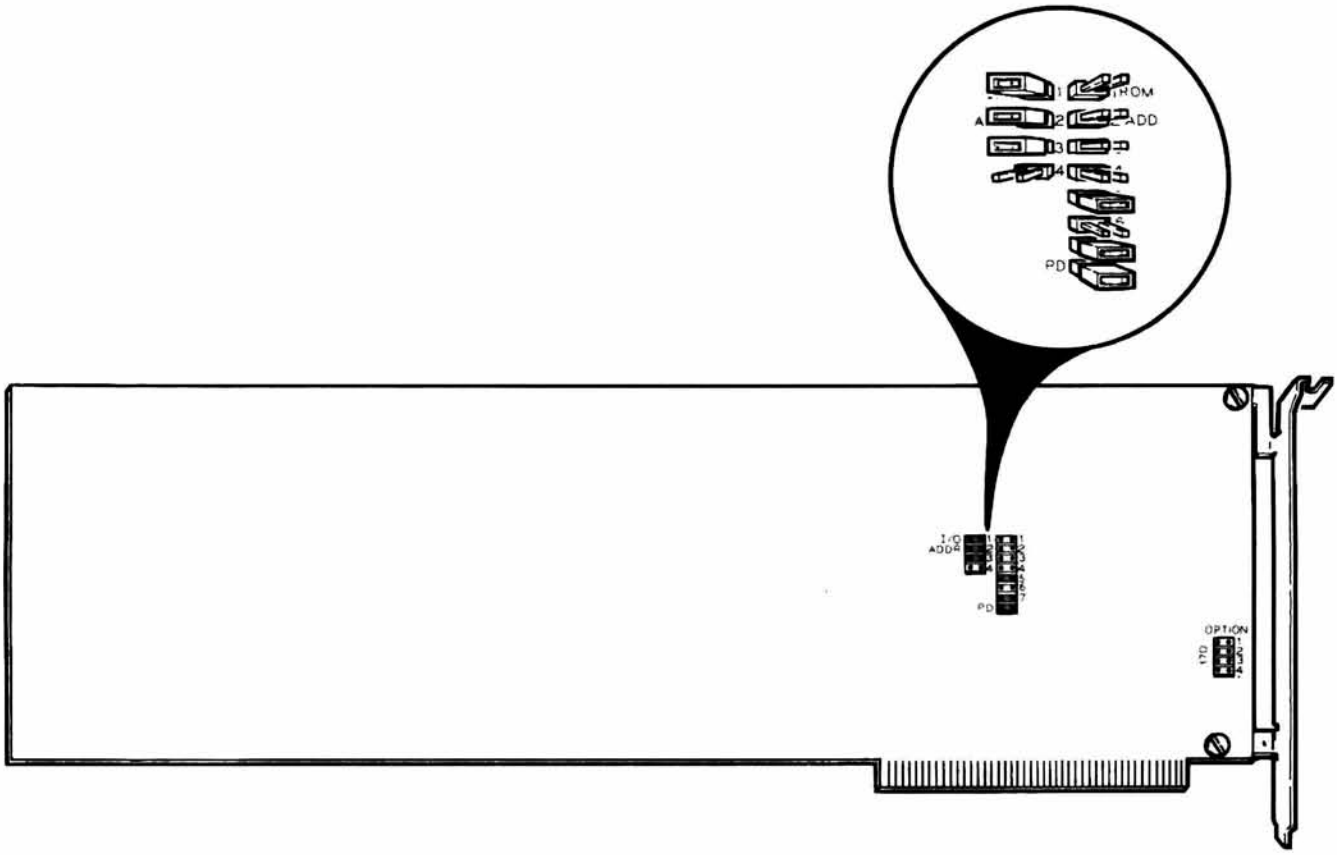



**Figure 2.2. Xebec Bit-Mapped Video Graphics Configuration**

**Table 2.2. ROM ADD (ROM Addressing)**

| HEXADECIMAL HOST ROM ADDRESS | I/O ADDR LINES (J = JUMPERED, O = OPEN) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 00000 | J | J | J | J | J | J | J |
| 02000 | J | J | J | J | J | J | O |
| 04000 | J | J | J | J | J | O | J |
| 06000 | J | J | J | J | J | O | O |
| 08000 | J | J | J | J | O | J | J |
| 0A000 | J | J | J | J | O | J | O |
| 0C000 | J | J | J | J | O | O | J |
| 0E000 | J | J | J | J | O | O | O |
| 10000 | J | J | J | O | J | J | J |
| 12000 | J | J | J | O | J | J | O |
| 14000 | J | J | J | O | J | O | J |
| 16000 | J | J | J | O | J | O | O |
| 18000 | J | J | J | O | O | J | J |
| 1A000 | J | J | J | O | O | J | O |
| 1C000 | J | J | J | O | O | O | J |
| 1E000 | J | J | J | O | O | O | O |
| 20000 | J | J | O | J | J | J | J |
| 22000 | J | J | O | J | J | J | O |
| 24000 | J | J | O | J | J | O | J |
| 26000 | J | J | O | J | J | O | O |
| 28000 | J | J | O | J | O | J | J |
| 2A000 | J | J | O | J | O | J | O |
| 2C000 | J | J | O | J | O | O | J |
| 2E000 | J | J | O | J | O | O | O |
| 30000 | J | J | O | O | J | J | J |
| 32000 | J | J | O | O | J | J | O |
| 34000 | J | J | O | O | J | O | J |
| 36000 | J | J | O | O | J | O | O |
| 38000 | J | J | O | O | O | J | J |
| 3A000 | J | J | O | O | O | J | O |
| 3C000 | J | J | O | O | O | O | J |
| 3E000 | J | J | O | O | O | O | O |
| 40000 | J | O | J | J | J | J | J |
| 42000 | J | O | J | J | J | J | O |
| 44000 | J | O | J | J | J | O | J |

**Table 2.2 (continued). ROM ADD (ROM Addressing)**

| HEXADECIMAL HOST ROM ADDRESS | I/O ADDR LINES (J = JUMPERED, O = OPEN) 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 46000 | J | O | J | J | J | O | O |
| 48000 | J | O | J | J | O | J | J |
| 4A000 | J | O | J | J | O | J | O |
| 4C000 | J | O | J | J | O | O | J |
| 4E000 | J | O | J | J | O | O | O |
| 50000 | J | O | J | O | J | J | J |
| 52000 | J | O | J | O | J | J | O |
| 54000 | J | O | J | O | J | O | J |
| 56000 | J | O | J | O | J | O | O |
| 58000 | J | O | J | O | O | J | J |
| 5A000 | J | O | J | O | O | J | O |
| 5C000 | J | O | J | O | O | O | J |
| 5E000 | J | O | J | O | O | O | O |
| 60000 | J | O | O | J | J | J | J |
| 62000 | J | O | O | J | J | J | O |
| 64000 | J | O | O | J | J | O | J |
| 66000 | J | O | O | J | J | O | O |
| 68000 | J | O | O | J | O | J | J |
| 6A000 | J | O | O | J | O | J | O |
| 6C000 | J | O | O | J | O | O | J |
| 6E000 | J | O | O | J | O | O | O |
| 70000 | J | O | O | O | J | J | J |
| 72000 | J | O | O | O | J | J | O |
| 74000 | J | O | O | O | J | O | J |
| 76000 | J | O | O | O | J | O | O |
| 78000 | J | O | O | O | O | J | J |
| 7A000 | J | O | O | O | O | J | O |
| 7C000 | J | O | O | O | O | O | J |
| 7E000 | J | O | O | O | O | O | O |
| 80000 | O | J | J | J | J | J | J |
| 82000 | O | J | J | J | J | J | O |
| 84000 | O | J | J | J | J | O | J |
| 86000 | O | J | J | J | J | O | O |
| 88000 | O | J | J | J | O | J | J |
| 8A000 | O | J | J | J | O | J | O |
| 8C000 | O | J | J | J | O | O | J |
| 8E000 | O | J | J | J | O | O | O |
| 90000 | O | J | J | O | J | J | J |
| 92000 | O | J | J | O | J | J | O |
| 94000 | O | J | J | O | J | O | J |
| 96000 | O | J | J | O | J | O | O |
| 98000 | O | J | J | O | O | J | J |

**Table 2.2 (continued). ROM ADD (ROM Addressing)**

| HEXADECIMAL HOST ROM ADDRESS | I/O ADDR LINES (J = JUMPERED, O = OPEN) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 9A000 | O | J | J | O | O | J | O |
| 9C000 | O | J | J | O | O | O | J |
| 9E000 | O | J | J | O | O | O | O |
| A0000 | O | J | O | J | J | J | J |
| A2000 | O | J | O | J | J | J | O |
| A4000 | O | J | O | J | J | O | J |
| A6000 | O | J | O | J | J | O | O |
| A8000 | O | J | O | J | O | J | J |
| AA000 | O | J | O | J | O | J | O |
| AC000 | O | J | O | J | O | O | J |
| AE000 | O | J | O | J | O | O | O |
| B0000 | O | J | O | O | J | J | J |
| B2000 | O | J | O | O | J | J | O |
| B4000 | O | J | O | O | J | O | J |
| B6000 | O | J | O | O | J | O | O |
| B8000 | O | J | O | O | O | J | J |
| BA000 | O | J | O | O | O | J | O |
| BC000 | O | J | O | O | O | O | J |
| BE000 | O | J | O | O | O | O | O |
| C0000 | O | O | J | J | J | J | J |
| C2000 | O | O | J | J | J | J | O |
| C4000 | O | O | J | J | J | O | J |
| C6000 | O | O | J | J | J | O | O |
| C8000 | O | O | J | J | O | J | J |
| CA000 | O | O | J | J | O | J | O |
| CC000 | O | O | J | J | O | O | J |
| CE000 | O | O | J | J | O | O | O |
| D0000 | O | O | J | O | J | J | J |
| D2000 | O | O | J | O | J | J | O |
| D4000 | O | O | J | O | J | O | J |
| D6000 | O | O | J | O | J | O | O |
| D8000 | O | O | J | O | O | J | J |
| DA000 | O | O | J | O | O | J | O |
| DC000 | O | O | J | O | O | O | J |
| DE000 | O | O | J | O | O | O | O |
| E0000 | O | O | O | J | J | J | J |
| E2000 | O | O | O | J | J | J | O |
| E4000 | O | O | O | J | J | O | J |
| E6000 | O | O | O | J | J | O | O |
| E8000 | O | O | O | J | O | J | J |
| EA000 | O | O | O | J | O | J | O |

**Table 2.2 (continued). ROM ADD (ROM Addressing)**

| HEXADECIMAL HOST ROM ADDRESS | I/O ADDR LINES (J = JUMPERED, O = OPEN) 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| EC000 | O | O | O | J | O | O | J |
| EE000 | O | O | O | J | O | O | O |
| F0000 | O | O | O | O | J | J | J |
| F2000 | O | O | O | O | J | J | O |
| F4000 | O | O | O | O | J | O | J |
| F6000 | O | O | O | O | J | O | O |
| F8000 | O | O | O | O | O | J | J |
| FA000 | O | O | O | O | O | J | O |
| FC000 | O | O | O | O | O | O | J |
| FE000 | O | O | O | O | O | O | O |

# OPTION

The OPTION jumpers select the drive number and the particular Winchester unit used (heads and cylinders). Jumpers one (1) and two (2) select the parameters for drive 0; jumpers three (3) and four (4) select the parameters for drive 1. Factory configuration is not jumpered. Refer to Table 2.3 for drive selection, number of heads, and number of cylinders. Refer to the particular Winchester OEM manual for the number of heads and cylinders.

**Table 2.3. OPTIONS**

| SELECT LINES (J = JUMPERED, O = OPEN) DRIVE 0 1 | 2 | DRIVE 1 3 | 4 | CYLINDERS | HEADS |
|---|---|---|---|---|---|
| O | O | O | O | 306 | 4 |
| O | J | O | J | 612 | 2 |
| J | O | J | O | 480 | 4 |
| J | J | J | J | 306 | 6 |

# Winchester Installation

**NOTE:** If you must change controllers (from Western Digital to Xebec or vice versa), the Winchester disk **must** be reinitialized. This means that you will have to run PREP and PART and reformat the partitions your customer will use.

To prevent loss of the customer's data on the Winchester disk, perform the BACKUP procedure for the customer's operating system. If a controller card failure has occurred, replace the card with another card of the same part number. After the Winchester disk has been prepared, partitioned, and formatted, use RESTORE to replace the customer's files on the Winchester disk.

Refer to Figure 2.3 while reading the following.

- Remove seven screws (10) and top cover (5).
- **Remove screw (170) and card guide (160).**
- Disconnect cable assembly (180) from floppy disk controller card (20).
- Disconnect any serial interface cables installed from floppy disk controller card (20).
- Remove screw (25) and floppy disk controller card (20).
- Disconnect the video display external cable from video/color/composite card (30).
- Remove screw (25) and video/color/composite card (30).
- Disconnect the keyboard from the system CPU card (35).
- Disconnect cable assembly (125) from the system CPU card (35).
- Remove screw (25) and system CPU card (35).
- Disconnect any exterior cables installed to the 128K memory card (40).
- Remove screw (25) and memory card (40).
- Remove two screws (25) and shipping bracket (166), if installed.

- Remove optional card(s), if installed.
- Disconnect power supply cable to backplane board (45).
- Disconnect power supply cables to the disk drive.
- Remove two screws (65) from rear of chassis.
- Remove four hex lock nuts (55) from the bottom of the chassis and power supply (50).
- Disconnect cable assembly (180).
- Remove six hex lock nuts (55) and disk drive chassis (75).
- Remove four screws (90) from the bottom drive and the bottom drive (85), if installed.
- Remove the four mounting support brackets (80), if installed.
- Remove Bezel if unit had only one drive installed.
- Mount the Winchester LED in the LED holder (225) on vented cover (100), and secure with the LED grommet (220).
- Route the vented cover (100) through the disk drive chassis (75), and snap into place.
- Install the Winchester disk drive (85) into the disk drive chassis (75), and secure with four screws (90).
- Install disk drive chassis (75), and secure with six hex lock nuts (55).
- Connect cable assemblies (205 and 210) to Winchester drive.
- Connect cable assembly (180).
- Install power supply (50), and connect the power cables to the disk drives (85) and backplane board (45).

- Secure the power supply (50) with two screws (65) and four hex lock nuts (55).

- Install cable strap (215) over cable assemblies (205 and 210), and secure with two hex lock nuts (220).

- Install Winchester controller card (200), and secure with screw (25).

  Connect cable assemblies (205 and 210) to Winchester controller card (200).

- Install optional cards, and secure with screw (25).

- Install memory card (40), and secure with screw (25).

If your customer wants the machine set for autoboot from the Winchester drive, refer to the *System CPU Card Service Module* and set the switches on that card.

- Install system CPU card (35), and secure with screw (25).

- Connect speaker/LED connector to the system CPU card (35).

- Install video/color/composite card (30), and secure with screw (25). Connect external video cables.

  Install floppy disk controller card (20), and secure with screw (25).

- Connect cable assembly (180) to floppy disk controller card (20).

- **Install card guide (160) and screw (170).**

- Install top cover (5), and secure with seven screws (10).

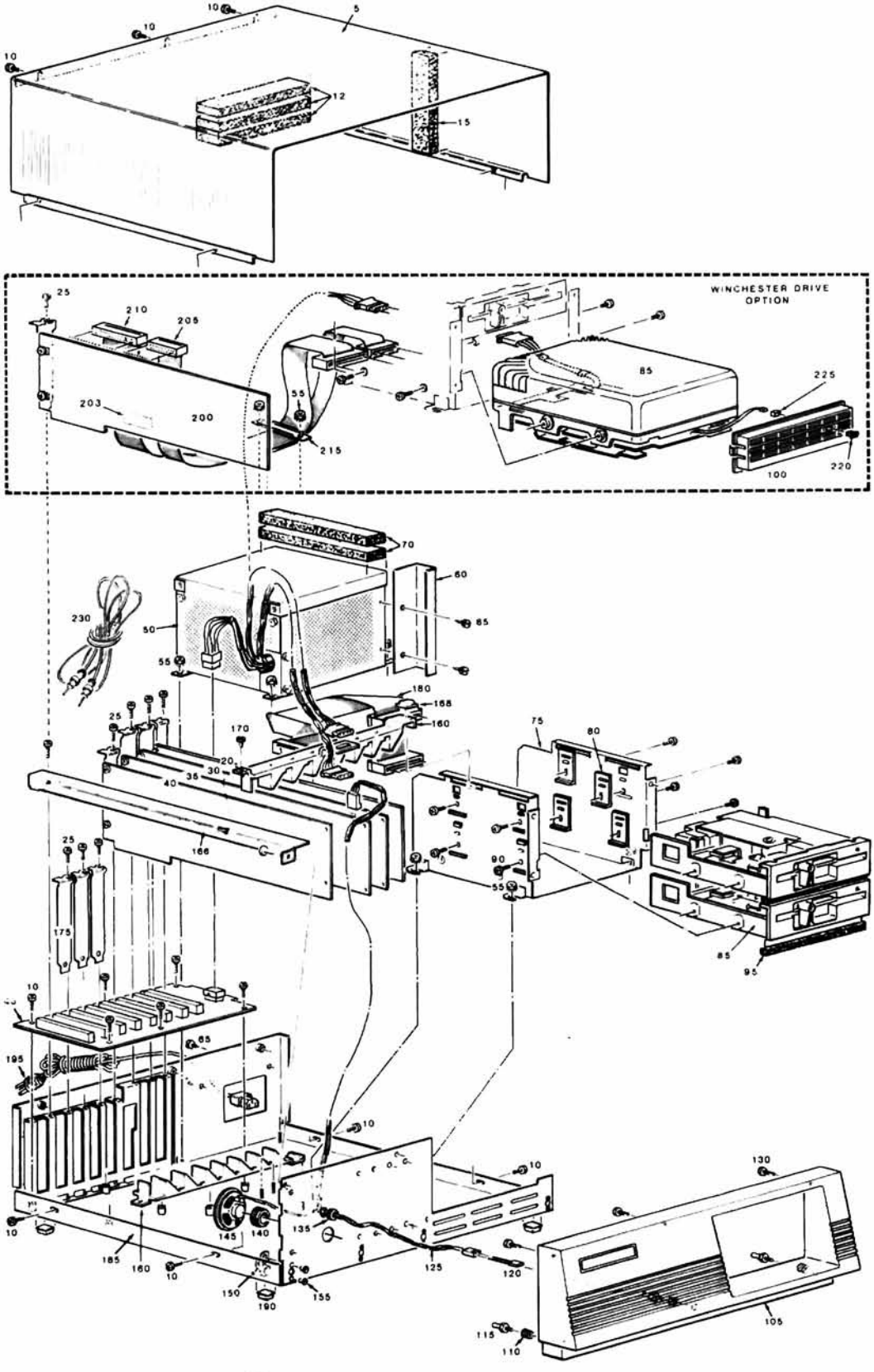



**Figure 2.3. Z-150 Exploded View**

# Preparing and Testing the Winchester Drive

**NOTE:** Once the Winchester system is physically installed in the computer, you will need to run the PREP utility from MS-DOS Version 2 (or higher) to prepare the disk surface and test its data retention capabilities. This test will take about four hours to run.

**NOTE:** The CMI Winchester drive requires the FORMAT utility Version 2.5 (or higher).

Turn on the computer and boot from MS-DOS Distribution Disk I.

Enter the date and time (optional), press **RETURN**.

Replace MS-DOS Distribution Disk I with Disk II.

Enter **PREP** and press the **RETURN** key. You will see a message that explains the operation of PREP displayed on the computer's screen.

At the bottom of the message you will see:

```
Do you wish to proceed with PREP (Y/N)?
```

Press the **Y** key. You will see:

```
Type P to proceed
```

Press the **P** key. The reason for this double prompt is to prevent accidental operation of PREP by the customer. PREP will destroy any valid (or invalid) data stored on the Winchester disk. Next, you will see:

```
Winchester drive unit number (0-7):
```

PREP will support up to eight separate Winchester drives. Normally, you will never install more than one drive in any one computer system. If you are installing more than one drive, you will be involved in special addressing considerations (only one Winchester drive is supported at this time).

Enter **0**.

If the installation was successfully made, the system will start the PREP process. Otherwise, you will see:

```
Can not communicate with Winchester controller.
```

If this message appears, software reset the system by pressing the CTRL, ALT, and DEL keys simultaneously, and repeat the Winchester preparation procedures.

# The PREP Process

During the PREP process, the disk will be initialized and then tested for data retention six times. Each test takes about 30 minutes, so the total test takes approximately 3-½ to 4 hours.

Messages will be displayed during each phase of the test, and the LED access indicator for the Winchester disk will flicker slightly (it will be on most of the time).

When PREP has finished, you will hear an audible beep from the speaker. If there is **no** bad disk space, the screen will display `Completed` and the operating system prompt.

If there **is** some bad disk space, the display will indicate the amount. Some bad space may be expected and is normal in Winchester systems. If the bad surface area exceeds the amount allowed by the manufacturer's standards, you will be informed by an appropriate error message. Otherwise, you may assume that your customer has a good drive.

Finish securing the cabinet. The system is installed and tested.

Run the SHIP utiity from MS-DOS Version 2 (or higher) before moving the system.

Chapter 3

# Xebec OEM Manual

This manual is reprinted with the permission of:

Xebec, an MSC Company
432 Lakeside Drive
Sunnyvale, California 94086

XEBEC, AN MSC COMPANY
432 LAKESIDE DRIVE
SUNNYVALE, CA 94086

# IBM PC AND PC/XT COMPATIBLE
# OEM CONTROLLER
# FOR 5¼" WINCHESTER DISK DRIVES STANDARD INTERFACE

## 1210A MANUAL

104838
REVISION A

## PREFACE

This manual contains technical information of the 1210A 5.25 Inch Winchester Disk Controller. New features have been added to the 1210A over the original 1210. The following is a list of additions:

1. Write Precompensation is selectable at 0, 5, and 10 nanoseconds. See Section 4.5.15 (Initialize Drive Characteristics).

2. Drives that have more than 8 heads and use the Reduced Write Current signal as head select 4 now operate on the 1210A. See Section 4.2.1.3 (Head Select Signals).

3. The sector format of the 1210A is compatable with the 1210. See Section 4.6 (Sector Format).

4. Harware has been added to provide for extra signals for the removeable cartridge Winchester Drives. (Firmware options will be available at a later date).

   Bios Driver Address Select by jumper blocks range from 00000 (Hex) to XXFFF (Hex). See Section 3.2.2.

6. Lower power requirements. See Section 2.2

# CHAPTER 1
# INTRODUCTION

## 1.1 GENERAL

The Xebec Integrated Single Board Disk Controller for the IBM PC and PC/XT compatible Computer can control the operation of up to two 5¼-inch Winchester disk drives that have interfaces that are compatible with the industry standard 5¼" hard disk drive interface. This controller is hardware compatible with both the IBM PC and XT Computer.

## 1.2 DESCRIPTION

The Xebec Controller is made to plug directly into any I/O slot in the computer. The following list highlights the operating and design features of the controller.

Interlocked data transfer.
Microprocessor-based architecture (patent pending).
Full-sector buffer.
Hardware 32-bit ECC polynomial with 11-bit burst correction.
Field-proven data separator.
Seagate Technology disk interface.
Automatic retries during disk access.
Internal Diagnostics.
Automatic burst error detection and correction.
Separate sector format for ID and data fields with individual ECC fields for both the ID and data fields.
High level command set.
Overlapped seek for buffered-step drive options.
Supports many of the drives which has imbedded servo at index time.

NOTE: Customer must furnish BIOS Driver.

## 1.3 FUNCTIONAL ORGANIZATION

The simplified block diagram in Figure 1-1 shows the functional organization of the Controller. Only the major areas are shown.

### 1.3.1 Host Interface

The host interface connects the internal data bus to the IBM I/O bus; the state machine controls the movement of data and commands through the host interface.

### 1.3.2 Processor

The eight-bit processor is the intelligence of the controller; it monitors and controls the operation of the controller.

### 1.3.3 State Machine

The state machine controls and synchronizes the operation of the host interface, SERDES, and sector buffer.

### 1.3.4 SERDES

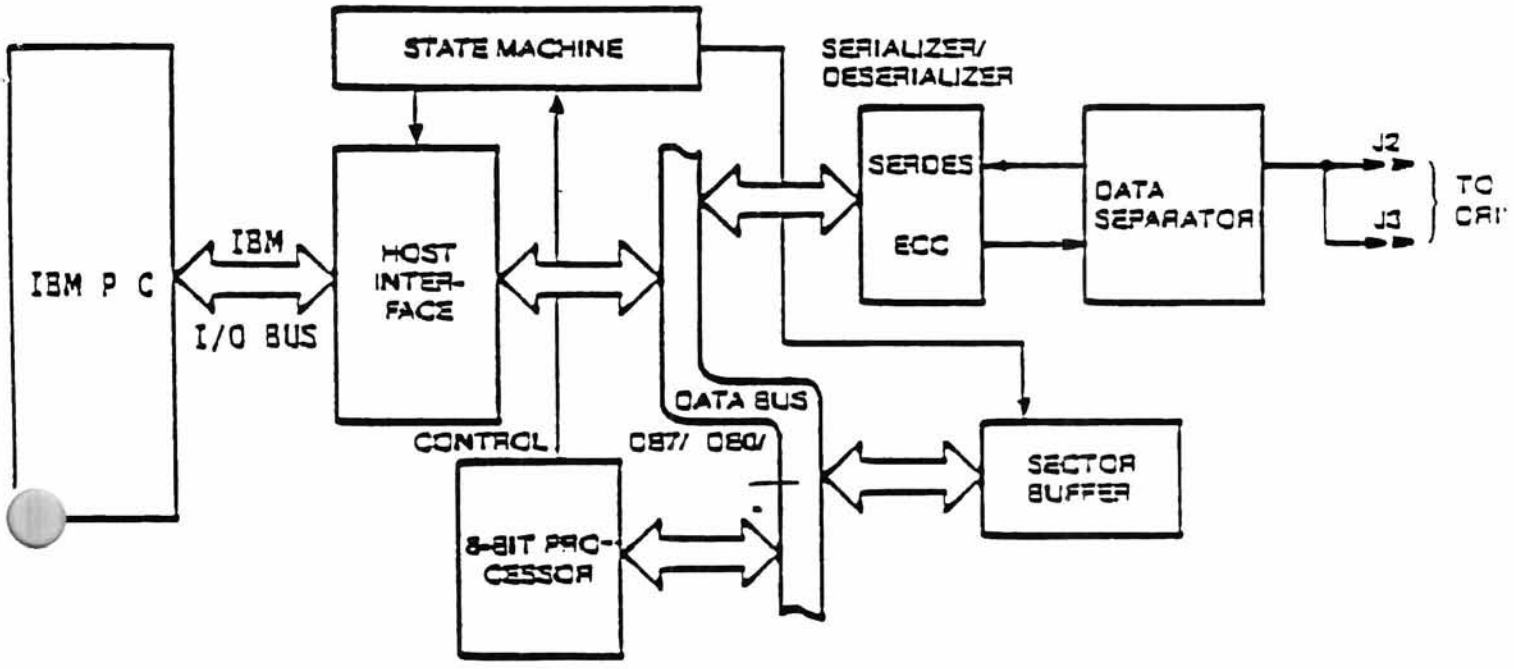
The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected disk drive. It converts serial data from the selected disk drive to parallel data which it places on the internal data bus.

### 1.3.5 Date Separator

The data separator converts serial NRZ data to MFM for transfer to the selected disk drive. It converts MFM data coming from the selected disk drive to serial NRZ data for the SERDES.

### 1.3.6 Sector Buffer

The sector buffer stages data transfers between the disk and the host to prevent data overruns.




XEBEC-IBM CONTROLLER, FUNCTIONAL ORGANIZATION

# CHAPTER 2
# SPECIFICATIONS

## 2.1 GENERAL

This chapter contains the overall specifications for the Controller. These specifications are meant to guide the user in placing the controller into operation. Some of the specifications indicate limits; the user must adhere to these in order to operate the controller successfully.

## 2.2 ELECTRICAL

Table 2-1 lists the electrical requirements of the controller.

**Table 2-1 Controller Electrical Requirements**

NOTE: All measurements are made on the controller printed circuit board at the CPU I/O connector.

| Voltage | Range | Current |
|---|---|---|
| +5.0 Vdc | 4.75 to 5.25 Vdc | 1.25 Amp. Max. |
| | | 1.0 Amp. Typ. |
| +12.0 Vdc | 10.8 to 13.2 Vdc | 15.0 ma. Max. |
| | | 10.0 ma. Typ. |

## 2.3 PHYSICAL SPECIFICATIONS

Figure 2-1 illustrates the dimensions of the board.

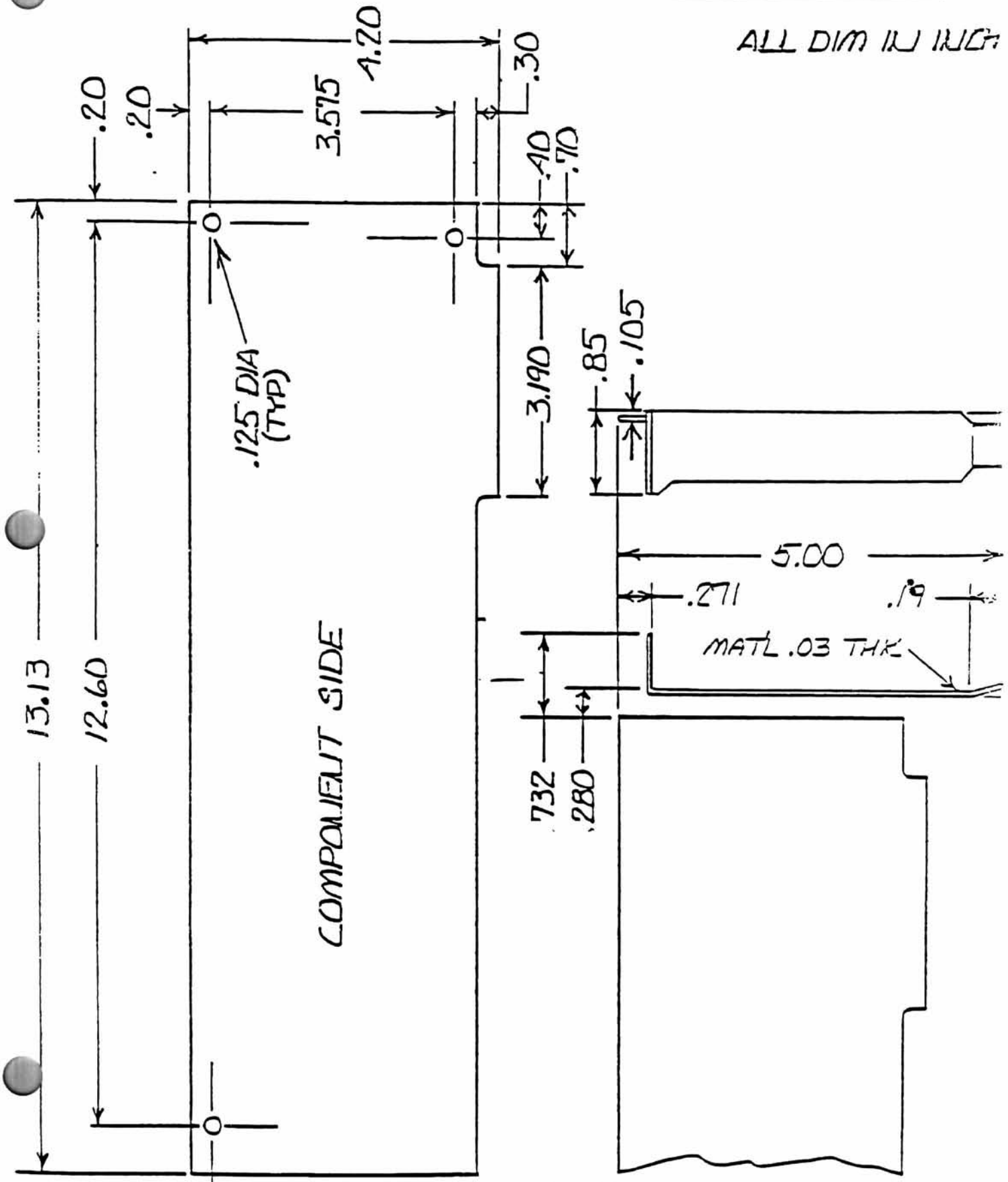



FIGURE 2-1 CONTROLLER BOARD DIMENSIONS

TABLE 2-2 CONTROLLER BOARD SPECIFICATIONS

## 2.4 ENVIRONMENTAL REQUIREMENTS

The controller will operate under the environmental conditions listed in Table 2-3. The controller does not normally require fans in standard operating environments where airflow is not restricted.

TABLE 2-3 ENVIRONMENTAL LIMITS

| ITEM | MEASUREMENT |
|---|---|
| Temperature | 0 to 50 degrees Celsius |
| Relative Humidity | 10 to 95 percent non-condensing |
| Altitude | Sea level to 10,000 feet |

## 2.5 CONNECTORS

| DESIGNATION | FUNCTION |
|---|---|
| J1 | Drive Control Signals |
| J2, J3 | Drive Data Signals |
| J4 | Test only, Do not connect a cable to J4 |
| P1 | Host interface |

## 2.6 CONNECTOR PIN ASSIGNMENTS

Tables 2-5 through 2-6 list the pin assignments of the connectors on the controller board. The tables identify the signals on the pins. The signals are defined in Chapter 4, Theory of Operation.

TABLE 2-5 CONNECTOR J1, CONTROL SIGNALS, PIN ASSIGNMENTS

| SIGNAL PIN | GROUND RETURN | SIGNAL NAME |
|---|---|---|
| 2 | 1 | Reduced Write Current- |
| 4 | 3 | Head $2^2$- |
| 6 | 5 | Write Gate- |
| 8 | 7 | Seek Complete- |
| 10 | 9 | Track 000- |
| 12 | 11 | Write Fault- |
| 14 | 13 | Head Select $2^0$- |
| 16 | 15 | Reserved |
| 18 | 17 | Head Select $2^1$- |
| 20 | 19 | Index- |
| 22 | 21 | Ready- |
| 24 | 23 | Step- |
| 26 | 25 | Drive Select 1- |
| 28 | 27 | Drive Select 2- |
| 30 | 29 | Reserved |
| 32 | 31 | Reserved |
| 34 | 33 | Direction In- |

**TABLE 2-6 CONNECTORS J2 AND J3, DATA SIGNALS, PIN ASSIGNMENTS**

| SIGNAL PIN | GROUND RETURN | SIGNAL NAME |
|---|---|---|
| 1 | 2 | Drive Selected- |
| 3 | 4 | Reserved |
| 5* | 6 | Spare |
| 7 | 8 | Reserved |
| 9 | 10 | Spares |
| 11 | 12 | Ground (GND) |
| 13 | | MFM Write Data |
| 14 | | MFM Write Data- |
| 15 | 16 | Ground (GND) |
| 17 | | MFM Read Data |
| 18 | | MFM Read Data- |
| 19 | 20 | Ground (GND) |

* Pin 5 of J2 and J3 is removed for cable keying.

# CHAPTER 3
# BOARD SETUP

## 3.1 GENERAL

This chapter contains the information for setting up and installing the controller before placing it in operation. These preparatory steps require the proper placement of jumpers, mounting the controller in its operating environment, and properly connecting the cables. In addition, the user has the option of using more than one controller in his system. Instructions for connecting multiple controllers appear later in the chapter.

## 3.2 BOARD SETUP

The host base address must be set, and the enable Host ROM option must be set before installing the board into the system.

### 3.2.1 Host Base Address

The base address of the controller is set by the I/O and jumper blocks. (See Figure 3-1). The address is preset at the factory for Hex 320. To change the address, change the jumper blocks for the described address.

| HEX BASE ADDRESS | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 300 | C | C | C | C |
| 304 | O | C | C | C |
| 308 | C | O | C | C |
| 30C | O | O | C | C |
| 310 | C | C | O | C |
| 314 | O | C | O | C |
| 318 | C | O | O | C |
| 31C | O | O | O | C |
| 320 | C | C | C | O |
| 324 | O | C | C | O |
| 328 | C | O | C | O |
| 32C | O | O | C | O |
| 330 | C | C | O | O |
| 334 | O | C | O | O |
| 338 | C | O | O | O |
| 33C | O | O | O | O |

C: CLOSE
O: OPEN

NOTE: Jumper Block specifications are AMP (530153-3) or BERG (65474-001) or equivalent.

### 3.2.2 Enable Host ROM

The Host driver ROM is set for memory hex address, by the jumper blocks. 00000 thru XXFFF. If multiple controllers are used in one system, one of the controllers must have it's Host ROM disabled. To disable, remove jumper block at PD. To enable the ROM install a jumper block at PD. (See Figure 3-1).

The board is shipped from the factory with the Host ROM enabled. The Host driver ROM is set for 8K-8. The ROM type is MK36000.

| HOST ROM ADDRESS (HEX) | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 00000 | C | C | C | C | C | C | C |
| 02000 | C | C | C | C | C | C | 0 |
| 04000 | C | C | C | C | C | 0 | C |
| 06000 | C | C | C | C | C | 0 | 0 |
| 08000 | C | C | C | C | 0 | C | C |
| 0A000 | C | C | C | C | 0 | C | 0 |
| 0C000 | C | C | C | C | 0 | 0 | C |
| 0E000 | C | C | C | C | 0 | 0 | 0 |
| 10000 | C | C | C | 0 | C | C | C |
| 12000 | C | C | C | 0 | C | C | 0 |
| 14000 | C | C | C | 0 | C | 0 | C |
| 16000 | C | C | C | 0 | C | 0 | 0 |
| 18000 | C | C | C | 0 | 0 | C | C |
| 1A000 | C | C | C | 0 | 0 | C | 0 |
| 1C000 | C | C | C | 0 | 0 | 0 | C |
| 1E000 | C | C | C | 0 | 0 | 0 | 0 |
| 20000 | C | C | 0 | C | C | C | C |
| 22000 | C | C | 0 | C | C | C | 0 |
| 24000 | C | C | 0 | C | C | 0 | C |
| 26000 | C | C | 0 | C | C | 0 | 0 |
| 28000 | C | C | 0 | C | 0 | C | C |
| 2A000 | C | C | 0 | C | 0 | C | 0 |
| 2C000 | C | C | 0 | C | 0 | 0 | C |
| 2E000 | C | C | 0 | C | 0 | 0 | 0 |
| 30000 | C | C | 0 | 0 | C | C | C |
| 32000 | C | C | 0 | 0 | C | C | 0 |
| 34000 | C | C | 0 | 0 | C | 0 | C |
| 36000 | C | C | 0 | 0 | C | 0 | 0 |
| 38000 | C | C | 0 | 0 | 0 | C | C |
| 3A000 | C | C | 0 | 0 | 0 | C | 0 |

| HOST ROM ADDRESS (HEX) | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 3C000 | C | C | 0 | 0 | 0 | 0 | C |
| 3E000 | C | C | 0 | 0 | 0 | 0 | 0 |
| 40000 | C | 0 | C | C | C | C | C |
| 42000 | C | 0 | C | C | C | C | 0 |
| 44000 | C | 0 | C | C | C | 0 | C |
| 46000 | C | 0 | C | C | C | 0 | 0 |
| 48000 | C | 0 | C | C | 0 | C | C |
| 4A000 | C | 0 | C | C | 0 | C | 0 |
| 4C000 | C | 0 | C | C | 0 | 0 | C |
| 4E000 | C | 0 | C | C | 0 | 0 | 0 |
| 50000 | C | 0 | C | 0 | C | C | C |
| 52000 | C | 0 | C | 0 | C | C | 0 |
| 54000 | C | 0 | C | 0 | C | 0 | C |
| 56000 | C | 0 | C | 0 | C | 0 | 0 |
| 58000 | C | 0 | C | 0 | 0 | C | C |
| 5A000 | C | 0 | C | 0 | 0 | C | 0 |
| 5C000 | C | 0 | C | 0 | 0 | 0 | C |
| 5E000 | C | 0 | C | 0 | 0 | 0 | 0 |
| 60000 | C | 0 | 0 | C | C | C | C |
| 62000 | C | 0 | 0 | C | C | C | 0 |
| 64000 | C | 0 | 0 | C | C | 0 | C |
| 66000 | C | 0 | 0 | C | C | 0 | 0 |
| 68000 | C | 0 | 0 | C | 0 | C | C |
| 6A000 | C | 0 | 0 | C | 0 | C | 0 |
| 6C000 | C | 0 | 0 | C | 0 | 0 | C |
| 6E000 | C | 0 | 0 | C | 0 | 0 | 0 |
| 70000 | C | 0 | 0 | 0 | C | C | C |
| 72000 | C | 0 | 0 | 0 | C | C | 0 |
| 74000 | C | 0 | 0 | 0 | C | 0 | C |
| 76000 | C | 0 | 0 | 0 | C | 0 | 0 |
| 7A000 | C | 0 | 0 | 0 | 0 | C | 0 |
| 7C000 | C | 0 | 0 | 0 | 0 | 0 | C |
| 7E000 | C | 0 | 0 | 0 | 0 | 0 | 0 |
| 80000 | 0 | C | C | C | C | C | C |
| 82000 | 0 | C | C | C | C | C | 0 |
| 84000 | 0 | C | C | C | C | 0 | C |
| 86000 | 0 | C | C | C | C | 0 | 0 |
| 88000 | 0 | C | C | C | 0 | C | C |
| 8A000 | 0 | C | C | C | 0 | C | 0 |
| 8C000 | 0 | C | C | C | 0 | 0 | C |
| 8E000 | 0 | C | C | C | 0 | 0 | 0 |
| 90000 | 0 | C | C | 0 | C | C | C |
| 92000 | 0 | C | C | 0 | C | C | 0 |
| 94000 | 0 | C | C | 0 | C | 0 | C |
| 96000 | 0 | C | C | 0 | C | 0 | 0 |

| HOST ROM ADDRESS (HEX) | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 98000 | 0 | C | C | 0 | 0 | C | C |
| 9A000 | 0 | C | C | 0 | 0 | C | 0 |
| 9C000 | 0 | C | C | 0 | 0 | 0 | C |
| 9E000 | 0 | C | C | 0 | 0 | 0 | 0 |
| A0000 | 0 | C | 0 | C | C | C | C |
| A2000 | 0 | C | 0 | C | C | C | 0 |
| A4000 | 0 | C | 0 | C | C | 0 | C |
| A6000 | 0 | C | 0 | C | C | 0 | 0 |
| A8000 | 0 | C | 0 | C | 0 | C | C |
| AA000 | 0 | C | 0 | C | 0 | C | 0 |
| AC000 | 0 | C | 0 | C | 0 | 0 | C |
| AE000 | 0 | C | 0 | C | 0 | 0 | 0 |
| B0000 | 0 | C | 0 | 0 | C | C | C |
| B2000 | 0 | C | 0 | 0 | C | C | 0 |
| B4000 | 0 | C | 0 | 0 | C | 0 | C |
| B6000 | 0 | C | 0 | 0 | C | 0 | 0 |
| B8000 | 0 | C | 0 | 0 | 0 | C | C |
| BA000 | 0 | C | 0 | 0 | 0 | C | 0 |
| BC000 | 0 | C | 0 | 0 | 0 | 0 | C |
| BE000 | 0 | C | 0 | 0 | 0 | 0 | 0 |
| C0000 | 0 | 0 | C | C | C | C | C |
| C2000 | 0 | 0 | C | C | C | C | 0 |
| C4000 | 0 | 0 | C | C | C | 0 | C |
| C6000 | 0 | 0 | C | C | C | 0 | 0 |
| C8000 | 0 | 0 | C | C | 0 | C | C |
| CA000 | 0 | 0 | C | C | 0 | C | 0 |
| CC000 | 0 | 0 | C | C | 0 | 0 | C |
| CE000 | 0 | 0 | C | C | 0 | 0 | 0 |
| D0000 | 0 | 0 | C | 0 | C | C | C |
| D2000 | 0 | 0 | C | 0 | C | C | 0 |
| D4000 | 0 | 0 | C | 0 | C | 0 | C |
| D6000 | 0 | 0 | C | 0 | C | 0 | 0 |
| D8000 | 0 | 0 | C | 0 | 0 | C | C |
| DA000 | 0 | 0 | C | 0 | 0 | C | 0 |
| DC000 | 0 | 0 | C | 0 | 0 | 0 | C |
| DE000 | 0 | 0 | C | 0 | 0 | 0 | 0 |
| E0000 | 0 | 0 | 0 | C | C | C | C |
| E2000 | 0 | 0 | 0 | C | C | C | 0 |
| E4000 | 0 | 0 | 0 | C | C | 0 | C |
| E6000 | 0 | 0 | 0 | C | C | 0 | 0 |
| E8000 | 0 | 0 | 0 | C | 0 | C | C |
| EA000 | 0 | 0 | 0 | C | 0 | C | 0 |
| EC000 | 0 | 0 | 0 | C | 0 | 0 | C |
| EE000 | 0 | 0 | 0 | C | 0 | 0 | 0 |
| F0000 | 0 | 0 | 0 | 0 | C | C | C |
| F2000 | 0 | 0 | 0 | 0 | C | C | 0 |

Factory set at C8000

| HOST ROM ADDRESS (HEX) | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| F4000 | 0 | 0 | 0 | 0 | C | 0 | C |
| F6000 | 0 | 0 | 0 | 0 | C | 0 | 0 |
| F8000 | 0 | 0 | 0 | 0 | 0 | C | C |
| FA000 | 0 | 0 | 0 | 0 | 0 | C | 0 |
| FC000 | 0 | 0 | 0 | 0 | 0 | 0 | C |
| FE000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

C: CLOSE
O: OPEN

HOST ROM PIN OUT

| | | | |
|---|---|---|---|
| 1 | Address bit 7 | 13 | Data bit 3 |
| 2 | Address bit 6 | 14 | Data bit 4 |
| 3 | Address bit 5 | 15 | Data bit 5 |
| 4 | Address bit 4 | 16 | Data bit 6 |
| 5 | Address bit 3 | 17 | Data bit 7 |
| 6 | Address bit 2 | 18 | Address bit 11 |
| 7 | Address bit 1 | 19 | Address bit 10 |
| 8 | Address bit 0 | 20 | Chip enable low |
| 9 | Data bit 0 | 21 | Address Bit 12 |
| 10 | Data bit 1 | 22 | Address bit 9 |
| 11 | Data bit 2 | 23 | Address bit 8 |
| 12 | Ground | 24 | VCC (+5) |

## 3.3 CONNECTING CABLES

Before the controller can be placed in operation, the cables to the drive and host must be connected. These cables are listed below:

J1 Control Cable (controller to last drive): maximum 20 feet

J2 Data Cable: maximum 20 feet

J3 Data Cable: maximum 20 feet (optional second drive)

Note: Do not attempt to connect a cable to connector J4. Connector J4 is for factory test only.

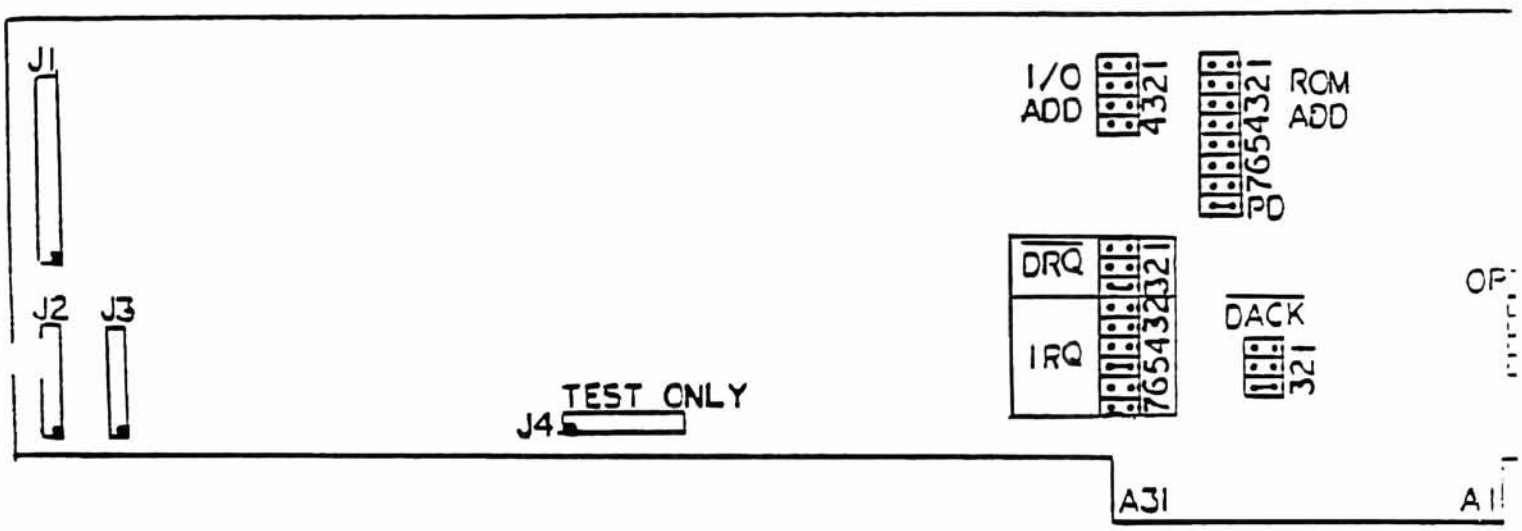



FIGURE 3-1 CABLE, CONNECTOR, AND JUMPER LOCATIONS

# CHAPTER 4
# THEORY OF OPERATION

## 4.1 GENERAL

This chapter discusses the theory of operation of the Xebec Controller and lays down the guidelines that will enable the user to use the Controller successfully in any number of applications.

### 4.1.1 Conventions

Signals or lines can be active in either a high or low state. The terms signal, signal lines, and lines mean the same thing. A low state is equivalent to a voltage level of 0.8 volts or less, and a high state is equivalent to a voltage level of 2.4 volts or more. Some texts use the term asserted to mean active. In this manual, only the term active is used; if the term asserted appears, it is only for reference.

### 4.1.2 Names and Abreviations

A dash (-), or the lack of one, indicates the active state of a signal. The active state of a signal is that state which is required for a given operation. When a dash appears before or is appended to end of a signal name, the signal is active when it is low. When no dash or a plus appears at the end of a signal name, the signal is active when it is high. Some signal lines have two so-called active (or significant) states. When the level on the line is high, a particular operation takes place. When the level on the line is low, a different operation takes place. The following examples show the use of these conventions.

DACK3- The signal DACK3- is active when it is at a low level because it has the dash appended.

DRQ3 The signal DRQ3 is active at a high level because it does not have the dash appended.

Other designations used to define signal lines are listed below.

| | |
|---|---|
| Drv | Driver |
| Rcvr | Receiver |
| OC | Open collector |
| Tri-State | Line has three states: high, low, high impedance |
| 220/330 | Line termination: 220 Ohms to source voltage/330 Ohms to ground. |

## 4.2 CONNECTOR PIN ASSIGNMENTS

Tables 2-7 through 2-8 list the pin assignments of the connectors on the controller board. The tables identify the signals on the pins.

**TABLE 2-7**

**CONNECTOR J1, CONTROL SIGNALS, PIN ASSIGNMENTS**

| Signal Pin | Ground Return | Signal Name |
|---|---|---|
| 2 | 1 | Reduced Write Current |
| 4 | 3 | Head Select $2^2$ |
| 6 | 5 | Write Select Gate |
| 8 | 7 | Seek Complete |
| 10 | 9 | Track 00 |
| 12 | 11 | Write Fault |
| 14 | 13 | Head Select $2^0$ |
| 16 | 15 | Reserved |
| 18 | 17 | Head Select $2^1$ |
| 20 | 19 | Index |
| 22 | 21 | Ready |
| 24 | 23 | Step |
| 26 | 25 | Drive Select 1 |
| 28 | 27 | Drive Select 2 |
| 30 | 29 | Reserved |
| 32 | 31 | Reserved |
| 34 | 33 | Direction In |

TABLE 2-8

CONNECTORS J2 and J3, SIGNALS, PIN ASSIGNMENTS

| Signal Pin | Ground Return | Signal Name |
|---|---|---|
| 1 | 2 | Drive Selected |
| 3 | 4 | Reserved |
| 5* | 6 | Spare |
| 7 | 8 | Reserved |
| 9 | 10 | Spare |
| 11 | 12 | Ground (GND) |
| 13 | | MFM Write Data+ |
| 14 | | MFM Write Data- |
| 15 | 16 | Ground (GND) |
| 17 | | MFM Read Data+ |
| 18 | | MFM Read Data- |
| 19 | 20 | Ground (GND) |

* Pin 5 of J2 and J3 is removed for cable keying.

### 4.2.1 Drive Control Input Signals

The control input signals are of two kinds: those to be multiplexed in a multiple drive system and those that do the multiplexing. The control input signals to be multiplexed are: Reduced Write Current, Write Gate, Head Select Line 0, Head Select Line 1, Head Select Line 2, Step, and Direction. The signal to do the multiplexing is Drive Select 0 and Drive Select 1.

The input lines have the following electrical specifications as measured at the drive.

True: 0.0 volt D.C. to 0.4 volt D.C. @I=40 milliamperes, maximum

False: 2.5 volts D.C. to 5.25 volts D.C. @IL=250 microamperes, maximum

All input lines share a 220/330 ohm resistor pack for line termination. Only the last drive in the chain should have the resistor pack installed.

NOTE: Refer to drive specifications for detailed information of these line.

#### 4.2.1.1 Reduced Write Current

When active, this line, together with Write Gate, causes the write circuitry to write on the disk with a lower write current. This line is set active at the cylinder specified in the initialize command.

When the controller is initialized for more than 8 heads, this line is used for head select $2^3$.

#### 4.2.1.2 Write Select Gate

The active state of this signal (logical zero level) enables write data to be written on the disk. The inactive state of this signal enables the data to be read from the drive. In addition, the inactive state enables the step pulse to step the read/write actuator. MFM write data is sent to the drive within 400 nsec after write is active.

#### 4.2.1.3 Head Select Signals $\overline{2_0}$ $\overline{2_1}$ $\overline{2_2}$

These three lines provide for the selection of each read/write head in a binary coded sequence. Head Select Line $2^0$ is the least significant line. When all Head Select Lines are false, Head 0 is selected.

#### 4.2.1.4 Step

This interface line is a control signal that causes the read/write head to move with the direction of motion defined by the Direction In line.

The access motion is initiated at the logical true-to-logical false transition or the trailing edge of this signal pulse. Change in the Direction In line is made at least 5.0 microseconds before the leading edge of the step pulse.

The minimum pluse width is 5.0 microseconds.

#### 4.2.1.5 Direction In

This signal defines the direction of motion of the read/write head when the Step line is pulsed. An open circuit or logical false defines the direction as "out". If a pulse is applied to the Step line, the read/write heads move away from the center of the disk. If this line is logical true, the direction is defined as "in", and the read/write heads move in toward the center of the disk. The direction line is set a minimum of 5 usec before step pulse are issued.

Seek Complete is verified to be true prior to changing directions and the application of additional step pulses.

#### 4.2.1.6 Drive Select 0, Drive Select 1

These control signals enable the selected drive's input receivers and output drivers. When logically false, the output drivers are open circuits or logically false and the input receivers do not acknowledge signals presented to them.

Drive addresses are assigned on the drive. Refer to Drive Manual for drive selection.

NOTE: Only one drive may be selected at a time.

### 4.2.2 Drive Output Signals

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40 milliamperes in a logical true state with a maximum voltage of 0.4 volt measured at the driver. When the line driver is in the logical false state, the driver transistor is off, and the collector cutoff is a maximum of 250 microamperes.

All output lines are enabled by the respective Drive Select lines.

#### 4.2.2.1 Seek Complete

This line goes true when the read/write heads have settled on the final track at the end of a seek. Reading or writing is not attempted when Seek Complete is false.

#### 4.2.2.2 Track 000

This interface signal indicates a true state only when the drive's read/write heads are positioned at Track 000, the outermost data track.

#### 4.2.2.3 Write Fault

This signal is used to indicate that a condition exists at the drive that could cause improper writing on the disk. When this line is true, further writing is inhibited.

#### 4.2.2.4 Index

This interface signal is provided by the drive once each revolution (16.7 milliseconds nominal) to indicate the beginning of the track. Normally, this signal is logical false and makes the transition to logical true to indicate Index. This line is edge detected on the logical false to logical true transition. The minimum pulse width is 200 nsecs, with the maximum pluse width less than one revolution of the disk.

#### 4.2.2.5 Ready

When true, this interface signal, together with Seek Complete, indicates that the drive is ready to read, write, or seek, and that the I/O signals are valid. When this line is false, all controller-initiated functions are inhibited.

#### 4.2.2.6 Select Status

A status line is provided at the J2,J3 connector to inform the controller of the selection status of the drive. This line is used to determine which port the drive data cable is connected.

### 4.2.3. Drive Data Transfer Signals

Data lines associated with the transfer of data between the drive and the Controller are differential in nature and may not be multiplexed. These lines are provided at the J3,J2 connector. Signal levels are defined by RS-422A.

Two pairs of balanced lines are used for the transfer of data: MFM Write Data and MFM Read Data.

#### 4.2.3.1 MFM Write Data

This is a differential pair of lines that defines the flux transition to be written on the track. The transition of the +MFM Write Data line going more positive than the -MFM Write Data line causes a flux reversal on the track if the Write Gate is active. This signal is driven to an inactive state (+MFM Write Data more negative then -MFM Write Data) by the Controller when in a read mode. Write Gate is inactive.

The delay from the leading edge of Write Gate to the Write Data pulse is 400 nanoseconds maximum.

#### 4.2.3.2 MFM Read Data

The data recovered by reading a prerecorded track is transmitted to the Controller via the differential pair of MFM Read Data lines. The transition of the +MFM Read Data lines going more positive then the -MFM Read Data line represents a flux reversal on the track of the selected head. This line is edge detected, minimum active pulse width is 50 nsec, maximum active pulse width is 150 nsec.

## DETAILED EXPLANATION OF THE XEBEC INTEGRATED 5¼" WINCHESTER DISK CONTROLLER

The signals which are used on the XEBEC disk controller from the CPU I/O bus are as follows:

| IBM SIGNAL | PIN NAME | FUNCTION |
|---|---|---|
| A19-A0 | A12-A31 | This is a positive true 20 bit address. The Least significant 10 bits contain the I/O address within the range 300 to 33F when an I/O read or write is executed by the IBM CPU. The full 20 bits are decoded to address the on-board Read Only Memory (ROM) between addresses 08000 and F9FFF. |
| D7-D0 | A2-A9 | This is a positive 8 bit data bus over which data and status information is passed between the host and the controller. |
| IOR- | B14 | This is a negative true signal which is asserted when the host reads status or data from the controller under either programmed I/O or DMA control. |
| IOW- | B13 | This is a negative true signal which is asserted when the host sends command or data information to the controller under either programmed I/O or DMA control. |
| AEN | A11 | This positive true signal is asserted when the DMA in the host is generating the I/O read (IOR-) or I/O write (IOW-) signals and has control of the address and data buses. |
| RESET | B2 | This is a positive true signal which forces the disk controller card to its initial power up condition. |

| | | |
|---|---|---|
| IRQ2-IRQ7 | B04(IRQ2)<br>B25(IRQ3)<br>B24(IRQ4)<br>B23(IRQ5)<br>B22(IRQ6)<br>B21(IRQ7) | This is a positive true interrupt request signal which is asserted by the controller card when the programmed interrupt condition occurs in the controller. The controller can be jumpered to interrupt the IBM central processor by installing the jumper in the proper connector. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. The board is shipped from the factory with IRQ5 installed. |
| DRQ1<br>DRQ2<br>DRQ3 | B18<br>B6<br>B16 | This is a positive true DMA request signal which is asserted by the disk controller when data is available for transfer to or from the controller under DMA control. This signal remains active until the DMA acknowledge signal (DACK-) is activated in response by the host DMA channel. There are three possible DMA channels available for data transfer in the IBM PC with DRQ1 as the highest priority and DRQ3 as the lowest. The board is shipped from the factory with DRQ3 installed. |
| DACK1-<br>DACK2-<br>DACK3- | B17<br>B26<br>B15 | This signal is negative true and is generated by the host DMA channel in response to a DMA request (DRQ). When the controller is Busy, the DACK is asserted, the controller sources the data bus, D7-D0. The board is shipped from the factory with DACK3- installed. |
| | NOTE: | The DRQ and DACK line must be selected at the same level. i.e., DRQ1 and DACK1. |

## IBM HOST INTERFACE HARDWARE DESCRIPTION

The following section will be referring to functional blocks the names of which appear next to the appropriate circuit or the schematic of the interface section of the controller.

### I/O ADDRESS COMPARATOR

This circuit compares the I/O address being sent on the CPU address bus with the controller I/O address select jumper blocks. The disk controller card requires 4 contiguous I/O read and write addresses for operation so the 2 Least significant address bits (A0, A1) are decoded directly by the I/O port decoder. (These addresses will be referred to as controller read ports 0 thru 3 and controller write ports 0 thru 3).

The true or complemented form of the next four address bits (A2, A3, A4, A5) are jumper selectable so that up to 16 controllers can reside on the CPU I/O bus simultaneously. The four jumper selectable address groups are as follows:

| I/O ADDRESS | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 300 | C | C | C | C |
| 304 | C | C | C | 0 |
| 308 | C | C | 0 | C |
| 30C | C | C | 0 | 0 |
| 310 | C | 0 | C | C |
| 314 | C | 0 | C | 0 |
| 318 | C | 0 | 0 | C |
| 31C | C | 0 | 0 | 0 |
| 320 | 0 | C | C | C |
| 324 | 0 | C | C | 0 |
| 328 | 0 | C | 0 | C |
| 32C | 0 | C | 0 | 0 |
| 330 | 0 | 0 | C | C |
| 334 | 0 | 0 | C | 0 |
| 338 | 0 | 0 | 0 | C |
| 33C | 0 | 0 | 0 | 0 |

C: CLOSE
O: OPEN

I/O PORT DECODER

The two least significant bits of the address bus are sent to the host I/O port decoder. There are two sections to the decoder, one section is enabled by the IBM I/O read signal (IOR-) and the other by the I/O write signal (IOW-). This results in 4 read ports and 4 write ports being assigned to the disk controller board. These will be referred to throughout this writeup as controller write ports 0 thru 3 and controller read ports 0 thru 3.

The AEN signal is asserted by the CPU host when DMA is in control of the data transfer. When AEN is asserted, the I/O port decoder is disabled.

The functions of the four read and four write ports are as follows:

| READ PORT | FUNCTION |
|---|---|
| 0 | Read data (from controller to CPU) |
| 1 | Read controller hardware status (controller to CPU) |
| 2 | Read option jumpers (controller to CPU) |
| 3 | Not used |

| WRITE PORT | FUNCTION |
|---|---|
| 0 | Write data (from CPU to controller) |
| 1 | Controller reset |
| 2 | Generate controller select pulse |
| 3 | Write interrupt and DMA mask register |

## CONTROLLER HARDWARE STATUS BUS DRIVER (TO HOST)

The controller hardware status is driven onto the IBM data bus when an I/O read is issued by the host program to controller read port 1.

The bits in the controller hardware are defined as follows:

| BIT | USAGE |
|---|---|
| 7 | Not used (MSB) |
| 6 | Not used |
| 5 | Interrupt pending (interrupt request flip-flop set) |
| 4 | DMA Request pending (DMA request flip-flop set) |
| 3 | Controller busy (BUSY). This bit is asserted in response to the select signal. Busy remains asserted until 20 microseconds following the input of the status byte at the end of a command. Select must not be set active until Busy is inactive. Busy enables the data path and handshake signals between the controller and the CPU. |
| 2 | +Command/-Data<br>1=Command byte on data bus, 0=Data byte on data bus. |
| 1 | +Hostin/-Hostout - transfer direction signal from the controller.<br>0=Command or data info is being sent to the controller<br>1=Status or data info is being sent by the controller |
| 0 | Request signal from the controller (REQUEST). If this bit=1, the request line is set by the controller indicating that a data or status byte is available from the controller during an input operation or when set on an output operation, the controller is ready to accept the next byte. The status of this signal is available as part of the hardware status so that the programmed I/O handshakes may be performed by the CPU. When the host transfers the byte of data, Request is cleared within 750 nsec from the end of the transfer. Do not send or receive bytes if REQUEST is not set. |
| NOTE: | Not Used bits may be high or low. |

DMA AND INTERRUPT MASK REGISTER

This is a 2 bit register which is written into by the host when it writes to controller I/O port 3. If neither bit 1 or 0 is active, the selected DMA and interrupt line to the host is set to the high impedance state.

The meaning of the bits in the Interrupt Mask Register are as follows:

| BIT | USAGE |
|---|---|
| 2 - 7 | Not used. |
| 1 | This bit is tied directly to the direct clear of the interrupt request flip flop. When this bit is set it allows the interrupt flip flop to be set by the return status byte sent by the controller at the end of the command. By clearing this bit, the host can acknowledge the interrupt and clear out the interrupt request. The interrupt line (IRQ) is in the high impedance state when this bit is reset.<br>NOTE: The Interrupt mask bit must be enabled before enabling the Interrupt bit on the host CPU. If this is not done, then false Interrupts can occur. |
| 0 | This bit is tied directly to the direct clear of the DMA request flip flop. When this bit is set, it allows the REQEST signal from the controller to activate the DMA request signal to the host (DRQ) to complete a DMA data handshake. If reset DRQ is in the high impedance state.<br>NOTE: The DMA mask bit must be enabled before enabling the DMA channel on the host CPU. If this is not done, the data request line will not be driven, while the host channel is active and false handshakes can occur. |

This register is cleared on a hardware reset (RESET line going high on the IBM bus) or a programmed reset (write to controller port 1), or by writing 0 into the register bits. Set the interrupt mask bit at beginning of CMD and reset before transfer of the status byte.

READ OPTION JUMPERS

The option jumpers are driven onto the data bus when an I/O read is issued to controller port 2. When a jumper is installed, it is read as a low (inactive); when a jumper is removed it is read as a high (active) state.

The option jumpers are defined below:

| BIT | USAGE |
|---|---|
| 4-7 | not used |
| 3 | jumper 1 |
| 2 | jumper 2 |
| 1 | jumper 3 |
| 0 | jumper 4 |

CONTROLLER BUS STATUS DECODE

The four possible combinations of the +command-data and +Hostin/-Hostout signals (valid only when REQUEST is active) from the controller's hardware status are as follows:

| +C-D | +I-O | CONDITION |
|---|---|---|
| High | Low | Command mode, bus driven to the controller. This condition exists when the host is sending command information to the controller. |
| Low | Low | Data mode, bus driven to the controller. This condition exists when the host is sending data to the controller, by either programmed I/O or DMA modes. |
| High | High | Status mode, bus is driven by the controller. This condition exists when the controller is sending status information to the CPU. Transferring this byte terminates the command, and BUSY from the controller is set inactive. One byte is transferred at the end of each command. The interrupt line is set if enabled, when the byte is ready to transfer. |

| | | |
|---|---|---|
| Low | High | Data mode, bus is driven by the controller. This condition exists when the controller is sending data to the host, under either programmed I/O or DMA modes. |

INTERRUPT REQUEST FLIP FLOP

This flip flop is set when enabled, and the controller is ready to send the return status byte at the end of each command. This flip flop is enabled by bit 1 in the interrupt mask register which is tied directly to the clear input. The output of this register is connected through a tri-state driver to the interrupt request line (IRQ) on the CPU I/O connector. This flip flop is cleared on a hardware reset (RESET line going high on the bus) or a programmed reset (write to controller port 1), or clearing the interrupt mask bit 1.

DMA REQUEST FLIP FLOP

This flip flop is set (if enabled by bit 0 of the interrupt mask register) by the positive going edge of the request line from the controller when data is being written to or read from the controller. The output of this flip flop is connected to the DMA request line (DRQ) through a tri-state driver. This flip flop is reset by the DMA acknowledge signal (DACK-) from the DMA channel or clearing the interrupt mask bit 0.

### 4.3.5 Command Sequence

- Set busy
- Issue 6 command bytes
- Transfer data if required
- Interrupt on status
- Read status
- Command complete

## 4.4 PROGRAMMING INFORMATION

The following paragraphs discuss communications between the controller and host from the point of view of the codes that are passed. The host sends commands to the controller, the controller then performs the commands and reports back to the host.

## 4.5 COMMANDS

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Figure 4-5 shows the composition of the DCB. The list that follows Figure 4-5 defines the bytes that make up the DCB.

At the end of a command, the controller returns a status byte to the host. The format of the byte is shown in Figure 4-5a.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | Cmd class | | | | Opcode | | | |
| Byte 1 | 0 | 0 | LUN | | Head Number | | | |
| Byte 2 | CYL. Hi | | | | Sector Number | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | Interleave or Block Count | | | | | | | |
| Byte 5 | Control Field | | | | | | | |

**Figure 4-5 Device Control Block (DCB), Format**

Byte 0 Bits 7, 6 and 5 identify the class of the command. Bits 4 through 0 contain the opcode of the command.

Byte 1 Bit 5 identifies the logical unit number (LUN). Bits 4 through 0 contain the disk head number. Bits 7 and 6 are not used.

Byte 2 Bits 7. and 6 contain 2 most signficant bits of cylinder numbers. Bits 4 through 0 contain the sector number. Bit 5 is not used.

Byte 3 Bits 7 through 0 contain the least significant 8 bits of the cylinder number.

Byte 4 Bits 7 through 0 specify the interleave or sector count.

Byte 5 Bits 7 through 0 contain the control field.

### 4.5.1 Control Byte

The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The format of this byte is as follows:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | r | a | 0 | v | s | s | s | s |

Bits 3-0 Define the drive type. The bit assignments are listed below:

The step options are encoded in control byte 5 of the command descriptor, the encoding is done with bits 0 thru 3 as follows:

| s 3 | s 2 | s 1 | s 0 | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Default 3 msec step rate |
| 0 | 0 | 0 | 1 | Spare (not used) |
| 0 | 0 | 1 | 0 | Spare (not used) |
| 0 | 0 | 1 | 1 | Spare (not used) |
| 0 | 1 | 0 | 0 | 200 usec buffered step |
| 0 | 1 | 0 | 1 | 70 usec buffered step |
| 0 | 1 | 1 | 0 | 30 usec buffered step |
| 0 | 1 | 1 | 1 | 15 usec buffered step |
| 1 | 0 | 0 | 0 | |
| thru 1 | 1 | 1 | 1 | Spare (for future use) |

Refer to the drive manufacturer manual in configuring the drive for fast step options. Do not use spare options as seek errors may occur.

Note: Other drive options are to be determined, set unused bits to 0.

Bit 4 If set to one, indicates the disk drives have disk servo information prior to index on each track. These "Imbedded Servo" drives use this servo information to control the rotational speed of the drive and to control position of the read/write head over the track. (Set this bit on format commands with imbedded servo drives.)

Bit 6 If set to zero, on Read commands, and an ECC error is detected, a reread is attempted. If no error is detected on the reread, than the command completes with no error status. If an ECC error is detected on a reread, correction is attempted, and the result reported to the host. If this bit is set to 1, no reread is attempted, and correction is performed on all ECC errors.

Bit 7 Disable the four retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive.

### 4.5.2 Status Byte Format

One byte of status is passed to the host at the end of each command. The byte informs the host if any errors occurred during the execution of the command. If interrupts are enabled, then the controller will send an interrupt when ready to transfer the status byte. The interrupt enable should be reset before handshaking the status byte.

After the byte is transferred, the command is completed, and BUSY from the controller is set inactive within 20 microseconds.

**Status Byte**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | d | 0 | 0 | 0 | ERR | 0 |

Bits 0, 2-4,6,7 Set to zero.

Bit 1 When set, error occurred during command execution.

Bit 5 Logical unit number of drive, d=0 or 1.

**Figure 4-5a Completion Status Byte**

COMMAND DESCRIPTION

Each command is described below. The description includes its class, opcode, and format. When a slash (/) represents a bit position, the slash means that the value of that bit is not important (a don't-care bit). These should be set to 0.

### 4.5.3 Test Drive Ready (Class 0, Opcode 00)

This command selects the drive specified by the byte 1 of DCB and read back the status from that drive. If all status bits are in the correct state, the command will not return an error code. If the drive status is not OK, the command will return an error code, usually DRIVE NOT READY, or DRIVE STILL SEEKING.

This command is usually used in 2 occasions:

A) When initially power on, the host should issue this command continuously with appropriate time out loop to insure the drive spins up to speed and comes ready.

B) When implementing overlapped seeks. First, issue a seek command to the 1st drive, then issue another seek command to the 2nd drive. Now keep issuing a TEST DRIVE READY command to each drive until either drive finishes its seek operation. Then continue with the normal READ/WRITE operation on that drive. The following diagram shows the format of the device control block for this command.

d = drive, 0 or 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Byte 1 | 0 | 0 | d | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

### 4.5.4 Recalibrate (Class 0, Opcode 01)

This command will move the drive arm to the track 00 position. This command should only be used to attempt to correct a drive position error, since it is slower than a direct seek to track 0. Also, if retrys are enabled, the Controller will recalibrate automatically in case of error. The difference between this command and a direct seek to track 0 is this command steps the drive one cylinder at a time looking for the signal TRACK00 from the drive to become active. A direct seek to track 0 is faster because the Controller steps the drive at the programmed step rate.

d = drive, 0 or 1
r = retries
s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Byte 1 | 0 | 0 | d | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

### 4.5.5 Reserved (Class 0, Opcode 02)

This opcode is not used.

### 4.5.6 Request Sense Status (Class 0, Opcode 03)

The status reported by this command corresponds to the drive addressed by Byte 1 of the DCB, i.e., separate status bytes are maintained for each drive. Status is updated after each command, so status clarifying an error previously reported to the host should be read before the next command to the same drive. Four bytes are sent to the host describing drive and controller status; the formats of these four bytes are shown after the DCB. The tables that follow the formats list the error codes.

When an error occurs on a multiple sector data transfer, (read or write), the Request Sense Status command returns the address of the failing sector in bytes 1, 2 and 3. If the Request Sense Status command is issued after any of the Format commands then the address returned by the controller points to one sector beyond the last track formatted if there was no error. If there was an error, then the address returned points to the track in error.

d = drive, 0 or 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Byte 1 | 0 | 0 | d | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

**Sense Bytes**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | SEE BELOW | | | | | | | |

| | |
|---|---|
| Bits 0-3 | Error Code |
| Bits 4-5 | Error Type |
| Bit 6 | Spare, set to zero |
| Bit 7 | Address valid, when set |

The address valid bit in the error code byte (bit 7) is set only when the previous command required a disk address, in which case it is always returned as a one; otherwise it is set to zero. For instance, if a Recalibrate command is followed immediately by a Request Sense Status command, the address valid bit would be returned as zero since this command does not require a disk address to be passed in its DCB.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | (see above) | | | | | | | |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | | Sector Number | | | |
| Byte 3 | Cylinder Low | | | | | | | |

d = drive, 0 or 1

**Table 4–6 Type 0 Error Codes, Disk Drive**

| HEX CODE | DEFINITION |
|---|---|
| 01 | No Index Signal from the Drive. This error occurs during any data transfer or format command if a normal drive select occurs, the drive is ready, but no index signal is detected from the drive within two revolutions of the disk.<br>Possible error causes are:<br>- Bad Drive<br>- Control Cable (J1)<br>- Controller |
| 02 | No Seek Complete Signal from the Drive. This error occurs on non buffered seek processing if the controller does not receive the Seek Complete signal from the Drive within one second following the last step pulse.<br>Possible error causes are:<br>- Bad Drive<br>- Control Cable (J1)<br>- Controller |
| 03 | Write Fault Signal Received from the Drive. This error occurs if the controller detects an active write fault signal from the disk drive either at the completion of a sector data transfer or initially after a successful drive select and the drive indicates ready.<br>Possible error causes are:<br>- Drive power supply voltages out of range<br>- Bad Drive<br>- Control Cable (J1)<br>- Unit Cable (J2, J3)<br>- Controller |

| HEX CODE | DEFINITION |
|---|---|
| 04 | Disk Drive Not Ready. This error occurs if the controller fails to receive the select signal from the drive, or the drive indicates not ready after selection.<br>Possible error causes are:<br>- Drive power supply voltages out of range<br>- Drive not yet up to operating speed following power on<br>- Bad Drive<br>- Control Cable (J1)<br>- Controller |
| 05 | Not used. |
| 06 | Track 00 Not Found. After stepping the drive 200 more steps than the number of cylinders during a recalibrate command, the Track 00 Signal was not received from the drive.<br>Possible error causes are:<br>- Incorrect Drive Size Initialization (too few cylinders)<br>- Bad Drive<br>- Control Cable (J1)<br>- Bad Controller |
| 07 | Not used. |
| 08 | Disk Drive Still Seeking. This status is returned in response to a test drive ready command if a buffered step seek was issued to a drive and the drive has not returned the seek complete signal. Software must time the seek to insure no system hang occurs if the drive fails to return the seek complete signal. Treat a seek incomplete condition the same as error code 02. |

**Table 4-7 Type 1 Error Codes, Controller**

| HEX CODE | DEFINITION |
|---|---|
| 10 | ID Field Read Error. During a data transfer or format command, address marks were detected, but the target sector was not found and an ECC error occured on one or more ID fields.<br>Possible error causes are:<br>- Media Defect on Drive<br>- Bad Drive (If errors are excessive or continuous)<br>- Bad Controller (If errors are excessive or continuous)<br>Media defects may be overcome by deleting the defective sectors from system use. |
| 11 | Uncorrectable Data Error in the Data Field. The controller detected a data error that could not be corrected using ECC.<br>Possible error causes are:<br>- Media Defect on Drive<br>- Bad Drive (If errors are excessive or continuous)<br>- Bad Controller (If errors are excessive or continuous)<br>Media defects may be overcome by deleting the defective sectors from system use. |
| 12 | Sector Address Mark Not Found. The controller did not detect an address mark (AM) from the drive within its timing window. An address mark is a special recording pattern preceeding the ID field of a sector. The AM is only written at format time. The AM tells the controller where new sector starts. The error may occur during any data |

| HEX CODE | DEFINITION |
|---|---|
| | transfer or format commands. The error may mean that no address marks were detected on the track, or the target sector address mark was not detected.<br>Possible error causes are:<br>- Media Defect on Drive<br>- Drive has not been Formatted<br>- Bad Drive<br>- Bad Unit Cable (J2, J3)<br>- Bad Controller<br>Media defects may be overcome by deleting the defective sectors from system use. |
| 13 | Not used. |
| 14 | Target Sector Not Found. The target sector was not located within two revolutions of the disk. This error usually occurs when there is a media defect in the address mark field of the target sector.<br>Possible error causes are:<br>- Media Defect on Drive<br>- Bad Drive<br>- Bad Controller |

| HEX CODE | DEFINITION |
|---|---|
| 15 | Seek Error. After a seek, the target disk address did not match the ID address read from the disk. Either the cylinder or head bytes did not match. Possible error causes are:<br>- Incorrect Seek Option Specified in the Command<br>- Bad Drive<br>- Bad Control Cable (J1)<br>- Bad Controller |
| 16 | Not used. |
| 17 | Not used. |
| 18 | Correctable Data Error. The controller detected a media error while reading that was corrected by ECC. This error code informs the host sofware that error correction has taken place. This is the only error where the data is passed to the host before returning the error status. |
| 19 | Track is Flagged Bad. The last data transfer command encountered a track that had been flagged defective using the format Bad Track Command. Host software is responsible for insuring that deleted tracks are never accessed. |
| 1A-1F | Not used. |

**Table 4–8 Types 2 and 3 Error Codes, Command and Miscellaneous**

| HEX CODE | DEFINITION |
|---|---|
| 20 | Invalid Command: The controller has received an invalid command from the host. |
| 21 | Illegal Disk Address: The controller detected an address that is beyond the maximum range. |
| 22 | Illegal Parameter: The controller detected an invalid passed parameter. |
| 30 | RAM Error: The controller detected a data error during the RAM sector-buffer diagnostic. Replace the controller. |
| 31 | Program Memory Checksum Error: The controller was unable to obtain a match between the calculated and compare checksum values. This is caused by a defect in the program memory chip of the Controller. Replace the Controller. |
| 32 | ECC Polynomial Error: During the controller's internal diagnostic, the hardware ECC generator failed its test. Replace the controller. |

The following is a summary of the error codes returned as the result of the Request Sense Status command.

NOTE: The address valid bit (bit 7) may or may not be set and is not included here for clarity.

| Error Code (hex) | Meaning. |
|---|---|
| 00 ..... | No error detected (command completed ok). |
| 01 ..... | No index detected from disk drive. |
| 02 ..... | No seek complete from disk drive |
| 03 ..... | Write fault from disk drive |
| 04 ..... | Drive not ready after it was selected. |
| 05 ..... | Not used. |
| 06 ..... | Track 00 not found. |
| 07 ..... | Not used. |
| 08 ..... | Drive still seeking. |
| 09-0F ..... | Not used. |
| 10 ..... | ID field read error. |
| 11 ..... | Uncorrectable data error. |
| 12 ..... | Address mark not found. |
| 13 ..... | Not used. |
| 14 ..... | Target sector not found. |
| 15 ..... | Seek error. |
| 16-17 ..... | Not used. |
| 18 ..... | Correctable data error. |
| 19 ..... | Bad track flag detected. |
| 1A-1F ..... | Not used. |
| 20 ..... | Invalid command. |
| 21 ..... | Illegal disk address. |
| 22 ..... | Illegal drive parameter error. |
| 23-2F ..... | Not used. |
| 30 ..... | Ram diagnostic failure. |
| 31 ..... | Program memory checksum error. |
| 32 ..... | ECC diagnostic failure. |
| 33-3F ..... | Not used. |

### 4.5.7 Format Drive (Class 0, Opcode 04)

This command recalibrates the drive, then seeks to the starting address specified by the byte 1, 2 and 3 of the DCB. It times the spindle speed, divides the track into equal size sectors, and writes out address mark (AM) and header field for all sectors. The contents of the sector buffer is used for the data pattern of the sector data fields. The sector buffer can be initialized by the Write Sector Buffer command (Opcode 0F hex) just before any Format command. Note that if the format command gets a hard error while formatting a track, the format operation stops immediately and the error is reported. To continue, the host software must provide the data fields for all logical sectors following the sector in error, then continue with the format command at the beginning of the next track. Also note that the format operation always starts at the first sector of track, even though the address specified in the DCB did not point to a track boundry.

If Bit 4 is set to one, the controller sets the format timing for an imbedded servo drive. If Bit 4 is set to zero, format timing is set for a conventional drive. It is the customer's responsibility to insure proper use of this feature. Formatting with the bit set incorrectly will likely result in irrecoverable disk errors. In this case, the drive must be reformatted with Bit 4 set properly. If the imbedded servo format is selected, the firmware times the disk rotation, subtracts off a 300 microsecond gap for the servo area, and formats the track. This firmware will work properly with drives that have a servo area that is smaller than 300 microseconds preceeding index and 40 microseconds following the leading edge of the index pulse; and the worst-case spindle speed variation falls within 3536 +/- 3.0% RPM for an inbedded servo drive, 3600 +/-3.0% RPM for a conventional drive. All drives must maintain speed tolerance of $\pm$ 1% after format.

d = drive, 0 or 1

r = retries

s = step option

v = imbedded servo drive

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | 0 | 0 | 0 | Interleave | | | | |
| Byte 5 | r | 0 | 0 | v | s | s | s | s |

Interleave:

1 to 16 for 512 byte sectors

### 4.5.8 Read Verify (Class 0, Opcode 05)

This command is identical to the Read command except no data transfer takes place. Starting at the initial address, the command varifies header and data ECC on the specified number of sectors. If an error occurs the request sense bytes contain the sector number in error.

d = drive, 0 or 1

r = retries

a = retry option data ECC error

s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | Block Count | | | | | | | |
| Byte 5 | r | a | 0 | 0 | s | s | s | s |

### 4.5.9 Format Track (Class 0, Opcode 06)

This command recalibrates the drive, seeks to the target track specified in byte 1, 2 and 3 of the DCB, and writes the ID and DATA fields with the interleave value specified in byte 4 of the DCB. This command can be used to clear the defective track bit, or to reformat one track that lacks data integrity on a drive. This command writes the contents of sector buffer as the data pattern of the data field.

NOTE: The v bit must be set for embedded servo drives.

d = drive, 0 or 1

r = retries

s = step option

v = imbedded servo drive option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Number Low | | | | | | | |
| Byte 4 | 0 | 0 | 0 | Interleave | | | | |
| Byte 5 | r | 0 | 0 | v | s | s | s | s |

Interleave:

1 to 16 for 512 byte sectors

### 4.5.10 Format Bad Track (Class 0, Opcode 07)

This command is the same as FORMAT TRACK command except the BAD TRACK flag is set in the ID field. DATA fields are not written. This command is used to prevent system access to defective tracks.

NOTE: The v bit must be set for embedded servo drives.

d = drive, 0 or 1

r = retries

s = step option

v = imbedded servo disk

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low | | | | | | | |
| Byte 4 | 0 | 0 | 0 | Interleave | | | | |
| Byte 5 | r | 0 | 0 | v | s | s | s | s |

Interleave:

1 to 16 for 512 byte sectors

### 4.5.11 Read (Class 0, Opcode 08)

This command will read 1 to 256 sectors as specified by the byte 4 of the DCB. The starting address is specified by byte 1, 2 and 3 of the DCB. If an error occurs during a multiple sector transfer, the transfer will terminate at the sector where the error occurs. For example, assume the user wants to read 10 sectors starting at sector address 10. If a correctable data error occurs at sector address 15, the Controller completes the transfer of 6 sectors, including the sixth one because the data was corrected. It terminates the read operation and sets the completion status byte error bit high. The host issues REQUEST SENSE Command to determine what error has occured. To continue the operation, the host calculates the difference between sectors desired and sectors completed. In this case, 6 out of 10 are completed, therefore, the host should issue a second read command of 4 remaining sectors at starting sector address 16. If any other error code occured, the data is not returned to the host, so the retry logical address is one sector less, and the retry sector count one sector more than the continuation after a correctable data error. In the previous example, the restart sector address is 15, and the transfer length is 5 sectors for any error other than a correctable data error.

d = drive, 0 or 1

r = retries

a = retry option on data ECC error

s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | Block Count | | | | | | | |
| Byte 5 | r | a | 0 | 0 | s | s | s | s |

### 4.5.12 Reserved (Class 0, Opcode 09)

This opcode is not used.

### 4.5.13 Write (Class 0, Opcode 0A)

This command will write from 1 to 256 sectors as specified by the byte 4 of the DCB, starting at the address specified by bytes 1, 2 and 3 of the DCB. The multiple sector transfer scheme works the same as the READ command. Each sector of data is 512 bytes long.

d = drive, 0 or 1

r = retries

s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low | | | | | | | |
| Byte 4 | Block Count | | | | | | | |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

### 4.5.14 Seek (Class 0, Opcode 0B)

This command initiates a seek to the track and selects the head number specified in the DCB. The drive must be formatted.

For drives employing buffered step seeks, seek commands can be overlapped. After the controller issues a seek to the drive, it returns with a completion status, not waiting for the drive to complete the seek. If the return status shows no error, than the seek was issued correctly. If there is an error, than the seek was not issued. After transferring the status, another command can be issued to either drive. If a new command is received for a drive with an outstanding seek,. then the

controller will wait, with Busy active, for the seek to complete before executing the new command (Except Drive Ready Command). There is a 500 millisecond timeout on this wait. If the Seek does not complete, a Seek Timeout error (Hex 02) is returned.

The Test Drive Ready command can be used with overlapped seeks to determine when a drive has completed seeking before issuing the next command. If the drive is still seeking, the status byte at the end of the command will indicate an error, and the sense status will indicate "drive still seeking" (type 0 error, code 8). A sequence of Test Drive Ready commands can thus be used to determine when the drive is ready for the next command.

Byte 5 of the DCB of this command instructs the Controller what type of seek algorithm to execute for this drive. There are currently 5 different seek types supported in this firmware, both buffered and non buffered modes. Buffered Step Drives are supported at 15, 30, 70, or 200 microseconds per step. Buffer step means the drive has seek intelligence built-in. It can accept step pulses at a fast rate, typically under 200 microseconds per step. After the Controller stops sending the drive step pulses (i.e. the Drive does not receive any more pulses within its timeout limit), the Drive seeks based on its own stepping algorithm (typically from firmware built-in to the drive). This scheme allows the Controller to finish the command without having to process the physical seek operation, making overlapped seeks possible. The last step rate is default 3 msec per step. This is used on all non-buffered drives.

d = drive, 0 or 1

r = retries

s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | / | / | / | / | / |
| Byte 3 | Cylinder Low | | | | | | | |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

### 4.5.15 Initialize Drive Characteristics (Class 0, Opcode 0C)

This command enables the user to configure the Controller to work with drives that have different capacities and characteristics. However, the characteristics of both drives are initialized at the same time. If drives of different characteristics are used, the command must be issued when switching between drives.

After the host sends the command (DCB) to the controller, it then sends and eight-byte block of data that contains the drive parameters. Some of the parameters occupy two bytes; all two-byte parameters are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

C= Maximum number of cylinders (2 bytes)
H= Maximum number of heads (1 byte)
W= Reduce write current cylinder (2 bytes)
P= Increase write precompensation cylinder (2 bytes)
E= Maximum ECC data burst length (1 byte)

When the controller is powered up or reset, the default values listed below are set.

Maximum number of cylinders = 306
Maximum number of heads = 4
Starting reduced write current cylinder = 306
Increase write precompensation cylinder = 306
Maximum ECC data burst length = 11 bits

The drive size parameters passed are relative to one. For example, if the drive has 306 cylinders and 6 heads, then the value of C is 306 and the value of H is 6. For the W and P parameters, the value specifies the cylinder number at which the event occurs. For example, if the value of W is set to 200, write current will be reduced starting at cylinder 200 and higher.

The controller offers precompensation values of 0, 5, and 10 nanoseconds. The most significant bit of the most significant byte of the "p" parameter determines the compensation value. If this bit is set to one, zero nanoseconds compensation is used below the P cylinder, and 10 nanoseconds is used at and above the P cylinder. If the most significant bit is set to zero, five nanoseconds compensation is used below the P cylinder, and 10 nanoseconds is used at or above the P cylinder. Usually, oxide media drives require the 5-10 nanosecond compensation at some intermediate cylinder value. Plated media drive require no compensation over the entire cylinder range. In this case, set the most significant bit of the P parameter to one, and set the cylinder value of P to the same value as the C parameter. These are only suggested methods, consult the disk drive technical manual for precompensation details.

The parameter for the maximum ECC burst length defines the length of a burst error in the data field that the controller will correct. The burst length is defined as the number of bits from first error bit to the last error bit. For example, the controller detected a 5-bit ECC error and the erroneous data appeared as C5 (1100 0101), before correction and could appear as D4 (1101 0100) after the correction.

However, if the host has set the maximum ECC burst length at 4 bits, the controller would flag this data as uncorrectable. This is a type 1, code 1 error.

## COMMAND BYTES

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

## Parameter Bytes

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | C | C | C | C | C | C | C | C |
| Byte 1 | C | C | C | C | C | C | C | C |
| Byte 2 | 0 | 0 | 0 | 0 | H | H | H | H |
| Byte 3 | W | W | W | W | W | W | W | W |
| Byte 4 | W | W | W | W | W | W | W | W |
| Byte 5 | P | P | P | P | P | P | P | P |
| Byte 6 | P | P | P | P | P | P | P | P |
| Byte 7 | 0 | 0 | 0 | 0 | E | E | E | E |

### 4.5.16 Read ECC Burst Error Length (Class 0, Opcode 0D)

This command is only valid following a Correctable Data Error (Error Code 18 Hex). It will transfer one byte to the host indicating the length of the error corrected. The error length is determined by counting the number of bits between the first and the last bit in error, including the first and the last bits. For example:

Assume the drive is formatted with the default format data pattern 6C Hex. The first 2 bytes expanded to the binary level has the pattern — 0110 1100 0110 1100. This is the 2 byte pattern stored on the disk. Now, if the data read back from the disk has an error, then:

| | | ERROR BURST LENGTH |
|---|---|---|
| CORRECT PATTERN | : 0110 1100 0110 1100 | 0 |
| READ BACK PATTERN | : 0111 1100 0110 1100 | 1 |
| READ BACK PATTERN | : 0111 1100 1110 1100 | 6 |
| READ BACK PATTERN | : 0111 1100 0110 1110 | 12 |

From the 3 pattern read above, the first and second patterns are correctable because the error bit span is less than or equal to 11 bits. The third pattern is uncorrectable since it exceeds the Controller's correction capability, which is 11 bits.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

#### 4.5.16.1 Read Data From Sector Buffer (Class 0, Opcode OE)

This command transfers the 512 bytes of data currently residing in the sector buffer to the host. It is also usually used in 2 ways:

A) Read the contents of the data buffer after writing it using WRITE SECTOR BUFFER command to test the RAM.

B) If an uncorrectable data error occurs, the Controller will not send data to the host, but reports the error immediately. If the host wants the corrupt data, it issues this command to retrieve it.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

### 4.5.16.2 Write Data to Sector Buffer (Class 0, Opcode 0F)

This command writes 512 bytes of data from the IBM CPU into the controller sector buffer. It is usually used in 2 ways:

A) Write a test pattern to the Controller and read it back to verify the Controller's buffer memory is functioning.

B) Before issuing the Format or Format Tracks command, use this command to initialize the sector buffer with a specified data pattern. The format commands use the sector buffer data for the sector data field data pattern. See Format Drive command for details.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

### 4.5.17 RAM Diagnostic (Class 7, Opcode 00)

This command does walking 1 and walking 0 pattern test of its internal RAM buffer.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

### 4.5.18. Reserved (Class 7, Opcode 01)

This opcode is not used.

### 4.5.19 Reserved (Class 7, Opcode 02)

This opcode is not used.

### 4.5.20 Drive Diagnostic (Class 7, Opcode 03)

This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and reads sector 0 of each track to verify that both ID and data field are correct. The controller does not perform any write operations during this command; it is assumed that the disk has been previously formatted.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| Byte 1 | 0 | 0 | d | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

### 4.5.21 Controller Internal Diagnostics (Class 7, Opcode 04)

This command checksums the Controller ROM by adding the value of each memory location modulo 256 across the programmed area. The newly calculated checksum is compared to the checksum stored permanently in the ROM. If the checksums do not compare, then a CHECKSUM ERROR (Error Code 31 Hex) is returned. The ECC circuitry is tested by introducing an artificial error to the data and check that the ECC circuitry detects the error. It also passes a good pattern and sees if the ECC circuitry detects no ECC error.
NOTE: The controller can not access or test the BIOS ROM resident on the controller card.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| Byte 1 | / | / | / | / | / | / | / | / |
| Byte 2 | / | / | / | / | / | / | / | / |
| Byte 3 | / | / | / | / | / | / | / | / |
| Byte 4 | / | / | / | / | / | / | / | / |
| Byte 5 | / | / | / | / | / | / | / | / |

### 4.5.22 Read Long (Class 7, Opcode 05)

This command is used to test the ECC circuitry. When the host issues a write command to the Controller (assume 512 bytes/sector), the Controller writes to the disk the 512 bytes sent by the host and appends the four bytes generated by the ECC hardware. During a normal read command, the Controller reads the 512 data bytes plus the 4 ECC bytes into the buffer. But the Controller sends only the 512 data bytes to the host. The 4 ECC bytes are used to determine if an ECC data error occured. The only difference between READ LONG and READ is the Controller appends the 4 ECC bytes to the data transfer, making the sector transfer 516 bytes long. The method to test the ECC circuitry is as follows:

A) Use the normal READ command to find a sector that does not have any data errors.

B) Use READ LONG to read that sector plus ECC into the host.

C) Modify the data pattern in a known way.

D) Use WRITE LONG to write the pattern to the same sector.

E) Use the READ command to read the same sector again.

F) If the pattern change is less than or equal to 11 bits in length, the controller flags it as a correctable data error. If the change is greater than 11 bits in length, the Controller will flag it as an uncorrectable data error.

G) Use a WRITE command to restore the sector for system use.

d = drive, 0 or 1

r = retries

s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | Block Count | | | | | | | |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

### 4.5.23 Write Long (Class 7, Opcode 06)

When this command is used, the host supplies the 4 bytes of ECC information following the 512 bytes data. This command is used to test the Controllers' ECC circuitry only. For detail description of the test, see the READ LONG command above.

d = drive, 0 or 1
r = retries
s = step option

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| Byte 1 | 0 | 0 | d | Head Number | | | | |
| Byte 2 | CYL Hi | | | Sector Number | | | | |
| Byte 3 | Cylinder Low Number | | | | | | | |
| Byte 4 | Block Count | | | | | | | |
| Byte 5 | r | 0 | 0 | 0 | s | s | s | s |

## 4.6 SECTOR FORMAT

Figure 4-6 shows the format of the sector and the names of the fields of the information traveling over the Controller-drive interface. Table 4-9 lists the fields and a description of each field.

**Table 4-9 Sector Field Description**

| FIELD | BYTES | FIELD DESCRIPTION |
|---|---|---|
| AM | 4 | Address Mark |
| GAP1 | 9 | Zero Byte Gap |
| SYNC1 | 1 | ID Sync Byte |
| GAP2 | 2 | ID Zero Byte Gap |
| COM | 1 | ID Compare Byte |
| CYLH | 1 | Cylinder High (MSB) |
| CYLL | 1 | Cylinder Low (LSB) |
| HEAD | 1 | Head Number |
| SEC | 1 | Sector Number |
| FLAG | 1 | Flag Byte |
| ZER | 1 | Zero Byte |
| ECC1 | 4 | ID ECC Bytes |
| GAP3 | 16 | Zero Byte Gap |
| SYNC2 | 1 | Data Field Sync Byte |
| GAP4 | 2 | Data Field Zero Byte Gap |
| DATA | 512 | Data Field |
| ECC2 | 4 | Data Field Ecc Bytes |
| GAP5 | 43 | Inter-record Zero Gap |

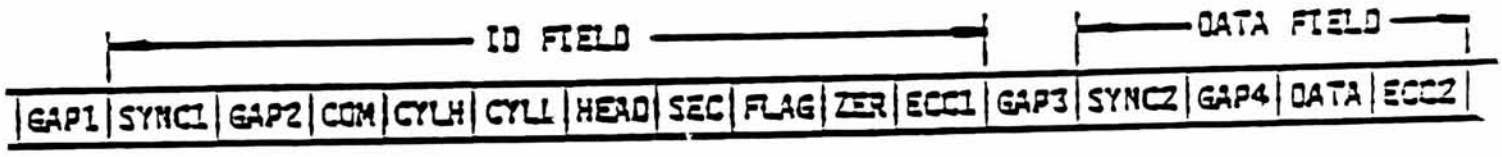



FIGURE 4-6 SECTOR FORMAT

## 4.7 EXECUTION OF DIAGNOSTICS

It is suggested that the diagnostics be envoked by the host in the following order:

1) Controller internal diagnostics (Command code E4). This diagnostic tests all the logical and decision making capability of the controller as well as the program memory checksum and the error detection and correction circuits (ECC). Execution of this diagnostic ensures that the controller can communicate with the host.

   The program memory test is a summation of all program memory bytes, including a checksum bytes. The value of the checksum byte was chosen to yield a total sum equal to an integral multiple of 256. If the test produces a different sum, an error code of 31 hex is entered into status, indicating that one or more program bytes is incorrect.

   The ECC test shifts known data through the ECC circuitry, and checks for the expected results. If an error is detected, the error code 32 hex is entered into status.

2) The Ram Diagnostic (Command code E0) should be executed next. This command verifies that the sector buffer is operational by writing, reading and verifying various data patterns to and from all locations.

   The RAM test is a non-destructive write/read test of all 1024 bytes in the RAM. The first byte in the RAM is saved in a CPU register. A zero is then written to the first RAM location, and read back for verification. The write/verify sequence is then reported, using the following byte values in sequence: 01, 02, 04, 08, 10, 20, 40, 80 (hex). The original RAM bytes is then retrieved from the CPU, and returned to its RAM location. The above test is then repeated for all remaining RAM location. After writing and verifying the whole RAM, the entire sequence above is repeated using the following byte values: FF, FE, FD, FB, F7, EF, DF, BF, 7F (hex).

If a mismatch is error between the bytes written to RAM and read from RAM, an error code 30 hex is entered into status.

3) If the parameters of the connected drives are different than the default parameters (see Section 4.5.15), the new configuration must be sent to the controller using the Initialize Drive Characteristics command (Command code 0C) before the Drive Diagnostic is executed.

4) Before the Drive Diagnostic is executed, the host program should continously issue a Test Drive Ready command to the controller (Command code 00) with the appropriate time-out until the drive becomes ready.

5) Drive Diagnostic (Command code E3). This diagnostic issues a Recalibrate to the disk drive and then steps through all tracks verifying the ECC on the identifier fields of the first sector of each track. If this diagnostic passes, it implies that the disk has been formatted and that the first ID field of each track is good.

## 4.8 ERROR CORRECTION PHILOSOPHY

Since the typical ECC error correction time of the Xebec controller is approximately 50 milliseconds and therefore greater than the time for one revolution of the disk, the sector in error is optionally re-read (if bit 6 is reset in byte 5 of the read command DCB) on the next revolution during a Read command. In most cases, the error will be soft and will not reappear on the re-read. This initial re-read of the failing sector is over and above the retry count passed in the DCB (bit 7, byte 5) which applies only to uncorrectable errors.

The retry count on uncorrectable errors is preset to 4 by the controller each time a sector has been read successfully. On a multiple sector transfer if an uncorrectable error was detected but subsequently found to be correctable on a retry, the retry count is reset to 4 before the next sector is read from the disk.

## 4.9 RETRY PHILOSOPHY

When any error is encounterd, except an ECC error in the data field, the Disk Controller examines Bit 7 of the Control Byte (Byte 5) to determine the retry method to use.

If Bit 7 is set, the Controller will not retry the operation, but reports the error immediately. If Bit 7 is reset, the controller will retry the operation 3 times, then recalibrate the drive, seek back to the current track, and retry once more. For example, if an ADDRESS MARK (AM) NOT FOUND error occurs, the Controller attempts to reread the same sector 3 times. If the error persists, the Controller recalibrates the drive to track 0, seeks to the target track and rereads for the last time. If the error still persists, the Controller aborts the command and reports the error to the host.

If Bit 6 is set, the Controller will not retry a read of a sector that contains a data error before attempting error correction. If Bit 6 is reset, the Controller will reread the sector before attempting error correction. It is faster and more reliable to read the data again than apply error correction

immediately. If the data error is transient in nature, such as noise or electrical interference in the disk heads or read amplifier, noise in cable, or a power supply transient, then another read of the sector will be successful. If the error occurs twice in succession, the error is caused by a media defect, so ECC correction is used to recover the data.

## 4.10 SECTOR INTERLEAVING

The Disk controller will accept any interleave value between zero and the number of sectors per track minus one. The interleave value tells the Controller where the next logical sector is located in relation to the current sector. For example, an interleave value of one specifies that the next logical sector is physically the next sector on the track. An interleave of two specifies that the next logical sector is two sectors ahead of the current sector, so there is one sector between each logical sector. An interleave of three specifies that the next logical sector is three sectors ahead, so there are two sectors between each logical sector. Thus, the number of physical sectors between any two adjacent logical sectors is the interleave value minus one. An interleave of zero will be converted to interleave of 1 automatically. Any out of range interleave value will result in an Invalid Parameter Error.

The interleave value can be set to improve system throughput based on overhead time of the host software, overhead time in tne disk driver, and overhead time for the controller to process a command. If the host system is capable of multisector transfers, system throughput can be optimized by setting the interleave value such that the next logical sector comes under the heads just as the Controller completes the data transfer of the previous sector. If the host is capable of passing a sector of data at DMA speed (one millisecond for a 512 byte sector), then the interleave value sould be set to four to optimize multisector transfers. This is the minimum value for continuous sector transfers. If a sector data transfer takes between one and two milliseconds, set the interleave value to five. The best method is to experimentally determine the best interleave value for your system using a representative benchmark.

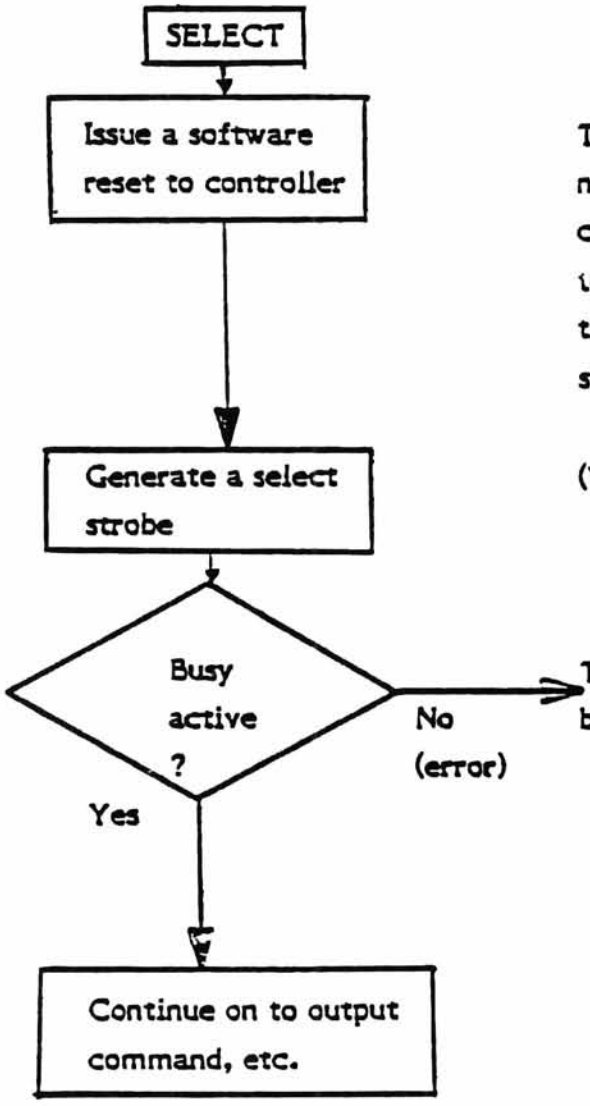
## XEBEC-IBM CONTROLLER PROGRAMMING EXAMPLES

The IBM integrated controller commands fall into three categories:

1 Non-data transfer commands
2 Data transfer commands
3 Status commands

Before a command is sent, the controller has to be selected.

## CONTROLLER SELECTION




This should only be necessary the first time the controller is selected (write to Port 1). It insures that the controller is in a known state.

(Write to Port 2)

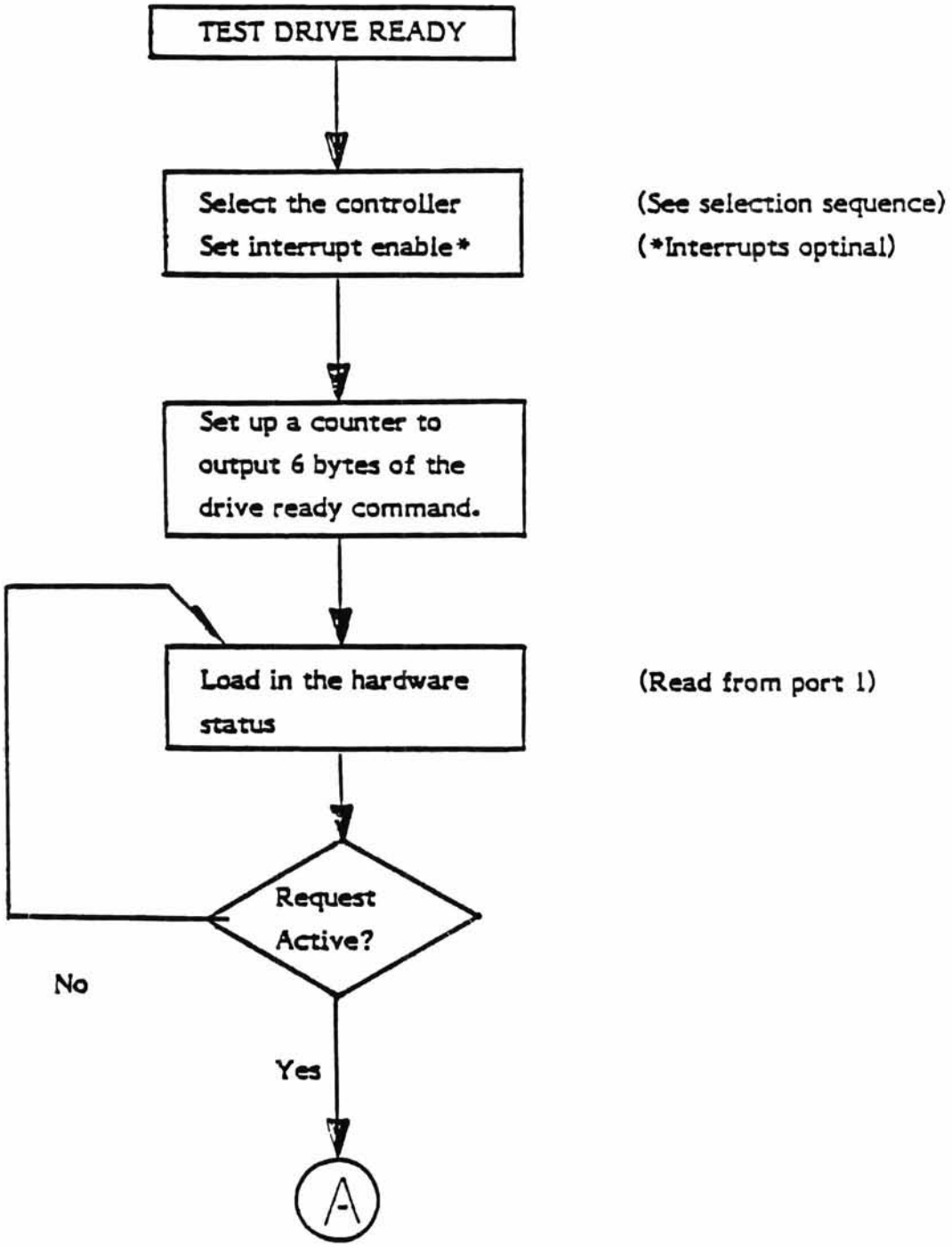
This controller should go busy right away.

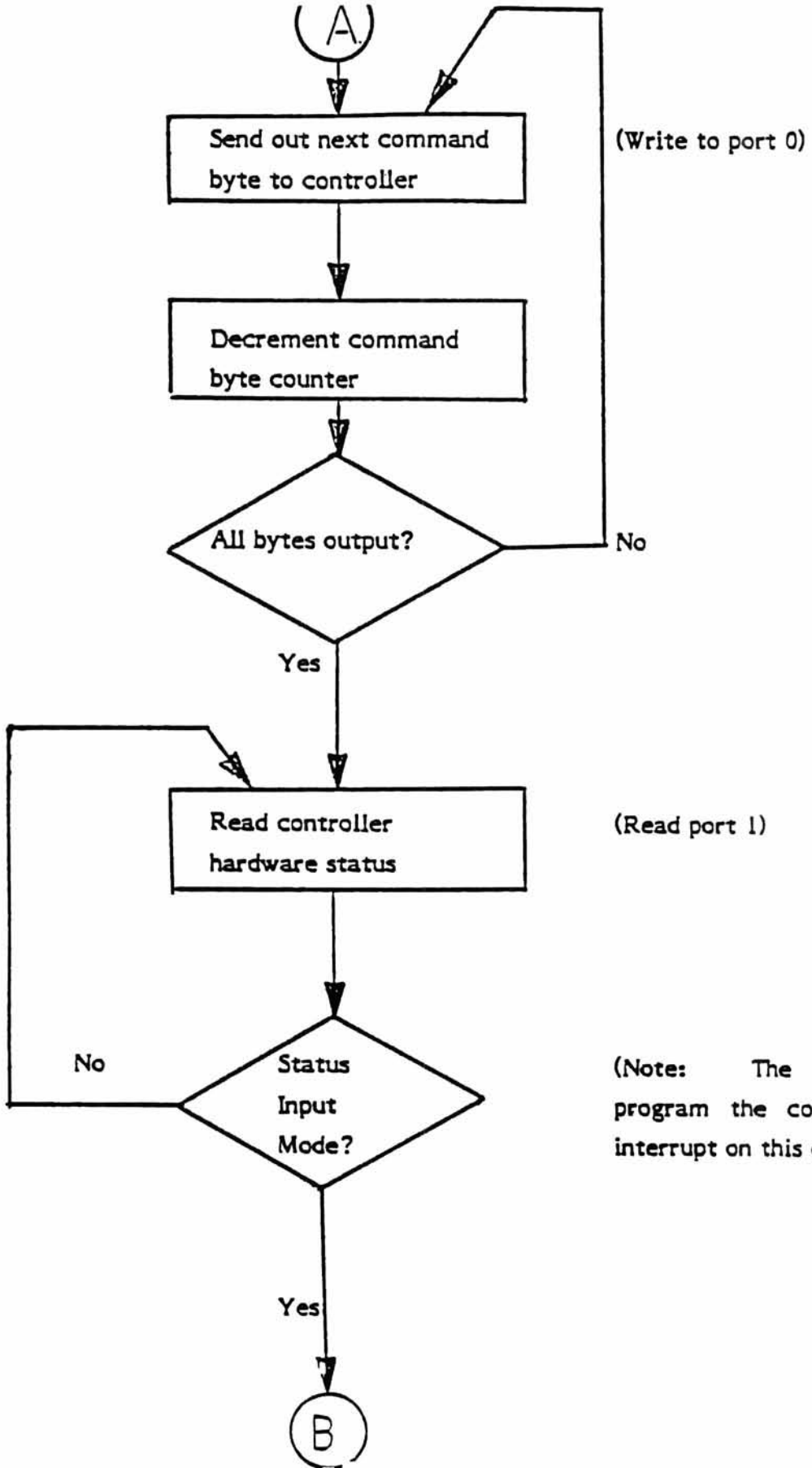
## NON DATA TRANSFER COMMANDS

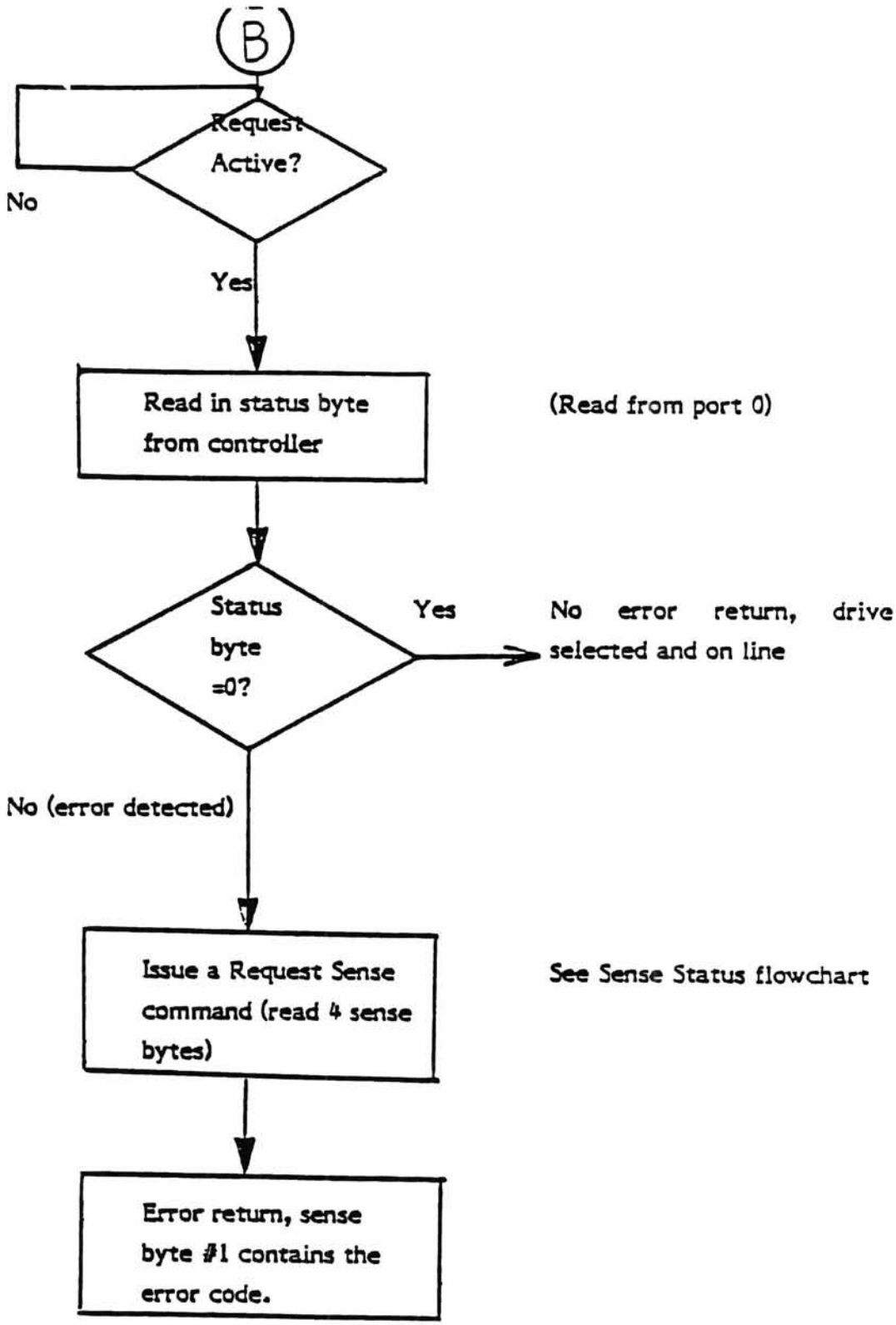
The test for Drive Ready command is shown here as an example of a non-data transfer command. Some of the other commands which fall into this category are:

1. Recalibrate
2. Format Disk Drive
3. Read Verify Command
4. Seek
5. Execution of various self tests

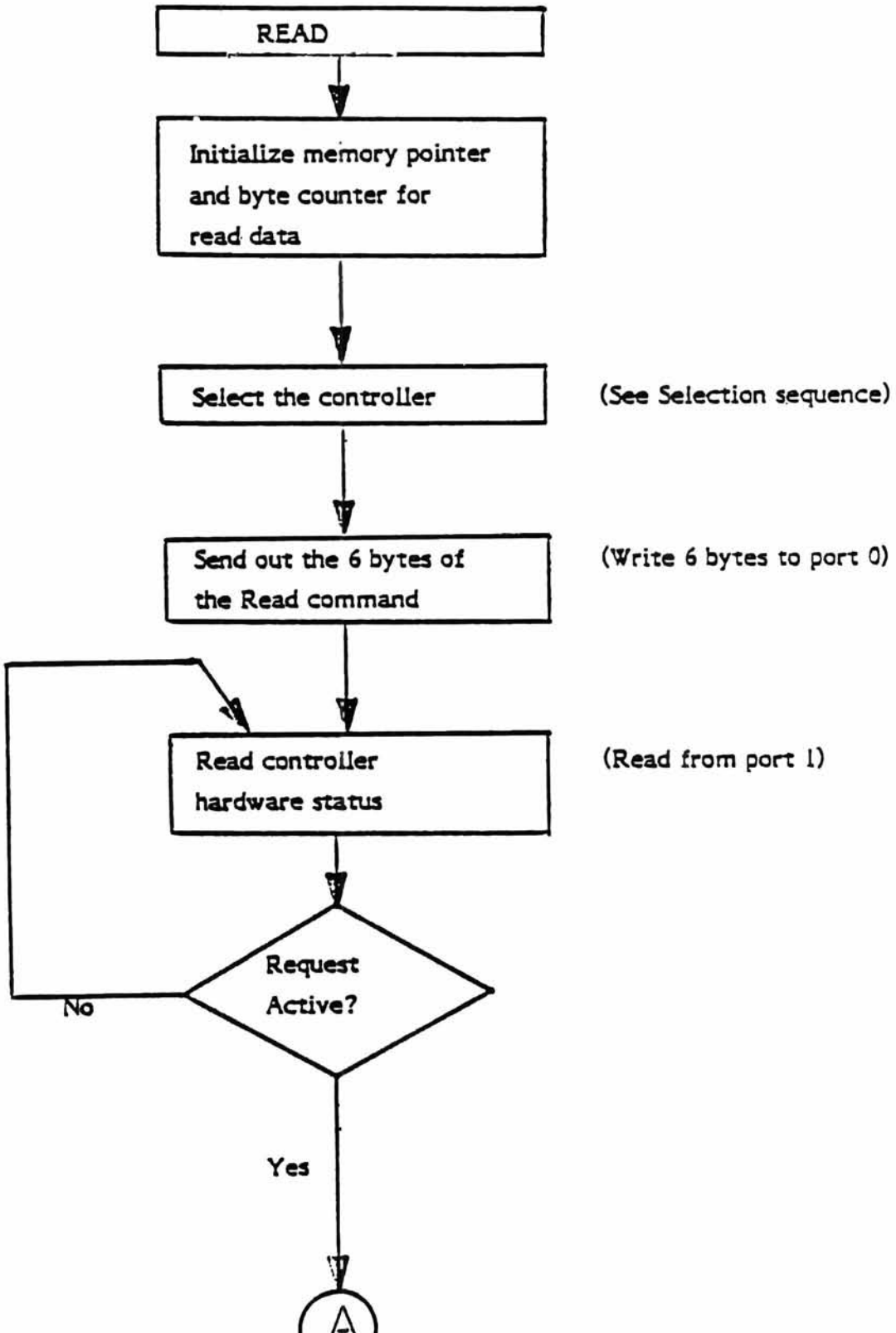
This command selects a specified disk drive and verifies that it is ready. This particular command should be issued initially to make sure all drives to be accessed during system operation are ready.

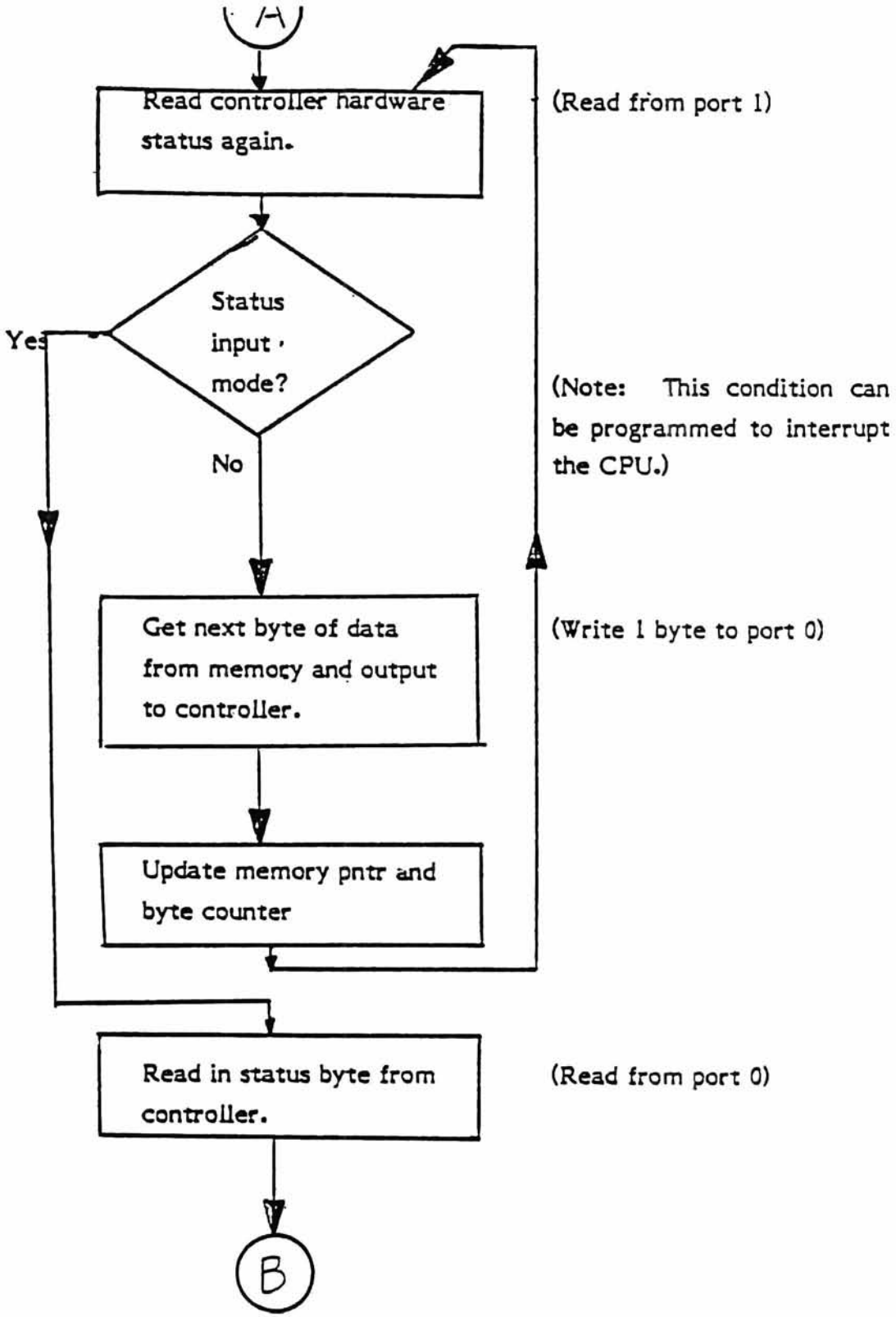



A
Send out next command byte to controller
(Write to port 0)
Decrement command byte counter
All bytes output?
No
Yes
Read controller hardware status
(Read port 1)
No
Status Input Mode?
(Note: The CPU can program the controller to interrupt on this condition.)
Yes
B

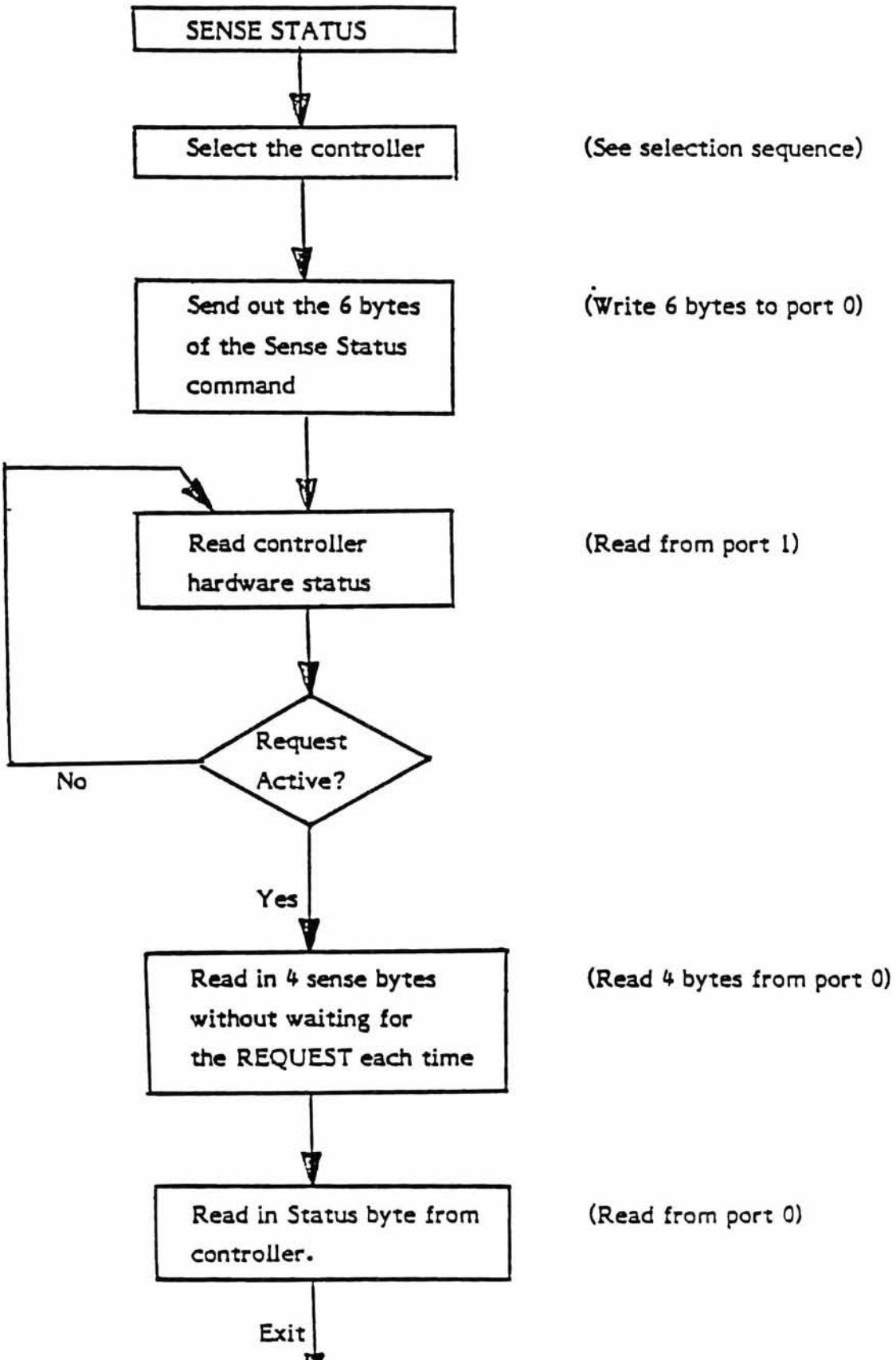

B
Request Active?
No
Yes
Read in status byte from controller
(Read from port 0)
Status byte =0?
Yes
No error return, drive selected and on line
No (error detected)
Issue a Request Sense command (read 4 sense bytes)
See Sense Status flowchart
Error return, sense byte #1 contains the error code.

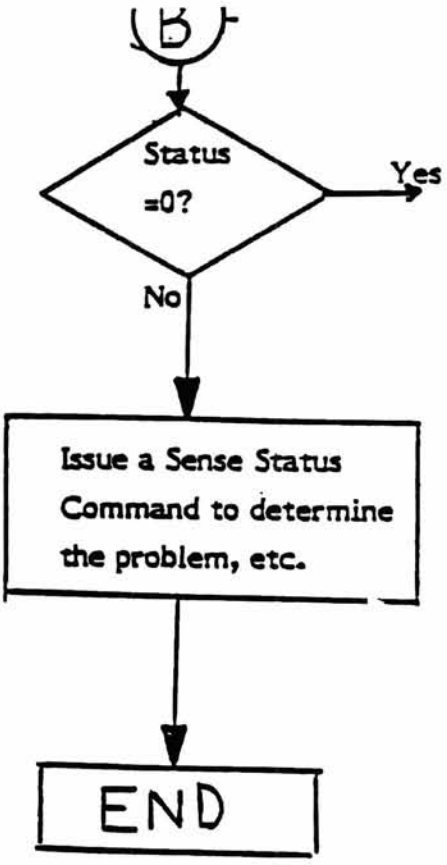
## READ USING NON-INTERRUPT PROGRAMMED I/O (NON-DMA)




A
Read controller hardware status again.
(Read from port 1)
Status input mode?
Yes
No
(Note: This condition can be programmed to interrupt the CPU.)
Get next byte of data from memory and output to controller.
(Write 1 byte to port 0)
Update memory pntr and byte counter
Read in status byte from controller.
(Read from port 0)
B

## SENSE STATUS COMMAND






Transfer completed ok

Chapter 4

# Parts List

## Introduction

This chapter includes a view of the Winchester drive option to assist in the identification of replacement parts. Adjacent to the item number are the part number and description, which must be supplied when ordering the replacement part.

## Winchester Drive Option Parts List

Refer to Figure 4.1 for identification of replacement parts.

| ITEM NUMBER | PART NUMBER | DESCRIPTION |
|---|---|---|
| 5 | HE 150-156 | Winchester, MiniScribe |
| | or | |
| | HE 150-164 | Winchester, CMI |
| | or | |
| | HE 150-167 | Winchester, Seagate |
| 10 | HE 250-1325 | Screw, 6-32 × .375 |
| 15 | HE 203-2203 | Vented cover |
| 20 | HE 150-190 | Xebec Winchester controller card |
| 25 | HE 444-365 | ROM |
| 30 | HE 134-1380 | Cable assembly |
| 35 | HE 134-1381 | Cable assembly |
| 40 | HE 267-25 | Cable strap |
| 45 | HE 252-756 | Nut, hex lock |
| 50 | HE 260-708-81 | LED clip |
| 55 | HE 260-708-82 | LED grommet |

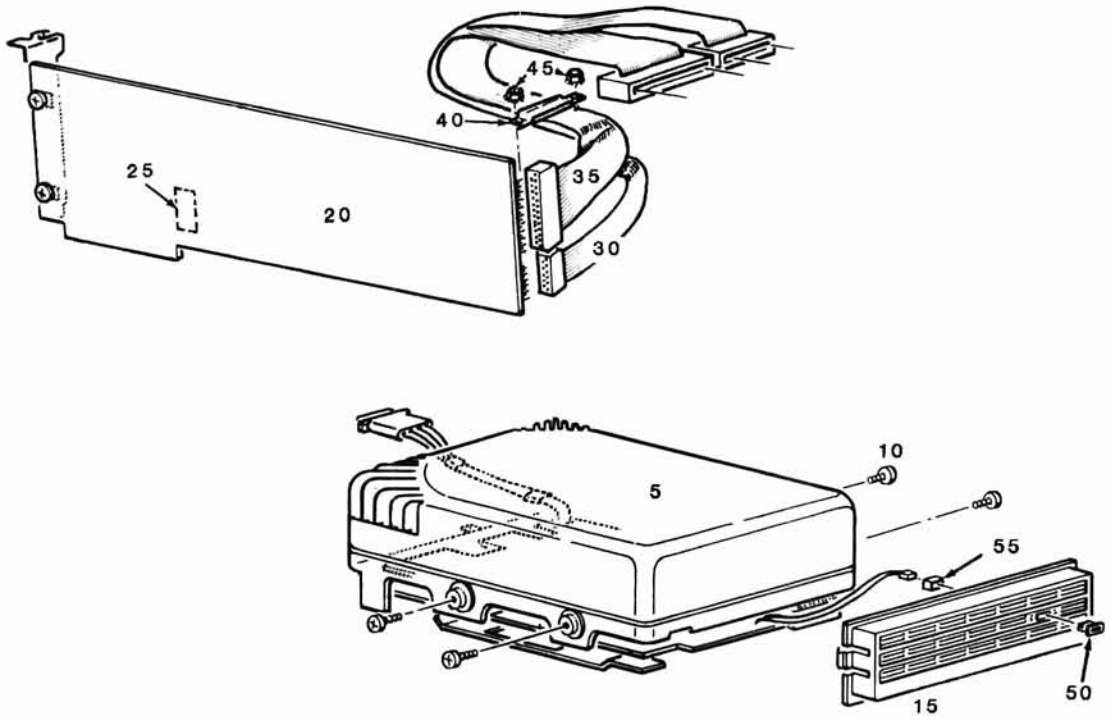



**Figure 4.1. Winchester Option View**

adaptec, inc.

Febuary 3, 1987 CS

WINCHESTER DRIVE PARAMETERS FOR USE WITH THE FOLLOWING ADAPTEC CONTROLLERS
ACB 2010A, ACB2070, ACB2071, ACB2072, ACB4000A, ACB4070

Please contact your prefered drive manufacturer for more drive information and for exact revision of drive. Adaptec will not accept returned material of the RLL products if running on drives and revisions not on this list and APPROVED by the drive manufacturer.

| MANUFACTURER | | MODEL | UNFMT CAP | FMT CAP | 2,7 RLL | HDS | CYL | STEP | AVG SEEK |
|---|---|---|---|---|---|---|---|---|---|
| ALPS | 3.5" | DRN010A | 12.7 | 10.0 | NR | 2 | 615 | | 85ms |
| | 3.5" | DRN020A | 25.5 | 20.0 | NR | 4 | 615 | | 85ms |
| | 3.5" | DRM010A | 12.5 | 10.0 | NR | 2 | 615 | | 80ms |
| | 3.5" | DRM020A | 25.5 | 20.0 | NR | 4 | 615 | | 80ms |
| ATASI | | 3020 | 20.2 | 16.8 | NR | 3 | 645 | 2.5-500us | |
| | | 3033 | 33.6 | 28.1 | NR | 5 | 645 | 2.5-500us | |
| | | 3046 | 47.0 | 39.3 | NR | 7 | 645 | 2.5-500us | |
| | | 3051 | 51.0 | 42.9 | NR | 7 | 704 | 2.5-500us | |
| | | 3075 | 85.0 | 67.1 | NR | 8 | 1024 | 2.5-500us | |
| | | 3085 | 85.0 | 67.1 | NR | 8 | 1024 | 2.5-500us | |
| BASF | | 6185 | 27.5 | 23.0 | NR | 6 | 440 | 10-200us | |
| | | 6186 | 18.3 | 15.3 | NR | 4 | 440 | 10-200us | |
| | | 6187 | 9.2 | 7.7 | NR | 2 | 440 | 10-200us | |
| BULL | | D530 | 30.0 | 25.0 | *38.0 | 3 | 987 | | |
| | | D550 | 51.0 | 42.9 | *63.2 | 5 | 987 | | |
| | | D570 | 70.0 | 59.0 | *88.4 | 7 | 987 | | |
| | | D585 | 85.0 | 67.1 | *104.5 | 7 | 1166 | | |
| CDC | | 9415-5 | 36.3 | 30.3 | NR | 5 | 697 | 8-200us | |
| | | 9415-5 | 21.8 | 18.2 | NR | 3 | 697 | 8-200us | |
| CMI | | 3212 | | | NR | 2 | | | |
| | | 3426 | 25.5 | 21.3 | NR | 4 | 612 | | |
| | | 5206 | 6.4 | 5.3 | NR | 2 | 306 | 5us | |
| | | 5412 | 12.7 | 10.7 | NR | 4 | 306 | 5us | |
| | | 5616 | 16.0 | 13.4 | NR | 6 | 256 | | |
| | | 5619 | 19.1 | 16.0 | NR | 6 | 306 | 5us | |
| | | 6213 | 13.3 | 11.1 | NR | 2 | 640 | )0.5us | |
| | | 6426 | 26.7 | 22.3 | NR | 4 | 640 | )0.5us | |
| | | 6640 | 40.0 | 33.4 | NR | 6 | 640 | )0.5us | |
| | | 7660 | 60.0 | 50.1 | NR | 6 | 960 | | |
| | | 7880 | 80.0 | 66.8 | NR | 8 | 960 | | |
| COGITO | | CG906 | 6.4 | 5.3 | NR | 2 | 306 | 5-200us | 85ms |
| | | CG912 | 12.7 | 10.7 | NR | 4 | 306 | 5-200us | 85ms |
| | | PT912 | 12.7 | 10.7 | NR | 2 | 512 | | 85ms |
| | | PT925 | 25.5 | 21.3 | NR | 4 | 612 | | 85ms |

NR - Not Recommended
* - Approximate 2,7 RLL format capacity

2344 SMD
2333 SMD

| MANUFACTURER | | MODEL | UNFMT CAP | FMT CAP | 2,7 RLL | HDS | CYL | STEP | AVG SEEK |
|---|---|---|---|---|---|---|---|---|---|
| DISCTRON (RMS) | | 503 | 3.2 | 2.7 | NR | 2 | 153 | 6-200us | |
| | | 504 | 4.5 | 3.7 | NR | 2 | 215 | 6-200us | |
| | | 506 | 6.4 | 5.3 | NR | 4 | 153 | 6-200us | |
| | | 507 | 6.4 | 5.3 | NR | 2 | 306 | 6-200us | |
| | | 509 | 9.0 | 7.5 | NR | 4 | 215 | 6-200us | |
| | | 512 | 12.7 | 10.7 | NR | 8 | 153 | 6-200us | |
| | | 513 | 13.4 | 11.2 | NR | 6 | 215 | 6-200us | |
| | | 514 | 12.7 | 10.7 | NR | 4 | 306 | 6-200us | |
| | | 518 | 17.9 | 15.0 | NR | 8 | 215 | 6-200us | |
| | | 519 | 19.1 | 16.0 | NR | 6 | 306 | 6-200us | |
| | | 526 | 25.5 | 21.3 | NR | 8 | 306 | 6-200us | |
| FUJI | | FK-305-54R | 32 | 27 | 45 RLL | | | 3.5" | |
| | | FK 305-55ER | 48 | 40 | 60 RLL | | | 3.5" | |
| FUJITSU | | M220 | 6.7 | 5.6 | NR | 2 | 306 | | |
| | 3.5" | M2223A | 12.7 | 10 | NR | 4 | 306 | | 85ms |
| | 3.5" | M2224A | 19.1 | 15.0 | NR | 6 | 306 | | 85ms |
| | | M2230AT | 6.7 | 5.6 | NR | 2 | 320 | .3us-.3ms | |
| | | M2233/AT | 13.3 | 10.5 | NR | 4 | 320 | .3us-.3msw | 95ms |
| | | M2234 | 20.0 | 15.7 | NR | 6 | 320 | .33us | 83ms |
| | | M2235 | 26.7 | 21.0 | NR | 8 | 320 | .33us | 83ms |
| | | M2241AS | 31.4 | 26.3 | NR | 4 | 754 | .33-200us | |
| | | M2242 | 59.9 | 43.2 | NR | 7 | 754 | .33-200us | 33ms |
| | | M2244 | 86.3 | 67.8 | NR | 11 | 754 | .33-200us | 33ms |
| | | 2227 | | 90 | 60 | | | | |
| HITACHI | | DK511-3 | 30.0 | | NR | | | | |
| | | DK511-5 | 50.0 | | NR | | | | |
| | | DK511-8 | 80.0 | | NR | | | | |
| IMI | | 2306H | 6.4 | 5.3 | NR | 2 | 306 | 3-200us | 85ms |
| | | 2312H | 12.7 | 10.7 | NR | 4 | 306 | 3-200us | 85ms |
| | | 5006H | 6.4 | 5.3 | NR | 2 | 306 | | 68ms |
| | | 5012H | 12.7 | 10.7 | NR | 4 | 306 | | 68ms |
| | | 5018H | 19.1 | 16.0 | NR | 6 | 306 | | 68ms |
| LAPINE | 3.5" | TITAN LT300 | 25.0 | NR | *31.5 | 4 | 616 | | 65ms |
| | 3.5" | TITAN LT200 | 25.0 | 20.0 | NR | 4 | 616 | | 65ms |
| MAXTOR | | 1065 | 66.9 | 55.3 | NR | 7 | 918 | 13us | |
| | | XT1085 | 85.3 | 67.1 | NR | 8 | 1024 | | 28ms |
| | | XT1105 | 105.2 | 82.7 | NR | 11 | 918 | 13us | 27ms |
| | | XT1140 | 143.5 | 112.8 | NR | 15 | 918 | 13us | 27ms |
| | | XT2085 | 89.2 | 70.2 | NR | 7 | 1224 | | 30ms |
| | | XT2140 | 140.2 | 110.3 | NR | 11 | 1224 | | 30ms |
| | | XT2190 | 191.2 | 150.4 | NR | 15 | 1224 | | 30ms |
| MICROPOLIS | | 1302 | 25.9 | 20.4 | NR | 3 | 830 | 2-200us | |
| | | 1303 | 43.2 | 34.0 | NR | 5 | 830 | 2-200us | |
| | | 1304 | 51.9 | 40.8 | NR | 6 | 830 | 2-200us | |
| | | 1323 | 42.7 | 33.6 | NR | 4 | 1024 | | 28ms |

NR - Not Recommended
* - Approximate 2,7 RLL format capacity

| ER | MODEL | UNFMT CAP | FMT CAP | 2,7 RLL | HDS | CYL | STEP | AVG SEEK |
|---|---|---|---|---|---|---|---|---|
| MICROPOLIS | | | | | | | | |
| S | 1323A | 53.3 | 41.9 | NR | 5 | 1024 | | 28ms |
| | 1324 | 64.0 | 50.0 | NR | 6 | 1024 | | 28ms |
| | 1324A | 74.7 | 58.7 | NR | 7 | 1024 | | 28ms |
| | 1325 | 85.0 | 67.1 | NR | 8 | 1024 | | 28ms |
| MICROSCIENCE | | | | | | | | |
| NCE 3.5" | HH315 | 12.7 | 10.7 | NR | 4 | 306 | | |
| 3.5" | HH325 | 25.5 | 21.3 | NR | 4 | 612 | | |
| 3.5" | HH330 | 25.5 | 21.3 | *31.0 | 4 | 612 | | |
| | HH612 | 12.7 | 10.7 | NR | 4 | 306 | 10-200us | 100ms |
| | HH625 | 25.5 | 21.3 | NR | 4 | 612 | 10-200us | |
| | HH725 | 25.5 | 21.3 | NR | 4 | 612 | | |
| | HH738 | 25.5 | 21.3 | *31.0 | | | | |
| | HH1050 | 55.4 | 44.0 | *66.0 | 5 | 1024 | | |
| AGE | MS212R | 12.7 | 10.7 | *15.6 | 4 | 306 | | 95ms |
| MINISCRIBE | | | | | | | | |
| | 2006 | 6.4 | 5.3 | NR | 2 | 306 | 6-200us | 85ms |
| | 2012 | 12.7 | 10.7 | NR | 4 | 306 | 6-200us | 85ms |
| JH | 3006 | 6.4 | 5.3 | NR | 2 | 306 | 6-200us | 85ms |
| | 3012 | 12.7 | 10.7 | NR | 2 | 612 | 6-200us | 155ms |
| | 3212 | 12.7 | 10.7 | NR | 2 | 612 | 2-200us | |
| | 3412 | 12.7 | 10.7 | NR | 4 | 306 | 2-200us | |
| | 3425 | 25.5 | 21.3 | NR | 4 | 612 | 2-500us | |
| | 3438 | 38.4 | NR | *31.0 | 4 | 612 | 2-500us | |
| | 4010 | 10.0 | 8.4 | NR | 2 | 480 | 6-200us | |
| | 4020 | 20.0 | 16.7 | NR | 4 | 480 | 6-200us | |
| | 5330 | 30.0 | 52.1 | NR | 6 | 480 | | 85ms |
| | 5338 | 38.2 | 32.0 | NR | 6 | 612 | | 95ms |
| | 5440 | 40.0 | 33.4 | NR | 8 | 480 | | 85ms |
| | 5451 | 51.0 | 42.6 | NR | 8 | 612 | | 95ms |
| | 6032 | 32.0 | 26.7 | NR | 3 | 1024 | 2-200us | |
| | 6053 | 53.3 | 44.6 | NR | 5 | 1024 | 2-200us | |
| | 6074 | 74.7 | 62.4 | NR | 7 | 1024 | 2-200us | |
| | 6128 | 128.0 | NR | ~~*31.0~~ I/O | | | | |
| 3.5" | 8438 | 38.4 | 21.3 | *31.0 | 4 | 612 | | |
| NEC - | | | | | | | | |
| 3.5" | 3126 | 25.0 | 20.0 | NR | 4 | 615 | | 85ms |
| 3.5" | D3127 | 38.4 | NR | *31.0 | 4 | 615 | | 85ms |
| | D5124 | 12.9 | 10.0 | *15.6 | 4 | 309 | | 85ms |
| | D5126 | 25.5 | 20.4 | *31.0 | 4 | 615 | | 85ms |
| | D5127 | 38.4 | NR | *31.0 | 4 | 615 | | 85ms |
| | D5126H | 25.5 | 20.4 | NR | 4 | 615 | | 40ms |
| | D5127H | 38.4 | NR | *31.0 | 4 | 615 | | 40ms |
| | D5146 | 51.24 | 40.3 | NR | 8 | 615 | | 85ms |
| → | D5146H | 51.24 | 40.3 | NR | 8 | 615 | | 40ms |
| | D4127H | 76.87 | NR | *65.0 | 8 | 615 | | 40ms |
| | 5224 | | | NR | | | | |
| | 5244 | | | NR | | | | |

| MANUFACTURER | MODEL | UNFMT CAP | FMT CAP | 2,7 RLL | HDS | CYL | STEP | AVG SEEK |
|---|---|---|---|---|---|---|---|---|
| SEAGATE | ST506 | 6.4 | 5.3 | NR | 8 | 153 | 5-500us | |
| | ST4026 | 25.6 | 21.4 | NR | 4 | 615 | 25-50us | 40ms |
| | ST4038 | 38.1 | 31.9 | NR | 5 | 733 | 10-70us | 40ms |
| | ST4051 | 50.8 | 42.5 | NR | 5 | 977 | 10-70us | 40ms |
| | ST4077R | 80.0 | NR | *68.2 | 5 | 1024 | | 28ms |
| | ST4096 | 96.0 | 80.2 | NR | 9 | 1024 | 3-70us | 40ms |
| | ST4144R | 144.0 | NR | *122.7 | 9 | 1024 | | 28ms |
| SHUGART | SA604 | 6.7 | 5.6 | NR | 4 | 160 | 5-200us | |
| | SA606 | 10.0 | 8.4 | NR | 6 | 160 | 5-200us | |
| | SA607 | 6.5 | 5.4 | NR | 2 | 311 | | |
| | SA612 | 13.0 | 10.8 | NR | 4 | 311 | | |
| | SA706 | 6.4 | 5.3 | NR | 2 | 306 | 5-200us | |
| | SA712 | 12.7 | 10.7 | NR | 4 | 306 | 5-200us | |
| SYQUEST | SQ306R | 6.4 | 5.3 | NR | 2 | 306 | 10-200us | 85ms |
| | SQ312R | 12.7 | 10.7 | NR | 2 | 612 | 10-200us | |
| | SQ319R | 12.7 | 10.7 | *15.5 | 2 | 612 | | |
| | SQ325 | 25.0 | 20.0 | NR | 4 | 612 | | |
| | SQ338 | 38.0 | 30.0 | NR | 6 | 612 | | |
| TANDON 3.5" | TM252 | 12.7 | 10.7 | NR | 4 | 306 | | |
| 3.5" | TM262 | 25.0 | 21.0 | NR | 4 | 615 | | 80ms |
| 3.5" | TM263 | 38.0 | NR | *31.0 | 4 | 615 | | 80ms |
| | TM501 | 6.4 | 5.3 | NR | 2 | 306 | 5-200us | |
| | TM502 | 12.7 | 10.7 | *15.6 | 4 | 306 | 5-200us | |
| | TM503 | 19.1 | 16.0 | NR | 6 | 306 | 5-200us | |
| | T0703 | 36.3 | 30.3 | NR | 5 | 695 | | |
| | TM755 | 51.4 | 43.0 | *62.0 | 5 | 980 | | 35ms |
| TOSHIBA | MK56FA | 80.0 | 67.0 | *105.0 | | | | |
| TULIN | TL213 | 13.3 | 11.1 | NR | 2 | 640 | 5-200us | |
| | TL226 | 26.7 | 22.3 | NR | 4 | 640 | 5-200us | |
| | TL240 | 40.0 | 33.4 | NR | 6 | 640 | 5-200us | |
| | TL238 | 38.0 | 32.0 | *48.0 | 4 | 640 | | |
| | TL258 | 58.0 | 48.0 | *72.0 | 6 | 640 | | |
| | TL338 | 38.0 | 32.0 | *48.0 | 4 | 640 | | |
| | TL358 | 58.0 | 48.0 | *72.0 | 6 | 640 | | |
| VERTEX (PRIAM) | V130 | 30.8 | 25.8 | NR | 3 | 9876 | 5-200us | |
| | V150 | 51.4 | 43.0 | *62.0 | 5 | 987 | 5-200us | |
| | V170 | 72.0 | 60.1 | *90.3 | 7 | 987 | 5-200us | |
| | V185 | 85.0 | 67.1 | *100.6 | 7 | 1166 | | |

* Approximate 2,7 RLL formatted capacity.
NR - Not Recommended

Drive capacities that format to greater than 64Mbytes and require a partitioning I/O driver to get the full capacity when used with IBM DOS or MS DOS. This driver is available from Ontrack Computer Systems (612) 941-4504 or Chase Technologies at (201) 894-5544.

adaptec, inc.

3/1/87 CS

# ESDI
# WINCHESTER DRIVE PARAMETERS
# FOR USE WITH THE ACB-4520A

| MANUFACTURER | MODEL | UNFMT CAP | FMT CAP | HDS | CYL | HARD/SOFT SECTORED |
|---|---|---|---|---|---|---|
| CDC Wren III | 94166-101 | 101.0 | 95.0 | 5 | 969 | HARD/SOFT |
| Wren III | 94166-141 | 141.0 | 120.0 | 7 | 969 | HARD/SOFT |
| Wren III | 94166-182 | 182.0 | 150.0 | 9 | 969 | HARD/SOFT |
| FUJITSU | M2244E | 85.8 | 67.4 | 5 | 823 | |
| | M2245E | 120.2 | 94.4 | 7 | 823 | |
| | M2246E | 171.0 | 134.8 | 10 | 823 | |
| HITACHI | DK512-8 | 86.1 | 67.4 | 5 | 823 | HARD/SOFT |
| | DK512-12 | 120.6 | 94.4 | 7 | 823 | HARD/SOFT |
| | DK512-17 | 172.3 | 134.8 | 10 | 823 | HARD |
| MAXTOR | EXT-4175 | 178.3 | 149.1 | 7 | 1224 | SOFT |
| | EXT-4280 | 280.2 | 234.4 | 11 | 1224 | SOFT |
| | EXT-4380 | 382.0 | 319.6 | 15 | 1224 | SOFT |
| (15Mbits/sec) | EXT-8380E | 408.0 | 320.8 | 8 | 1632 | HARD/SOFT |
| (15Mbits/sec) | EXT-8760E | 765.0 | 601.6 | 15 | 1632 | HARD/SOFT |
| MICROPOLIS | 1353 | 85.3 | 73.4 | 4 | 1024 | HARD/SOFT |
| | 1353A | 106.7 | 91.8 | 5 | 1024 | HARD/SOFT |
| | 1354 | 128.0 | 110.1 | 6 | 1024 | HARD/SOFT |
| | 1354A | 149.3 | 128.5 | 7 | 1024 | HARD/SOFT |
| | 1355 | 170.6 | 146.8 | 8 | 1024 | HARD/SOFT |
| | 1554 | 280.0 | 261.0 | 11 | 1024 | HARD/SOFT |
| | 1555 | 305.0 | 285.0 | 12 | 1024 | HARD/SOFT |
| | 1556 | 331.0 | 309.0 | 13 | 1024 | HARD/SOFT |
| | 1557 | 356.0 | 333.0 | 15 | 1024 | HARD/SOFT |
| | 1558 | 382.0 | 357.0 | 16 | 1024 | HARD/SOFT |
| MINISCRIBE | 6085E | 85.3 | 71.3 | 8 | 1024 | |
| | 6170E | | | | | 16ms $185 |
| | 4180 | 380 | 338 | | | |
| MITSUBISHI | MR5310 | 100.0 | 92.0 | | | (1/2 height) |
| NEC | D5652 | 172.76 | 134.84 | 10 | 832 | HARD |
| NEWBURY DATA | 4000 | 382.0 | 319.6 | 15 | 1224 | HARD |
| PRIAM | 617 | 178.4 | 166.6 | 7 | 1224 | HARD |
| | 628 | 280.4 | 261.9 | 11 | 1224 | HARD |
| | 638 | 382.4 | 357.2 | 15 | 1224 | HARD |
| SIEMENS Mega File | 1300 | | 306.0 | | | HARD |
| TOSHIBA | MK153F | 86.5 | 72.2 | 5 | 830 | HARD/SOFT |
| | MK154F | 121.0 | 101.6 | 7 | 830 | HARD/SOFT |
| | MK156F | 173.0 | 144.5 | 10 | 830 | HARD/SOFT |