FDC 880H HARDWARE MANUAL

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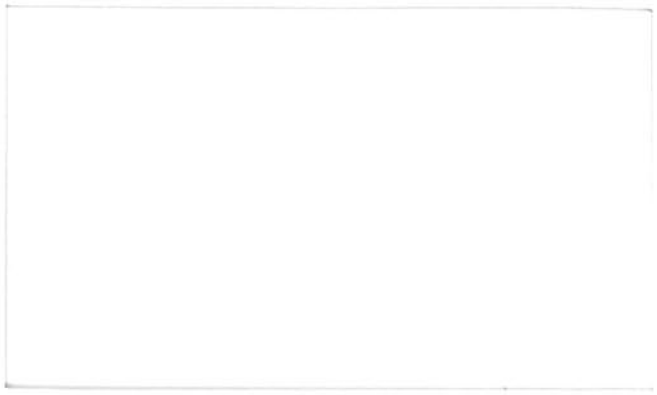

C.D.R. Systems
INCORPORATED

7210 Clairemont Mesa Blvd. • San Diego, California 92111 • Telephone: (714) 560-1272

FDC 880H HARDWARE MANUAL

LIMITED WARRANTY

This unit is warranted for a period of 1 year from the date of purchase to be free from material or workmanship defects. Should the product fail to perform satisfactorily return it prepaid to **C. D. R. Systems Inc.** and it will, at our option, be repaired or replaced free of charge, provided the unit is received during the warranty period. This warranty is invalid if product has been misused or modified. Warranty is limited to replacement of defective parts and no responsibility is assumed for damage to other equipment.

This warranty is made in lieu of all other warranties expressed or implied.

OPERATIONS MANUAL

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January 1981

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SECTION I
INTRODUCTION

1.1 GENERAL

FDC 880H-1 is a single board floppy disc controller containing the Western Digital FD1797 floppy controller chip, H88 or H89 I/O decoding circuits, a phase lock loop for read data synchronization, floppy drive buffering, head load timing and a floppy drive interconnect cable.

The FDC 880H-1 supports a mix of four drives, single density 8" or 5-¼", double density 8" or 5-¼" or double sided versions of 8" or 5-¼" drives.

1.2 FUNCTIONAL DESCRIPTION

Figure 1-1 is a block diagram describing the functional blocks comprising the FDC 880H-1. The following sections describe each of the blocks in Figure 1-1.

1.3 CONTROL LATCH

The Control Latch (Z7) receives input from the H88/H89 data bus when addressed by the address decoder at D3H and latches the data. The data latched is comprised of drive select information, 8" or 5-¼" drive in use, single or double density in use, and interrupt enable/disable.

1.4 STATUS BUFFER

The Status Buffer (Z14), when read at address D3H will contain information on drive selected, interrupt status, side selected (for double-sided drives), size of drive (8" or 5-¼") and interrupt requests from the floppy controller chip.

1.5 WRITE PULSE TIMER

The Write Pulse Timer is a monostable that synchronizes the write pulse received from the H88/H89 with the address and data received from the H88/H89, for proper timing with the floppy controller chip.

1.6 READ PULSE TIMER

The Read Pulse Timer is a monostable that synchronizes the data received from the floppy controller chip and the read pulse from the H88/H89

The Read Pulse Timer also controls the data buffer latch function to allow the floppy controller chip to operate at full speed.

1.7 DATA BUFFER

The data Buffer (Z18) is used to latch read data received from the floppy controller until the H88/H89 is ready to operate on the data.

Read and write data from the floppy controller are obtained by using interrupts with data synchronized by wait states after the interrupt has caused entry into the read or write program.

1.8 ADDRESS DECODER

The address Decoder is used to synchronize read and write pulses from the H88/H89 to the requirement of the WD1797 floppy controller chip Data Request line and Interrupt Request line. This chip also controls adddress decoding for the control latch, status buffer, and FD1797 (U16).

1.9 WAIT LATCH

This block is driven by the address decoder and provides a latch for interrupts and for wait states. The wait states for the H88/H89 are used as FD1797 to H88/H89 synchronization for either Read or Write Data Requests from the FD1797.

1.10 DRIVE SELECT BUFFERS

The Drive Select Buffers are open collector drivers used to couple signals from the control latch to the floppy drive.

1.11 CONTROL BUFFER

The Control Buffer is an open collector driver used to couple signals from th FD1797 to the floppy drive. An additional buffer (Z3) is used as a terminated line receiver to couple, and properly terminate through R6, signals from the floppy drive to the FD1797.

1.12 HEAD LOAD TIMING

This block is a monostable used to delay the head load command from the FD1797 to the floppy drive. The time constant of this signal is changed for minifloppy drives by a control line (5-¼ select)and is also used to provide a "Ready" signal to the FD1797 when minifloppies are in use. Minifloppies do not have a "Ready" signal.

1.13 READ WRITE CONTROL DECODER

This block is comprised of Z15 and Z9. Z15 receives input from the FD1797 and in conjunction with Z9, produces the write compensation required in double density drives. Write precompensation is provided by examining the outputs "Early" and "Late" from the FD1797 and selecting the proper input to the shift register Z9. Precompensation is provided in 250 nanosecond increments. Late pulses are written 250 nanoseconds late, while Early pulses are written 250 nanoseconds early from the optimum position. The decoder only applies this precompensation in double density when the track in use on the disk is between tracks 43 and track 77. No precompensation is provided or required for single density drives and the decoder input DDEN deselects precompensation when DDEN is at a logic high. 5¼" drives are always precompensated in double density.

1.14 OSCILLATOR

The FD1797 requires a 2 mHz clock for 8" drives and a 1 mHz clock for minifloppy drives. Z6 provides a basic 4 mHz crystal (Y1) controlled clock. This signal is divided by Z10 and sent to the Read/Write control decoder which then selects the proper clock rate for the FD1797. The oscillator occupies only one-half of Z6. The other half of Z6 is a variable frequency oscillator for the phase lock loop.

1.15 PHASE LOCK LOOP

The Phase Lock Loop is comprised of Z22, Z13, Z6 and Z17 with the Read/Write decoder Z15 providing frequency selection for double density or single density. The phase lock loop has raw read data as reference input to a phase detector Z22. Z8 provides a 150 ns signal to the floppy controller chip. The signal input to the phase detector is derived from the variable frequency oscillator (VFO) in Z6. The phase detector provides a pulse output which is integrated in Z13. The output of Z13 is the difference between the phase detector output and the voltage setting of R22. With no output

from the phase detector, the output of Z13 will be a voltage sufficient to drive the variable frequency oscillator to 8 mHz output. If there is a phase or frequency difference between the reference input to the phase detector and the divided by eight output of the VFO, the phase detector will output a signal that will be added to or subtracted from the output of the Z13 thus decreasing or increasing the output frequency of Z6.

The reference input to the phase detector is actually (via Z8), the reshaped and inverted floppy drive read signal. Therefore the output of the VFO will track the phase of the read signal from the floppy drive.

The output of the VFO is divided by eight in Z15 and Z10 and used as input to the phase detector. This divided by eight signal is again divided by two in Z17 and used as the data window required by the FD1797. Note that the division ratio changes depending upon disk size and the density selected for that disk.

The RC network surrounding Z13 is used as a filter for the pulses at the output of the phase detector Z22 and as the low pass filter required for proper lock and capture range of the phase lock loop.

1.16 JUMPERS AND MODIFICATIONS (See SUPPLIMENT Sheet for REV. B & C Boards)

Provision has been included in the FDC880H-1 to allow only one modification. The modification, if used, will require a different BIOS (see software manual for a complete description of the BIOS.) The bootprom will be CDR 81C or 81B depending upon the Zenith/Heath I/0 prom 444-61 or 444-43 and cassette usage desired.

If other I/0 devices or modifications are made to the H88/H89 it may be desired to operate the FDC 880H-1 at a different I/0 port. Provision has been made to allow cutting the printed circuit trace between E1 and E2 and installing a jumper between E2 and E3 to allow using the H88/H89 with the Zenith/Heath supplied I/0 prom 444-61 for controller operation. This requires a different BIOS supplied by CDR Systems.

Prom 81B is supplied by CDR Systems with your order if you are using an H88 or H89 containing prom set 444-44, 444-42, 444-43. The FDC 880H is then addressed at the I/0 serl port (DO HEX) and may be placed in any I/0 slot. This will allow using the cassette system if desired along with the floppy system.

Prom 81C is supplied by CDR Systems with your order if you are using an H88 or H89 which contains the MTR 89 monitor prom from Heath/Zenith and the I/0 prom 444-61 with I/0 port DO HEX used. The FDC 880H is then constrained to the cassette I/0 slot and the jumper on the FDC 880H between E1 and E2 must be cut. A jumper must be placed between E2 and E3. The FDC 880H is then addressed at cassette I/0 port 7BH thru 7FH.

Note that CDR Systems supplies a zero origin prom for H88/H89 when your unit does not contain the Heath prom 444-66 (zero origin for CP/M).

1.17 INDEX STRIPPER

The Index Stripper block is used to allow separation of 5¼" hard sector disk sector pulses from the 5¼" hard sector disk index pulses. The circuit is configured to allow only index pulses to appear at the floppy controller chip.

SECTION II
INSTALLATION

2.1 INTRODUCTION

The FDC 880H-1 is intended to be installed inside the H88/H89 All-in-One Computer. It may be installed in any one of the two card positions provided for accessories, i.e., the cassette, Serial I/O [redacted] position. The FDC 880H-1 obtains power and signals from any of these positions. If the Heath/Zenith I/0 prom 444-61 is at position U550, then the FDC 88H must be placed in the cassette slot.

2.2 CABLE

The output of the FDC 880H-1 is a cable connected to J3 and/or J4. The cable is routed around the I/O card positions and feeds through the space between the hinges for the top of the H88/H89. The cable has standard board edge connectors configured for Shugart or Siemans floppy disk drives. The H89 floppy drive may be connected to J4. Other 5¼" drives may be daisy chained from this connector.

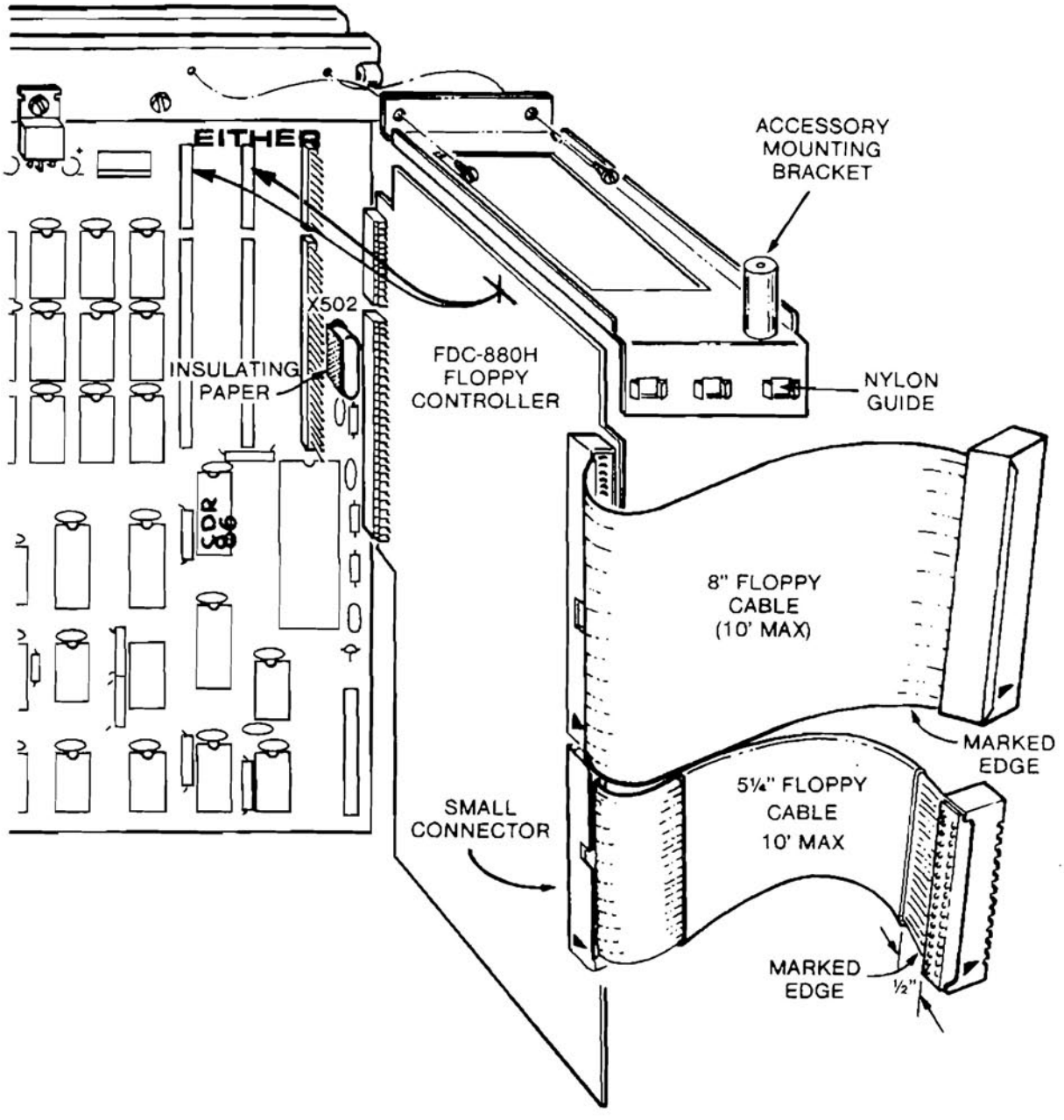
2.3 PROMS (SEE SUPPLIMENT)

Two proms must be installed in the H88/H89 to utilize the standard software for CP/M [redacted] 2.2. These proms are simply plugged into the provided sockets at U517 and U520. U517 is the famous zero origin prom required for CP/M and U520 contains the FDC 880H-1 BOOT program to allow the H88/H89 to start immediately running CP/M. If you already have the Heath/Zenith prom 444-66 you may leave it in place. SEE APPENDIX A-7.

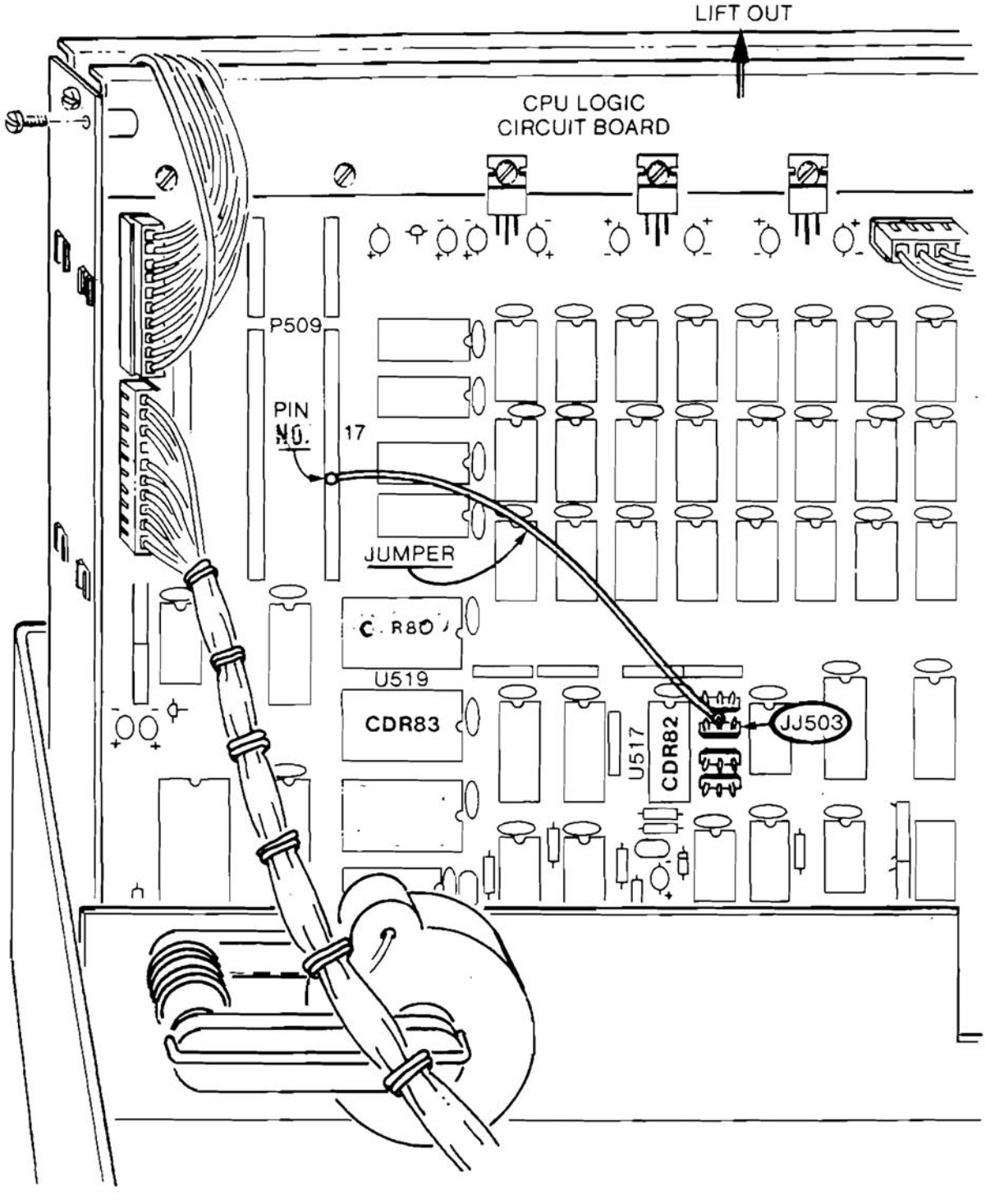
2.4 PHASE LOCK ADJUSTMENTS

The phase lock loop is adjusted by varying R22. This adjustment is factory preset. In the rare event that the phase lock loop requires adjustment the following procedure should be used:

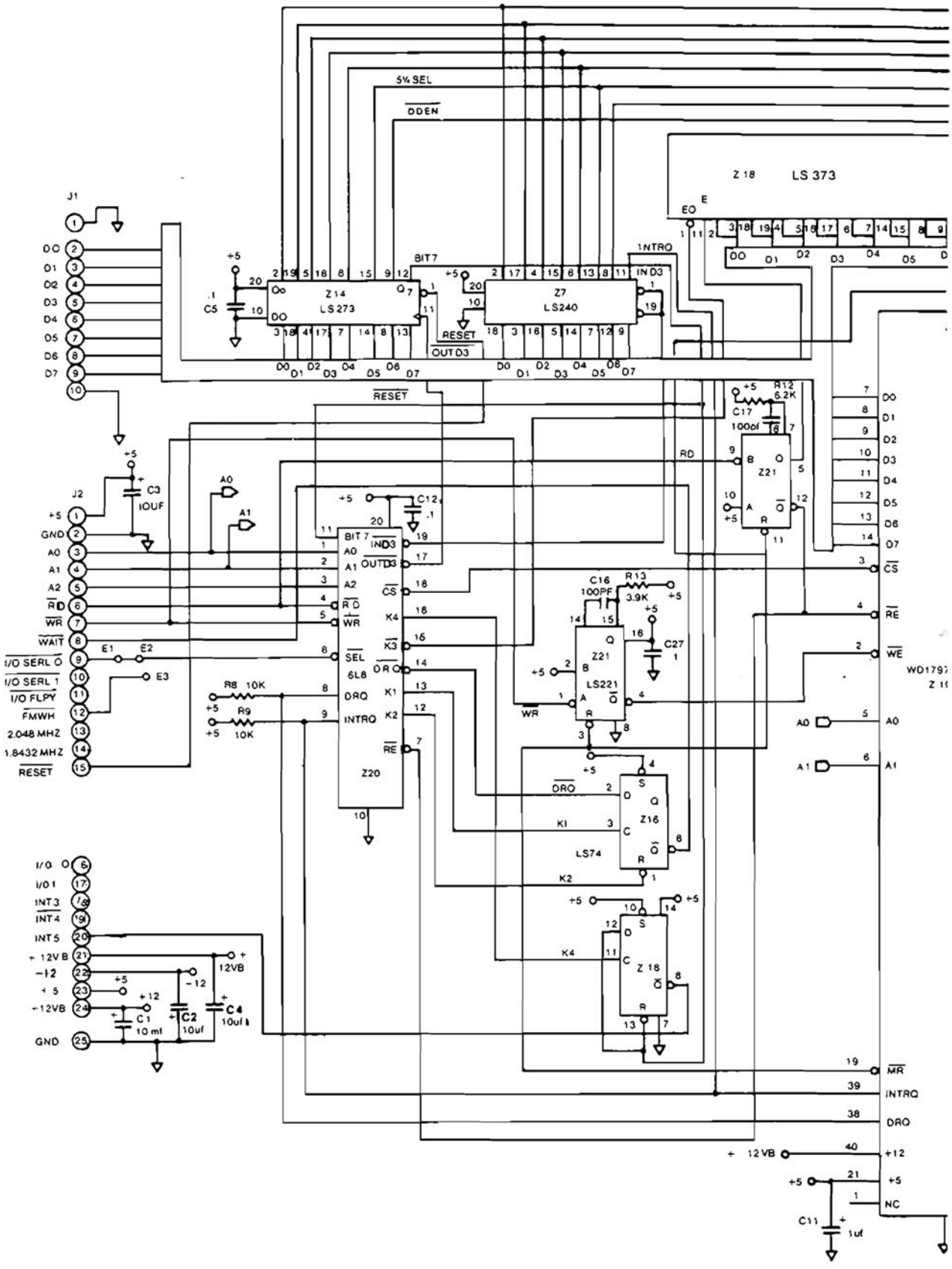
a. Obtain a dual oscilloscope, and an alignment diskette; i.e., a disk with all ones or a header area with all ones or all zeros.
b. Connect one channel of the scope to Z17 Pin 9 sync on this channel and the other channel to Z22 Pin 1.
c. Using a single density disk for alignment, adjust R22 until the signal at Z22 Pin 1 has its leading edge centered on the positive or negative half of the signal at Z17 Pin 9.
d. Note the voltage at Pin 3 at U13. It should be between 3.10 and 3.90 volts.
e. Note the frequency of the signal at Z17 Pin 9. It should be between 1.7 MHz and 2.0 MHz , nominal 1.95 MHz
f. The diagnostic program contained in the BOOT Prom supplied with the FDC 880H will allow continuous reading from a disk. It is suggested that this program be executed and R22 adjusted into the middle of the range that provides proper operation; i.e., no read errors reported on the screen during the execution of the program and a bell signal that is heard when the next track is accessed. The bell signal indicates a successful track read or signals that the screen should be observed for an error. Error messages are listed in the Software Manual.



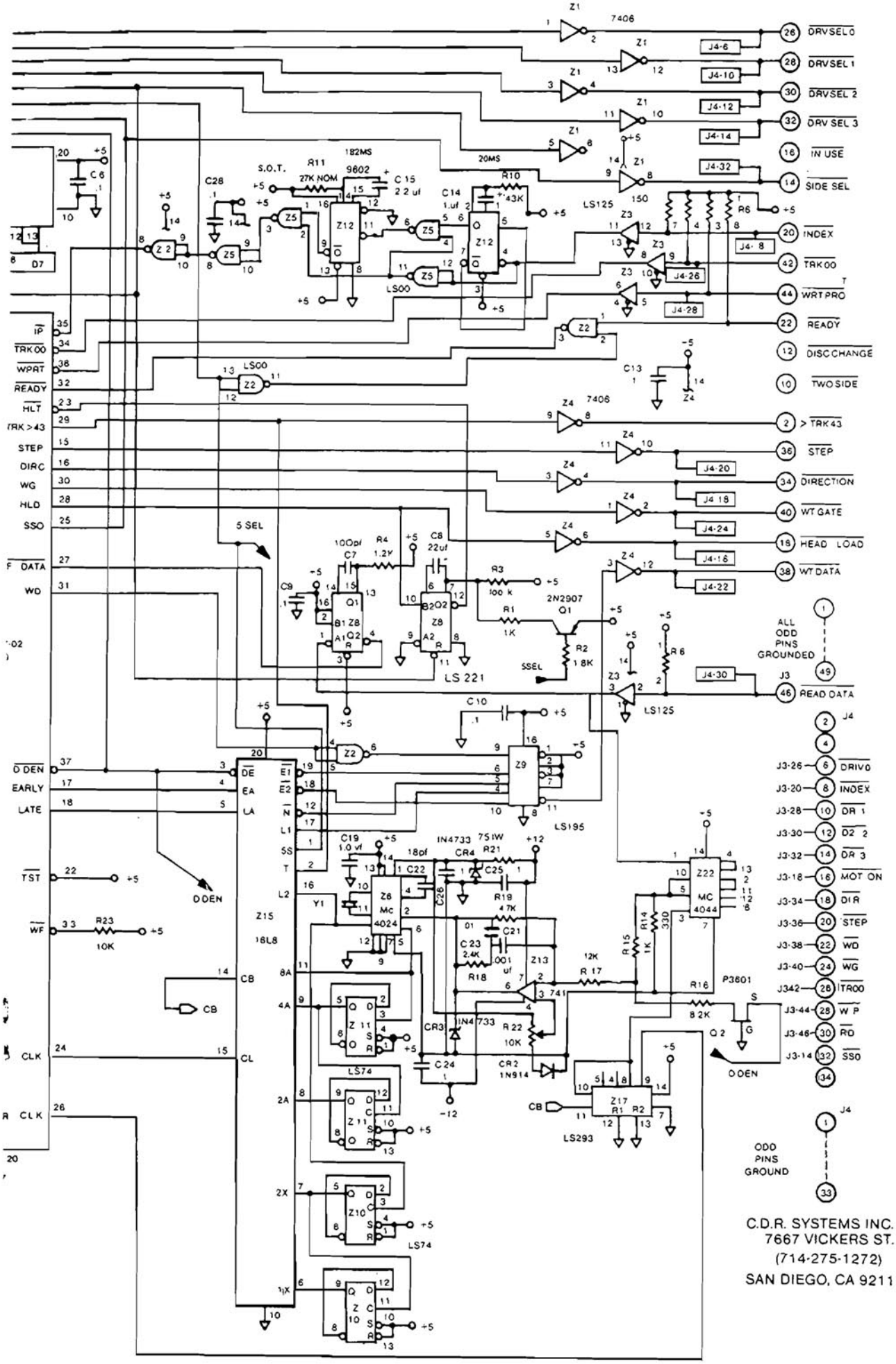
FDC-880H INSTALLATION GUIDE



PROM AND JUMPER INSTALLATION GUIDE


5¼ SEL
DDEN
Z 18 LS 373
J1
BIT7
INTRQ
Z14 LS 273
Z7 LS240
RESET
OUT D3
IN D3
J2
C3 10UF
C12 .1
C5 .1
R12 6.2K
C17 100pf
Z21
RD
A0
A1
BIT 7
IND3
OUTD3
CS
RD
WR
K4
K3
SEL
6L8
DRQ
INTRQ
K1
K2
RE
Z20
C16 100PF
R13 3.9K
C27 1
LS221
WR
WD1797
Z 16
LS74
Z 18
E1
E2
E3
R8 10K
R9 10K
WAIT
I/O SERL 0
I/O SERL 1
I/O FLPY
FMWH
2.048 MHZ
1.8432 MHZ
RESET
I/O 0
I/O 1
INT3
INT4
INT5
+ 12VB
-12
+ 5
-12VB
GND
C1 10 mf
C2 10uf
C4 10uf
C11 1uf
MR
INTRQ
DRQ
+12
+5
NC

Schematic


7406
DRVSEL0
DRVSEL 1
DRVSEL 2
DRV SEL 3
IN USE
SIDE SEL
INDEX
TRK00
WRT PRO
READY
DISC CHANGE
TWO SIDE
> TRK43
STEP
DIRECTION
WT GATE
HEAD LOAD
WT DATA
READ DATA
ALL ODD PINS GROUNDED
ODD PINS GROUND
LS 221
LS125
LS195
LS74
LS293
2N2907
IN4733
IN914
P3601
182MS
20MS
S.O.T.
5 SEL
SSEL
DDEN
CB
Z15
16L8
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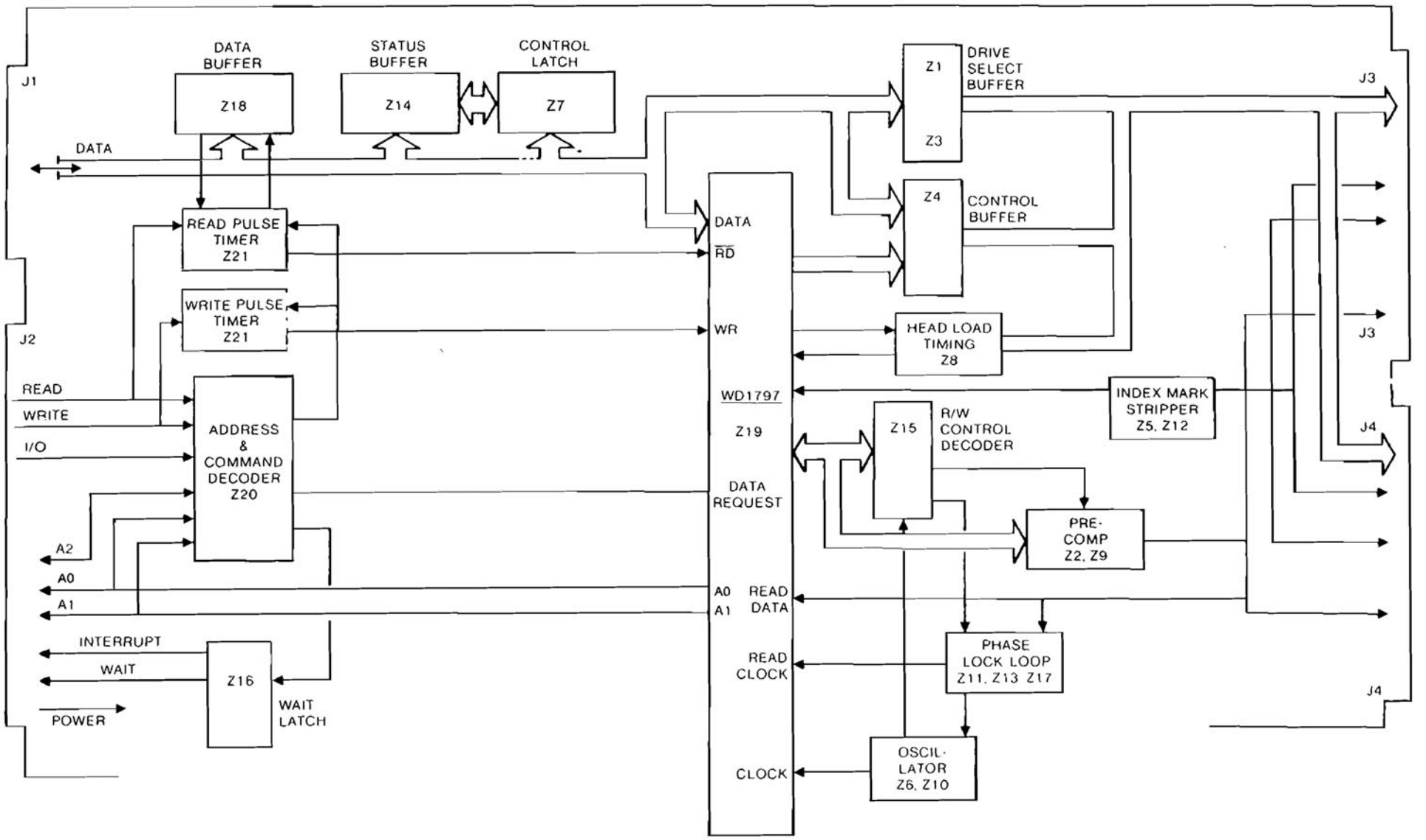
(714-275-1272)
SAN DIEGO, CA 92111

SECTION III
APPENDICES



BLOCK DIAGRAM FDC-880H

PARTS LIST

CDR Systems •

DESCRIPTION	DWG. NO.	08708	
FDC 880H-1	DATE: 1-4-81	SH 1 OF 3	REV. A
	PART NO.		

ITEM	QUANT.	NOMEN/DESCRIPTION		VENDOR	CDR NO.		
C1			10 UF 25V TANT.				
C2			10 UF 25V TANT.				
C3			10 UF 10V TANT.				
C4			.1 UF 50V CERAMIC				
C5			.1 UF 50V CERAMIC				
C6			.1 UF 50V CERAMIC				
C7			100 pf 5% DIPPED MICA				
C8			22 UF 10V TANT.				
C9			.1 UF 50V CERAMIC				
C10			.1 UF 50V CERAMIC				
C11			1.0 UF 25V TANT.				
C12			.1 UF 50V CERAMIC				
C13			.1 UF 50V CERAMIC				
C14			1 UF 25V TANT.				
C15			22 UF 10V TANT.				
C16			100 pf 5% DIPPED MICA				
C17			100 pf 5% DIPPED MICA				
C18			.1 UF 50V TANT.				
C19			1.0 UF 25V TANT.				
C20			.1 UF 50V CERAMIC				
C21			.001UF MYLAR 10%				
C22			18 pf 5% DIPPED MICA				
C23			.01 UF MYLAR 10%				
C24			.1 UF 50V CERAMIC				
C25			.1 UF 50V CERAMIC				
C26			1 UF 25V TANT.				
C27			.1 UF 50V CERAMIC				
C28			1 UF 25V TANT.				
			- ACCESSORIES -				
Z30	1	PROM	6309-1		CDR 82		
Z31	1	PROM	TMS 2716		CDR 83		
A1	1		CABLE, 10', WITH CONNECTIONS		CDR 09078		
Z32		PROM	2716		CDR 81B		
Z32		PROM	2716 ALT. TO Z32		CDR 81C		

PARTS LIST

CDR Systems •

DESCRIPTION: FDC 880H-1

DWG. NO. 08708

DATE: 1-4-81 | SH 2 OF 3 | REV. A

PART NO.

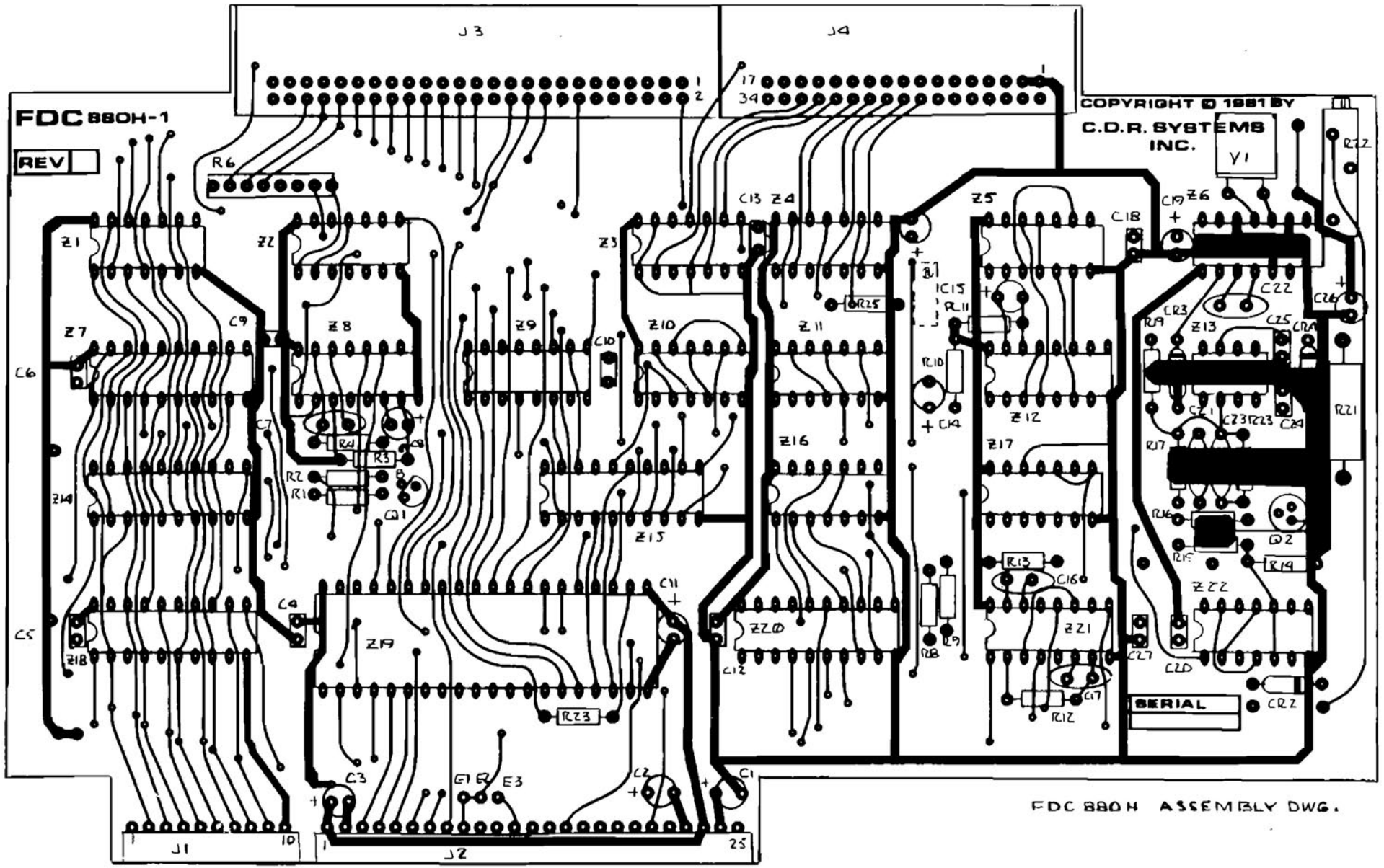
ITEM	QUANT.	NOMEN/DESCRIPTION	VENDOR	CDR NO.		
R1		1.0k ohms 5% ¼W				
R2		1.8k ohms 5% ¼W				
R3		100k ohms 5% ¼W				
R4		1.2k ohms 5% ¼W				
R5		NOT USED				
R6		150 ohms SIP				
R7		NOT USED				
R8		10k ohms ¼W 5%				
R9		10k ohms ¼W 5%				
R10		43k ohms ¼W 5%				
R11		27k ohms ¼W5% nominal (Two resistors may be used)				
R12		6.2k ohms ¼W 5%				
R13		3.9k ohms ¼W 5%				
R14		330 ohms ¼W 5%				
R15		1k ohms ¼W 5%				
R16		8.2k ohms ¼W 5%				
R17		12k ohms ¼W 5%				
R18		2.4k ohms ¼W 5%				
R19		4.7k ohms ¼W 5%				
R20		NOT USED				
R21		75 ohms 1W 5%				
R22		10k ohms POTENTIOMETER				
R23		10k ohms 5% ¼W				
R24		NOT USED				
R25		330 ohms ¼W 5%				
CR1		NOT USED				
CR2		1N914 DIODE				
CR3		IN4733A ZENER				
CR4		IN4733A ZENER				
SK4	11	14 PIN SOCKET				
SK6	4	16 PIN SOCKET				
SK8	1	8 PIN SOCKET				
SK20	5	20 PIN SOCKET				
SK40	1	40 PIN SOCKET				

PARTS LIST

CDR Systems •

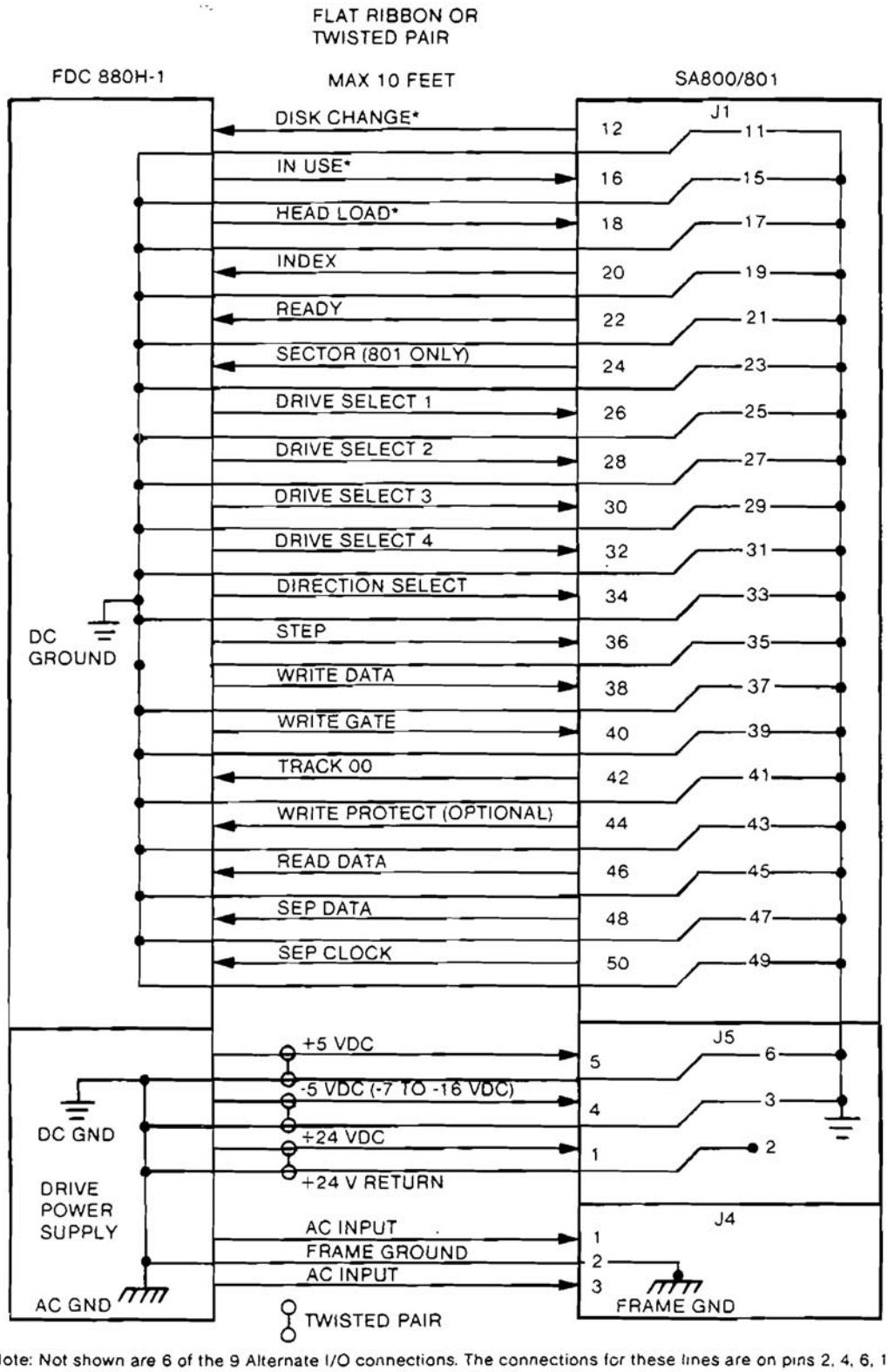
DESCRIPTION	DWG. NO.	08708
FDC 880H-1	DATE: 1-4-81	SH 3 OF 3 REV. A
	PART NO.	

ITEM	QUANT.	NOMEN/DESCRIPTION	VENDOR	CDR NO.
Z1		7406		
Z2		74LS00		
Z3		74LS125		
Z4		7406		
Z5		74LS00		
Z6		MC4024		
Z7		74LS240		
Z8		74LS221		
Z9		74LS195		
Z10		74LS74		
Z11		74LS74		
Z12		F 9602		
Z13		LM741C		
Z14		74LS273		
Z15		16L8		CDR 85A
Z16		74LS74		
Z17		74LS293		
Z18		74LS373		
Z19		WD1797-02		
Z20		16L8		CDRi84
Z21		74LS221		
Z22		MC4044		
Q1		2N2907 TRANSISTOR		
Q2		P3601 FET		
Y1		4MHz CRYSTAL	H18 CASE	
J1		10 PIN CONNECTOR	MOLEX	
J2		25 PIN CONNECTOR	MOLEX	
J4		34 PIN CONNECTOR	BERG	
J3		50 PIN CONNECTOR	BERG	
PC1		PRINTED CIRCUIT CARD		FDC-880H-1



FDC 880H ASSEMBLY DWG.

A-5 Cable Diagram



Note: Not shown are 6 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 10, and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively.

*These lines are alternate input/output lines and they are enabled by plugs

ADDRESS	BIT	DEFINITION
READ D3H or 7BH H88 H89 (STATUS) REV A1, B, and C Boards use 3BH	7 6 5 4 3 2 1 0	0 = INTERRUPT PENDING 1 = SIDE 0, 0 = SIDE 1 1 = 8" DISK, 0 = 5¼" DISK 0 = RESET, 1 = OPERATE FH = NO DRIVE SELECTED EH = DRIVE 0 DH = DRIVE 1 BH = DRIVE 2 7H = DRIVE 3
WRITE D3H or 7BH H88 H89 (COMMAND) REV A1, B, and C Boards use 3BH	7 6 5 4 3,2,1,0	1 = INTERRUPTS ENABLED 1 = SINGLE DENSITY, 0 = DOUBLE DENSITY 1 = 5.25" DRIVE, 0 = 8" DRIVE 1 = OPERATE, 0 = RESET 0 = NO DRIVE 1 = SELECT DRIVE 0 2 = SELECT DRIVE 1 4 = SELECT DRIVE 2 8 = SELECT DRIVE 3

A-7

CPU PROM LOCATIONS AND SWITCH SETTINGS FOR FDC-880H

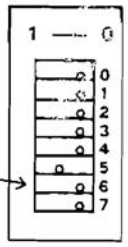
PROM CHART (SEE SUPPLIMENT SHEET, THIS CHART IS NOT VALID FOR) (REVISION A1 , B, AND C BOARDS)

PROM	CPU LOCATION	HEATH H88/H89		ZENITH Z89
MONITOR	U518	444-40	444-62	444-64
ADDRESS DECODE	U517	CDR 82	CDR 82 or 444-66	CDR 82 or 444-66
I/O DECODE	U550	444-43	444-61	444-61
FLOPPY ROM	U520	CDR 81B*	CDR 81C* or CDR 81B*	CDR 81C* or CDR 81B*

SWITCH SETTINGS:

S6 can be placed in the "1" position for 19200 band operation.

SW501



To Boot Primary to CDR Board
Place SW501 s2,s4,s5 ON.
Then you may Boot Secondary
to the Heath Board (H88-1).
"ON" is the "1" position.

JUMPER LOCATIONS:

MEMORY SIZE

CONNECTOR	16K	32K	48K	64K
JJ501	0	1	0	1
JJ502	0	0	1	1
JJ503	CENTER PIN CONNECTED TO PIN 17 ON P507 or P 508 or P509			
JJ504	B	B	B	B
JJ505	O	O	O	O
JJ506	O	O	O	O
JJ507	A	A	A	A

REV B&C Boards NO longer support the Cassette .

*NOTES: 1) PROM 81B uses port DOH, this allows the cassette I/O to be used with the H88/H89. The FDC 880H may then occupy the floppy disc I/O position at P506 and P512.

2) PROM 81C uses the cassette I/O port or (port 78H thru 7FH), thus taking the place of the Z47 I/O board. The FDC 880H must be placed in the cassette I/O slot at P504 and P510.

3) The I/O decode ROM supplied by Heath or Zenith will determine which ROM should be used. If normal cassette operation is still desired then the 444-43 I/O ROM must be in place. The FDC 880H will then use port DOH with PROM CDR 81B required.