UniSite™

Universal Programmer

Maintenance Manual

DATA I/O Corporation

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Safety Summary

General safety information for operating personnel is contained in this summary. In addition, specific **WARNINGS** and **CAUTIONS** appear throughout this manual where they apply and are not included in this summary.

Antistatic Wrist Strap

To avoid electric shock, the antistatic wrist strap must contain a 1MΩ (minimum) to 10MΩ (maximum) isolating resistor.

Definitions

WARNING statements identify conditions or practices that could result in personal injury or loss of life. **CAUTION** statements identify conditions or practices that could result in damage to equipment or other property.

Fuse Replacement

For continued protection against the possibility of fire, replace the fuse only with a fuse of the specified voltage, current and type ratings.

Grounding the Product

The product is grounded through the grounding conductor of the power cord. To avoid electric shock, plug the power cord into a properly wired and grounded receptacle only. Grounding this equipment is essential for its safe operation.

Power Cord

Use only the power cord specified for your equipment.

Power Source

To avoid damage, operate the equipment only within specified line (ac) voltage.

Servicing

To reduce the risk of electric shock, perform only the servicing described in this manual.

Symbols

This symbol indicates that the user should consult the manual for further detail.

V~ This symbol stands for Vac, for example, 120 V ~ = 120 Vac.

This symbol stands for fuse ratings.

This symbol denotes a ground connection.

Certificate of RFI/EMI Compliance with VDE 0871 Limit B

Data I/O certifies that this product complies with the Radio Frequency Interference (RFI) and Electromagnetic Interference (EMI) requirements of VDE 0871 Limit B, as required in German postal regulation number vfg 1046/1984, page 1943.

Data I/O further certifies that the German Postal Service (DBP) has been notified of Data I/O's intention to market this equipment in Germany. Data I/O acknowledges that the DBP reserves the right to retest this equipment to verify its compliance with the regulation.

Zusammenfassende Sicherheitsinformationen

Diese Zusammenfassung enthält allgemeine Sicherheitsinformationen für das Bedienerpersonal. Zusätzlich erscheinen, wenn zutreffend, ausdrückliche Hinweise (ACHTUNG!, VORSICHT!) im Verlauf des Textes. Diese Hinweise werden in dieser Zusammenfassung nicht wiederholt.

Antistatik-Armband

Zum Schutz gegen Stromschläge muß das Antistatik-Armband einen Isolierwiderstand von minimal 1MΩ und maximal 10MΩ enthalten.

Definitionen

Mit **ACHTUNG!** überschriebene Hinweise dienen zur Identifizierung und Warnung vor Zuständen oder Vorgängen, die Verletzungen oder Tod herbeiführen können. **VORSICHT!** dient zum Hinweis auf Zustände und Schritte, die zu Geräte- oder andersartigen Sachschäden führen können.

Ersetzen von Sicherungen

Ersetzen Sie zu Ihrem Schutz gegen Brandgefahr eine durchgebrannte Sicherung nur mit einer Sicherung der angegebenen Nennspannung, Stromart und Typenbestimmung.

Erdung des Gerätes

Das Gerät ist durch den dritten Leiter der Netzschnur geerdet. Stecken Sie die Netzschnur zur Vermeidung von Stromschlägen nur in eine geerdete Steckdose. Richtige Erdung ist für den problemfreien Betrieb dieses Gerätes unerläßlich.

Netzschnur

Verwenden Sie nur die für dieses Gerät vorgesehene Netzschnur.

Stromquelle

Vermeiden Sie Beschädigungen des Gerätes durch den Betrieb an der vorgeschriebenen AC-Netzspannung.

Wartung/Reparatur

Führen Sie zum Vermeiden von Stromschlägen nur die in diesem Handbuch erwähnten Wartungsarbeiten durch.

Symbole

Dieses Symbol bedeutet, da das Handbuch weitere dem Bediener hilfreiche Hinweise enthält.

V~ Dieses Symbol bedeutet VAC (Volt Wechselstrom); z.B. 120V ~ = 120 VAC.

Dieses Symbol bezeichnet Sicherungsdaten.

Dieses Symbol für Masseverbindung.

Bescheinigung des Herstellers/ Importeurs

Data I/O bescheinigt hiermit, daß dieses Erzeugnis in Übereinstimmung mit den Bestimmungen der DBP-Verfügung Nr. 1046/1984, Seite 1943 (Amtsblattverfügung) funkentstört ist und den Vorschriften der Grenzwertklasse B nach DIN VDE 0871/6.78 entspricht.

Data I/O erklärt weiterhin, daß das Inverkehrbringen dieses Gerätes in Deutschland der Deutschen Bundespost angezeigt wurde, und daß letzterer die Berechtigung auf Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt wurde.

Résumé des consignes de sécurité

Ce résumé comprend les informations relatives à la sécurité pour les opérateurs. De plus, tout au long de ce manuel, on retrouve aux endroits appropriés, des **MISES EN GARDE** et des **AVERTISSEMENTS** spécifiques qui ne sont pas inclus dans ce résumé.

Bracelet antistatique

Afin d'éviter tout choc électrique, le bracelet antistatique doit renfermer un résistor de 1MΩ (minimum) à 10MΩ (maximum).

Définitions

Les indications de **MISE EN GARDE** signalent les conditions ou pratiques qui pourraient causer des blessures corporelles ou la mort. Les indications d'**AVERTISSEMENTS** signalent les conditions ou pratiques qui pourraient endommager l'équipement ou entraîner d'autres dommages matériels.

Remplacement du fusible

Pour assurer une protection continue contre les risques d'incendie, il faut remplacer le fusible uniquement avec un fusible de voltage, courant et type spécifiés.

Mise à la terre du produit

Le produit est mis à la terre par l'entremise de la borne de mise à la terre du cordon d'alimentation. Pour éviter tout choc électrique, il faut brancher le cordon d'alimentation uniquement dans un réceptacle mis à la terre correctement et dont les fils ont été rattachés correctement. Il est essentiel de mettre cet appareil à la terre pour qu'il puisse fonctionner sans danger.

Cordon d'alimentation

N'utiliser que le cordon d'alimentation spécifié pour votre appareil.

Source d'alimentaion

Pour éviter d'endommager l'appareil, il faut respecter la tension (ca) spécifiée.

Service

Afin de réduire les risques de choc électrique, il faut s'en tenir aux opérations d'entretien et de réparation spécifiées dans ce manuel.

Symboles

Ce symbole indique que l'utilisateur doit consulter le manuel pour obtenir de plus amples détails.

Ce symbole représente le voltage en courant alternatif V ca, par exemple, 120 V ∿ = 120 V ca.

Ce symbole donne les spécifications techniques par rapport au fusible.

Ce symbole dénote un lien à la masse.

Certificat de conformité RFI/EMI en accord avec YDE 0871 Limit B.

Data I/O certifie que ce produit est conforme aux exigences du RFI (Radio Frequency Interference) et du EMI (Electromagnetic Interference) pour le VDE 0871 Limit B, tel que requis par le règlement postal allemand numéro vfg 1046/1984, page 1943.

Data I/O certifie de plus que le service postal allemand (DBP) a été informé des intentions de Data I/O de commercialiser cet appareil en Allemagne. Data I/O reconnaît que DBP se réserve le droit de refaire des essais sur l'appareil afin d'en vérifier la conformité avec la réglementation.

Riepilogo di sicurezza

Questo riepilogo contiene informazioni di sicurezza per il personale addetto alle operazioni. Inoltre, specifiche note di **ATTENZIONE** e di **AVVISO** relative al contesto fanno parte di questo manuale e non sono state ripetute in questo riepilogo.

Cinghia antistatica da polso

Per evitare le scosse elettriche, la cinghia antistatica da polso deve contenere un resistore di isolamento da 1MΩ (minimo) a 10MΩ (massimo).

Definizioni

Le note di **ATTENZIONE** identificano condizioni o procedure che potrebbero causare infortuni personali o decessi. Le note di **AVVISO** identificano condizioni o procedure che potrebbero causare danni all'equipaggiamento o ad altra proprietà.

Sostituzione dei fusibili

Per una continua protezione contro l'eventualità di incendi, sostituire il fusibile solo con un fusibile dai valori nominali di tensione, corrente e tipo specificati.

Messa a terra del prodotto

Il prodotto viene messo a terra tramite il conduttore della messa a terra del cavo elettrico. Per evitare scosse elettriche, innestare il cavo elettrico in una presa correttamente cablata e messa a terra. La messa a terra di questo equipaggiamento è essenziale per un funzionamento sicuro.

Cavo elettrico

Usare solo il cavo elettrico specificato per l'equipaggiamento.

Fonte di alimentazione

Per evitare danni, operare l'equipaggiamento solo entro la tensione (ca) di linea specificata.

Manutenzione

Per ridurre il rischio di scossa elettrica, svolgere solo la manutenzione descritta in questo manuale.

Simboli

Questo simbolo indica che l'utente deve consultare il manuale per ulteriori dettagli.

V~ Questo simbolo indica Vca, ad esempio, 120V~ = 120 Vca.

Questo simbolo indica la capacità nominale dei fusibili.

Questo simbolo contrassegna una messa a terra.

Certificato di conformità RFI/EMI con VDE 0871 Limite B

La Data I/O certifica che questo prodotto è conforme ai requisiti per l'Interferenza delle frequenze radio (RFI) e l'Interferenza elettromagnetica (EMI) di VDE 0871 Limite B, secondo li regolamento postale tedesco numero vfg 1046/1984, pagina 1943.

La Data I/O certifica inoltre che il Servizio postale tedesco (DBP) è stato avvisato dell'intenzione della Data I/O di vendere questo equipaggiamento in Germania. La Data I/O riconosce che il DBP si riserva il diritto di riprovare questo equipaggiamento per verificare la relativa conformità al regolamento.

Resumen de seguridad

En este resumen se proporciona información general sobre seguridad para el personal operario. Además, aparecen notas de **ADVERTENCIA** y **CUIDADO** por todo el manual, donde son apropiadas y no se incluyen en este resumen.

Muñequera antiestática

Para evitar descargas eléctricas, la muñequera antiestática debe contener un resistor aislante de 1 MΩ (como mínimo) a 10 MΩ (como máximo).

Definiciones

Las notas de **ADVERTENCIA** identifican condiciones o prácticas que pudieran dar como resultado lesiones personales o pérdida de la vida. Las notas de **PRECAUCION** identifican condiciones o prácticas que pudieran dar como resultado daños en equipos u otras propiedades.

Reemplazo de fusibles

Para tener protección continua contra las posibilidades de que se produzcan incendios, reemplace los fusibles sólo con otros del tipo, el voltaje y la corriente que se especifican.

Conexión a tierra del producto

El producto se conecta a tierra por medio del conductor de masa del cable de alimentación. Para evitar descargas eléctricas, enchufe el cable de alimentación en un receptáculo alambrado y conectado a tierra de modo correcto.

Cable de alimentación

Use sólo el cable de alimentación especificado para el equipo de que se trate.

Fuente de alimentación

Para evitar daños, haga funcionar el equipo sólo dentro de los voltajes de línea especificados (de ca).

Servicios

Para reducir los riesgos de que se produzcan descargas eléctricas, lleve a cabo sólo los servicios descritos en este manual.

Símbolos

Este símbolo indica que el usuario debería consultar el manual para obtener más detalles.

Este símbolo representa V ca. Por ejemplo, 120 V ∿ = 120 V ca.

Este símbolo representa valores de fusibles.

Este símbolo indica una conexión a tierra.

Certificado de cumplimiento de RFI/EMI con VDE 0871 Límite B

Data I/O certifica que este producto satisface los requisitos de interferencia de radiofrecuencias (RFI) e interferencias electromagnéticas (EMI) de VDE 0871 Límite B, como se requiere en el reglamento postal alemán número vfg 1046/1984, página 1943.

Además, Data I/O certifica también que el Servicio Postal Alemán (DBP) ha recibido una notificación de la intención que tiene Data I/O de vender estos equipos en Alemania. Data I/O reconoce que el DBP se reserva el derecho a reverificar estos equipos para comprobar su cumplimiento de los reglamentos.

Preface

The Preface contains details about telephone support, repair and warranty services, Keep Current™ subscription service, the Bulletin Board Service, typographic conventions and more.

Customer Support Offices

United States

For technical assistance, contact

Data I/O Customer Resource Center
Telephone: 800 247-5700
Fax: 206 882-1043

For repair, warranty service, or Keep Current subscription service, contact your nearest Data I/O Service Center below:

Data I/O Corporate Office
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Telephone: 206 881-6444
Fax: 206 882-1043
Telex: 152167

Data I/O California
1701 Fox Drive
San Jose, CA 95131
Telephone: 408 437-9600
Fax: 408 437-1218

Data I/O Northeastern United States
20 Cotton Road
Nashua, NH 03063
Telephone: 603 889-8511
800 858-5803 (NJ & NY only)
Fax: 603 880-0697

Canada

For technical assistance, contact:

Data I/O Customer Resource Center
Telephone: 800 247-5700
Fax: 206 882-1043

For repair, warranty service, or Keep Current subscription service, contact:

Data I/O Canada
6725 Airport Road, Suite 302
Mississauga, Ontario
L4V 1V2 Canada
Telephone: 416 678-0761
Fax: 416 678-7306

Japan

For technical assistance, repair, warranty service, or Keep Current subscription service, contact:

Data I/O Japan
Sumitomoseimei Higashishinbashi Bldg. 8F
2-1-7, Higashi-Shinbashi
Minato-Ku, Tokyo 105, Japan
Telephone: 03 3432-6991
Fax: 03 3432-6094 (Sales)
03 3432-6093 (Other)
Telex: 2522685 DATAIO J

Germany

For technical assistance, repair, warranty service, or Keep Current subscription service, contact:

Data I/O-Instrumatic Electronic Systems Vertriebs GmbH
Lochhammer Schlag 5a
D-8032 Gräfelfing
Germany
Telephone: 089 858580
Fax: 089 8585810

Other European Countries

For technical assistance, repair, warranty service, or Keep Current subscription service, contact the office below and ask for the number of your local Data I/O representative:

Data I/O Europe
World Trade Center
Strawinskylaan 537
1077 XX Amsterdam, The Netherlands
Telephone: +31 (0)20 6622866
Fax: +31 (0)20 6624427

Other Countries Worldwide

For technical assistance, repair, warranty service, or Keep Current subscription service, contact the office below and ask for the number of your local Data I/O representative:

Data I/O Intercontinental
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA USA 98073-9746
Telephone: 206 881-6444
Fax: 206 882-1043
Telex: 4740166

Technical Assistance

Calling

To help us provide quick and accurate assistance, please be at your UniSite when you call, and have the following ready:

- Software version number and EPROM version (displayed on the UniSite power-up screen)
- UniSite part number, serial number, and model number (on the plate above the port connectors on the back)
- Controller board version. See table below.

UniSite Part Number	Controller Board Version
901-0058-001 — 901-0058-011	First (701-2012)
901-0058-012 and up	Second (701-2313)

To check the controller board version if your UniSite has been serviced or upgraded at a Data I/O Service Center, remove UniSite's cover and look at the lower left corner of the controller board. If it does not have SIMM RAM sockets, it is the first version. If it has SIMM RAM sockets, it is the second version.

- Detailed description of the problem you are experiencing
- Error messages (if any)
- Device manufacturer and part number (if device-related)
- *UniSite Universal Programmer User Manual*

For technical assistance, contact the appropriate Customer Support office listed at the front of the Preface.

Electronic Mail

You can also reach Data I/O via electronic mail (e-mail). To help us provide quick and accurate assistance, please include the information listed above. Also, include your name, phone number, and e-mail address in your message, and send it to one of the following addresses:

```
techhelp@Data-IO.COM
```

or

```
{apple|decwrl|rutgers|gatech|uunet}!pilchuck!techhelp
```

Note: Select one of the five addresses listed above in braces. For example, you might send e-mail to the following address: `uunet!pilchuck!techhelp`.

See your system administrator if you need more information on which address to use.

Warranty Information

Data I/O Corporation warrants this product against defects in materials and workmanship at the time of delivery and thereafter for a period of one (1) year.

The foregoing warranty and the manufacturers' warranties, if any, are in lieu of all other warranties, expressed, implied or arising under law, including, but not limitied to, the implied warranties of merchantability and fitness for a particular purpose.

Data I/O maintains customer service offices throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. For warranty service, contact the appropriate Customer Support office listed at the front of the Preface.

Keep Current Subscription Service

Data I/O offers a one-year subscription to keep your product and documentation up-to-date with the latest features and device support. This subscription also incorporates manufacturer-recommended changes to existing device support to maintain optimum yields, throughput, and long-term reliability.

For more information, or to order a Keep Current subscription service, contact the appropriate Customer Support office listed at the front of the Preface.

Repair Service

After the warranty period, repair services are available at Data I/O Service Centers on a time-and-materials basis, and through a fixed price annual agreement that covers all parts and labor needed to correct normal malfunctions. The annual agreement also provides semiannual performance certification.

For more information, or to order a Repair Service Agreement, contact the appropriate Customer Support office listed at the front of the Preface.

Bulletin Board Service

From the Customer Support Bulletin Board Service (BBS) you can obtain a wide range of information on Data I/O products, including current product information, new revision information, known bugs (and work-arounds), helpful application notes, and other miscellaneous information. In addition, the BBS has a collection of DOS utilities you can download.

Also, the Customer Support BBS message facility allows you to leave messages for Customer Support personnel. For example, you could request support for a specific device or suggest how we can improve our products.

To learn more about the U.S. Customer Support BBS, call it at 206 882-3211. The protocol is 1200/2400/9600 (Courier HST) baud, 8 data bits, 1 stop bit, and no parity. Online help files throughout the BBS help you learn more about the BBS.

For your nearest Bulletin Board Service outside the U.S., contact the appropriate Customer Support office listed at the front of the Preface.

End User Registration and Address Change

If the end user for this product or your address has changed since the Registration Card was mailed, please notify your nearest Customer Support office as listed at the front of the Preface. This ensures that you receive information about product enhancements. Be sure to include the product serial number, if available.

Typographic Conventions

Throughout this manual different typographic conventions represent different cases of input and output.

Keyboard Keys

Keyboard keys may be shown in boxes (for example, [Q]) or as bolded text.

The **Enter** key (or on some keyboards, the **Return** key) is represented by this symbol: [↵].

Key Combinations

Key combinations, such as **Control-Z**, are shown as two key boxes separated by a dash; for example, [Ctrl] – [Z].

A key combination like [Esc] [Ctrl] – [T] means to press and release [Esc], then press [Ctrl] and [T] at the same time.

Variable Input

Variable input is italicized and should be replaced with the requested information. For example, enter **copy** ***filename.hex*** means type copy just as you see it and replace ***filename.hex*** with the name of your file.

Optional Input

Optional items of a command are shown in brackets; for example

[*option1*] [*option2*]...[*optionn*]

Items separated by a vertical bar (for example, OR | OR | ...) are mutually exclusive; that is, only one of the options listed can be specified.

Displayed Messages

Text that appears on the screen will be displayed in a typewriter-like typeface; for example,

```
You will see this text displayed on the screen.
```

1 Introduction

This manual contains the maintenance information for UniSite, and is divided into the following sections:

Introduction	Includes an overview of the product and a complete list of product options.
Disassembly and Reassemby	Describes how to disassemble and reassemble UniSite for troubleshooting or maintenance work.
Theory of Operation	Describes UniSite's theory of operation at the general level and at the detailed block diagram level.
Maintenance/ Troubleshooting	Describes routine maintenance for UniSite and includes information on cleaning and reducing electrostatic discharge and on fault isolation.
Messages	Lists and describes UniSite's system and error messages.
Index	
Appendixes	Includes a list of mnemonics for signal/bus lines used on the controller board schematic, read/write diagrams, and a set of UniSite schematics.

Standard Features

The basic UniSite comes with support for all 28-pin DIP devices, 1MB of RAM, a 40-pin or 48-pin DIP socket module, two 3-1/2" disk drives and two serial (RS-232C) ports.

Available Options

The items listed below are designed to complement the UniSite Universal Programmer. For more information, or to order an item below, contact your nearest Data I/O Customer Support Office as listed in the Preface.

Keep Current Subscription Service
Data I/O offers a one-year subscription to keep your programmer and documentation up-to-date with the latest features and device support. This subscription also incorporates manufacturer-recommended changes to existing device support to maintain optimum yields, throughput, and long-term reliability.

RAM Upgrades
Expands system RAM to a total of 4MB.

PinSite
Expands support to PGA and surface-mount packages (including PLCC, LCC, and SOIC) for all device types up to 84 pins. Uses MatchBook™ Device Carriers to improve throughput and reduce damage that may be caused by traditional sockets for SMD devices.

HandlerSite
Connects UniSite to popular high-speed device handlers for volume programming. Includes HandlerLink™ software for programming and data file management, as well as real-time control of the UniSite and handler. All programming functions are initiated from the PC keyboard. Provides easy "one-button" production setup.

SetSite
Provides set and gang programming support for up to eight E/EPROMs. Accommodates skinny or wide DIP EEPROMs and EEPROMs up to 40 pins.

USM-340 (FPGA Gang Module)
Provides gang programming for up to eight FPGAs. Eight 68-pin PLCC devices can be programmed simultaneously. Requires a minimum of 1MB RAM in UniSite.

Pin Driver Board
Provides additional support for devices with higher pin counts. Each pin driver board provides additional support for four pins. For example, if your UniSite has ten pin drivers, you can program devices with up to 40 pins. If you want to program 48-pin devices, you need to add two pin driver boards to your UniSite.

Cable Set
Includes an additional RS-232C cable and gender changer.

Carrying Case
Protects UniSite from damage during travel. The custom-designed, soft-sided carrying case holds UniSite, the Algorithm disk, the System disk, and the *UniSite Universal Programmer User Manual* . The carrying case is ideal if you use UniSite in the field.

2 Disassembly and Reassembly

This section describes how to disassemble and reassemble UniSite for troubleshooting or maintenance work.

WARNING: The procedures described in this manual should be performed only by trained electronics service personnel. Do not attempt these procedures if you are not qualified to do so.

CAUTION: Observe the ESD requirements outlined in the "Maintenance/Troubleshooting" chapter when performing the disassembly and reassembly procedures.

To perform the disassembly and reassembly procedures, you need the following tools and equipment:

- 3/16" thin-walled nut driver or 3/64" hex key
- Medium flat-head screwdriver
- Long Phillips screwdriver; minimum 5" blade
- Grounded wrist strap
- Antistatic workstation

Table 2-1 lists circuit boards and OEM items, and what needs to be removed in order to gain access to each:

Table 2-1
UniSite Dissassembly

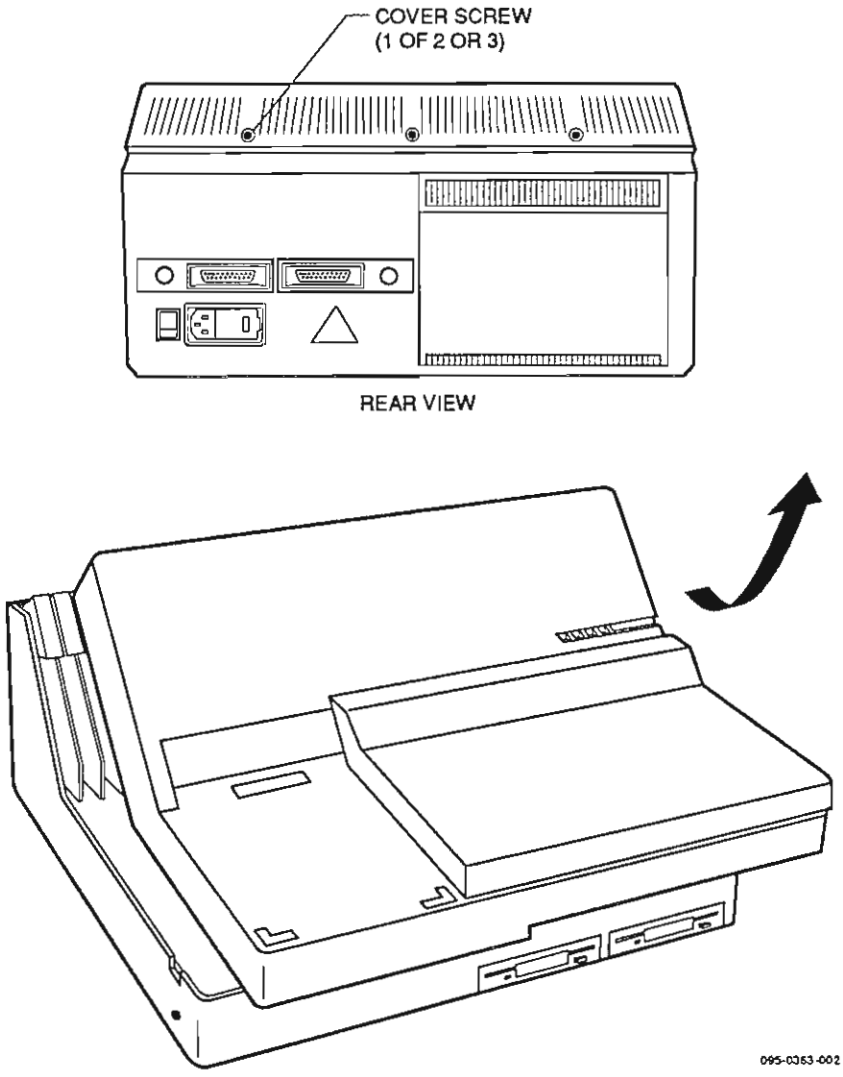
To Access	Remove
Pin driver boards	Top cover
Controller board	Top cover and pin driver boards
Expansion RAM board	Top cover, pin driver boards and controller board
Waveform board, power supply, or fan assembly	Top cover, pin driver boards, controller board and rear panel

Removing the Top Cover

WARNING: To avoid electrical shock, disconnect the power cord before removing the top cover. Do not reconnect the power cord until the top cover has been reinstalled.

1. Place UniSite on an antistatic workstation.
2. Turn off UniSite's power switch.
3. Remove any front panel modules that may be installed (such as the Site 48 or PinSite). You need not remove a blank FSM panel.
4. Remove the power cord from UniSite's rear panel.
5. Using the Phillips screwdriver, remove the two or three retaining screws, shown in Figure 2-1.
6. Remove the top cover by first sliding it toward the front (about 1/4"), then lifting the cover straight up.

Figure 2-1
Removing the Top Cover

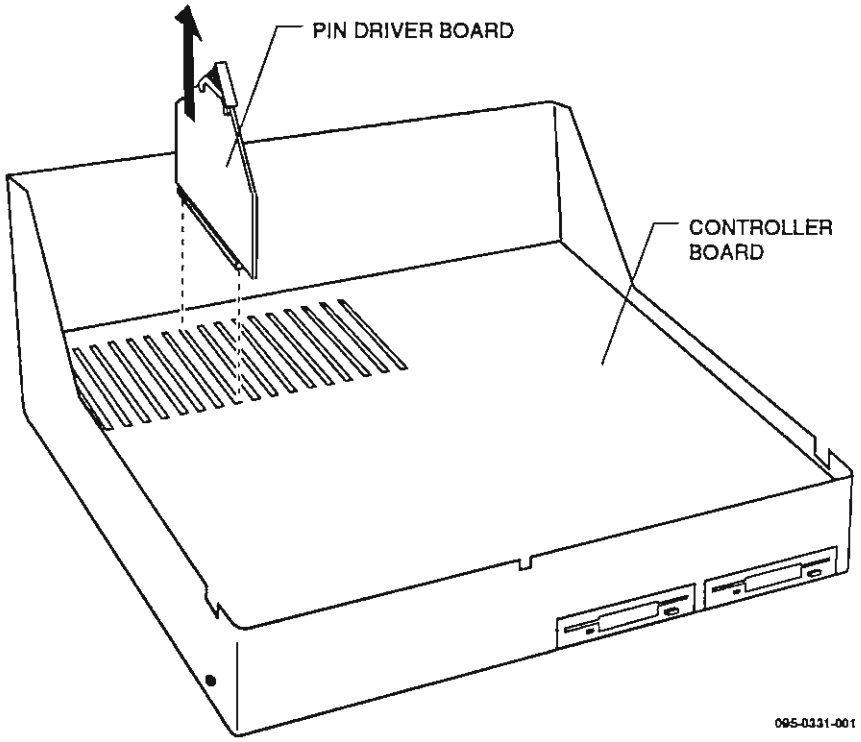


Removing a Pin Driver Board

CAUTION: ***Many of UniSite's components are static-sensitive. Observe standard handling precautions AT ALL TIMES. Perform the procedures at an antistatic workstation and wear a grounded wrist strap; otherwise, damage to the unit may result.***

1. Attach your grounded wrist strap.
2. Lift each pin driver board straight up, making sure you do not bend the controller board's connector pins. See Figure 2-2.
3. Lay each pin driver board on a flat surface on the antistatic workstation.

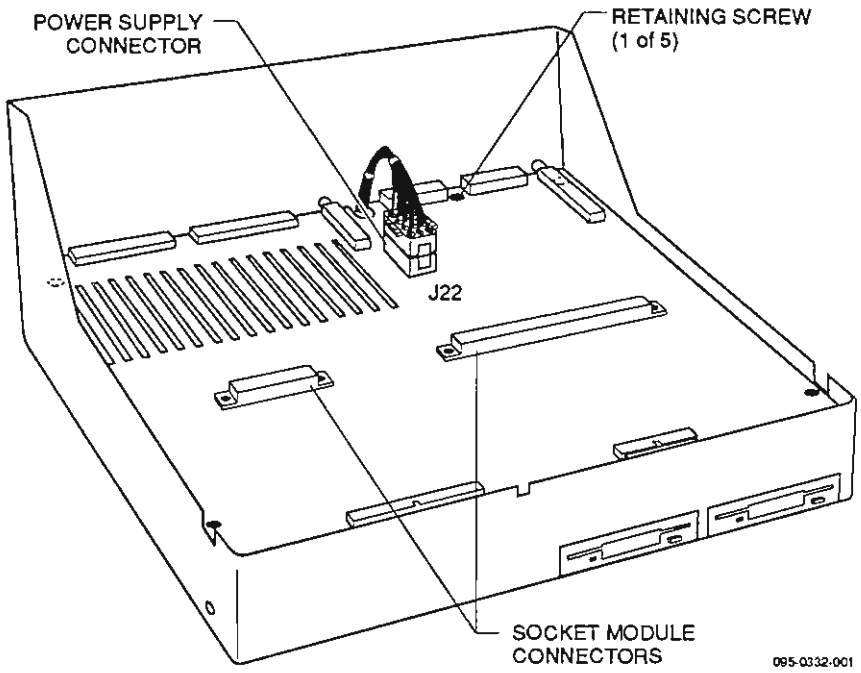
Figure 2-2
Removing a Pin Driver Board



Removing the Controller Board

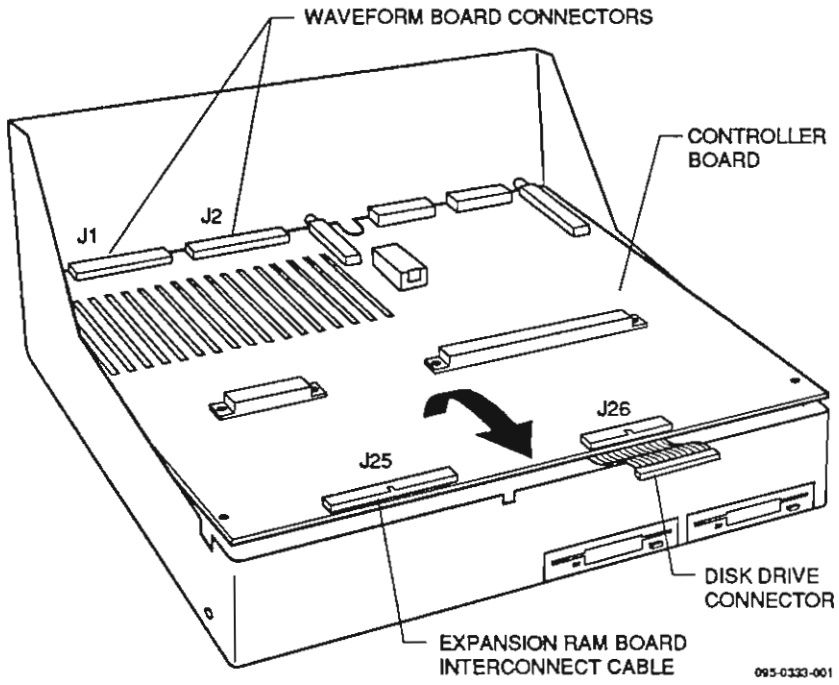
1. Remove the power supply connector cable, located at J22 of the Controller board (see Figure 2-3). Squeeze the two locking tabs on either side of the connector to release it from J22.
2. Using the screwdriver, remove the five retaining screws (see Figure 2-3). Use the nut driver or hex key to remove the four guide pins located at the socket module connectors. If you are using the hex key, insert it into the small holes in the sides of the guide pins.

Figure 2-3
Controller Board Retaining Screw Locations



3. Lift the front edge of the controller board and disconnect the disk drive cable connector, located at J26 (see Figure 2-4). Also, if installed, remove the Expansion RAM board interconnect cable, J25. To avoid damaging the waveform board's connecter pins, do not lift the board vertically more than about one inch.
4. Remove the controller board from the chassis, carefully pulling it away from the two waveform board connecters, J1 and J2.

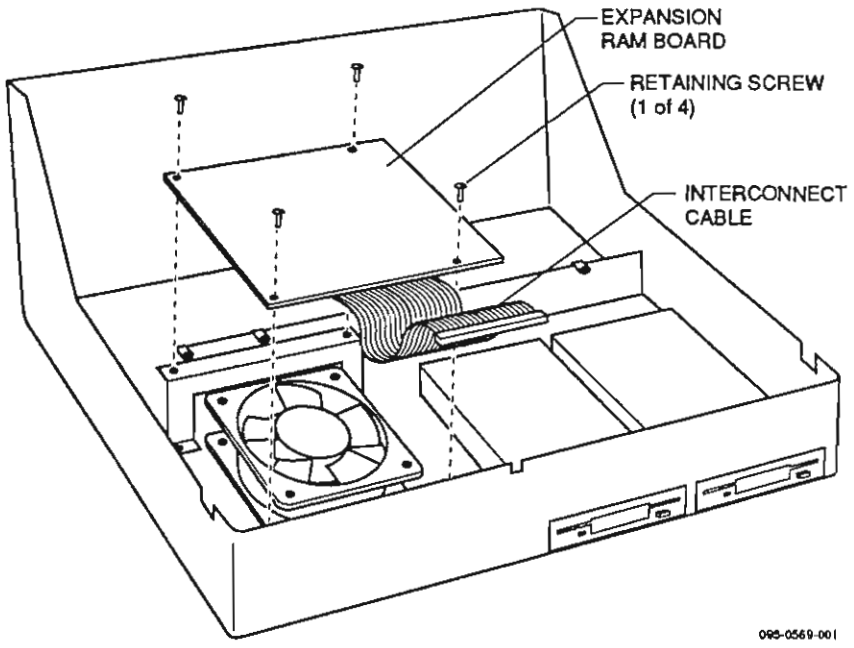
Figure 2-4
Removing the Controller Board



Removing the Expansion RAM Board

1. Remove the top cover, pin driver boards and controller board as described in the previous sections.
2. Remove the four RAM board retaining screws shown in Figure 2-5.

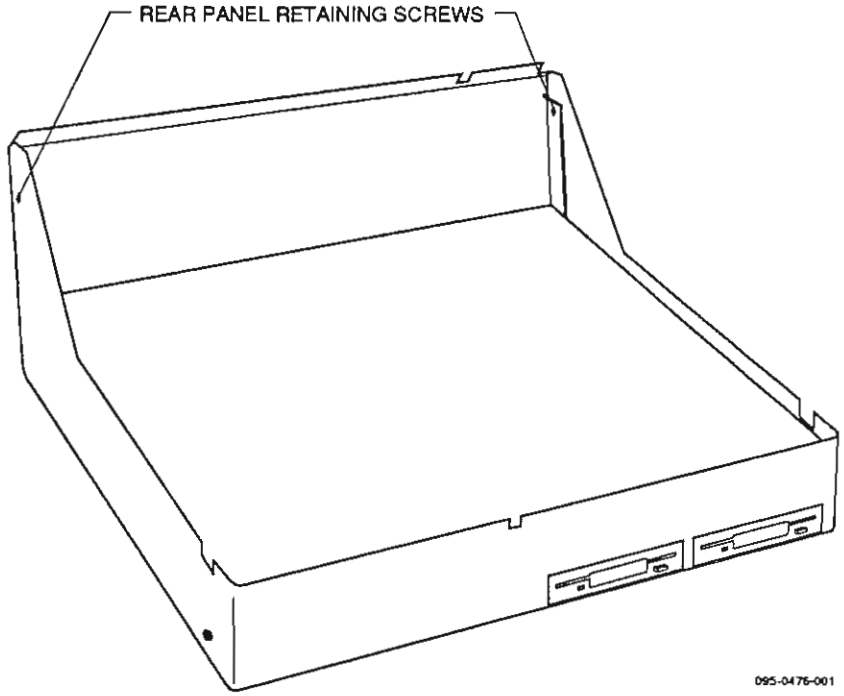
Figure 2-5
Removing the Expansion RAM Board



Removing the Rear Panel

1. Remove the top cover, pin driver boards and controller board as described in the previous sections.
2. Remove the two rear panel retaining screws shown in Figure 2-6. You can now remove the rear panel.

Figure 2-6
Removing the Rear Panel



Accessing the Waveform Board

1. Remove the top cover, pin driver boards, controller board and rear panel, as described in the previous sections.
2. You need not remove the waveform board from the rear panel assembly for troubleshooting or maintenance work.

Other Disassembly

Note: If you have a problem with the disk drives, power supply or fan assembly, remove the faulty unit, and contact your nearest Data I/O Customer Support office to arrange to send the unit in for servicing.

Removing a Disk Drive

1. Remove the four Phillips head screws securing the disk drive to UniSite's chassis.
2. Pull the disk drive from its receptacle.
3. Disconnect the cables to the power supply and controller board.

Removing the Power Supply

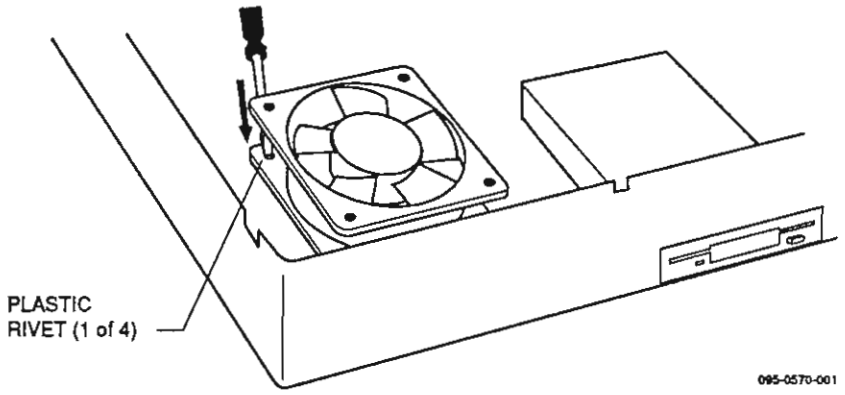
1. Remove the top cover, pin driver boards, controller board and rear panel, as described in the previous sections.
2. Remove the interconnect cable to the fan.
3. Remove the four retaining screws located on UniSite's bottom panel.

Removing the Fan Assembly

1. Remove the top cover, pin driver boards, controller board and rear panel, as described in the previous sections.
2. If your UniSite has an expansion RAM board, remove it at this time.
3. a. If your UniSite fan assembly has plastic rivets holding it to the chassis, press the center of each rivet with a slender (#1) screwdriver until you have pushed it down about 1/8 inch. Then pull the four rivets through the chassis bottom. (See Figure 2-7).

   b. If your UniSite fan is held by screws, tip UniSite so that its bottom panel is facing you, and remove the four fan retaining screws.

Figure 2-7
Removing the Fan Assembly



Reassembly

In general, boards may be installed in the reverse order they were removed. Following are some special hints or notes regarding reassembly.

Reinstalling the Expansion RAM Board

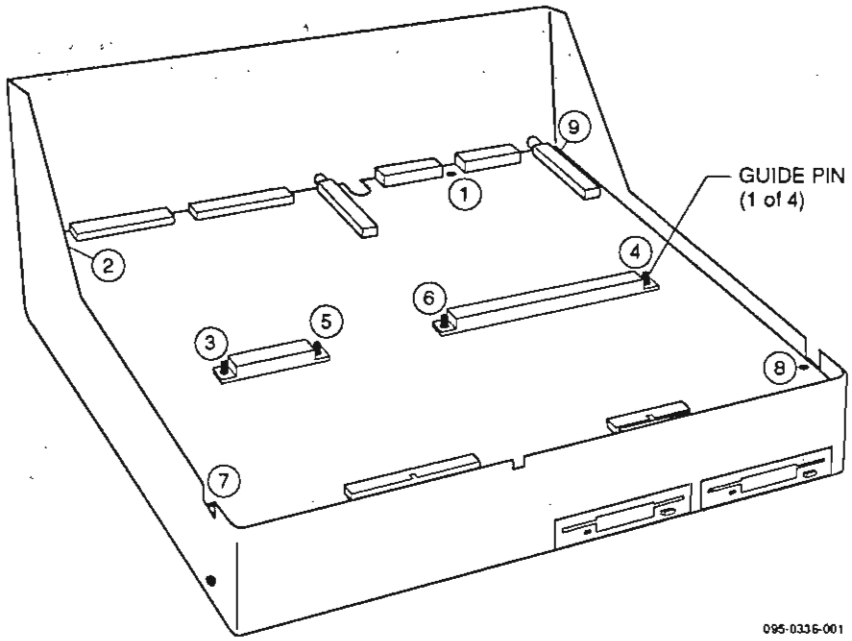
Reinstall the expansion RAM board as follows:

1. Attach the controller board's interconnect cable to the RAM board.
2. Lay the expansion board on the bracket and standoffs, component side down and with the interconnect cable toward the front. Attach the board to the bracket and standoffs using four screws.
3. Thread the expansion board and disk drive interconnect cables up and rest them on the front panel.

Reinstalling the Controller Board

1. Insert the controller board into the waveform board connecters. Take care not to bend the waveform board's interconnect pins.
2. Insert the RAM board interconnect and disk drive cables into the controller board. Gently lower the controller board into the chassis. Push the extra RAM cable length under the expansion board, NOT between the controller and RAM boards.
3. Install the five screws and four guide pins in the order shown in Figure 2-8.

Figure 2-8
Reinstalling the Controller Board



Reinstalling the Pin Driver Boards

CAUTION: Many of UniSite's components are static-sensitive. Observe standard handling precautions AT ALL TIMES. Perform the procedures at an antistatic workstation and wear a grounded wrist strap; otherwise, damage to the unit may result.

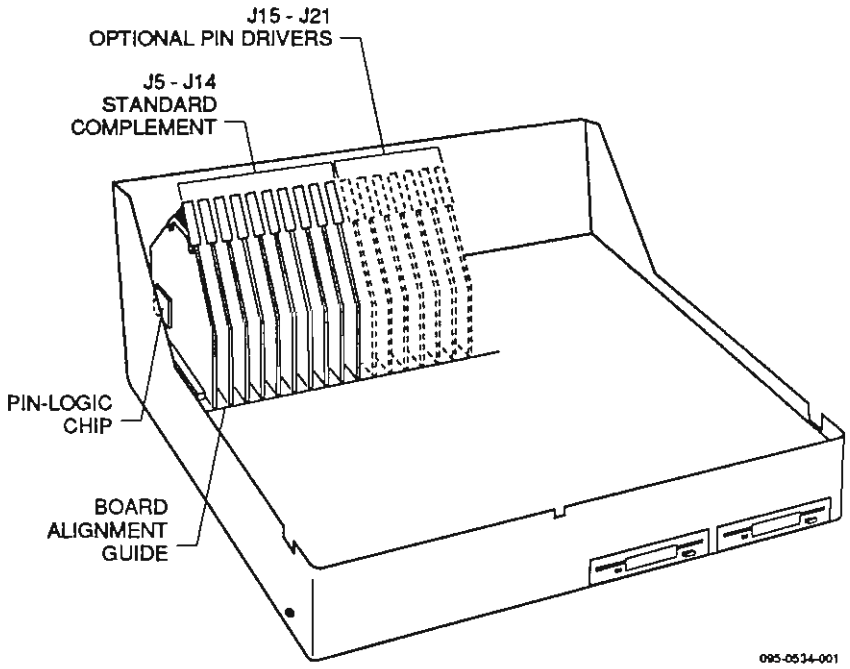
1. Install the pin driver boards with the 68-pin, pin-logic chip facing to the left (see Figure 2-9).
2. Take special care and make certain that the pin driver board connector is perfectly aligned with the controller board's connector pins before you push the board down. Use the white stripe on the controller board as an alignment guide.

CAUTION: USE EXTREME CAUTION WHEN REINSTALLING THE PIN DRIVER BOARDS: THEY ARE LIKELY TO BE DAMAGED IF INSERTED INCORRECTLY!

3. Insert the pin driver boards starting with the J5 connector, and work toward the right. After all the boards have been installed, inspect them to make sure they are correctly inserted: no pins should be visible at the board's base, and the boards should appear evenly aligned with each other.

CAUTION: ***Powering up a UniSite with incorrectly installed pin driver boards can destroy those boards!***

Figure 2-9
Installing the Pin Driver Boards



PLCC/LCC Base Conductive Pad Replacement

About the Pad

The conductive pad is a key element in the MatchBook technology. It is important to keep this pad free of dirt or contamination to ensure good contact between the programmable device pins and the pad.

The life of the pad depends on proper care as well as the device types being used. Typical insertion rates for a standard 20-pin PLCC are around 10,000 cycles. However, not all devices have the same tolerances and each device type may result in different life cycles for the pads.

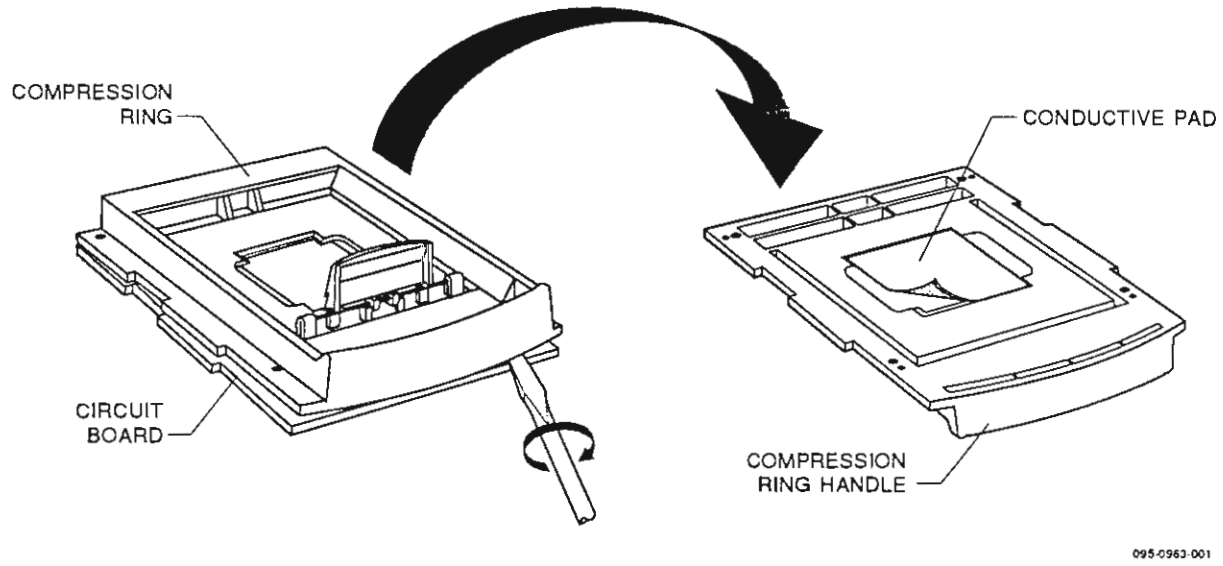
If you experience a sudden drop in your programming yields, it may be an indication that the pad needs to be replaced. The base has been designed to allow you to quickly and easily replace the pad with minimum downtime. Replacement pads are available from Data I/O.

Removing the Old Pad

To replace the conductive pad, you must first separate the compression ring from the circuit board (base unit).

1. While holding the base, gently pry the circuit board from the compression ring with a small screwdriver. (See Figure 2-10.)
2. Turn the compression ring upside down with the handle toward you.
3. Lift the old conductive pad from the compression ring and discard it. Adhesive strips are along the front and back edge.

Figure 2-10
Removing Old Conductive Pad

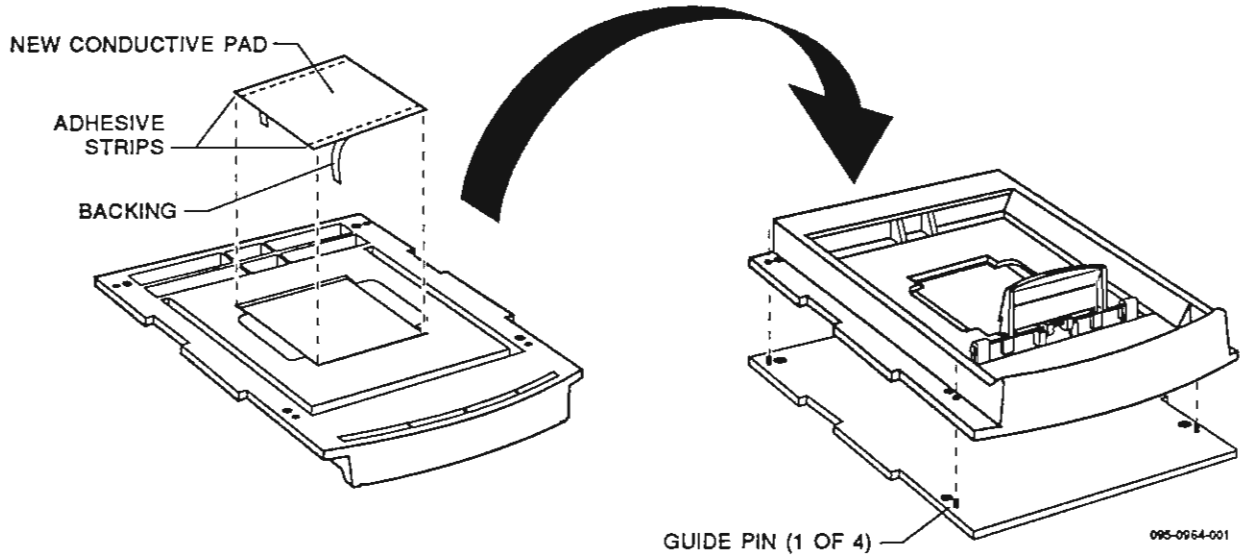


Inserting a New Pad

Use the following procedure to insert a new conductive pad.

1. Take a replacement conductive pad from the plastic bag and remove the adhesive strip backing. (See Figure 2-11.)
2. With the compression ring resting on a flat surface, place the new conductive pad in the recessed area of the compression ring as shown in Figure 2-11.
3. Gently press the adhesive edges down.

Figure 2-11
Installing New Conductive Pad



Reassembling the Base Unit

To reassemble the base, align the guide pins on the circuit board with the guide holes on the compression ring as shown in Figure 2-11. Gently press the circuit board into the compression ring. You may need pliers to ensure that the circuit board in fully engaged.

Pad Care

Inspect and clean each pad as needed; we recommend cleaning the pad approximately every 1000 insertions or once a month. It is normal for the pad to show signs of discoloration as it is used.

Clean the conductive pad of debris by blowing air over the pad. If you use compressed air, direct the air stream from the front or back of the base adapter. Avoid air streams from the side of the pad, which could lift the pad off the circuit board. To further clean the pad, apply a small amount of denatured alcohol on a cotton swab and gently wipe the pad to dislodge dirt. Make sure the pad is clear of any filament left over from the cleaning process.

WARNING: Do not use any petroleum-based or freon-based products to clean the pad. These substances cause premature deterioration of the pad material.

3 *Theory of Operation*

This chapter describes the theory of operation on two levels. It begins with an overall description and block diagram. This is followed by a circuit description and detailed block diagram description of the individual printed circuit boards. The following circuitry is discussed in this chapter.

- Overall UniSite System
- Controller Board
- Waveform Board
- Site 48 Program Specific Module (PSM)
- Site 40 PSM
- PinSite Function Specific Module (FSM)
- SetSite FSM
- ChipSite FSM
- Optional Expansion RAM Board

Note: Because the disk drives and the power supply are not manufactured by Data I/O, their circuitry information is not available for this manual. The pin driver board circuitry is proprietary and is not described here. If you need any of these items serviced, contact your nearest Data I/O Customer Support office.

Overview

The UniSite circuitry consists of the following main components, as shown Figure 3-1.

- CPU
- EPROM
- Pin Control Unit (PCU)
- Power Supply/Fan
- Pin Drivers
- Serial Ports
- Dynamic RAM
- Floppy Disk Controller
- Waveform Board
- 40- or 48-pin Socket Module (Site 40 or Site 48)
- Optional PLCC/SOIC Socket Module (ChipSite or PinSite)
- Optional Gang/Set Module (SetSite)
- Optional Expansion RAM

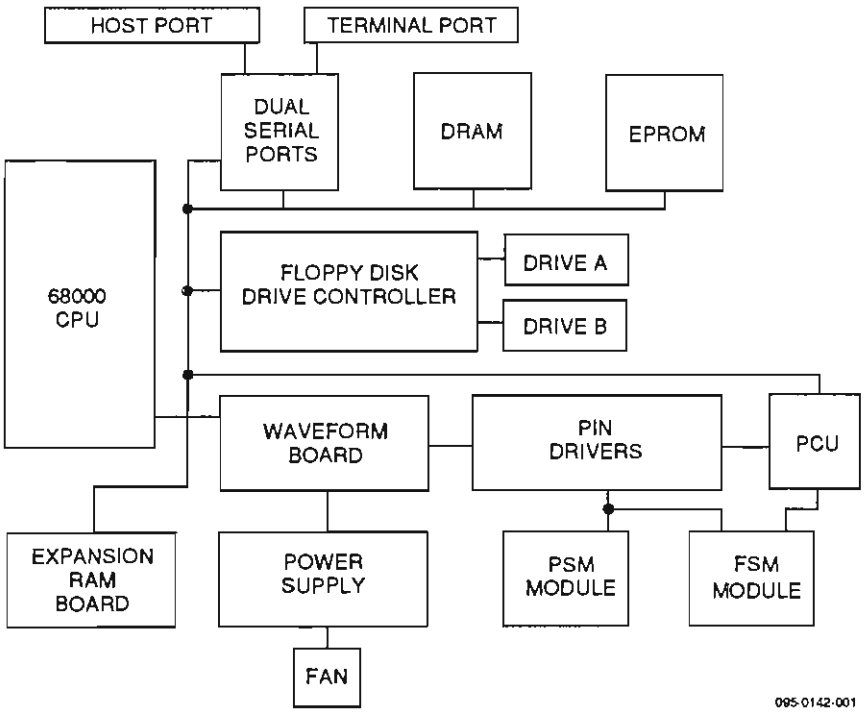


Figure 3-1
UniSite System Block Diagram

General System Description

The central processing unit (CPU) centers around the 10 MHz, 16-bit 68000 microprocessor, which controls all user operations for UniSite. The CPU also has 64K of program memory (EPROM) and from 640KB to 8.5 MB of RAM, depending on configuration. System RAM extends from address 080000 to 0FFFFF on the 701-2012 board and from E00000 to E7FFFF on the 701-2313 board. User RAM occupies address locations from 100000 to 8FFFFF on the 701-2012 board and from 900000 to 9FFFFF on the 701-2313 board.

A complete memory map for controller board 701-2012 is shown in Figure 3-2. A complete memory map for controller board 701-2313 is shown in Figure 3-3.

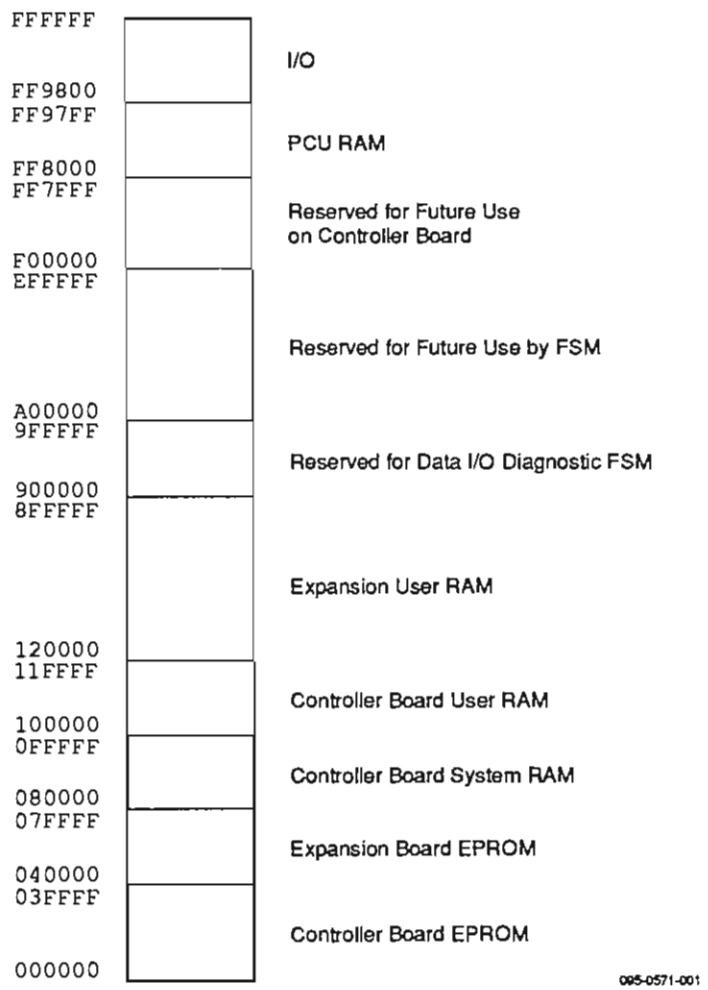
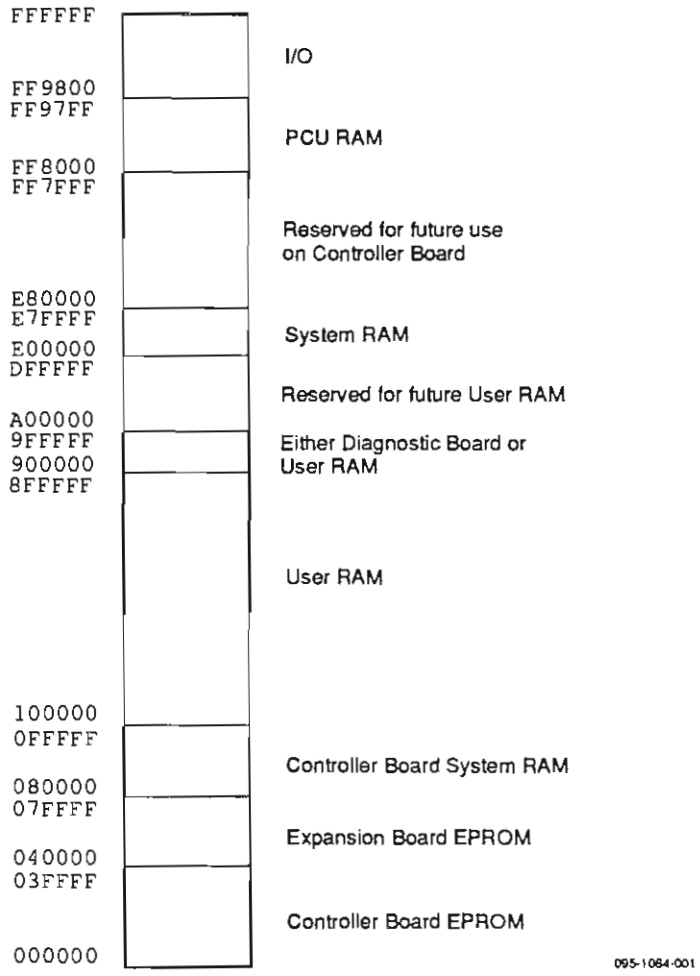


Figure 3-2
Memory Map for Controller Board 701-2012

Figure 3-3
Memory Map for
Controller Board 701-2313



Note: See Appendix A for supplementary control signal diagrams and Appendix B for a list and description of the mnemonics (signal line abbreviations) used in the controller board's schematic.

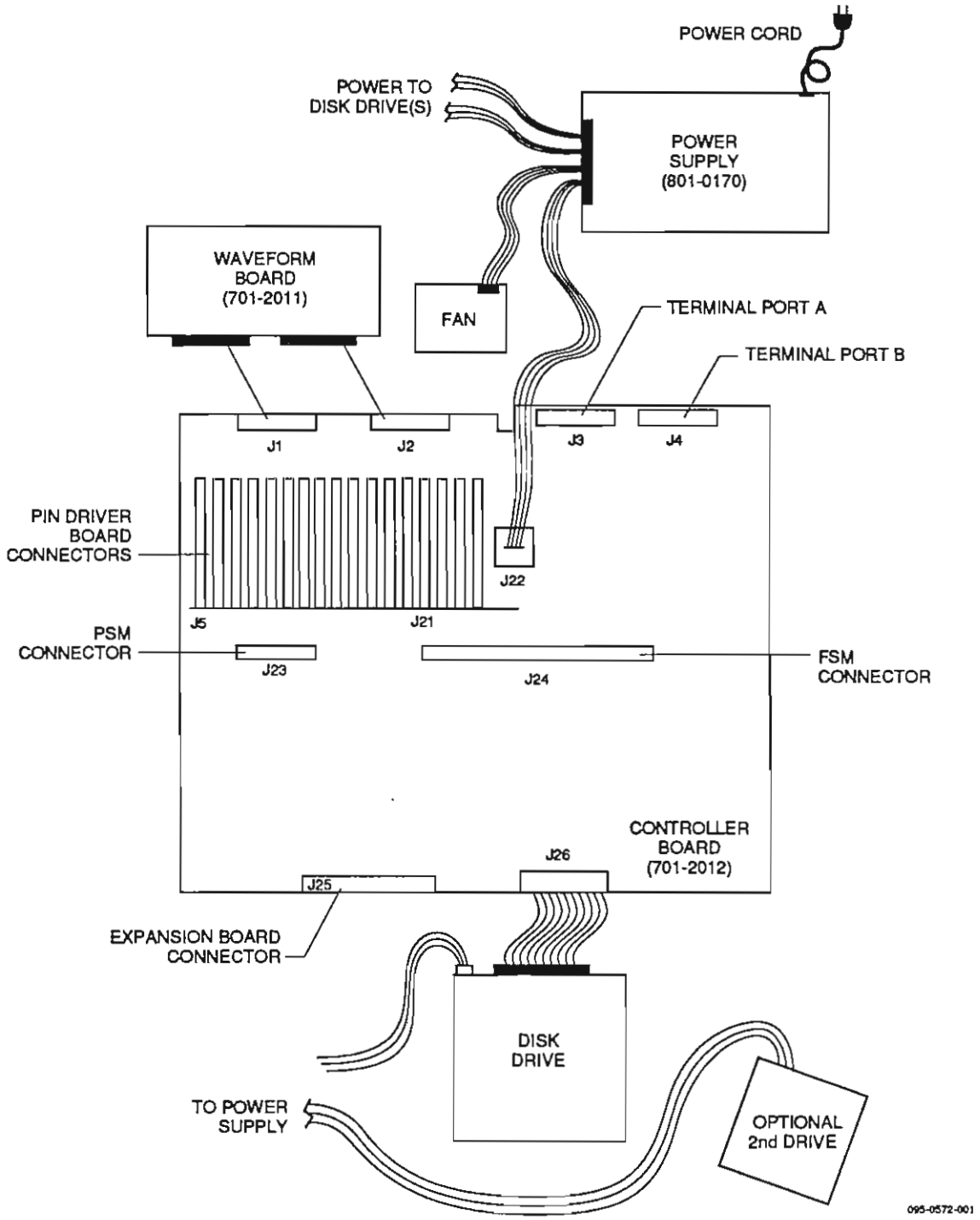
The controller board contains special digital circuitry called the Pin Control Unit (PCU). The PCU provides an interface between the 68000 and the pin logic ICs on the pin driver boards, controlling all the Read/Write operations to the pin drivers.

UniSite's programming hardware is contained in the waveform board and pin driver boards. The waveform board is controlled from the CPU and supplies the necessary voltage and current levels for the pin drivers. See the interconnect diagram shown in Figure 3-2. The pin driver boards interface to the PCU and the waveform board. Each pin driver board has one pin logic IC and two pin driver ICs, supporting four device socket pins.

UniSite includes a custom parallel programming processor, consisting of the PCU and the pin logic ICs on the pin driver boards. Each pin logic chip acts as a 32-bit slice of the programming processor. Therefore, a UniSite with ten pin driver boards installed has an effective word-width of 320 bits.

Optional expansion RAM expands memory capabilities to over 1MB. The RAM may be in the form of SIMMs or it may be located on an expansion board, depending upon the type of controller installed. The expansion RAM board must be installed by authorized Data I/O Customer Support personnel.

Figure 3-4
System Interconnect Diagram



Controller Board

UniSite's controller board (701-2012 or 701-2313) circuitry includes the CPU, disk controller, PCU, EPROM and DRAM. A block diagram of the controller board is shown in Figure 3- 5. See Appendix B for a list and description of mnemonics for the controller board.

Oscillators

First Version Controller (701-2012)

The main frequency generator for the controller board is the 40 MHz oscillator, U67. U41 and U66 combine to make the divide-by-5 and divide-by-4 circuitry. The divide-by-5 becomes 8 MHz that drives both the PCU and disk controller; the divide-by-4 becomes the 10 MHz used by the 68000. The 8 MHz generated from the divide-by-5 is further divided by U44, into 4, 2, 1 and 0.5 MHz clocks. These frequencies are for clock signals used when programming microcontroller devices.

The 68681 DUART obtains its clock signal from crystal Y1. The 68681 oscillator's output is also divided by two, then by 256 twice. The resultant frequency is 28.125Hz, which is used as a real time clock interrupt.

Second Version Controller (701-2313)

Two oscillators generate system timing in conjunction with U66 timing generator. The 40 MHz oscillator provides RAM timing and a 10 MHz clock for the 68000. The 32 MHz oscillator provides 8 MHz for the floppy disk controller. The 8 MHz CLK8 is further divided by U44 into clocks of 4, 2, 1, and 0.5 MHz.

The 68681 DUART obtains its clock signal from crystal Y1. The 68681 oscillator's output is also divided by two, then by 256 twice. The resultant frequency is 28.125Hz, which is used as a real time clock interrupt.

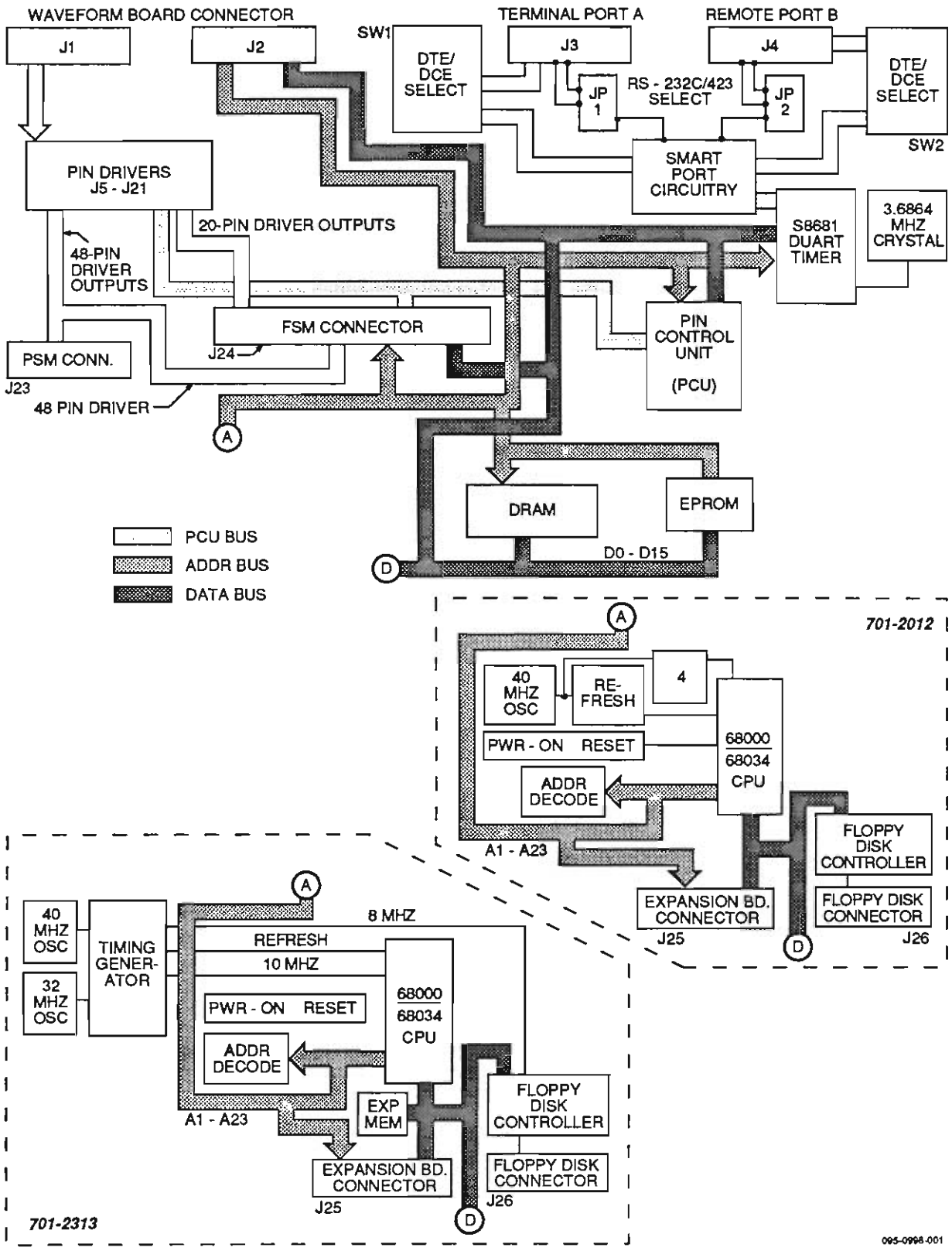
Decoding

U91 arbitrates between refresh and normal memory cycles, and provides five RAS decodes. U91 also controls the data bus buffer and the DTACK signal for DRAM and EPROM. U110 provides detection of emulator cycles, ensuring that no glitches occur in RAS/CAS timing when the controller board is used with an Applied Microsystems 68000 emulator. PAL U92 provides CAS decoding to DRAM, EPROM, the FSM and I/O decodes. U95, U96, U111 and U112 together provide the rest of the system decoding.

Note: The emulator's continuous address strobe parameter has to be enabled in order for the emulator to work correctly.

U39 is a shift register used as a delay, which provides timing signals. These signals are used to generate the DTACK signal at the appropriate times, for all devices decoded by U95 and U96. U90 and U93 are address multiplexers for DRAM. U37 and U78 cause the processor to use auto-vectoring during interrupts. (The processor obtains the interrupt vectors from predetermined EPROM locations.) U63 and U64 buffer the data bus onto the controller board from the kernel (68000, DRAM and EPROM).

Figure 3-5
Controller Board Block Diagram



U94 has a special test shunt, normally installed. When this shunt is removed, it forces the 68000 to execute Move Quick (Read) instructions from all memory address locations. This feature is useful for diagnostic testing of address lines and decoding. While in this condition, the processor executes consecutive Reads throughout the entire memory range.

Dynamic RAM Refresh Circuitry

Dynamic RAM (DRAM) refresh for UniSite occurs every 12 µs. Read/Write timing diagrams for dynamic RAM may be found in Appendix A. U100 takes the 8 MHz from the oscillator circuitry and divides it by 6, yielding 1.33 MHz. U43 works as a delay element to get the 12 µs. U43's pin 9 is the refresh request line, and connects to U99. U99 is used to synchronize the refresh cycle with the end of a 68000 bus cycle. U98 establishes refresh timing and is a shift register, with 100ns delay between RAS and CAS refresh. The DRAM uses the CAS-before-RAS refresh mode, and supplies its refresh address internally.

Serial Port Interfacing

Resistors and capacitors on the port connectors prevent damage to buffers when the SmartPort switch is in the wrong position, and also help protect against electrostatic discharge (ESD).

Two zener diodes on each of the drivers (CR1 and CR2, for example) prevent opposing drivers from harming UniSite and provide ESD protection. The 3.3K resistors going into the receivers also protect against ESD. R47 sets the slew rate for the terminal port; R36 performs the same function for the remote port.

68681 DUART

Serial port interface to the controller board is via the 68681 DUART, U14. The DUART contains two independent serial ports, a baud rate generator, 8 parallel output lines and 6 parallel input lines. Crystal Y1 provides a 3.6864 MHz signal, used by the 68681's baud rate generator.

RS-232C and RS-423 Configurations

Jumpers JP1 and JP2 configure the interface for RS-232C and RS-423 operation. In RS-423 configuration, ground lines for each of the drivers are separated from those of the receivers, providing better noise immunity. Pin 9 of the serial connectors is used as the separate receiver ground in RS-423 configuration.

Floppy Disk Control Circuitry

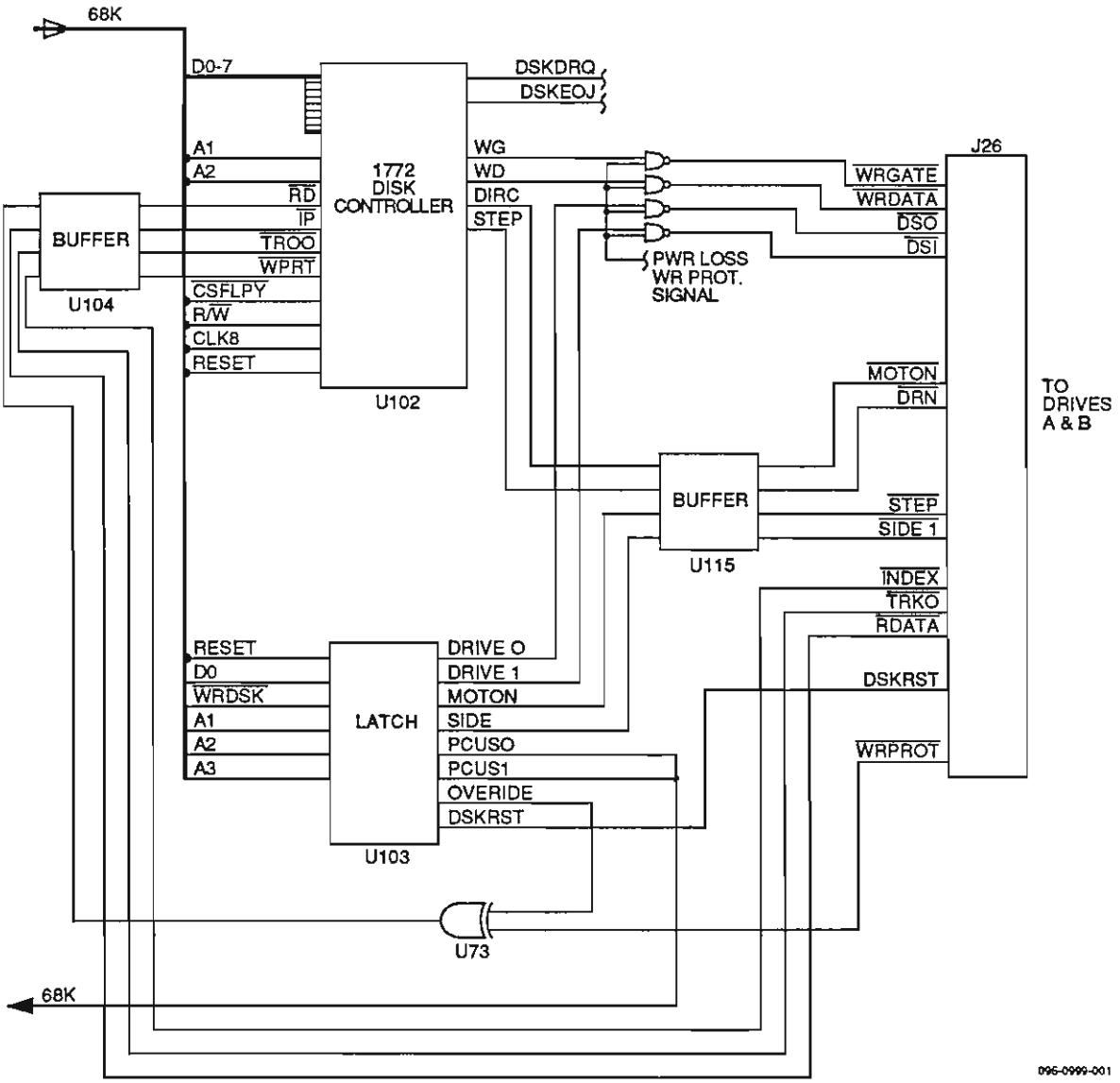
The WD1772 floppy disk controller, U102, provides the interface from the controller board to the disk drives. A block diagram of the disk control circuitry is shown in Figure 3-6.

Data and control signals from the 68000 are routed to the 1772 and to an 8-bit latch, U103. From there, signals are either fed through buffer U115 or through NAND gates to J26, the disk drive connector. Buffer U104 feeds back disk drive information to the 1772.

Four of the disk controller circuitry's signals are logically AND'ed with the Power-loss Write Protect signal, ensuring that no disk Write operations occur during power up and power down. The four NAND'ed inputs are WG and WD (Write Gate and Write Data) from the 1772 and DRIVE0 and DRIVE1 from latch U103.

Buffer U115 takes Step and Direction signals from the 1772, and Side and Motor-on signals from latch U103. Output from U103 are signals MOTON-, DIRIN-, STEP- and SIDE1-. These signals tell the disk drive to turn on, tell the drive head which direction to go and tell it which side to read.

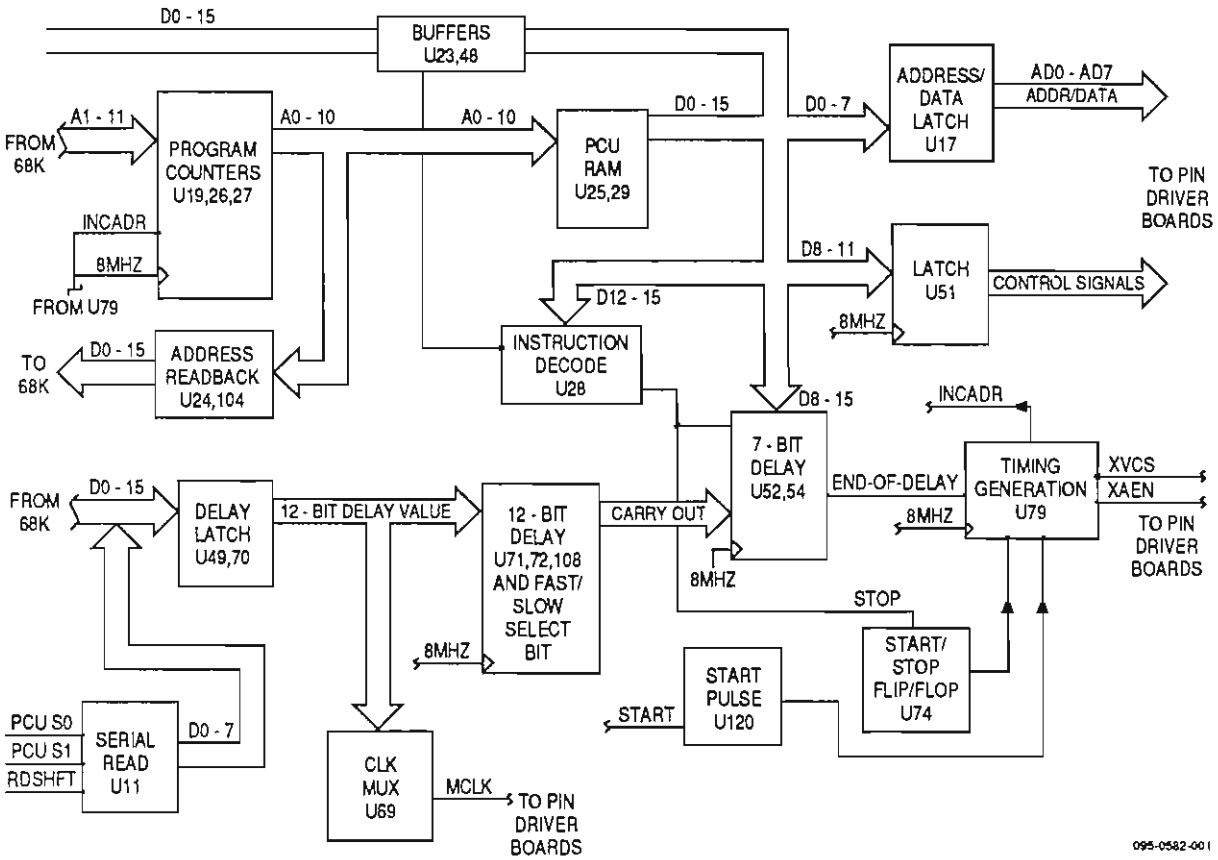
Figure 3-6
Floppy Disk Control Circuitry



Pin Control Unit (PCU)

The controller board's PCU performs all the Write operations to the pin logic ICs on the pin driver boards. The pin logic ICs, in turn, control the pin drivers. The block diagram in Figure 3-7 shows the major components of the PCU. The PCU's hardware and software is discussed in this section. The hardware discussion includes address decoding and signal routing to the pin driver boards. The software description explains some of the PCU's internal functions; how commands are interpreted by the PCU via the 32-bit instruction word. Because of the proprietary nature of the pin logic IC interface, a detailed software description is not available.

Figure 3-7
PCU Block Diagram

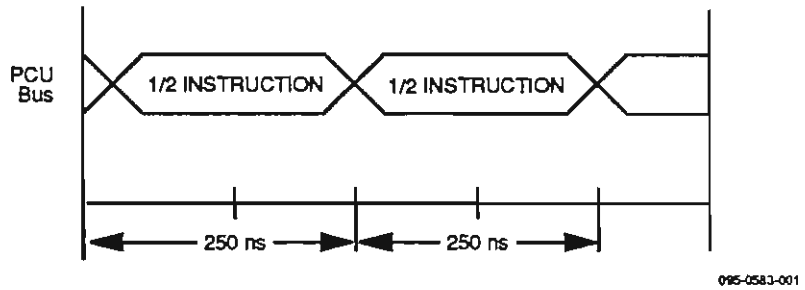


PCU RAM

The PCU's memory consists of two 2K x 8 static RAMs, U25 and U29. PCU RAM resides at addresses FF8000-FF8FFF in the microprocessor's memory map (see Figures 3- 2 and 3-3).

Commands are sent to the pin logic ICs via a 32-bit instruction word, stored in U25. 16 bits of information are sent out at a time onto the PCU bus. Figure 3-8 shows a sample timing diagram for the PCU driver bus. When the XAEN line is low (logic 0), 16 bits of address instruction information are sent out on the pin driver bus. When the XVCS line is low, the other 16 bits are sent out. Read/Write timing for the PCU RAM is available in Appendix A.

Figure 3-8
PCU Timing Diagram



Address and Data Word Instructions

Latch U17 multiplexes instructions from PCU RAM, U25. The resulting AD0-AD7 are then buffered by U9 and U15 and passed through impedance-matching resistors. These resistors—R4, 60, 62, 66 and 72—help match impedance between the transmission line and the two buffers, to minimize over- or undershoot. Buffer U9 outputs are routed to the internal pin driver bus (IPD); U15's outputs go to the FSM's pin driver bus (FPD). U21 reads back AD0-AD7 to the 68000. U4 and U5 are wire-ORed, making the IPD and FPD busses appear to the system as just one bus.

Delay Word

The 8-bit delay portion consists of one timing bit, FS, and a 7- bit delay value. The PCU uses either a 7-bit or a 19-bit delay circuit, depending on the programming time of the socketed device. If the FS bit is a logic 1, then the fast (7-bit) delay is selected; 0 selects the slow delay (the 7-bit PLUS the 12- bit delays).

The 4-bit counters used in the delay circuit are synchronously clocked from the 8 MHz PCUCLK signal. A shift register, U11, is used to read serial information via the pin driver boards, and works with serial-oriented devices. The pin driver boards' CMP line is fed into U11 through its two serial-input lines, SL and SR. The I/O decoder, U112, enables the data from the shift register, U11. This data is then put onto the 68000 bus via the RDSHFT line. Two inputs from the processor, PCUS0 and PCUS1, direct U11 to shift either left or right.

When the 68000's PCUDLY line goes high, delay and clock select information is loaded into U49 and U70. The delay consists of an 8-bit output from U49 coupled with 4 bits from U70. This 12-bit delay is then sent to U71, U72 and U108. The remaining 4-bits from U70 are used to select one of the available clock sources. U69's output, XPCLK, is used as a clock signal. This signal is used by UniSite either when programming microcontrollers or when using test vectors.

Logic circuitry takes the output from the 7- and 12-bit delays and functions as a slow or fast counter, depending on the delay required. When the delay period has cycled through, the EVOKE line is pulled low. This tells U79 to start the next instruction. U79 is a shift register, functioning as a timing generator. U79 synchronizes address/data to the pin drivers.

Waveform Board

The primary function of the waveform board is to produce several individually controlled voltages for use by the pin drivers. These voltages provide the pin drivers with power to operate, they serve as reference levels to control the pin drivers, and provide voltages which are either re-regulated and applied to the part being programmed or switched there directly.

Address / Decode

Each output on the waveform board has a specific address location, as shown in Table 3-1. Decoding is done in the following manner.

The controller board's CSWFB- line, J2 pin 6, is the main waveform board enable signal. It becomes active when valid addresses whose most-significant four hexadecimal digits equal FFB8 are issued by the controller. The two least significant digits of the six-digit hex address are decoded by the decode PAL, U24.

The decode PAL uses R/W-, CSWFB-, and A2-A8 as inputs to generate ten decode signals which form the decode bus. These signals provide enables to all memory-mapped devices on the board.

Table 3-1
Waveform Board Read/Write Addresses

Write Only Addresses	
FFB800	Cmpref
FFB804	DUTVCC
FFB808	Ref 1
FFB80C	Ref 2
FFB810	Ref 3
FFB820	V+
FFB822	V-
FFB824	VLH
FFB826	VLL
FFB828	FCHR
FFB82A	FCLR
FFB82C	FCLC
FFB82E	FCHC
FFB830	CC (Coarse Current)
FFB832	T Vslew
FFB834	Future use (always set to 0)
FFB836	Clamp
FFB83C	Output Latch (U14)
Read Only Address	
FFB8F8	Comparator Latch (U3, U4)

Data Bus

The 16-bit data bus (D0 through D15) is used to carry binary data from the controller to each of the eight DAC IC inputs and the output latch, U14. It also carries information from the comparator latches (U3 and U4) to the controller.

The data Buffers (U11 and U12) isolate the controller board's data bus from the waveform board's data bus. They are enabled by a low level on the CSWFB- signal. The direction of these buffers is controlled by the inverted R/W- signal. A low on the direction input defines the B side of the buffers as inputs and the A side as outputs; a high reverses this direction.

Power Supply System

The waveform board receives its power from four of the five system power supply outputs. These are used directly and re-regulated to lower levels for use on the waveform and pin driver boards.

Raw Voltages

The system power supply outputs go directly to the controller board. From there, the +5, +21, -15, and +48V outputs are routed to the waveform board connectors.

Re-Regulated Voltages

The +21V supply is re-regulated to +15V, +18.5V, and the 21PR voltage. This process is described below.

+15 and +18.5 Voltages

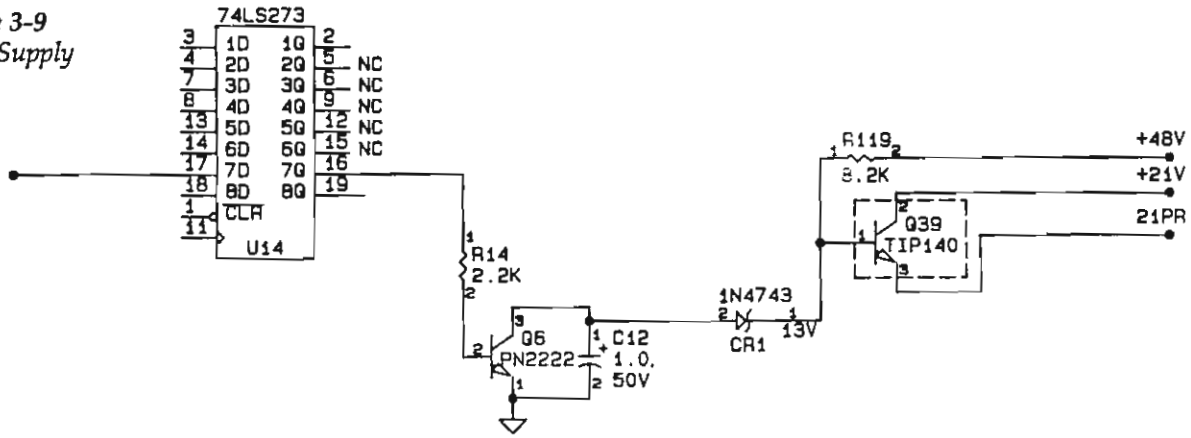
These voltages are produced by single three-terminal, series regulators, VR2 and Q5.

21PR Voltage

This voltage has two levels, depending on the state of the output latch (U14) pin 16. When this output is in the TTL Low state, Q6 is turned off. This allows R119 to pull the base of Q39 to approximately +22. This, in turn, produces a voltage of approximately +20V on the 21PR output.

By setting pin 16 of the output latch to a TTL high, Q6 is turned on. When this occurs, the anode of the zener diode (CR1) is pulled to ground, which sets the base of Q39 to approximately 13V. Since Q39 is a darlington transistor, the emitter will then be held at about two volts less than its base; about +11V.

Figure 3-9
21PR Supply



The +48V supply is re-regulated down to +40V using a discrete regulator circuit, as described below.

+40 Volts

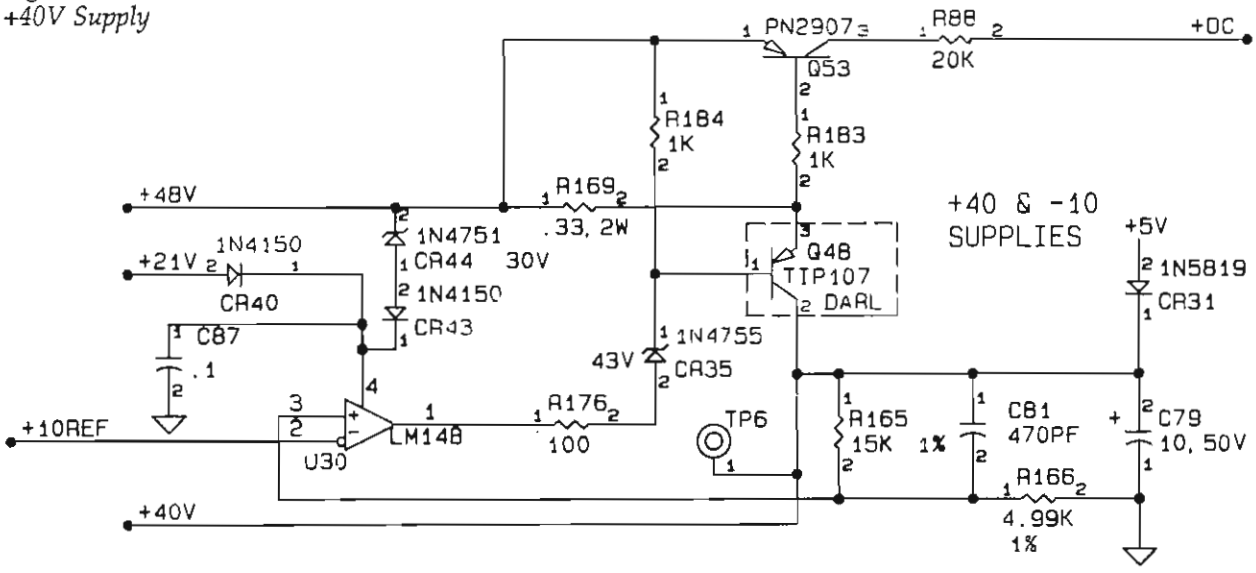
This is a precision voltage source (±1.5%). The collector of the darlington power transistor (Q48) is held at +40V in the following manner. The collector voltage of Q48 (+40V output) is divided by four, using the voltage divider network formed by R165 and R166. When the +40V from the output is present at this divider, the resulting +10V level is produced and applied to the positive input of op amp (U30 pin 3).

The negative input of this op amp (pin 2) is held at +10V by the precision reference. The op amp output (pin 1) voltage adjusts the anode of the 43V zener diode (CR35) within the +1V to -3V region. The cathode of CR35, in turn, adjusts the base of Q48 to a voltage which holds the collector of Q48 to the desired +40V level.

An overcurrent trip circuit is incorporated at the emitter of Q48, which includes R88, R183, R169, and Q53. The action of this circuitry is typical of the overcurrent circuitry described at the end of this section.

R184 is used to provide current to CR35. CR40, CR43, and CR44 ensure that the op amp is supplied with enough operating voltage in the event that +21V is not present. This condition may occur upon system power up or power down. CR31 ensures that the +40V supply goes no lower than about +4V when an overcurrent condition turns the +40V supply off. This is done to prevent damage to the semi-custom linear IC on the pin driver boards.

Figure 3-10
+40V Supply



The -15V supply is re-regulated down to -5 and -10V, as described below.

-5 Volts

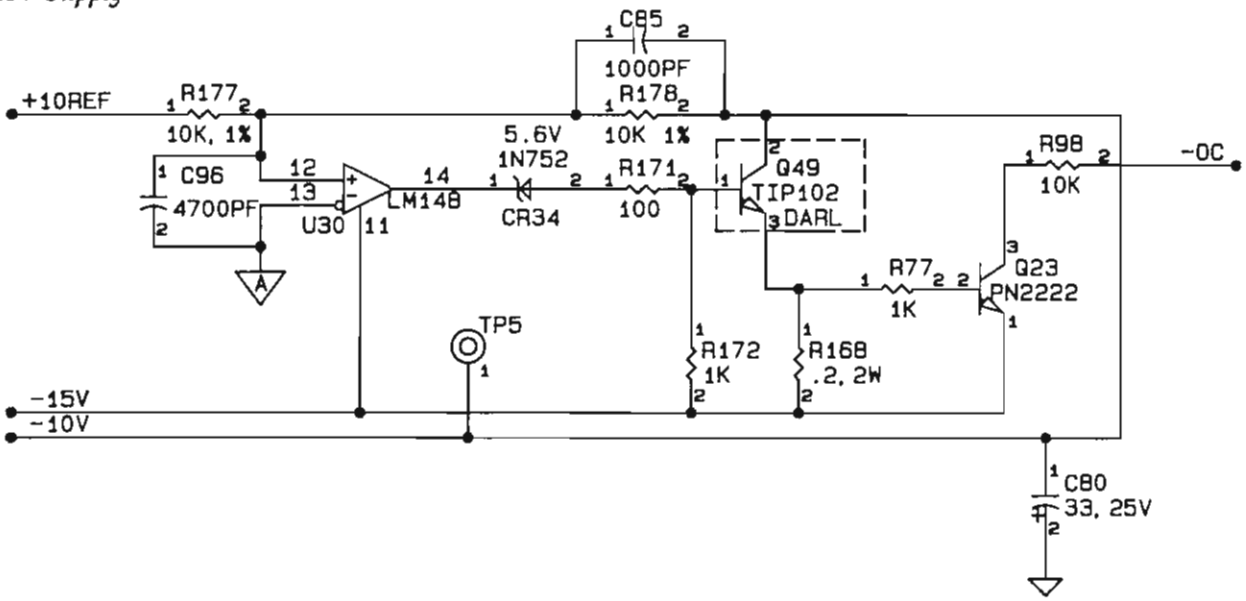
This voltage is produced by a single three-terminal series regulator IC, VR3.

-10 Volts

This voltage (±2%) is developed at the collector of the darlington power transistor (Q49) in the following manner.

The collector voltage of Q49 (-10V output) is applied to a voltage-divider network, composed of 10KΩ resistors (R178, 177). The other end is connected to the precision +10V reference. The resulting voltage of this divider is a halfway point between the end points; nominally 0V. This level is then applied to the positive input of the op amp (U30 pin 12). The negative input of the op amp (pin 13) is tied to analog ground, which is a sense of the actual programming site's ground. The cathode of CR34 is driven by the output of the op amp (pin 14). The anode of CR34 then adjusts the voltage at the base of Q49 such that a regulated -10V is developed at the collector

Figure 3-11
-10V Supply



Grounding System

It is important to note the difference between the two ground nodes used on the waveform board: PGND and AGND. PGND is the power ground, serving as the return current path for all of the analog circuitry on the waveform board as well as the rest of the system. AGND is a sense line. In normal operation, this line is connected to PGND by the Programming Module, installed on the front of UniSite. In the event that this connection is not made, which may be the case when servicing the system, a 100Ω resistor, R49, will make this connection. This resistor is not small enough to allow the system to calibrate without either an FSM or a PSM installed.

Waveform Board Outputs

This section describes in detail the purpose, the output range and the circuit operation of each individual waveform board voltage source.

Reference 1, 2, and 3

Purpose: These voltages are used as input to the pin driver's voltage source circuit.

Output Range: The voltage level of all three of these outputs swings between +5 and -10V.

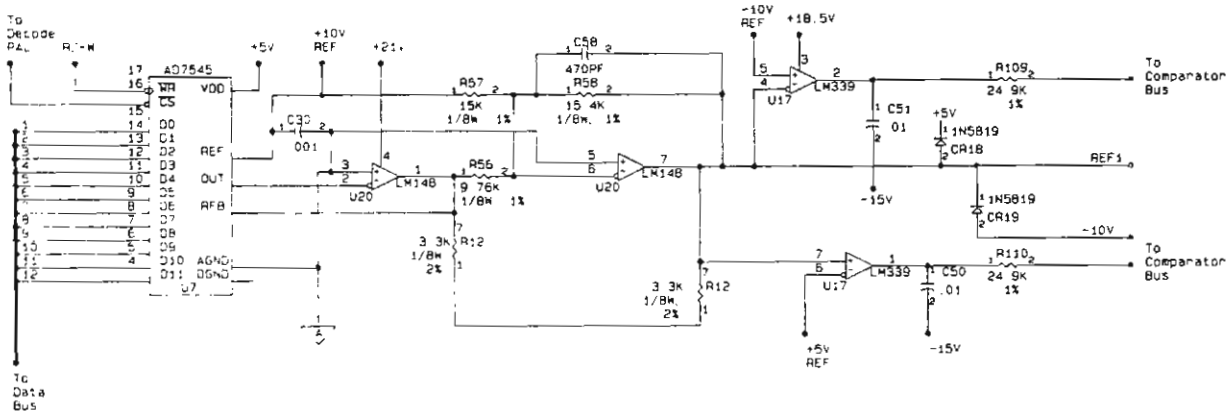
Circuit Operation: Because these three supplies vary so little from each other, a description of the Reference 1 supply will be given and will apply to the operation of all three.

The output of DAC IC U7 (Figure 3-12) is converted to a voltage by the LM148 op amp, U20. This voltage is applied to R56. Since the + input of U20 (pin 5) is connected to ground, the op amp will adjust its output to hold the – input (pin 6) at the same ground potential. This is done in the following manner.

The – input (pin 6) of the op amp is connected by R56, R57, and R58 to three different voltage levels. R57 always pulls the input to the +10V level, while R56 compensates by always pulling to the negative level set by the DAC output. It is these two resistors that allow (by varying the DAC voltage) the – input voltage to be set at either a positive or negative level. R58 supplies the feedback current from the op amp output required to hold the op amp inputs at the same potential. When the DAC voltage rises, the - input also rises. As a result, the op amp output lowers its voltage, allowing R58 to pull the input back down to ground potential. C58, which is placed across R58, stabilizes the op amp, eliminating oscillation.

Two voltage comparators of U17 are connected to the op amp output. They are used to indicate when the output crosses either the +10V level or the -5V level.

Figure 3-12
Ref 1,2, and 3



Comparator Reference

Purpose: The output of this circuit is used exclusively by the waveform board's comparator inputs.

Output Range: -10V to +15V.

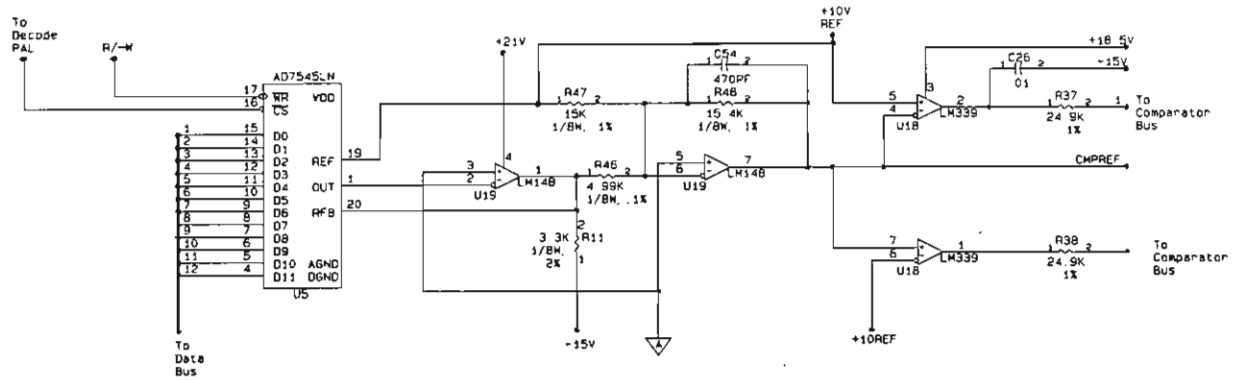
Circuit Operation: The output of DAC U5 (see Figure 3-13) is converted to a voltage by the LM148 op amp, U19 at pin 1. This voltage is applied to R46. Since the + input of U19, pin 3, is connected to ground, the op amp will adjust its output to hold the – input, pin 2, at the same (ground) potential. This is done in the following manner:

The – input (pin 6) of the op amp is connected by R46, R47, and R48 to three different voltage levels. R47 always pulls the input to the positive 10V level while R46 compensates by always pulling to the negative level, set by the DAC output. By varying the DAC voltage, these two resistors allow the – input voltage to be set at either a positive or negative level. R48 supplies the feedback current, from the op amp output, required to hold the op amp inputs at the same potential.

When the DAC voltage rises, the – input also tries to rise. As a result, the op amp output lowers its voltage, allowing R48 to pull the input back down to ground potential. C54, which is placed across R48, stabilizes the op amp to eliminate oscillation.

Two voltage comparators of U18, are connected to the op amp output. They are used to indicate when the output crosses either the +10V level or the -10V level.

Figure 3-13
Comparator Reference



Vcc

Purpose: This circuit supplies voltage directly to the Vcc pin of the programmable device, when the appropriate Vcc relay is closed on the programming module.

Output range: No load: -10V to +20V. Full load: (2.5 amps) -6V to +15V.

Circuit operation: The output of DAC U6 (see Figure 3-14) is converted to a voltage by the LM148 op amp, U19, at pin 14. This voltage is applied to R148. The output voltage is developed by adjusting the voltage drop across the D44H11 and D45H11 output transistors, Q43 and Q44. The op amp (U29) output voltage applied to R154, establishes the op amp output current from either the positive or negative supply. It is this current, when directed through R152 or R151, that controls the Vcc voltage level.

Since the op amp's + supply current must flow through the 160Ω resistor R152, (assuming Q32 is off) the resistor will develop the voltage required to turn Q35 on. This causes the collector of D44H11 to pull up to a positive voltage.

The reverse in operation occurs when the op amp's output voltage is a negative value. The op amp output current flows through R151 (assuming Q29 is off), which develops the voltage required to drive Q34. This causes the collector of Q43 to pull to a negative voltage.

The change of Vcc output voltage is sensed by the VCC SENSE signal. The VCC SENSE signal is normally connected to the Vcc output at the programming site on the programming module, but if the module is not installed, the VCC SENSE signal is connected to the Vcc output via the 100Ω resistor R145.

When the DAC voltage tries to change the op amp's – input, the resultant change in Vcc and VCC SENSE counteracts this change by applying an opposing voltage to the – input through R149. This satisfies the op amp's requirement to keep both + and – inputs at the same voltage level, while changing the output voltage to its new level.

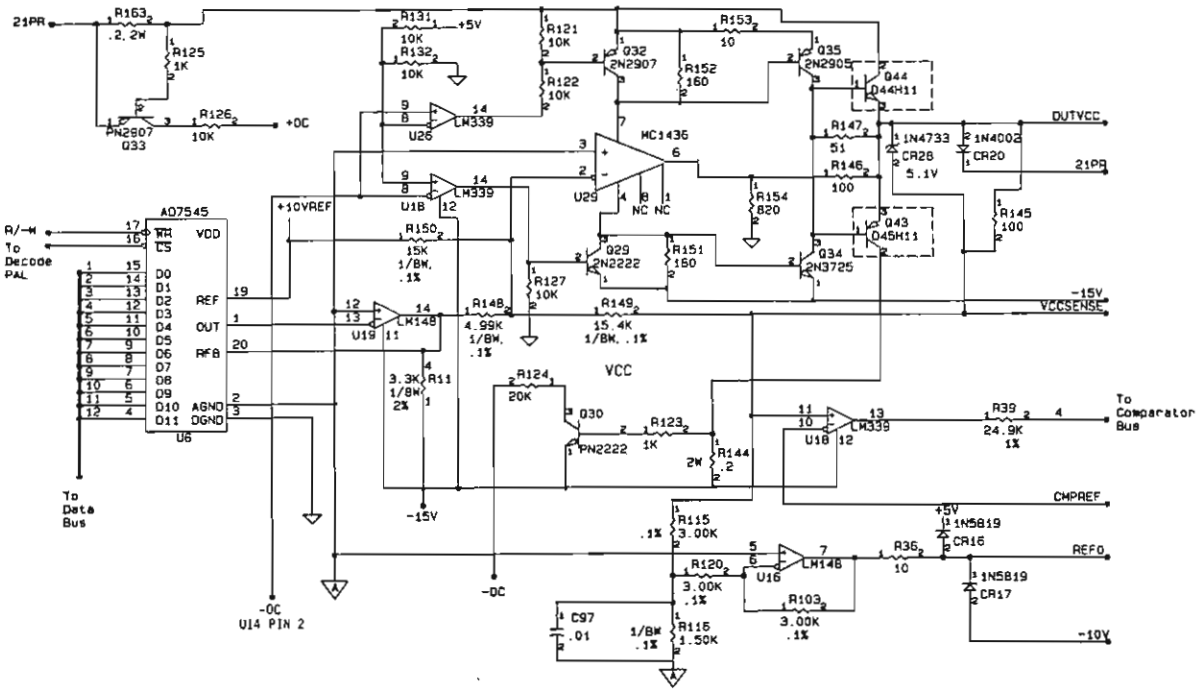
Operation of the Vcc supply depends both Q32 and Q29 being off. This is not the case when the over-current circuit has tripped. When this happens, the LM339 inputs, U18 pin 8 and U26 pin 9 go low. Since the other inputs on these comparator are connected to a 2.5V level, divided between +5V and ground by R131 and 132, the output of U26 lowers and the output of U18 rises from the -15V rail to ground. This turns on both Q32 and Q29, shorting out R151 and R152, which shuts off the entire Vcc supply.

Reference 0

Purpose: The pin driver's circuitry requires that one of the Reference outputs (0 through 3), tracks the voltage level on the Vcc supply output. Like the Reference 1, 2, and 3 sources, Reference 0 is another input to the pin driver board's voltage source circuit. The difference is that this reference voltage tracks the Vcc supply output, and is not independently adjustable.

Output range: -3.75 V to +1.5 V. **Circuit operation:** The Vcc supply output voltage (see Figure 3-14) is divided down to 1/3 of its value by R115 and R116. This voltage is applied to the inverting, unity-gain amplifier circuit, R120, R103, and pin 6 of U16. This supplies the pin driver with a reference which is 1/3 the voltage of Vcc, and opposite in polarity. CR16 and CR17 are clamp diodes.

Figure 3-14
Vcc and Ref 0 Supplies



V+

Purpose: This output is the positive power supply to the pin drivers' voltage source, located on the pin driver board.

Output range: Full load: 0V to +37V No load: 0V to +40V

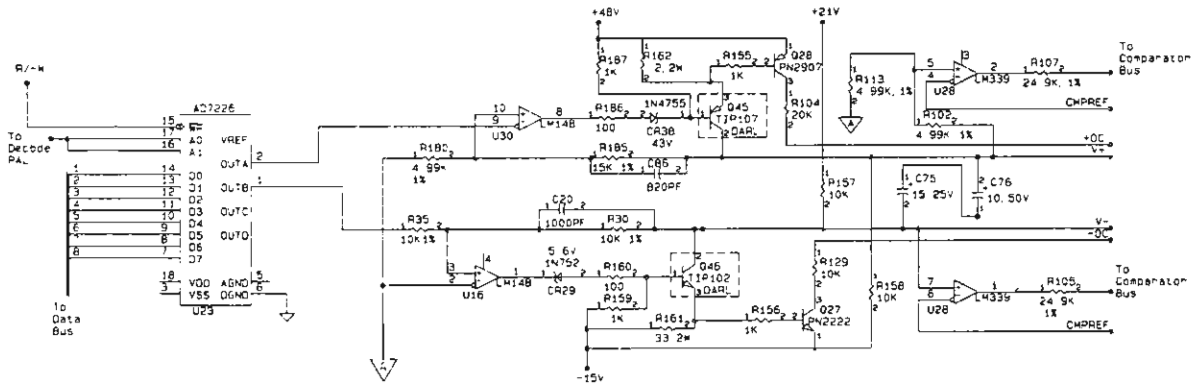
Circuit operation: DAC U23 pin 2 outputs its voltage level to the – input of op amp U30, pin 9 (see Figure 3-15). The voltage at the + input, pin 10, is set to 1/4 of the V+ output voltage by the resistor divider network, R180 and R185.

To turn the output transistor on, its base voltage need only drop to 0.6V below the +48 supply voltage. Since CR38 is a 47V zener diode, the output transistor will turn on when the op amp output voltage is at, or below, about 0V.

As the DAC voltage rises, the op amp output voltage will drop, which raises the V+ output voltage (collector of Q45). The V+ voltage is fed back to the + input of the op amp, to balance its input voltages.

The +OC signal goes high when too much V+ output current is sensed by R162 and the overcurrent transistor, Q28, turns on. The output voltage of this supply is sensed by the + input of U28 pin 5. It is compared against the COMPREF signal. The output connects to the comparator bus.

Figure 3-15
V+ and V- Supplies



V-

Purpose: This output is the negative power supply to the pin driver voltage source, located on the pin driver board.

Output range: -10V to 0V

Circuit operation: The – input of the op amp, U16 pin 2, is connected to ground (see Figure 3-15). As the DAC voltage changes, the V+ output voltage will change to a level that is equal and of opposite polarity, to maintain the + input (pin 3) at 0V.

To turn the output transistor on, its base voltage need only rise to 0.6V above the -15 supply voltage. Since CR29 is a 5.6V zener diode, the output transistor will turn on when the op amp output voltage is at, or above, about -9V.

As the DAC voltage rises, the op amp output voltage will rise. This causes the V- output voltage (collector of Q46) to drop. The V- voltage is fed back to the + input of the op amp to balance its input voltages.

The -OC signal goes low when too much V- output current is sensed by R161 and the overcurrent transistor, Q27, turns on. The output voltage of this supply is sensed by the + input of U28 pin 7. It is compared against the COMREF signal. The output connects to the comparator bus. A 15 µF capacitor is connected to the output for stability and filtering.

VLH

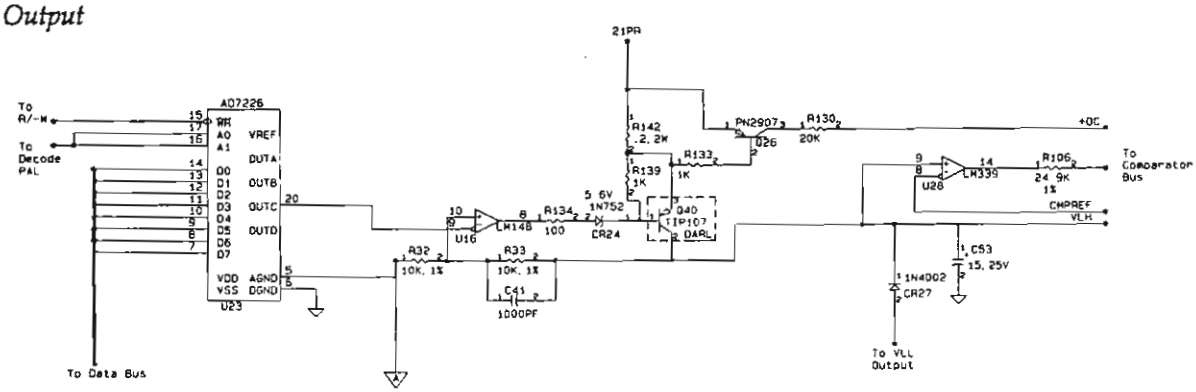
Purpose: This supply provides power to the logic driver circuit on the pin driver boards.

Output range: Full load: 0 to +20V No load : 0 to +17.5V

Circuit operation: The DAC output (see Figure 3-16) is connected to the – input of the LM148 op amp, U16 pin 9. When this voltage is increased, the op amp output decreases. This raises the VLH output (collector of Q40) to a higher voltage. This voltage is sensed by the + input of the op amp through R33, to balance the op amp input voltages. The +OC signal goes high when too much VLH output current is sensed by R142 and the overcurrent transistor, Q26 turns on.

The output voltage of this supply is sensed by the + input of the LM339, U28 pin 9. It is then compared against the COMREF signal. The output connects to the comparator bus. A 15 µF capacitor is connected to the output for stability and filtering.

Figure 3-16
VLH Output



VLL

Purpose: The VLL supply provides the negative voltage required by the logic driver on the pin driver boards.

Range: No load: 0 to -10V Full load: 0 to -8V

Circuit operation: The DAC's output is connected to the 60.4KΩ resistor, R31. The output of the VLL supply is connected to the 60.4KΩ resistor, R34. R34 and R31 are connected together at the – input of op amp U16, pin 13. When the DAC's output rises, the op amp output voltage lowers to a level that is two base-emitter voltage drops—that of the Q41 darlington transistor—away from the final output voltage.

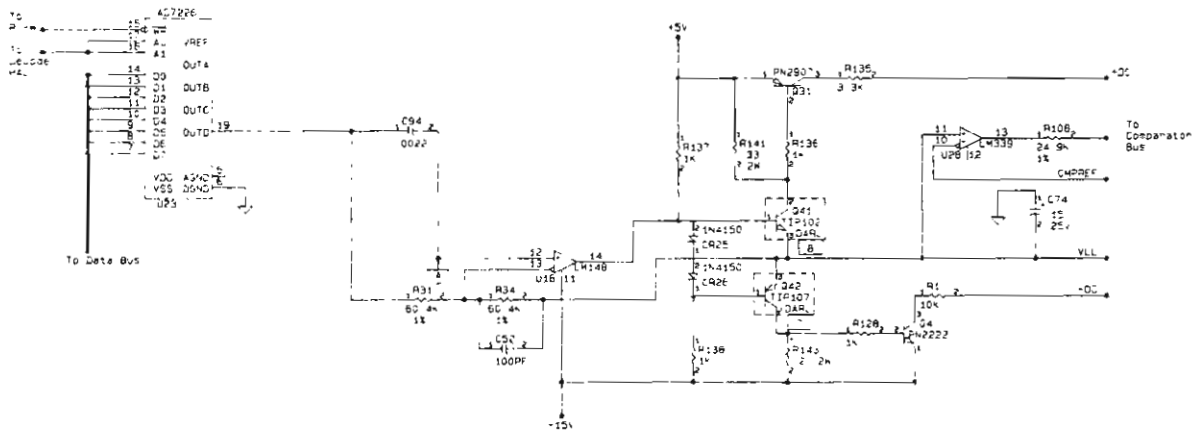
While Q41 is supplied by +5V, the VLL output never goes above 0V. The reason for its presence in the circuit is to allow the VLL supply to source as well as sink current at a negative voltage, a condition required by the pin driver boards.

The reason for the two series diodes is to compensate for one of the two base-emitter voltage drops in each of the darlington transistors, Q41 and Q42. This way, the op amp output does not have to swing as far to turn on either of the two output transistors.

The -OC signal goes negative when too much VLL output current is sensed by R143 and the overcurrent transistor, Q4, turns on. The +OC signal goes positive when too much VLL output current is sensed by R141 and the overcurrent transistor, Q31, turns on. R137 and R138 provide current for the two series diodes to operate.

The output of the VLL supply is compared to the COMPREF signal by pins 11 and 10 of U28. The output of this comparator goes to the comparator bus. C74 is used for stabilization and filtering of the VLL output voltage.

Figure 3-17
VLL Output



FCHR

Purpose: This circuit provides the fine current source on the pin driver board with a reference voltage. This reference voltage sets the current level of the fine current source.

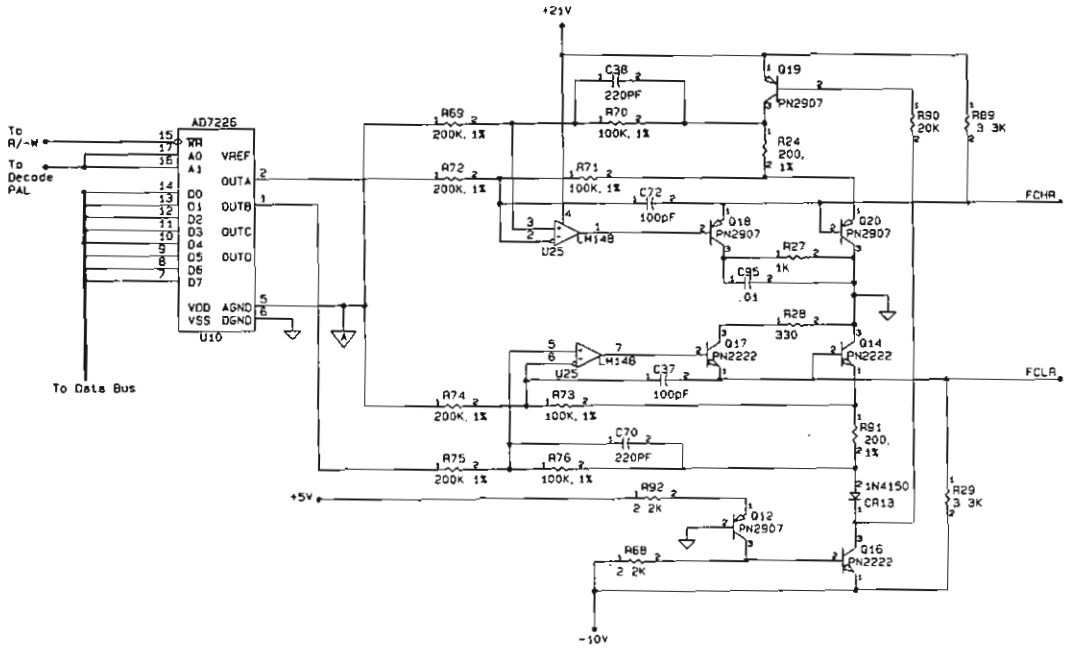
Range: +14.3 to +19.3V

Circuit operation: This circuit (see Figure 3-18) runs a desired current through a 200Ω resistor (R24 and R91 in this case), measures the resultant voltage drop across that resistor and delivers that voltage to the pin driver board. The circuitry functions as follows:

Q19 is always on, so its effects can be ignored. The DAC's output voltage is applied to the 200KΩ resistor, R72 while the FCHR output is connected to the 100KΩ resistor, R71. R72 and R71 are connected together at pin 2 of the LM148 op amp. The other input of the LM148 is connected to a voltage divider set up by R70 and R69 between +21V and ground. This holds the inputs of the op amp at about +14V.

When the DAC voltage rises, Q18's emitter voltage drops. The emitter voltage of Q20 is then one base-emitter voltage drop below the FCLR voltage. The emitter voltage is also applied to the 200Ω resistor, R24.

Figure 3-18
FCHR and FCLR Supplies



FCLR

Purpose: To provide the fine current source on the pin driver board with a reference voltage. This reference voltage sets the current level of the fine current source.

Range: -3.6V to -8.6V

Circuit operation: The DAC's output (see Figure 3-19) is applied to the + input of op amp U25 through R75. The output voltage is sensed on the – input of the op amp through R73.

When the DAC's output voltage decreases, the op amp's output also decreases. This voltage appears on the emitter of Q17 (minus a base-emitter voltage drop) and is the FCLR output. This decreases the voltage across the 200Ω resistor R91 through the base-emitter of Q14. The lower output voltage is fed back the – input of the op amp through R73, balancing both inputs of the op amp. Q12 and Q16 remain on all the time.

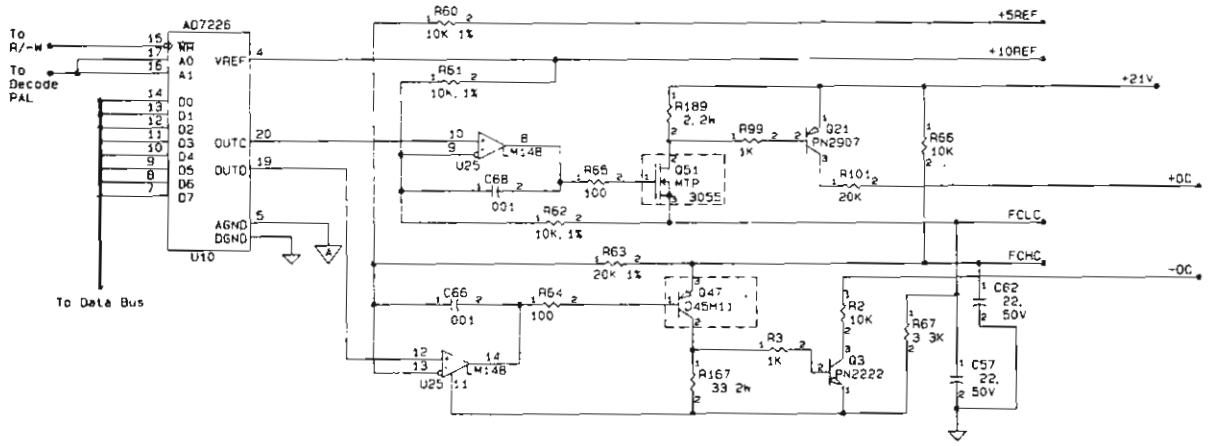
FCLC

Purpose: To set a clamp voltage on the pin driver's output when the pin driver's fine current source is sinking current.

Range: No load: -10 to +10V Full load: -8.8 to +10V

Circuit operation: The – input of the op amp, U25 pin 9 (see Figure 3-19), is set to a voltage that is halfway between the output voltage and the +10V ref signal. The + input is set by the DAC's output. The output of the op amp drives the gate of Q51. The output voltage is fed back to the – input of the op amp through R62 to balance the op amp inputs. When overcurrent is sensed on R189, Q21 is turned on, pulling over-current.

Figure 3-19
Fine Current Clamps



FCHC

Purpose: To set a clamp voltage on the pin driver's output when the pin driver's fine current source is sourcing current.

Range: No load: -7.3V to +16.3V Full load: -5V to +20V

Circuit operation: The – input voltage of the op amp (see Figure 3-20) is set between the output of the FCHC supply and the +5V ref signal. The + input voltage is set by the DAC's output. The op amp output drives the base of Q47 such that its emitter becomes the output. The output voltage is fed back to the – input of the op amp through R63 to balance the op amp inputs. When overcurrent is sensed on R167, Q3 is turned on, pulling over-current.

Overcurrent Integrator

Purpose: To accept overcurrent signals from the waveform board circuits and the pin driver board's OCTRIP signal.

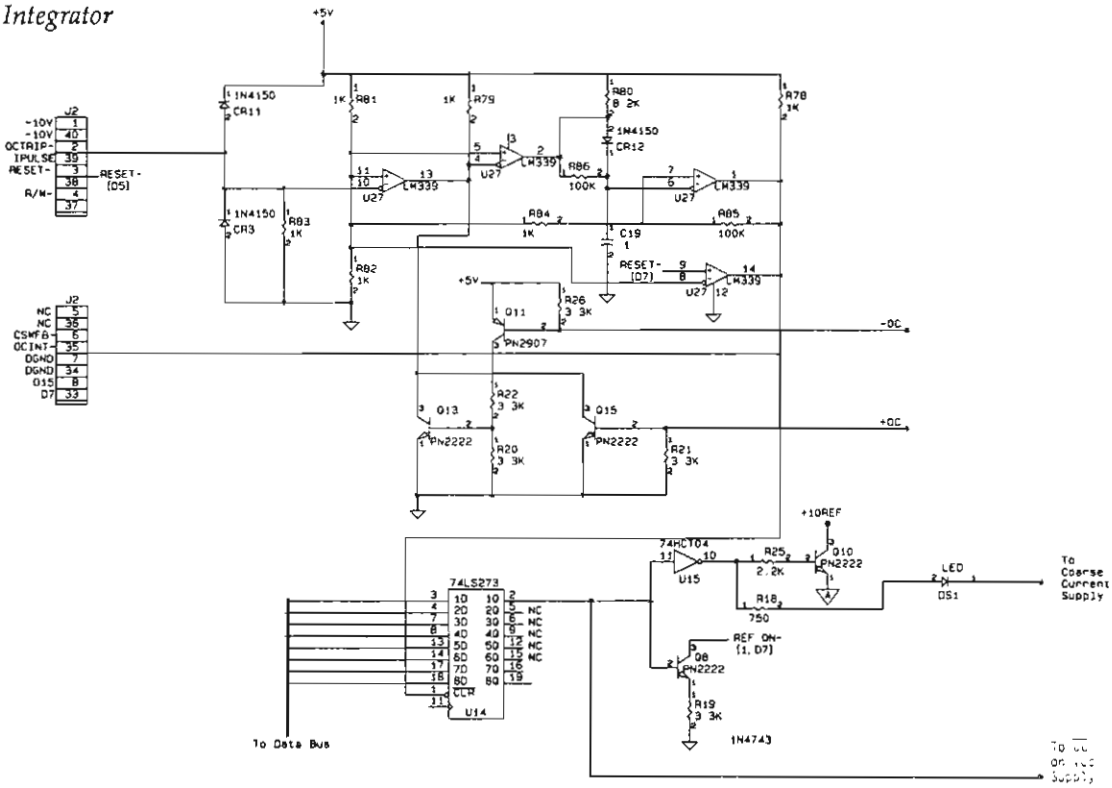
Circuit operation: When the – input of the comparator, U27 pin 4, lowers to less than its + input voltage (see Figure 3-20), the comparator output goes high and C19 begins to charge to a positive voltage through R80 and CR12. When the voltage across C19 exceeds 2.5V, the output of the next comparator, U27 pin 1, goes low. This output pulls the CLEAR input of the auxiliary latch, U14, low and sets all its outputs to a low. When the output of U27 (pin 2) goes low, the charge across C19 is drained off through R86. In this way, the overcurrent integrator will not respond to transient overcurrent inputs—those caused by slewing of supply output voltages—but will respond to any long-duration overcurrent inputs (those that are more than one millisecond).

The – input of U27, pin 4, can be pulled low in either one of three ways: the OCTRIP (active high) signal can be raised, Q15 can be turned on, or Q13 can be turned on.

The OCTRIP signal comes from the pin driver boards when their overcurrent circuit activates. Q13 is turned on when any of the -OC signals goes low. Q15 is turned on when any of the +OC signals goes high.

R81 and R82 form a voltage divider to produce a 2.5V reference that U27's comparators use. R83 is a pull-down resistor for the input of U27, pin 10. CR3 and CR11 clamp the OCTRIP input to ground and +5V. The 100KΩ and 1KΩ resistors on pin 7 of U27 provide the output of U27, pin 1, with 25mV of hysteresis for stabilization.

Figure 3-20
Overcurrent Integrator



Coarse current (CC)

Purpose: This supply provides the pin driver output with a constant current which is adjustable down to the 1mA level. This supply will only source current.

Range: Voltage: 0 to 33V Current: 0 to 250 mA

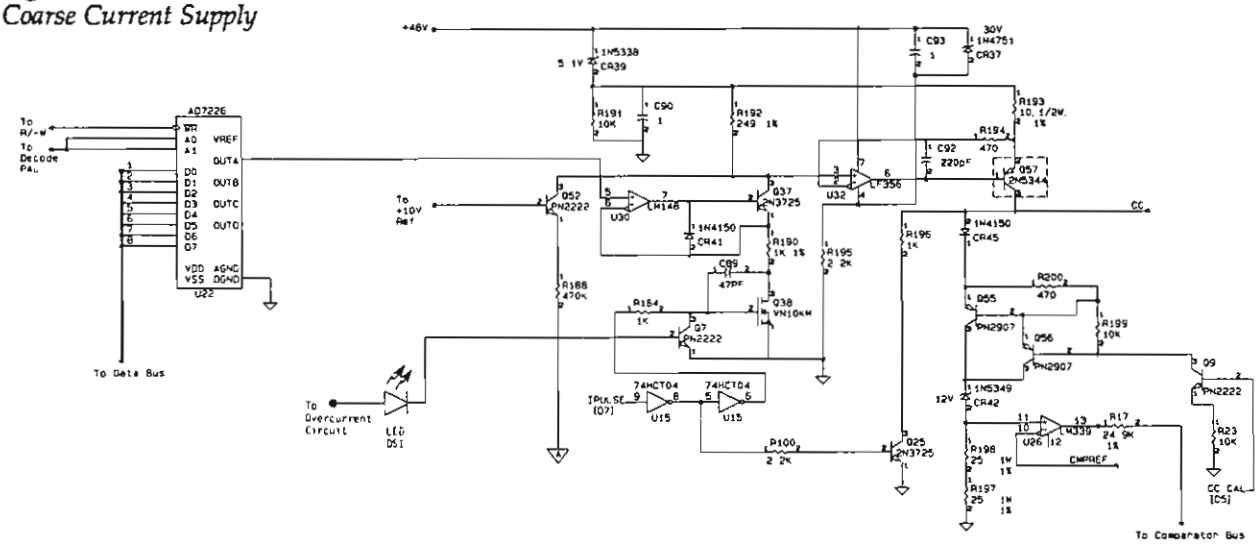
Circuit operation: The goal of this circuit is to set up a regulated voltage across the 10Ω resistor, R193. In doing so, a constant current will be established. The DAC's output voltage is applied to the + input of U30, pin 5. The op amp of U30 pins 5, 6, and 7 is set up in a unity gain configuration (its input voltage equals its output voltage). The output of this op amp is tied directly to the base of Q37. The emitter voltage of Q37 is applied to a 1KΩ resistor, R190.

When the FET, Q38 is turned on, a constant current is established through it. This current comes from the +48V supply, through R192. Since the op amp of U32 pins 2, 3, and 6 is also set up as unity gain, the voltage developed across R192 will appear across R193 and thus establish the final output current.

For this to happen, two conditions must be satisfied: the overcurrent condition must be cleared, and the IPULSE signal must be in a high state. Clearing the overcurrent condition causes Q7 to turn off, allowing the FET, Q38, to turn on. Pulling overcurrent will also lower the +10ref signal to 0V. This action turns off Q52, which shuts off the coarse current completely. Having the IPULSE signal in the high state turns on Q38, which enables the entire circuit.

CR 39 and R191 work together to drop the +48V supply level to limits which are acceptable to the output transistor, Q57. CR37 and R195 work together to drop the +48V supply level to limits which are acceptable to the op amp, U32. The output of the coarse current supply is connected to the coarse current calibration circuit. When the CC CAL signal is taken high, Q9, Q56 and Q55 all turn on. This directs current from the coarse current supply through CR45, CR42 and a fixed load of 50Ws. The 50W load is made up of R198 and R197. The voltage developed across these resistors is input to the comparator, U26 pin 11. The other input to this comparator is connected to the CMPREF signal. By varying the CMPREF level, a current measurement can be made. The output of the comparator is connected to the comparator bus.

Figure 3-21
Coarse Current Supply



Slew Rate reference (Vslew)

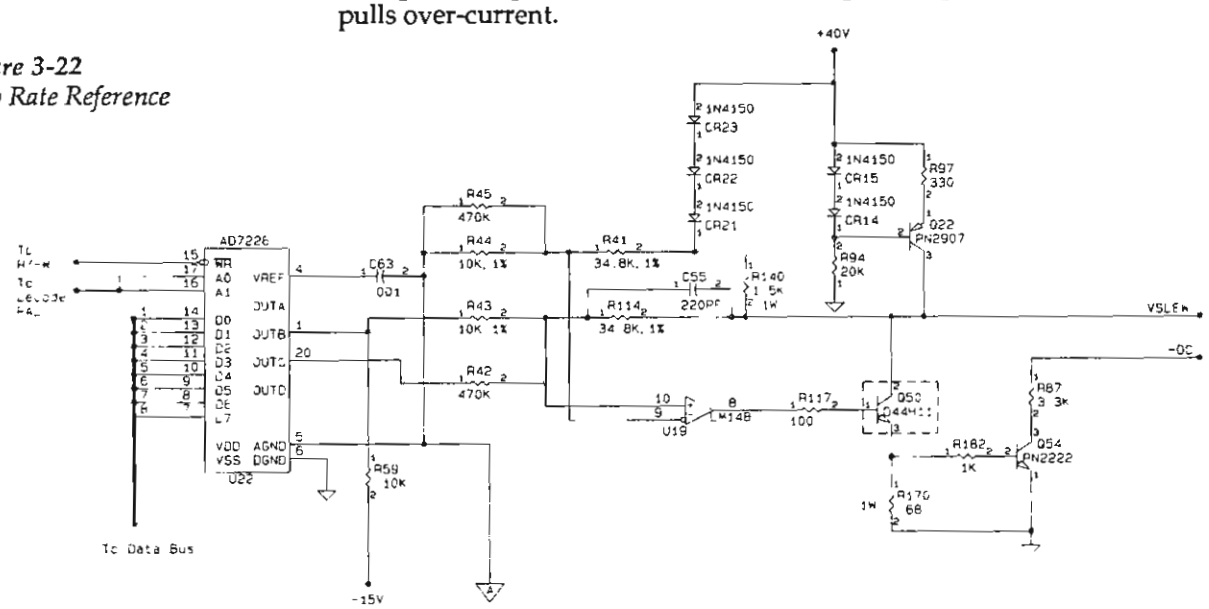
Purpose: This supply provides the custom linear IC, mounted on the pin driver boards, with a reference voltage which it uses to determine the slew rate of the pin driver voltage source.

Range: +3.4 to +38.4V **Circuit operation:** The voltage level of the + input of the op amp, U19 pin 10, is set at a point between the DAC's output voltage and the Vslew supply output voltage by R43 and R114. The voltage of the – input on the op amp is set at a point between the voltage at the cathode of CR21 and ground.

Since the – input is held at a constant voltage, the output of the op amp adjusts the collector of Q50 to a voltage which feeds back and keeps both inputs equal. There are two DAC outputs associated with this supply. One is applied to the op amp input through a 10KΩ resistor and the other is applied the 470KΩ resistor R42. The DAC output associated with the 10KΩ resistor makes large adjustmentts to the output voltage, while changes on the DAC's output associated with the 10KΩ resistor make fine adjustments.

The three diodes CR21, CR22, and CR23, have no function on the waveform board itself, but are required by the pin driver board's linear IC. R140 provides a current source for the output transistor. CR14 and CR15 in conjunction with R94, R97 and Q22 form a 2 mA current source which can pull the output voltage up in addition to the current supplied by R140. The output current is monitored by R170. When the voltage developed across this resistor is high enough, Q54 turns on and pulls over-current.

Figure 3-22
Slew Rate Reference



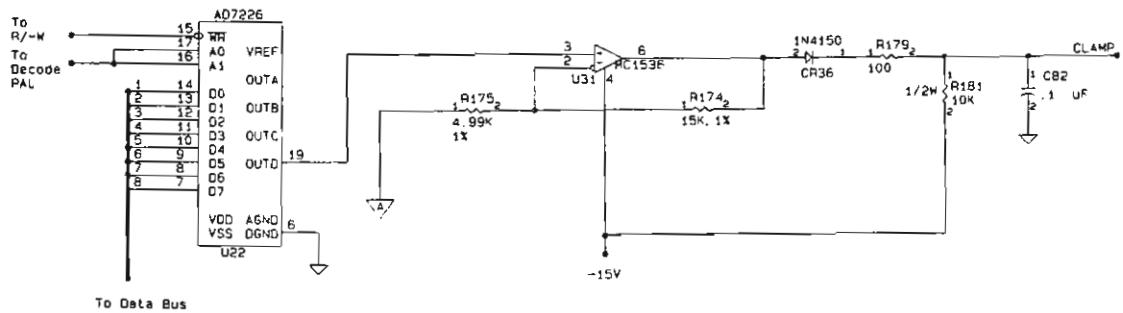
Clamp

Purpose: The output of this supply provides a capacitor, charged to a predetermined voltage level, to the device socket pins. The device socket pins are connected to this capacitor through a diode. If the voltage on Clamp is 10V and the voltage on the pin tries to momentarily rise to a higher voltage than 10V, it will be clamped by the diode on the device socket pin, eliminating overshoot that may occur in any operation done on a device in the socket.

Range: 0 to +40V

Circuit operation: The + input of the op amp, U31 pin 3, is set to a voltage by the DAC's output while the – input, pin 2, is set to a level between the output voltage and ground. The output of the op amp adjusts to a voltage which will keep both inputs at the same level. The 10KΩ resistor to ground provides a current path for current that comes out of the op amp and doesn't go to charge C82. The op amp current is limited by R179, the 100Ω resistor.

Figure 3-23
Clamp



Basic Operation of the Waveform Board's Outputs

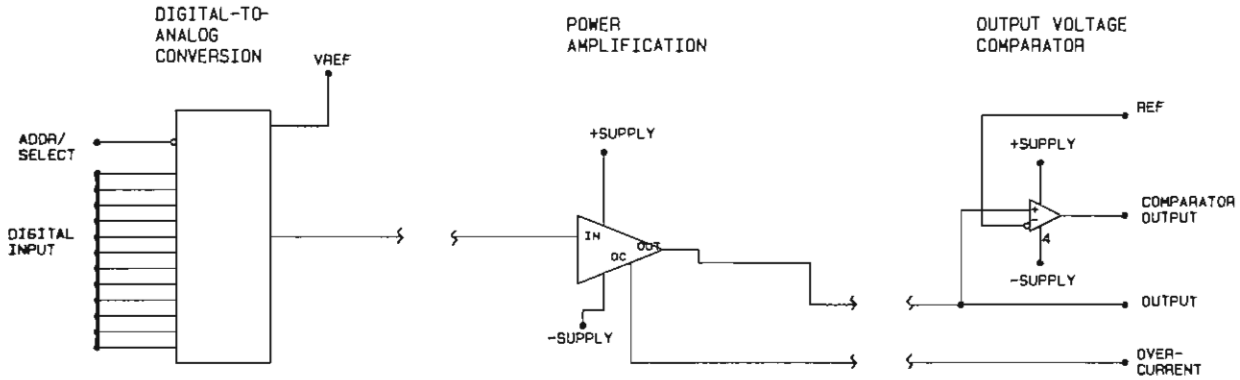
Note: This section describes the basic operation of the waveform board voltage outputs, and is not intended for personnel already experienced in working with analog circuitry.

Following are the three basic elements of a typical waveform board's voltage source. These three elements are found in several (but not all) of the individual waveform board outputs.

- DAC IC (Digital-to-Analog Convertor)
- Power amplifier
- Output comparator

The DAC IC converts a binary value, placed at its inputs, to an analog voltage associated with that binary value. This action is initiated when the chip select (CS) or address lines (A0, A1) are active, and the Write (WR) signal makes the proper transition.

Figure 3-24
Basic Elements of a Waveform Board Output



The waveform board uses two types of DAC ICs: the 7545 and the 7226. The 7545 uses twelve binary digits as its digital input, and contains only one voltage output. The 7226 uses eight binary digits as input, and outputs four separate analog voltages. The 7545 is selected by a chip select (CS) signal, and is written to with a positive transition on the write (WR) signal. Since the 7226 contains four DAC's, each DAC is selected by an appropriate address on the A0 and A1 inputs. The 7226 is written to with a negative transition on the write input.

When troubleshooting the DAC ICs, it is important to understand that the 7545 DAC outputs an analog current, which is difficult to measure. This current is converted to an analog voltage by the op amp connected to its output. Usually the best way to verify the operation of the DAC is to measure the output of the output op amp. The 7226 DAC, however, contains its own op amps, so its output is on an analog voltage that is easier to measure.

The power amplifier is composed of either an op amp driving a power transistor or, where less current is required, an op amp alone. The function of the op amp is to maintain regulation of each waveform board output.

All the op amps on UniSite's waveform board are configured to operate as shown in Figures 3-25 or 3-26.

Figure 3-25
An Op Amp Power Amplifier

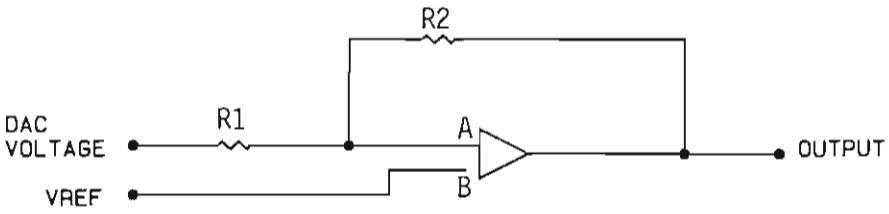
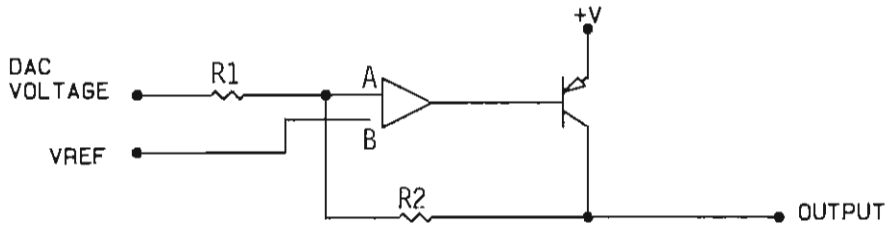


Figure 3-26
A Power Amplifier that Uses an Output Transistor



The op amp functions in the following way: when the + input voltage is greater than the – input voltage, the output voltage will approach the + supply voltage. Conversely, when the + input voltage is less than the – input voltage, the output voltage approaches the – supply voltage. Keep this in mind as you look at the operation of the circuit shown in Figure 3-25.

R1 and R2 form a resistor divider network, with the DAC output voltage applied to one end, and the op amp output voltage to the other. The center of the divider network is connected to input A of the op amp. Op amp input B is connected to a fixed reference voltage. It is the function of the op amp to adjust its output voltage, such that the resistor divider holds input A at the same voltage as the reference voltage on input B. When the DAC voltage changes, the op amp output voltage changes correspondingly to maintain the same voltage on both op amp inputs.

If the two op amp inputs are not at the same voltage level, a problem is indicated. The circuit shown in Figure 3-25 works the same way as that of Figure 3-26; the only difference is the output transistor, which is placed between the op amp output and the feedback resistor R2. The transistor provides far more current to the output than the op amp could supply on its own.

As shown in Figure 3-25, when the DAC voltage of Figure 3-26 changes, current through R1 tries to change the voltage on input A of the op amp. The op amp responds by using its output to adjust the collector voltage of the output transistor. When the collector voltage changes, current through R2 is fed back to the A input of the op amp. This readjusts the voltage at the A input such that it equals the voltage of the B input again. In this fashion, the output voltage will always adjust to a level which offsets the DAC voltage level placed at R1, the input of the power amplifier circuit. This output voltage is used by the rest of the programming electronics.

The output comparator is either an LM339 or an LM148 IC. One of its inputs is connected to a reference voltage and the other to the output of the power amplifier. The output is connected via the Comparator Bus to the input of the Comparator Latch, U3 and U4. The reference voltage is either fixed, as in the case of the +5REF, +10REF, and the -10REF, or is variable, as in the case of the COMPREF signal. The comparator provides a way for the system controller (located on the controller board) to monitor the output voltage level of each voltage source. By varying COMPREF until the comparator output toggles, the voltage source output level can be accurately determined. In the case of +5REF, +10REF, and -10REF, the output of the voltage source is varied until the comparator output toggles. This is important when performing system diagnostics such as self test and auto-calibrate.

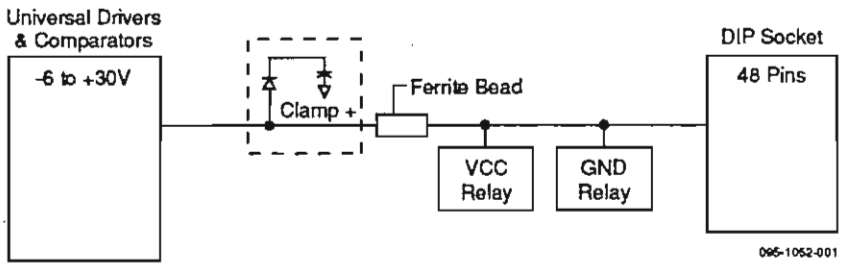
In the low state, the comparator outputs pull down to the -15V supply rail. Since this is an unacceptable level for the 74HC373 comparator latch, it is connected to one end of a 24.9KΩ resistor. The other end is connected to the 74HC373 input and a 10KΩ resistor to form a voltage divider network. This provides acceptable input voltages to the comparator latches. There is a 0.01 µF capacitor on the output of each comparator, whose function is to stabilize the output when both inputs are at equal levels.

Site 48 Board

The Site 48 board (701-2158) provides an interface between the controller board and the 48-pin device socket.

The module features universal pin driver capability on all 48 pins of a DIP socket. Pin driver functions include pull-up and pull-down, high-speed logic drive, adjustable current source, and voltage drive of -6 to +33 volts. Relays K1 through K96 are used to produce clean Vcc and ground signals, and allow configuration specific to each device (refer to Figure 3-27). Clamp diodes CR49 through CR72 coupled with 0.01 µF capacitors C18 through C21 prevent voltage overshoots to the device pins. Ferrite beads B1 through B48 prevent current spikes at the device pins. The READY and ACTIVE LED indicators connect to the relay circuitry to indicate the device programming status.

Figure 3-27
Site 48 Block Diagram



Site 40 Board

The Site 40 board (701-2021) provides an interface between the controller board and the 40-pin device socket.

Relays K1 through K40 are used to cleanly produce Vcc and ground signals to the sockets. READY and ACTIVE LEDs attached to these relays indicate whether a device is being programmed. Clamping diodes CR1 through CR6 prevents voltage spikes to socketed devices.

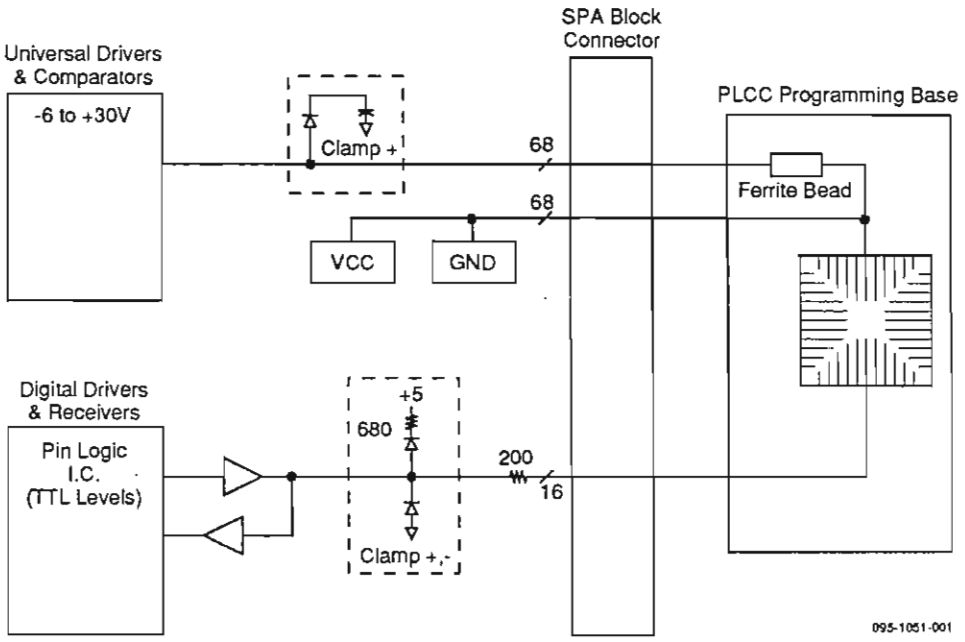
PinSite Board

The PinSite relay board (701-2230), when used in with one of the programming bases, such as a PLCC base, provides an interface between the controller board and devices to be programmed. See Figure 3-28.

The module contains 68 universal pin drivers and 16 digital pin drivers to provide programming support for up to 84 individual pin requirements. Relays K1 through K136 provide clean Vcc and ground signals to the sockets. READY and ACTIVE LEDs attached to these relays indicate whether a device is being programmed. U1, Q1, and Q2 generate 4.5 volts to supply the digital ICs. Clamp diodes coupled with 0.01 µF capacitors prevent voltage overshoot from reaching the devices.

The SPA block provides the interface between the relay board and the interchangeable programming base. This base routes the pin driver and relay signals to the appropriate pins for each type of device package. Ferrite beads are used to reduce current spikes.

Figure 3-28
PinSite Block Diagram

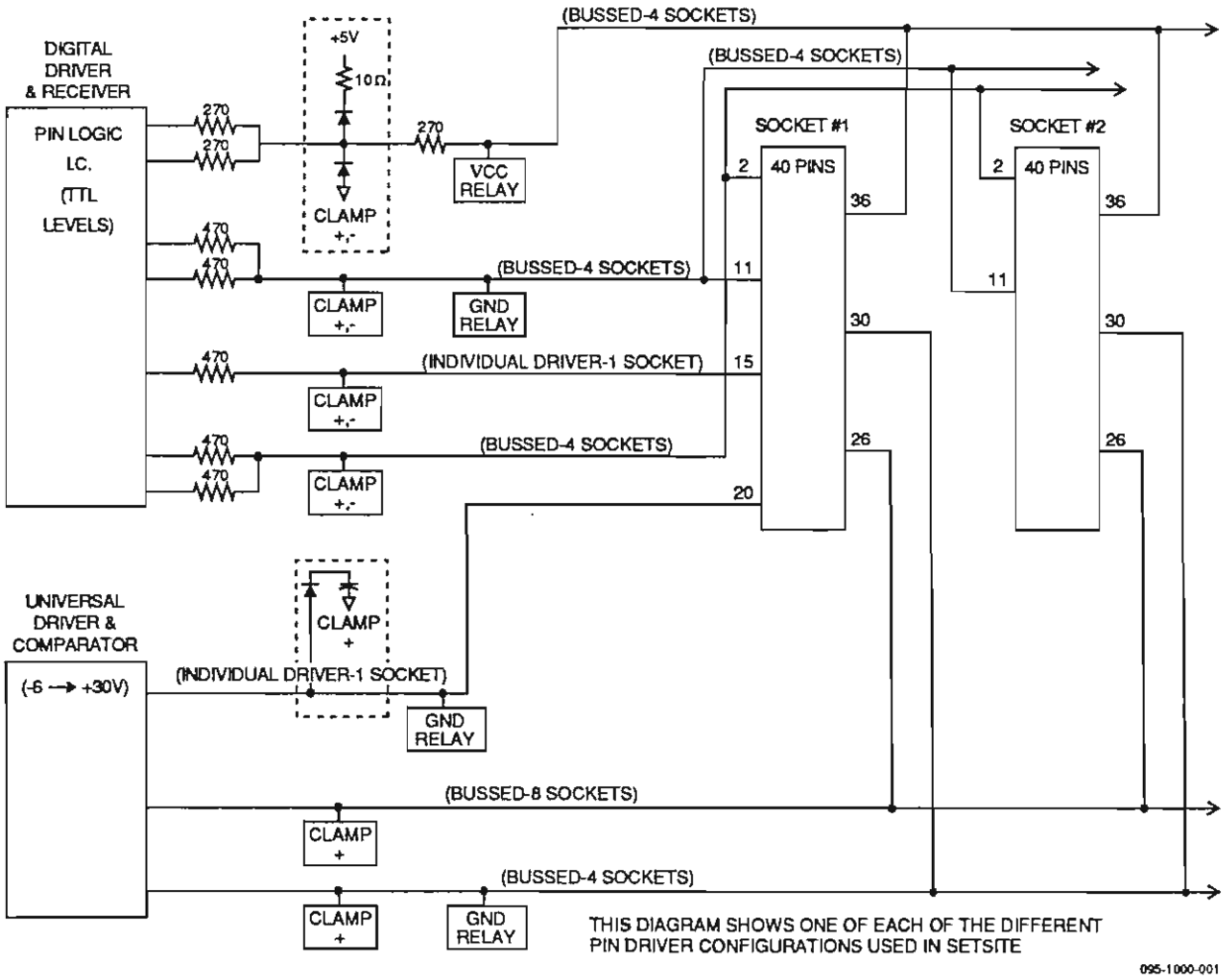


SetSite Board

The SetSite board (701-2016) provides an interface between the controller board and the eight ganged 40-pin device sockets of the SetSite Module.

The SetSite board (refer to Figure 3-29) uses 40 universal pin drivers and 170 digital pin drivers to route the programming signals to the socket pins required by the devices selected and installed in the eight programming sockets. The signals are routed to the programming sockets through the drivers in either an individual line, four socket bus, or eight socket bus format. The ground and Vcc relays pull the digital driver lines either high or low under the direction of the UniSite controller. The universal driver lines are supplied with the applicable voltage between -6 Vdc and +30 Vdc through voltage clamps and the ground relays as determined by the controller, based on the selected device type.

Figure 3-29
SetSite Board



ChipSite Board

The ChipSite FSM board (701-2042) provides an interface between the controller board and the LCC/SOIC device sockets.

Clamp diodes CR1-15 coupled with 0.01 µF capacitors prevent voltage spikes to socketed devices. Relays K1-K40 produce clean Vcc and ground signals to the sockets. Individual socket and ACTIVE LEDs connected to the relay circuitry indicate that a device is being programmed. 12 0.1µF capacitors on all +5V lines reduce noise.

Expansion RAM Board

CAUTION: ***The Expansion RAM Board (PN 701-2114) is to be used with the first version of the controller board only (part number 701-2012). It is not compatible with the second version of the controller board (part number 701-2313). RAM is added to the second version of the controller by installing SIMMs.***

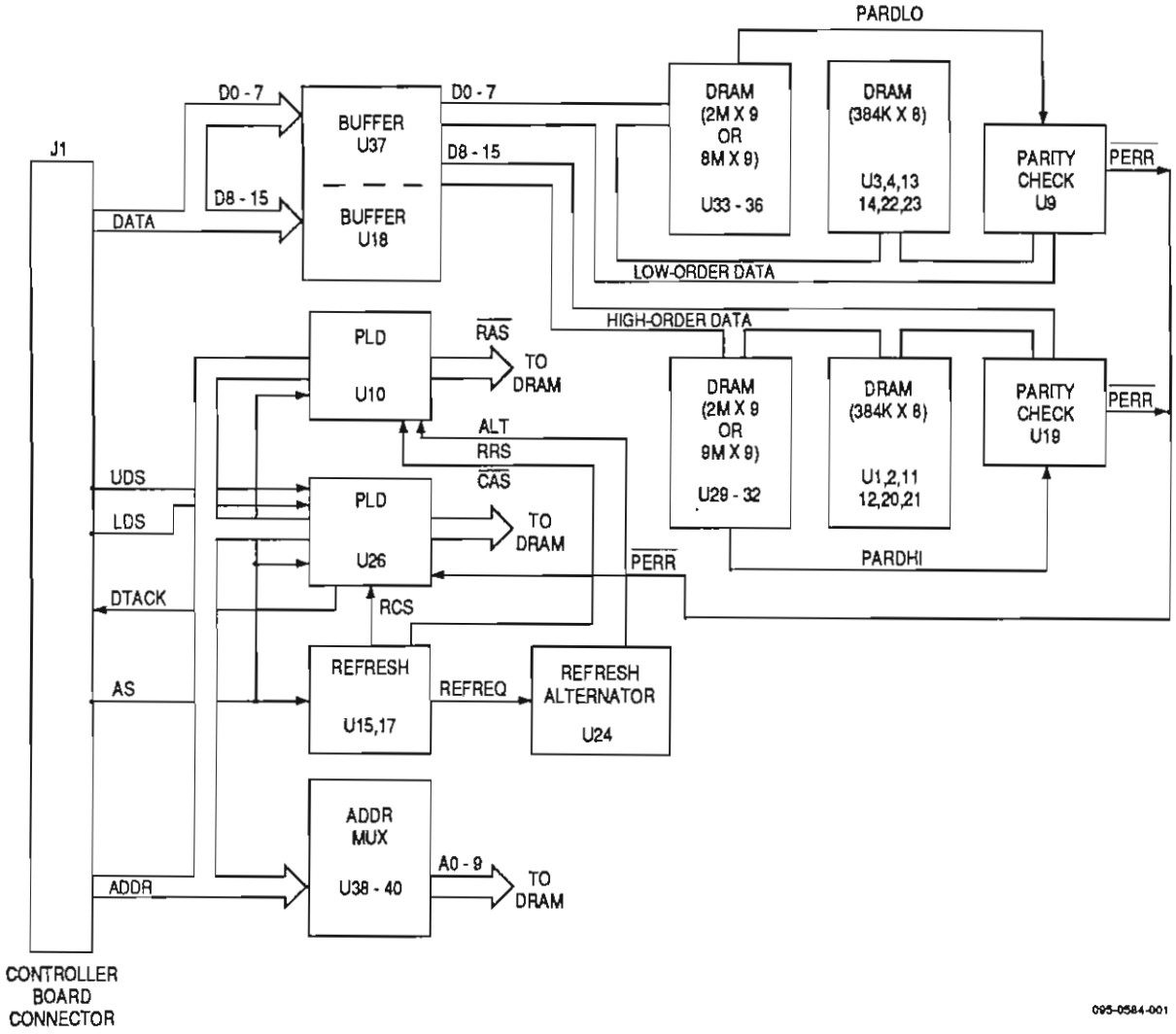
Signals between the Expansion RAM board and the controller board are routed through connector J1 (see Figure 3-30). The RAM board's DRAM consists of eight 9-bit-wide SIMMs and 12 64K x 4 DIPs, split between the high- and low-order data bytes. DRAM uses the CAS-before-RAS refresh mode.

Address lines A1-A20 are multiplexed through U38,U39 and U40. The resulting addresses, low- and high- A0-A9, are then routed to DRAM. A17-23 are the address lines for the two decode PLDs.

Data lines are buffered by either U18 or U37, and then routed to either the high- or low-order DRAM. D0-D7 are routed through buffer U37 to the low-order DRAM; D8-D15, to buffer U18 and the high-order DRAM. Parity checking for the by-9 SIMMs is performed by parity checkers U9 and U19. If a parity error occurs during a memory cycle, U9 or U19 send a logic low onto the PERR- line to PLD U26. U26 then stops sending a DTACK (data acknowledge) signal to the 68000. The 68000 waits for the DTACK signal for 3ms; then signals a bus error. A parity error will then appear on UniSite's screen.

Refresh for DRAM occurs through the refresh circuitry, U15, U17 and U24. Data strobe lines UDS and LDS are fed through J1 to the RAM board's PLD U26. A refresh request is routed from U17 to the refresh alternator, U24, via a logic high on the REFREQ line. The column- and row-refresh signals, RCS and RRS, are routed to the two PLDs. PLD U10 then sends out RAS- to DRAM; PLD U26 sends the CAS- signals.

Figure 3-30
Expansion RAM Board



4 Maintenance/Troubleshooting

This chapter describes the UniSite maintenance and troubleshooting procedures and also includes information on preventing static damage to UniSite circuitry.

WARNING: **This manual is intended for use only by service personnel. Do not attempt any of these procedures unless you are qualified to do so.**

Reducing Electrostatic Discharge

Some devices installed in or programmed by UniSite are susceptible to electrostatic discharge (ESD), which may cause subsequent failure or unsatisfactory operation of the part or its related circuitry. The effects of ESD are reduced through the use of special equipment and procedures. This section describes methods you can use to lessen the likelihood of ESD.

ESD Precautions

The easiest way to prevent ESD damage is to make sure a common static potential (ground) exists between the static-sensitive device, its environment, and you. To accomplish this, ground the operator to the workstation via an antistatic strap and cover the surface of the work area with an antistatic material.

Devices to be programmed may also be protected by either placing them on a non-conductive foam pad or enclosing them in an antistatic material. The most common antistatic material is a special, conductive plastic, commonly referred to as "pink poly."

Use the following precautions at a prepared workstation to reduce ESD.

- Do not install or remove static-sensitive (or any other) devices from a circuit that has power or signals applied to it.
- Install antistatic tops and wrist strap grounding studs on work benches and tables. (UniSite has a factory-installed grounding stud.)
- Provide antistatic trays, carriers or toteboxes for transporting assemblies.
- Maintain the relative humidity above 40%.
- Connect UniSite's chassis to ground using the banana plug receptacle on UniSite's rear panel.

Static-sensitive Devices

The following is a partial list of particularly static-sensitive devices you may encounter while operating or servicing UniSite.

- MOS and CMOS devices
- Schottky and low power Schottky TTL logic circuits
- Small-signal diodes
- TTL logic circuits
- Junction FETs
- Small-signal transistors
- Metal-oxide resistors

Maintenance

Periodic maintenance of UniSite consists of cleaning the unit and checking the sockets. UniSite requires no calibration, although the controller frequency, the waveform board's VREF supply, and the power supply's voltages may be checked periodically (see the "Calibration" section).

Cleaning

Clean UniSite's exterior with a clean cloth, dampened with water and a mild detergent. Never use caustic cleaning agents that could damage the surface. To prevent any damage, always disconnect the power cord before cleaning.

Socket Maintenance

Check the DIP socket module(s) periodically for accumulation of dirt and debris and remove dust with dry, compressed air. Clean the socket itself with only methyl alcohol, Freon TE™, or detergent and water. When checking the socket, also check for signs of socket wear; the average lifetime of a socket is 25,000 to 50,000 insertions. If the socket is not opening and closing smoothly, it may need replacing.

The PLCC/LCC Base uses an elastomeric pad which makes electrical connections between a programmable device and the PLCC Base. Reliability testing shows that the pad can accept over 10,000 device insertions for each package size without degradation. To extend the pad life, blow clean dry air over the pad to remove any dust debris that may accumulate. Do this every 1000 insertions or as needed.

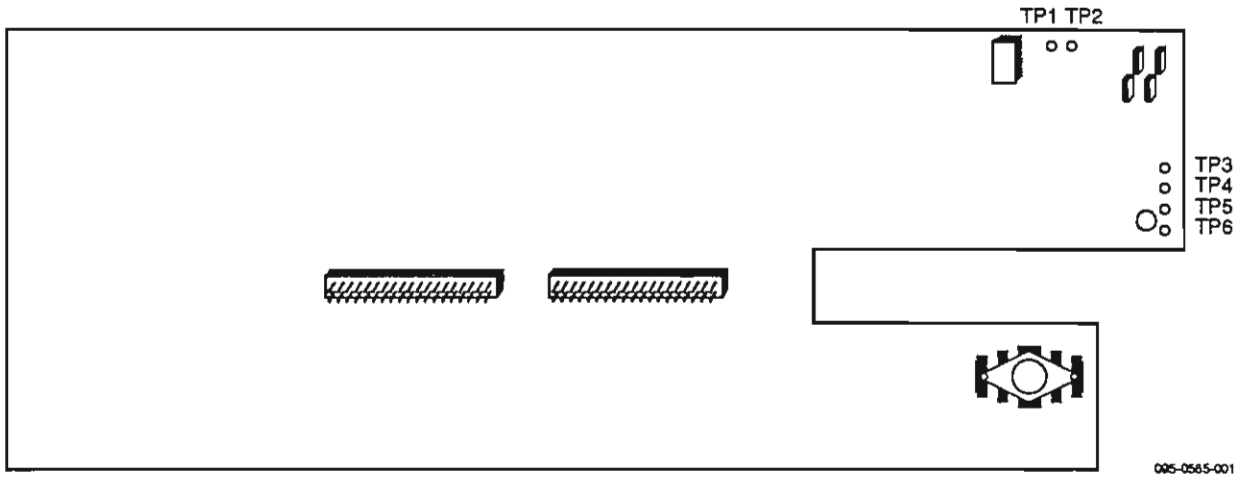
Calibration

UniSite never needs to be calibrated by a user. All calibration is performed by software and is compared to a laser-trimmed voltage reference on the waveform board. You may check the voltage, VREF, by using a digital multimeter. See Table 4-1 for allowable values. Figure 4-1 shows test point locations.

Table 4-1
Waveform Board Supply Voltages

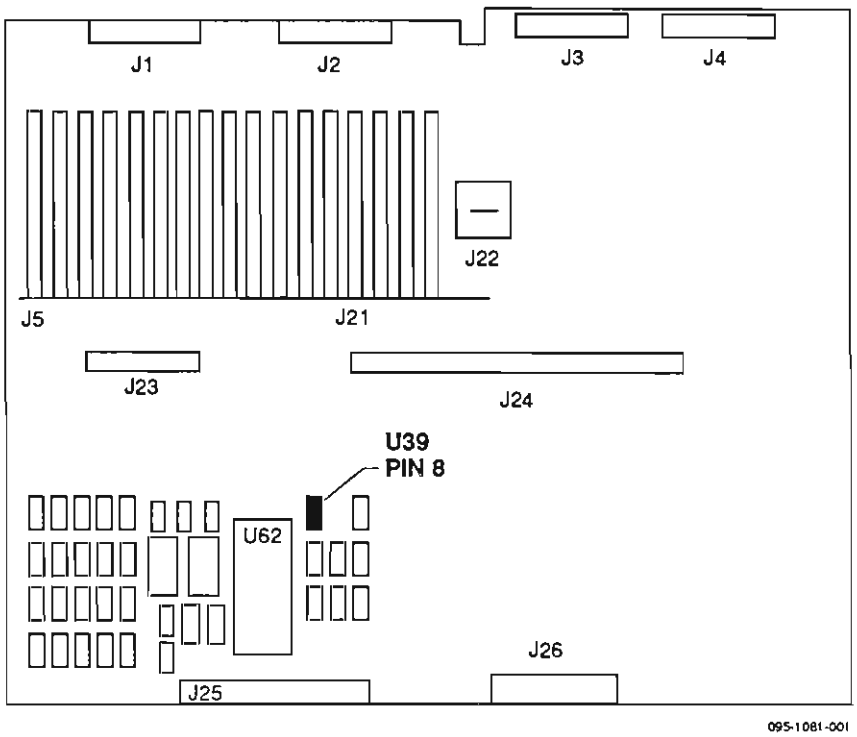
Test Point	Tolerance
TP1 (+10 REF)	+9.990V to +10.010V
TP2 (A GND)	GND
TP3 (+5 REF)	+4.5V to +4.8V
TP4 (-10 REF)	-9.8V to -10.2V
TP5 (-10V)	-9.8V to -10.2V
TP6 (+40V)	+39.20V to +40.80V

Figure 4-1
Waveform Board Test Point Locations



You can check the system master clock at U39 pin 8 on either version of the controller board. See Figure 4-2. The frequency should be between 9.9990 and 10.0010 MHz.

Figure 4-2
Controller Board Frequency Test Point



Troubleshooting

Using the Front Panel LEDs to Isolate Faults

UniSite always performs a self-test upon power-up. The four front panel LEDs illuminate in different patterns, depending on the results of the self-test. Table 4-2 shows all possible LED combinations and the meaning of each.

This section explains what to do if the LEDs signal an error condition, usually a faulty circuit board. After isolating the problem board by following the procedures described below, contact your nearest Data I/O Customer Support office and arrange to send the unit in for servicing.

Table 4-2
Front Panel Indicators

INDICATOR				DESCRIPTION
Power	Terminal	Remote	Self Test	
On	Off	Off	On	Self-test in progress. No error condition.
On	On	Off	Off	Terminal port OK; self-test finished. No error condition.
On	Off	On	Off	Remote port OK; self-test finished. No error condition.
On	On	On	Off	Remote & terminal ports OK; self-test finished. No error condition.

INDICATOR				DESCRIPTION
Power	Terminal	Remote	Self Test	
On	Off	Off	Off	Terminal port not properly connected; check connection.
Off	n/a	n/a	n/a	Power supply off, or no 5V supply.
On	Blinking	Off	On	Bad CPU, EPROM, U50 or power-fail detect.
On	Off	Blinking	On	Bad system RAM (locations 80000-FFFFF).
On	Blinking	Blinking	On	Bad serial port DUART (68681).

Terminal Indicator Blinks; Remote LED Is Off

If the terminal indicator on the front panel blinks after power-up while the REMOTE LED is off, the problem is either a bad CPU, EPROM, bad U50 device or a power-fail detect error.

If the CPU is faulty, the Controller board may need replacement. If the problem is in EPROM, verify the checksum of each EPROM on the Controller board using another UniSite—the EPROM may need to be changed out. If the problem is a power-fail detect error, the power supply may be bad. In all cases, UniSite needs servicing.

Check to see if U50 is properly inserted. The circuitry is designed to not allow operation if U50 is missing.

Remote Indicator Blinks; Terminal LED is Off

If the remote indicator on the front panel blinks after power-up while the terminal LED is off, the problem is bad system RAM, at locations 80000-FFFFF. If this is the case, one or more of the system RAM chips may need replacing.

Remote and Terminal Indicators Blink; All Other Indicators Illuminated Continuously

If the terminal AND the remote indicators on the front panel blink after power-up while the other two indicators are illuminated continuously, the problem is with the serial port. Check the 68681 serial port device, U14. See the circuit description in Chapter 3, "Theory of Operation," for more information.

Power Indicator Blinks or Does Not Illuminate

When the power LED indicator on the front panel either blinks or does not light up, the problem may be with either the Waveform board's power transistors or the Power Supply. Check the power supply connector's test points, as explained in the following two procedures:

1. Remove the top cover, as described in Chapter 2.
2. With the power supply connector plugged in (J22), measure all five of the power supply's outputs, located next to J22 on the Controller board (see Figure 4-3). Table 4-3 shows the allowable values for each supply. If the measured values are not within those measured in the table below, you may have a bad power supply. Contact your nearest Data I/O Customer Support office.

Figure 4-3
Power Supply Outputs

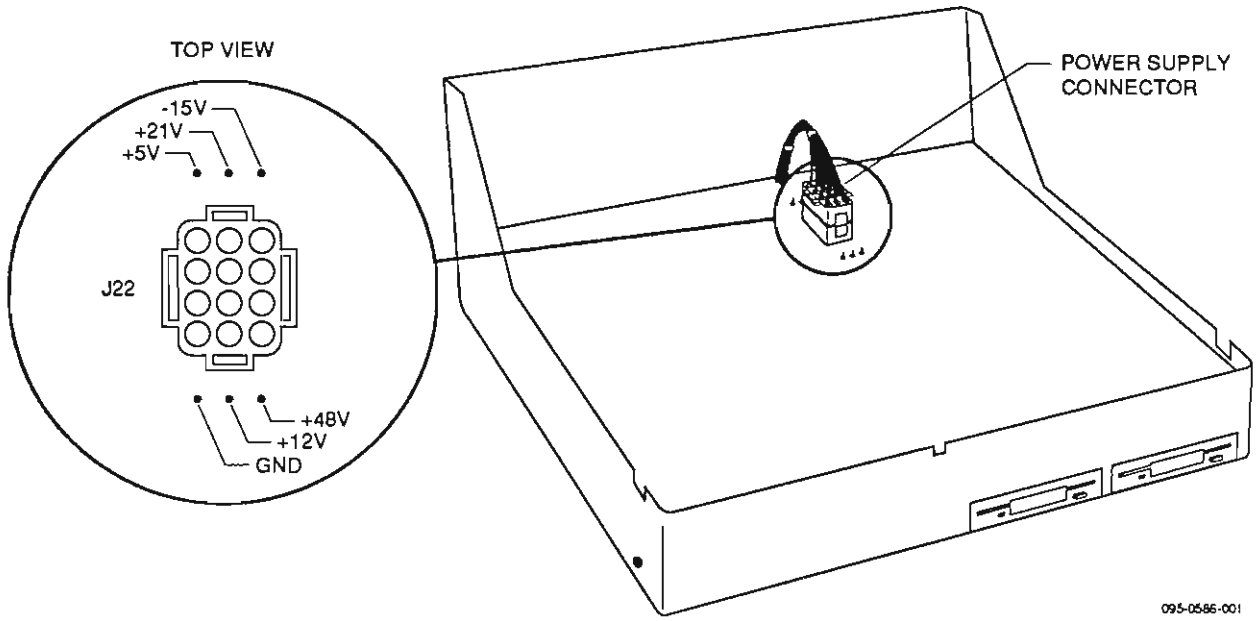


Figure 4-3
Power Supply Outputs

Test Point	Range
-15V	-14.29 to -15.3V
+5V	+4.75 to +5.25V
+12V	+11.4 to +12.6V
+21V	+19.9 to +22.8V
+48V	43.0 to 55.0V

3. Disconnect the power supply connecter, J22. Using a digital multimeter, measure the resistance between the GND test point and each of the other five test points next to J22. Table 4-4 shows the allowable resistance values. If the measured resistances do not fall within those specified here, there may be a short on one of the circuit boards. To isolate the problem board, disconnect each board in turn, and check the values listed in Table 4-3. contact your nearest Data I/O Customer Support office.

Table 4-4
Resistance Values

Output	Typical Resistance from Ground
-15V	Greater than 5Ω
+5V	Greater than 0.5Ω
+12V	Greater than 14Ω
+21V	Greater than 8Ω
+48V	Greater than 50Ω
Supply-to-supply	Greater than 200Ω

Using Power-up Error Messages to Isolate Faults

On power-up, UniSite checks all major systems. If there is a malfunction, the following error message is displayed at the top of the screen

```
POWER UP SELF-TEST FAILED
```

This message is accompanied by a list of problems detected by the self-test. Listed below are those possible messages and what to check. See the circuit description in Chapter 3 for more details on operation.

FSM/PSM Socket not Empty

If you get this error during the power-up self-test, make sure there are no devices in the programming sockets. If this error appears AFTER self-test, it could mean there is a bad pin driver board; see the next section.

No FSM or PSM Installed

Install the FSM or PSM, if none is installed, and cycle the power (turn UniSite off and then on again).

If an FSM or PSM is installed and you get this message, check U107 (74LS251) and U73 (74LS86) on the controller board. These are FSM/PSM detect devices. If either one is bad, replace both devices since electrostatic discharge (ESD) may have damaged them. See "Reducing Electrostatic Discharge" in this chapter for more information.

No Pin Drivers Installed

UniSite must have a pin driver board installed in connector J5, the left-most connector, in order to pass the self-test. Make sure that the pin driver boards are properly installed.

PCU Error

Cycle the power. If the message returns, then the PCU is bad, there is a bad pin driver board in the left-most position, or the waveform board is faulty.

Pin Driver Error

Check the self-test screen to see which pin driver board is faulty. Remove the top cover and the faulty pin driver board according to the procedure in Chapter 2, and call your nearest Data I/O Customer Support office to arrange for replacement of the board.

Waveform Board Error

Remove the top cover and switch the left-most pin driver board (installed at J5) with any other pin driver board. The waveform board's self-test requires a functioning pin driver board to be in the left-most position, so if the test passes after you swap board positions, the problem is with the pin driver rather than the waveform board.

Note: To fully calibrate the Site 40's PSM module, the first TEN pin driver board sockets (J5-J14) must contain a board. This is necessary so that the self-test may check all the FSM relays.

Isolating Errors that Occur after Self-test

Disk Drive Errors

If you get a disk drive failure error, try using a different disk. If that does not alleviate the problem, remove the problem drive (according to the procedure in Chapter 2) and call your nearest Data I/O Customer Support office to arrange for service.

Note: Make sure the controller board's mounting screw located between the two RS-232C connectors is inserted completely. This screw makes the chassis ground connection to the controller board and is necessary for reliable disk drive operation.

Socket Not Empty Error

If you get this error after the self-test has ended, the problem may be with either the pin drivers or one of the socket modules. Execute the Self-test command and see if the PSM/FSM tests pass and if the pin driver boards pass. See the "Waveform Board Error" paragraph in the previous section.

FSM or PSM Errors

If any problems seem to be related to the FSM or PSM, check the following components on the controller board: U73, U77, U107 and U117. These chips interface between the controller board and the FSM or PSM. Also make sure enough pin driver boards are installed: to fully calibrate the Site 40's PSM module, each of the first ten pin driver board sockets (J5-J14) must contain a board so that the self-test can check all the PSM relays.

Using the Kernel Jumper Checks to Isolate Problems

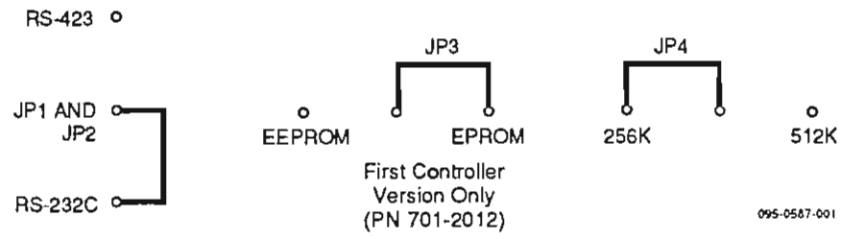
If UniSite will not power up, you can use a kernel jumper test to diagnose the problem. Follow the procedures below to check JP1-JP4, remove the controller board's DIP jumper, and read signal outputs. (For more information on the Controller board's circuitry, see the "Controller Board" section in Chapter 3.)

Checking JP1-JP4

Remove the top cover as described in Chapter 2. Make sure controller board's four jumpers are properly positioned. JP1 and JP2 select the serial port configuration, JP3 specifies EPROM as the type of program memory and JP4 selects EPROM size. See Figure 4-4 for proper jumper positioning.

Note: If 27256 EPROMs are installed, JP4 is optional.

Figure 4-4
Controller Board Jumper Positioning



Checking the 68000's Signals

Remove the DIP jumper, U49, on the controller board. Removing this jumper causes the 68000 processor to execute continuous read operations of UniSite's entire memory range, allowing you to pinpoint the problem by checking various control signals. Appendix A contains diagrams of various controller board signal waveforms during normal operation. With the jumper removed, check the following signals:

68000 Control Signals	CLK, AS-, LDS-, and UDS- should be toggling.
	RESET-, HALT-, BERR-, IPL0-, IPL1-, and IPL2- should be at a logic high.
68000 Address and Data Lines	All address lines (A1-A23) should all be toggling. Data lines should toggle when the processor cycles through the EPROM memory range; this will appear as an infrequent burst of data.
Decode Signals	Decodes related to read operations should toggle (may be brief).
Dynamic RAM Refresh Signals	REFRAS- and REFCAS- should be low for 300ns and occur every 12µs.
Real-time Clock Signal	Should have about a 35ms period.
8-MHz clock Signal	At the 1772 disk-control chip, U14.

Finally, reinstall the U94 jumper.

Power-up Retesting

To test UniSite after reassembly, do the following:

1. Plug in UniSite's power cord.
2. Insert the UniSite system disk into drive A.
3. Plug in the ASCII terminal's power cord and power up the terminal.
4. Turn on UniSite. The Power and Self Test indicators on UniSite's front panel illuminate. Drive A's active indicator will also be illuminated. If the drive indicator does not illuminate, check to see that the disk is properly inserted.
5. When the drive A indicator goes off, make sure all self-tests have been completed. The Self Test indicator extinguishes when the self-test is completed. The Terminal indicator on UniSite's front panel now illuminates. If this indicator does not light up, press the terminal port's DCE/DTE switch on UniSite's back panel.

6. When the Terminal indicator lights up, the serial port connection has been properly established.

Note: If the terminal indicator still does not light up after you have pressed the DCE/DTE switch, your RS-232C cable or terminal may be defective.

If the terminal now displays random or incorrect characters, press [BREAK] [A] . This automatically sets UniSite's baud rate to that of the terminal. The terminal should now display the UniSite system configuration information.

7. Verify that the terminal type is correct.
8. Verify that the RAM size configuration information appearing on the screen matches the actual UniSite RAM size.
9. Respond to the question concerning terminal type. If you do not want to select a new terminal type, press [↵] . Press [Y] if you do.
10. Get to the Self-test screen, by pressing [M] and then [S] . The Self-test screen appears.

Note: To perform the Self-test, the System disk should be installed into drive A. If you have a second disk drive, install the Utility disk there. You must also have a PSM installed in order to perform the Self-test.

11. Move the cursor to `Perform all Tests` and press [↵] .
12. Testing begins immediately. The cursor flashes beside the area being tested. `TESTING` appears on the large reverse video block at the top of the screen.
13. If the RAM board was installed correctly, `PASS` is displayed on the screen next to the various UniSite systems.

If a `FAIL` message appears, recheck your reassembly procedure, making sure all cables are installed correctly.

If you check the reassembly and the problem still persists, try to isolate the area of concern by disconnecting the RAM board and running a complete system self-test. If available, you may use a UniSite Diagnostic board to check the system. If you still cannot isolate the problem, call your nearest Data I/O Customer Support office.

5 *Messages*

This chapter lists and describes UniSite's system and error messages. If a message requires action, instructions for that action are included in the message's description. Messages are listed in alphabetical order.

Some system and error messages were not documented in this chapter because UniSite provides online help for these messages. To access the online help for a message, press F3 or ? when the message appears.

Note: PSM (Package Specific Module) and FSM (Function Specific Module) refer to the modules that are installed on UniSite's front panel. The PSM is the small module located on the left side of the top panel; the FSM is the optional, large module on the right.

Message List

0 div err

UniSite has experienced a divide-by-zero error that it cannot recover from. This is a fatal error; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.

Addr err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] *or* [?] *when the message appears.*

Address out of range

The address you tried to select is beyond the selected device's range. Select an address that is within the limits of the device or select a different device. This message appears while you are in the memory editor, fuse editor, or using the under/overblow feature.

Altera POF translator must be selected for POF devices

This message appears when you have selected an Altera POF device and attempt a data transfer operation, such as a download, and have not selected the POF data translation format. Select the POF format as the data translation format and try the operation again.

ASCII entry not allowed in 4-bit mode

This message appears in the memory editor when attempting to go into ASCII entry mode when a 4-bit device is selected. Re-select device or edit in hex mode only.

Beginning of file

This message appears when you are viewing the first block of data and press [Ctrl] – [P] (previous page) when you are using the memory editor, vector editor, fuse editor, or the under/overblow feature.

Begin address too large

The beginning address you selected in the memory editor was too large and is beyond the limits of the selected device. Change the begin address to one within the device's range.

Booting non-system disk. Insert system disk. Type ESC and CTRL W to reboot.

This message will appear if UniSite detects a disk other than the System disk installed in drive A during power up. Insert the System disk.

Bus err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.

Bytes copied = nnnnnn

This message appears while the Copy File operation is in progress; *nnnnnn* refers to the number of bytes copied.

Cannot access system disk

This message indicates a non-system disk is installed. Make sure the Algorithm disk and System disk are installed.

Calculating sumcheck

This message appears when you are using the Device Check's Sumcheck screen, informing you that the RAM sumcheck is being calculated.

[Computer Remote Control: enter Control-Z to exit.]

This message informs you that UniSite is now in remote control mode and all programmer commands are now read from the remote port. Typing [Ctrl] – [Z] returns control to terminal mode.

Constant over-current fault

This message indicates that an over-current condition exists and UniSite is unable to clear the condition. The over-current could be caused by a hardware failure in UniSite. Reboot the system. If the condition persists, contact your nearest Data I/O Customer Support Office.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] or [?] when the message appears.

Constructing Job File Directory	The job files are now being read, in order to put together a job file directory. You can then select one of the files for playback.
Copying file1.ext to file2.ext. Bytes copied = xxxx	This message appears during a Copy operation if you are using the wildcard designation. *xxxx* in the display is the number of bytes copied into the destination file.
Copying sectors ssss - ssss+120 Reading source disk	This message appears while the Disk Copy command is proceeding. The information presented in this message displays the number of sectors copied in each pass. There are 1440 sectors on each disk. This message is accompanied by the message "Copying sectors ssss - ssss Writing destination disk" which appears while UniSite is writing data onto the destination disk.
Copying sectors ssss - ssss+120 Writing destination disk	This message appears during the Disk Copy routine, indicating that the data is being copied.
Could not initialize default system parameters from disk	When UniSite was booting up, the default and programming system parameters could not be loaded. Reboot UniSite with a different system disk, or call your nearest Data I/O Customer Support Office for assistance.
Data transfer complete	This message appears after a data transfer with an external source was successfully completed.
Data transfer complete. Data Sum = ssssssss	After a data transfer, this message appears. The data sum represents the calculated sumcheck for the data bytes transferred.
Data transfer complete. Data Sum = ssss. Xmit = ssss.	After a data transfer of a JEDEC file, this message appears. The data sum represents the calculated checksum for the data bytes in the fusemap section of the data transferred. The Xmit sum represents the calculated checksum for all the bytes transferred.
Data transfer complete. Data Sum = ssss. POF CRC = ssss.	After a data transfer of a POF file, this message appears. The data sum represents the calculated checksum for the data bytes transferred. The POF CRC represents the calculated Cyclic Redundancy Check for all the bytes in the POF file up to, but not including, the CRC value.
Data operation complete: data saved on disk	After a data file is downloaded to disk, this message appears.
Destination file already exists. Hit return to continue, ^Z to abort.	The filename that you have designated as the destination for the data already exists, so existing data will be written over if you execute the operation. This is a precautionary message which occurs on any file operation which could overwrite an existing file.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] or [?] when the message appears.

Disk boot err	UniSite has experienced an error that it cannot recover from. Turn UniSite off and reboot the system. If the problem persists, use another copy of the System disk.
Disk data error	The read or write operation that was attempted could not be completed because there is a problem with the disk; try the operation again with a different disk.
Disk duplication overwrites user RAM. Hit Return to continue, ^Z to abort.	If you copy a disk, UniSite uses User RAM as a buffer. Anything already in User RAM will be overwritten. If you don't want to change User RAM, type [Ctrl] – [Z] to halt the disk duplication. Press [↵] to proceed with the operation.
Disk error, terminal type not saved!	If you try to save the terminal type as one of the power-up parameters and there is a write problem with the disk (the disk is either full or is defective), this message will appear.
Disk open error. Type ESC and Control W to reboot.	This message appears if you try to boot UniSite without the System disk in the disk drive. Insert the System disk in the disk drive and reboot UniSite.
Disk write-protected, terminal type not saved!	If you try to save the terminal type as one of the power-up parameters and the disk is write-protected, this message will appear. Move the write-protect slide so that the hole through the disk is blocked.
Done.	The operation is completed. Proceed to the next operation you want to perform.
Done. Bytes copied = nnnnnn	This message appears after the Copy File operation is complete. It displays the size of the file that was copied in hexadecimal bytes. Proceed to the next operation you want to perform.
End of file	This message appears when you are viewing the last block of data and press [Ctrl] – [N] (next page) when you are using the memory editor, vector editor, fuse editor, or the over/under blow feature.
Fatal system err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.
FILE ERROR: Can't reach track 0.	If this message appears, a fatal disk error has occurred. The disk drive may be faulty. Contact your nearest Data I/O Customer Support Office.
FILE ERROR: Error in sector preamble.	This error appears when UniSite detects an error with the format of a disk. Use a different disk or reformat the existing disk and try the operation again.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] *or* [?] *when the message appears.*

FILE ERROR: No disk in drive.

This message appears when UniSite is trying to access a disk file but the disk drive is empty. Insert the disk with the file to be used.

FILE ERROR: Track not found.

This message appears if UniSite cannot find the disk track associated with the system file, or cannot find the data needed to support whatever action you just requested. If you try the operation again and the error message reappears, a new disk (or a new copy of whatever software or data the unit needs) must be used.

File not initialized! Enter 'C' to initialize, any other key to quit

This message appears within the fuse editor, vector editor or when the under/overblow feature is selected. The file that you have selected is not in a format that is compatible with the feature that you want to use. If you want to use the fuse editor, and the data file you have is not formatted for the device you have selected, typing [C] reformat the data file to be compatible with the device.

Formatting and initializing user disk.

This message appears while a disk is being formatted.

Hit PF3 or ? to view device specific message

The selected device has specific information associated with it.

Hit return to continue, ^Z to abort.

This message appears after a Verify operation has failed. If you want to ignore the warning and not examine the errors, and proceed with the verify operation, press [J] . If you want to investigate the verify errors, press [Ctrl] – [Z] and the Verify screen will reappear.

Hit return to switch user menu port, ^Z to abort.

This message is displayed whenever you toggle the User Menu Port parameter. To cancel the port switch operation, press [Ctrl] – [Z] , otherwise, press [J] to switch the port. The cable between the programmer and the PC (or terminal) should then be moved to the port specified by the parameter.

IOX init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Illegal instr err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Illegal Key Input: Type control-Z to abort parameter entry.

You pressed a key that is illegal for the field where the cursor is positioned. For example, if you type in a hex number for the Data Word Width field (only decimal numbers are allowed), this message will appear.

Illegal terminal type!

The terminal type number you entered was not one of the choices presented on the Terminal Type screen. Type in a valid terminal type number.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] or [?] when the message appears.

Insert blank device. Hit return.

This message appears during a Quick Copy operation. Remove the newly programmed device or the master device from the device socket, place a blank device in the socket and press [↵] . UniSite will then begin programming the blank device with RAM data loaded from the master device.

Insert destination disk. Hit return to continue.

This message may appear during the Duplicate Disk or Copy File operation. When this message appears, remove the source disk, insert the destination disk (the disk where you want the data to go to) and press [↵] . Make sure to use a formatted disk: if you insert an unformatted disk, UniSite will abort the operation and display "Sector not found." If this occurs, perform the Format Disk operation and restart the Duplicate Disk or Copy File operation.

Insert master device. Hit return to continue.

This message appears during a Quick Copy operation. Place the master device into the device socket, lock it into place, and press [↵] . UniSite will then start to load RAM with data from the master device.

Insert blank device. Hit return to continue or push START lever forward

This message appears during a Quick Copy operation if you are using the SetSite module. Place the blank devices into the SetSite sockets, lock them into place and press [↵] or move the socket lever to the START position. UniSite will then start to program the parts with data from RAM.

Insert master device. Hit return to continue or push START lever forward

This message appears during a Quick Copy operation if you are using the SetSite module. Place the master device into device socket number one, lock it into place, and press [↵] or move the socket lever to the START position. UniSite will then start to load RAM with data from the master device.

Insert source disk. Hit return to continue.

This message appears during a Duplicate Disk operation. When this message appears, remove the destination disk from the disk drive, insert the source disk and press [↵] .

Job file playback ended.

This message informs you that a job file's playback has ended and you may continue with the operation where the job file left off.

Job file save aborted. Keystrokes not recorded.

This message appears in the following situation: If you attempt to end job file recording, and either the system disk is not in the drive or UniSite has difficulty reading the disk, an error message will appear. If you press [Ctrl] – [Z] after seeing that message, the above message will appear.

Keystroke recording ended. Select job file for saving.

This message appears after you have pressed [Esc] [Ctrl] – [J] a second time to end recording keystrokes for a job file. Specify a job file number, by typing a number between 0 and 9. Then type in a job file description.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] *or* [?] *when the message appears.*

Keystroke recording for job file has begun.	After you press [Esc] [Ctrl] – [J] once, this message will appear. You are now in the job file record mode: every keystroke that you make will be recorded. Type [Esc] [Ctrl] – [J] a second time to end the session.
Loading data from file.	This message appears while data is being loaded into User RAM from a disk's data file.
Loading device algorithm	When you restore a set of system parameters that include a specific device, this message will appear while the programming algorithm is being loaded.
Loading device algorithm file into user RAM.	This message appears when the device programming algorithm is being loaded into User RAM at the first device selection operation after the RAM Device Selection parameter is enabled.
Loading device menu data	This message indicates that UniSite is loading the device and manufacturer selection files.
Loading from disk.	This message appears when UniSite is reading system information or routines from the disk.
Loading programming parameters	When you restore a set of system parameters from the Configuration file directory, this message will appear while the programming parameters are being loaded.
Loop count nnnn = Hit CTRL Z to abort this test	This message appears while a self-test is running in the continuous mode. The loop count *nnnn* is the number of times the selected test has been repeated.
Memory parity error at:hhhhhhh	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the problem persists, record the location at which the error is occurring (represented above by *hhhhhh*), and call your nearest Data I/O Customer Support Office.
No disk in drive A.	There is no disk in the disk drive. Insert the System disk into drive A and try the operation again.
Non-blank device. Hit return to continue, ^Z to abort.	This message appears after UniSite has performed a blank check on a device and has detected bits that are not in their erased or blank state, and are not illegal bits. If you press [↵] , UniSite proceeds with the Programming operation and programs over the existing data. If you press [Ctrl] – [Z] , the Program screen will reappear and you can try the operation again with another device. The Blank Check parameter must be enabled before this test can be performed.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] or [?] when the message appears.

Odd Memory Begin Address is not allowed	This message appears when the Memory Begin Address is set to an odd number and you try a device operation on a 16-bit (or larger) device. Set the Memory Begin Address to an even number and retry the device operation.
OPERATION COMPLETE.	The operation you selected has been completed; you may now proceed with other operations.
OPERATION COMPLETE. Device = hhhhhhhh.	This message appears after a successful Compare Electronic ID operation. *hhhhhhhh* represents the device's electronic ID.
OPERATION COMPLETE. Sumcheck = hhhhhhhh	This message appears after the completion of a Program, Load, or Verify operation. *hhhhhhhh* represents the sumcheck of the data that was programmed into the device.
OPERATION COMPLETE. Sumcheck = hhhhhhhh. Set Sumcheck = ssssssss	This message appears after the completion of a Set Program, Load, or Verify operation. *hhhhhhhh* is the sumcheck of data that was just programmed into the last set member. *ssssssss* is the sumcheck of all the set members that have been programmed.
Options installed. Hit Return after changing your terminal settings.	This message appears on the Serial Port Configuration screen after serial port parameters have been changed and [↵] has been pressed. When this message appears, UniSite suspends screen output until you press [↵] a second time. Make sure you configure the terminal to match the new settings for the serial port.
Parameter Entered	This message acknowledges that the parameter you entered was accepted.
Parameter Field Full. Hit return or arrows to enter, CTRL Z to abort.	This message appears when you try to enter too many characters into a parameter field. Press [↵], [F1] or [F2] to enter the parameter.
Power Down	UniSite has experienced a power down condition.
Pre-format check.	This message appears when you have selected the Format Disk operation, and means that UniSite is checking to see if the disk you want to format is a system disk. If this error occurs, go to the self-test screen and re-execute the test(s) that show status of F (Fail). If the test(s) fails while the device socket is empty, UniSite may require service. Contact your nearest Data I/O Customer Support Office.
Purging filename.ext	This message will appear if you are using the wildcard (*) designation to purge more than one file at once; for example, type 27*.dat to delete both the files 27512.dat and 27256.dat.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] or [?] when the message appears.

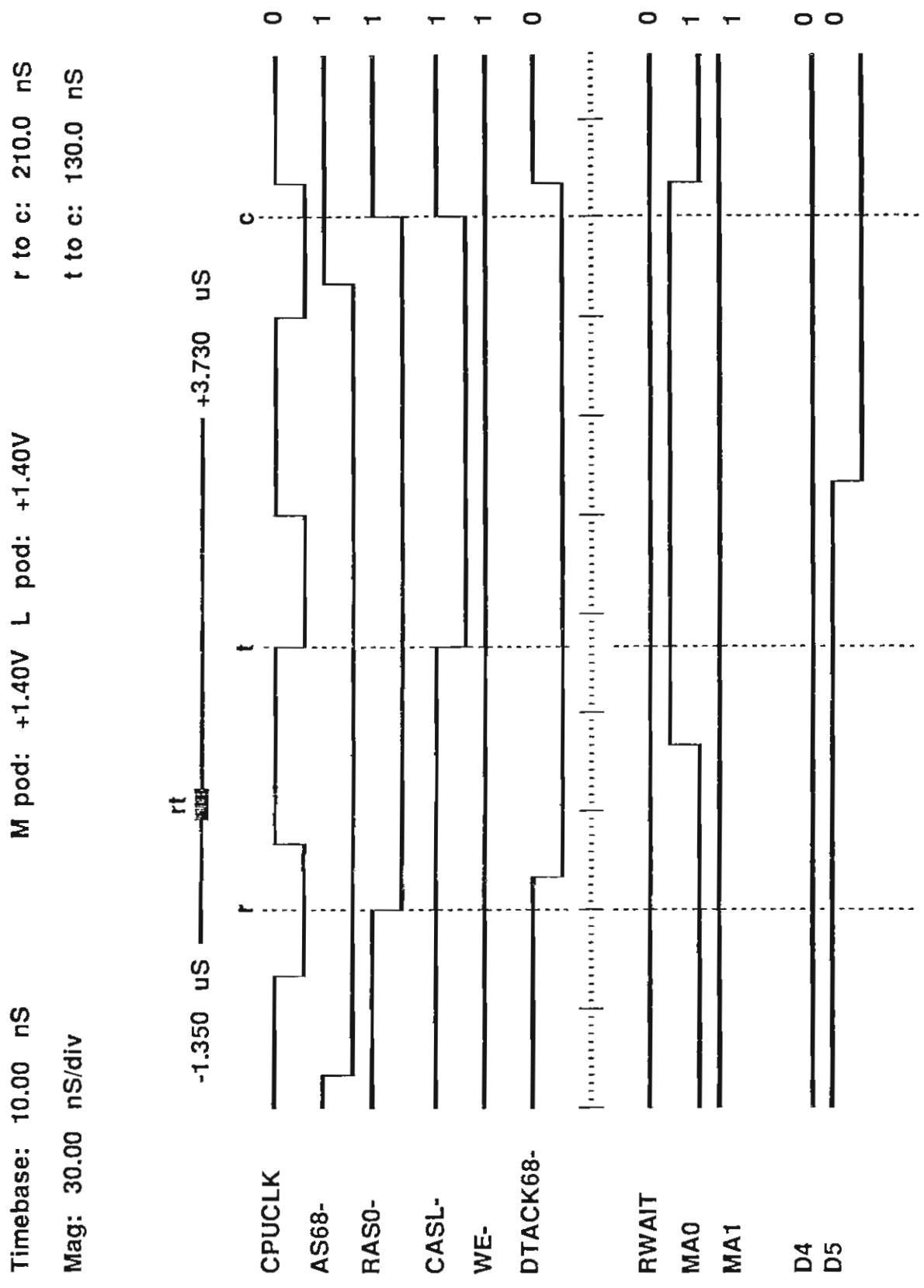
Reading user data file size	This message appears while UniSite is reading the data file size from disk.
Recording system state parameters.	This message appears after you select a file number for the set of system parameters that you want to save. This message remains until UniSite is finished recording the parameters.
Restoring system state variables.	This message appears while UniSite is reading the recorded system variables from the selected file.
RTC err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.
RTE init err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.
Saving data to file.	This message appears while data is being written to a file on disk.
Saving parameters	This message appears when UniSite is saving the selected variables onto the disk.
Saving job file.	This message appears when UniSite is saving a job file.
Search pattern not found	If you specified a data pattern for a file that does not contain that pattern, this message will appear. This message appears while UniSite is in the memory editor or in the under/overblow display.
Security fuse violation. Hit return to continue, ^Z to abort	This message appears when you try to program an EE device with the security fuse already blown. If you continue by pressing [↵], the program operation will be performed and previous data in the device will be overwritten.
System error. Please contact Data I/O.	Contact your nearest Data I/O Customer Support Office.
System parameters restored.	This message appears when you have restored a configuration file from the Restore System Parameters screen.
System parameters saved.	This message appears when you save a set of system parameters.
Task error	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.

Note: Some system and error messages were omitted on purpose. UniSite provides online help for these messages. To access online help for a message, press [F3] *or* [?] *when the message appears.*

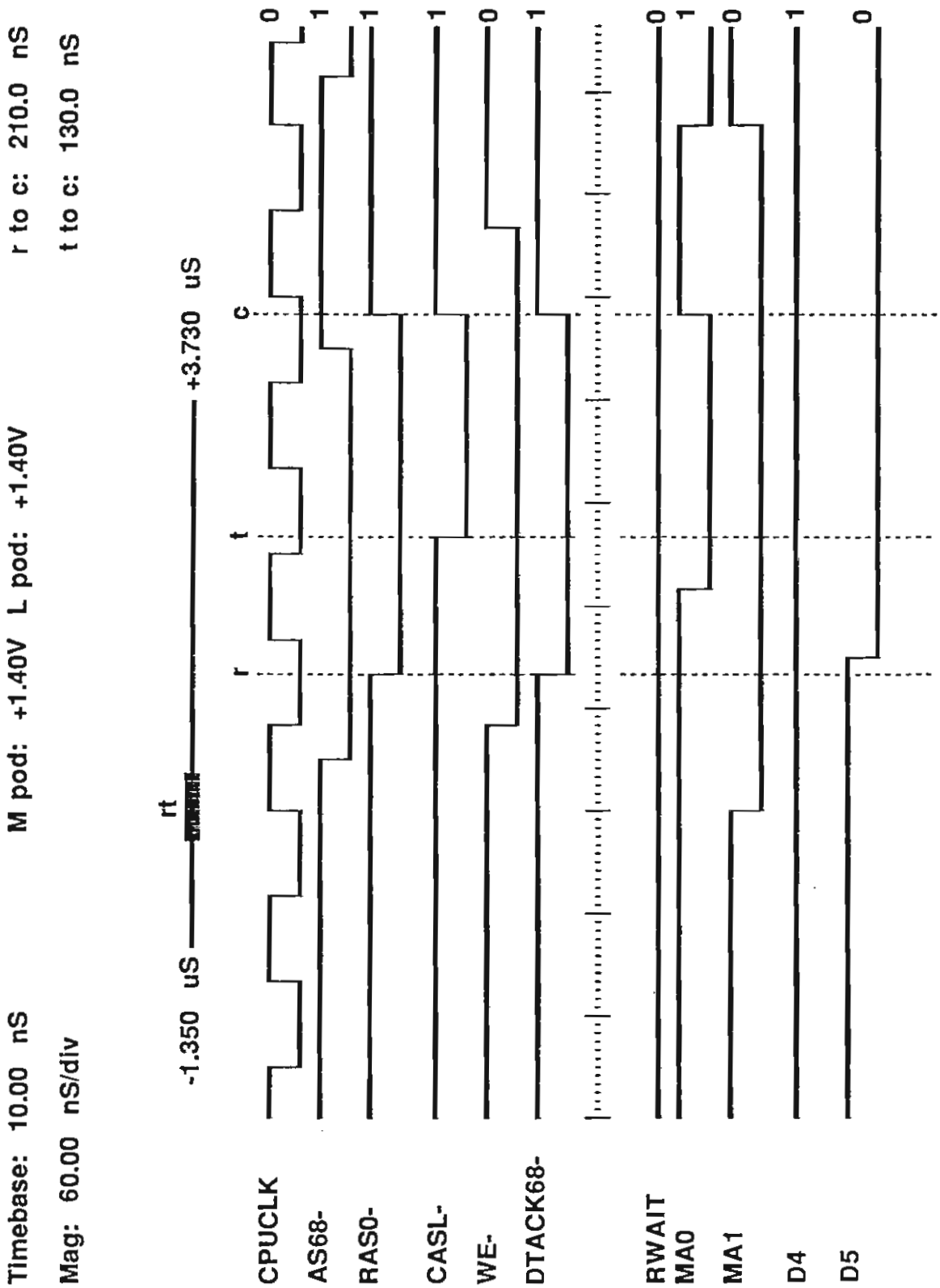
Testing	This message appears when a self-test is in progress.
TEST HALTED: Socket not empty, hit return to continue, ^Z to abort.	The self-test that you are attempting requires that the device socket does not contain any devices. Remove the socketed part and try the operation again, or type [Ctrl] – [Z] to abort the operation.
	CAUTION ***If you press the carriage return key, UniSite will run the test and the socketed device could be damaged.***
Transferring data.	This message appears while a data transfer operation is being performed.
[transparent mode]	This message appears on the screen when UniSite enters the transparent mode. To exit transparent mode, type [Esc] [Ctrl] – [T] .
Trc init err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact your nearest Data I/O Customer Support Office.
Updating device algorithms	This message appears when the algorithm disk is being updated in the Update Device Algorithms operation. Do not remove the algorithm disk or turn off system power for the duration of the operation.
User RAM sumcheck = ssssssss	This message contains the sumcheck for all of User RAM and is generated in the Sumcheck device check screen. This calculation is done regardless of whether user data is in RAM or on disk.
Vector out of range	The vector you tried to select does not exist for the device you have selected. Select a vector that is within the limits of the device or select a different device. This message may appear while you are using the vector editor.
Waiting for self-test completion.	This power-up message shows up only if you are changing the terminal selection before the power-up self-test has been completed.
WARNING Algorithm disk in drive. Hit return to continue, ^Z to abort.	This message will appear if you are attempting a file operation and have the Algorithm disk installed in the disk drive.
WARNING: System disk in drive. Hit return to continue, ^Z to abort.	This message appears during any file operation that displaces disk data. Any information currently on the disk will be erased and is not retrievable. Press [↵] to go ahead with the operation. Press [Ctrl] – [Z] , to cancel the operation.

A Waveforms

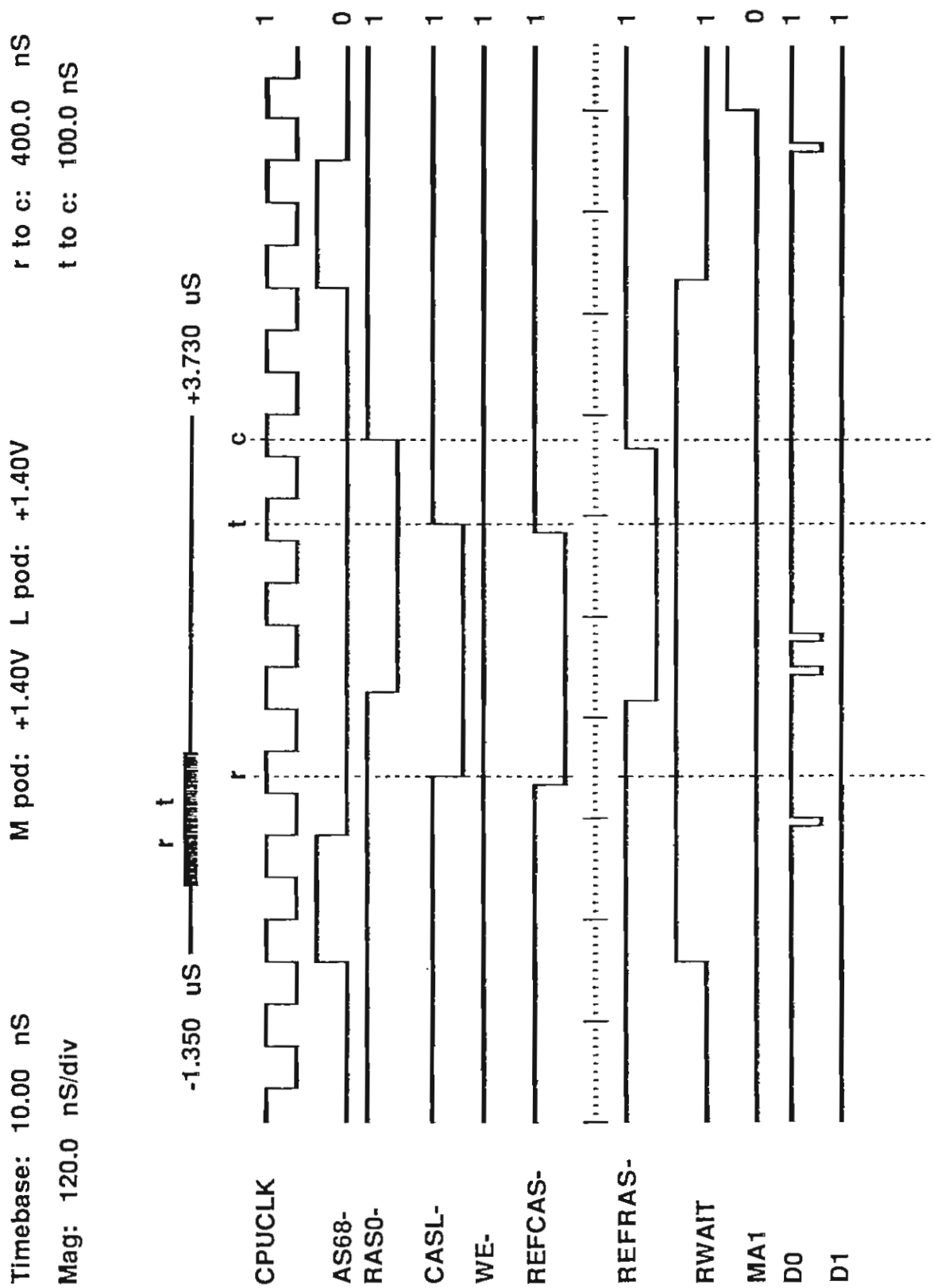
This appendix contains waveform diagrams, taken with a logic analyzer, that will help you isolate UniSite memory problems. You do not need an analyzer to compare waveforms, but using one will yield more information. You may also use an oscilloscope to compare portions of the waveforms.


Timebase: 10.00 nS
Mag: 30.00 nS/div
M pod: +1.40V L pod: +1.40V
r to c: 210.0 nS
t to c: 130.0 nS
-1.350 uS
rt
+3.730 uS
r
t
c
CPUCLK
AS68-
RAS0-
CASL-
WE-
DTACK68-
RWAIT
MA0
MA1
D4
D5
0
1
1
1
1
0
0
1
1
0
0

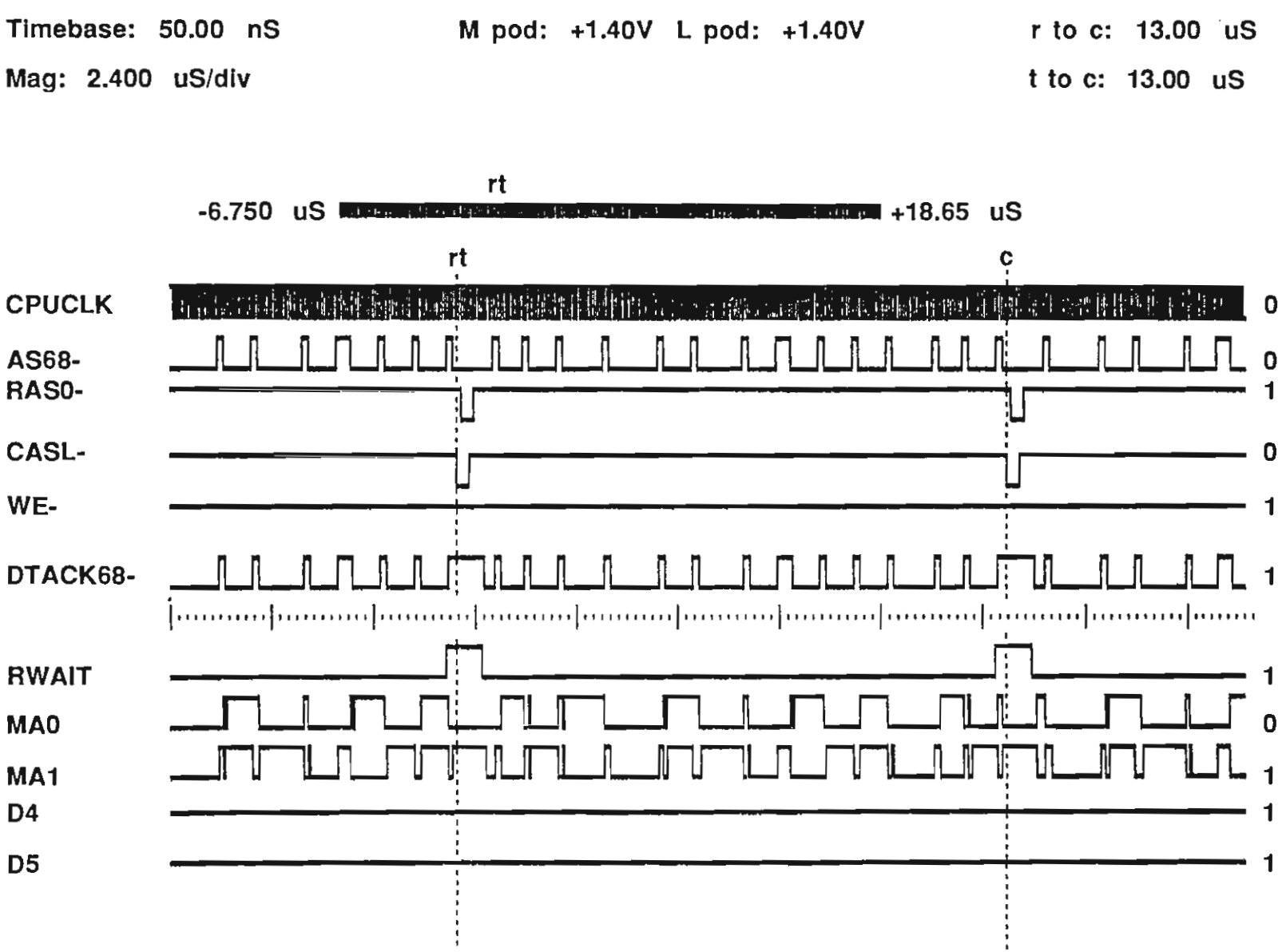
DRAM READ



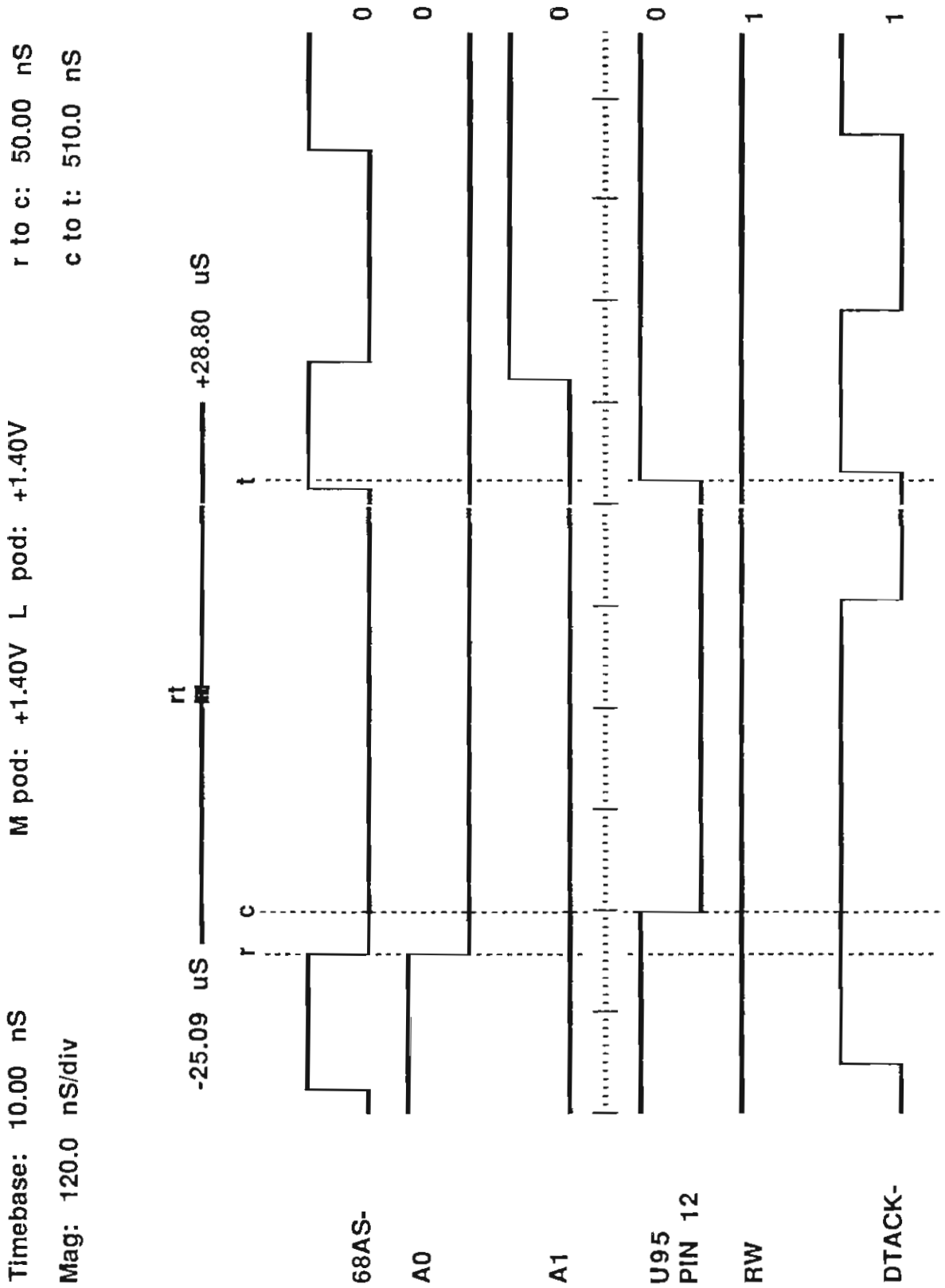
DRAM WRITE CYCLE



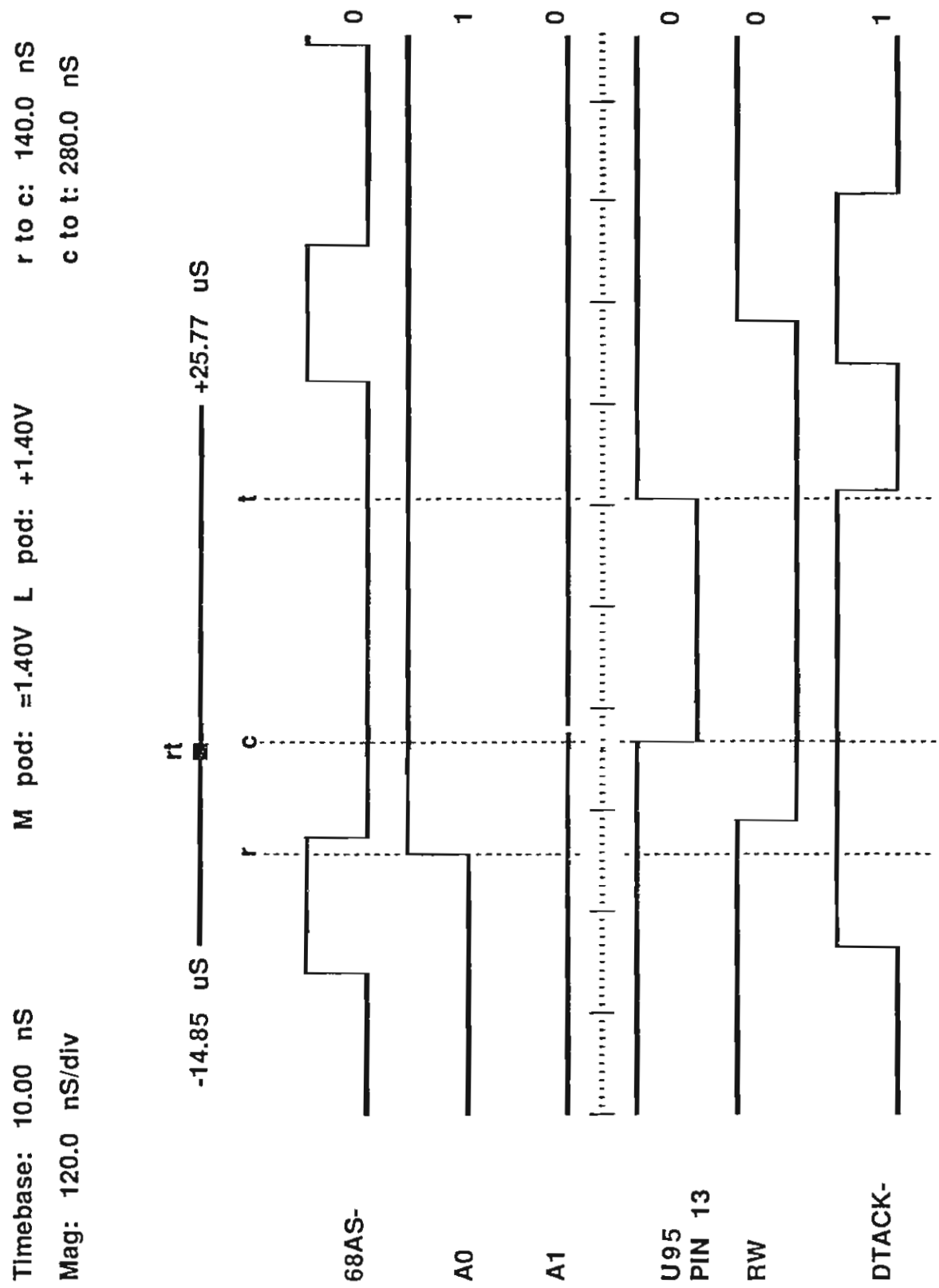
DRAM REFRESH CYCLE



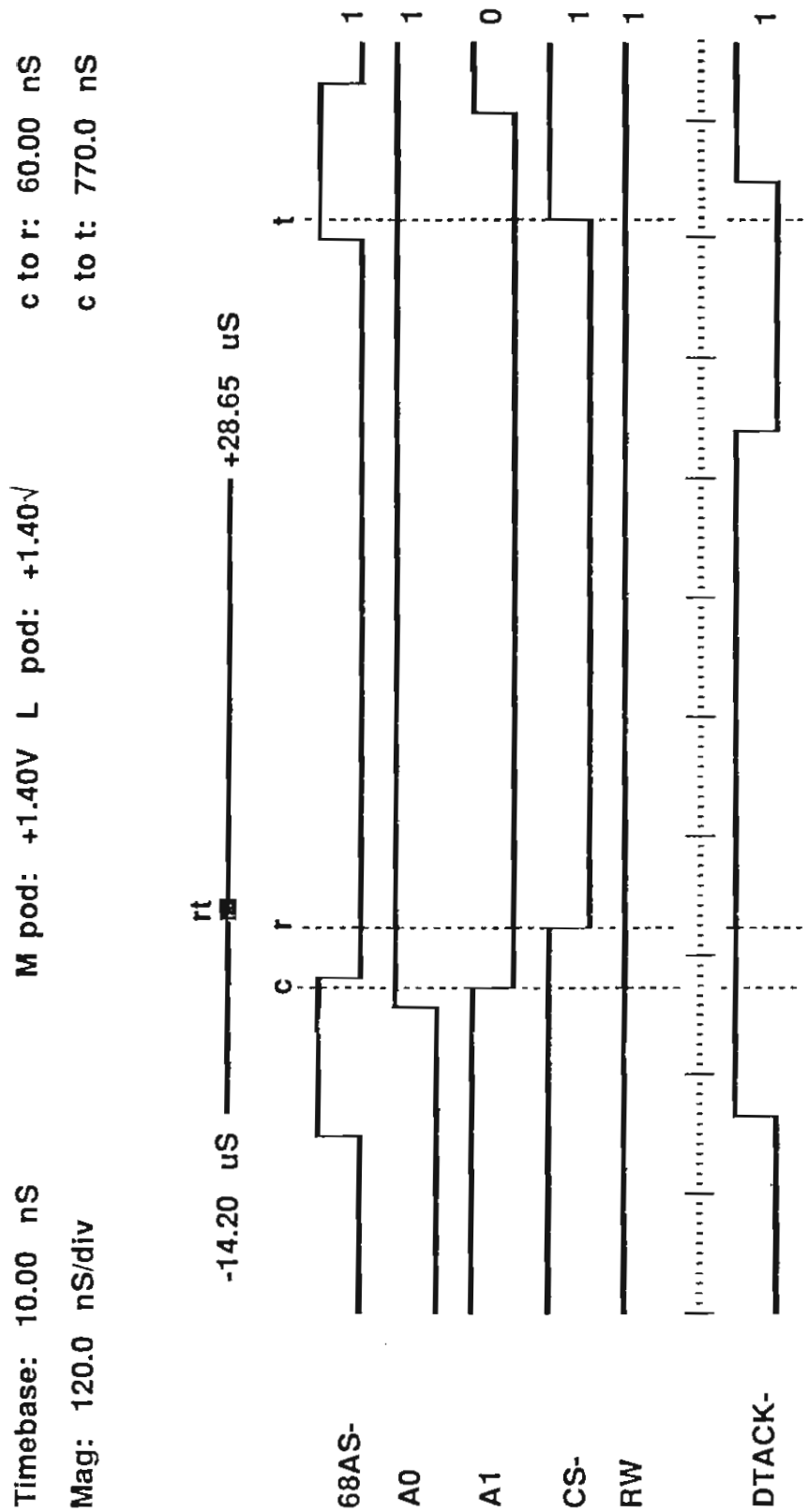
DRAM REFRESH, TWO CYCLES



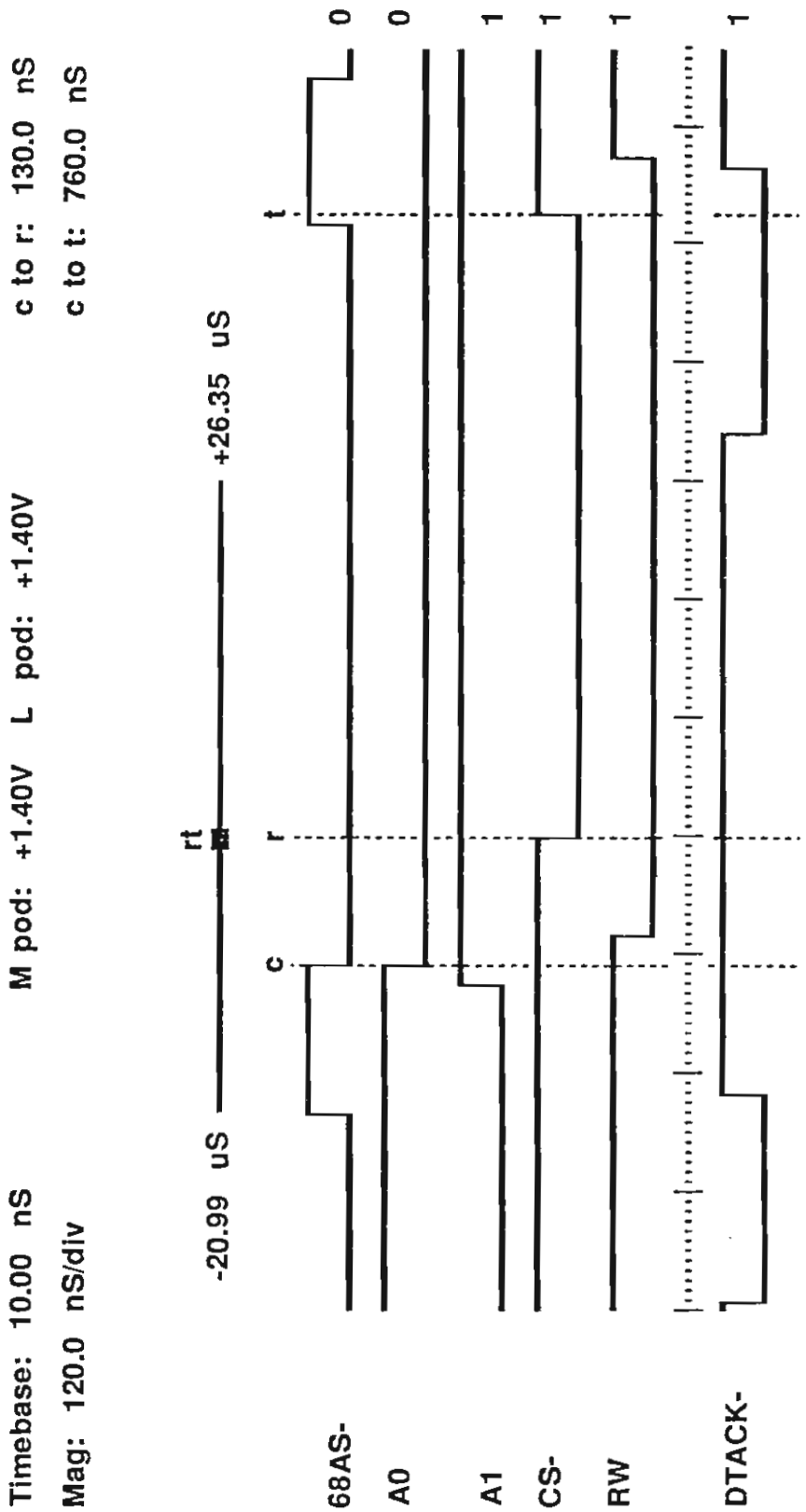
GENERAL I/O READS



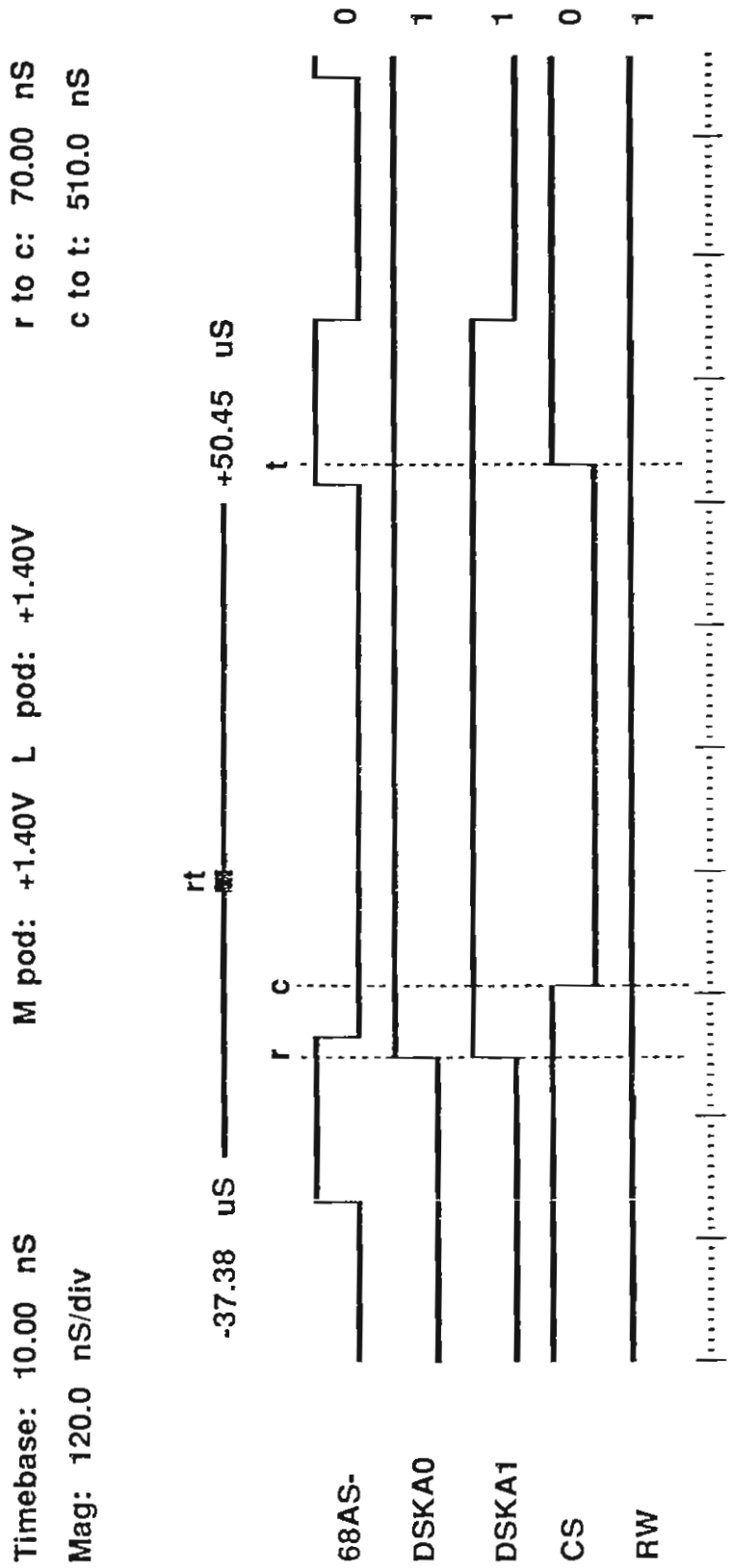
GENERAL I/O WRITE OPERATION


Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V
L pod: +1.40V
c to r: 60.00 nS
c to t: 770.0 nS
-14.20 uS
rt
+28.65 uS
c
r
t
68AS-
A0
A1
CS-
RW
DTACK-
1
1
0
1
1
1

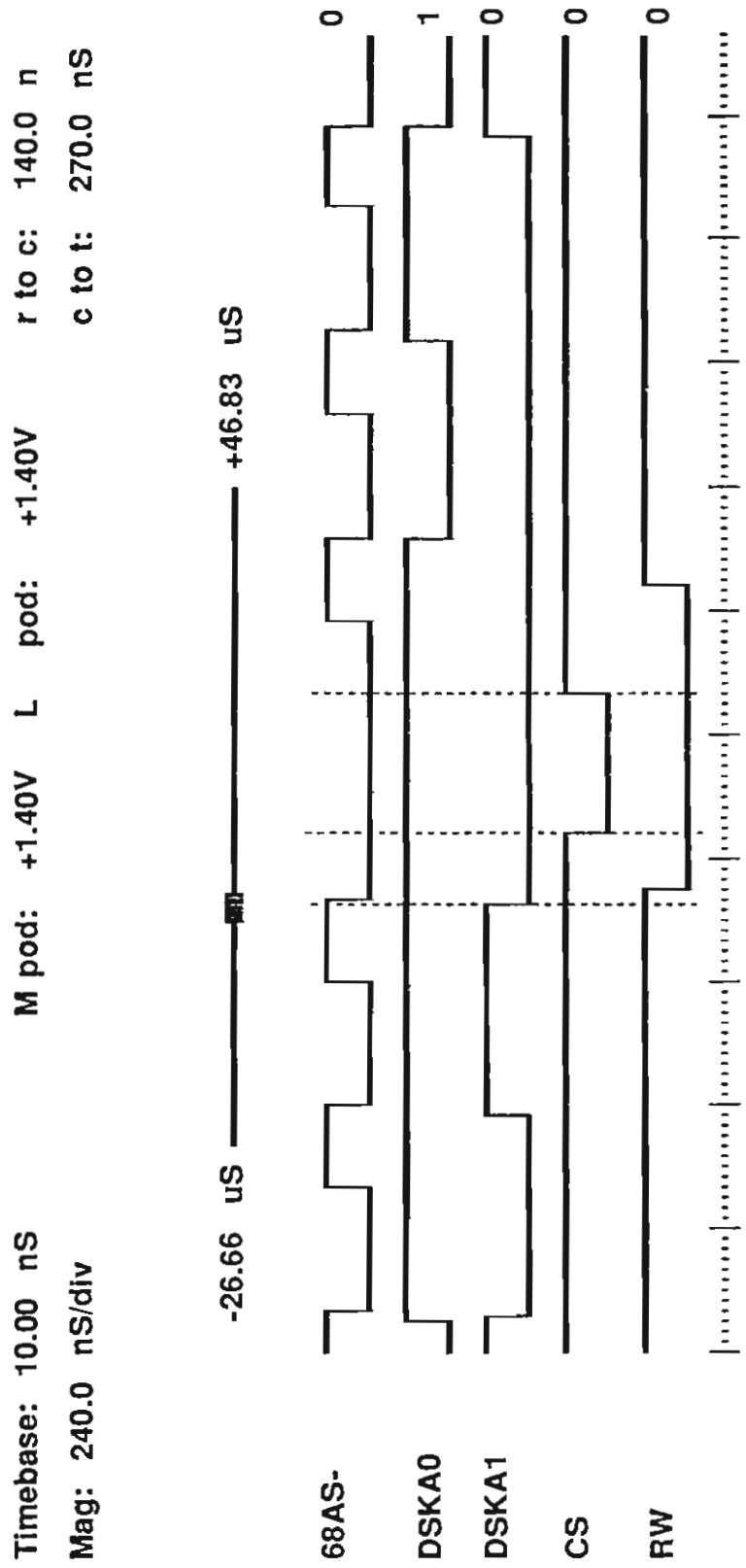
68681 READ


Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V
L pod: +1.40V
c to r: 130.0 nS
c to t: 760.0 nS
-20.99 uS
+26.35 uS
rt
c
r
t
68AS-
A0
A1
CS-
RW
DTACK-
0
0
1
1
1
1

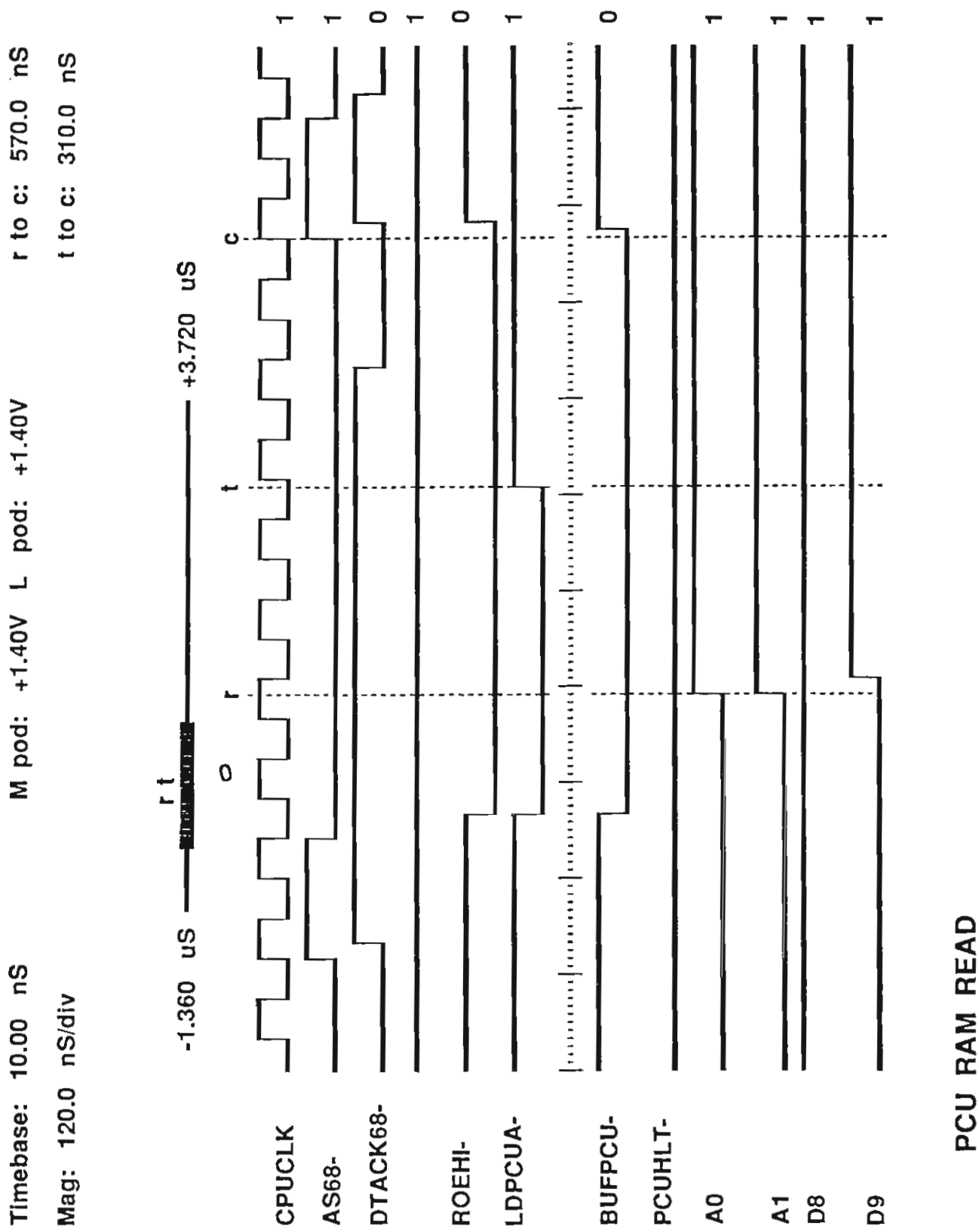
68681 WRITE

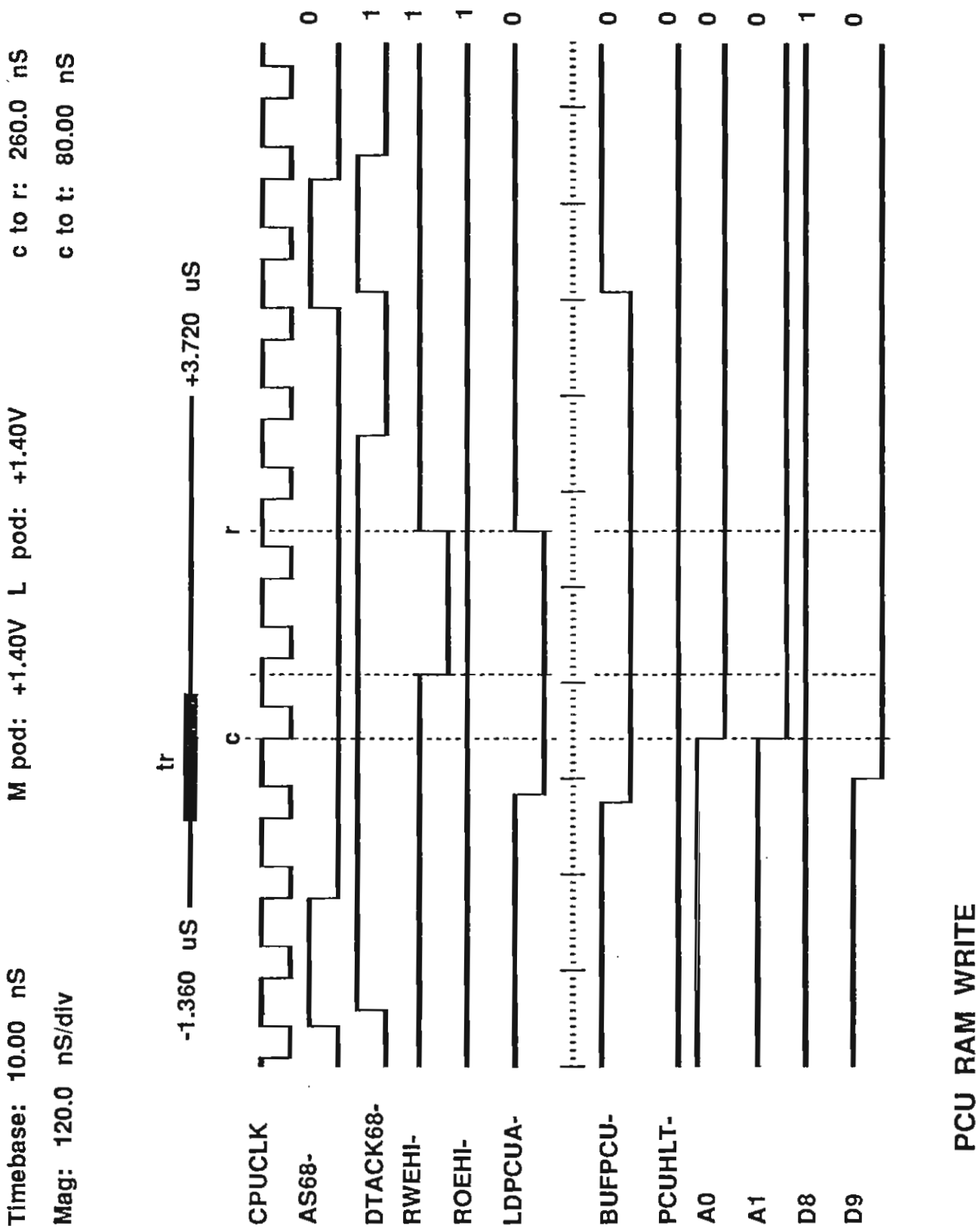

Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V L pod: +1.40V
r to c: 70.00 nS
c to t: 510.0 nS
-37.38 uS
+50.45 uS
r
c
t
rt
68AS-
DSKA0
DSKA1
CS
RW
0
1
1
0
1

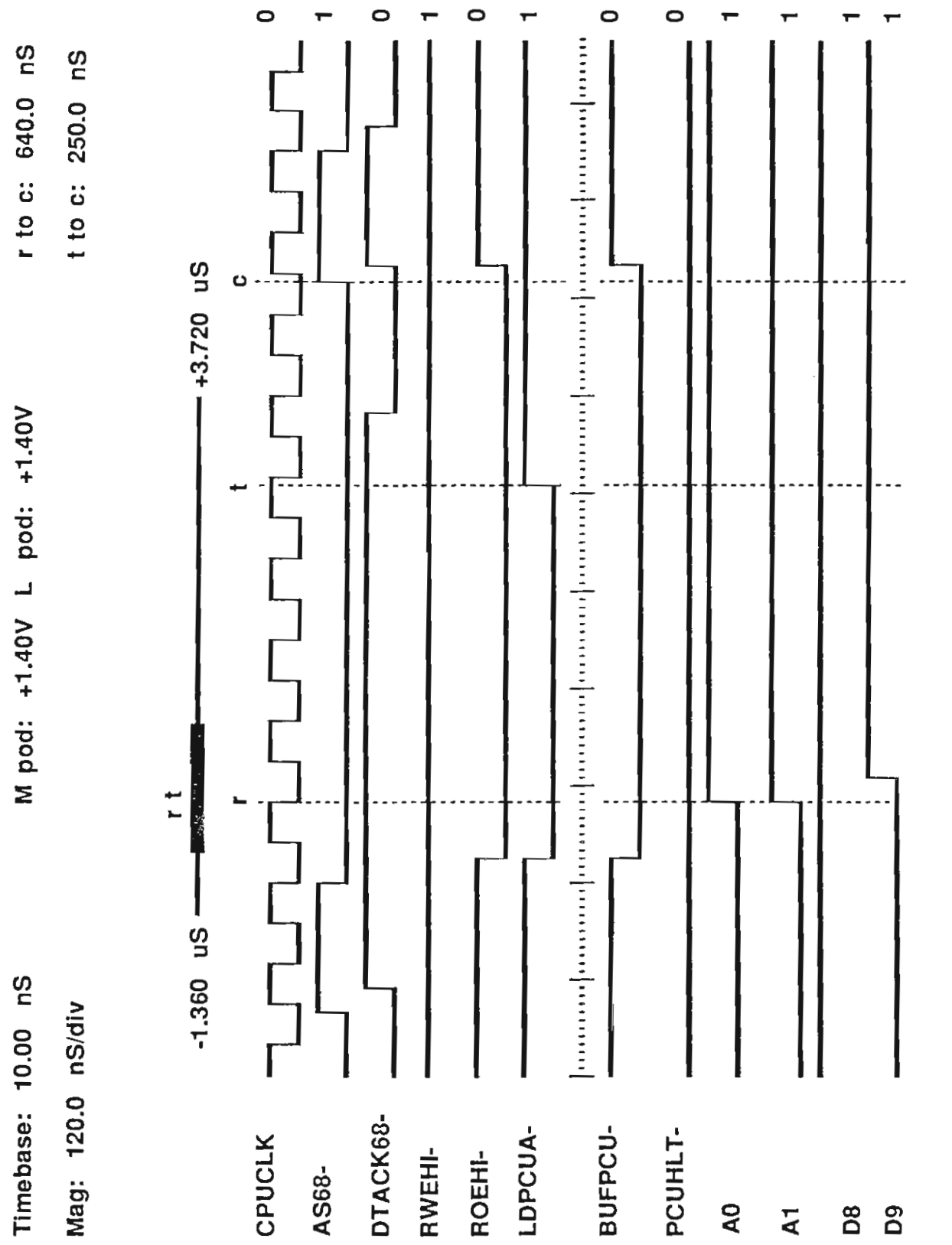
1772 READ


Timebase: 10.00 nS
Mag: 240.0 nS/div
M pod: +1.40V
L pod: +1.40V
r to c: 140.0 n
c to t: 270.0 nS
-26.66 uS
+46.83 uS
68AS-
DSKA0
DSKA1
CS
RW
0
1
0
0
0

1772 WRITES


Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V L pod: +1.40V
r to c: 570.0 nS
t to c: 310.0 nS
-1.360 uS
+3.720 uS
r t
0
r
t
c
CPUCLK
AS68-
DTACK68-
ROEHI-
LDPCUA-
BUFPCU-
PCUHLT-
A0
A1
D8
D9
1
1
0
1
0
1
0
1
1
1
1
PCU RAM READ


Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V L pod: +1.40V
c to r: 260.0 nS
c to t: 80.00 nS
-1.360 uS
tr
c
r
+3.720 uS
CPUCLK
AS68-
DTACK68-
RWEHI-
ROEHI-
LDPCUA-
BUFPCU-
PCUHLT-
A0
A1
D8
D9
0
1
1
1
0
0
0
0
0
1
0
PCU RAM WRITE


Timebase: 10.00 nS
Mag: 120.0 nS/div
M pod: +1.40V L pod: +1.40V
r to c: 640.0 nS
t to c: 250.0 nS
-1.360 uS
+3.720 uS
r t
r
t
c
CPUCLK
AS68-
DTACK68-
RWEHI-
ROEHI-
LDPCUA-
BUFPCU-
PCUHLT-
A0
A1
D8
D9
0
1
0
1
0
1
0
1
0
1
1
1

PCU RAM READ

B Mnemonics

Appendix B lists the main signal and bus line mnemonics used on the controller board schematic, and gives a description of each. Refer to this list when reading the circuit description or when troubleshooting UniSite.

Bus/line Mnemonic	Description
68K	68000 CPU control bus
ADR/CNT	Strobe used to latch control and address information in PCU
AEN	Address enable; signal latching address to pin logic chips
AGND	Sense line for ground at PSM/FSM
AS	Buffered address strobe from 68K
AS68	Address strobe directly from 68K
BERR	Bus error signal to 68K
BGACK	Bus grant acknowledge from DMA peripheral
BUFENA	Buffer enable for 68K data bus
BUFPCU	PCU RAM buffer
CMPF	Compare line from PSM bus
CSFLPY	Floppy controller (1772) select
CSSER	68681 DUART select
CSWFBD	Chip-select line for waveform board
DAT/DLY	Strobe signal used to latch data and delay information in PCU.
DCHG	Disk change signal from floppy disk
DIRIN	Floppy disk step direction
DRDY	Floppy disk ready
DSKRST	Floppy disk reset
DSKEOJ	Disk end-of-job interrupt
DSKDRQ	Disk data request interrupt
DTACK	Data acknowledge to the 68K
DUTVCC	Device-under-test (DUT) Vcc
EEWR	EEPROM write strobe

EHELLO	Expansion board insertion/removal interrupt
EVOKE	Instruction cycle execution signal in PCU
EXPINT	Expansion board interrupt
FAST	Fast/slow delay select in PCU
FCHC	Fine-current high clamp
FCLC	Fine-current low clamp
FCHR	Fine-current high rail (used by pin driver)
FCLR	Fine-current low rail (used by pin driver)
FHELLO	FSM insert/removal interrupt
FPD	FSM pin driver bus
FSMAS	FSM addr strobe from 68K
FSMDTK	FSM data acknowledge to 68K
FSMINT	FSM interrupt to 68K
HLOENA	Insert/removal interrupt disable/enable
HLT68	68000 halt
INCADR	PCU instruction address increment
INDEX	Index pulse from floppy disk drive
IPD	Internal pin driver bus
IRQ681	Interrupt request from 68681 DUART
LATCHP	Latch output signal to PSM, used to transfer serial data to LEDs and relays
LDS	Buffered lower data strobe from 68K; indicates D0-D7 are being used.
LDS68	Lower data strobe direct from 68K.
LDPCUA	Load PCU address
LSIF	Serial output data to FSM, used to initialize virtual address to pin logic chips
LSII	Serial output data to IPD bus, used to initialize virtual address to pin logic chips
LSOI	Serial input data from IPD bus (pin logic chips)
MA0-MA7	Memory address bits 0-7 to DRAM
MOTON, MOTORON	Motor-on signal to floppy disk drive
OCINT	Overcurrent interrupt from Waveform board to 68K
OCTRIP	Overcurrent trip-line from Pin Driver boards to the waveform board (2.5V threshold point)
OVCENA	Overcurrent interrupt enable
OVERCUR	Overcurrent interrupt output
OVERIDE	Override diskette write-protection
PCUDLY	Write strobe from 68K, used to load the 12-bit slow-delay counter in the PCU
PCUENA	PCU interrupt enable
PCUHOLD	Hold signal from PCU instruction decoder to counters.
PCUINT	PCU interrupt
PCURST	PCU reset
PCUS0, PCUS1	PCU serial data shift register's direction select lines
PD	Pin driver bus
PGND	Programming ground; the high-current ground for programming supplies
PHELLO	PSM insert/removal interrupt

PUP1	Pullup resistor 1
PUPALY	Pullup resistor to sense-line relay control flip/flop
RAM	RAM data
RDATA	Read data from floppy disk
RDDUT	Read device-under-test's (DUT's) data
RDINT	Read interrupt status
RDMISC	Read LSO, SODAT, PCU and disk status
RDPCUA	PCU address readback
RDSER	Read serial status
RDSHFT	Read shift register
REFACK	Refresh acknowledge
REFCAS	Refresh column-address strobe
REFRAS	Refresh row-address strobe
ROEHI	Output enable (high-order) to PCU RAM
ROELO	Output enable (low-order) to PCU RAM
RST68	68000 reset
RTCINT	Real-time clock interrupt enable
RWEHI	Write enable (high-order) to PCU RAM
RWELO	Write enable (low-order) to PCU RAM
RXRDY	Receiver-ready interrupt from 68681 to the 68000
SCLKF	Serial clock to FSM: used for LEDs, relay, ID, shift data clock
SCLKP	Serial clock to PSM: used for LEDs, relay, ID, shift data clock
SIDATP	Serial data sent to PSM, LEDs and relays
SIDATF	Serial data sent to FSM, LEDs and relays
SIDE, SIDE1	Side-select signals to disk drives
SODATF	Serial data from FSM: identifier code
SODATP	Serial data from PSM: identifier code
STEP	Floppy disk's step-to-next-cylinder signal
STRT, STRTPCU	Start PCU signals
TRK0	Track zero indicator from floppy disk
TSTCLR	GenRad test input, used to clear PCU counters.
UDS	Buffered upper data strobe from 68K
UDS68	Upper data strobe direct from 68K
VCS	Virtual chip select from PCU to pin driver bus
VPA68	Valid peripheral address, also used for auto-vector interrupt acknowledge
WRDATA	Write data to floppy disk
WRDSK	Write strobe for disk-control signals
WRGATE	Floppy disk write enable
WRLED	Write strobe for LEDs and interrupt enable latches
WRMISC	Write strobe for setup clocks, data and control
WRPROT	Write-protect status from floppy disk
WRRELAY	Write strobe for FSM/PSM sense relay
XAEN	Address enable signal to FSM and internal pin driver bus
XPCLK	Clock signal used for generating device-under-test (DUT) processor clock or structured test clocks

XRCLK	Receive DUT data latch signal
XVCS	Virtual chip select signal to FSM and internal pin driver bus

C Schematics

The following schematics are included in this Appendix.

Description	Part Number
Waveform Board	30-701-2011
Controller Board (First Version)	30-701-2012
Controller Board (Second Version)	30-701-2313
Site 28/40/48 Board	30-701-2021
PinSite Board	30-701-2230
SetSite Board	30-701-2016
ChipSite Board	30-701-2042
Expansion RAM board	30-701-2114