DATA I/O

Model 60 Logic Programmer Maintenance Manual

DATA I/O Corporation

MODEL 60A AND MODEL 60H LOGIC PROGRAMMERS

Maintenance Manual

972-0026-002 *August 1988*

Data I/O Corporation warrants to the original purchaser of the product described by this manual that the product was fully functional to the extent of its specification at the time of shipment from the factory. Data I/O further certifies that the equipment used to test the product was calibrated to standards that are traceable to the National Bureau of Standards as appropriate.

ORDERING INFORMATION

When ordering this manual, use Part Number 972-0026-002.
Applies to: Engineering Part No. 901-0005-016 and up.

SAFETY SUMMARY

General safety information for operating personnel is contained in this summary. In addition, specific WARNINGS and CAUTIONS appear throughout this manual where they apply and are not included in this summary.

DEFINITIONS

WARNING statements identify conditions or practices that could result in personnel injury or loss of life.

CAUTION statements identify conditions or practices that could result in damage to equipment or other property.

SYMBOLS

 This symbol appears on the equipment and it indicate that the user should consult the manual for further detail.

V~ This symbol stands for V AC. For example, 120 V~ = 120 V AC.

 This symbol stands for fuse ratings.

 This symbol denotes a ground connection.

QUALIFIED SERVICE PERSONNEL

This manual contains instructions to be performed by qualified service personnel only. To avoid personal injury do not perform any servicing instructions unless you are qualified to do so.

POWER CORD

Use only the power cord specified for your equipment.

GROUNDING THE PRODUCT

The product is grounded through the grounding conductor of the power cord. To avoid electric shock, plug the power cord into a properly wired and grounded receptacle only. Grounding this equipment is essential for safe operation.

SERVICING

To reduce the risk of electric shock, do not perform any servicing other than that described in this manual.

Voltage transients can destroy devices installed in the sockets. Be sure that power is OFF before inserting devices into the programming sockets.

POWER SOURCE

Check the voltage selector in the power cord receptacle to verify that the equipment is configured for the appropriate line voltage. The programmer can be damaged if operated at the wrong voltage seting.

FUSE REPLACEMENT

For continued protection against the possibility of fire, replace only with a fuse of the specified voltage, current and type ratings.

DEVICE HANDLERS

Refer to the appropriate Handler manual for instructions before attempting to operate or service the device handler.

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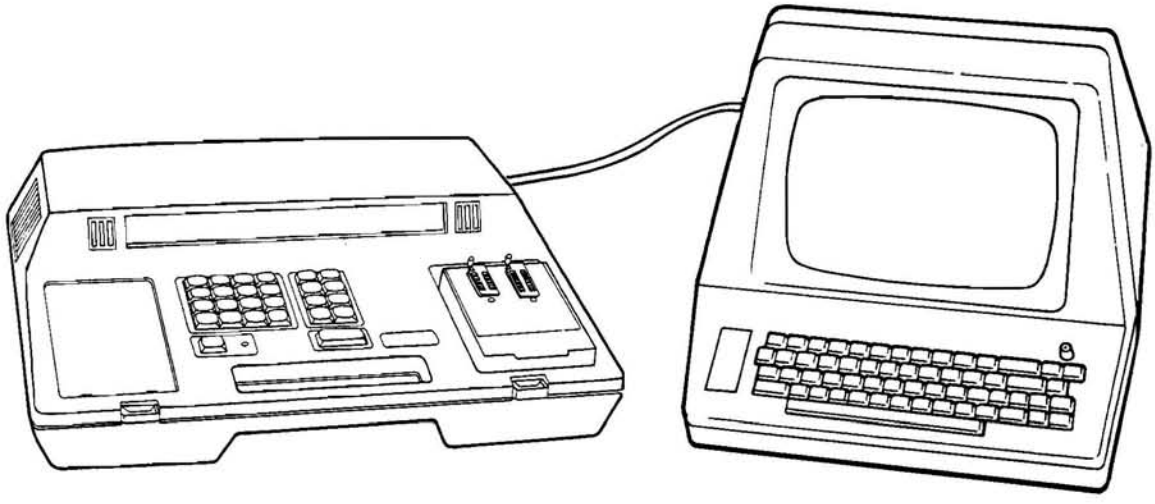
1. INTRODUCTION

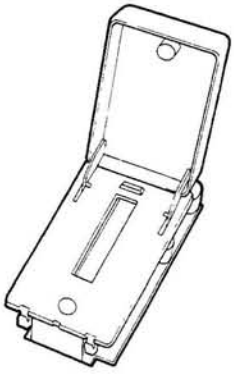
1.1 PRODUCT DEFINITION

Data I/O's Model 60 provides the user reliable and versatile programming of Programmable Logic Devices (PLDs) and Erasable Programmable Read Only Memory devices (EPROMs). Individual programming adapters allow you to select the specific device support you need from a wide variety of PLDs and memory devices. Standard features of the Model 60 include RS-232C port, menu scrolling, approved speed-optimized algorithms, and Computer Remote Control (CRC). The Model 60 offers the Full and Kernel JEDEC translation formats for logic devices and seven other translation formats for memory devices. You may also choose the line voltage and the programming adapters.

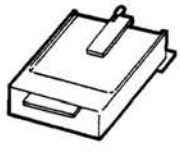


MODEL 60A PROGRAMMER

REMOTE CONTROL



OPTIONAL UV LAMP ASSY



OPTIONAL PROGRAMMING ADAPTER

095-0101-001

*Terminal not included

1.2 HOW TO USE THIS MANUAL

This manual contains maintenance information for the Model 60 Logic Programmer with either a logic or memory programming adapter installed. If you have one of the logic adapters installed, or no adapter installed, the Model 60 will respond in logic device mode. If a memory adapter is installed, the Model 60 will respond in memory device mode.

Listed below are descriptions of the remaining sections in this manual.

- INTRODUCTION (Section 1) — Includes a product definition, a description of the manual, a system overview, a list of optional features, programmer specifications, and customer information.
- INSTALLATION (Section 2) — Includes instructions on line voltage selection and checking the back panel fuses, powering up the programmer, inserting a device, programming a socketed logic or memory device, installation of the optional UV lamp, and installation of the Exatron, MCT, and Model 300 handlers.
- THEORY OF OPERATION (Section 3) — Contains the overall and block diagram level circuit description of the boards and adapters used with the Model 60 Logic Programmer.
- MAINTENANCE (Section 4) — Includes preventive maintenance instructions for operator care and cleaning of the programmer plus assembly and disassembly instructions for the removal of assemblies for repair or replacement.
- CALIBRATION (Section 5) — Contains the calibration procedures and measurement chart required to calibrate the Model 60 programmer.
- TROUBLESHOOTING (Section 6) — Contains troubleshooting procedure, error codes, and troubleshooting chart required to perform corrective maintenance (troubleshooting) on the programmer.
- INDEX — An alphabetical guide to all the major topics covered in the manual.

1.3 SYSTEM OVERVIEW

The Model 60 is a transportable programmer that provides a fully integrated means of programming, testing, and verifying a variety of logic and memory devices, depending on the adpater that is installed.

1.3.1 Remote Control

The standard Computer Remote Control (CRC), controls the Model 60 with a host computer. Terminal mode allows you to send commands to the Model 60 from a terminal. (See the Remote Control section of this manual for descriptions of the terminal menus and terminal mode operation).

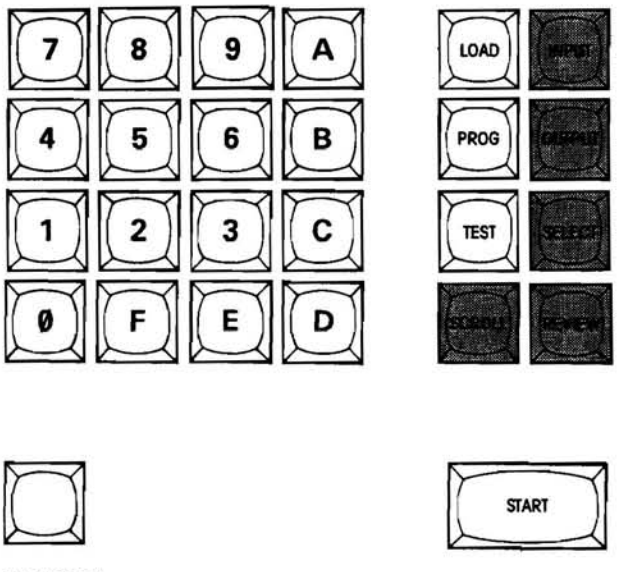
1.3.2 Model 60 Front Panel Description

NOTE

The following describes the front panel keys of the Model 60. The sections in this manual on "Programming With Logic Adapter" and "Programming With Memory Adapter" describe the Model 60 responses when programming with a logic or memory device.

Front panel operation of the Model 60 is provided by a set of three Mode (blue) keys: **LOAD**, **PROG** and **TEST**. These are used in conjunction with several function keys (see figure) and a hexadecimal keyboard. The following diagrams show the basic function of the **LOAD**, **PROG**, **TEST**, **INPUT**, **OUTPUT** and **SELECT** keys.

Hex Keyboard:
Allows entry of hexadecimal values.



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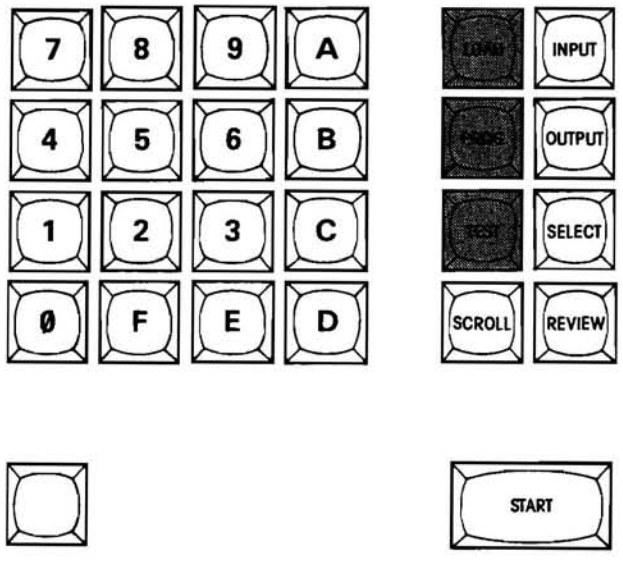
Mode Operation Keys

LOAD key:
Used to read device information and store it in the programmer's memory (RAM).

PROG key:
Used to program and selectively test a device installed in the adapter.

TEST key:
Used to compare the device information with the information stored in the programmer's RAM. For logic devices, this may include a functional test of the device if "structured test vectors" are present in RAM and/or if Logic Fingerprint is enabled.

Hex Keyboard:
Allows entry of hexadecimal values.



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START key:
Used to initiate the function selected on any of the other keys or to advance through a multiple step operation

INPUT key:
Used to receive input from the serial I/O port, translate it, and store it in the programmer's RAM.

OUTPUT key:
Used to transmit data stored in the programmer's RAM, translate it, and send it out the serial I/O port.

SELECT key:
Used in conjunction with the entry of a two-character command code to select any of the programmer functions.

REVIEW key:
Used in conjunction with the SCROLL key to allow reverse scrolling through the menus. This key can also convert the display of manufacturer and part type to family and pinout code.

SCROLL key:
Used to advance through the menus or prompts on the programmer display.

1.3.3 Specifications

The Model 60's specifications are listed below.

1.3.3.1 Functional Specifications

- Programming Support: 360A-001, 360A-002, 360A-003 and 360A-005 programming adapters
- Keyboard: 16-key hexadecimal, 10-key functional
- Display: 16-character alphanumeric
- Input/Output: Serial RS-232C
- Baud Rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19,200 (software selectable)
- Remote Control: Computer Remote Control (CRC)
Terminal Mode
- Translation Formats: JEDEC Full, JEDEC Kernel, ASCII-Hex Space STX, Motorola EXORciser, Intel Intellec 8/MDS, Tektronix Hexadecimal, Extended Tektronix Hexadecimal, Motorola EXORmax, Intel MCS-86 Hex Object.

1.3.3.2 Power Requirements

- Operating Voltages: 100, 120, 220 or 240 Vac ± 10%
- Frequency Range: 48-63 Hz
- Power Consumption: 100W maximum, 125 VA maximum
- Fuse Protection: Primary and secondary fuse protection

1.3.3.3 Physical And Environmental

- Dimensions: 34 x 43 x 11 cm (13.5 x17.0 x4.5 in.)
- Unit Weight: 7.3 kg (16 lbs)
- Operating Temperature: + 5° to 45°C (41° to 113° F)
- Storage Temperature: - 40° to 70°C (- 40° to 140°F)
- Humidity: to 80% noncondensing
- Operational Altitude: to 3 km (10,000 ft.)

1.3.3.4 Safety

The Model 60 is designed to comply with the following safety standards.

- UL 1244 (Underwriters Laboratories)
- CSA C22.2 NO. 151 (Canadian Standard Association)
- IEC 348 (International Electrotechnical Commission)

1.4 OPTIONAL FEATURES

The Model 60 offers the following optional features. If you wish to purchase any of these features, contact your nearest Data I/O sales representative.

- 20/24-pin PLD: 360A-001
- 20/24-pin integrated fuse logic: 360A-002
- 28-pin integrated fuse logic: 360A-003
- 28/32/40-pin memory: 360A-005
- 20/28-pin PLD PLCC (JEDEC): 360A-006
- 28/28-pin PLD PLCC (non-JEDEC): 360A-007
- 20/28-pin integrated fuse logic PLCC: 360A-0082
- 28-pin integrated fuse logic PLCC: 360A-009
- Ultraviolet lamp assembly: 950-0211

1.5 ORDERING

Orders made with Data I/O must contain the following information:

- description of the equipment
- quantity of each item ordered
- shipping and billing address of firm, including ZIP code
- name of person ordering equipment
- purchase order number
- desired method of shipment

1.6 WARRANTY AND CUSTOMER SUPPORT

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year, unless specified otherwise, begins when you receive the equipment. Refer to the warranty card inside the back cover of this manual for information on the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Customer Support Center.

Data I/O maintains customer support centers throughout the world, each staffed with factory- trained technicians to provide prompt, quality service. This includes repairs, calibration, updates and upgrades of all Data I/O products. A list of all Data I/O Customer Support Centers is located in the back of this manual.

2. INSTALLATION

This section explains how to prepare your Model 60 programmer for operation. Included are procedures to power up the programmer, to program a logic device and a memory device from the programmer's keyboard, to install the optional UV unit, and to install the handlers available for the Model 60H. For details on operating the programmer using a terminal or computer refer to the Operator's Manual.

This section includes the following procedures:

- Dust Cover Removal
- Power Connection
- Verify/Change the Line Voltage and Line Fuse
- Programming Adapter Installation
- Programmer Power Up
- Logic Adapter Sample Programming Session
- Memory Adapter Sample Programming Session
- Optional UV Unit Installation
- Handler Installation (Model 60H only)

2.1 DUST COVER REMOVAL

Use the following procedure to gain access to your Model 60 programmer and its component pieces by removing the programmer's protective dust cover.

1. Orient the case so that the handle is facing you.

2. With your thumbs, push in on the cover release tabs as shown in the figure 2-1a.

3. Lift up on the dust cover lid about 2 inches, pulling it toward you, and Remove it from the programmer (figure 2-1b).

4, Set the cover on a flat surface upside down for access to the accessories stored in the dust cover (figure 2-1c).

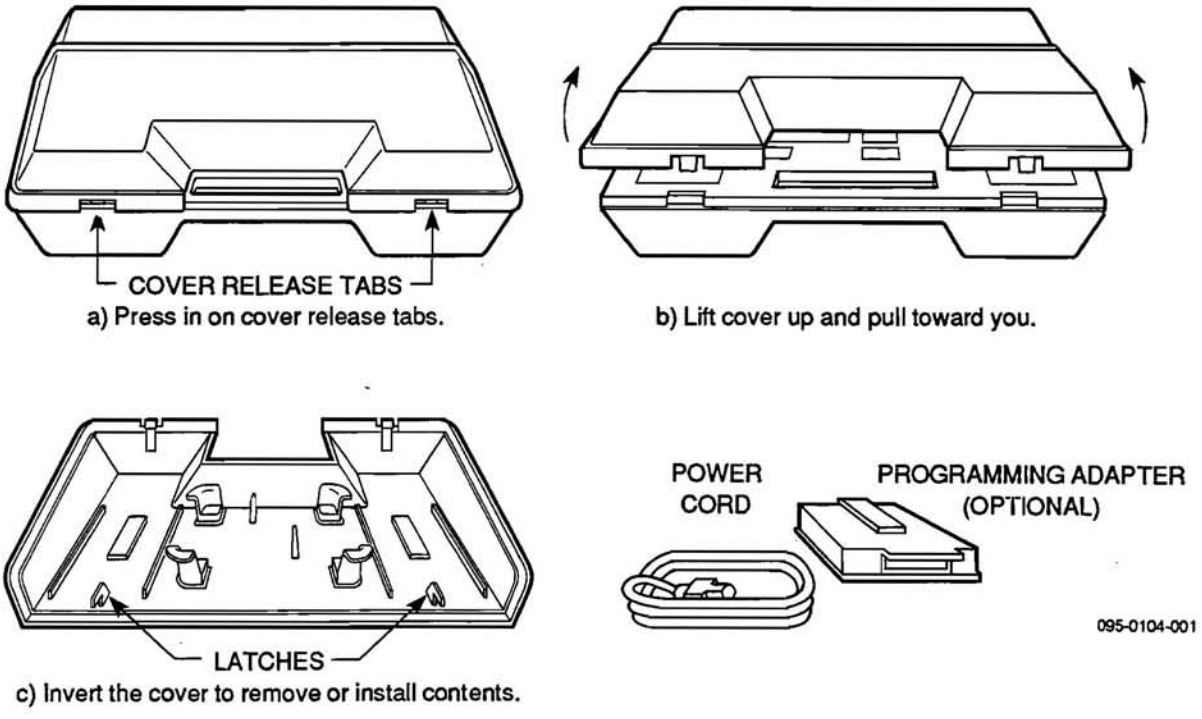


Figure 2-1. Removing the Dust Cover

2.2 POWER CONNECTION

Before applying power to your programmer, make sure that the line voltage selection is correct, that the line fuse is intact, and that the unit is properly grounded. When you have set and/or verified the above, proceed to the next subsection, Programming Adapter Installation.

2.2.1 Verifying/Changing the Line Voltage

The factory has selected the proper voltage according to your specification. A voltage reading is visible through a window in the door that covers the voltage selector wheel, located on the back panel, as shown in the figure. This voltage should be the same as the line voltage on which the machine will operate. If the voltage that appears in the window is incorrect, change the operating voltage according to the following procedure.

CAUTION

This instrument may be damaged if operated with the wrong line voltage.

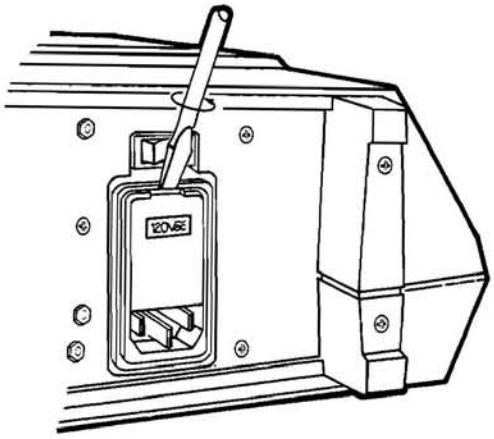
The procedures to verify and/or change the operating voltage are described here and illustrated in figure 2-2.

1. Disconnect the power cord.
2. Gently pry open the door that covers the voltage wheel selector with a flat-blade screwdriver.
3. Pull the voltage wheel selector out of its slot.
4. Rotate the selector until the correct operating voltage points toward you.
5. Insert the selector back into its slot.

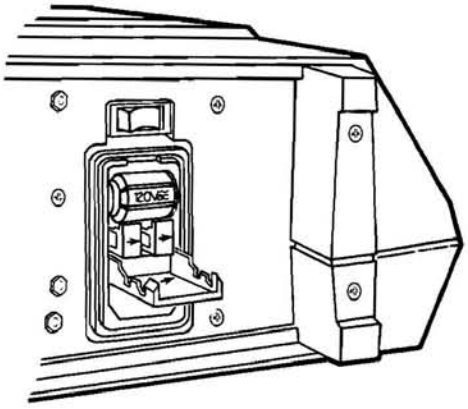
NOTE

If you wish to access the line fuse at this point, proceed to step 2 in the Verifying/ Replacing the Line Fuse procedure.

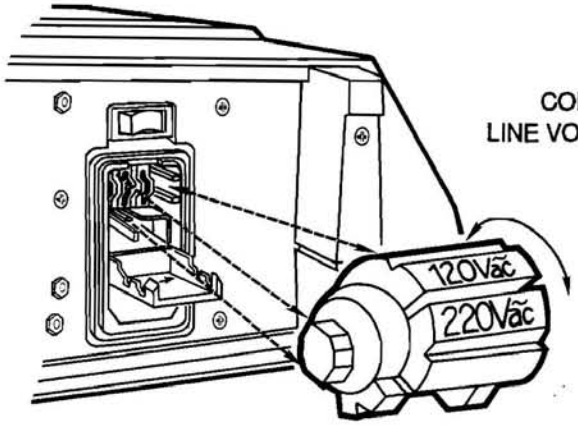
6. Snap the door closed.
7. The correct voltage reading will now appear in the window.



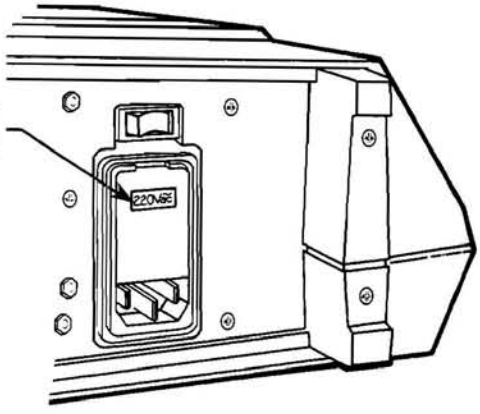
Open door.



Pull wheel out of its slot.



Rotate wheel so that the correct line voltage points toward you.



Correct line voltage setting.

NOTE: Changing the operating voltage may require a change in fuse value.

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Figure 2-2. Changing the Line Voltage

2.2.2 Verifying/Replacing the Line Fuse

The line fuse is located behind the same door that covers the voltage wheel selector. Perform the following procedure to verify that the line fuse is correct and intact. In the event that the fuse is blown, replace it with one of the correct size. Procedure steps are illustrated in figure 2-3.

1. Gently pry open the door that covers the fuse holder using a flat-blade screwdriver.

NOTE

There are two fuse receptacles; only the one on the right is connected to the programmer's circuitry. The left receptacle is a spare fuse tray. See the next subsection for more information on this spare tray.

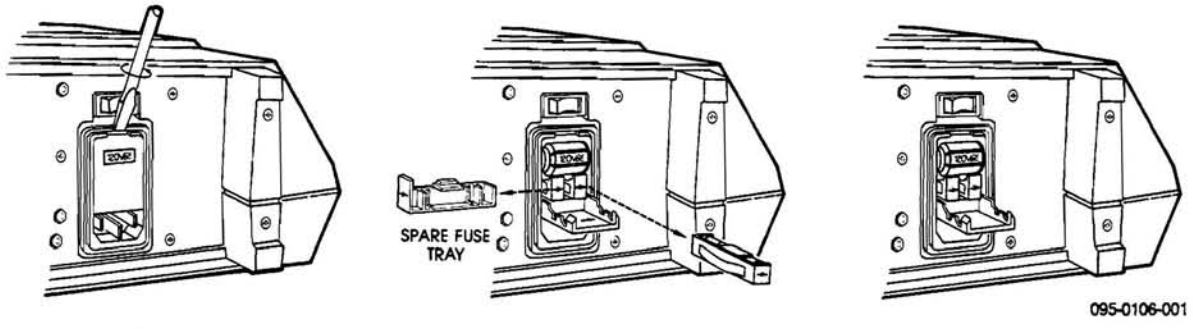


Figure 2-3. Replacing the Line Fuse

2. Pull the right fuse holder out of its slot.

3. Check to determine whether the fuse is intact. If it is intact, proceed to step 4. If it is blown, install a new fuse. See table 2-1 for line fuse ratings.

CAUTION

For continued protection against the possibility of fire, replace only with a fuse of specified voltage, current and type ratings.

4. Insert the fuse holder into its slot so that the arrow on the fuse holder points in the same direction as the arrows on the door.

5. Snap the door closed.

Table 2-1 Line Fuse Rating

Operating Voltage	Current	Voltage	Type	Data I/O Part Number
100	1.5A	250V	Fast-blow	416-0005
120	1.5A	250V	Fast-blow	416-0005
220	0.8A	250V	Fast-blow	416-1550
240	0.8A	250V	Fast-blow	416-1550

2.2.3 Spare Line Fuse Tray

All Model 60 programmers are equipped with two line fuse trays (see the previous figure). The white fuse tray accepts 1/4 x 1 1/4 inch fuses; the black tray accepts 5 x 20 millimeter fuses, commonly available in Europe. Only the right fuse receptacle is connected to the programmer's circuitry.

2.2.4 Grounding the Unit

The Model 60 is shipped with a three-wire power cable. This cable connects the chassis of the unit to the earth ground when the cable is connected to a three-wire (grounded) receptacle.

WARNING

Continuity of the grounding circuit is vital for the safe operation of the unit. Never operate this equipment with the grounding conductor disconnected.

2.3 PROGRAMMING ADAPTER INSTALLATION

Programming operations require the use of the correct adapter. Any of the adapters may be installed and be removed with the programmer's power on; this feature allows you to retain data in the Model 60 RAM when changing programming adapters.

CAUTION

Voltage transients can cause device damage. Be sure that all sockets are empty when switching power on or off or installing or removing an adapter.

To install an adapter into the Model 60, refer to figure 2-4 and follow this installation procedure.

1. Orient the adapter over the front panel socket receptacle.
2. Tilt the adapter down and slide into receptacle and push forward.
3. Push the adapter wing handle down so that the adapter connector mates with the receptacle connector.

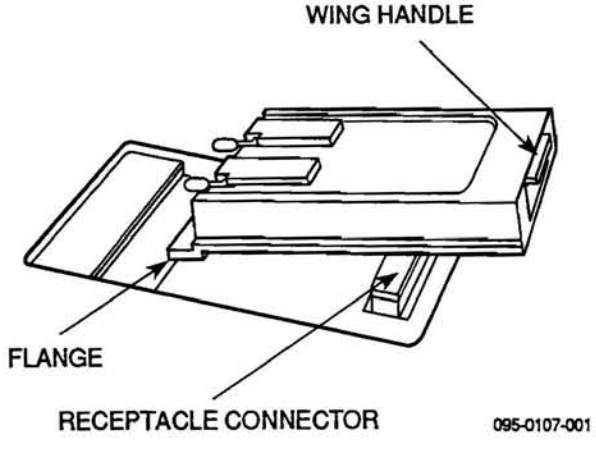


Figure 2-4. Installing a Programming Adapter

2.4 POWERING UP

Use the following procedure to apply power to your Model 60 programmer.

1. Check to make sure the sockets are empty. If a device is in a socket, remove it.

   NOTE

   If a device is in a socket, lift the socket lever and lift the device out of the socket. Failure to remove the device could result in damage to the device.

2. Check to be sure the voltage selector is in the proper position. Plug the AC power cord into the rear of the programmer and into a power receptacle.

3. Press the power switch at the back of the programmer to the "ON" position (see figure 2-5).

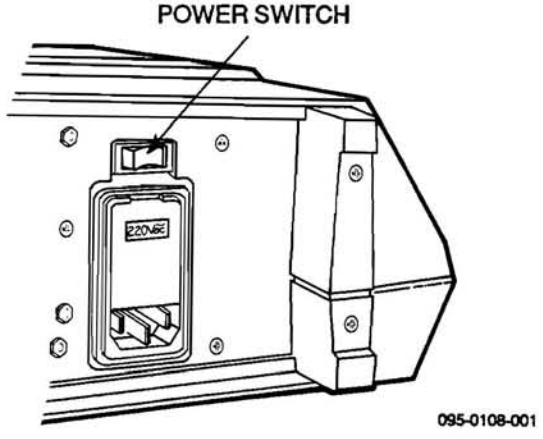


Figure 2-5. Power ON Switch

When the programmer is powered up, it automatically performs the self-test routine, which initializes the programmer's hardware and checks system memory. While the self-test is being performed, the programmer will display

```
SELF  TEST  ⊗
```

The symbol at the right-most digit of the display is the "action symbol," which "rotates" when the programmer is performing an operation.

When the self-test has been successfully completed, the programmer will display

```
SELF  TEST - OK
```

If an error message is displayed, check the error codes in the Troubleshooting section of this manual.

2.4.1 Sample Programming Section For Logic Operation

The following steps describe how you would program a logic device using a master device (a part that has been previously programmed and is used as a "master"' to program other parts). This procedure assumes that the programming data has already been created (using a development system) and transferred to the master device. For more details on logic device programming, see the "Programming With Logic Adapter" section of the Operator's Manual. Information about operating in Terminal mode and the associated menus are in the Remote Control section of the Operator's Manual.

CAUTION

The Model 60 response in the following procedure assumes that the appropriate logic adapter for the device to be programmed is installed.

1. Plug power cord into the programmer and into a power receptacle.
2. Make sure all the device sockets are empty.
3. Power-up the programmer and wait for display

   ```
   SELF TEST – OK
   ```

4. Install the appropriate logic adapter.
5. Press **LOAD**

   to prepare the programmer to transfer the master device data to the programmer's data RAM.

   The programmer will display

   ```
   LOAD  (mfg)  (dev)
   ```

   or

   ```
   LOAD   FXX   PXX
   ```

6. Enter **X X Y Y**

   the family/pinout code for the last device saved or choose a device. Refer to the User Note for correct family and pinout codes. The programmer will then display

   ```
   LOAD  (mfg)  FXX ^ PYY
   ```

7. Lift up the lever on the socket that has an illuminated LED below it (see figure 2-6). Line up pin 1 of the device so that it is nearest the lever and set the device into the socket. Press down on the lever to lock the device in place.

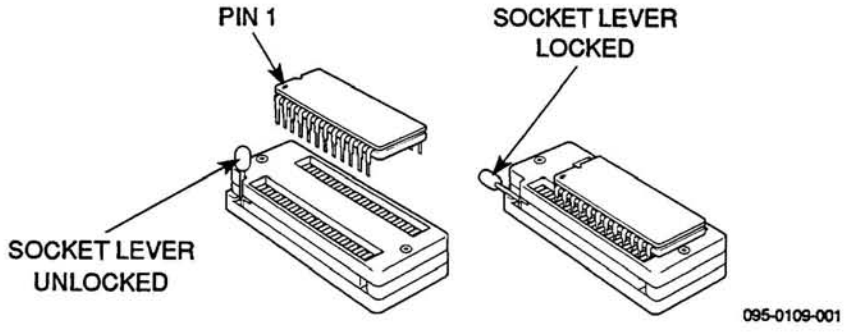


Figure 2-6. Loading a Device in the Logic Programming Socket

8. Press **START**. During the operation, the programmer will display

   `LOAD ARRAY (mfg) ⊗`

   If Logic Fingerprint is enabled, the display will then read

   `LEARN FPRINT ⊗`

   When the operation is complete, the programmer will display

   `LOAD DONE XXXX`

   NOTE

   "XXXX" is the sumcheck of the device.

9. Lift up the socket lever and remove the master device from the socket. The master device data is now transferred to RAM. The next part of the procedure transfers that data to a blank device.

10. Press **PROG**

    to prepare the programmer to transfer the data to the blank device. The programmer will display

    ```
    PROG  (mfg)  (dev)   **
    ```

    NOTE

    The device shown on the display may not match the one being programmed since family and pinout codes are unique. Select proper Family/Pinout for device to be programmed.

11. Line up pin 1 of the blank device so that it is nearest the lever and set the device into the socket. Press down on the lever to lock the device in place.

12. Press **START** . The programmer will display

    ```
    ILLEGAL BIT CHK  ⊗
    PROG ARRAY (mfg) ⊗
    TEST ARRAY (mfg) ⊗
    TEST FPRINT              (If Logic Fingerprint is enabled, this line will appear)
    PROG DONE     XXXX
    ```

    NOTE

    "XXXX" in the above display represents the device's sumcheck; the hexadecimal sum of all the bytes in the device. The number displayed should match the sumcheck displayed during step 8 of this procedure.

13. Lift up the socket lever and remove the device from the socket. The device is now programmed.

14. To program another device of the same type, simply place it in the socket, press down on the socket lever and press **START**.

2.4.2 Sample Programming Section For Memory Operation

The following steps describe how you would program a memory device using a master device (a part that has been previously programmed and is used as a "master" to program other parts). This procedure assumes that the programming data has already been created (using a development system) and transferred to the master device. For more details on memory device programming, see the "Programming With Memory Adapter" section of this manual. Information about operating in Terminal mode and the associated menus are in the Remote Control section of this manual.

1. Plug power cord into the programmer and into a power receptacle.

2. Make sure all the device sockets are empty.

3. Power-up the programmer and wait for display

   ```
   SELF  TEST – OK
   ```

4. Install the memory adapter.

5. Press **LOAD**

   to prepare the programmer to transfer the master device data to the programmer's data RAM.

   The programmer will display

   ```
   DEVICE ^ ADDR/SIZE
   ```

6. Press **START** . The programmer will display

   ```
   DEVICE  ADDR ^ SIZE
   ```

7. Press **START** . The programmer will display

   ```
   LOAD  RAM ^ ADDR
   ```

8. Press **START**. The programmer will display

   ```
   LD  FAM ^ XX  PIN ^ YY
   ```

   or

   ```
   LD  (mfg)  (dev)
   ```

9. Enter **X X Y Y**

   Either use the default family/pinout code or choose a device. Refer to the Operator Manual User Note for correct family and pinout code. The programmer will then display

   ```
   LD  FAM  XX  PIN ^ YY
   ```

10. Lift up the lever on the socket. Line the bottom pins of the device so that they are at the bottom of the socket (bottom justified) as shown in the figure 2-7. Set the device into the socket and press down on the lever to lock the device in place.

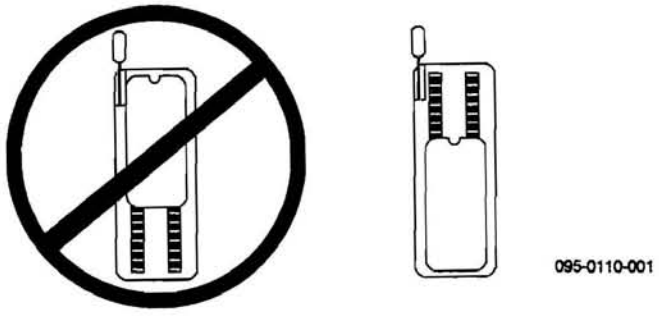


Figure 2-7.Loading a Device in the Memory Programming Socket

11. Press **START** . The programmer will display

```
LOADING   DEVICE  ⊗
LOAD DONE      XXXX
```

NOTE

"XXXX" is the sumcheck of the device.

The load operation could take from a few seconds to more than 60 seconds depending on the size of the device. Any audible sounds resulting from the relays in the memory adapter is normal.

12. Lift up the socket lever and remove the master device from the socket. The master device data is now transferred to RAM. The next part of the procedure transfers that data to the blank device.

13. Press **PROG**

to prepare the programmer to transfer the data to the blank device. The programmer will display

```
DEVICE ^ ADDR/SIZE
```

NOTE

The device shown on the display may not match the one being programmed since family and pinout codes are unique. Select proper Family/Pinout for device to be programmed.

14. Line up the bottom pins of the blank device so that they are at the bottom of the socket. Set the device into the socket and press down on the lever to lock the device in place.

15. Press **START** 3 times. The programmer will show the following displays

```
DEVICE   ADDR ^ SIZE
PROG   RAM ^ ADDR
PG   FAM ^ XX    PIN YY
```

or

```
PG   (mfg)   (dev)
```

16. Press **START**. The programmer will display

```
TEST   DEVICE ⊗
PROGRAM   DEVICE  ⊗
VERIFY   DEVICE   ⊗
PROG DONE      XXXX
```

17. Lift up the socket lever and remove the device from the socket. The device is now programmed.

or

If the device is pre-programmed, then the display will show

```
NON   BLANK    20
```

or

```
ILLEGAL   BIT  21
```

If the display shows ILLEGAL BIT, then the device must be erased or try a new device.

Press **START**. The programmer will display

```
PROGRAM   DEVICE  ⊗
VERIFY   DEVICE   ⊗
PROG   DONE    XXXX
```

NOTE

"XXXX" is the sumcheck of the device. Programming can take several minutes.

18. Lift up the socket lever and remove the device from the socket. The device is now programmed.

2.5 OPTIONAL UV LAMP INSTALLATION PROCEDURES

The Model 60's optional UV lamp assembly provides you with the capability of erasing programmed MOS EPROMS and erasable logic devices. This section explains use of the UV lamp.

2.5.1 Blank UV Cover Removal

WARNING

The instructions contained in this subsection are for qualified service personnel only. Do not attempt them unless you are qualified to do so.

This subsection explains how to remove the blank UV cover. This cover will need to be removed if you have purchased and wish to install the optional UV lamp assembly.

WARNING

To avoid the possibility of electric shock, disconnect the power cord before removing the blank UV cover. Keep the power cord disconnected until installation is completed.

To remove the cover, you will need a flatblade screwdriver or similar instrument. Use the following procedure to remove the cover.

1. Apply a firm downward pressure at the rear portion of the cover as shown in the figure.

2. While continuing the pressure at the rear of the cover, apply a slight rotational motion with the screwdriver inserted into each of the slots in turn (see figure 2-8). This releases the cover from the front panel.

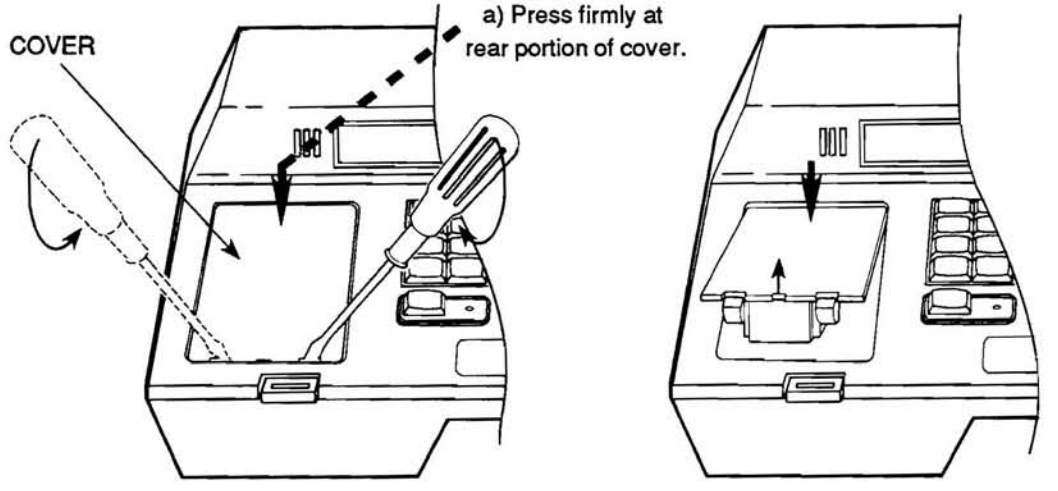
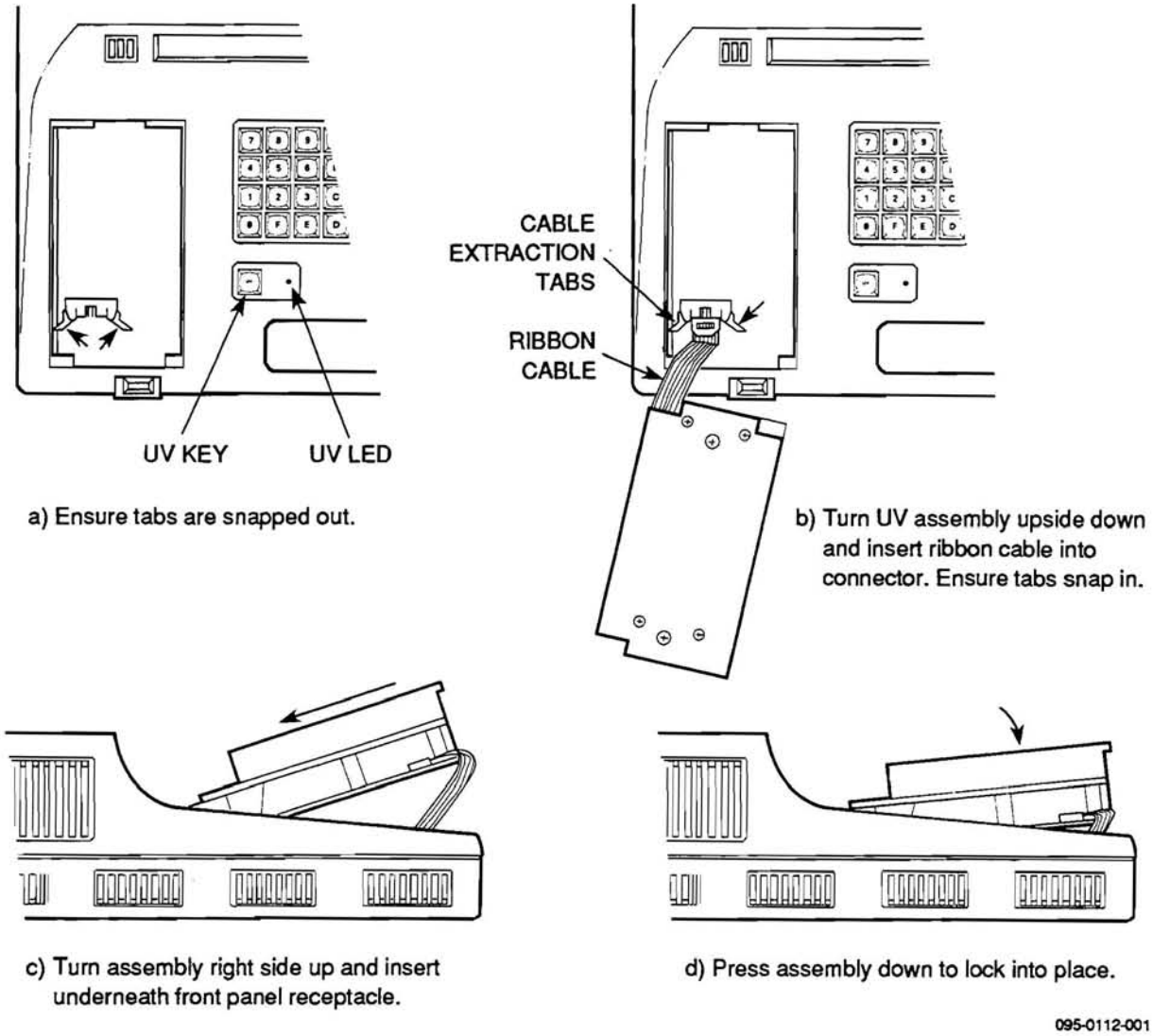


Figure 2-8. UV Cover Removal

2.5.2 UV Lamp Assembly Installation

To install the optional UV lamp assembly, perform the following procedure.

1. Remove the blank UV cover according to the instructions in the previous section.
2. Be sure that the cable extraction tabs on the controller board are snapped out (see figure 2-9).
3. Insert the ribbon cable (P204) into the connector (J204) on the controller board (see figure). Ensure that the tabs are now snapped in.
4. Tilt the UV lamp assembly down, placing the front end into the receptacle as shown in the figure.
5. Press the assembly down to lock it into place.



a) Ensure tabs are snapped out.

b) Turn UV assembly upside down and insert ribbon cable into connector. Ensure tabs snap in.

c) Turn assembly right side up and insert underneath front panel receptacle.

d) Press assembly down to lock into place.

095-0112-001

Figure 2-9. UV Assembly Installation

2.5.3 Erasing Device With Optional UV Lamp Assembly

2.5.3.1 UV Lamp Specification

The UV lamp intensity is rated at 7000μW/cm^2. Typically, EPROM device manufacturers recommend an erasure dose of 15W-sec/cm^2. This yields an erasure time of 35 minutes.

2.5.3.2 Procedure For Erasing EPROMS

To erase programmed devices, use the following procedure.

1. Open the UV lamp cover door by lifting the flange on the front edge as shown in figure 2-10.

2. With the device's lens facing down, place the device that you wish to erase on the UV tube (see figure 2-10).

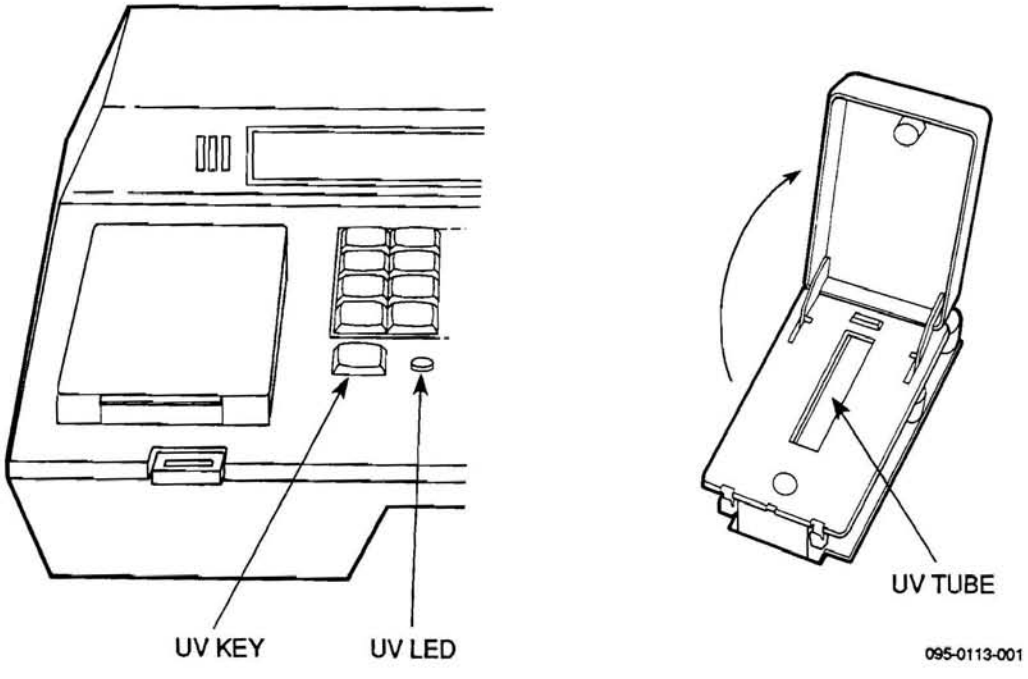


Figure 2-10. PROM UV Erasure Procedure

3. Enable or disable timeout (35 minute) using select code FD (UV timer set). Refer to the Select Code section of the Operator Manual for the exact sequence.

4. Close the UV lamp cover door. The magnetic catch will hold it closed.

5. Press the UV key, located on the Model 60's front panel. The UV LED should now illuminate, indicating erasure has begun. A lens located above the UV door indicates whether the lamp is on (see figure on previous page).

WARNING

Exposure to UV lamp radiation is harmful to eyes and skin. The UV lamp cover door closes on a sensor. If the door is opened during the erase cycle, the UV lamp will automatically switch off, preventing possible exposure to UV radiation. Do not defeat the purpose of the UV lamp cover door interlock sensor.

Touching the hot UV lamp tube could cause a burn. Avoid contact with the tube after it has been on.

NOTE

Pressing the UV key at any point in the procedure resets the programmer to the beginning of the erasure cycle. The UV lamp's on time is lengthened in conjunction with the other machine operations. The UV lamp cannot be turned on while other operations are in progress.

6. When the UV timeout expires, the UV LED turns off. The devices are now erased.

7. Open the UV lamp cover door and remove the devices.

2.6 HANDLER INSTALLATION (Model 60H only)

Handler interface kits are available for three different handlers, the MCT, Exatron, and Model 300. Instructions for installing the required equipment for each of the three handlers follows.

2.6.1 Exatron Handler Interface Installation

WARNING

The Instructions contained in this subsection are for qualified service personnel only. Do not attempt them unless you are qualified to do so.

CAUTION

Refer to the Exatron manual for detailed instructions and information on the handler before beginning this procedure.

Installing the adapter interface for use with the Exatron handler requires the following steps:

- Wire the sort category jumpers (if not already done)
- Install the adapter module and performance board
- Connect the control cable

2.6.1.1 Wiring the Sort Category Jumpers

Each time a device is programmed and tested, the Model 60H sends one of five sort category signals to the device handler. These sort categories are used by the Exatron handler to sort devices into bins. For example, all correctly programmed devices can be put into one bin, and all devices with an illegal-bit error can be put into another bin.

NOTE

Model 60H Sort conditions such as PASS, or FAIL are assigned sort categories from the Model 60H front panel.

Before you start programming with the handler, the Model 60H sort categories must be assigned to specific handler bins. To do this, wire the appropriate sort category jumpers on the handler.

The sort category jumpers are located on the front panel PCB #2500-058 directly above the 24-pin control connector (refer to figure 2-11). The white side panel must be removed to gain access to the jumpers.

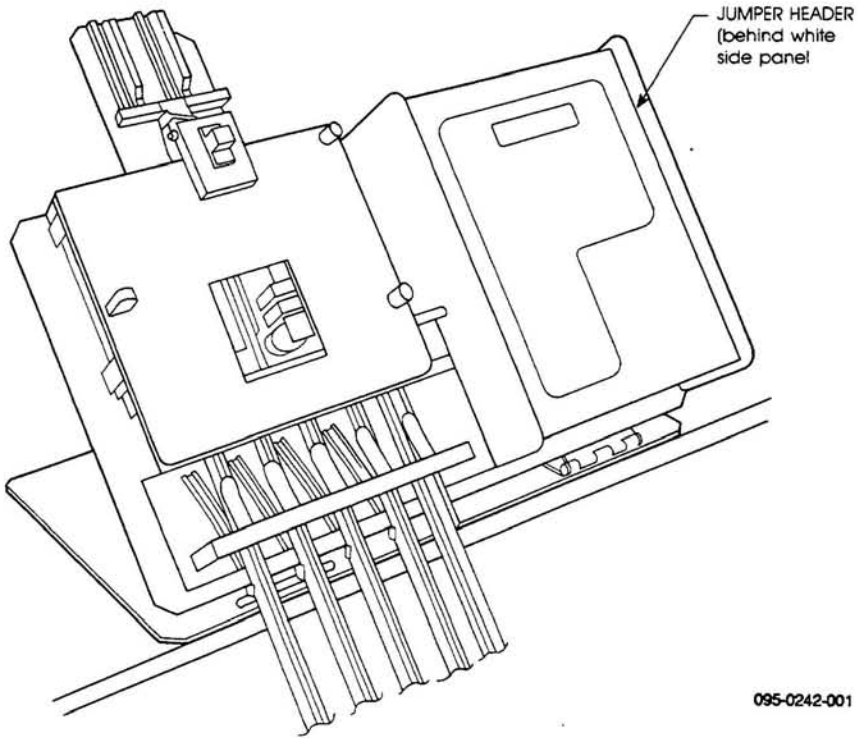


Figure 2-11. Location of the Exatron Sort Category Jumpers

Figure 2-12a shows a close-up of an unwired jumper header. As indicated, one side of the header corresponds to handler bins and the other side corresponds to sort categories. Wiring a sort category to a bin causes all devices in a category to be sorted into that bin.

Since the 60H has five sort categories and the Exatron handler has five sort bins, the most straightforward wiring is sort category 1 to bin 1, category 2 to bin 2, and so on, as shown in figure 2-12b. You can; however, wire any category to any bin. For example, you may want four pass bins and one bin for all error categories. This would be wired as shown in figure 2-12c. For more information, consult the Exatron technical manual.

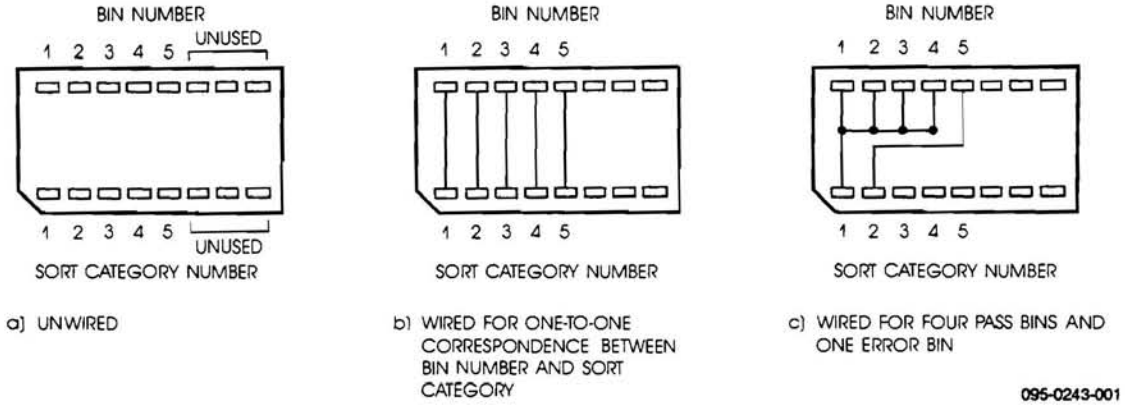


Figure 2-12. Exatron Sort Category Jumper Header

2.6.1.2 Installing the Adapter Module and Performance Board

Installing the interface adapter for use with an Exatron handler requires the following procedures:

- If required, install the performance board mounting brackets
- Install the adapter module into the Model 60H
- Connect the adapter module to the performance board
- Install the performance board onto the handler

Installing the Exatron Performance Board Mounting Brackets

The performance board is mounted to the Exatron handler via mounting brackets and Velcro strips. Use the following procedure to install the brackets and Velcro on the performance board and handler.

1. Locate the four screw holes on the Exatron side of the performance board (see figure 2-13).

2. Position the Exatron mounting brackets (P/N 415-1338) over the screw holes, and attach them to the performance board with the screws provided. Note that one bracket is taller than the other. Install them in the positions shown on figure 2-13.

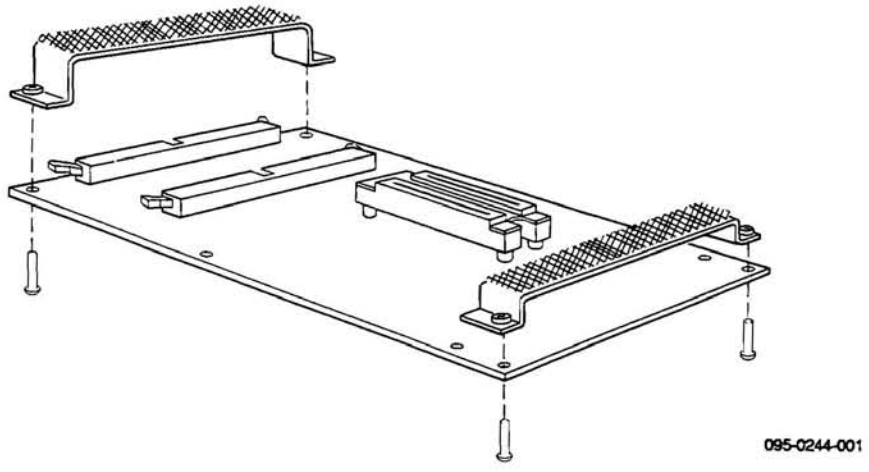


Figure 2-13. Installing the Velcro Mounting Brackets on the Performance Board

3. Install the mating Velcro strips on the back of the device handler:

   a. Press the matching Velcro strips onto the Velcro on the mounting brackets.

   b. Remove the adhesive backing on the Velcro strips.

   c. With the Exatron side of the performance board facing the back of the handler, slide the performance board onto the pin on the rear of the handler as shown in figure 2-14.

   NOTE

   Some Exatron handlers do not have a guide pin on the contactor assembly. This guide pin is required to ensure proper installation of the 20 and 24-pin performance boards. If your handler does not have a guide pin, one may be ordered from Exatron.

   d. Press the performance board against the back of the device handler so that the adhesive surface sticks to the back of the handler. When the performance board is removed, the Velcro strips should remain attached to the handler in the correct position.

The mounting brackets and Velcro are now installed.

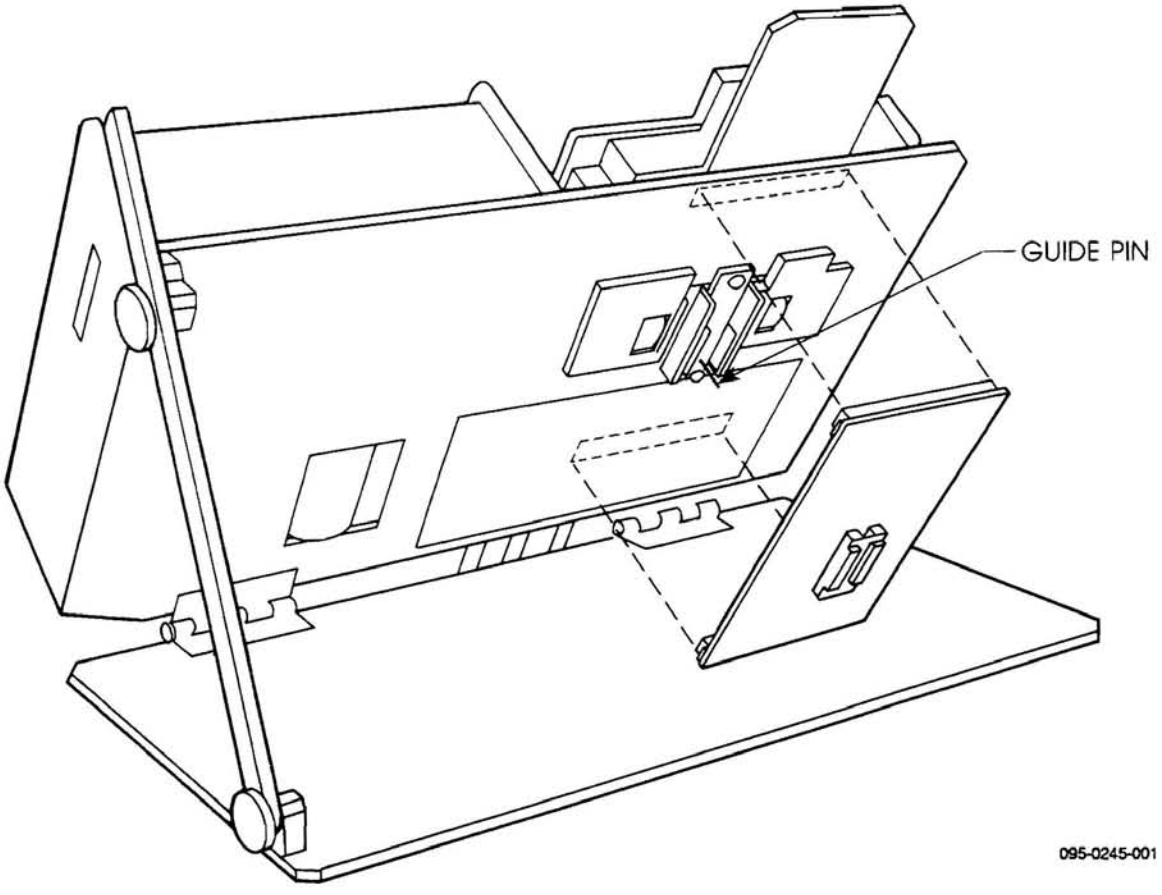


Figure 2-14. Mounting the Velcro Strips on the Exatron Handler

Installing/Removing the Adapter Module

Use the following procedure to install the adapter module:

1. Hold the adapter above the front panel socket receptacle (refer to Figure 2- 15).
2. Tilt the adapter down and into the receptacle, and push forward.
3. Push down the wing handle so that the adapter connector mates with the receptacle connector.

Use the following procedure to remove the adapter module:

1. Pull up on the socket adapter wing handle (refer to figure 2-15).
2. Pull the adapter toward you and away from the front panel receptacle.

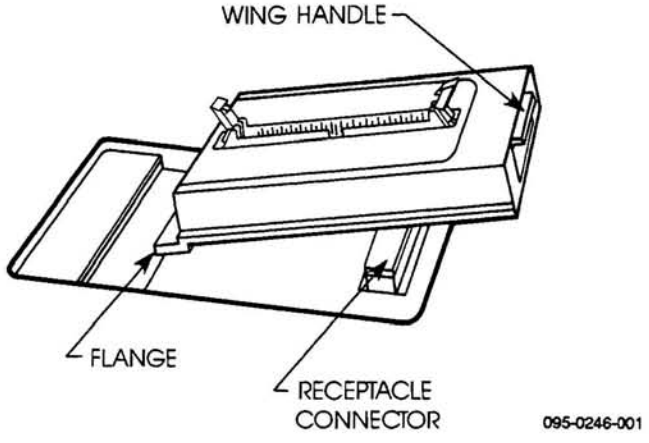


Figure 2-15. Installing the Adapter Module

Connecting the Adapter Module to the Performance Board

The adapter module connects to the performance board via a 60-pin ribbon cable. Use the following procedure to connect the cable:

1. Ensure that the connector tabs on the top of the adapter are snapped out (refer to figure 2-16a).
2. With the colored sidestrip (indicating pin 1) of the cable on the left, insert the 60-pin ribbon cable into the adapter's connector (refer to figure 2-17).
3. Ensure that the connector tabs on the adapter are now snapped in (refer to figure 2-16b).

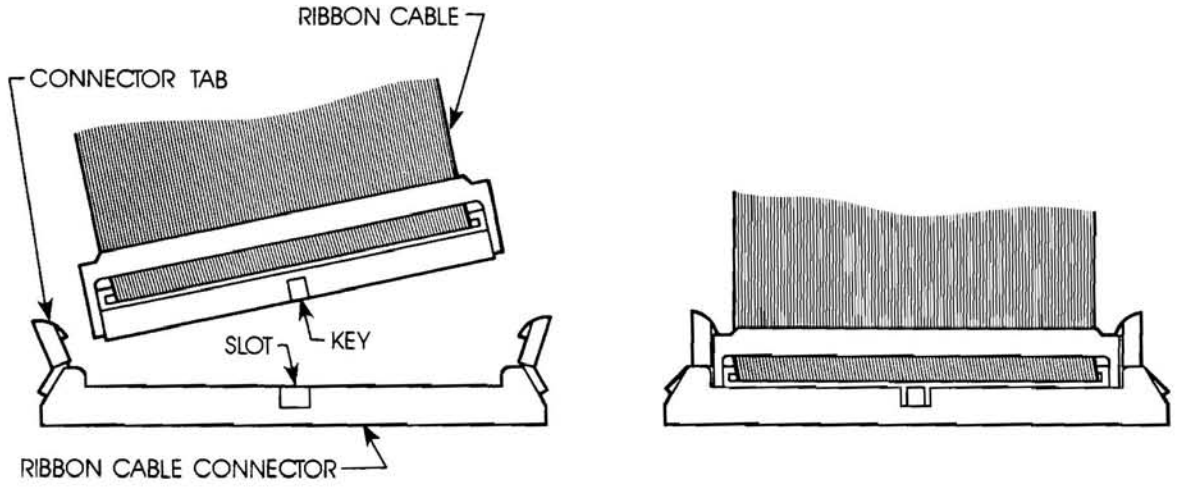


Figure 2-16. Connector Tabs on a Ribbon Cable Connector

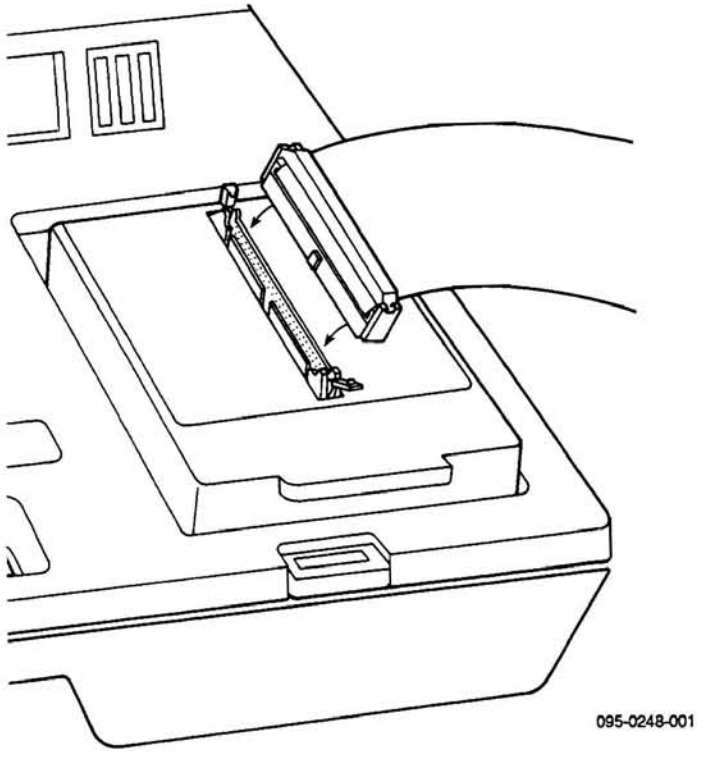


Figure 2-17. Connecting the Ribbon Cable to the Adapter Module

4. Locate the appropriate connector (PAL or IFL) for the type of devices to be programmed on the Exatron side of the performance board. (Exatron is marked on the performance board to indicate the Exatron side of the board.) The two ribbon connectors on the board are marked to indicate either PAL or IFL (refer to figure 2-18).

NOTE

The 28-pin IFL performance board has only one connector and is used only for IFL programming.

5. Ensure that the connector tabs on the performance board are snapped out (refer to figure 2-19).

6. Insert the 60-pin ribbon cable into the connector as shown in figure 2-19. Ensure that the connector tabs are now snapped back in.

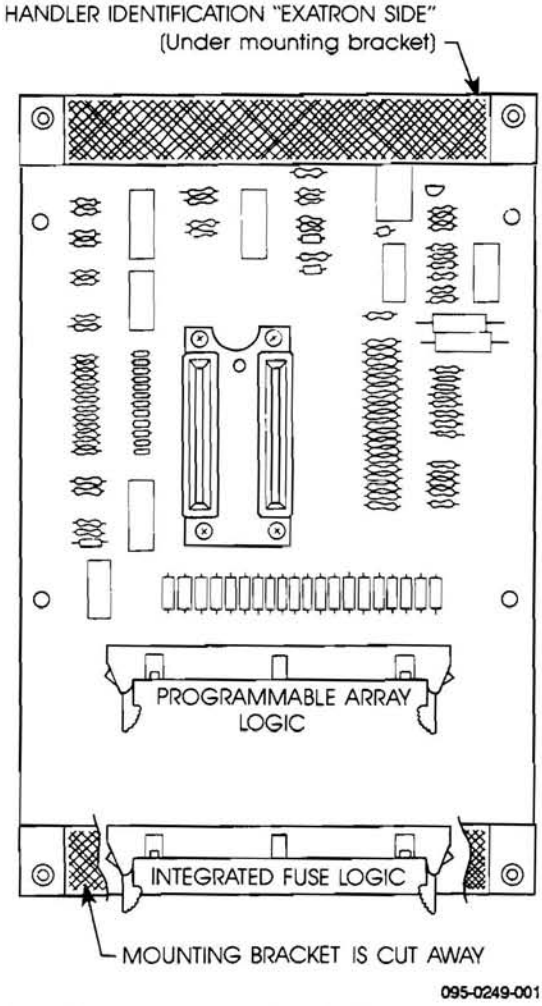


Figure 2-18. Exatron Side of a Performance Board

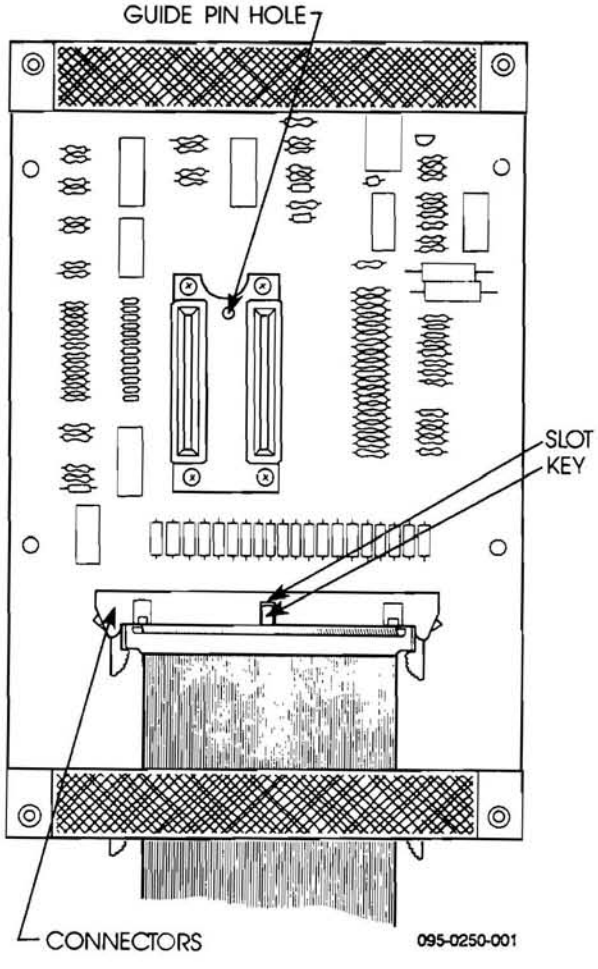


Figure 2-19. Connecting the Ribbon Cable to the Performance Board

Installing the Performance Board

Use the following procedure to install the performance board on the handler:

1. With the Exatron side of the performance board facing the back of the handler slide the performance board onto the connector with the ribbon cable connectors upward (refer to figure 2-20).

NOTE

Some Exatron handlers do not have a guide pin on the contactor assembly. This guide pin is required to ensure proper installation of the 20 and 24-pin performance boards. If your handler does not have a guide pin, one may be ordered from Exatron.

2. Secure the board by pressing the two sides of the Velcro strips together (refer to figure 2-20).

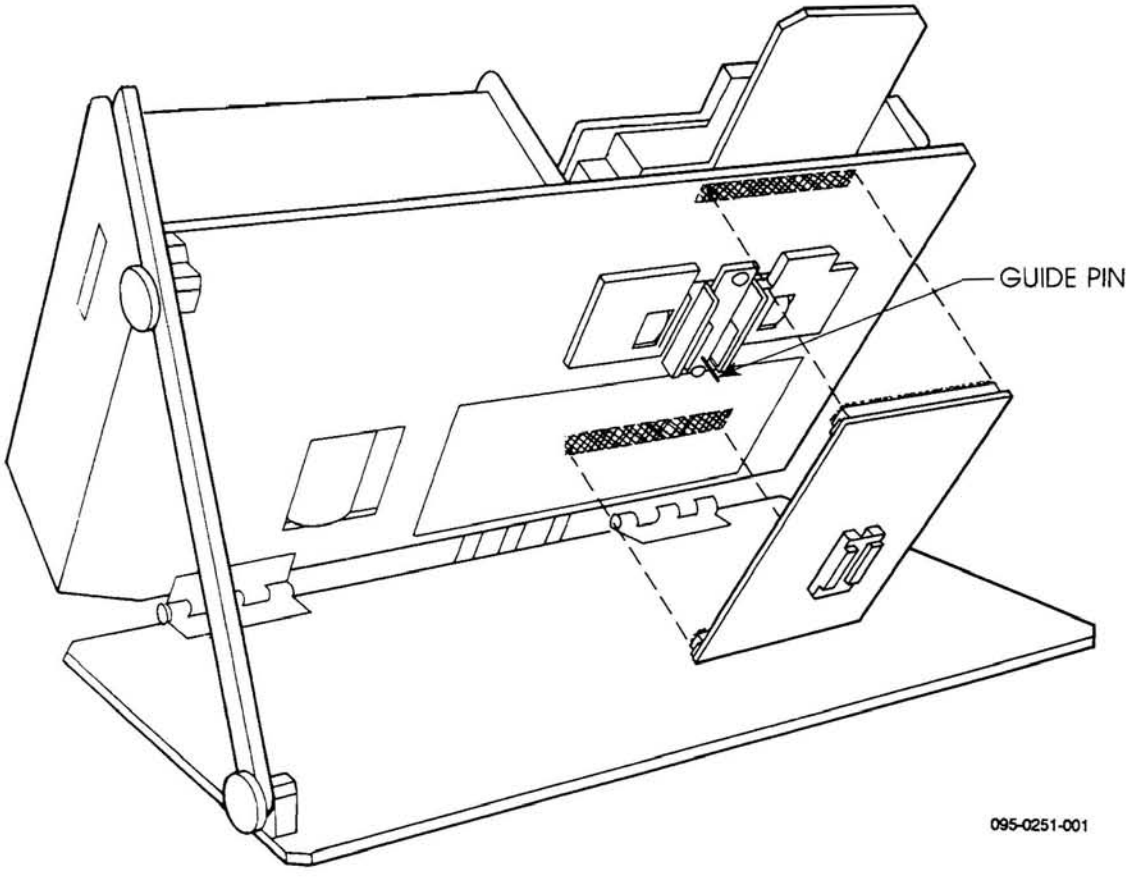


Figure 2-20. Installing the Performance Board on the Exatron Handler

2.6.1.3 Connecting the Control Cable

The Exatron control cable provides handler control and binning signals. The control cable is marked Exatron and is connected between parallel ports on the 60H and the handler (refer to figure 2-21). One end of the cable is labelled PROG and the other end is labeled HANDLER. Install the cable so that the PROG end is connected to the programmer and the HANDLER end to the handler.

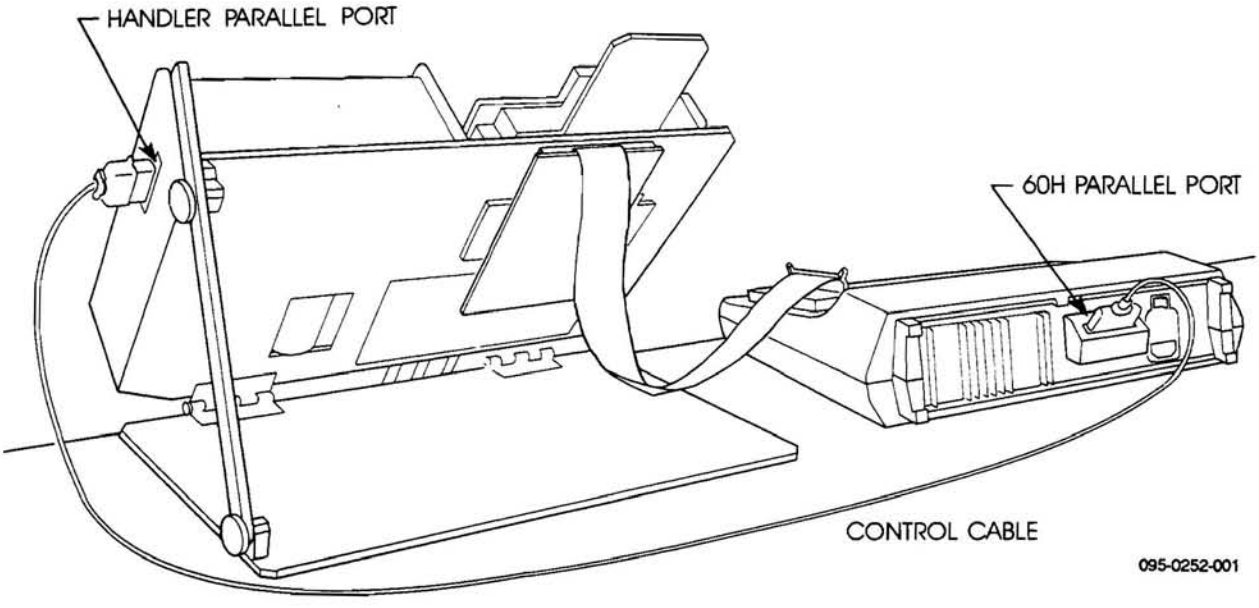


Figure 2-21. Connecting the Control Cable Between the 60H and the Exatron Handler

2.6.2 MCT Handler Interface Installation

WARNING

The instructions contained in this subsection are for qualified service personnel only. Do not attempt them unless you are qualified to do so.

CAUTION

Refer to the MCT manual for detailed instructions and information on the handler before beginning this procedure.

Preparing the MCT Handler for use with the Model 60H requires four operations.

- Modifying the opto-interface board
- Setting the category switches
- Installing the adapter module and performance board
- Connecting the control cable

2.6.2.1 Modifying OPTO-Interface Board

The opto-interface board for the MCT handlers must be modified slightly for the interface to function properly. The modification procedures for each of the three models follows. Complete information on the handler's interface circuitry can be found in MCT technical manuals.

MCT Models 2604 and 2608

To prepare the MCT model 2604 and model 2608 opto-interface boards (see figures 2-22) perform the following procedure:

1. Ensure that jumpers I-1 through I-5 are installed for negative true category select signals (I-1 through I-4 for the 2604).

2. Remove the I-24 and I-26 jumpers.

3. Place a 0.22 µf capacitor across I-24.

4. Swap the locations of resistors R51 (68K) and R52 (30K).

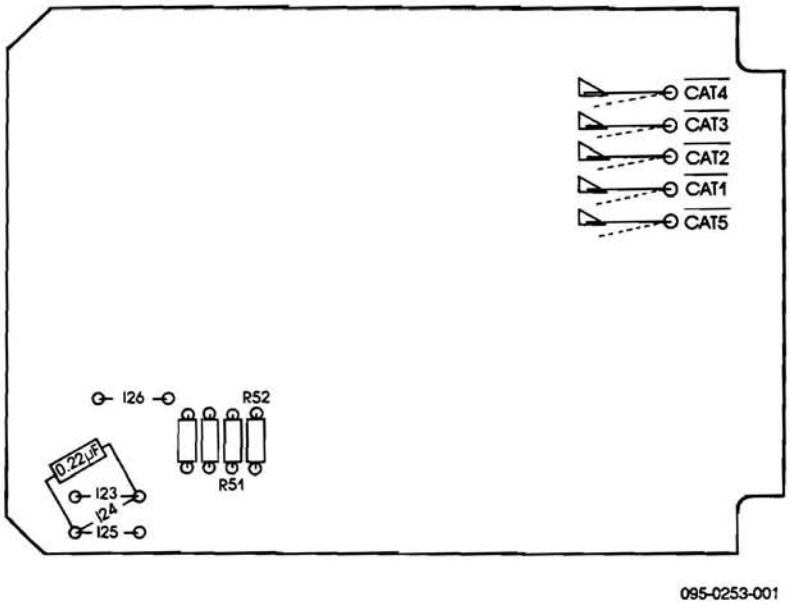


Figure 2-22. 2604/2608 Opto-Interface

MCT Model 3608

To prepare MCT models 3608 (see figure 2-23) perform the following procedure:

1. Remove all jumpers except the NEG jumpers in CH1-CH5 and the OFF jumper in the "EOT" section. If no jumpers are installed in these locations, install them.

2. Install a 0.22 µf capacitor in the NEG location of the "TEST READY" section.

3. Swap the locations of resistors R33 (68K) and R34 (30K).

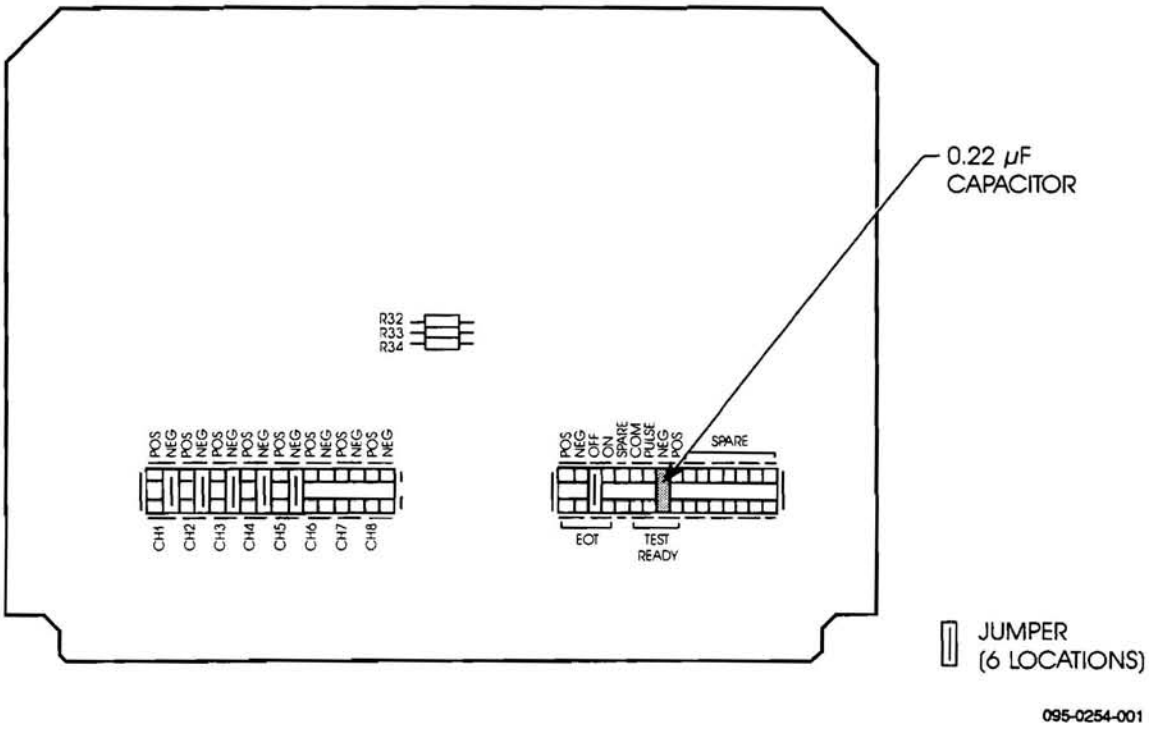


Figure 2-23. 3608 Opto-Interface Board After Necessary Modifications

2.6.2.2 Setting the Sort Category Switches

Each time a device is programmed or tested, the Model 60H sends one of five sort category signals to the device handler. These sort categories are used by the MCT handler to sort devices into bins. For example, all correctly programmed devices can be put into one bin, all devices with an illegal-bit error can be put into another bin.

NOTE

Model 60H Sort conditions, such as PASS, or ARRAY FAIL, are assigned sort categories from the Model 60H front panel.

Before you start programming with the handler, the Model 60H sort categories must be assigned to specific handler bins. To do this, set the appropriate sort category switches on the handler.

The sort category switches are located at the front of the handler as shown in figure 2-24. There is one set of wight switches for each MCT sort category. The MCT supports wight sort categories so there are eight sets of switches. Each switch within a set corresponds to one of the eight output bins (reservoirs) and is numbered with the bin number. To set the sort category switches, flip the switch corresponding to the desired bin to the ON position.

NOTE

The MCT Handler supports eight sort categories; however, the Model 60H supports only five. Therefore, only the first five MCT categories can be used. To use all eight MCT bins, assign more than one bin to the five usable categories.

2.6.2.3 Installing the Adapter Module and Performance Board

Installing the interface adapter for use with an MCT handler requires the following procedures:

- If required, install the performance board mounting brackets
- Install the adapter module into the Model 60H
- Connect the adapter module to the performance board
- Install the performance board onto the handler

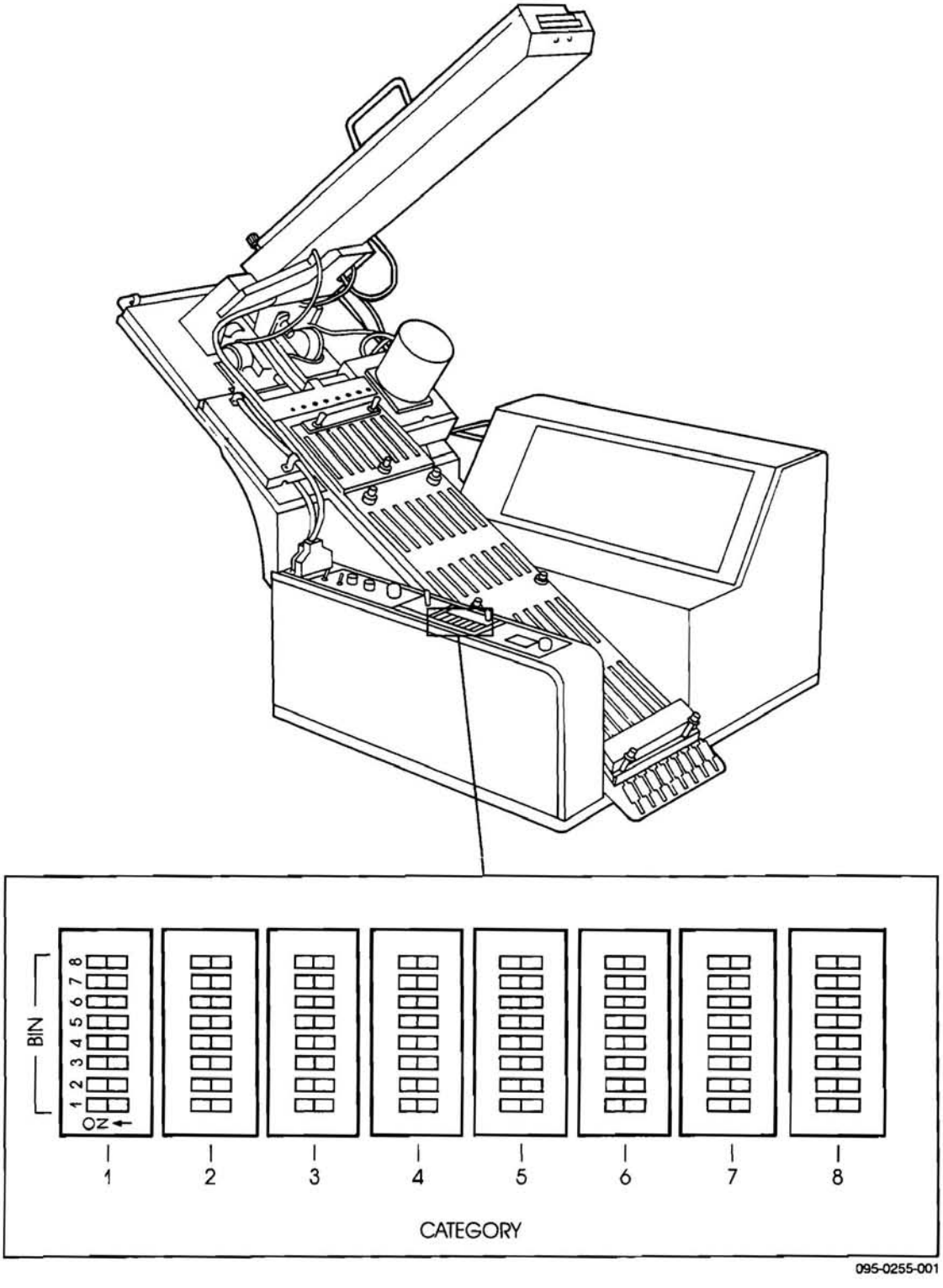


Figure 2-24. Category Selection Switches on the MCT Handler

MCT Performance Board Mounting Bracket Installation

The performance board can be mounted to the device handler using four screws and standoffs or mounting brackets faced with Velcro strips.

If you want to use the screw and standoff mounting method, no initial preparation of the performance board is required and you can proceed to "Installing/Removing The Adapter Module".

To install the brackets and Velcro, perform the following procedure:

1. Locate the four screw holes on the MCT side of the performance board (see figure 2-25).

2. Position the MCT mounting brackets (P/N 415-1336) over the screw holes, and attach them to the performance board with the screws provided.

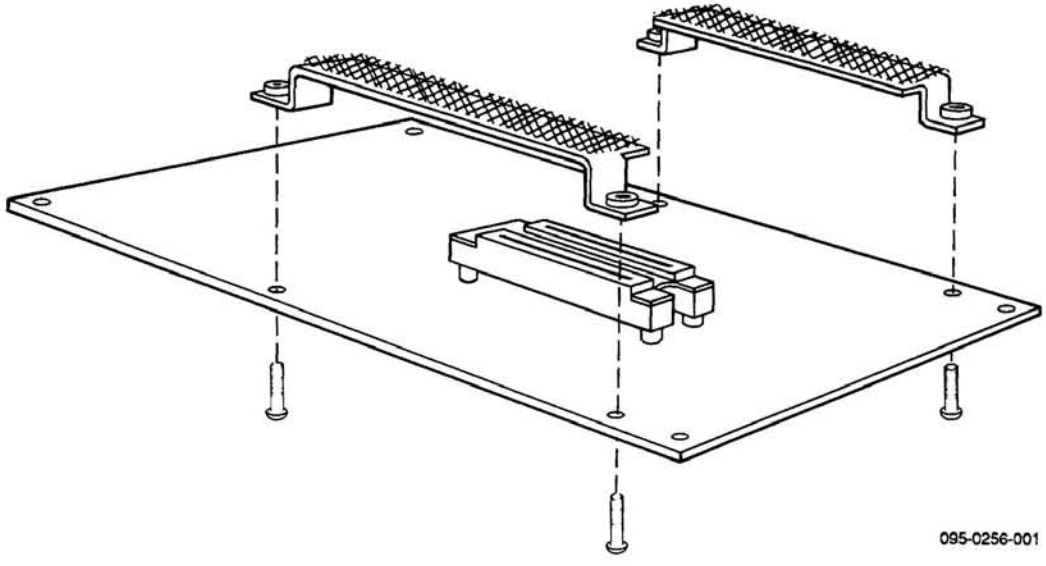


Figure 2-25. Installing the Velcro Mounting Brackets on the Performance Board

3. Install the mating Velcro strips on the back of the device handler:

   a. Press the matching Velcro strips onto the Velcro on the mounting brackets.

   b. Remove the adhesive backing on the Velcro strips.

   c. With the MCT side of the performance board facing the back of the handler, slide the performance board onto the pin on the rear of the handler as shown in figure 2-26.

   d. Press the performance board against the back of the device handler so that the adhesive surface sticks to the back of the handler. When the performance board is removed, the Velcro strips should remain attached to the handler in the correct position.

The mounting brackets and Velcro are now installed.

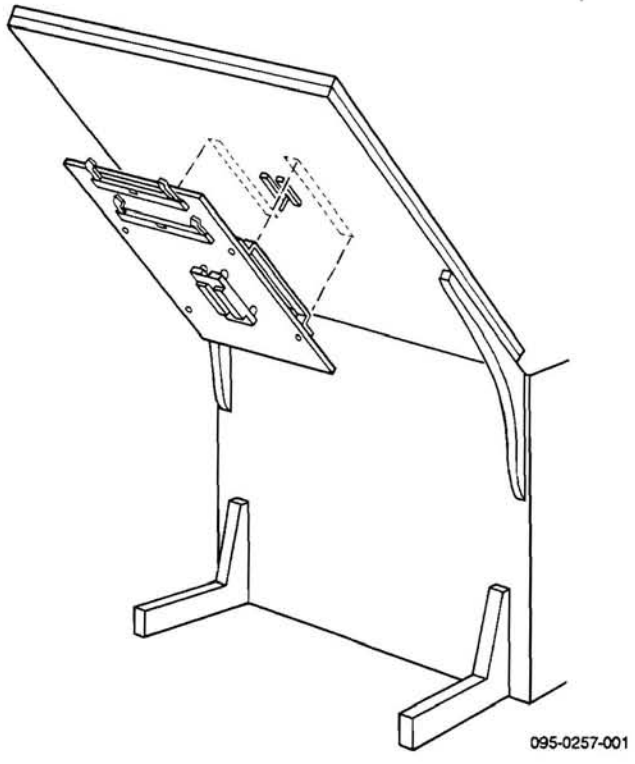


Figure 2-26. Mounting the Velcro Strips on the MCT Handler

Installing/Removing the Adapter Module

Use the following procedure to install the adapter module:

1. Hold the adapter above the front panel socket receptacle (refer to Figure 2- 27).
2. Tilt the adapter down and into the receptacle, and push forward.
3. Push down the wing handle so that the adapter connector mates with the receptacle connector.

Use the following procedure to remove the adapter module:

1. Pull up on the socket adapter wing handle (refer to figure 2-27).
2. Pull the adapter toward you and away from the front panel receptacle.

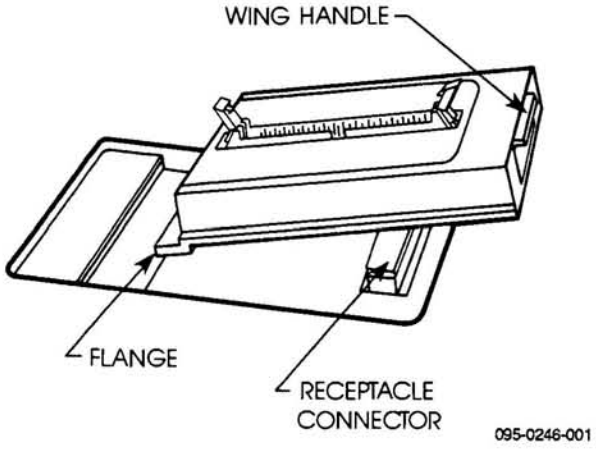


Figure 2-27. Installing the Adapter Module

Connecting the Adapter Module to the Performance Board

The adapter module connects to the performance board via a 60-pin ribbon cable. Use the following procedure to connect the cable:

1. Ensure that the connector tabs on the top of the adapter are snapped out (refer to figure 2-28a).

2. With the colored sidestrip (indicating pin 1) of the cable on the left, insert the 60-pin ribbon cable into the adapter's connector (refer to figure 2-29).

3. Ensure that the connector tabs on the adapter are now snapped in (refer to figure 2-28b).

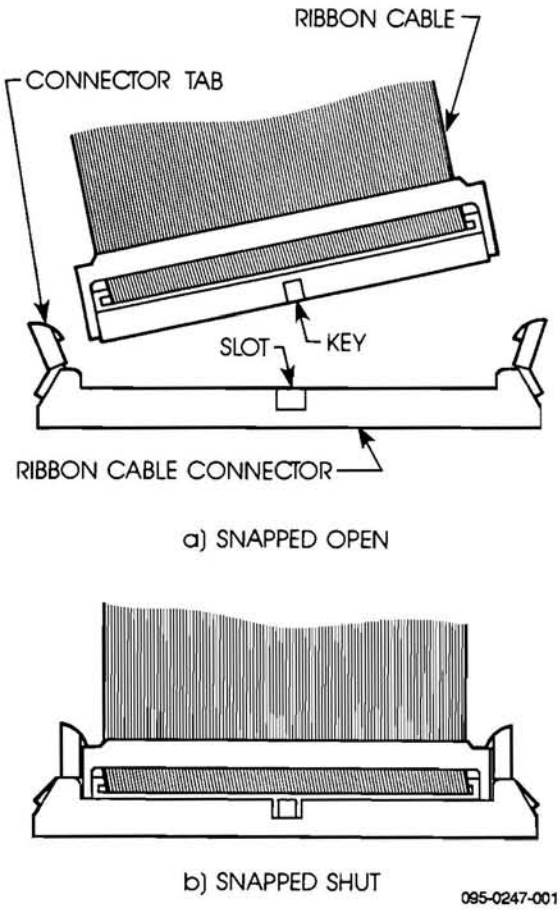


Figure 2-28. Connector Tabs on a Ribbon Cable

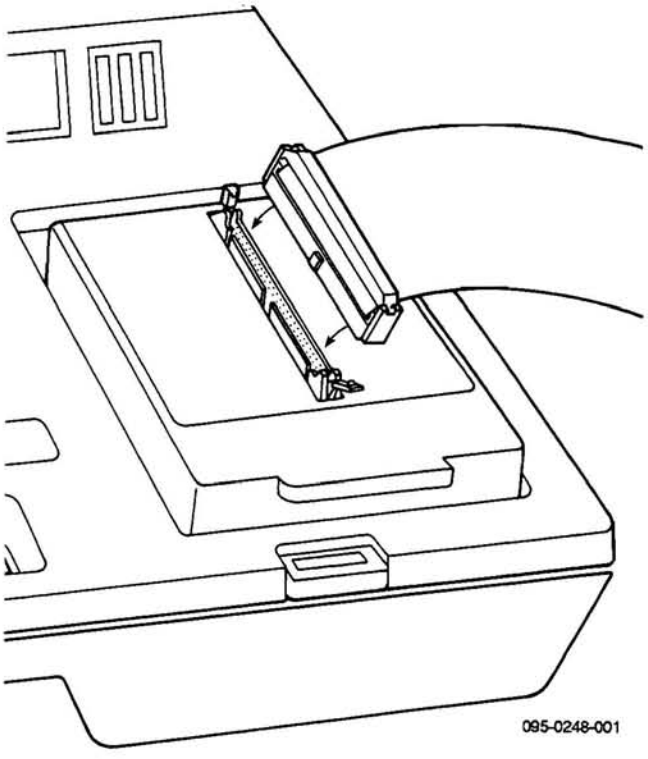


Figure 2-29. Connecting the Ribbon Cable to the Adapter Module

4. Locate the appropriate connector (PAL or IFL) for the type of devices to be programmed on the Exatron side of the performance board. The two ribbon connectors on the board are marked to indicate either PAL or IFL (refer to figure 2-30).

NOTE

The 28-pin IFL performance board has only one connector and is used only for IFL programming.

5. Ensure that the connector tabs on the performance board are snapped out (refer to figure 2-31).

6. Insert the 60-pin ribbon cable into the connector as shown in figure 2-31. Ensure that the connector tabs are now snapped back in.

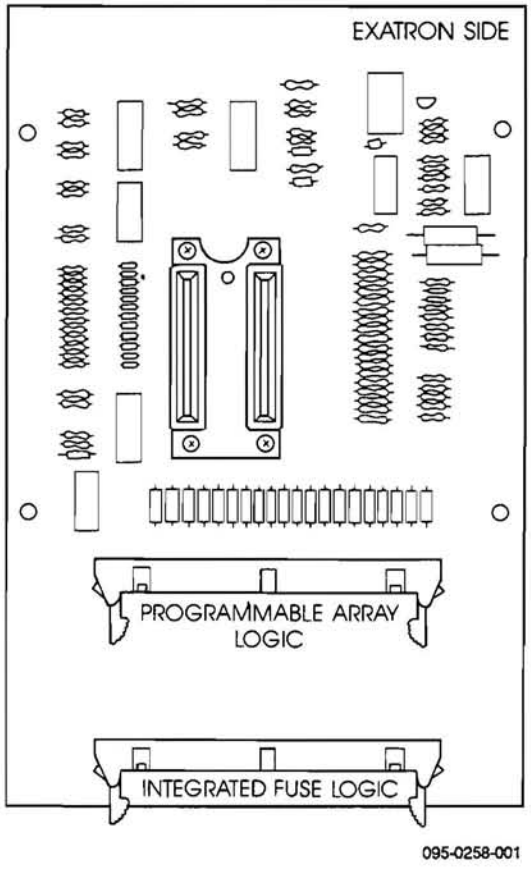


Figure 2-30.
Exatron Side of a Performance Board

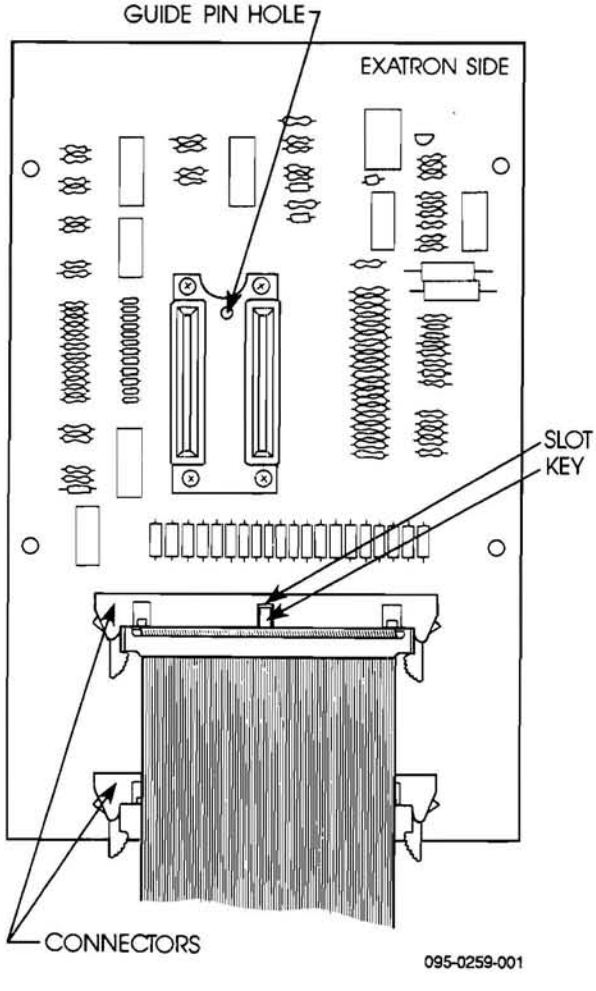


Figure 2-31. Connecting the Ribbon Cable to the Performance Board

Installing the Performance Board

Use the following procedure to install the performance board on the handler:

1. With the MCT side of the performance board facing the back of the handler slide the performance board onto the connector with the ribbon cable connectors upward.

2. If using the screw and standoff securing method secure the board with four screws supplied, using the four standoffs to provide spacing between the board and handler (refer to figure 2-32a).

   If using the bracket and Velcro method press the mating Velcro strips together (refer to figure 2-32b).

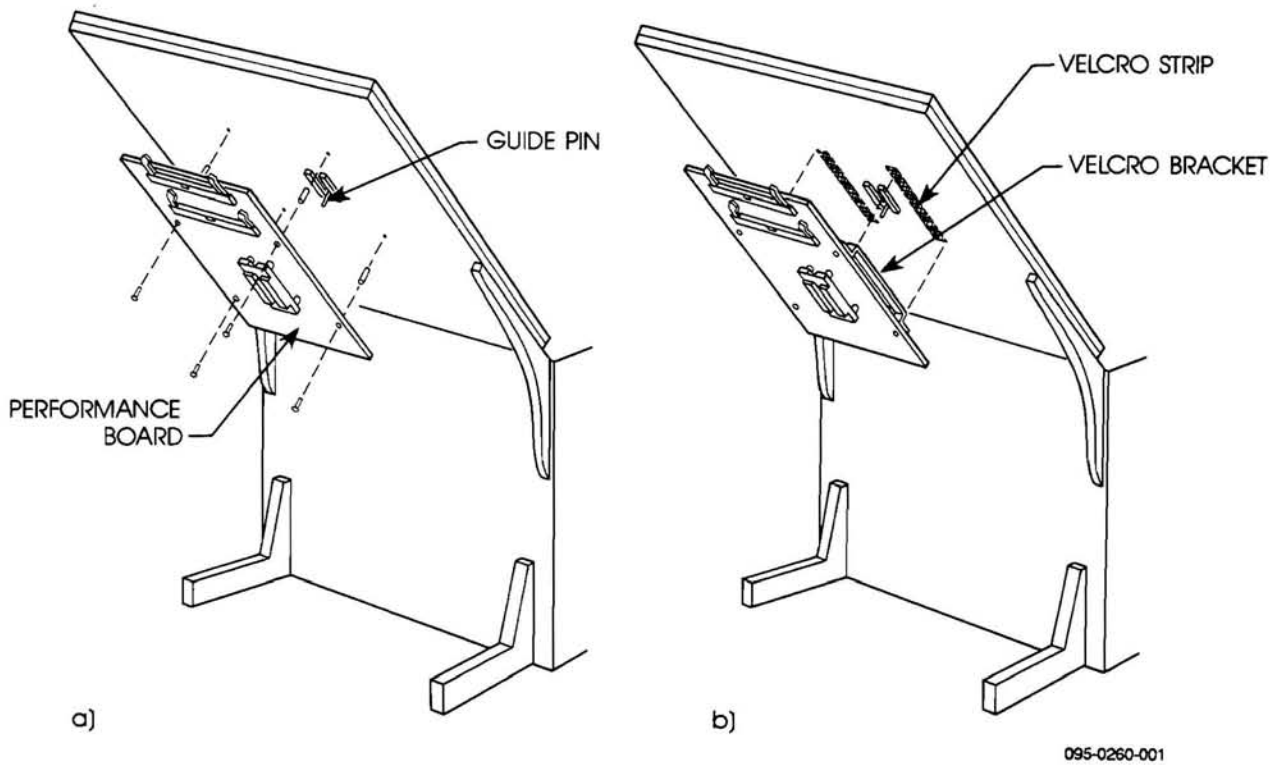


Figure 2-32. Installing the Performance Board on the MCT Handler

2.6.2.4 Connecting the Control Cable

The MCT control cable provides handler control and binning signals. The control cable is marked MCT and is connected between parallel ports on the 60H and the handler (refer to figure 2-33). One end of the cable is labelled PROG and the other end is labeled HANDLER. Install the cable so that the PROG end is connected to the programmer and the HANDLER end to the handler.

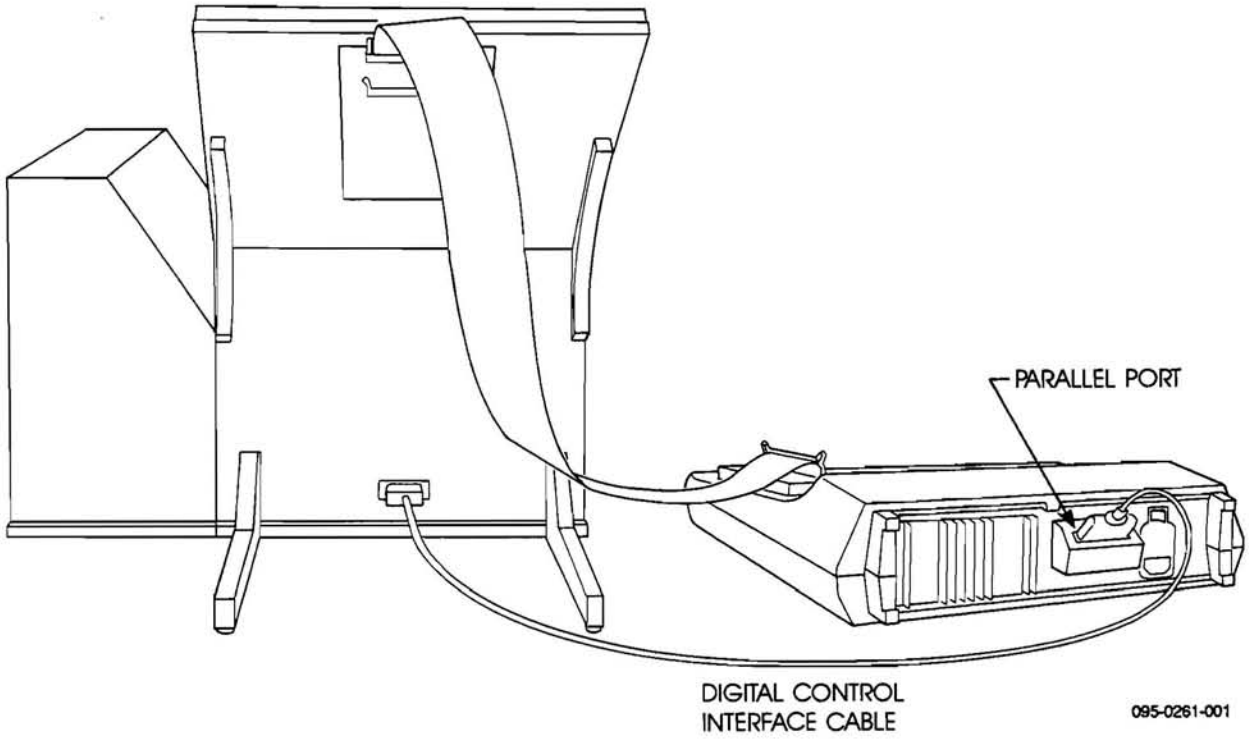


Figure 2-33. Connecting the Control Cable Between the 60H and MCT Handler

2.6.3 Data I/O Model 300 Handler Interface Installation

WARNING

The instructions contained in this subsection are for qualified service personnel only. Do not attempt them unless you are qualified to do so.

This subsection explains how to install the adapter interface on the Data I/O Model 300 handler. The adapter module, ribbon cable, performance board, and control cable must all be installed.

Each time a device is programmed or tested, the Model 60H sends one of five sort category signals to the device handler. These sort categories are used by the Model 300 handler to sort devices into bins. For example, all correctly programmed devices can be put into one bin, all devices with an illegal-bit error can be put into another bin.

NOTE

Model 60H Sort conditions, such as PASS, or ARRAY FAIL, are assigned sort categories from the Model 60H front panel.

Before you start programming with the handler, the Model 60H sort categories must be assigned to specific handler bins. To do this, set the appropriate sort categories from the Model 60H front panel.

2.6.3.1 Installing the Adapter Module and Performance Board

Installing the interface adapter for use with a Data I/O Model 300 handler requires the following procedures:

- Install the performance board onto the handler
- Install the adapter module into the Model 60H
- Connect the adapter module to the performance board

Installing the Performance Board

The performance board provides signal conditioning circuits for lines that extend from Model 60H to the handler. These circuits compensate for any signal degradation that may be introduced by the interconnecting cable.

The performance board installs on the back of the handler as shown in figure 2-34. Each performance board supplied with the interface kit is identified as being 20-pin or 24-pin. Select the performance board required for the programming operation.

To install the performance board on the handler, perform the following steps.

1. Mount the performance board on the back of the handler with the two blue connectors on the performance board facing out from the handler.

2. Using the supplied screws, fasten the board to the back surface of the handler (refer to figure 2-34).

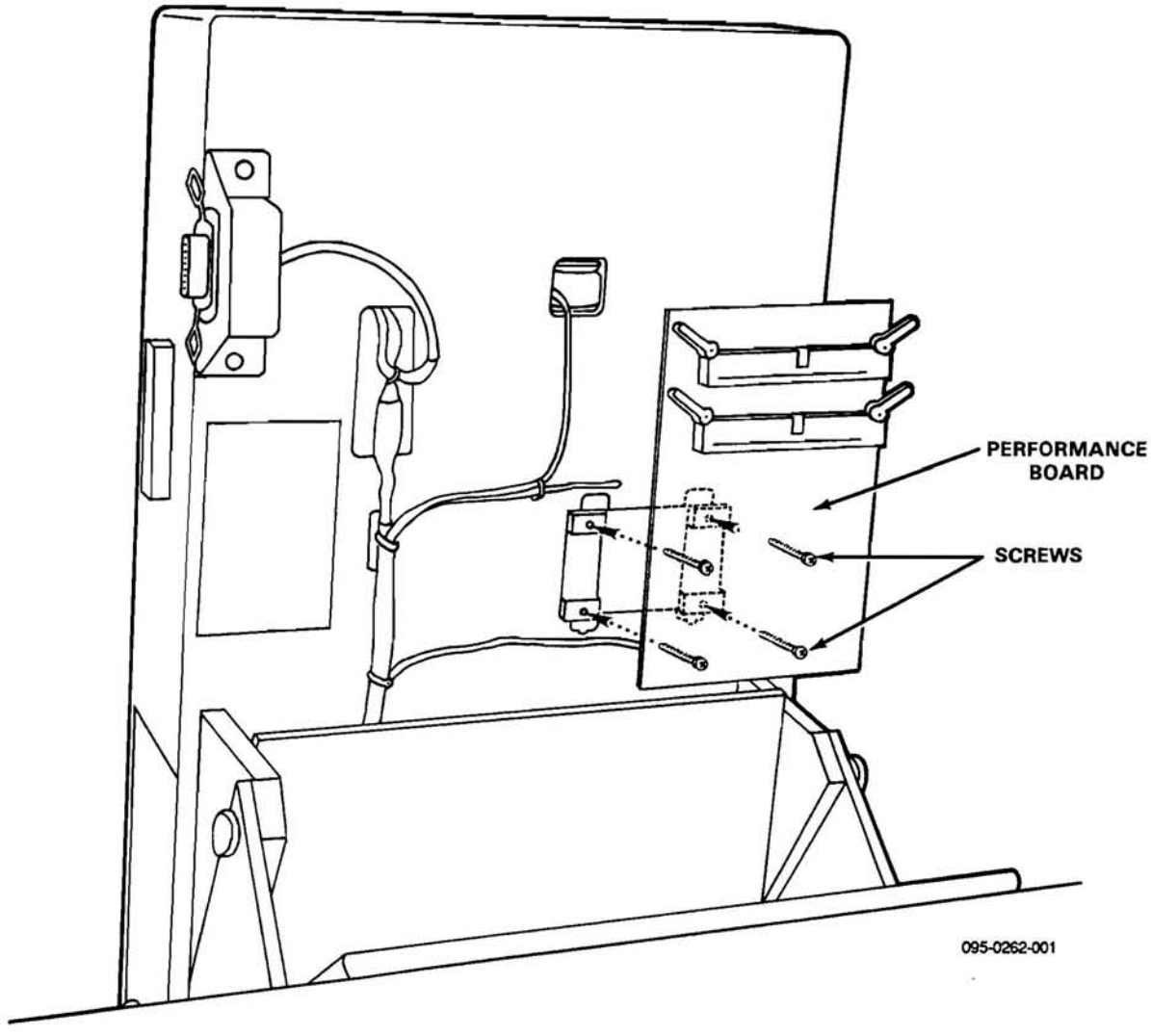


Figure 2-34. Installing the Performance Board

Installing/Removing the Adapter Module

Use the following procedure to install the adapter module:

CAUTION

Voltage transients can damage a device. Be sure that the handler is free of devices before you apply power to the system or before you install or remove the handler interface adapter.

1. Hold the adapter above the front panel socket receptacle (refer to Figure 2-35).
2. Tilt the adapter down and into the receptacle, and push forward.
3. Push down the wing handle so that the adapter connector mates with the receptacle connector.

Use the following procedure to remove the adapter module:

CAUTION

Voltage transients can damage a device. Be sure that the handler is free of devices before you apply power to the system or before you install or remove the handler interface adapter.

1. Pull up on the socket adapter wing handle (refer to figure 2-35).
2. Pull the adapter toward you and away from the front panel receptacle.

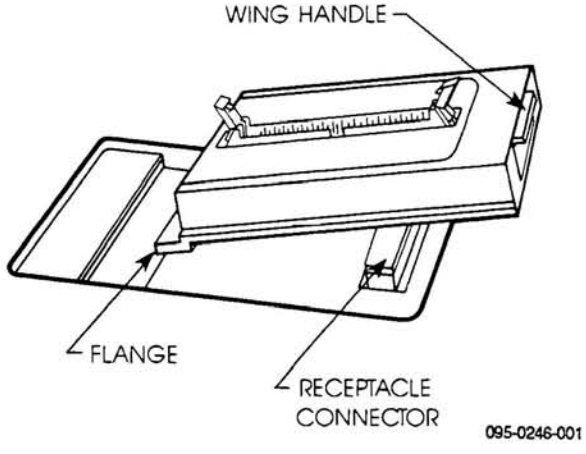


Figure 2-35. Installing the Adapter Module

Connecting the Adapter Module to the Performance Board

The adapter module connects to the performance board via a 60-pin ribbon cable. Use the following procedure to connect the cable:

1. Ensure that the connector tabs on the top of the adapter are snapped out (refer to figure 2-36a).

2. With the colored sidestrip (indicating pin 1) of the cable on the left, insert the 60-pin ribbon cable into the adapter's connector (refer to figure 2-37).

3. Ensure that the connector tabs on the adapter are now snapped in (refer to figure 2-36b).

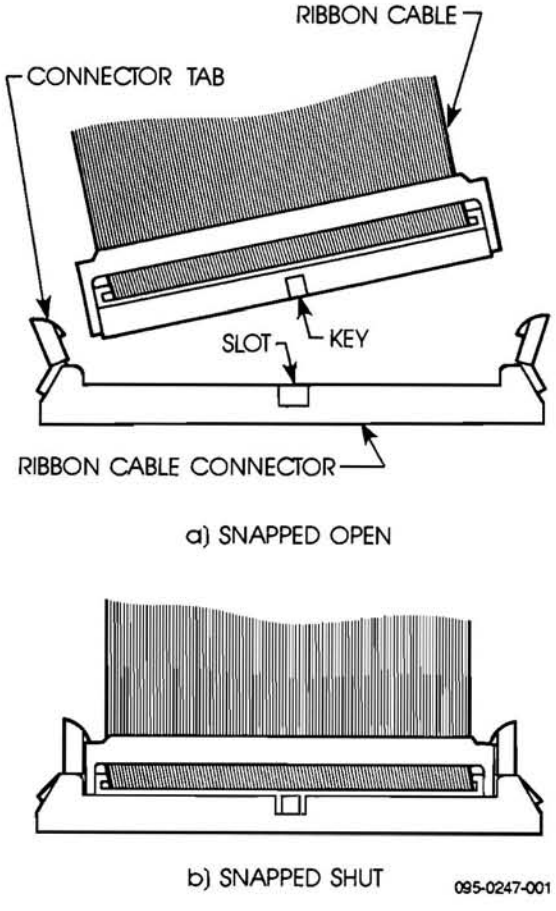


Figure 2-36. Connector Tabs on a Ribbon Cable Connector

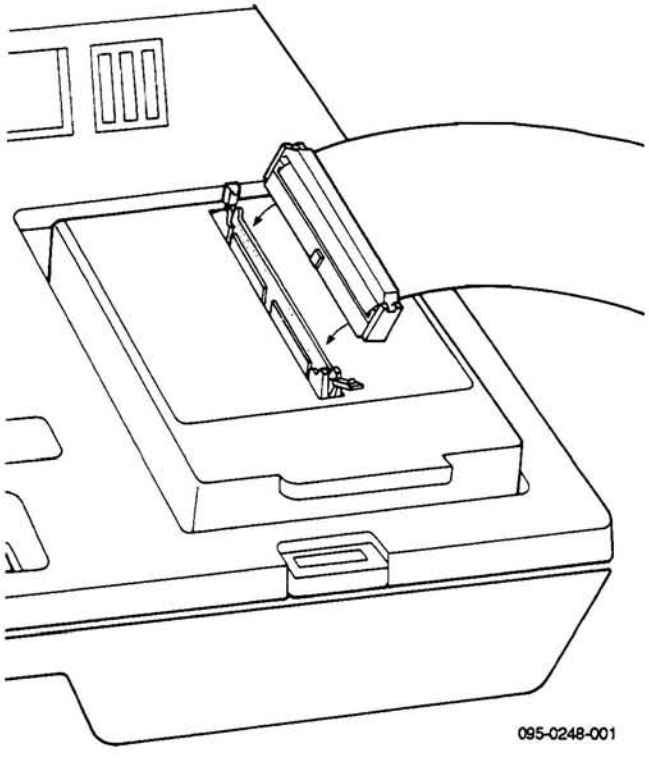


Figure 2-37. Connecting the Ribbon Cable to the Adapter Module

4. Locate the appropriate connector (PAL or IFL) for the type of devices to be programmed. The two ribbon connectors on the board are marked to indicate either PAL or IFL (refer to figure 2-38).

5. Ensure that the connector tabs on the performance board are snapped out (refer to figure 2-38).

6. Insert the 60-pin ribbon cable into the connector as shown in figure 2-38. Ensure that the connector tabs are now snapped back in.

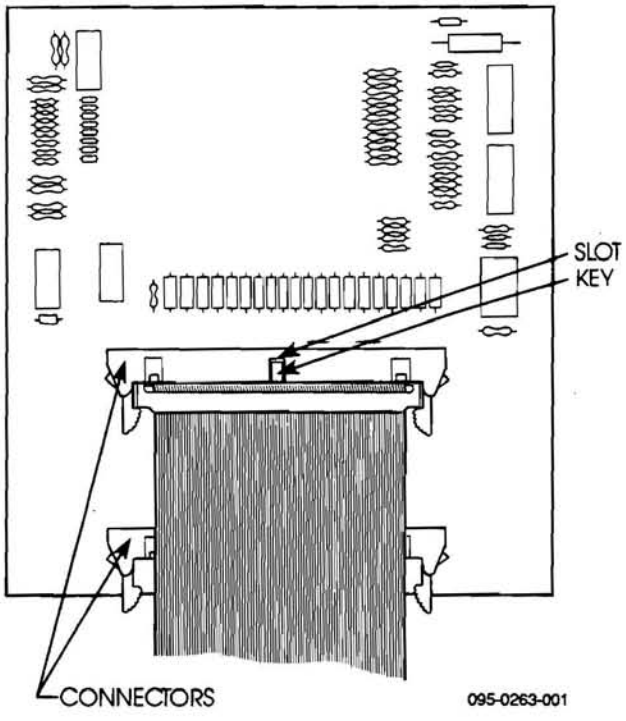


Figure 2-38. Connecting the Ribbon Cable to the Performance Board

2.6.3.2 Connecting the Control Cable

The Model 300 control cable provides handler control and binning signals. The control cable is connected between parallel ports on the 60H and the handler (refer to figure 2-39). One end of the cable is labelled PROG and the other end is labeled HANDLER. Install the cable so that the PROG end is connected to the programmer and the HANDLER end to the handler.

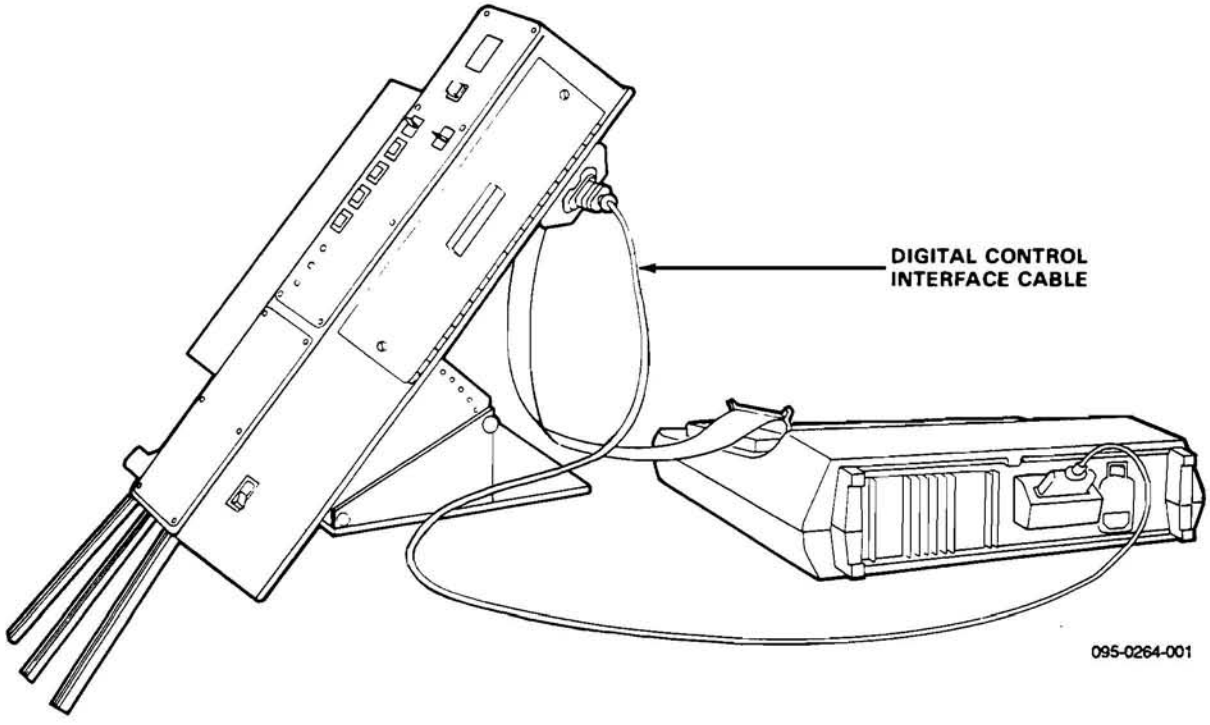


Figure 2-39. Installing the Control Cable

3. CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This section describes the Model 60 programmer's circuitry. It includes both general and detailed circuit descriptions of the programmer's main functions. Each function is described in its own subsection along with a block diagram.

This section also discusses the main components of the series 60 programmer, address map assignments, and assembly cabling.

3.2 GENERAL CIRCUIT DESCRIPTION

The Model 60 is a microprocessor-based programmer utilizing bus style architecture. Figure 3-1 shows the functional arrangement of the Model 60. The blocks shown in figure 3-1 are described in the following paragraphs.

AC line voltage passes through a voltage selector and filter to the transformer and a cooling fan. The AC is rectified, filtered and regulated for use by all other circuits in the Model 60.

A microprocessor controls all programming operations for the Model 60, and is interfaced to a keyboard and display. The actual programming of devices is performed through the socket adapter which receives signals from the waveform generator.

An internal RAM in the Model 60 provides storage for all programming information whether downloaded from a master device or from an external source (computer, terminal, etc.).

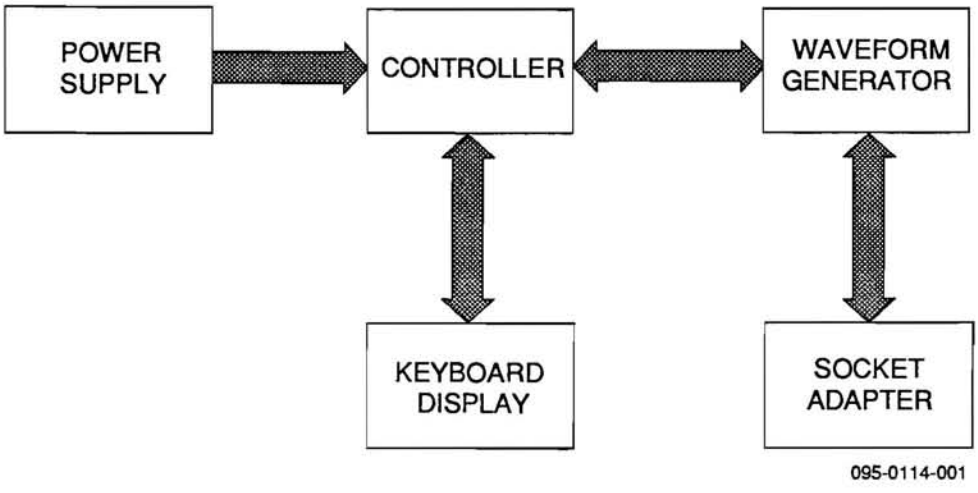


Figure 3-1. System Block Diagram

3.3 DETAILED CIRCUIT DESCRIPTION

Figure 3-2 shows an interconnect diagram of the programmer. Each of the circuit areas (power supplies, keyboard/display, controller board, and waveform generator) is described in the following paragraphs and shown in separate block diagrams.

Figure 3-2 also shows the cabling between assemblies along with associated connector cables and part numbers. The schematic for each board is located in Appendix A.

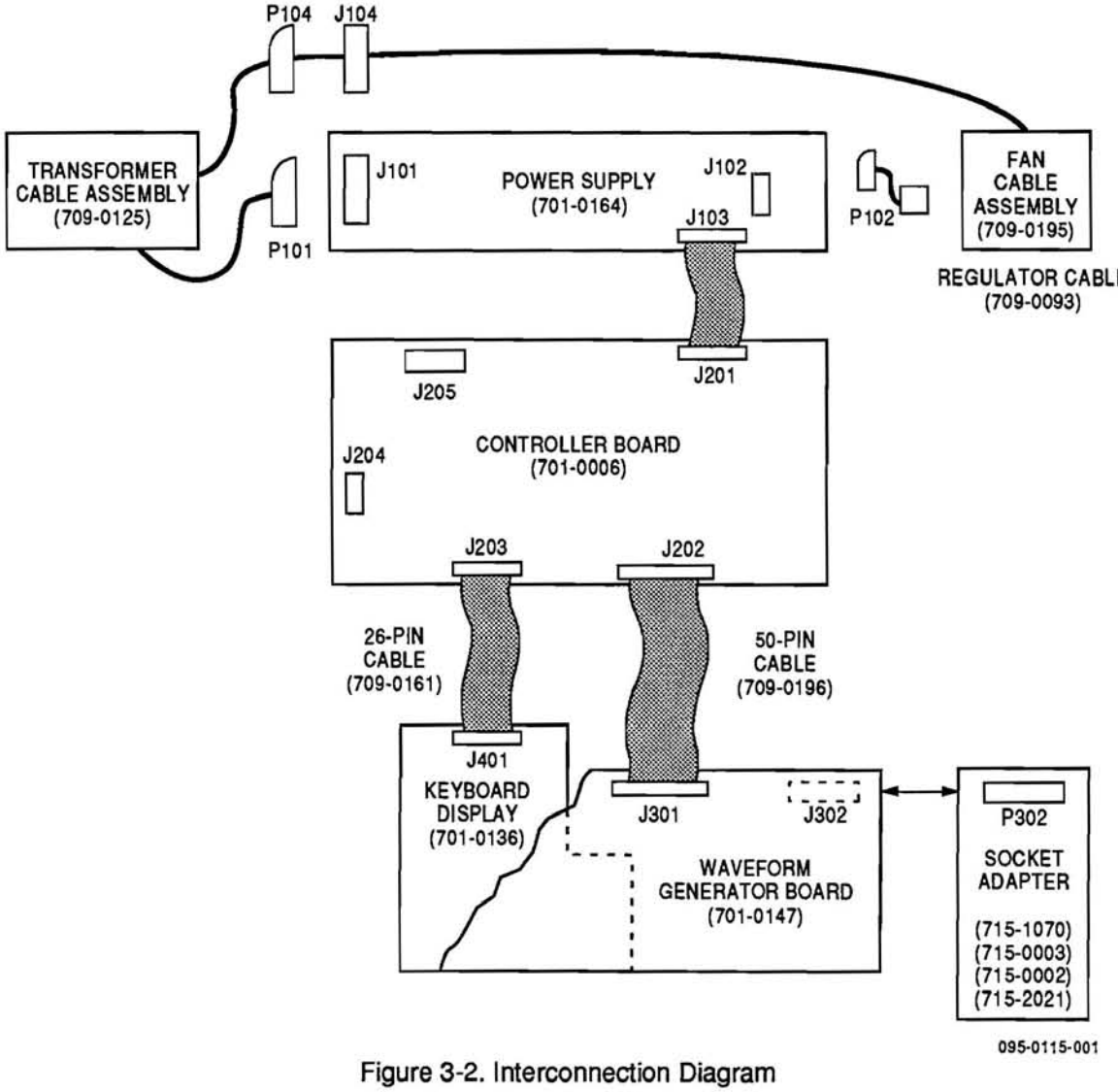


Figure 3-2. Interconnection Diagram

3.3.1 Power Supply

The power supply is divided into two main subassemblies: the transformer cable assembly (709-0125) and the power supply assembly (701-0164). Refer to figure 3-3. These subassemblies are described in this subsection.

3.3.1.1 Transformer Cable Assembly

The transformer cable assembly is made up of the AC line filter, AC line fuse, power switch, voltage selector, and transformer. The AC line filter, line fuse and voltage selection wheel are all in a single unit. The voltage selector unit adapts the programmer to the correct line voltage. This AC line voltage selection process is described in section 2. The transformer primary contains taps which provide for operation at 100, 120, 220 or 240 volts.

3.3.1.2 Power Supply Regulator

The transformer secondary is tied to the rectifier, filter and regulator network.

The -15 volt supply is applied through fuse F1. The -15 and + 48 volt unregulated supplies are rectified by diodes CR1 through CR4 and CR5 through CR8. They are filtered by capacitors C4 and C5. The + 25 volts is a regulated supply rectified by diodes CR9 through CR12, filtered by capacitor C1 and regulated by the three-terminal regulator, VR2. The output of the + 25 volt supply is further regulated by VR1 to provide a + 15 volt supply. This + 15 volt supply is reduced to 9.1V by CR18 and R7 and is applied to the center tap of the secondary winding. The other two legs of this winding provide 5.5 volts AC to the filaments of the FIP (fluorescent indicator panel) display. The + 5 volts is a regulated supply rectified by diodes CR13 through CR16 and filtered by capacitors C2 and C3 and regulated by VR3. Regulator VR3 is located on the back panel and is connected to the power supply by the regulator cable (709-0093).

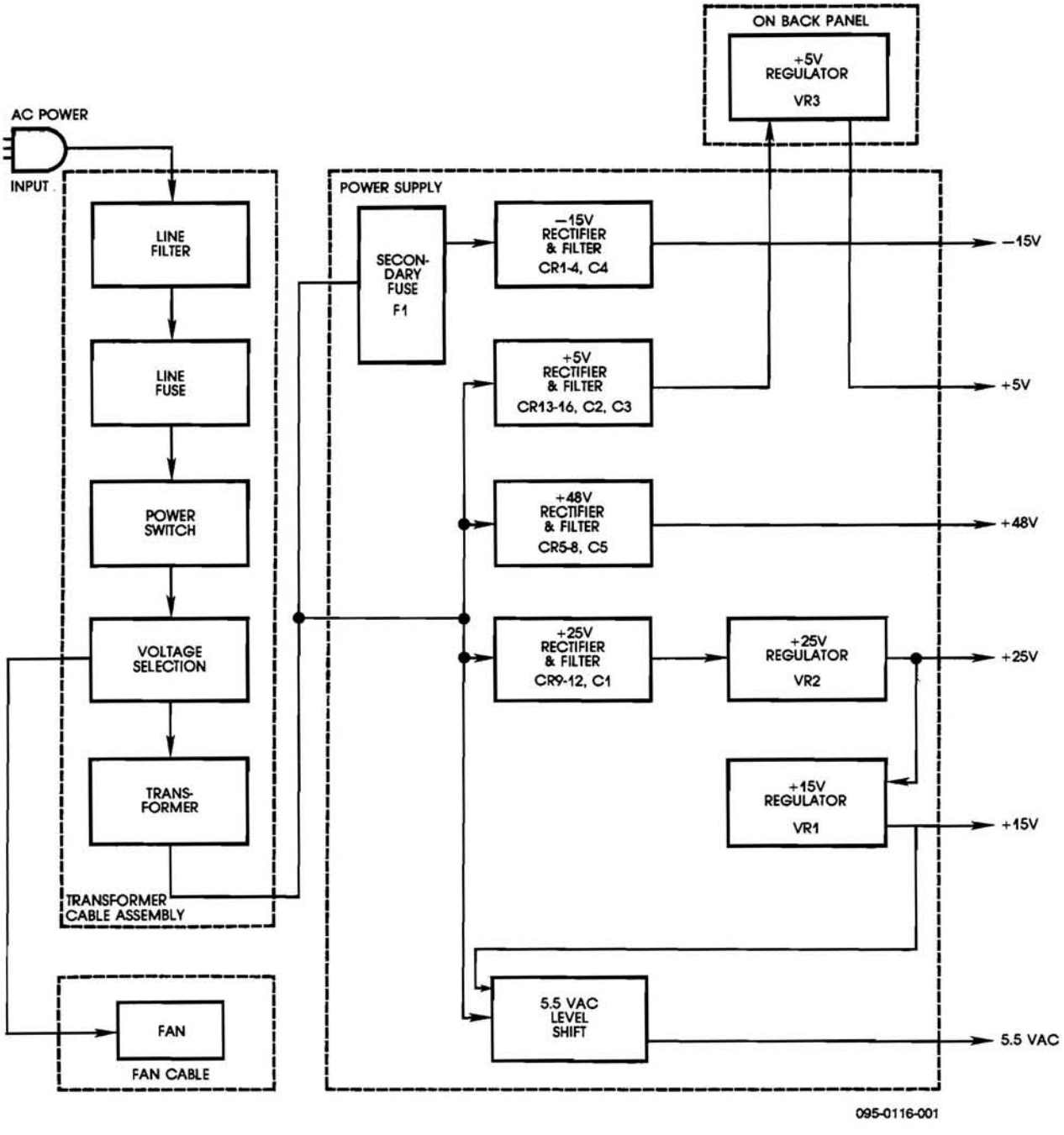


Figure 3-3. Power Supply Diagram

3.3.2 Keyboard/Display

The keyboard/display block diagram is illustrated in figure 3-4 and described in the following paragraphs.

3.3.2.1 Keyboard/Display Controller

The keyboard/display controller chip U49 is located on the controller board and provides the necessary interface signals for the display and the keyboard.

3.3.2.2 Keyboard Drive

Scan lines on the controller U49, SL0 through SL3, are decoded by U15 and applied to the matrix of keys.

3.3.2.3 Keyboard

Commands from the matrix of keys are returned to the controller U49 by way of return line RL0 through RL3 and RL7.

3.3.2.4 Display Drive

The signals for the FIP (fluorescent indicator panel) display originate from the controller outputs A0, A1, and B0 through B3. These signals are applied to the character generator PROM (U13). The character generator PROM outputs control the data segments that appear in the display. This data is timed by decoder U12 and counter U14, and is applied to the display latches U3 through U6. Segment drives U10 and U11 level shift the outputs of the display latches to the voltages required by the FIP display inputs. The four scan lines from the controller (SL0 through SL3) are decoded by U1 and U2. These lines are level shifted by digit drives U8 and U9 to provide the necessary digit select signals.

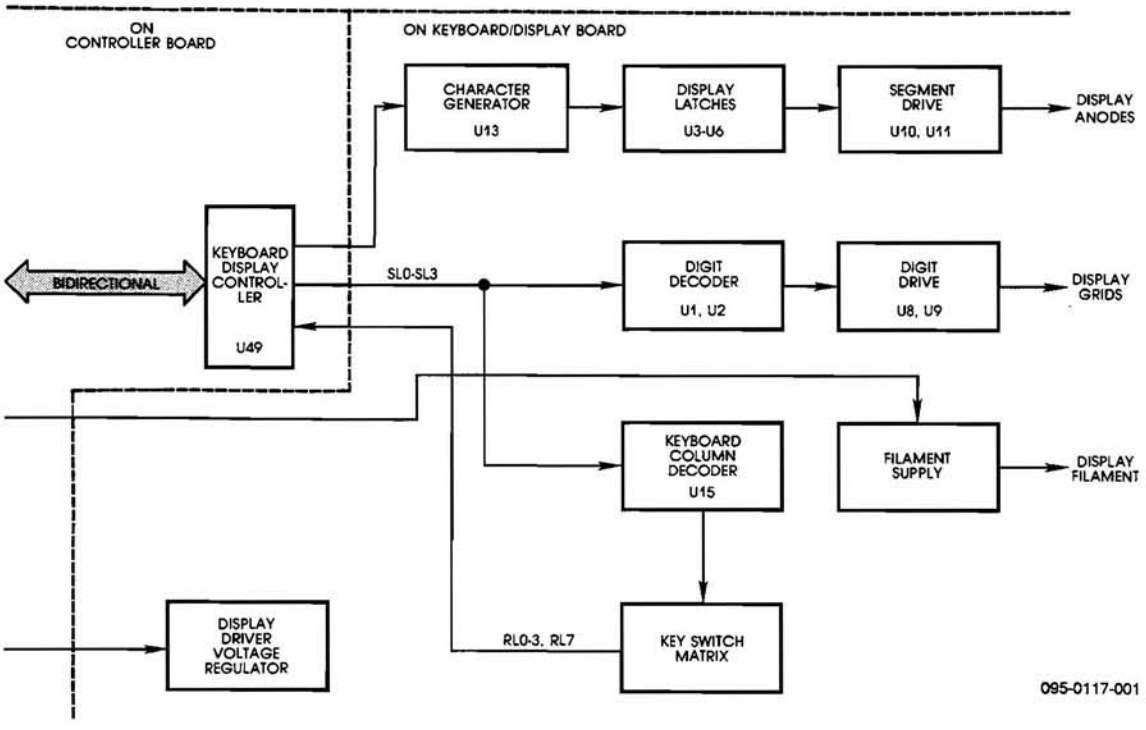


Figure 3-4. Keyboard/Display Function Block Diagram

3.3.3 Socket Adapters

The Model 60 Programmer has socket adapters that allow you to program PAL, IFL, or EPROM devices. Each of these adapters are described below.

3.3.3.1 PAL/IFL Adapters

Seven optional socket adapters are available with the Model 60. There are one PAL DIP (20/24-pin), two PAL PLCC (20/24-pin and 28/28-pin), two IFL DIP (20/24- pin and 28-pin), and two IFL PLCC (20/24-pin and 28-pin) socket adapters. These socket adapters provide the proper connections of the programmer to the device to be programmed. Since available devices differ significantly, the socket adapter accommodates these differences.

Within the socket adapter are clamp diode networks for noise suppression. Also contained in the socket adapter is a hard-wired shift register that can be read by the programmer to identify the type of adapter installed in the programmer.

3.3.3.2 40-Pin EPROM Adapter

The Model 60 EPROM adapter (refer to figure 3-5) consists of two circuit boards housed inside a plastic adapter casing. The mother board contains circuitry to allow for adapter identification, and four extension registers. This board has no circuitry or configuration dedicated to any specific device support. One of the extension registers has dedicated connections to the daughter board (extension write-only I/O lines) and two other registers are dedicated to relay control (one line each for set and reset control of eight relays). The forth register is presently not used; however, an additional select is available so that four more registers can be added for future designs.

The daughter board is dedicated to the device(s) intended to be programmed with the adapter. In addition to the ZIF socket, it contains the relays used to move VCC and ground connections to the appropriate pins on the ZIF socket. It also contains the over- voltage diode clamp circuits.

Expansion of device support to 40 pins requires adding 7 new I/O lines since the Model 60 has only 32 I/O lines. These are generated in the adapter by multiplexing the four adapter select lines in the Register Controller and converting them into a nibble bus in the I/O Expansion Line block.

In the other adapters these select lines are used to control the LED indicators and the ID register. The lines are connected in this adapters ID register in an identical manner and; therefore, can use the same identity reading routines without modification.

The adapter performs a series of operations prior to programming a device. It builds voltage level tables by taking actual voltage measurement on the device under test and builds a continuity table involving measurements and comparisons. It then checks the continuity table for an open socket and the proper justification. It then verifies for a backwards device and again performs a continuity check.

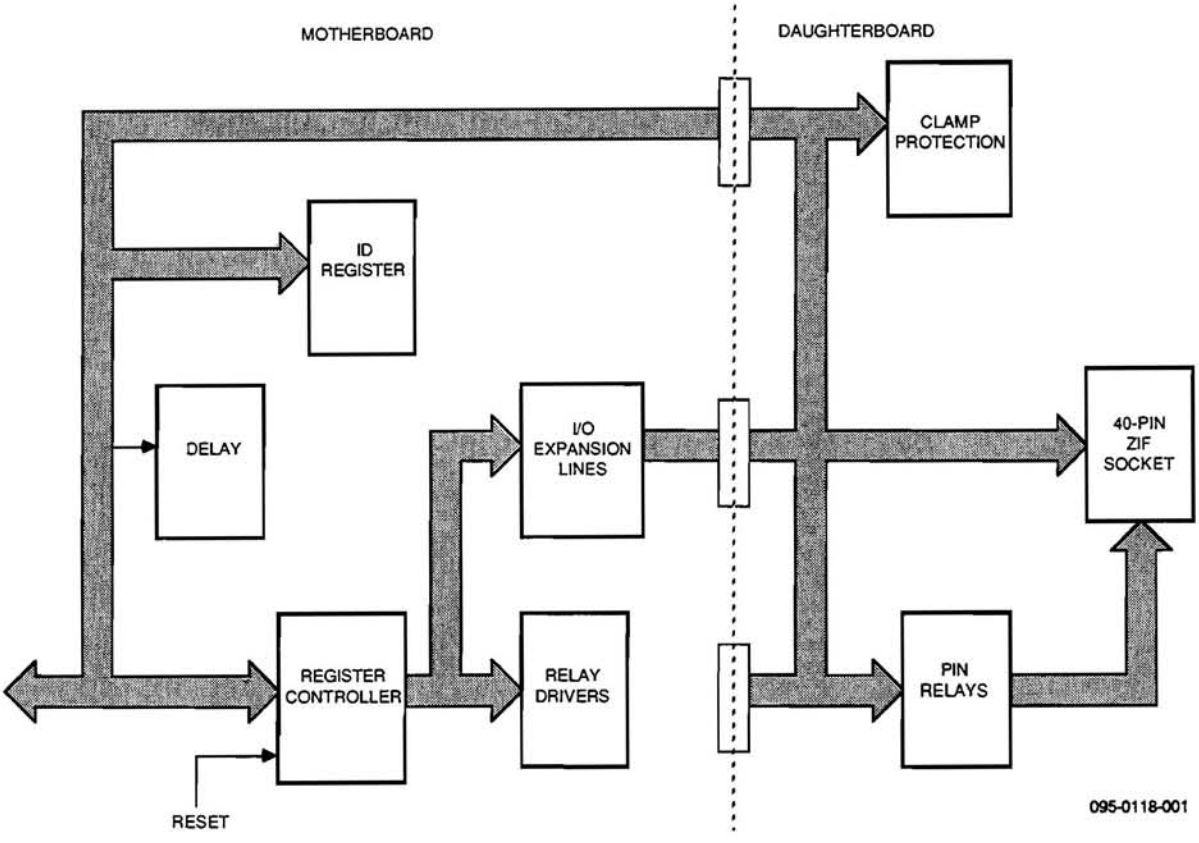


Figure 3-5. EPROM Adapter Block Diagram

Register Controller

The register controller has two modes of operation. These are: the Select Mode and the Write Mode. When the Select Mode is selected, the address on the nibble bus is 0 through 7, and a write pulse occurs, the controller selects which register (0 - 7) will be used for subsequent operations. If the address is 8 through 11 and a write pulse occurs, all of the register contents are set to zero (software reset). Addresses above 11 will have no effect on the controller. When the Write Mode is selected and a write pulse occurs, the data on the nibble bus is written into the selected register.

The controller reset command (invoked on power-up) ensures that the coils to the relays are not energized.

Delay Circuit

The write pulses used by the adapter are generated by the pulse generator on Model 60 controller board. The pulses are sent directly to the register controller and through the delay circuit so that both a direct and delayed versions of the pulse are presented to the register controller. The register enable pulse in the figure 3-6 is derived from both pulses so that data is latched into the registers early in the pulse. With the trailing edge of the pulse the address select flip-flops in the register make a transition to the next state.

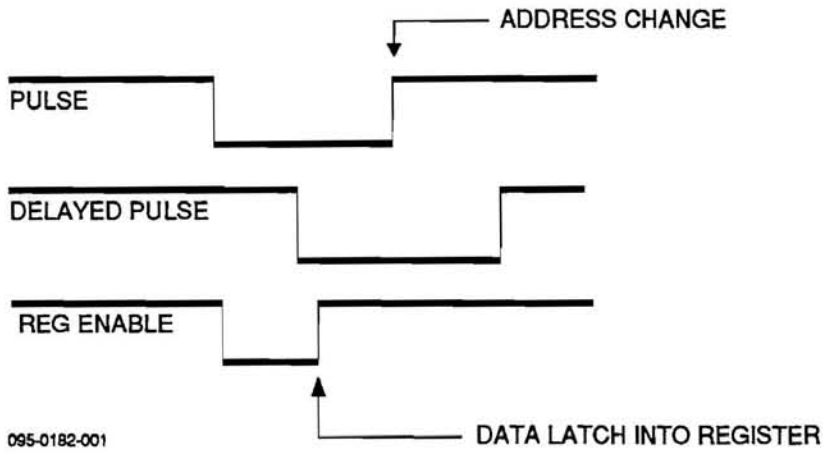


Figure 3-6. EPROM Adapter Timing Diagram1

I/O Expansion Lines

To support continuity tests the seven I/O expansion lines need to produce approximately the same drive capabilities as the other 32 I/O lines. This achieves a level on all I/O lines that are within a diode voltage drop (0.7 Volts) of each other so that the influence of a arbitrary I/O line being pulled low would be predictable. This duplicates the logic level high so that when all of the I/O lines are brought to the same logic level high (3.6 Volts in the Model 60 sink drivers), the individual lines of the IC can be toggled and the levels on the VCC and Ground connections can be monitored. From this information, backward device and pin continuity can be derived.

Relay Drivers

The relay drivers separate the register controller output from the pin relays on the daughterboard. In addition to isolating the register controller from the surge effects of relays, the devices contain a diode network (they are designed as relay drivers) to deal with surge currents.

The relays require a reset circuit to insure that the coil drivers do not remain energized when the unit is turned on, or an adapter is plugged in the main unit. Since the relay drivers could come up in a random state, the worst case situation would be having all of the relays energized simultaneously and continuously. At power up software can check this bit to see if the adapter is undergoing a hardware reset. After the hardware reset is over software can do whatever adapter initialization is required.

Pin Relays

The pin relays control the input to the pins that may be used for V_{CC} or ground. The relay drivers, based on their input from the register controller, will energize either K2 or K3 to route ground to either pin 20 (K3) or pins 11 and 30 (K2). The routing of V_{CC} is controlled by either K1 (pin 34), K4 (pin 36) or K5 (pin 32).

40-Pin Socket

All of the pins on the 40-pin socket are terminated by an I/O line except for V_{CC}. To compensate for this a relay selectable in or out voltage divider circuit is included to pull V_{CC} to the same drive and level (3.6 Vdc logic high at the device under test) as the other pins. Because of the "times-two" voltage division that occurs in the V_{CC} comparator circuit in the main unit's waveform board, voltages read by software will be half the value as seen on the other pins. Also, this causes the resolution on monitoring V_{CC} to be approximately 0.1 Volts instead of the 0.05 Volts seen on the other pins.

Clamp Protection

Of the ZIF socket pins exposed to the user, only those connected to the register controller are of concern here. All other pins are connected directly to the drivers in the Model 60's waveform board and are subject to that unit's limitations.

3.3.3.3 Handler Adapter Module (Model 60H Only)

The adapter module connects the 60-conductor ribbon cable to the Model 60H. Two P-channel MOSFETs are on the adapter as part of the overcurrent protection circuit for the CE and BIT supplies. The adapter also contains a set of ferrite beads in series with the programmer I/O lines. The ferrite beads (also found on the Adapter performance boards) present a series impedance at high frequencies to isolate the device under test from the capacitance of the cable and programmer electronics. This prevents oscillation problems with high-speed logic devices.

3.3.3.4 Handler Performance Boards (Model 60H Only)

Available for the Model 60H are handler performance boards that interface to the Model 300, MCT, and Exatron handlers. The Model 300 interface provides two performance boards, both similar in operation, a 20-pin PAL/IFL and a 24-pin PAL/IFL version (refer to figure 3-7 for a block diagram of the 24-pin performance board. The MCT/Exatron interface provides three performance boards, again similar in operation, a 20-pin PAL/IFL, a 24-pin PAL/IFL, and a 28-pin PAL only version.

The performance boards contain ferrite beads to prevent oscillations with high- speed devices, voltage spike clamps, and input capacitors. Placing this circuitry on the performance board, mounted as near as possible to the handler contactors provides optimum programming and testing performance.

On the performance boards, switching the ribbon cable between the PAL and IFL connectors causes circuit elements (input capacitors and load resistors) to be switched in or out to optimize the circuitry for programming and testing of the desired device type. The PAL/IFL switch also changes the input to an ID register. The register allows the programmer to identify which connector the cable is plugged into and indicates an error if the wrong configuration is being used for a particular device.

The boards also include transistors to provide a current-sinking capability for the VCC line. The 24-pin board has a special circuit to provide a high-speed clock (used for Logic Fingerprint) to pin 14. Finally, there is a continuity testing circuit to assure there is solid contact between the device pins and the handler's connectors.

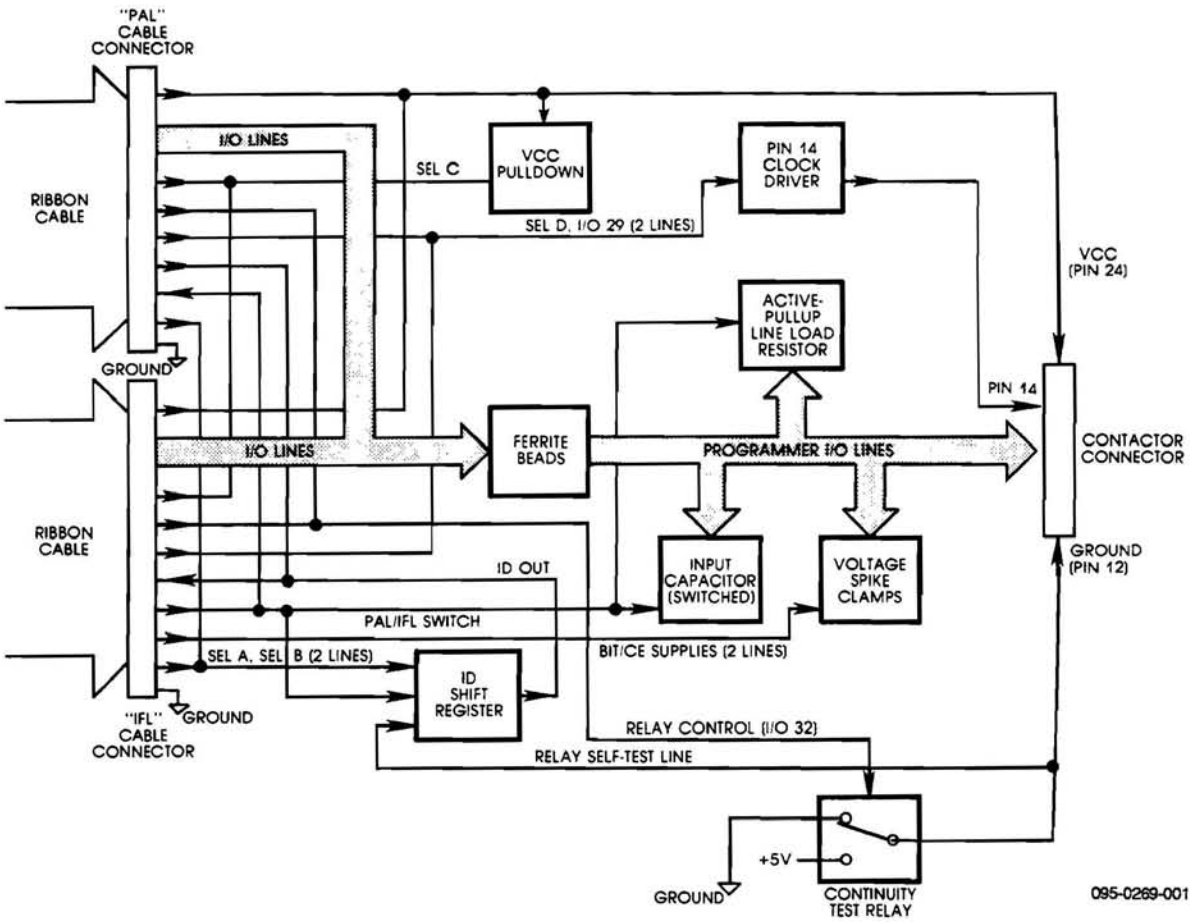


Figure 3-7. 24-Pin Performance Board Block Diagram

3.3.4 Controller

The following describes the processor portion of controller board 701-0006. The circuitry functions of the processor are described in this subsection and illustrated in figure 3-8.

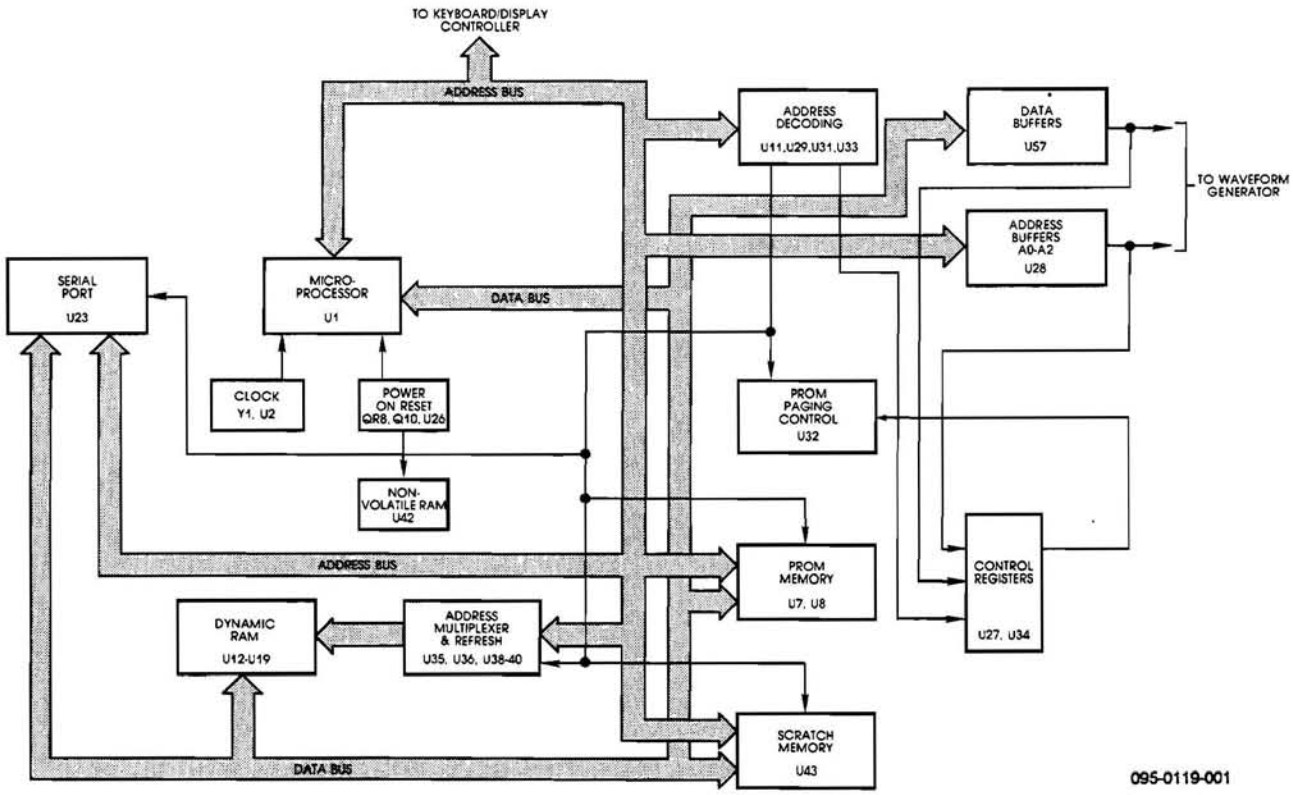


Figure 3-8. Controller Block Diagram

3.3.4.1 Microprocessor Decode and Memory

The Model 60 uses a 68A09 microprocessor. The processor clock is generated with crystal Y1 and inverter U2. The power-on reset circuit CR8, Q10 and U26 provide a reset for the processor and an array recall signal for the nonvolatile RAM U42.

The controller consists of a 16-bit address bus, an 8-bit data bus, power supply lines and control lines. The microprocessor's address bus is decoded by PAL U11 and decoders U29, U31, and U33. The address assignments are detailed in table 3-1 and figure 3-9.

Table 3-1. Address Map

Address	Function
C800-CBFF	Configuration PROM, U7-20
CC00-CC3F	Nonvolatile RAM, U42-7
CC40-CC41	Keyboard/display, U44-22
CC80-CC83	Serial port, U23-11
CD50	Pulse generator, U59-11
CD70	Scope trigger (ST2), TP16
CD80-87	Control register 1, U27-4
CD88	Nonvolatile store, U42-9
CD90-CD97	Control register 2, U34-4
CD98	Read gate 1, U55-12
CDA0	Read gate 2, U55-13
CDA8	VCC voltage DAC, U65-15
CDA9	VCC current DAC, U65-15
CDB0	Bit supply DAC, U63-15
CDB1	CE supply DAC, U63-15
CDB8	Comparator reference DAC, U61-15
CDB9	Variable load DAC, U61-15

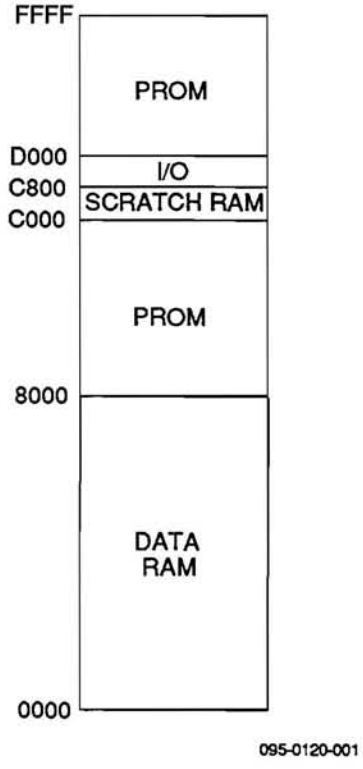


Figure 3-9. Address Map

Program memory is provided by two on-line PROMs (U7 and U8) and three page PROMs (U6, U9, and U10). Page selection of these PROMs is provided through U32 and control register U27. The microprocessor's nonvolatile and scratch RAM is provided by U42 and U43. Address assignments are shown in figure 3-9.

3.3.4.2 Data RAM

The Model 60 contains up to 256K X 8 of paged dynamic data RAM. Refresh for the dynamic RAM is generated by signals from the microprocessor using gates U37 and U41, address multiplexers (U35,U36, U39, U40) and refresh counter U38. The RAM is divided into pages which overlay the same address space. Page selection is provided by control register U27.

3.3.4.3 Serial Port

The RS232 compatible serial interface device is U6. The interface signals from U23 are shifted to the proper RS232 levels by interface of U20 and U21, and are then routed to the serial port connector. The address of the I/O port is listed in table 3-1.

3.3.4.4 Address and Data Buffers

The three lower address lines (A0 through A2) are buffered by register U28. The data lines are buffered by register U57. These two registers provide isolation between the processor and some of the circuitry located on the processor board. Address lines A3-A5 and the data bus are not buffered between the controller and waveform generator board.

3.3.4.5 Control Registers

The control registers (U27 and U34) provide the necessary control signals for other functions on the controller.

3.3.4.6 Device Voltage Signals

The device voltage supplies include Vcc, bit and chip enable (CE), reference and -9 volts. For the following descriptions, refer to the schematic 30-701-0006 located in Appendix E at the back of this manual.

The Vcc voltage is generated by DAC U65 op amp U52 and U53 and pass element Q7. The Vcc current limit is adjustable by DAC U65, op amp 53 and potentiometer R108. Feedback from the remote sense returns via potentiometer R109 to the input of op amp U52.

The voltage for the bit and CE supplies is generated from DAC U63 through op amps U49, U50 and U51 and pass elements Q9 and Q12.

The voltage reference (V Reference) provides a stable 5-volt reference for all DACs used as voltage supplies to waveform generation circuitry. It consists of regulator VR2 and transistor Q8.

The -9-volt supply is provided by regulator VR1 and provides a negative reference voltage for other waveform generation circuitry.

3.3.5 Waveform Generator Board

Figure 3-10 shows a block diagram of the functions required for the waveform generator. The waveform generator contains its own controller circuits to control and order each event of waveform generator operation. A rise-time (t/rise) circuit causes the outputs of the source drivers to rise at a selectable rate to accommodate a wide range of programmable devices. The t/rise circuit, in response to commands from the controller board, uses the BIT and/or CE supplies (contained on the controller board) to provide a control voltage to the source drivers. This control voltage developed by the t/rise circuit has a specific rise time selected by the controller board. The overall effect of circuit arrangement is that the t/rise circuit receives voltage from the BIT and CE supplies and actually controls the application of this voltage to the logic device being programmed and tested.

A series of 47 source drivers provide the fuse-blowing current and the control signals required to program the logic device installed in the socket adapter. One or two source drivers are provided for each device pin and is individually selectable by the controller board as required to perform programming and testing operations.

A series of 32 individual comparator circuits allows the comparison of the voltage level appearing at each device pin with a selected reference voltage. By reading the contents of each comparator, the controller board can determine such things as the fuse map of a device (as long as the security fuse is not blown) or the condition of the device outputs during a structured vector test.

A series of 32 sink drivers are employed to apply logic levels to the device being programmed. An optional handler port may also provided to support an automatic device handler. The handler port operates independently from the waveform generator function. The data bus from the controller board is buffered from the handler port with an 8-bit register (U34, U42) so that the controller board can issue commands to and receive responses from the handler unit.

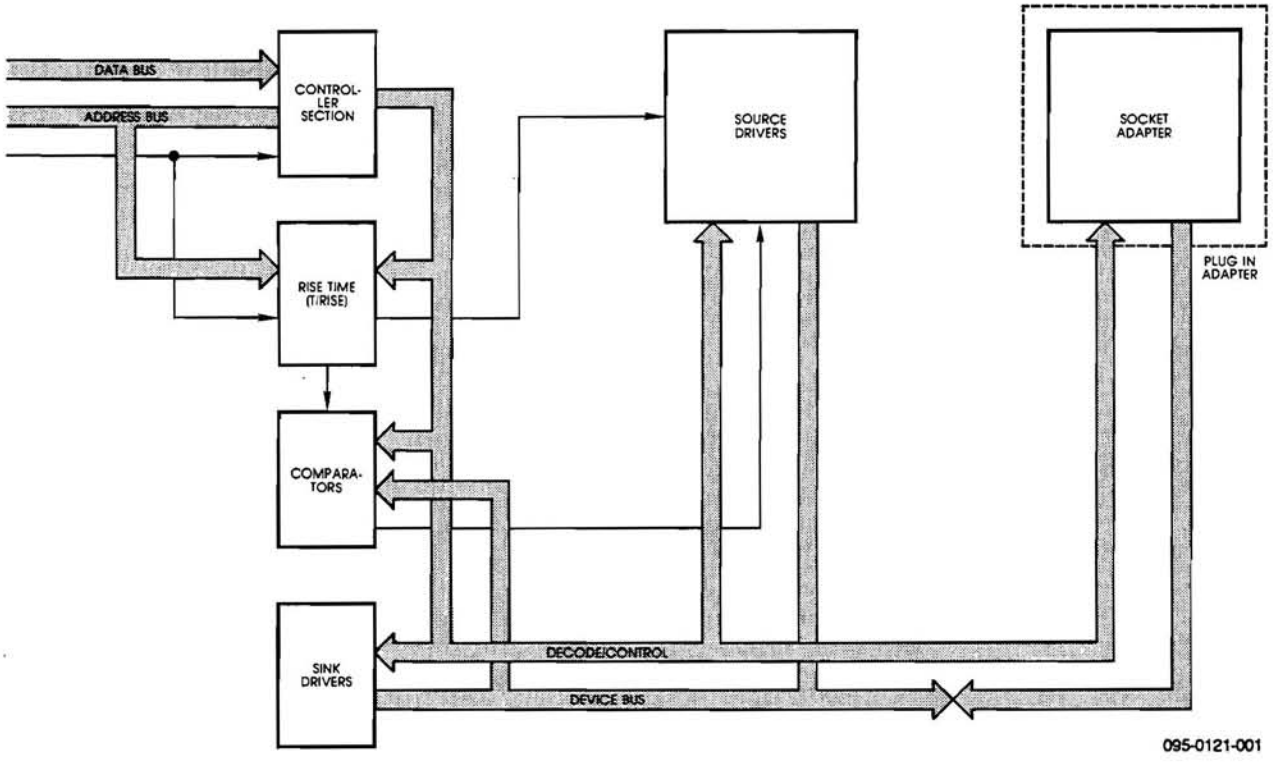


Figure 3-10. Elements of the Waveform Generator

3.3.5.1 Controller Section

The controller section is shown in the block diagram of figure 3-11. Because of the large amount of serial data that must be written and read during programming and testing operations, the controller section operates at high speed. A free-running crystal-controlled oscillator U69 produces a 6.144 MHz pulse that synchronizes the serial read and write operations, and also the logic fingerprint operations, with the microprocessor operations (on the controller board).

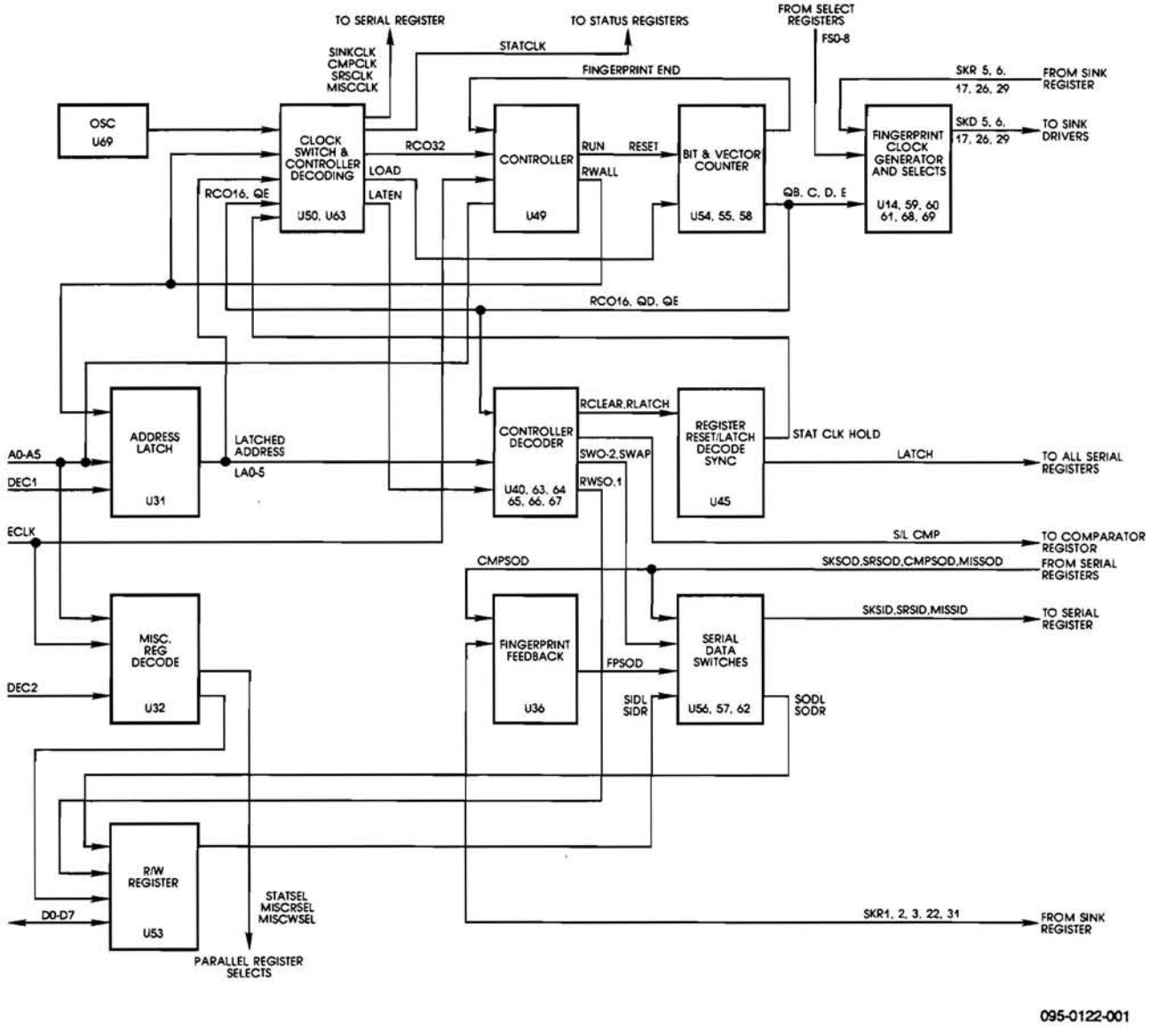


Figure 3-11. Waveform Generator, Controller Section (1 of 2)

During a microprocessor read or write operation, data is serially transferred, under direction of the controller section, between the read/write register U53 and the appropriate waveform generator section; source driver registers, sink driver registers, or comparator registers. During a read of write operation, the source driver registers, the sink driver registers, and the comparator registers appear as individual memory locations. These and other registers have separate write (CDC0-CDCF) and read (CDD0-CDDF) locations in memory since there is not R/W line provided from the controller board. Writing is accomplished by simply writing to a specific memory location.

During a read operation, the microprocessor must first read the memory address associated with the desired register, and then read the contents of the read/write register. The first read triggers the serial controller to deposit the contents at the selected register into the read/write register where it is picked up by the second read operation.

The microprocessor sends instructions to the controller section by applying the appropriate address. The address describes which high-speed cycle the controller section should perform. During each cycle, the control counter, controllers and decode logic determine what control states should exist for that cycle. These states, the counter, and the latched address are further decoded into control lines which are routed to the serial switches U56, U57, U62, and other functional blocks.

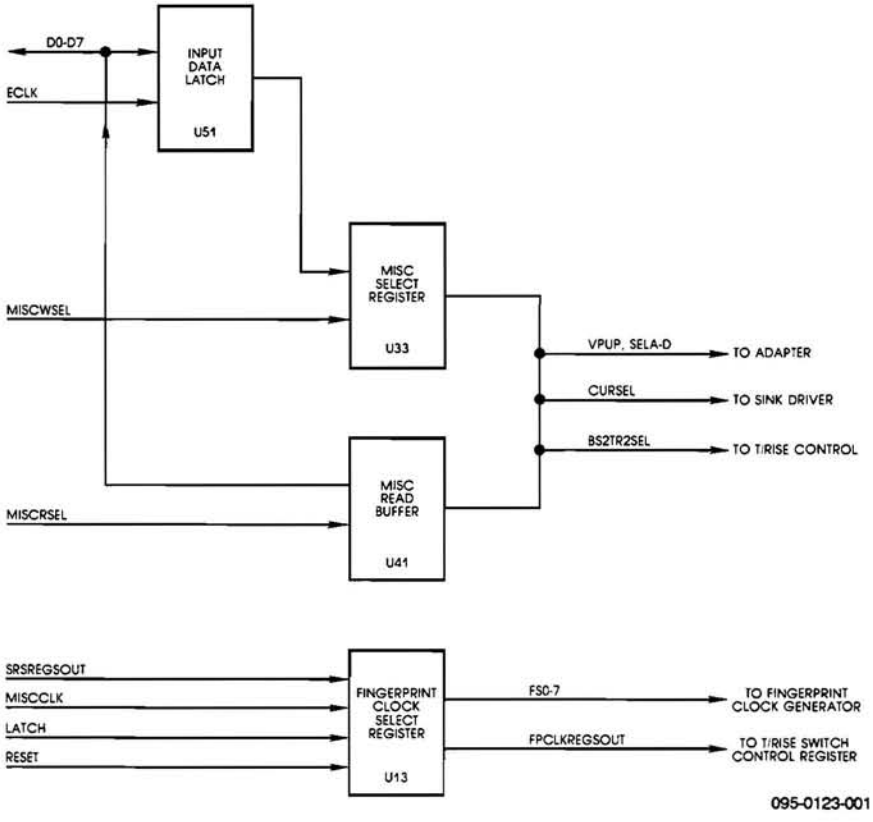


Figure 3-11. Waveform Generator, Controller Section (2 of 2)

3.3.5.2 Source Drivers

As shown in figure 3-12, a series of 47 source drivers provide the necessary current to program and test each fuse of the logic device. Each source driver is a pnp transistor switch driven by a current source and controlled by an output of the source register. The current source provides a constant base drive to the pnp switches at all switch voltages.

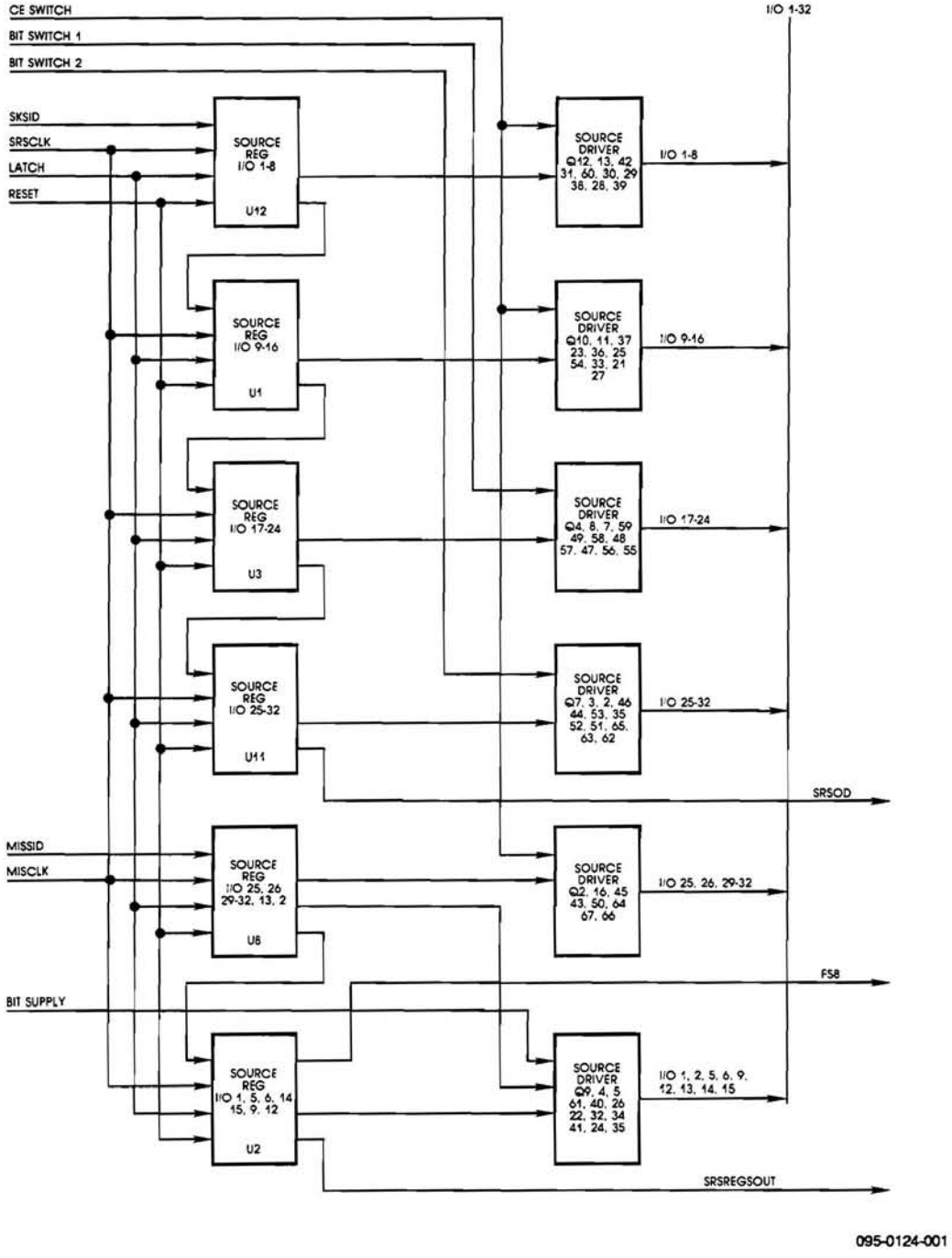


Figure 3-12. Source Drivers Section, Block Diagram

The source register is serially loaded, from the read/write register, with the on/off drive data that originates at the microprocessor on the controller board. Once the data is serially loaded, it is appears at the parallel outputs of the source register U1, U2, U3, U8, U11, U12, for application to the individual current source switches.

3.3.5.3 Sink Drivers

A series of 32 sink drivers U15, U20, U21, U30, U47, are provided, one per driver pin. These drivers provide the minimum amount of drive current necessary to establish proper logic levels for a programmable logic input. This approach is used so that, during a logic fingerprint operation, a programmable device pin (which may be an output) can successfully pull the node high or low regardless of the state of that particular sink register bit. The output comparators (U22-29) must be able to read the state of all programmable device outputs, under all logic test conditions, regardless of the state of the sink register. (Refer to figure 3-13.)

The sink driver is a resistor/diode network with pullups to a logic high. As a group, the sink driver is programmable to allow for high current (for bipolar) or low current (for CMOS). A pull up/down select circuit Q1, Q6, U18, U19 operates on command from the microprocessor to select the appropriate current drive for bipolar device testing.

The sink driver registers U7, U9, U10, U38, U43, U44, are serial shift registers with output latches. During serial shifting (during fingerprint or read/write operations) the output of the most recent vector is held in the output latches. The registers are serially loaded and unloaded under operation of the controller section.

3.3.5.4 T/Rise Circuit

The t/rise circuit, shown in figure 3-14, provides any of three individual rise time waveforms for application to their corresponding source drivers. The t/rise circuit uses the outputs of the BIT and CE supplies contained on the controller board as the destination voltage for the time rise selected. Selection between the three rise time waveforms is made by means of the switch control register, U37, which also determines the switch (BIT switch 1, BIT switch 2, or the CE switch) to be activated.

The outputs of the switches (BIT and CE) and the non- switched V_{CC} sense line are connected to the switch comparators U17. The comparators allow the switch and Vcc functions to be output as status to the status register U52. Controller-ready status along with the switch/V_{CC} status are monitored by the microprocessor over the data bus during the self-test of the programmer. The status register also contains the adapter identification bit as well as an overcurrent trip indication.

3.3.5.5 Comparators

A series of 32 comparator circuits U22-U29 allow the comparison of the voltage at each logic device pin with a selected reference voltage. The outputs of the comparators reflect the differences between the applied inputs and are loaded into the parallel inputs of the comparator output registers, as indicated in figure 3-15. The contents of the output registers (U5, U6, U39 and U48), which is the result of the compare operation, are serially shifted over to the read/write register U53. From the read/write register, the result of the compare operation is read by the microprocessor.

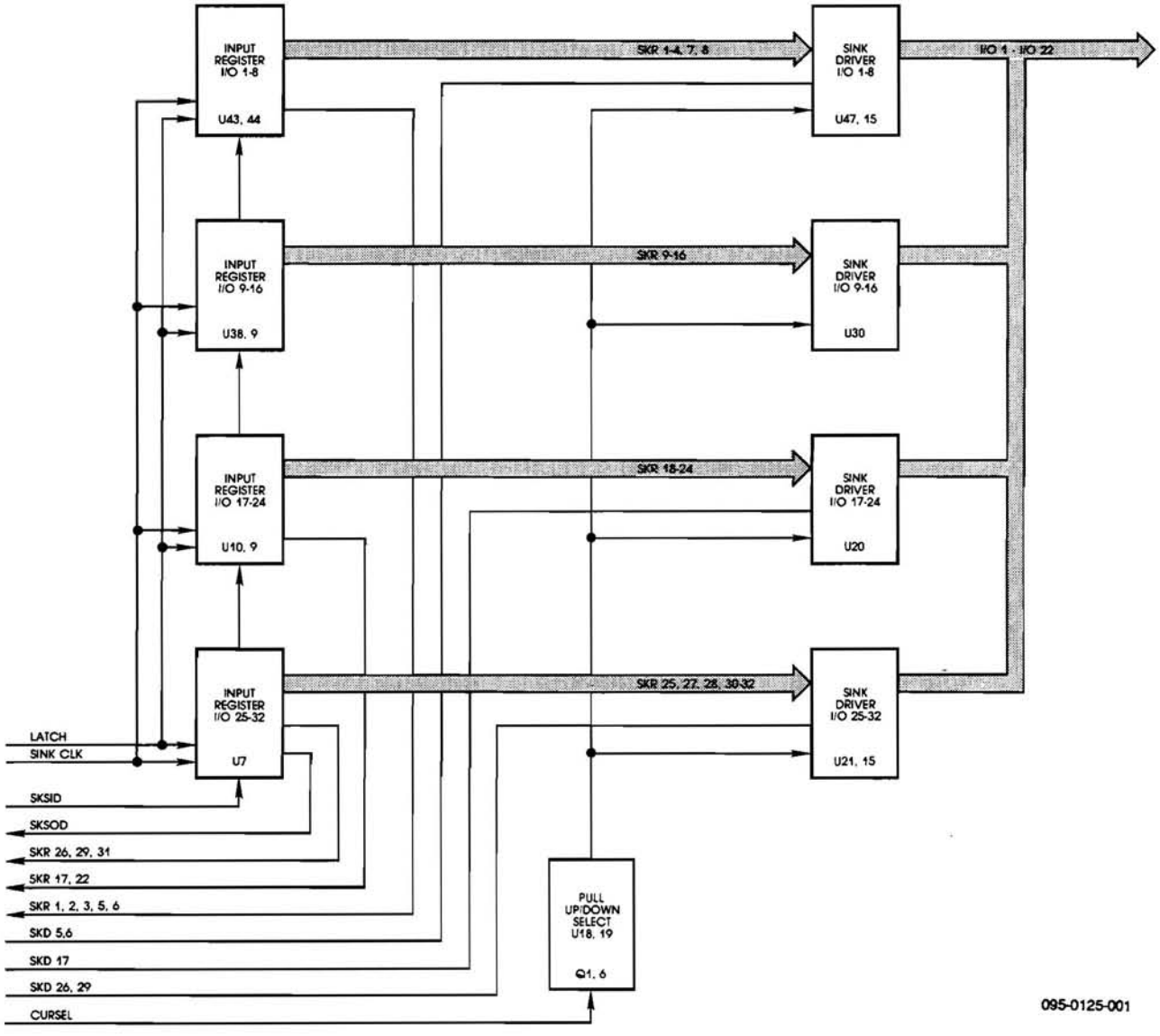


Figure 3-13. Sink Drivers Section, Block Diagram

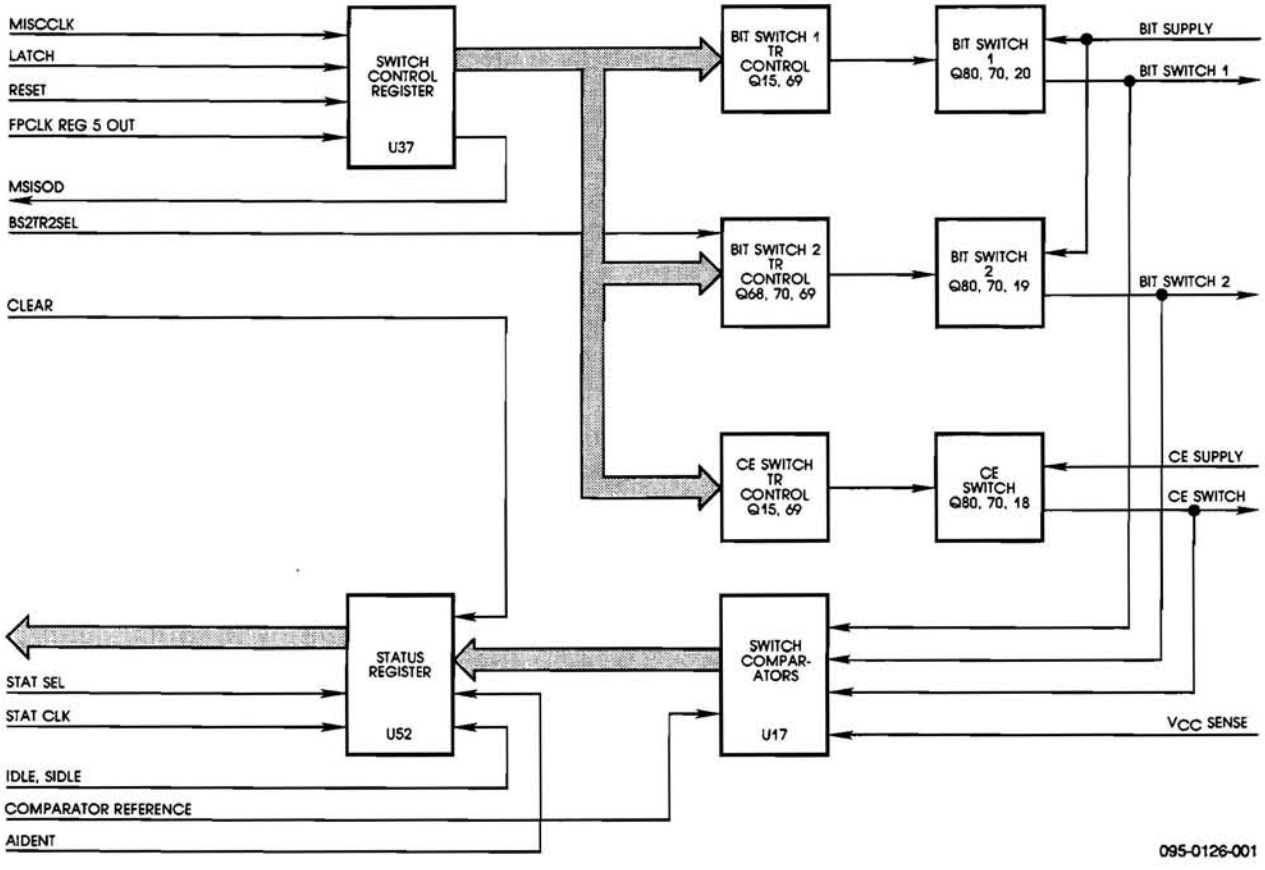


Figure 3-14. T\Rise Circuit, Block Diagram

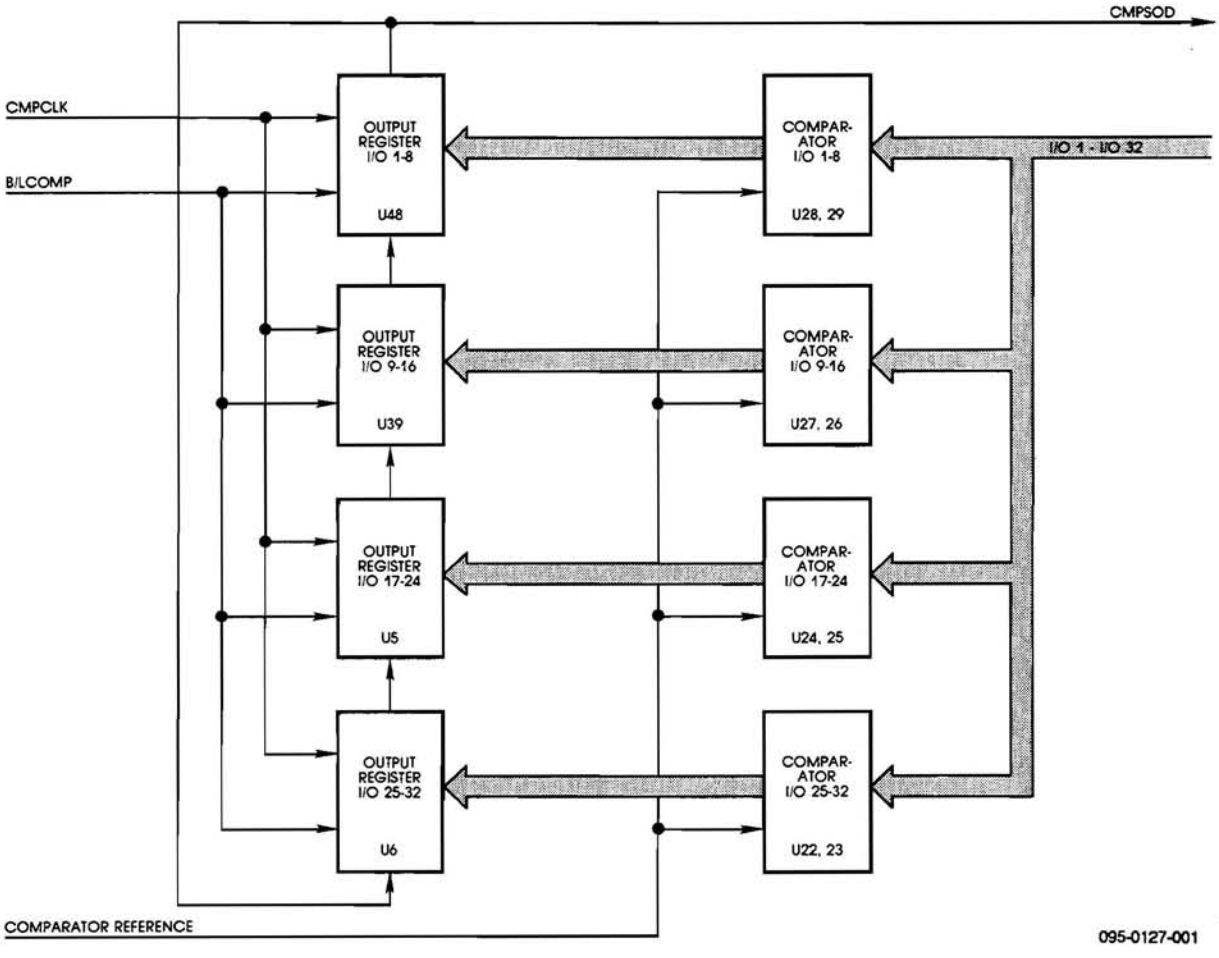


Figure 3-15. Comparator Section, Block Diagram

4. MAINTENANCE

4.1. OVERVIEW

WARNING

The instructions contained in this section are for qualified service personnel only. Do not attempt to perform them unless you are qualified to do so.

This section includes information on preventive maintenance, for your Model 60 programmer.

4.2. DISASSEMBLY/ASSEMBLY

4.2.1 Programmer Disassembly

WARNING

To avoid electrical shock, disconnect the power cord before disassembling the programmer.

To disassemble the Model 60, perform the following procedure:

1. Turn the programmer's power off.

2. Place the programmer so that its rear panel faces you. Remove the screw located in the top-central part of the rear panel (see figure 4-1a).

3. Stand the programmer on end so that the bottom of the programmer faces you. The programmer's feet should be firmly planted and the carrying handle should be pointing up.

4. Remove the eight screws from the bottom panel of the programmer (see figure 4-1b).

CAUTION

When reassembling the programmer, do not overtighten these eight screws (9.0 in-lb max).

5. Return the programmer to the normal operating position; position the carrying handle end closest to you (see figure 4-1c).

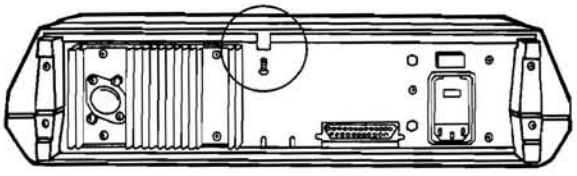
6. Firmly grip the left- and right-hand sides of the top panel; pull the panel up and toward you (see figure 4-1c). As soon as the two halves of the instrument are separated sufficiently to gain access to the interior of the instrument reach inside and disconnect the three-wire power cable connected to the waveform generator in the top cover.

7. Position the top panel as shown in figure 4-1 so that access is available to the waveform generator board (top board).

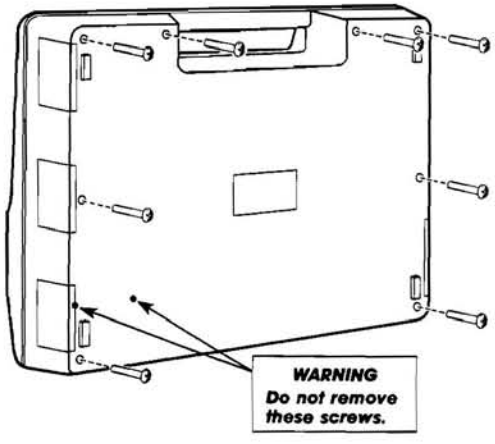
NOTE

If the Model 60 is being disassembled for periodic preventive maintenance only the disassembly procedure is completed at this point. Proceed to the Preventive Maintenance procedures in the next subsection.

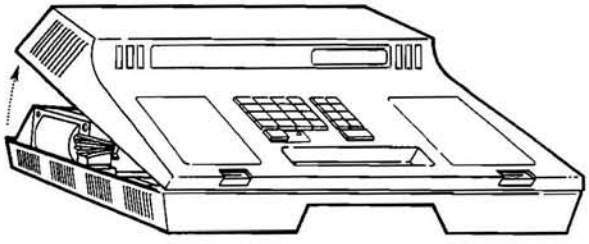
8. When any maintenance required is completed reassemble the model 60 in the reverse order of disassembly.



a) Remove the screw located in the top-central portion of the rear panel



b) Remove the eight screws from the bottom of the programmer



C) Pull the back of the programmer up and toward you until cables are taught

095-0128-001

Figure 4-1. Disassembly of the Model 60

4.2.2 Top Cover Board Removal

The waveform generator (701-0147) and keyboard/display (701-0136) are attached to the top cover. Use the following procedure to remove the replaceable assemblies from the Model 60 top cover:

1. Perform or verify completion of the programmer disassembly procedure above.

2. Spread the plastic clips on the waveform generator ribbon cable connector to release the cable.

3. Lift the ribbon cable clear of the connector.

NOTE

When removing the two screws at the top of the board slide the spacers that separate the waveform generator and keyboard/display boards out from between the boards and set them aside until you are ready for reassembly.

4. Remove the six phillips head screws securing the waveform generator board to the keyboard/display board.

5. Lift the waveform generator board clear of the top cover and place it on a smooth, flat, antistatic surface.

NOTE

If the waveform generator is that only board that needs to be removed from the cover assembly at this time skip to step 9 of this procedure.

6. Remove the four screws attaching the keyboard/display board to the top cover.

7. Lift the keyboard/display board clear of the top cover and place it on a smooth, flat, antistatic surface.

NOTE

Perform the following step only if you are replacing the display assembly on the keyboard/display board.

8. To remove the display from the keyboard/display board remove the three screws from the noncomponent side that attach the display to the board and disconnect the display from connector XDS2.

9. When any maintenance or component replacement has been completed reassemble the parts removed in the reverse order of their removal.

4.2.3 Instrument Base Board Removal

The controller (701-0132) and power supply (702-1774) are attached to the instrument base. Use the following procedure to remove the replaceable assemblies from the Model 60 instrument base:

1. Perform or verify completion of the programmer disassembly procedure above.
2. Spread the plastic clips on the controller ribbon cable connectors to release the cables.
3. Lift the ribbon cables clear of the connectors.
4. Disconnect the power supply connector from the controller board.
5. Remove the single remaining screw that secures the controller board to the instrument base (the other screws were previously removed during programmer disassembly).
6. Lift the controller board clear of the instrument base and place it on a smooth, flat, antistatic surface.

NOTE

If the controller is that only board that needs to be removed from the instrument base assembly at this time skip to step 12 of this procedure.

7. Turn the instrument base over and remove the remaining screws accessible on the instrument bottom (figure 4-1 shows these screws with the notation do not remove).
8. Slide the power module clear of the frame and set it on a clear, flat, antistatic work area.

NOTE

The three assemblies on the power module (power supply board, fan, and transformer assembly) may be removed in any order. Remove only those assemblies that require maintenance.

9. To remove the power supply board disconnect the cables from J101, J102, and J103 and remove the five screw fastening the board to the backplate; then lift the board clear of the power module.
10. To remove the fan disconnect the two wires at the spade connectors that connect the fan to the transformer and remove the two screws that fasten the fan motor to the bracket attached to the backplate. If not previously removed, remove the top three screws from the power supply board to free the fan power cable; then lift the fan clear of the bracket.

NOTE

Support the transformer assembly with your hand while removing the screws to relieve strain on the screws and prevent the assembly from falling to a hard surface.

11. To remove the transformer assembly remove the four screws securing the assembly to the backplate and lift the assembly clear.

12. When any maintenance or component replacement has been completed reassemble the parts removed in the reverse order of their removal.

4.3. PREVENTIVE MAINTENANCE

Regular preventive maintenance of the Model 60 consists of cleaning and inspection. To gain access to the inside of the programmer, follow the disassembly procedure given in below.

4.3.1 Cleaning

Inspect the Model 60 inside and out for accumulated dirt or dust. To gain access to the inside of the programmer, refer to the procedure above and figure 4-1 for disassembly instructions. To clean the Model 60, perform the following procedure:

1. Wipe any dust or dirt off the outside of the programmer with a clean, damp cloth.

CAUTION

Do not use caustic or abrasive agents; these will damage the programmer.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.3.2 Inspection

You can help prevent malfunctions by periodically inspecting your Model 60. Check cable connections, circuit board and component mountings for proper seating, wear, and visible damage.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This situation, however, is an abnormal condition. If you cannot determine the cause of the overheating, contact your nearest Data I/O service center.

5. CALIBRATION

WARNING

The instructions contained in this subsection are for qualified service personnel only. Do not attempt them unless you are qualified to do so.

The need for calibration varies with how much you use your Model 60 programmer. Generally, we suggest calibration whenever one of the following occurs:

WARNING

To avoid electric shock always test for voltage before touching when working inside the equipment.

- programming yields fall below the manufacturer's recommended minimums
- troubleshooting has been completed, or
- the user's company policy requires periodic calibration certification.

Calibration of the Model 60 consists of:

1. DC calibration — steps 1 through 7 on the measurement chart. These procedures consist of measuring and adjusting critical DC voltage levels generated by the programmer.

2. DC voltage and waveform observation — steps 12-17.

5.1. CALIBRATION EQUIPMENT

The following equipment is required for calibrating the Model 60:

- Three and a half-digit digital multimeter
- Dual-trace oscilloscope (Tektronix 465 or equivalent)
- Potentiometer adjustment tool, or 1/8-inch flatblade screwdriver
- Resistors:
  - 50-ohm, 5-watt
  - 100-ohm, 5-watt
  - 100-ohm, 1-watt
  - 10-ohm, 5-watt
  - 12-ohm, 5-watt
  - 12-ohm, 10-watt
  - 5-ohm, 5-watt

NOTE

All resistors should be within ±10% of nominal value.

5.2. DC CALIBRATION

The DC calibration procedures described in this subsection enable you to check and adjust critical DC voltage levels generated by the Model 60. The measurement charts, tables 5-1 through 5-11, list all the calibration steps.

For DIP socket adapters calibration procedures refer to table 5-1 when using a 20/24-pin programmable array logic adapter (360A-001), table 5-2 when using a 20/24-pin IFL adapter (360A-002), or table 5-3 and 5-4 when using a 40-pin EPROM adapter (360A-005).

For PLCC socket adapters calibration procedures refer to table 5-5 when using a 20/28-pin programmable array logic (JEDEC) adapter (360A- 006), table 5-6 when using a 28/28-pin programmable array logic (non- JEDEC) adapter (360A-007), table 5-7 when using a 20/28-pin IFL adapter (360A-009), or table 5-8 when using a 28-pin IFL adapter (360A-008).

For handler adapter calibration procedures refer to table 5-9 when using the Model 60H handler 20-pin performance board, table 5-10 when using the handler 24-pin performance board, or table 5-11 when using the 28-pin performance board. All performance boards use the 360A-101 adapter.

Figure 5-1 shows the DIP socket locations and figure 5-2 shows the locations of the pins to probe for the various calibration steps. Figure 5-3 shows the PLCC socket removal procedure. Figure 5-4 shows the test points and potentiometers used in verifying and adjusting voltage levels to within the values listed in the measurement chart.

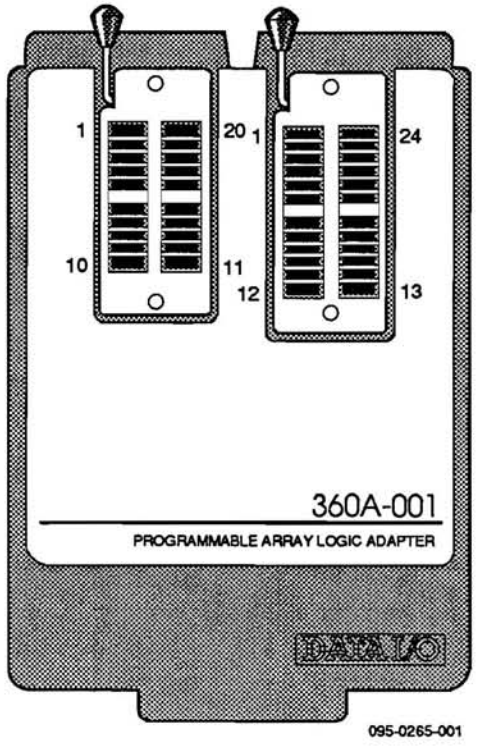
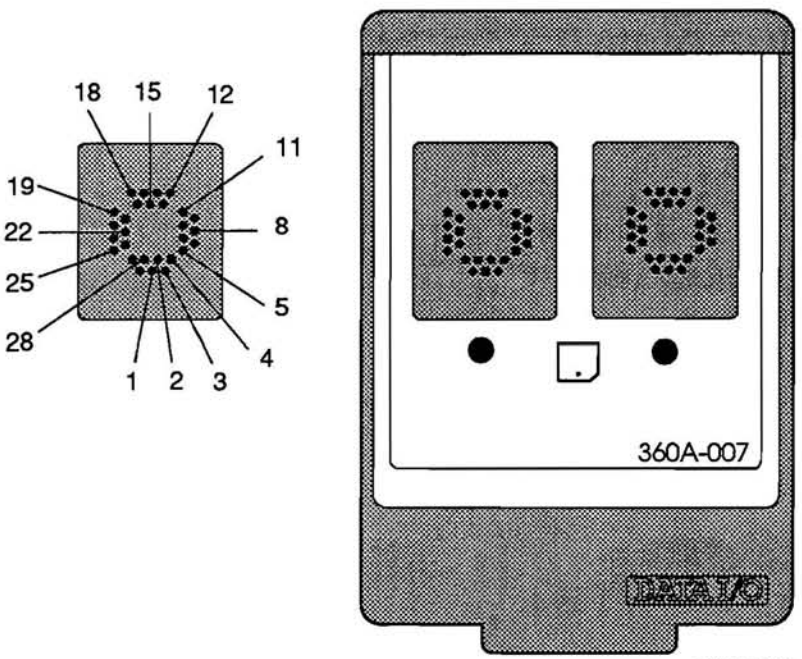


Figure 5-1. Pin Numbers of the DIP Device Sockets



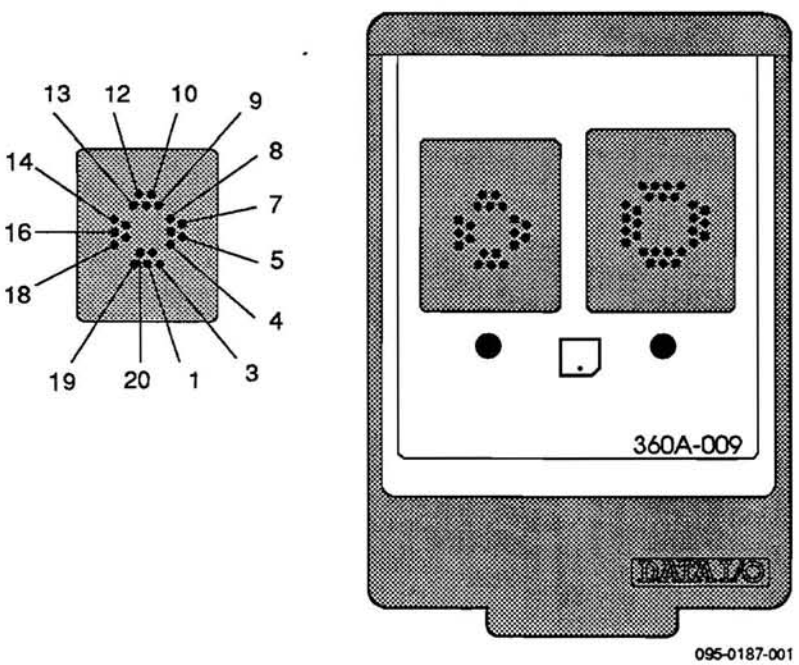


Figure 5-2. Pin Numbers of the PLCC Sockets

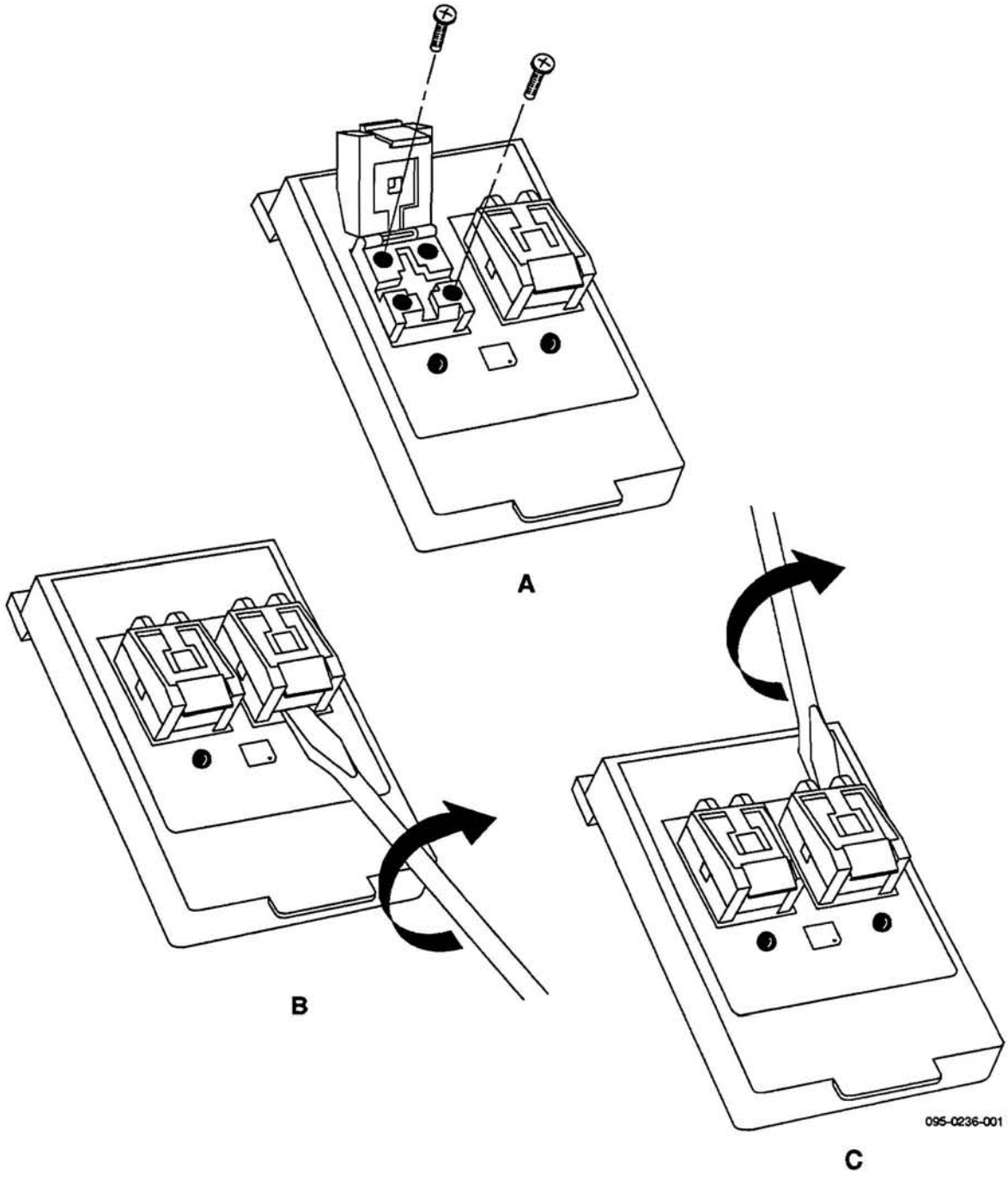
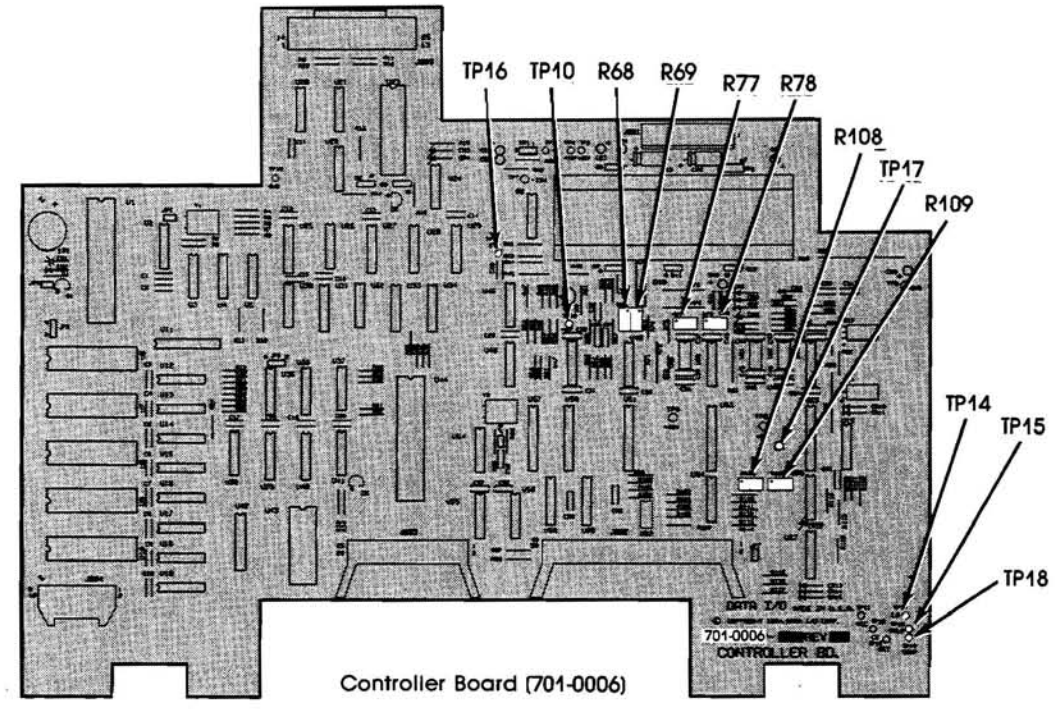
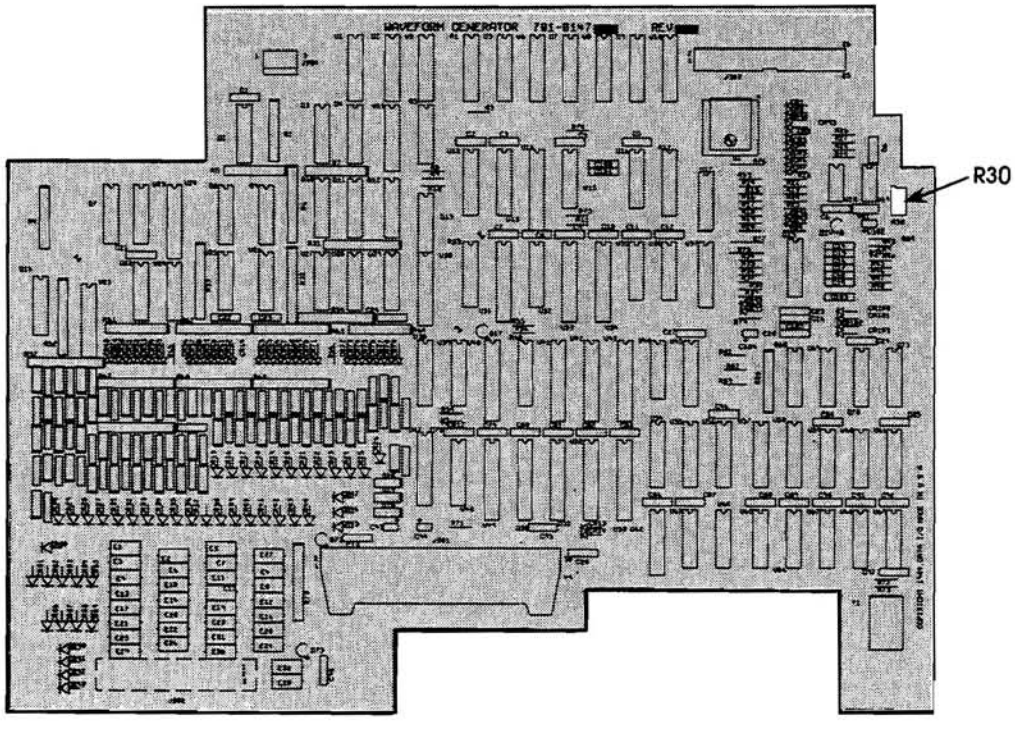


Figure 5-3. PLCC Socket Removal Procedure



Controller Board (701-0006)



Waveform Generator Board (701-0147)

Figure 5-4. Adjustments and Test Point Locations

5.2.1 Entering The Calibration Mode

Enter the calibration mode by performing the following procedure:

1. Remove any devices that may be in the front panel socket(s).

2. Turn the programmer's power on.

3. Enable the programmer's calibration mode using command code C1:

   a. Press **SELECT**.

   b. Enter C1.

   c. Press **START**.

   d. Press **START** again to execute calibration step 1, or enter desired calibration step and then press **START**.

   NOTE

   Calibration step 9 and subsequent require the procedure be repeated for each step. The procedure will not automatically increment past step 8.

   e. Use START to increment to the next calibration step; use **REVIEW** to backstep.

4. Perform the calibration steps on the measurement chart, tables 5-1, 5-2 or 5-3 and 5-4. Refer to table 5-5 for calibration error codes.

   NOTE

   Some calibration steps will not pass, or will not function, without the appropriate adapter plugged into the main unit.

5.2.2 Using The Measurement Chart

The measurement chart, table 5-1, contains the information required for all DC and optional calibration procedures. The chart contains the following column headings:

- Step Number — tells which step to use for each test. Step numbers are set at the programmer's keyboard (by pressing **START** or **REVIEW**) and are reflected in the display.
- Test Number — identifies individual tests for the calibration steps.
- Test Description — describes the function being tested.
- Measurement Test Location — tells which socket pins or test points to probe when measuring voltages.
- Measurement — specifies allowable measurement ranges.

- Adjustment Location — tells which potentiometer to adjust if a measurement is out of range.
- Comments — gives special instructions for particular tests.

For each step on the measurement chart, do the following:

- On the DIP socket adapters ground the multimeter to pin 10, 12, 14 or 20 on the adapter's 20, 24, 28 or 40 pin socket respectively (see figure 5-1).
- On the PLCC socket adapters ground the multimeter to pin 10 or 14 on the adapter's 20 or 28 pin socket respectively.
- Take measurement readings at the points indicated on the measurement chart.
- If the measurement is out of range, adjust it at the adjustment location listed for the particular step (see figure 5-4). If a reading falls outside the range and you cannot adjust it to within the range listed, call your nearest Data I/O service center; do not use the programmer until the problem is corrected.
- For waveform observation steps, refer to the waveforms which immediately follow the measurement chart. They include the bit switch rise rate and DAC waveforms.

5.2.3 PLCC Socket Test Procedures

Calibration of the PLCC Adapters requires voltage tests at the socket pins. Because of the close proximity of the pins, damage can result from shorting two or more pins with the test probes. Use the following procedure to remove the PLCC sockets from the adapter for access to the connector (refer to figure 5-3).

CAUTION

Do not attempt to perform the calibration voltage tests on the PLCC sockets. Remove the PLCC socket from the adapter and make the tests at the connectors.

1. Open the PLCC socket cover.
2. Remove the screws securing the socket to the adapter.

CAUTION

Be extremely careful when removing the socket that you do not bend any of the pins or mar the surface of the adapter. Damage to the adapter or devices could result.

3. Insert the tip of a small screwdriver between the socket and the adapter and lift the socket free so that it can be easily removed with the fingers.
4. When the calibration tests are completed replace the socket on the adapter. The pins are offset so ensure that they are properly aligned with the connector before attempting to push them into place.

Table 5-1. 20/24-Pin Programmable Array Logic Adapter Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
1	1	All pins low	24 pin/all pins 20 pin/all pins	-0.4		0.8		CAUTION [b]
2	2	Self-test, sink drivers						See Table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm 20-pin LED on, 24-pin off. For test 5-19, see note [c].
	4	Comparator reference	701-0006/TP18	1.45	1.50	1.55	R68 701-0006	CAUTION [d]
	5	V_{CC} supply	24 pin/pin 24	11.80	12.00	12.20	R109 701-0006	Load with 50Ω 5W resistor to ground [d,e].
	6	CE supply	24 pin/pin 13	19.6	19.8	20.0	R78 701-0006	Load with 100Ω 5W resistor to ground [d,e].
	7	Bit supply SW 1	24 pin/pin 19	19.6	19.8	20.0	R77 701-0006	Load with 100Ω 5W resistor to ground [d,e].
	8	Bit supply SW 2	24 pin/pin14	19.5		20.1		Load with 100Ω 5W resistor to ground [d,e].
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See Table 5-12 if errors result. Possible errors are E0-FF.
	11	LED test 2						Confirm that 24 pin socket LED is on and 20 pin LED is off.
	12	Socket pins TTL high	24 pin/pins 2,4,6,8, 10,13,16,18,19,21,23	3.0		5.2		
			20 pin/pins 2,4,6,8, 11,13,15,17,19	3.0		5.2		
	13	Socket pins TTL low	24 pin/pins 1,3,5,7, 9,11,14,15,17,20,22	-0.4		0.8		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	-0.4		0.8		
5	14	Socket pins TTL low	24 pin/pins 2,4,6,8, 10,13,16,18,19,21,23	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
			20 pin/pins 2,4,6,8, 11,13,15,17,19					
	15	Socket pins source	24 pin/pins 1,3,5,7, 9,11,14,15,17,20,22	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	3.0		5.2		

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.

Table 5-1. 20/24-Pin Programmable Array Logic Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
6	16	Socket pins source	24 pin/pins 2,4,6,8, 10,13,16,18,19,21,23	9.5		10.5		
			20 pin/pins 2,4,6,8, 13,15,17,19	9.5		10.5		
	17	Socket pins TTL high	24 pin/pins 1,3,5,7, 9,11,14,15,17,20,22	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	3.0		5.2		
7	18	Socket pins TTL high	24 pin/pins 2,4,6,8, 10,13,16,18,19,21,23	3.0		5.2		
			20 pin/pins 2,4,6,8, 11,13,15,17,19	3.0		5.2		
	19		24 pin/pins 1,3,5,7, 9,11,14,15,17,20,22	9.5		10.5		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	9.5		10.5		
8	20	Backwards device test	24 pin/pin 24 20 pin/pin 20					CAUTION [b,c] Load Error with 10Ω 5W to ground, Confirm error 32.
9	21	Overcurrent test Low range V_{CC}	24 pin/pin 24 20 pin/pin 20	9.9 9.9	10V 10V	10.1 10.1	R108 701-0006 R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed. Adjustments are interactive. Adjust until error 31 is displayed without further adjustment.
		CE switch	24 pin/pin 13				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	24 pin/pin 19				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	24 pin/pin 14				N/A	Load with 12Ω 5W to ground, confirm error 31. CAUTION [c]
10	22	Overcurrent test High range V_{CC}	24 pin/pin 24 20 pin/pin 20	9.9 9.9	10V 10V	10.1 10.1	N/A N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	23	High range V_{CC}	24 pin/pin 24 20 pin/pin 20				N/A N/A	Load with 5Ω 5W to ground, confirm error 31.
11	24	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b - Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c - Insert load resistor after pressing START; remove immediately after performing test.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.

Table 5-1. 20/24-Pin Programmable Array Logic Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
12	25	Static programming Levels						Note [b,c]
		VCCP	20 pin/pin 20	11.5		12.0		
		CE Gen VIHH	20 pin/pin 1	11.5		12.0		Voltages are for fuse 32.
		BIT Gen VIHH	20 pin/pin 19	11.5		12.0		Family PO code = 2217.
	26	Static programming Levels						
		VCCP	20 pin/pin 20	5.1		5.3		Voltages are for fuse 32.
		VIHH	20 pin/pin 1	10.75		11.25		Family PO code = 9717.
		VIHH	20 pin/pin 19	19.75		20.25		
13	27	Skip this step. Not used for calibration.						
14	28	Skip this step. Not used for calibration.						
15	29	Skip this step. Not used for calibration.						
16	30	Rise time adjust (tr2)						Adjust R30 for TR as shown on
		CE switch	24 pin/pin 2				R30 701-0147	timing diagram (this step number).
		BIT switch 1	24 pin/pin 23					All 3 rise times should be visible on
		BIT switch 2	24 pin/pin 18					all 3 pins. Verify all TR. See note [d].
17	31	Supply linearity						Verify waveforms per timing
		Vcc supply	24 pin/pin 24					diagram (this step number).
		CE supply	24 pin/pin 13					Waveforms should be linear as
		BIT supply	24 pin/pin 19					shown. See note [d].

Step 12, Test No. 26
VIHH pin 19
Voltage 18 ± .2V
As per Telcon with
Peggy Craddock at
Data I/O Customer Support
1-800-247-5700
She will FAX change.
2in

To Input Code
Press LOAD
ENTER Code 22 17
Press PROG
Press Select C1
Press Start
Press 12 - Start
Enter 82 For Fuse
Press Start
2in

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Table 5-2. 20/24-Pin IFL Adapter Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
1	1	All pins low	24 pin/all pins 20 pin/all pins	-0.4		0.8		CAUTION [b]
2	2	Self-test, sink drivers						See Table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm 20-pin LED on, 24-pin off. For test 5-19, see note [c].
	4	Comparator reference	701-0006/TP18	1.45	1.50	1.55	R68 701-0006	CAUTION [d,e]
	5	V_{CC} supply	24 pin/pin 24	11.8	12.0	12.2	R109 701-0006	Load with 50Ω 5W resistor to ground [d,e].
	6	CE supply	24 pin/pin 17	19.6	19.8	20.0	R78 701-0006	Load with 100Ω 5W resistor to ground [d,e].
	7	Bit supply SW 1	24 pin/pin 10	19.6	19.8	20.0	R77 701-0006	Load with 100Ω 5W resistor to ground [d,e].
	8	Bit supply SW 2	24 pin/pin 13	19.5		20.1		Load with 100Ω 5W resistor to ground [d,e].
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See Table 5-12 if errors result. Possible errors are E0-FF.
	11	LED test 2						Confirm that 24 pin socket LED is on and 20 pin LED is off.
	12	Socket pins TTL high	24 pin/pins 1,2,6,8, 10,14,16,17,18,20,22	3.0		5.2		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	3.0		5.2		
	13	Socket pins TTL low	24 pin/pins 3,4,5,7, 9,11,13,15,19,21,23	-0.4		0.8		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	-0.4		0.8		
5	14	Socket pins TTL low	24 pin/pins 1,2,6,8, 10,14,16,17,18,20,22	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
			20 pin/pins 2,4,6,8, 12,14,16,17,19					
	15	Socket pins source	24 pin/pins 3,4,5,7, 9,11,13,15,19,21,23	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	3.0		5.2		

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.

Table 5-2. 20/24-Pin IFL Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
6	16	Socket pins source	24 pin/pins 2,6,8,10, 14,16,17,18,20,22	9.5		10.5		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	9.5		10.5		
	17	Socket pins TTL high	24 pin/pins 1,3,4,5, 7,9,11,13,15,19,21,23	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	3.0		5.2		
7	18	Socket pins TTL high	24 pin/pins 1,2,6,8, 10,14,16,17,18,20,22	3.0		5.2		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	3.0		5.2		
	19	Socket pins source	24 pin/pins 3,4,5,7, 9,11,13,15,19,21,23	9.5		10.5		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	9.5		10.5		
8	20	Backwards device test	24 pin/pin 24 20 pin/pin 20					CAUTION [b,c] Load with 10Ω 5W to ground, Confirm error 32.
9	21	Overcurrent test Low range V_{CC}	 24 pin/pin 24 20 pin/pin 20	 9.9 9.9	 10V 10V	 10.1 10.1	 R108 701-0006 R108 701-0006	CAUTION [c] Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed. Adjustments are interactive. Adjust until error 31 is displayed without further adjustment.
		CE switch	24 pin/pin 17				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	24 pin/pin 10				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	24 pin/pin 13				N/A	Load with 12Ω 5W to ground, confirm error 31. CAUTION [c]
10	22	Overcurrent test High range V_{CC}	 24 pin/pin 24 20 pin/pin 20	 9.9 9.9	 10V 10V	 10.1 10.1	 N/A N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	23	High range V_{CC}	24 pin/pin 24 20 pin/pin 20				N/A N/A	Load with 5Ω 5W to ground, confirm error 31.

a-Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b-Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c-Insert load resistor after pressing START; remove immediately after performing test.

Table 5-2. 20/24-Pin IFL Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 10 or 12 [a])
11	24	Skip this test. Not used for calibration.						
12	25	Static programming Levels						Note [b,c]
		VCCP	24 pin/pin 24	4.9		5.1		
		CE Gen VIHH	24 pin/pin 1	17.25		17.75		Voltages are for fuse 32.
		BIT Gen VIHH	24 pin/pin 23	9.75		10.25		Family PO code = 9669.
	26	Static programming Levels						
		VCCP	20 pin/pin 20	8.4		8.6		Voltages are for fuse 32.
		VIHH	20 pin/pin 18	14.55		15.05		Family PO code = 9666.
13	27	Skip this test. Not used for calibration.						
14	28	Skip this test. Not used for calibration.						
15	29	Skip this test. Not used for calibration.						
16	30	Rise time adjust (tr2)						Adjust R30 for TR as shown on
		CE switch	24 pin/pin 22				R30 701-0147	timing diagram (this step number).
		BIT switch 1	24 pin/pin 16					All 3 rise times should be visible on
		BIT switch 2	24 pin/pin 8					all 3 pins. Verify all TR. See note [d].
17	31	Supply linearity						Verify waveforms per timing diagram
		V_{CC} supply	24 pin/pin 24					(this step number). Waveforms
		CE supply	24 pin/pin 17					should be linear as shown.
		BIT supply	24 pin/pin 10					See note [d].

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 12 on a 24-pin socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Table 5-3. 40-Pin EPROM Adapter Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments
1	1	All pins low	40 pin/all pins	-.1		.3		Ground pin 20
2	2	TTL self check						
3	3	Comparator reference	701-006/7P18	1.45	1.5	1.55	R68 701-0006	Use family/pin 93/32 CAUTION:
	4	V_{CC} Supply	40 pin/pin 34	11.80	12.00	12.20	R108 701-0006	Load with 50Ω 5W resistor to ground.
	5	CE Supply	40 pin/pin 1	19.60	19.80	20.00	R78 701-0006	Load with 100Ω 5W resistor to ground.
	6	Bit Supply	40 pin/pin 19	19.60	19.80	20.00	R77 701-0006	Load with 100Ω 5W resistor to ground.
	7	DAC reference	701-0006/7P10	4.80		5.20		
4	8	Even pins TTL high, odd pins low	40 pin/ pins 2,4,6,8, 10,12,14,16,18,22,24, 26,28,30,32,34,36	3.0		5.2		Ground is pin 20
5	9	Odd pins TTL high, even pins low	40 pin/pins 1,3,5,7, 9,11,13,15,17,19,21, 23,25,27,29,31,33, 35,37,39	3.0		5.2		Ground is pin 20
6	10	Even pins to 20V	40 pin/pins 2,4,6,8 10,12,14,16,18,22, 24,26,28,30	19.5		20.2		Ground is pin 20
7	11	Odd pins to 20V	40 pin/pins 1,3,5,7, 9,11,13,15,17,19,21, 23,25,27,29,33,35	19.5		20.2		Ground is pin 20
8		Skip this step. Not used for calibration.						
9		Skip this step. Not used for calibration						
10		Skip this step. Not used for calibration						
11	12	Test Relays	See table 1					

Relay Tests

Perform the following:

1. Press **[SELECT] C1 [START] 11 [START] [START]**

2. Confirm `RELAY TEST K1 1` is displayed.

3. Confirm the voltage is present on the corresponding pins for each relay step below. To advance to the next relay test press **[START]**

Table 5-4. 40-Pin EPROM Adapter Relay Test

Relay	Step	Ground	Pin #'s	Voltage Max.	Voltage Min.
K1	1	20	34	5.2V	4.8V
K1	2	20	34	.8V	-0.1V
K1	3	20	34	5V	2.4V
K1	4	20	34	.8V	-0.1V
K2	1	20	11 & 30	5V	2.4V
K2	2	20	11 & 30	.8V	-0.1V
K2	3	20	11	.8V	-0.1V
		20	30	5V	2.4V
K2	4	20	11 & 30	.05V	0V
K2	5	20	11 & 30	.05V	0V
K3	1	11	20	5V	2.4V
K3	2	11	20	.05V	0V
K3	3	11	20	.05V	0V
K4	1	20	36	5.2V	4.8V
K4	2	20	36	.8V	-0.1V
K4	3	20	36	5V	2.4V
K4	4	20	36	.8V	-0.1V
K5	1	20	32	5.2V	4.8V
K5	2	20	32	.8V	-0.1V
K5	3	20	32	5V	2.4V
K5	4	20	32	.8V	-0.1V

K6 Pass if no errors

Table 5-5. 20/28-Pin PLCC Programmable Array Logic Adapter (JEDEC) Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10, 14, or 15 [a])
1	1	All pins low	20 pin/all pins 28 pin/all pins	-0.4		0.8		CAUTION [b,f]
2	2	Self-test, sink drivers						See Table 5-12 if error results; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm 20-pin LED on, 28-pin off.
	4	Comparator reference	701-0006/TP18	1.45	1.5	1.55	R68 701-0006	CAUTION [d]
	5	V_{CC} supply	28 pin/pin 28	11.8	12.0	12.2	R109 701-0006	Load with 50-ohm 5W resistor to ground. [d,e,f]
	6	CE supply	28 pin/pin 16	19.6	19.8	20.0	R78 701-0006	Load with 100-ohm 5W resistor to ground. [d,e,f]
	7	Bit supply SW 1	28 pin/pin 23	19.6	19.8	20.0	R77 701-0006	Load with 100-ohm 5W resistor to ground. [d,e,f]
	8	Bit supply SW 2	28 pin/pin 17	19.5		20.1		
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See table 5-12 if error results Possible errors are E0-FF.
	11	LED test 2						Confirm that 28 pin socket LED is on and 20 pin LED is off.
	12	Socket pins TTL high	28 pin/pins 3,5,7,10, 12,16,19,21,23,25,27	3.0		5.2		
			20 pin/pins 2,4,6,8, 11,13,15,17,19	3.0		5.2		
	13	Socket pins TTL low	28 pin/pins 2,4,6,9, 11,13,17,18,20,24,26	-0.4		0.8		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	-0.4		0.8		
5	14	Socket pins TTL low	28 pin/pins 3,5,7,10, 12,16,19,21,23,25,27	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
			20 pin/pins 2,4,6,8, 11,13,15,17,19	-0.4		0.8		
	15	Socket pin source	28 pin/pins 2,4,6,9, 11,13,17,18,20,24,26	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	3.0		5.2		

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 or 15 on a 28-pin socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.
f - Remove PLCC socket cover to ease measuring.

Table 5-5. 20/28-Pin PLCC Programmable Array Logic Adapter (JEDEC) Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10, 14, or 15 [a])
6	16	Socket pins source	28 pin/pins 3,5,7,10, 12,16,19,21,23,25,27	9.5		10.5		
			20 pin/pins 2,4,6,8, 13,15,17,19	9.5		10.5		
	17	Socket pins TTL high	28 pin/pins 2,4,6,9, 11,13,17,18,20,24,26	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	3.0		5.2		
7	18	Socket pins TTL high	28 pin/pins 3,5,7,10, 12,16,19,21,23,25,27	3.0		5.2		
			20 pin/pins 2,4,6,8, 11,13,15,17,19	3.0		5.2		
	19		28 pin/pins 2,4,6,9, 11,13,17,18,20,24,26	9.5		10.5		
			20 pin/pins 1,3,5,7, 9,12,14,16,18	9.5		10.5		
8	20	Backward device list	28 pin/pin 28 20 pin/pin 20					CAUTION [b,c] Load with 10Ω 5W to ground, confirm error 32.
9	21	Overcurrent test Low range V_{CC}	28 pin/pin 28 20 pin/pin 20	9.9 9.9	10V 10V	10.1 10.1	R108 701-0006 R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed. Adjustments are interactive. Adjust until error 31 is displayed without further adjustment.
		CE switch	28 pin/pin 16				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	28 pin/pin 23				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	28 pin/pin 17				N/A	Load with 12Ω 5W to ground, confirm error 31.
10	22	Overcurrent test						
		High range V_{CC}	28 pin/pin 28 20 pin/pin 20	9.9 9.9	10.0 10.0	10.1 10.1	N/A N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	23	High range V_{CC}	28 pin/pin 28 20 pin/pin 20				N/A N/A	Load with 5Ω 5W to ground, confirm error 31.
11	24	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 or 15 on a 28-pin socket.
b - Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c - Insert load resistor after pressing START; remove immediately after performing test.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.

Table 5-5. 20/28-Pin PLCC Programmable Array Logic Adapter (JEDEC) Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10, 14, or 15 [a])
12	25	Static programming Levels						Note [b,c]
		VCCP	20 pin/pin 20	11.5		12.0		Voltages are for fuse 32.
		CE Gen VIHH	20 pin/pin 1	11.5		12.0		Family PO code = 2217.
	26	Static programming Levels						
		VCCP	20 pin/pin 20	5.1		5.3		Voltages are for fuse 32.
		VIHH	20 pin/pin 1	10.75		11.25		Family PO code = 9717.
		VIHH	20 pin/pin 19	19.75		20.25		
13	27	Skip this test. Not used for calibration.						
14	28	Skip this test. Not used for calibration.						
15	29	Skip this test. Not used for calibration.						
16	30	Rise time adjustment (tr2)						Adjust R30 for TR as shown on
		CE switch	28 pin/pin 3				R30 701-0147	timing diagram (this step number).
		BIT switch 1	28 pin/pin 27					All 3 rise times should be visible on
		BIT switch 2	28 pin/pin 21					all 3 pins. Verify all TR. See note [d].
17	31	Supply Linearity						Verify waveforms per timing
		V_{CC} supply	28 pin/pin28					diagram (this step number).
		CE supply	28 pin/pin 16					Waveforms should be linear as
		BIT supply	28 pin/pin 23					shown. See note [d].
18	32	Relay testing	20 pin/pin 20 (V_{CC})					Short V_{CC} and GND pins together
			20 pin/pin 10 (GND)				and hit START. If no error occurs,	relay is okay.

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 or 15 on a 28-pin socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Table 5-6. 28/28-Pin PLCC Programmable Array Logic Adapter (Non-JEDEC) Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 14 or 15 [a])
1	1	All pins low	28 pin/all pins R [g] 28 pin/all pins L	-0.4		0.8		CAUTION [b,f]
2	2	Self-test, sink drivers						See Table 5-12 if error results; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm left LED on, right LED off.
	4	Comparator reference	701-0006/TP18	1.45	1.5	1.55	R68 701-0006	CAUTION [d]
	5	V_{CC} supply	28 pin/pin 28, R or L	11.8	12.0	12.2	R109 701-0006	Load with 50Ω 5W resistor to ground. [d,e,f]
	6	CE supply	28 pin/pin 16, R or L	19.6	19.8	20.0	R78 701-0006	Load with 100Ω 5W resistor to ground. [d,e,f]
	7	Bit supply SW 1	28 pin/pin 23, R or L	19.6	19.8	20.0	R77 701-0006	Load with 100Ω 5W resistor to ground. [d,e,f]
	8	Bit supply SW 2	28 pin/pin 17, R or L	19.5		20.1		
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See table 5-12 if error results Possible errors are E0-FF.
	11	LED test 2						Confirm that right LED is on and left LED is off.
	12	Socket pins TTL high	28 pin R/pins 3,5,7,9, 12,16,20,22,23,25,27	3.0		5.2		
			28 pin L/pins 2,4,7,10, 13,16,20,22,23,25,27	3.0		5.2		
	13	Socket pins TTL low	28 pin R/pins 2,4,6,8, 10,13,17,18,21,24,26	-0.4		0.8		
			28 pin L/pins 1,3,6,9, 12,14,17,18,19,21,24,26	-0.4		0.8		
5	14	Socket pins TTL low	28 pin R/pins 3,5,7,9, 12,16,20,22,23,25,27	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
			28 pin L/pins 2,4,7,10, 13,16,20,22,25,27	-0.4		0.8		
	15	Socket pin source	28 pin R/pins 2,4,6,8, 10,13,17,18,21,24,26	3.0		5.2		
			28 pin L/pins 1,3,6,9, 12,14,17,18,21,24,26	3.0		5.2		

a - Connect the ground of the DVM to ground pin 14 or 15 on the right socket or to pin 15 on the left socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.
f - Remove PLCC socket cover to ease measuring.
g - R is the right socket, L is the left socket.

Table 5-6. 28/28-Pin PLCC Programmable Array Logic Adapter (Non-JEDEC) Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 14 or 15 [a])
6	16	Socket pins source	28 pin R/pins 3,5,7,9, 12,16,20,22,23,25,27	9.5		10.5		
			28 pin L/pins 2,4,7,10, 13,16,20,22,23,25,27	9.5		10.5		
	17	Socket pins TTL high	28 pin R/pins 2,4,6,8, 10,13,17,18,21,24,26	3.0		5.2		
			28 pin L/pins 1,3,6,9, 12,14,17,18,21,24,26	3.0		5.2		
7	18	Socket pins TTL high	28 pin R/pins 3,5,7,9, 12,16,20,22,23,25,27	3.0		5.2		
			28 pin L/pins 2,4,7,10, 13,16,20,22,23,25,27	3.0		5.2		
	19		28 pin R/pins 2,4,6,8, 10,13,17,18,21,24,26	9.5		10.5		
			28 pin L/pins 1,3,6,9,12, 14,17,18,21,24,26	9.5		10.5		
8	20	Backward device list	28 pin/pin 28, R and L R socket ground = pin 14 and 15 L socket ground = pin 15					CAUTION [b,c] Load with 10Ω 5W to ground, confirm error 32.
9	21	Overcurrent test Low range Vcc	28 pin/pin 28, R and L	9.9	10V	10.1	R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed.
		CE switch	28 pin/pin 16, R and L				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	28 pin/pin 23, R and L				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	28 pin/pin 17, R and L				N/A	Load with 12Ω 5W to ground, confirm error 31. CAUTION [c]
10	22	Overcurrent test High range Vcc	28 pin/pin 28, R and L	9.9	10.0	10.1	N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	23	High range Vcc	28 pin/pin 28, R and L				N/A	Load with 5Ω 5W to ground, confirm error 31.
11	24	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to ground pin 14 or 15 on a right socket or to pin 15 on the left socket.
b - Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c - Insert load resistor after pressing START; remove immediately after performing test.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.

Table 5-6. 28/28-Pin PLCC Programmable Array Logic Adapter (Non-JEDEC) Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 14 or 15 [a])
12	25	Static programming Levels	Right socket					Note [b,c]
		VCCP	28 pin/pin 1 and 28	5.75	6.00	6.25		Voltages are for fuse 37.
		CE Gen VIHH	28 pin/pin 16	12.00	12.50	13.00		Family PO code = 2659.
	26	Static programming Levels	Left socket					
		VCCP	28 pin/pin 28	4.8	5.0	5.2		Voltages are for fuse 32.
		VIHH	28 pin/pin 1	11.5	11.75	12.0		Family PO code = 2277.
		VIHH	28 pin/pin 21	11.5	11.75	12.0		
13	27	Skip this test. Not used for calibration.						
14	28	Skip this test. Not used for calibration.						
15	29	Skip this test. Not used for calibration.						
16	30	Rise time adjustment (tr2)						Adjust R30 for TR as shown on
		CE switch	28 pin R/pin 3				R30 701-0147	timing diagram (this step number).
		BIT switch 1	28 pin R/pin 27					All 3 rise times should be visible on
		BIT switch 2	28 pin R/pin 22					all 3 pins. Verify all TR. See note [d].
17	31	Supply Linearity						Verify waveform per timing
		V_{CC} supply	28 pin/pin28, R and L					diagram (this step number).
		CE supply	28 pin/pin 16					Waveforms should be linear as
		BIT supply	28 pin/pin 23					shown. See note [d].
18	32	Relay testing	28 pin R/pin 1 or 28 (V_{CC})				Short V_{CC} and GND pins together	
			28 pin R/pin 14 or 15 (GND)					and hit START. If no error occurs, relay is okay.

a - Connect the ground of the DVM to ground pin 14 or 15 on the right socket or to pin 15 on the left socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels: refer to step 12.

Table 5-7. 20/28-Pin IFL PLCC Adapter Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10 or 14 [a])
1	1	All pins low	20 pin/all pins 28 pin/all pins	-0.4		0.8		CAUTION [b,f].
2	2	Self-test, sink drivers						See Table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm 20-pin LED on, 28-pin off For test 5-19, see note [c].
	4	Comparator reference	701-0006/TP18	1.45	1.5	1.55	R68 701-0006	CAUTION [d,e,f]
	5	V_{CC} supply	28 pin/pin 28	11.8	12.0	12.2	R109 701-0006	Load with 50Ω 5W resistor to ground. [d,e]
	6	CE supply	28 pin/pin 20	19.6	19.8	20.0	R78 701-0006	Load with 100Ω 5W resistor to ground. [d,e]
	7	Bit supply SW 1	28 pin/pin 12	19.6	19.8	20.0	R77 701-0006	Load with 100Ω 5W resistor to ground. [d,e]
	8	Bit supply SW 2	28 pin/pin 15	19.5		20.1		Load with 100Ω 5W resistor to ground. [d,e]
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See table 5-12 if error results Possible errors are E0-FF.
	11	LED test 2						Confirm that 28 pin LED socket is on and 20 pin LED is off.
	12	Socket pins TTL high	28 pin/pins 1,2,7,9, 12,16,18,20,21,23,26	3.0		5.2		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	3.0		5.2		
	13	Socket pins TTL low	28 pin/pins 3,4,6,8, 10,13,15,17,22,24,27	-0.4		0.8		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	-0.4		0.8		
5	14	Socket pins TTL low	28 pin/pins 1,2,7,9, 12,16,18,20,21,23,26	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
			20 pin/pins 2,4,6,8, 12,14,16,17,19	-0.4		0.8		
	15	Socket pin source	28 pin/pins 3,4,6,8, 10,13,15,17,22,24,27	3.0		5.2		
			20 pin/pins 1,3,5,7,9, 11,13,15,18	3.0		5.2		

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.
f - Remove PLCC socket cover to ease measuring.

Table 5-7. 20/28-Pin IFL PLCC Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10 or 14 [a])
6	16	Socket pins source	28 pin/pins 2,7,9,12, 16,18,20,21,23,26	9.5		10.5		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	9.5		10.5		
	17	Socket pins TTL high	28 pin/pins 1,3,4,6, 8,10,13,15,17,22,24,27	3.0		5.2		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	3.0		5.2		
7	18	Socket pins TTL high	28 pin/pins 1,2,7,9, 12,16,18,20,21,23,26	3.0		5.2		
			20 pin/pins 2,4,6,8, 12,14,16,17,19	3.0		5.2		
	19	Socket pins source	28 pin/pins 3,4,6,8, 10,13,15,17,22,24,27	9.5		10.5		
			20 pin/pins 1,3,5,7, 9,11,13,15,18	9.5		10.5		
8	20	Backward device list	28 pin/pin 28 20 pin/pin 20					CAUTION [b,c] Load with 10Ω 5W to ground, confirm error 32.
9	21	Overcurrent test Low range Vcc	28 pin/pin 28 20 pin/pin 20	9.9 9.9	10V 10V	10.1 10.1	R108 701-0006 R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed. Adjustments are interactive. Adjust until error 31 is displayed without further adjustment.
		CE switch	28 pin/pin 20				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	28 pin/pin 12				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	28 pin/pin 15				N/A	Load with 12Ω 5W to ground, confirm error 31. CAUTION [c]
10	22	Overcurrent test High range Vcc	28 pin/pin 28 20 pin/pin 20	9.9 9.9	10.0 10.0	10.1 10.1	N/A N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	23	High range Vcc	28 pin/pin 28 20 pin/pin 20				N/A N/A	Load with 5Ω 5W to ground, confirm error 31.
11	24	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c - Insert load resistor after pressing START; remove immediately after performing test.

Table 5-7. 20/28-Pin IFL PLCC Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground to pin 10 or 14 [a])
12	25	Static programming Levels						Note [b,c]
		VCCP	28 pin/pin 28	8.4	8.5	8.6		Voltages are for fuse 32.
		BIT Gen VIHH	28 pin/pin 1	17.4	17.5	17.6		Family PO code = 9674.
	26	Static programming Levels						
		VCCP	20 pin/pin 20	8.4		8.6		Voltages are for fuse 32.
		VIHH	20 pin/pin 18	14.55		15.05		Family PO code = 9666.
13	27	Skip this test. Not used for calibration.						
14	28	Skip this test. Not used for calibration.						
15	29	Skip this test. Not used for calibration.						
16	30	Rise time adjustment (tr2)						Adjust R30 for TR as shown on
		CE switch	28 pin/pin 26				R30 701-0147	timing diagram (this step number)
		BIT switch 1	28 pin/pin 18					all 3 rise times should be visible on
		BIT switch 2	28 pin/pin 9					3 pins. Verify all TR. See note [d].
17	31	Supply Linearity						Verify waveform per timing
		V_{CC} supply	28 pin/pin 28					diagram (this step number).
		CE supply	28 pin/pin 20					Waveforms should be linear
		BIT supply	28 pin/pin 12					as shown. See note [d].
18	32	Relay testing	20 pin/pin 20 (V_{CC})					Short V_{CC} and GND pins together
			20 pin/pin 10 (GND)					and hit START. If no error occurs, relay is okay.

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Table 5-8. 28-Pin IFL PLCC Adapter Calibration Chart

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 14 [a])
1	1	All pins low	28 pin/all pins	-0.4		0.8		CAUTION [b,f]
2	2	Self-test, sink drivers						See Table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	LED test 1						Confirm 28-pin LED on. For test 5-19, see note [c].
	4	Comparator reference	701-0006/TP18	1.45	1.5	1.55	R68 701-0006	CAUTION [d,e,f]
	5	V_{CC} supply	28 pin/pin 28	11.8	12.0	12.2	R109 701-0006	Load with 50Ω 5W resistor to ground. [d,e]
	6	CE supply	28 pin/pin 5	19.6	19.8	20.0	R78 701-0006	Load with 100Ω 5W resistor to ground. [d,e]
	7	Bit supply SW 1	28 pin/pin 18	19.6	19.8	20.0	R77 701-0006	Load with 100Ω 5W resistor to ground. [d,e]
	8	Bit supply SW 2	28 pin/pin 19	19.5		20.1		Load with 100Ω 5W resistor to ground. [d,e]
	9	DAC reference	701-0006/TP10	4.8		5.2		
4	10	Self-test source drivers						See table 5-12 if error results. Possible errors are E0-FF.
	11	Socket pins TTL high	28 pin/pins 1,3,5,7,9, 11,13,16,18,21,23,25,27	3.0		5.2		
	12	Socket pins TTL low	28 pin/pins 2,4,6,8,10, 12,14,15,17,19,20,22, 24,26	-0.4		0.8		
5	13	Socket pins TTL low	28 pin/pins 1,3,5,7,9, 11,13,14,16,18,21,23, 25,27	-0.4		0.8		If error 76 occurs during steps 5 thru 16, perform steps 2 and/or 4 for diagnostics.
	14	Socket pin source	28 pin/pins 2,4,6,8,10, 12,15,17,19,20,22,24,26	3.0		5.2		

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - Do not leave programmer unattended in calibration mode beyond step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Insert load resistor after pressing START; remove immediately after performing test.
e - During adjustment only, measured value must be within + 0.05 Volts of nominal.
f - Remove PLCC socket cover to ease measuring.

Table 5-8. 28-Pin IFL PLCC Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 14 [a])
6	15	Socket pins source	28 pin/pins 3,5,7,9, 11,13,16,18,21,23,25,27	9.5		10.5		
	16	Socket pins TTL high	28 pin/pins 2,4,6,8,10 12,15,17,19,20,22,24,26	3.0		5.2		
7	17	Socket pins TTL high	28 pin/pins 1,3,5,7,9, 11,13,16,18,21,23,25,27	3.0		5.2		
	18		28 pin/pins 2,4,6,8,10, 12,15,17,19,20,22,24,26	9.5		10.5		
8	19	Backward device list	28 pin/pin 28					CAUTION [b,c] Load with 10Ω 5W to ground, confirm error 32.
9	20	Overcurrent test Low range V_{CC}	28 pin/pin 28	9.9	10V	10.1	R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 displayed.
		CE switch	28 pin/pin 5				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 1	28 pin/pin 18				N/A	Load with 12Ω 5W to ground, confirm error 31.
		Bit switch 2	28 pin/pin 19				N/A	Load with 12Ω 5W to ground, confirm error 31. CAUTION [c]
10	21	Overcurrent test High range V_{CC}	28 pin/pin 28	9.9	10.0	10.1	N/A	Load first with 100Ω 1W then with 12Ω 10W resistor to ground, confirm no errors. CAUTION [c]
	22	High range V_{CC}	28 pin/pin 28				N/A	Load with 5Ω 5W to ground, confirm error 31.
11	23	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - Cannot increment beyond this step; must enter calibration at an advanced step. (See Table 4-2)
c - Insert load resistor after pressing START; remove immediately after performing test.

Table 5-8. 28-Pin IFL PLCC Adapter Calibration Chart (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment Location	Comments (Ground pin 14 [a])
12	24	Static programming Levels						Note [b,c]
		VCCP	28 pin/pin 28	8.4	8.5	8.6		Voltages are for fuse 32.
		BIT Gen VIHH	28 pin/pin 1	17.4	17.5	17.6		Family PO code = 9663.
13	25	Skip this test. Not used for calibration.						
14	26	Skip this test. Not used for calibration.						
15	27	Skip this test. Not used for calibration.						
16	28	Rise time adjustment (tr2)						Adjust R30 for TR as shown on
		CE switch	28 pin/pin 8				R30 701-0147	timing diagram (this step number)
		BIT switch 1	28 pin/pin 17					all 3 rise times should be visible on
		BIT switch 2	28 pin/pin 9					all 3 pins. Verify all TR. See note [d].
17	29	Supply Linearity						Verify waveform per timing
		V_{CC} supply	28 pin/pin 28					diagram (this step number).
		CE supply	28 pin/pin 5					Waveforms should be linear as
		BIT supply	28 pin/pin 18					shown. See note [d].
18	30	Relay testing	28 pin/pin 28 (V_{CC}) 28 pin/pin 14 (GND)					Short V_{CC} and GND pins together and hit START. If no error occurs, relay is okay.

a - Connect the ground of the DVM to ground pin 10 on a 20-pin socket or to pin 14 on a 28-pin socket.
b - A family pin code must be entered or error 30 will be flagged. See timing diagrams for valid code.
c - A fuse number must be entered or default to fuse 0 will occur.
d - An oscilloscope trigger signal is available at TP16 on 701-0006.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Table 5-9. Measurement Chart for the Model 60H 20-pin Performance Board

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment. Location	Comments (Ground = pin 10 [a]) (All measurements in volts.)
1	1	All pins low	PAL/all pins	-0.4		0.8		CAUTION [b]
2	2	Self-test, sink drivers						See table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	Comparator reference	701-0006/TP18	1.45	1.50	1.55	R68 701-0006	
	4	Vcc supply	PAL/pin20 IFL/pin 20	11.80	12.00	12.20	R109 701-0006	No load resistors required for test 4-17. For tests 4-17, see note [c].
	5	CE Supply	PAL/pin 11 IFL/pin 2	19.80	20.00	20.20	R78 701-0006	
	6	Bit Supply SW1	PAL/pin19 IFL/pin 16	19.80	20.00	20.20	R77 701-0006	
	7	Bit supply SW2	PAL/pin 14 IFL/pin11	19.70	20.00	20.30		
	8	DAC reference	701-0006/TP10	4.8		5.2		
4	9	Self-test, source drivers						See table 5-12 if errors result. Possible errors are E0-FF.
	10	Socket pins TTL high	PAL/pins 2,4,6,8, 11,13,15,17,19 IFL/pins 2,4,6,8, 12,14,16,17,19	3.0		5.2		
	11	Socket pins TTL low	PAL/pins 1,3,5,7, 9,12,14,16,18 IFL/pins 1,3,5,7, 9,11,13,15,18	-0.4		0.8		
5	12	Socket pins TTL low	PAL/pins 2,4,6,8, 11,13,15,17,19 IFL/pins 2,4,6,8, 12,14,16,17,19	-0.4		0.8		If error 76 occurs during steps 5-15, perform steps 2 and/or 4 for diagnostics.
	13	Socket pins TTL high	PAL/pins 1,3,5,7, 9,12,14,16,18 IFL/pins 1,3,5,7, 9,11,13,15,18	3.0		5.2		
6	14	Socket pins source	PAL/pins 2,4,6,8, 11,13,15,17,19 IFL/pins 2,4,6,8, 12,14,16,17,19	9.5	10.5			
	15	Socket pins TTL high	PAL/pins 1,3,5,7, 9,12,14,16,18 IFL/pins 1,3,5,7, 9,11,13,15,18	3.0		5.2		

a - Connect the ground of the DVM to pin 10 of the contactor connector.
b - Do not leave the programmer unattended in calibration mode beyond step 1. Do not power down after step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.

Table 5-9. Measurement Chart for the Model 60H 20-pin Performance Board (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adustment. Location	Comments (Ground = pin 10 [a]) (All measurements in volts.)
7	16	Socket pins TTL high	PAL/pins 2,4,6,8, 11,13,15,17,19	3.0		5.2		
			IFL/pins 2,4,6,8, 12,14,16,17,19					
	17	Socket pins source	PAL/pins 1,3,5,7, 9,12,14,16,18	9.5		10.5		
			IFL/pins 1,3,5,7, 9,11,13,15,18					
8	18	Backward device test	PAL/pin 20 IFl/pin 20					CAUTION [b,c] Load with 10Ω 5W to ground, confirm error 32.
9	19	Overcurrent test Low Range V_{CC}	PAL/pin 20 IFL/pin 20	9.9	10.0	10.1	R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 is displayed.
		CE switch	PAL/pin 11 IFL/pin 2				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 1	PAL/pin19 IFL/pin 16				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 2	PAL/pin 14 IFL/pin 11				N/A	Load with 12Ω 5W to ground, confirm error 31.
10	20	Overcurrent test High Range V_{CC}	PAL/pin 20 IFL/pin 20	9.9	10.0	10.1	N/A	Load first with 100Ω 1W then with 12Ω 10W to ground, confirm no errors. CAUTION [c]
	21	V_{CC}	PAL/pin 20 IFL/pin 20				N/A	Load with 5Ω 5W to ground, confirm error 31.
11	22	Skip this test. Not used for calibration.						
12	23	Static programming levels PAL VCCP VHH VOP	PAL/ pin 20 pin 1 pin 19	 5.1 10.75 19.75		 5.3 11.25 20.25		Family/pinout code 9717 [d]. Enter fuse number 0000.
		Static programming levels IFL VCCP VIHH	IFL/ pin 20 pin 18	 8.4 14.55		 8.6 15.05		Family/pinout code 9666 [d]. Enter fuse number 0000.

a - Connect the ground of the DVM to pin 10 of the contactor connector.
b - Cannot increment beyond this step; must enter calibration at an advanced step.
c - Insert load resistor after pressing START; remove immediately after performing test.
d - A family pinout code must be entered or error 30 will be flagged.

Table 5-9. Measurement Chart for the Model 60H 20-pin Performance Board (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adustment. Location	Comments (Ground = pin 10 [a]) (All measurements in volts.)
13	24	Skip this test. Not used for calibration.						
14	25	Skip this test. Not used for calibration.						
15	26	Skip this test. Not used for calibration.						
16	27	Rise time adjust (tr2)						
		CE switch	PAL/pin 2 IFL/pin 14				R30 701-0147	Adjust R30 for TR as shown on timing diagram (this step number). All three rise times should be visible on all three pins. Verify all rise times. See note [b,c].
		BIT switch 1	PAL/pin 19 IFL/pin 16					
		BIT switch 2	PAL/pin 14 IFL/pin 11					
17	28	Supply linearity						
		V_{CC} supply	PAL/pin 20 IFL/pin 20					Verify waveforms per timing diagram (this step number). Waveforms should be linear as shown. See note [b,c].
		CE supply	PAL/pin 11 IFL/pin 2					
		BIT supply	PAL/pin19 IFL/pin16					

a - Connect the ground of the oscilloscope or DVM to pin 10 of the contactor connector.
b - An oscilloscope trigger signal is available at TP16 on 701-0006.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.

Table 5-10. Measurement Chart for the Model 60H 24-pin Performance Board

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adjustment. Location	Comments (Ground = pin 12 [a]) (All measurements in volts.)
1	1	All pins low	PAL/all pins IFL/all pins	-0.4		0.8		CAUTION [b]
2	2	Self-test, sink drivers						See table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	Comparator reference	701-0006/TP18	1.45	1.50	1.55	R68 701-0006	
	4	V_{CC} supply	PAL/pin 24 IFL/pin 24	11.80	12.00	12.20	R109 701-0006	No load resistors required for tests 4-17. For tests 4-17, see note [c].
	5	CE supply	PAL/pin 13 IFL/pin 17	19.80	20.00	20.20	R78 701-0006	
	6	Bit supply SW1	PAL/pin 19 IFL/pin 10	19.80	20.00	20.20	R77 701-0006	
	7	Bit supply SW2	PAL/pin 14 IFL/pin 13	19.70		20.30		
	8	DAC reference	701-0006/TP10	4.8		5.2		
4	9	Self-test, source drivers						See table 5-12 if errors result. Possible errors are E0-FF.
	10	Socket pins TTL high	PAL/pin 2,4,6,8,10, 13,16,18,19,21,23 IFL/pins 1,2,6,8,10, 14,16,17,18,20,22	3.0		5.2		
	11	Socket pins TTL low	PAL/pins 1,3,5,7,9, 11,14,15,17,20,22 IFL/pins 3,4,5,7,9, 11,13,15,19,21,23	-0.4		0.8		
5	12	Socket pins TTL low	PAL/pins 2,4,6,8,10, 13,16,18,19,21,23 IFL/pins 1,2,6,8,10,. 14,16,17,18,20,22	-0.4		0.8		IF error 76 occurs during steps 5-15, perform steps 2 and/or 4 for diagnostics
	13	Socket pins TTL high	PAL/pins 1,3,5,7,9, 11,14,15,17,20,22 IFL/pins 3,4,5,7,9, 11,13,15,19,21,23	3.0		5.2		
6	14	Socket pins source	PAL/pins 2,4,6,8,10, 13,16,18,19,21,23 IFL/pins 2,6,8,10,14 16,17,18,20,22	9.5		10.5		
	15	Socket pins TTL high	PAL/pins 1,3,5,7,9, 11,15,17,20,22 IFL/pins 1,3,4,5,7,9, 11,13,15,19,21,23	3.0		5.2		

a - Connect the ground of the DVM to pin 12 of the contactor connector.
b - Do not leave the programmer unattended in calibration mode beyond step 1. Do not power down after step 1.
c - Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.

Table 5-10. Measurement Chart for the Model 60H 24-pin Performance Board (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adustment. Location	Comments (Ground = pin 12 [a]) (All measurements in volts.)
7	16	Socket pins TTL high	PAL/pins 2,4,6,8,10, 13,16,18,19,21,23	3.0		5.2		
			IFL/pins 1,2,6,8,10, 14,16,17,18,20,22					
	17	Socket pins source	PAL/pins 1,3,5,7,9, 11,14,15,17,20,22	9.5		10.5		
			IFL/pins 3,4,5,7,9, 11,13,15,19,21,23					
8	18	Backward device test	PAL/pin 24 IFL/pin24					CAUTION [b,c]. Load with 10Ω 5W to ground, confirm error 32.
9	19	Overcurrent test Low Range V_{CC}	PAL/pin 24 IFL/pin 24	9.9	10.0	10.1	R108 701-0006	Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 is displayed.
		CE switch	PAL/pin 13 IFL/pin 17				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 1	PAL/pin 19 IFL/pin 10				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 2	PAL/pin 14 IFL/pin 13				N/A	Load with 12Ω 5W to ground, confirm error 31
10	20	Overcurrent test High Range V_{CC}	PAL/pin 24 IFL/pin 24	9.9	10.0	10.1	N/A	Load first with 100Ω 1W then with 12Ω 10W to ground confirm no errors. CAUTION [c]
	21	V_{CC}	PAL/pin 24 IFL/pin 24				N/A	Load with 5Ω 5W to ground, confirm error 31.
11	22	Skip this test. Not used for calibration.						
12	23	Static programming levels						
		PAL	PAL/					Family/pinout code 9728 [d].
		VCCP	pin 24	5.1		5.3		Enter fuse number 0000.
		VHH	pin 1	10.5		11.5		
		VOP	pin 22	14.5		15.5		
		IFL	IFL/					Family/pinout code 9669 [d].
		VCCP	pin 24	4.9		5.1		Enter fuse number 0000.
		VIX	pin 23	9.75		10.25		
		VOPF	pin 1	17.25		17.75		
13	24	Skip this test. Not used for calibration.						
14	25	Skip this test. Not used for calibration.						

a - Connect the ground of the DVM to pin 12 of the contactor connector.
b - Cannot increment beyond this step; must enter calibration at an advanced step.
c - Insert load resistor after pressing START; remove immediately after performing test.
d - A family pinout code must be entered or error 30 will be flagged.

Table 5-10. Measurement Chart for the Model 60H 24-pin Performance Board (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adustment. Location	Comments (Ground = pin 12 [a]) (All measurements in volts.)
15	26	Skip this test. Not used for calibration.						
16	27	Rise time adjust (tr2) CE switch BIT switch 1 BIT switch 2	 PAL/pin 2 IFL/pin 22 PAL/pin 23 IFL/pin 16 PAL/pin 18 IFL/pin 8				 R30 701-0147	Adjust R30 for TR as shown on timing diagram (this step number). All three rise times should be visible on all three pins. Verify all TR. See note [b,c].
17	28	Supply linearity V_{CC} supply CE supply BIT supply	 PAL/pin 24 IFL/pin 24 PAL/pin 13 IFL/pin 17 PAL/pin 19 IFL/pin 10					Verify waveforms per timing diagram (this step number). Waveforms should be linear as shown. See note [b,c].

a - Connect the ground of the oscilloscope or DVM to pin 12 of the contactor connector.
b - An oscilloscope trigger signal is available at TP16 on 701-0006.
c - Voltage levels are for calibration purposes only and are not specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.

Table 5-11. Measurement Chart for the Model 60H 28-pin Performance Board

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Measurement Nom.	Measurement Max.	Adjustment. Location	Comments (Ground = pin 14 [a]) (All measurements in volts.)
1	1	All pins low	All pins	-0.4		0.8		CAUTION [b]
2	2	Self-test, sink drivers						See table 5-12 if errors result; errors must be corrected to continue. Possible errors are A0-DF.
3	3	Comparator reference	701-0006/TP18	1.45	1.50	1.55	R68 701-0006	
	4	V_{CC} supply	pin 28	11.80	12.00	12.20	R109 701-0006	No load resistors required for tests 4 through 17. For tests 4 through 17, see note [c].
	5	CE supply	pin 5	19.80	20.00	20.20	R78 701-0006	
	6	Bit supply SW1	pin 13	19.80	20.00	20.20	R77 701-0006	
	7	Bit supply SW2	pin 19	19.70		20.30		
	8	DAC reference	701-0006/TP10	4.8		5.2		
4	9	Self-test, source drivers						See table 5-12 if errors result. Possible errors are E0-FF.
	10	Socket pins TTL high	pins 1,3,5,7,9,11, 13,16,18,21,23,25,27	3.0		5.2		
	11	Socket pins TTL low	pins 2,4,6,8,10,12, 15,17,19,20,22,24,26	-0.4		0.8		
5	12	Socket pins TTL low	pins 1,3,5,7,9,11, 13,16,18,21,23,25,27	-0.4		0.8		IF error 76 occurs during steps 5-15, perform steps 2
	13	Socket pins TTL high	pins 2,4,6,8,10,12, 15,17,19,20,22,24,26	3.0		5.2		
6	14	Socket pins source	pins 3,5,7,9,11, 13,16,18,23,25,27	9.5		10.5		
	15	Socket pins TTL high	pins 1,2,4,6,8,10,12, 15,17,19,20,22,24,26	3.0		5.2		
7	16	Socket pins TTL high	pins 3,5,7,11,13, 16,18,21,23,25,27	3.0		5.2		
	17	Socket pins source	pins 2,4,6,8,10,12, 15,17,19,20,22,24,26	9.5		10.5		
8	18	Backward device test	pin 28					CAUTION [d,e]. Load with 10Ω 5W to ground, confirm error 32.
9	19	Overcurrent test Low Range V_{CC}	pin 28	9.9	10.0	10.1	R108 701-0006	CAUTION [e] Load with 100Ω 1W resistor to ground. Adjust pot clockwise just until error 31 is displayed.
		CE switch	pin 5				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 1	pin 13				N/A	Load with 12Ω 5W to ground, confirm error 31.
		BIT switch 2	pin 1				N/A	Load with 12Ω 5W to ground, confirm error 31.

a - Connect the ground of the DVM to pin 14 of the contactor connector.
b - Do not leave the programmer unattended in calibration mode beyond step 1. Do not power down after 1.
c - Voltage levels are for calibration purpose only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
d - Cannot increment beyond this step;must enter calibration at an advanced step.
e - Insert load resistor after pressing START; remove immediately after performing test.

Table 5-11. Measurement Chart for the Model 60H 28-pin Performance Board (cont.)

Step	Test No.	Test Description	Measurement Location (Socket/pins or circuit board test points)	Measurement Min.	Nom.	Max.	Adustment. Location	Comments (Ground = pin 14 [a]) (All measurements in volts.)
10	20	Overcurrent test High Range V_{CC}	pin 28	9.9	10.0	10.1	N/A	CAUTION [b] Load first with 100Ω 1W then with 12Ω 10W to ground confirm no errors.
	21	V_{CC}	pin 28				N/A	Load with 5Ω 5W to ground. Confirm error 31.
11	22	Skip this test. Not used for calibration.						
12	23	Static programming levels Fuse 0 (AND array)						Family/pinout code 9661 [c]. Enter fuse 0 [d].
		VCCP	pin 28	4.75		5.25		
		VIX	pins 19,20	9.5		10.5		
		VFEH	pin 1	17.0	18.0			
		Fuse 32 (OR array)						Enter fuse 32 [d].
		VCCS	pin 28	8.25		8.75		
		VFEH	pin 1	17.0		18.0		
		VIX, VOPF	pins 18,19	9.5		10.5		
		Fuse 1920 (output polarity)						Enter fuse 1920 [d].
		VCCL	pin 28	0.0		0.8		
		VOPH	pin 18	17.0		18.0		
13	24	Skip this test. Not used for calibration.						
14	25	Skip this test. Not used for calibration.						
15	26	Skip this test. Not used for calibration.						
16	27	Rise time adjust (tr2)						
		CE switch	pin 27				R30 701-0147	Adjust R30 for TR as shown on timing diagram (this step number). All three rise times should be visible on all three pins. Verify all TR. See note [e,f].
		BIT switch 1	pin 18					
		BIT switch 2	pin 9					
17	28	Supply linearity						
		V_{CC} supply	pin 28					Verify waveforms per timing diagram (this step number). Waveforms should be linear as shown. See note [e,f].
		CE supply	pin 5					
		BIT supply	pin 19					

a - Connect the ground of the DVM to pin 14 of the contactor connector.
b - Insert load resistor after pressing START; remove immediately after performing test.
c - A family pinout code must be entered or error 30 will be flagged.
d - A fuse number must be entered or default to fuse 0 will occur.
e - An oscilloscope trigger signal is available at TP16 on 701-0006.
f - Voltage levels are for calibration purpose only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.

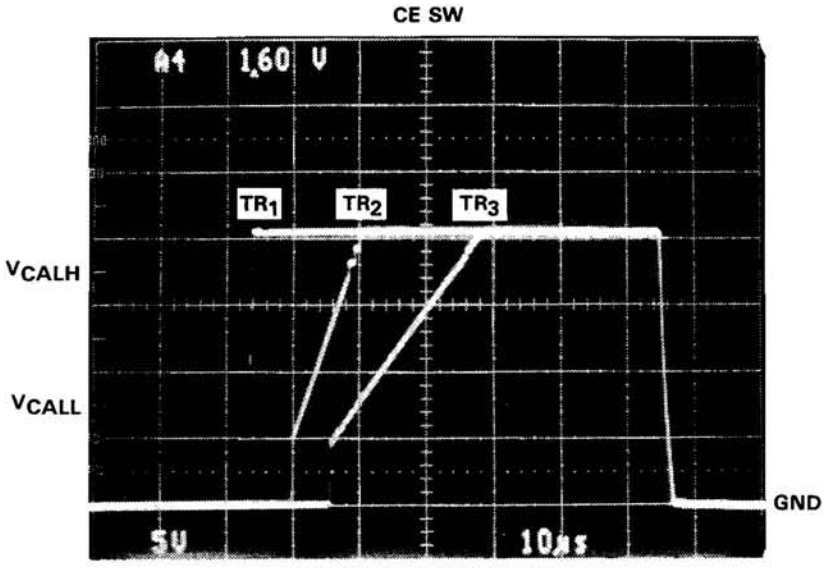
Table 5-12. Calibration Error Codes

Error	I/O Line Pin No.	J302*	Condition	Error	I/O Line Pin No.	J302*	Condition
A0	1	5	Failure to	D0	17	7	Failure to
A1	2	8	read desired	D1	18	10	read desired
A2	3	11	level on input	D2	19	13	TTL level on
A3	4	14	register	D3	20	16	output pin
A4	5	3		D4	21	19	
A5	6	2		D5	22	22	
A6	7	17		D6	23	25	
A7	8	20		D7	24	28	
A8	9	23		D8	25	31	
A9	10	26		D9	26	34	
AA	11	29		DA	27	37	
AB	12	32		DB	28	40	
AC	13	35		DC	29	43	
AD	14	38		DD	30	46	
AE	15	1		DE	31	47	
AF	16	4		DF	32	48	
B0	17	7	Failure to	E0	1	5	Failure to
B1	18	10	read desired	E1	2	8	read desired
B2	19	13	level on input	E2	3	11	10V level on
B3	20	16	register	E3	4	14	desired
B4	21	19		E4	5	3	output pin
B5	22	22		E5	6	2	
B6	23	25		E6	7	17	
B7	24	28		E7	8	20	
B8	25	31		E8	9	23	
B9	26	34		E9	10	26	
BA	27	37		EA	11	29	
BB	28	40		EB	12	32	
BC	29	43		EC	13	35	
BD	30	46		ED	14	38	
BE	31	47		EE	15	1	
BF	32	48		EF	16	4	

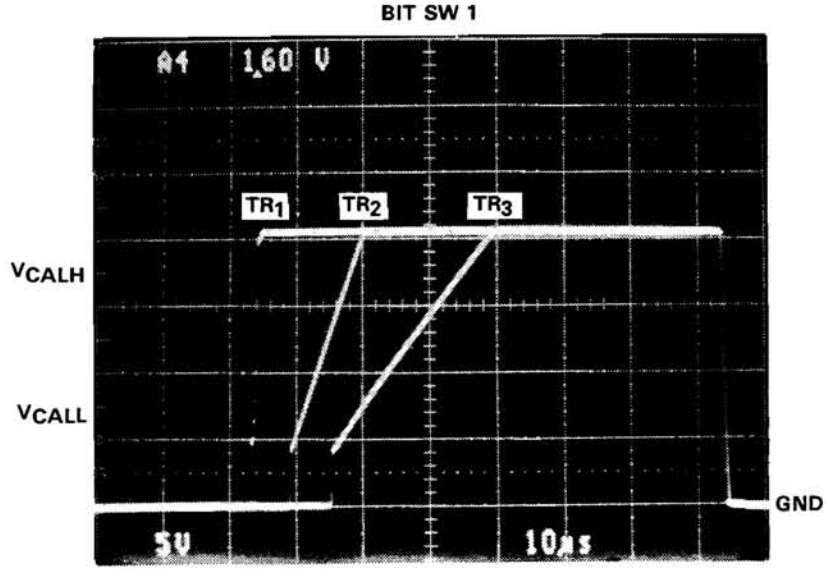
Table 5-12. Calibration Error Codes (cont.)

Error	I/O Line Pin No.	J302*	Condition	Error	I/O Line Pin No.	J302*	Condition
C0	1	5	Failure to read	F0	17	7	Failure to
C1	2	8	desired TTL	F1	18	10	read desired
C2	3	11	level on	F2	19	13	10V level on
C3	4	14	output pin	F3	20	16	desired
C4	5	3		F4	21	19	output pin
C5	6	2		F5	22	22	
C6	7	17		F6	23	25	
C7	8	20		F7	24	28	
C8	9	23		F8	25	31	
C9	10	26		F9	—	—	
CA	11	29		FA	27	37	
CB	12	32		FB	28	40	
CC	13	35		FC	—	—	
CD	14	38		FD	—	—	
CE	15	1		FE	—	—	
CF	16	4		FF	—	—	

*J302 is located on the waveform generator board.



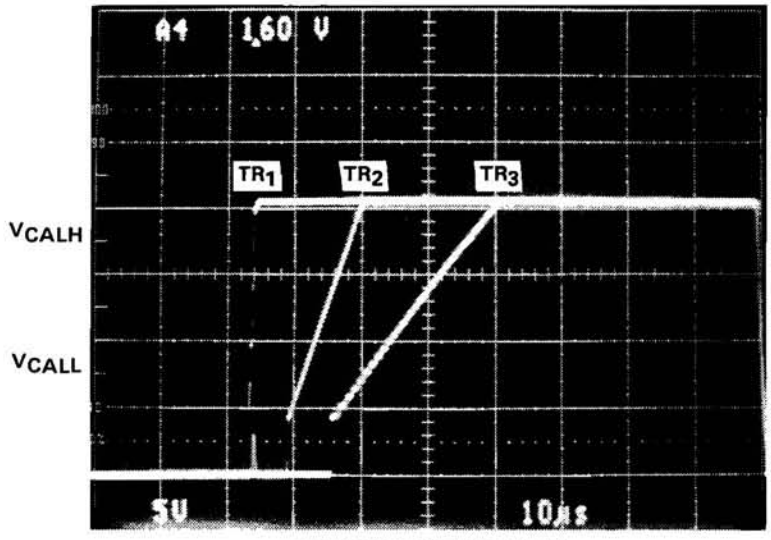
PIN 2 360A-001 ADAPTER
PIN 22 360A-002 ADAPTER



PIN 23 360A-001 ADAPTER
PIN 16 360A-002 ADAPTER

Figure 5-5. Waveform Diagrams

BIT SW 2



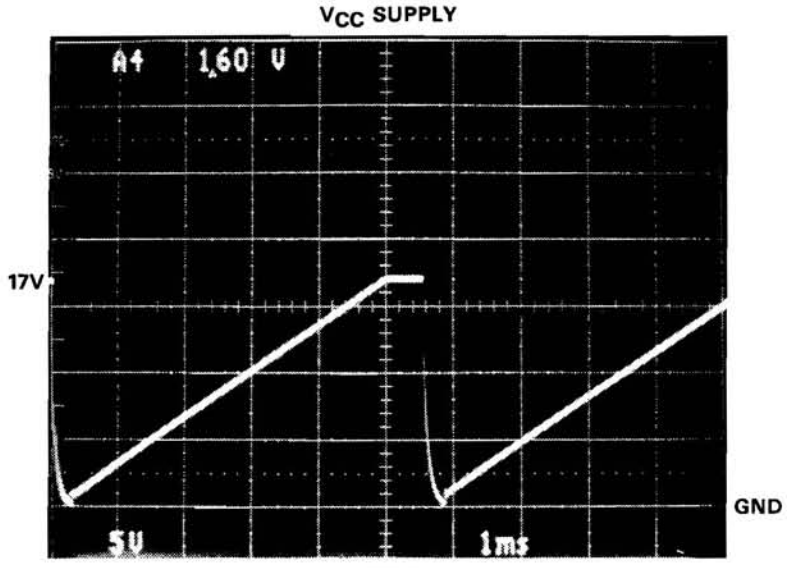
PIN 18 360A-001 ADAPTER
PIN 8 360A-002 ADAPTER

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CALH}	--	18.0	--	V	Adjust R30 on 701-0147 BRD for TR2 CE SW as shown. Verify others are within limits.
	V_{CALL}	--	8.0	--	V	
	T_{R1}	0.33	--	0.50	us	Rise times are measured from V_{CALL} to V_{CALH} on an imaginary line drawn through straight portion of rise time (voltage levels for reference only).
	T_{R2}	5.6	6.7	8.3	us	
	T_{R3}	11.4	--	17.1	us	

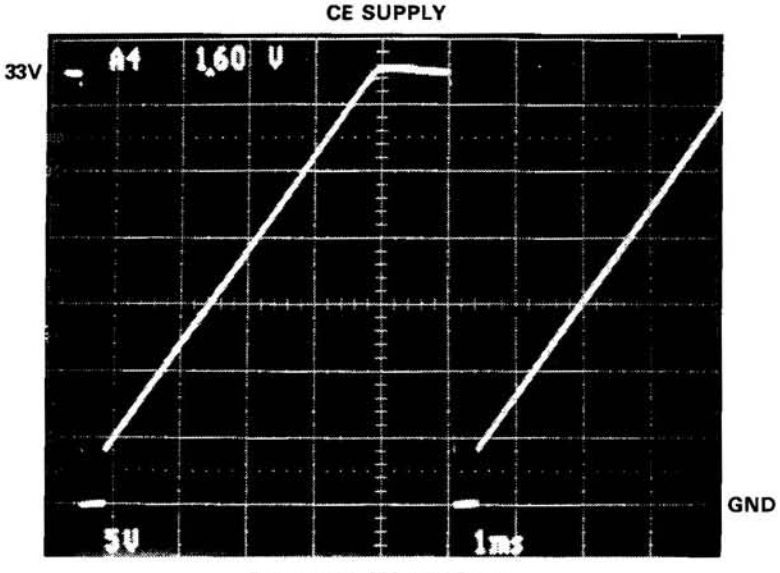
NOTES

1. *Scope trigger: TP16, 701-0006 board.*
2. *Cal step 16.*
3. *Test points are for the 24-pin socket.*

Figure 5-5. Waveform Diagrams (continued)



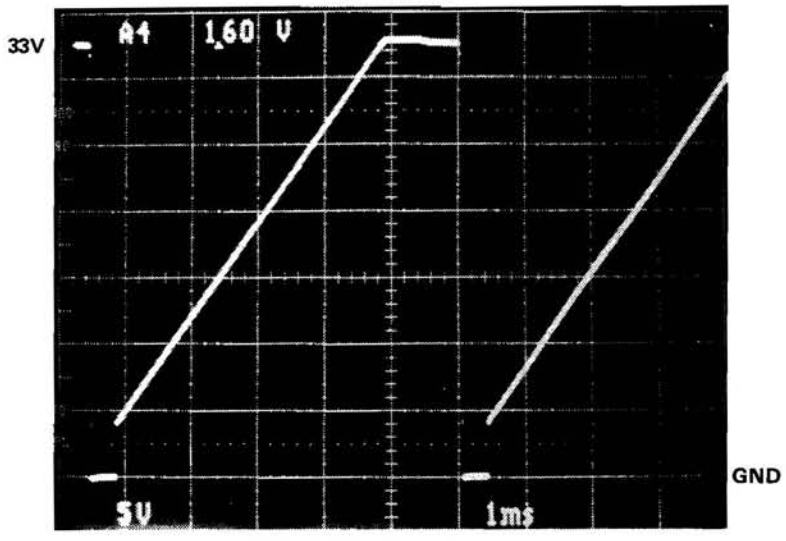
PIN 24



PIN 1 360A-001 ADAPTER
PIN 17 360A-002 ADAPTER

Figure 5-5. Waveform Diagrams (continued)

BIT SUPPLY



PIN 19 360A-001 ADAPTER
PIN 10 360A-002 ADAPTER

NOTES

1. *Scope trigger: TP16, 701-0006 board.*
2. *Cal step 17.*
3. *Test points are for the 24-pin socket.*

Figure 5-5. Waveform Diagrams (continued)

6. TROUBLESHOOTING

6.1 INTRODUCTION

The following troubleshooting information is intended to help you interpret and isolate failures and problems in the Model 60. It is recommended that you perform a complete calibration before consulting this section. If the problem still persists after calibration, use this section along with the circuit description information in section 3 and the schematics to isolate and resolve the problem.

In general, troubleshooting of the Model 60 proceeds in this manner:

1. Does the display light up when the programmer is switched on?
2. Does the programmer pass the self-test?
3. Is the keyboard functioning properly?
4. Are I/O operations functioning properly?
5. Does the programmer display an Error Code?
6. After checking the above systems, calibrate the programmer.
7. If the problem still persists, call your nearest Data I/O service center.

6.2 FAULT ISOLATION

The following subsections discuss the various parameters to check when troubleshooting your programmer to isolate the fault.

6.2.1 Programmer's Display Fails to Illuminate

If the programmer's display does not illuminate on power up:

1. Ensure that the power supply line fuse is intact (see section 2).
2. Be certain that the AC power value is correct by looking at the value showing through the rear panel door. If the value is incorrect, change it to the correct value (see section 2).
3. Ensure that all the interconnect cables are making complete contact with the receptacles.
4. Be certain that the fan is operating. If the fan is operating, then the fuse is not blown.
5. Ensure that the secondary fuse, located next to J10 on the Power Supply board, is intact and not blown.

6.2.2 Erratic Programmer Display or No Keyboard Response

If the programmer's display is erratic, this usually indicates a problem with the microprocessor, its associated circuitry or one of the memory circuits. If there is no response from keyboard commands, there may be a problem with the keyboard and/or the display circuitry. If your programmer has an erratic display or the keyboard is not responding:

1. Be certain that all the interconnect cables are making complete contact with the receptacles.

2. Verify that all PROMs are installed properly: Check for bent pins and be certain that the PROMs make complete contact with the sockets. The PROMs are located on the controller board directly beneath the socket adapter receptacle.

6.2.3 Programmer Displays an Error Code

Refer to Table 6-1 for the displayed error code and take any steps listed under the corrective action column. For steps that list only an operator type action call your local Data I/O service center if the operator type actions does not alleviate the problem.

6.2.4 Programmer Will Not Perform a Device-Related Operation Properly

If the programmer does not perform a load, program or verify operation correctly, check the following:

1. Check the device table in Appendix A to ensure that the family and pinout codes you have entered are correct for the device you are using.

2. Enter the calibration mode, verifying the voltages listed for steps 2 through 20.

3. Verify your programmer's waveforms against those in appendix D.

6.2.5 Programmer Will Not Perform a Port-Related Operation Properly

If your Model 60 does not perform port operations correctly, check the following:

1. Check that the correct baud rate, stop bit(s) and parity setting are in effect (see section 2).

2. Ensure that the RS232C interface is hooked up correctly (see section 2).

3. Be certain that the RS232C voltages are at the proper levels: check J205 on the controller board, pins 2, 4 and 20. They should vary from -9V to +12V during an output operation.

Table 6-1. System Error Codes

NOTE

If you get a recurring error, call your local customer support center .

Code	Name	Description	Corrective Action
16*	FUNCTION ABORT	Command in progress was aborted by operator.	None
17*	COMMAND ERROR	Illegal key sequence while in Computer Remote Control (CRC).	Check key sequence and re-enter.
20	NONBLANK	Device failed the blank test.	Press **START** to override this error and program the device.
21	ILLEGAL BIT	Not possible to program the device due to already programmed locations of incorrect polarity.	Erase the device if possible or discard it.
22	PROGRAM FAIL	The program electronics were unable to program the device.	Either the device is bad or the programmer is inoperative or out of calibration.
23	VERIFY FAIL 1	The device data was incorrect on the first pass of the automatic verify sequence during device programming.	This error indicates that the device failed the low voltage verify; the data in the part is not the same as the RAM data.
24	VERIFY FAIL 2	The device data was incorrect on the second pass of automatic verify sequence during programming.	This error indicates that the device failed the high voltage verify; data in the part is not the same as the RAM data.
26	WRONG SKT ADP	Operation was attempted with the wrong adapter installed.	Install the appropriate adapter. Check the ID register for faults. Check the appropriate registers on the waveform board.
27	RAM EXCEEDED	There is insufficient RAM. The total allotment of RAM resident is less than the word limit or block size, or the begin address is set too high.	Program smaller parts or specific lower beginning address. If enough RAM is installed, it may be faulty.

* Remote Control only; will not occur during front panel operation, hence no front panel display.

Table 6-1. System Error Codes (cont.)

Code	Name	Description	Corrective Action
30	FAM/PIN ERROR	An incorrect family and pinout code was entered from the front panel control or a valid pinout code was not appropriate for the operation attempted.	Check the User Note for correct family and pinout code.
31	EXCSS CURRENT	In the operation just attempted, the device was drawing more current than the device manufacturer's specification.	If the device is faulty, replace it. If this is not the problem, run calibration steps 1 thru 8 and 77 to determine the circuitry affected. manual.
32	BACKWARDS DEV	Backward device	Check for a backwards or faulty device. If adapters 360A-001 or 360A-002 are installed check the V_{CC} pulldown.
32	MISJUSTIFY ER	Device is not bottom-justified.	Check to be sure that the bottom-most pins of the device are at the bottom of the socket.
32	I/O LEVEL ERR	Hardware malfunction in EPROM adapter.	Check the Pulse Generator followed by calibration steps 1 thru 8, if required.
34	FAM/PIN ERROR	An incorrect family and pinout code was entered.	Check the User Note for correct family and pinout code.
38	BAD CAL STEP	An inappropriate calibration step was entered.	Recheck the calibration chart for the correct calibration step and try again. The calibration chart is in the maintenance manual.
39	SEC FUS BLOWN	An attempt was made to program a device with the security fuse blown.	Device cannot be programmed again if the security fuse is blown.
3A	NO FUNC DATA	A load or a test operation was attempted with test mode selected for structured vector and fingerprint test only, and no vectors are loaded and the number of fingerprint cycles are zero.	Select an alternate test mode or resolve the undefined vectors or cycle count.

Table 6-1. System Error Codes(cont.)

Code	Name	Description	Corrective Action
3D	LOGIC OPTION	Identifies a function that applies to logic operation. Occurs when a memory adapter is installed.	Choose a different function or change the adapter.
3E	MEMORY OPTION	Identifies a function that applies to memory operation. Occurs when a logic adapter is installed.	Choose a different function or change the adapter.
41	FRAME ERR	The serial interface detected a start bit but the stop bit was incorrectly positioned.	Check the baud rate and stop bit options (selects DA and DC) or use handshake.
42	OVERRUN ERR	The serial interface received characters when the programmer was unable to service them.	Check the baud rate and stop bit options or use hardware handshake. See the remote control section for instructions.
46	I/O TIMEOUT	No character (or only nulls and rubouts) were received on serial input for 25 seconds after pressing the START key, or no characters could be transmitted for a period of 25 seconds due to the state of the handshake lines.	Check all connections; then restart the operation, I/O timeout can be disabled by select code F9, which will then allow more than 25 seconds for serial port inputs.
48	I/O OVERRUN	The serial port input buffer received too many characters after the handshake line informed the sending device to stop.	Make sure the handshake lines are hooked up and operative.
52	I/O VFY FAIL	The data from the serial port did not match the data in RAM.	
63	RAM WRITE ERR	The programmer is unable to write the intended data in RAM.	Failure of the associated RAM chip; replace the failed chip.
64	RAM DATA ERR	The programmer detected a spurious change in RAM data.	Reload data into RAM. If problem persists, contact your local Data I/O Service Center.
66	IRQ ERR	The IRQ line to the processor was held low for no apparent reason.	Ignore. If the error persists, service the programmer.

Table 6-1. System Error Codes (cont.)

Code	Name	Description	Corrective Action
67*	ERROR	Programmer received a non-valid command in Computer Remote Control (CRC).	Re-enter the command.
69	RAM BANK ERR	RAM bank error.	The address size is out of range for the programming adapter installed; reduce the block size to 4000.
74	FNGRPRNT FAIL	Logic Fingerprint test verify error.	Indicates one of the following Logic Fingerprint errors: 1. Device passed fuse verify but failed Logic Fingerprint defective device 2. Operator has entered wrong Fingerprint vectors 3. Device cannot be tested with Logic Fingerprint (refer to the device-support list in the User Note)
75	VECTOR FAIL	Structured test verify error	The device passed fuse verify but failed structured test-defective device. Check structured test vectors and make sure they are correct. If not, re-enter the correct vectors. The vector could be invalid, or the operator may have mis-keyed a valid vector.
76	SELF TEST ERROR	Hardware failure on one of the device pin drivers.	Perform calibration steps 1 through 8, and 77 to isolate the error. Contact your local Data I/O Service Center, if required.
77	SECURITY FAIL	Security fuse programming error.	The security fuse for the given device failed to program.
79	PRELOAD ERR	Preload implementation error.	The preload algorithm is not implemented for this device or it is implemented incorrectly.
81	PARITY ERR	The incoming data has incorrect parity.	Check the parity option (select BD and try again.

* Remote Control only; will not occur during front panel operation, hence no front panel display.

Table 6-1. System Error Codes (cont.)

Code	Name	Description	Corrective Action
82	SUMCHK ERR	The sumcheck field received by the programmer does not agree with its own calculated sumcheck. For ASCII Binary formats, this error message indicates a missing F character.	Check all connections of units in the system, data format, and data source, and then try again.
83*	OUT OF RANGE	Value out of range for correct operation in CRC.	Enter legal parameters.
84**	INVALID DATA	The programmer received invalid or not enough data characters during format reception. JEDEC Field: F - Invalid character in the field. Only "1" and "0" are allowed. L - A space or carriage return did not follow the fuse number. L - An invalid character was in the fuse state field. Only "1" and "0" are allowed. Spaces, line feeds, and carriage returns are ignored. S - Invalid character in the field. Only "1", "0" and "N" are allowed. V - Too few or too many test conditions.	Check the connection of all units in the system, data format and data source, and then try again.
90	INVALID FORM	1) An I/O operation was attempted while in the logic mode with a non-JEDEC I/O translator. 2) An I/O operation was attempted while in the memory mode with the JEDEC translator selected.	Enter a legal format code for the adapter that is installed.

* Remote Control only; will not occur during front panel operation, hence no front panel display.

** Logic Device operations only.

Table 6-1. System Error Codes (cont.)

Code	Name	Description	Corrective Action
91**	I/O FORM ERR	The programmer received an invalid character in the address field. JEDEC Field: C - Invalid character in field, must be four digit hexadecimal number. G - Invalid character in field. Only "1" and "0" allowed. L - fuse number exceeds fuse limit for device or invalid fuse number (must be decimal). P - Too few or too many pins or invalid pin number for device. T - Test cycles greater than 99. R - Invalid character in the field; must be eight digit hexadecimal number.	Check the connection of all units in the system, data format, and data source, and then try again.
92	I/O FORM ERR	The address check was in error Tektronix Hexadecimal format only).	Check the connection of units in the system, data format, and data source, and then try again.
93	I/O FORM ERR	The number of input records did not equal the Record Count	Check the connection of all units in the system, data format, and data source, and then try again.
94	BAD REC TYPE	The record type was in error. (Intel-Intellec 8/MDS, Intel MCS-86) formats only.)	Check the connection of all units in the system, data format, and data source, and then try again.
97	BLOCK MOVE ERR	Block Move was attempted outside RAM boundaries.	Select new RAM boundaries.
98	DEV EXCEEDED	Programming data exceeded the last device address.	Redefine parameters.
A1	NO ID FOUND	Programmer failed to detect an electronic identifier in the device.	Enter the correct family and pinout code for the device. See the device-support list in the User Note.

** Logic Device operations only.

Table 6-1. System Error Codes (cont.)

Code	Name	Description	Corrective Action
A2	INVALID ID	Device cannot be programmed with the current family and pinout codes if in effect.	Consult the device-support list in the User Note for the correct family and pinout code and re-enter the information into the programmer.
—	SYSTEM EPROM ERR	Programmer failed to detect the proper revision level of installed software.	Contact your local Data I/O Service Center.

Index

APPENDIX A

SCHEMATICS

Drawing No.	Title	Sheet(s)
30-701-0006	Schematic Diagram, Controller Board	4
30-701-0147	Schematic Diagram, Model 60A Waveform Generator Board	4
30-701-0136	Schematic Diagram, Keyboard/Display	1
30-701-0164	Schematic Diagram, Power Supply	1
30-701-0144	Schematic Diagram, PAL 20/24 Pin Adapter	1
30-701-0004	Schematic Diagram, IFL 20/24 Pin Adapter	1
30-701-0005	Schematic Diagram, IFL 28 Pin Adapter	1
30-701-2142	Schematic Diagram, Generic Mother Board	1
30-701-2143	Schematic Diagram, EPROM DIP Daughter Board	1
30-701-2189	Schematic Diagram, 28 Pin PLCC IFL Adapter	1
30-701-2190	Schematic Diagram, 20/28 Pin PLCC JEDEC Adapter	1
30-701-2191	Schematic Diagram, 20/28 Pin PLCC IFL Adapter	1
30-701-2192	Schematic Diagram, 28/28 Pin PLCC Non-JEDEC Adapter	1
30-701-0172	Model 60 Logic Programmer Handler Adapter	1
30-701-0196	Model 60H 20-Pin Performance Board	1
30-701-0197	Model 60H 24-Pin Performance Board	1
30-701-0198	Model 60H 28-Pin Performance Board	1
30-701-2007	Handler 300 20-Pin Performance Board	1
30-701-2008	Handler 300 24-Pin Performance Board	1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DAT:
A	RELEASE	SH			
B	INC ADCN A1 , ECP 0260	MP	BV		
C	INC ADCN B1 , ECP 0558	MP	BV	KIC	7-88

RDR PWR SW

J205 SERIAL PORT

SERIAL I/O INTF.

PROCESSOR

ADDRESS DECODE

TP16 ST2

POWER ON RESET

POWER SUPPLY J201

ADDRESS BUFFER

CONTROL GATING

CONTROL REG 1

PROM PAGING CONTROL

J202

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50 V.
3. LAST REFERENCE DESIGNATOR USED:
   C62, Q15, R123, U67, LS1, JP7, CR16, Y2, VR2, J205, TP19

4. PWR & GND.

REF. DES.	+ 5	GND
U11,57,59	20	10
U25,27-29,31,33-36, 39,40,58,60	16	8
U23	26	4
U2-5,21,22,24,26 30,32,37,38,41 45,46,54-56,66	14	7
U43	24	12
U1	7	1
U6-10	28	14
U44	40	20
U61,63,65	17	5
U12-19	8	16

5. IC'S WITH SPARE GATES:
   U2,3,20,22,24,45,46, 50,53,54,55,64,66,67

6. REFERENCE DESIGNATORS NOT USED:
   C32, 60,35,30,31, Q6, Q11, Q13, Q14
   TP1,2,14,15, JP1,3, U47, U62
   R42,71,70,63,62,52,69,65,64,60,54,55,61 58,57,102,99,100,101,56,51,118,120,119 121,92,91,93,94,115,117
   CR14, 13, 10, 11

P/N 701-0006-003

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O			
DSN. ENGR.	DATE:	TOLERANCES, UNLESS OTHERWISE SPECIFIED .XX ± .XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM, CONTROLLER BOARD			
MFG. ENGR.	DATE:					
QUAL. ASSUR.	DATE:	DRAWN BY: SUENEE H	DATE: 10/26/88	SIZE: D	CODE IDENT NO: 54193	DRAWING NO: 30-701-0006
ENGR. MGR.	DATE:	CHECKED BY:	DATE:	SCALE: NONE	D.A.D.	SHEET 1 OF 2

LTR	DESCRIPTION	DR	CHK	APPR	DATE
C	SEE SHT 1				8/13/7

P 1·A4 | E 1·A6 | B 1·A6 | L 1·A4 | C 1·A6 | U 1·A3 | R 1·A3 | M N 1·A4 | J K 1·A5 | D 1·A6 | CC 1·3A | F 1·A5

PROGRAM MEMORY

U8 2764 (E000-FFFF) OR 27128 (D000-FFFF)

U7 2732/2764 (C800-CBFF)

U6 2764/27128 PAGE2 (8000-BFFF)

U9 2764/27128 PAGE1 (8000-BFFF)

U10 2764/27128 PAGE0 (8000-BFFF)

U30 74HC04

U25 (CD78-F3) 4099

U5 74HC30

U30 74HC04

DRAM A8 MUX

EEPROM WRITE ENABLE

U4 74LS00 4PLCS

R17 33

DATA RAM (0000-7FFF)

J202

+48	49	+48 V
+25	45	+25 V
+5	30	+ 5 V
-9	47	- 9 V
	26	DIGITAL GND
	27	
	35	
	36	
TP9	25	
	3	ANALOG GND
	7	
	9	
	11	
	15	
	17	
	44	D_7
	42	D_6
	40	D_5
	38	D_4
	37	D_3
	39	D_2
	41	D_1
	43	D_0
	22	A_5
	19	A_4
	20	A_3
	21	A_2
	24	A_1
	23	A_0

U12 4164 | U13 4164 | U14 4164 | U15 4164 | U16 4164 | U17 4164 | U18 4164 | U19 4164

C3 .1 | C4 .1 | C5 .1 | C6 .1 | C7 .1 | C8 .1 | C9 .1 | C10 .1

U43 2K x 8 SRAM (C000-C7FF)

SCRATCH RAM

U42 X2210 (CC00-CC3F)

R33 1K

U32 74LS126

NONVOLATILE RAM

R18,33

U30 74HC04

U37 74LS00

U41 74LS00

R27,33

U37 74LS00

U41 74LS02 4 PLCS

U37 74LS00

D RAN ADDR. MUX.

R20 R24 R23 R19 33 4 PLCS

U36 74LS 157

U40 74LS 157

R22 R26 R25 R21 33 4 PLCS

U35 74LS 157

U39 74LS 157

JP5

POS A = NON PAGE MODE
POS B = PAGE MODE

U38 74LS 393

REFRESH COUNTER

C 4·D7 | X 4·D6 | L 4·D7 | J K 4·D5 3·D7

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
PROJ. ENGR.	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM, CONTROLLER BOARD
ENG. MGR.	DO NOT SCALE DRAWING	
Q.C. E. Bartlett 10/26/84	DRAWN BY: SUENEE H 10/16/84	SIZE D · CODE IDENT NO 54193 · DRAWING NO 30-701-0006
DATE	CHECKED BY: Ben Bartlett 10/26/84	SCALE NONE · SHEET 2 OF 4

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
C	SEE SHT 1				8/13/7

VCC SUPPLY

BIT SUPPLY

CE SUPPLY

V REFERENCE

VCC SWITCH

OVERCURRNT SENSE

J202
48 VREF
8 VCC
2 VCC RS
10 CE SUPPLY
12 BIT SUPPLY

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED xx ± xxx ± ANGULAR	TITLE SCHEMATIC DIAGRAM, CONTROLLER BOARD	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY SUENEE H	DATE	SIZE D / CODE INDENT NO 54193 / DRAWING NO 30-701-0006
ENGR MGR	DATE	CHECKED BY	DATE	SCALE NONE / SHEET 3 OF 4

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
e	SEE SHT 1				8/15/7

KB / DISPLAY J203

+48 V 1 — +48
+5 V 25 — +5
FIL 1 23 — FIL 1
FIL 2 22 — FIL 2
D GND 12, 19, 14, 20
RL7 21
RL3 18
RL2 17
RL1 16
RL0 15
LAMP ON 24
SL3 11
SL2 10
SL1 9
SL0 8
A1 2
A0 3
B3 4
B2 5
B1 6
B0 7
E 13
LAMP DOOR OUT 26

U44 (CC40-7F) 8279-5
WR RD RES CS A0 IRQ CLK
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
RL7 RL6 RL5 RL4 RL3 RL2 RL1 RL0
SL3 SL2 SL1 SL0
A3 A2 A1 A0 B3 B2 B1 B0
NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC

DATA BUFFER

U57 74LS373
8D 7D 6D 5D 4D 3D 2D 1D
8Q 7Q 6Q 5Q 4Q 3Q 2Q 1Q
G OE
R35 3.3K +5

U34 (D90-7) 1099
A B C D EN CL

CLOCK

U2 74LS04
R3 1K
R2 1K
Y1 5.0688 MHZ
JP2
C2 100PF 10CV
C1 470PF

Y2, 10 MHZ
U54 74S04
R95 1K
R96 1K
C57 100PF 100V
C56, 470PF
JP6

U59 74C374 (CD50)
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
CK OE

PULSE GENERATOR

U58 74LS161
CLR T LD A B C D CK P CY

U60 74LS161
T CLR LD A B C D CK P CY

U56 74LS74
P D Q CK CLR

U55 74LS00

U54 74S04

J202

31 PULSE
29 RD1 (CD98)
32 RD2 (CDA0)
33 OVCUR CLEAR
13 COMP

R97 10K
TP18 COMP

U61 AD7528 (CD88-9)
D7 D6 D5 D4 D3 D2 D1 D0
REF B RFB A OUT A AGND RFB B OUT B
CS WR A/B

U48 LM148
C36, .1
C33, .1
C34, 470PF
R66 4.99K, 1%
R67 12.7K, 1%
R68 .5W 5K, 18T → CW

UV DRIVE J204

+25
D GND
ON DETECT
START
ON

U37 74LS00
Q5 2N2222A
R34, 100K
R32, 10K
R31, 4.7K

BEEPER
CR1 IN4370A 2.4V
R2 1N148
LS1 GMB01
JP4
R1 10K
Q1 2N2222A

U3 7406
U2 74L04

APPROVALS	DATE
DSN ENGR	
MFG ENGR	4/1/84
QUAL ASSUR	10/26/84
ENGR MGR	

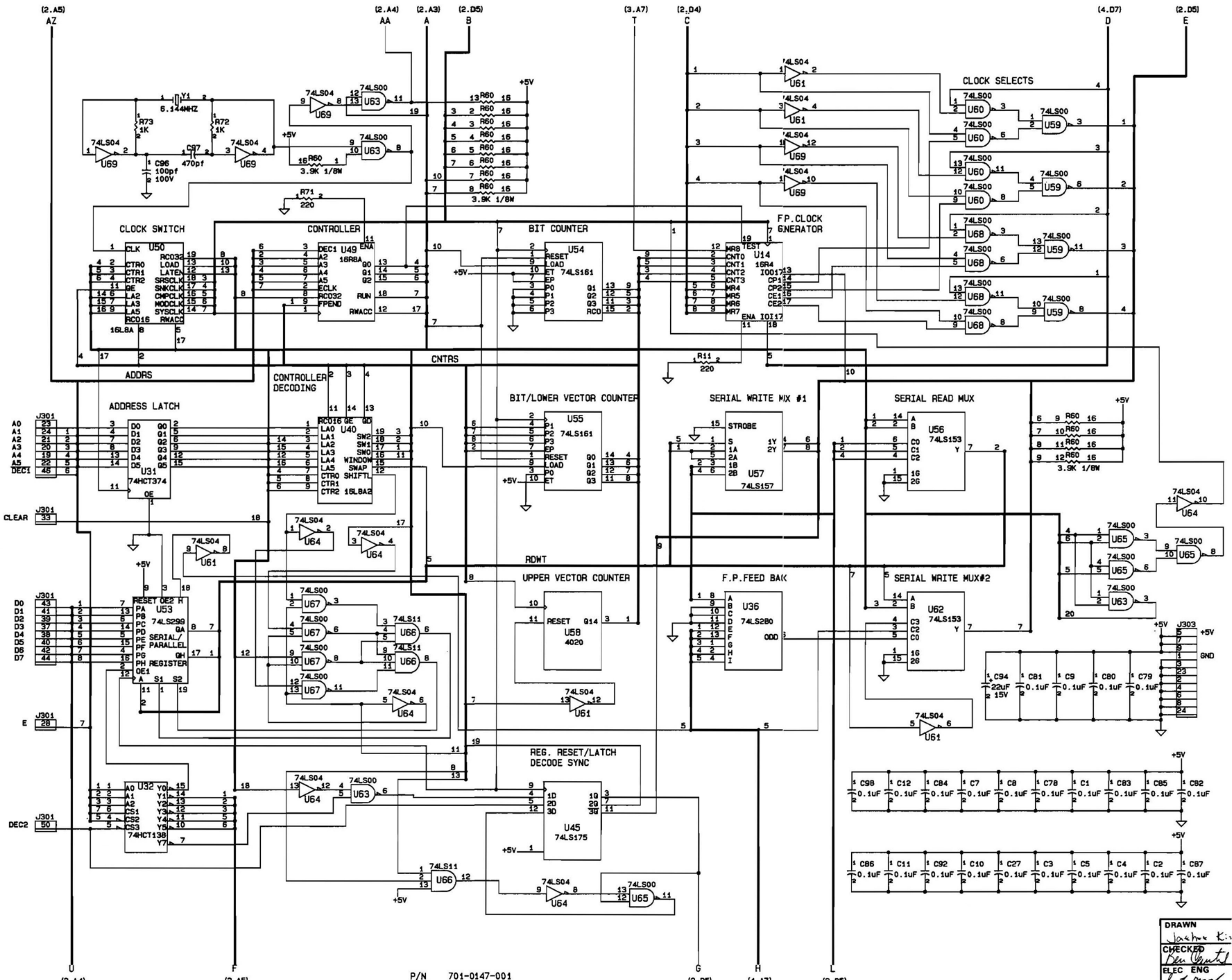
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED XX XXX ANGULAR

DRAWN BY SUENEE H DATE 10/16/84
CHECKED BY DATE 10/24/84

DATA I/O

TITLE
SCHEMATIC DIAGRAM, CONTROLLER BOARD

SIZE D | CODE IDENT NO 54193 | DRAWING NO 30-701-0006
SCALE NONE | SHEET 4 OF 4



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				
B	INC. PER ECP0067, ADCN A1	NL			
C	" " " ADCN B1+B2	SH			
D	" " ECPO115 ADCN C1	SH			

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5 %.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148 EXCEPT CR15-47, 80-93.
4. LAST REFERENCE DESIGNATOR USED: CR103, Q77, C105, E32, R91, U69
5. REFERENCE DESIGNATORS NOT USED: U4, U46, C99, R40-42, 49-51, 85-88, Q70.
6. R4-7, 31, 32, 52-54, 58 ARE 2W, 2%.
7. C30-58, 60-77 ARE 100V.
8. POWER AND GROUND:

REFERENCE DESIGNATOR	+5V	GND
U1-3, 5-13, 32, 37-40, 45, 48, 54-58, 62	16	8
U14, 31, 33, 34, 41-43, 49-53	20	10
U15, 16, 35, 36, 44, 59-61, 63-69	14	7

	DATE
DRAWN Joshua Kim	10/84
CHECKED	10/24/4
ELEC ENG	
MECH ENG	
MFG ENG	
QUAL ASSUR	
APPD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE SCHEMATIC DIAGRAM, MODEL 60A WAVEFORM GENERATOR 80.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-0147

SCALE NONE SHEET 1 OF 4

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
D	SEE SHEET ONE				

FERRITE BEADS

OUTPUT REGISTER

F.P. CLOCK SELECT REGISTER

T-RISE SELECT RESISTER

INPUT DATA LATCH

STATUS REGISTER

MISC. READ BUFFER

MISC. REGISTER

HANDLER INPUT REGISTER

HANDLER OUTPUT REGISTER

TSEL

LDAT

HDLRI

HDLRO

DRAWN	Jaehee Kim	DATE	11/22
CHECKED			6.2.94
ELEC ENG			
MECH ENG			
MFG ENG			
QUAL ASSUR			
APPD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES. UNLESS OTHERWISE SPECIFIED:
.XX ±
.XXX ±
ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DIAGRAM, MODEL 60A WAVEFORM GENERATOR BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-0147

SCALE NONE SHEET 2 OF 4

BRUNING 44-141

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
D	SEE SHEET ONE	JK	[illegible]		

SOURCE DRIVER REGISTERS

U12 U1 U3 U11 UB U2 — 74HC595 (A, CK, SCK, RESET, OE; LA–LH)

Q13 Q10 Q8 Q7 Q3 Q2 Q16 PQ3725 — R31 1K; R6 1K; R5 220; R4 220; R2 220

Q42 Q31 Q30 Q29 Q38 Q28 Q39 Q37 Q23 Q36 Q41 MJE251 — 330PF

Q25 Q54 Q21 Q27 Q61 Q40 Q26 Q22 Q32 Q34 Q24 MJE251 — 330PF

Q59 Q58 Q48 Q57 Q47 Q56 Q55 Q46 Q44 Q53 Q35 MJE251 — 330PF

Q52 Q51 Q65 Q63 Q62 Q45 Q43 Q50 Q64 Q67 Q66 MJE251 — 330PF

CR26 CR46 CR45 CR24 CR44 CR21 CR22 CR43 CR20 CR40 CR19 CR25

CR39 CR38 CR16 CR36 CR35 CR47 CR23 CR42 CR37 CR15 CR17 CR41

CR34 CR33 CR32 CR31 CR30 CR29 CR28 CR27 CR93 CR91 CR89 CR18

CR88 CR87 CR85 CR83 CR81 CR92 CR90 CR86 CR84 CR82 CR80 CR18

B (4.D8) K (2.D5) L (2.D6) T (1.D5)

DRAWN	Jaehoe Kim	DATE	11/6/84
CHECKED	[illegible]		
ELEC ENG			
MECH ENG			
MFG ENG			
QUAL ASSUR			
APPD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

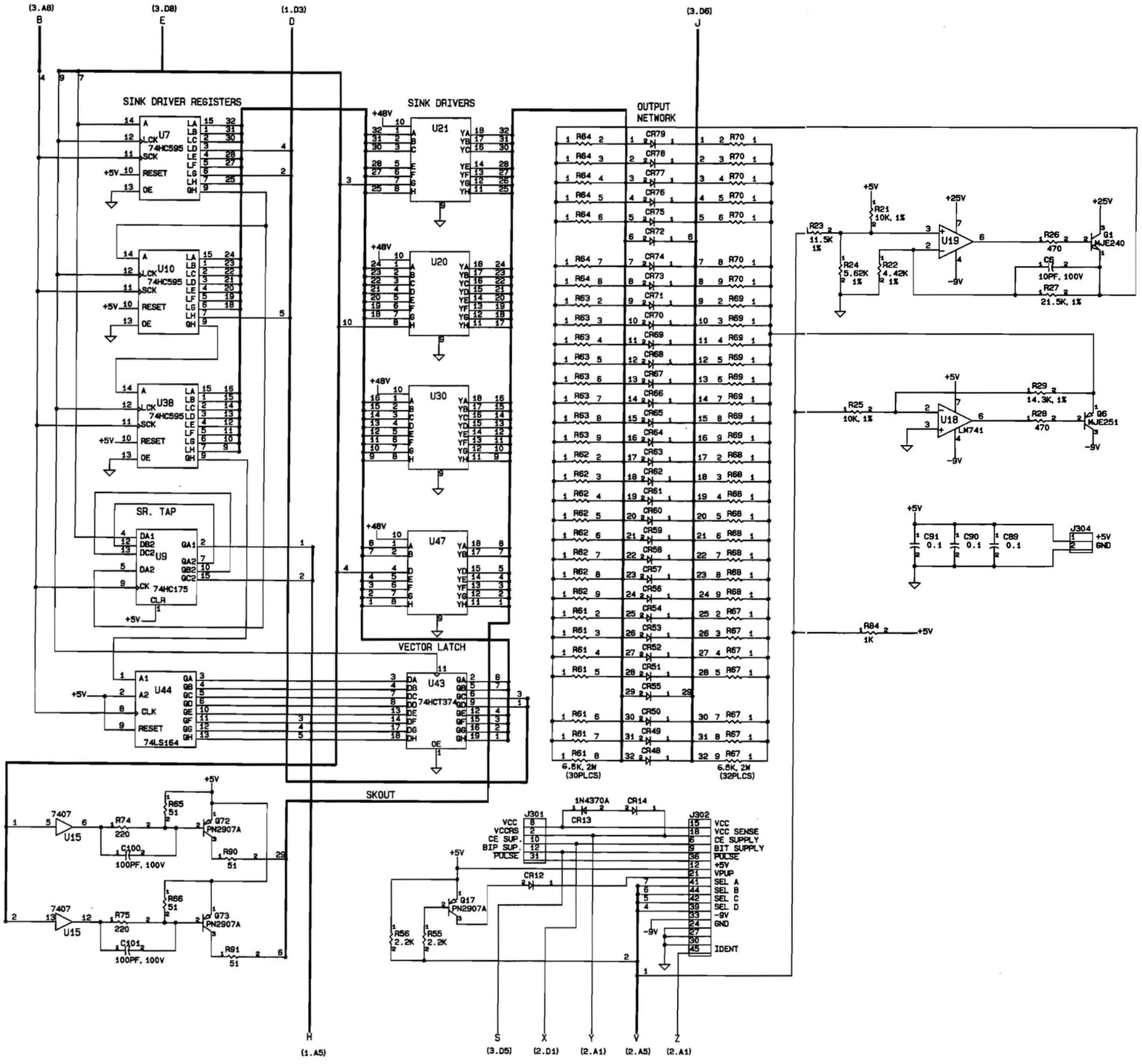
TITLE: SCHEMATIC DIAGRAM, MODEL 60A WAVEFORM GENERATOR BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-0147

SCALE NONE SHEET [illegible] OF [illegible]

BRUNING 44 141

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
D	SEE SHEET ONE				



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DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
Jaehee Kim	10/86		
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM, MODEL 60A WAVEFORM GENERATOR BD.
ELEC ENG			
MECH ENG		DO NOT SCALE DRAWING	SIZE: D; FSCM NO.: 54193; DRAWING NO.: 30-701-0147
MFG ENG			
QUAL ASSUR			SCALE NONE; SHEET OF
APPD			

BRUNING A4 141

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	[illegible]	[illegible]	RJS	11-1-79
B	INCORP ADCN A1 PER ECP 0009	RL	[illegible]	[illegible]	4-3-84
C	INCORP ADCN B1 PER ECP 0074	SH	[illegible]		
D	INCORP ADCN C1 PER ECP 0103	JK	[illegible]	[illegible]	[illegible]
E	INCORP ADCN D1 PER ECP 0160	MP	[illegible]	[illegible]	3-26-85

J401 IN

BO 7
B1 6
B2 5
B3 4
AO 3
A1 2

U13 PROM TS 256X4

U12 74LS138

U14 74LS93

U15 4051

U7 74LS04

UV LAMP LED IND DS1

R5 470

LAMP ON 24

E 13

SL0 8
SL1 9
SL2 10
SL3 11

RL0 15
RL1 16
RL2 17
RL3 18
RL7 21

LAMP DOOR OUT 26

+48V 1
+5V 25

DIGITAL GND 12
DIGITAL GND 14
DIGITAL GND 19
DIGITAL GND 20

FIL 1 23
FIL 2 22

C1,2 .1
C3 .1

R6 750 1/2W
Q1 MJE240

CR1 1N4754A/39V
CR2 1N4734A 5.6V

U6 74LS175
U5 74LS175
U4 74LS175
U3 74LS175

U11 6118
U10 6118
U9 6118
U8 6118

C5 .1
C4 .1

R4 10K
R3 10K
R2 10K
R1 10K

J2 4028
J1 4028

DISPLAY DRIVER

KEYBOARD

S1 S2 S3 S4 S5 S6
S7 S8 S9 S10 S11 S12
S13 S14 S15 S16 S17 S18
S19 S20 S21 S22 S23 S24
S25 S26

DS2 OUT

TO F.I.P. DISPLAY ANODES (CHARACTER SEGMENTS)

34	A
32	B
30	K
28	I
25	L
23	H
21	C
19	DP
17	D
15	M
13	J
12	COM
10	N
8	E
6	G
4	F
36	NC
26	NC
2	NC

35	G1
33	G2
31	G3
29	G4
27	G5
24	G6
22	G7
20	G8

TO F.I.P. DISPLAY GRIDS (DIGITS)

18	G9
16	G10
14	G11
11	G12
9	G13
7	G14
5	G15
3	G16
1	F FILIMENT
37	F SUPPLY

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS VALUES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REFERENCE DESIGNATOR USED: U15, C 2, J401, R6, S26, DS2, CR2, Q1.
4. CONNECTIONS NOT SHOWN:

I.C. NUMBER	+44	+5	GND
U1-6,12,13,15		16	8
U14		5	10
U8, 9, 10, 11	10		9
U7		14	7

5. UNUSED GATES:

U7 74LS04, 4 PLACES

6. DISPLAY SEGMENTS 311-2000

DECIMAL POINT
COMMA

7 JPR-CR2 FOR -006 ONLY.

701-0136-008 SHOWN
-010 NOTED 7

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		DATA I/O			
DSN. ENGR. [illegible]	DATE 11-1-79	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ANGULAR		TITLE SCHEMATIC DIAGRAM, KEYBOARD/DISPLAY			
MFG. ENGR. [illegible]	DATE 4/3/84						
QUAL. ASSUR. [illegible]	DATE 4-10-84	DRAWN BY: G.R./AK	DATE 6-19-82	SIZE D	CODE IDENT. NO. 54193	DRAWING NO. 30-701-0136	
ENGR. MGR. [illegible]	DATE 4/10/84	CHECKED BY: [illegible]	DATE 11/10/79	SCALE NONE		SHEET 1 OF 1	

BRUNING 49270

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	[illegible]	[illegible]	[illegible]	[illegible]
B	INC ADCN A1,2,3 ECP 0197,0253,0328	[illegible]		[illegible]	8-17-87

VOLTAGE	CONTACTS
100	a,c,e
120	b,c,e
220	a,d
240	b,d

GREEN
WHITE
WHITE
FAN
RED/WHT
BLACK
F
E
D
BLACK
B
OFF-ON
C
BLK/GRN
A
BLK/RED
G
FUSE
1.5A
L
GND
N
LINE FILTER
N GND L
NEUT
GND
LINE

P101
YEL 1
YEL 8
11.7 VRMS
ORN 4
ORN 6
8.2 VRMS
BLUE 2
BLUE 9
37.6 VRMS
BRN 3
BRN 7
27.5 VRMS
RED 10
RED/YEL 12
5.5 VRMS CT
RED 11

J101
F1 2A
1N4002 4 PL
CR3 CR1 CR4 CR2
C4 2200/50V
R5 10K
LM 323 K VR 3 (REF) V IN GND VOUT
P102 1 2 3
J102 1 2 3
IN5822 4 PL
CR14 CR16 CR13 CR15
C3 6800/16V
C2 6800 16V
R6 1K 1/2W
C8 1/50V
CR17 IN53?A 6.2V 5W
RADIAL LEAD 1N4002 4 PL
C9 .1 100V
CR7 CR5 CR8 CR6
C5 1000/63V
R2 15K 1/2W
1N5392 4 PL
CR11 CR9 CR12 CR10
C1 2200 50V
R1 10K 1/2W
VP.2 LM317T IN OUT ADJ
R4 4.75K 1%
R3 249 1%
R7 1K
CR18 1N4739A 9.1V, 1W
C7 1/50V
7815CT VR1 OUT IN GND
C6 1/50V

J103
5 -15V
2 +5V
3 GND
1 GND
6 +48V
9 +25V
8 5.5 VAC
10 +15V
7 5.5 VAC

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REFERENCE DESIGNATOR USED: C9, CR18, F1, J103, R7, VR2

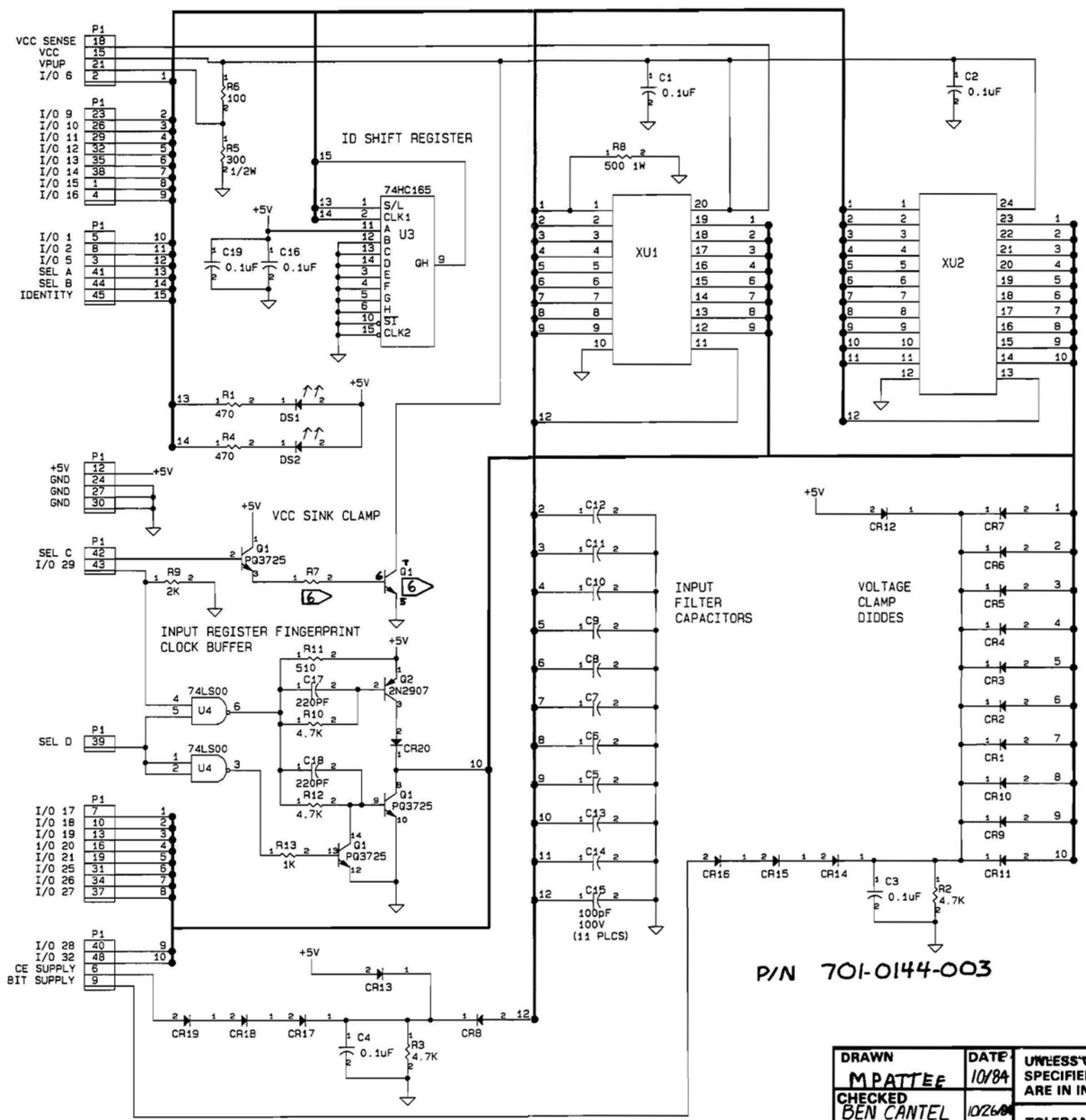
REF ONLY
44-709-0125

701-0164-003

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O			
DSN. ENGR. [illegible]	DATE [illegible]	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, POWER SUPPLY			
MFG. ENGR. [illegible]	DATE [illegible]					
QUAL. ASSUR. [illegible]	DATE [illegible]	DRAWN BY: [illegible]	DATE [illegible]	SIZE D	CODE IDENT. NO. 54193	DRAWING NO. 30-701-0164
ENGR. MGR. [illegible]	DATE [illegible]	CHECKED BY: [illegible]	DATE [illegible]	SCALE NONE	D.A.D.	SHEET 1 OF 1

BRUNING 49270

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	BC	J.L.GRAY	10/84
B	INC ADCN A1 PER ECP 0478	RW	KAT	K. MILLER	6/85
C	INC ADCN PER ECP 0504	LW	BV 3-9-88	3-9-88	2/88



P/N 701-0144-003

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED. R13, C19, CR20, DS2, P1, Q2, U4.
5. PWR & GND.

REF. DESIG.	+5V	GND
U3	16	8
U4	14	7

6 COMPONENTS OMITTED: R7, Q1 (PINS 5, 6, 7 ONLY)

DRAWN	M PATTEE	10/84
CHECKED	BEN CANTEL	10/26/84
ELEC ENG	J. L. GRAY	10/26/84
MECH ENG	S. T. R.	10/26/84
MFG ENG	RON FISCHER	10/26/84
QUAL ASSUR	E. BARTLETT	10/26/84
APPD	G. JAMES	10/26/84

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

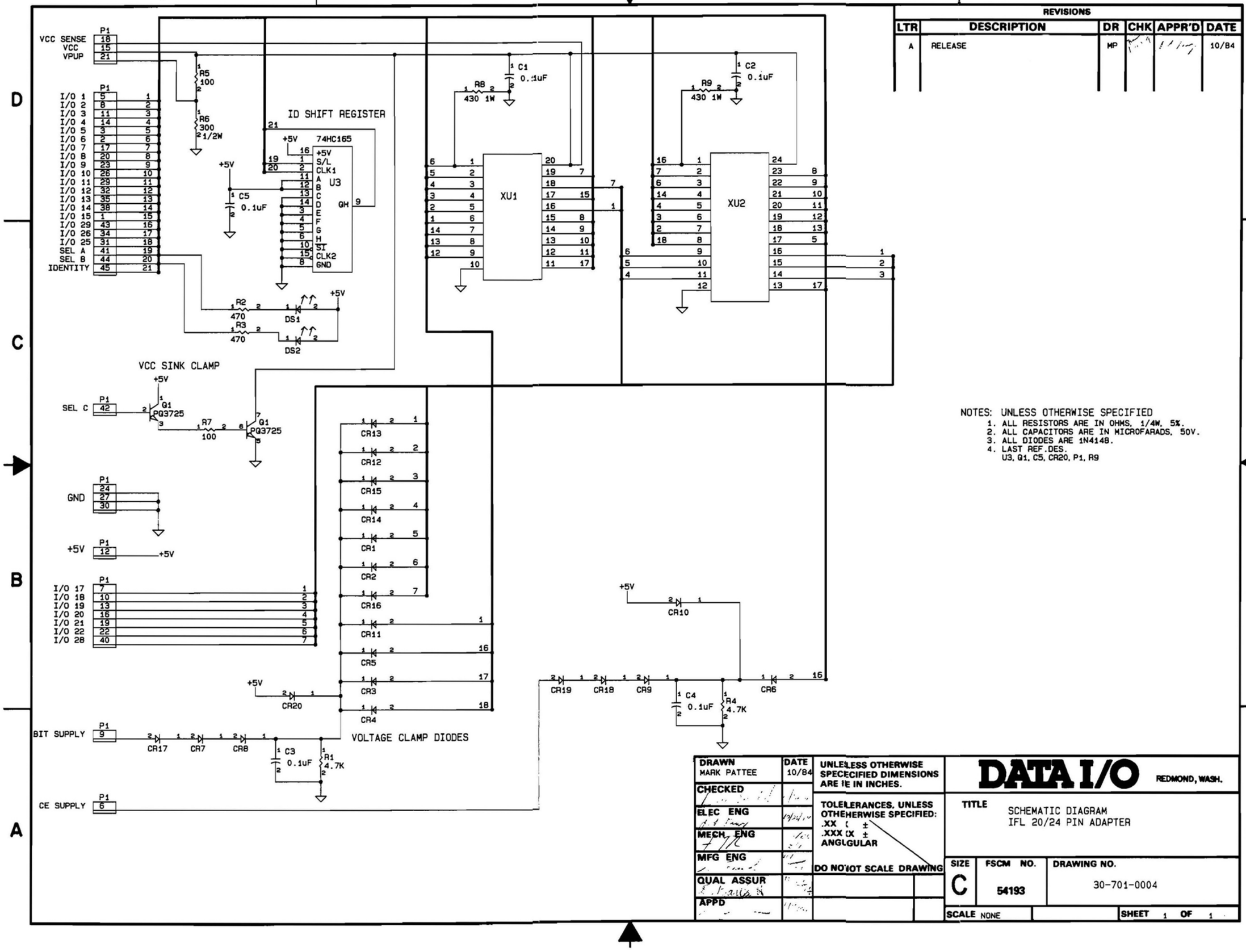
DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DIAGRAM PAL 20/24 PIN ADAPTER

SIZE	FSCM NO.	DRAWING NO
C	54193	30-701-0144

SCALE NONE SHEET 1 OF 1

FERGUSON & SONS 100867

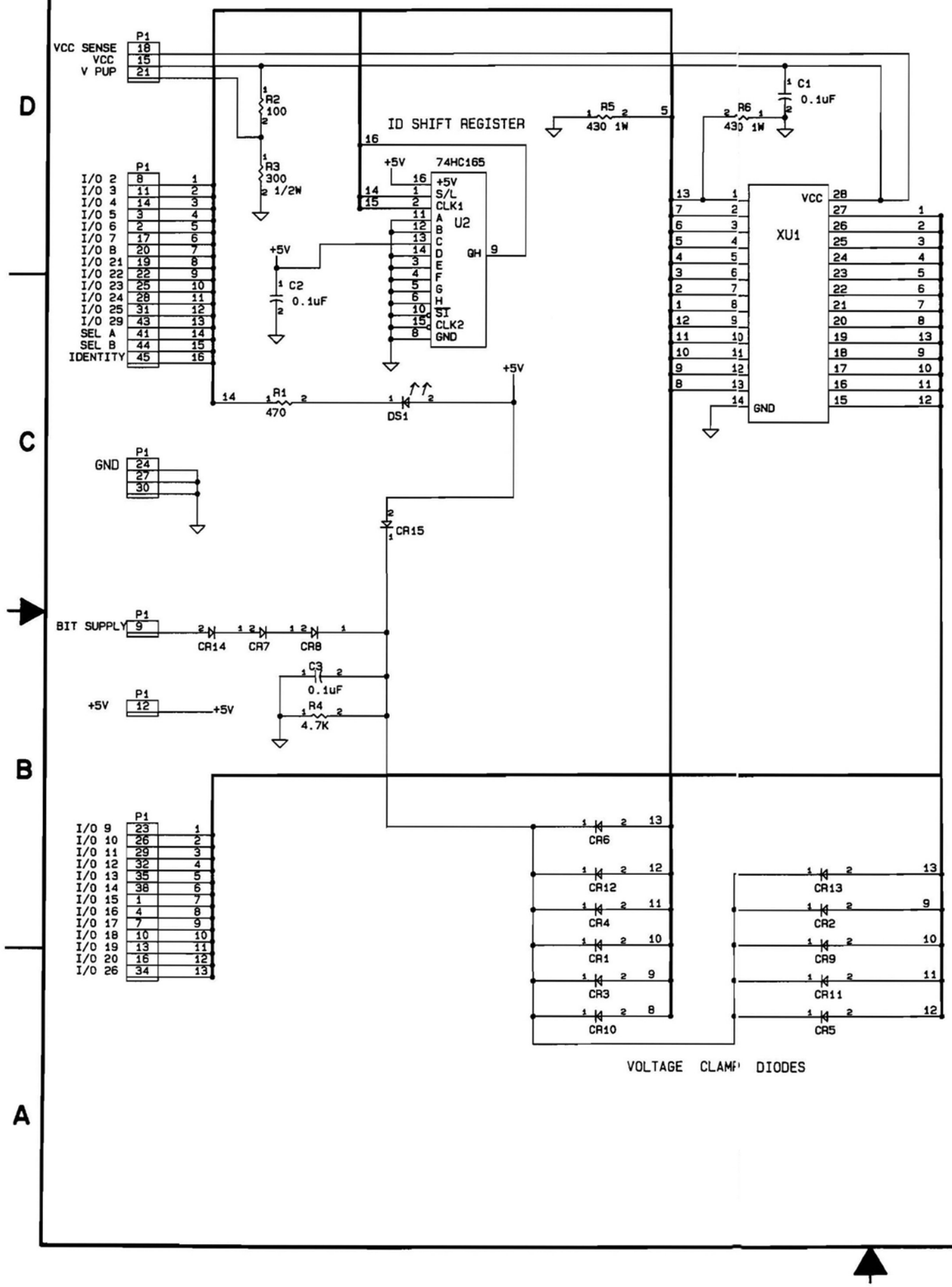


REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP			10/84

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REF.DES.
U3, Q1, C5, CR20, P1, R9

DRAWN MARK PATTEE	DATE 10/84	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX (± .XXX (± ANGULAR	TITLE SCHEMATIC DIAGRAM IFL 20/24 PIN ADAPTER
ELEC ENG		DO NOT SCALE DRAWING	SIZE C · FSCM NO. 54193 · DRAWING NO. 30-701-0004
MECH ENG			SCALE NONE · SHEET 1 OF 1
MFG ENG			
QUAL ASSUR			
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP			10/84

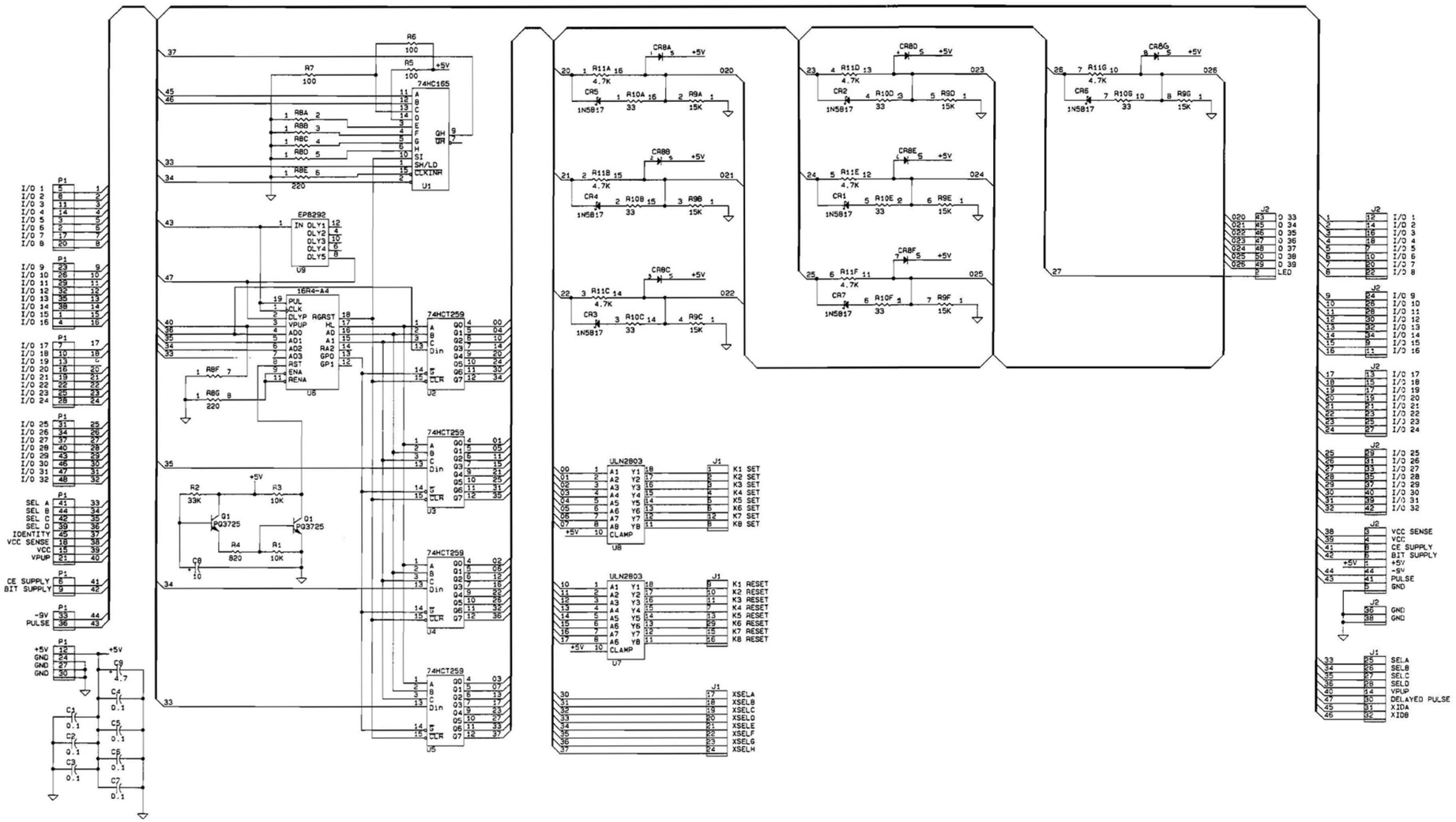


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W, 5% IN OHMS.
2. ALL CAPACITORS ARE 50V AND IN MICOFARADS.
3. ALL DOIDES ARE 1N4148.
4. LAST REF DES USED:
   U2, R6, CR15, C3, DS1, P1

DRAWN MARK PATTEE	DATE 10/84	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM IFL 28 PIN ADAPTER
ELEC ENG			
MECH ENG		DO NOT SCALE DRAWING	SIZE C · FSCM NO. 54193 · DRAWING NO. 30-701-0005
MFG ENG			
QUAL ASSUR			SCALE NONE · SHEET 1 OF 1
APPD			

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
B	REDRAWN W/O CHANGE, INC. ADCN A1, PER ECP 0000	[illegible] 9-87	BB 9-28-87	Barry Valdivia	9-28-87



P/N 701-2142-001

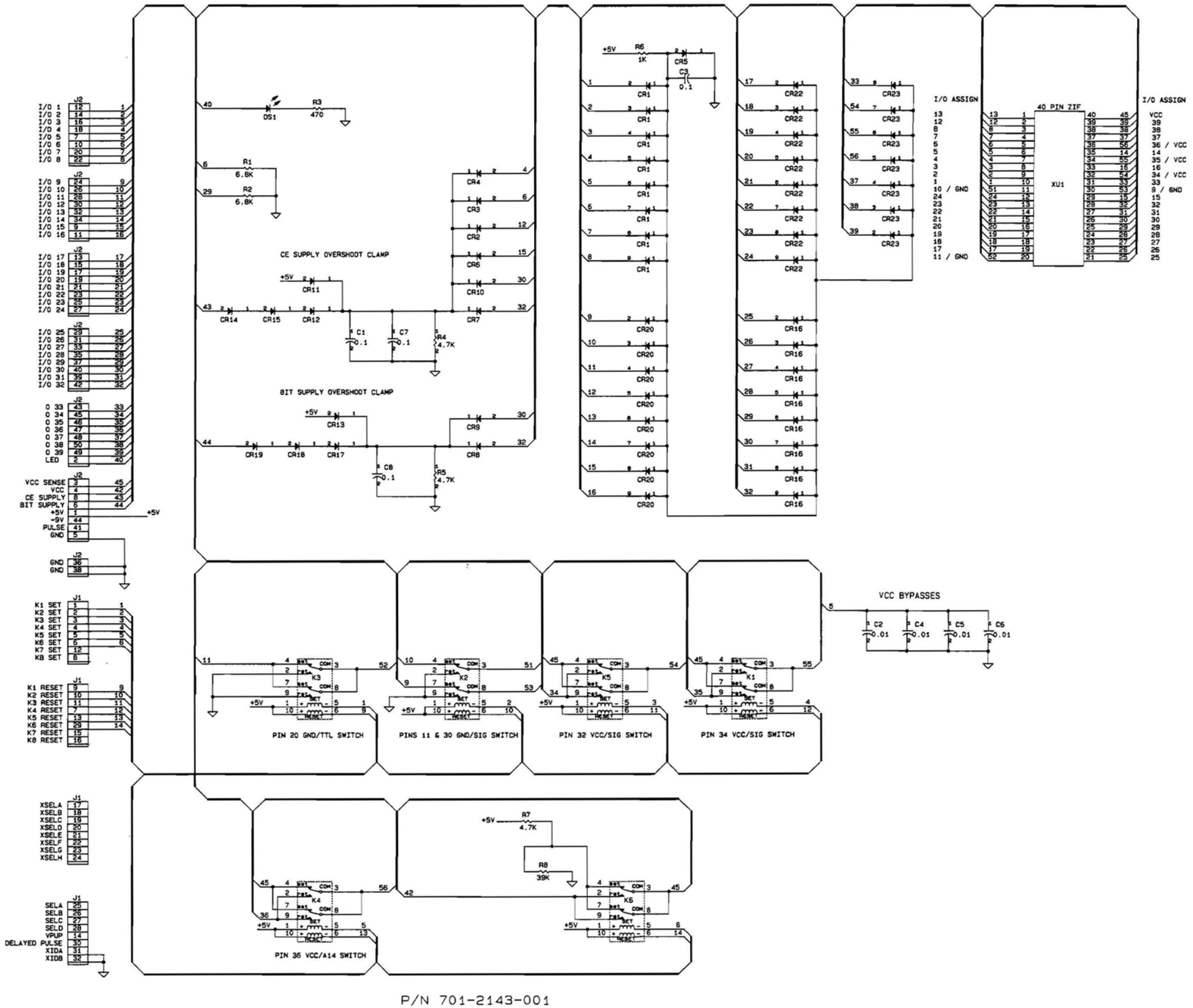
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5% .
2. ALL CAPACITORS ARE IN MICROFARADS, 50V .
3. ALL DIODES ARE 1N4148 .
4. LAST REFERENCE DESIGNATOR USED: CR8, R11, C9, J2, P1, Q1, U9
5. POWER AND GROUND:

REFERENCE DESIGNATOR	GND	+5V
U1-U5	8	16
U6	10	20
U7, U8	9	18
U9	7	14

DRAWN	DATE 9-28-87	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. REGESTER		TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, GENERIC MOTHER BOARD
ELEC ENG J. GRAY			
MECH ENG B. VALDIVIA		DO NOT SCALE DRAWING	SIZE D / FSCM NO. 54193 / DRAWING NO. 30-701-2142
MFG ENG A. BAKCUS			
QUAL ASSUR R. SHAW			SCALE — / D.A.D. / SHEET 1 OF 1
APPD K. MILLER			

FERGUSON & SONS 100024

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP			3-27-87
B	INCORP. APCH#1 PERFCP0000	SH			8/87



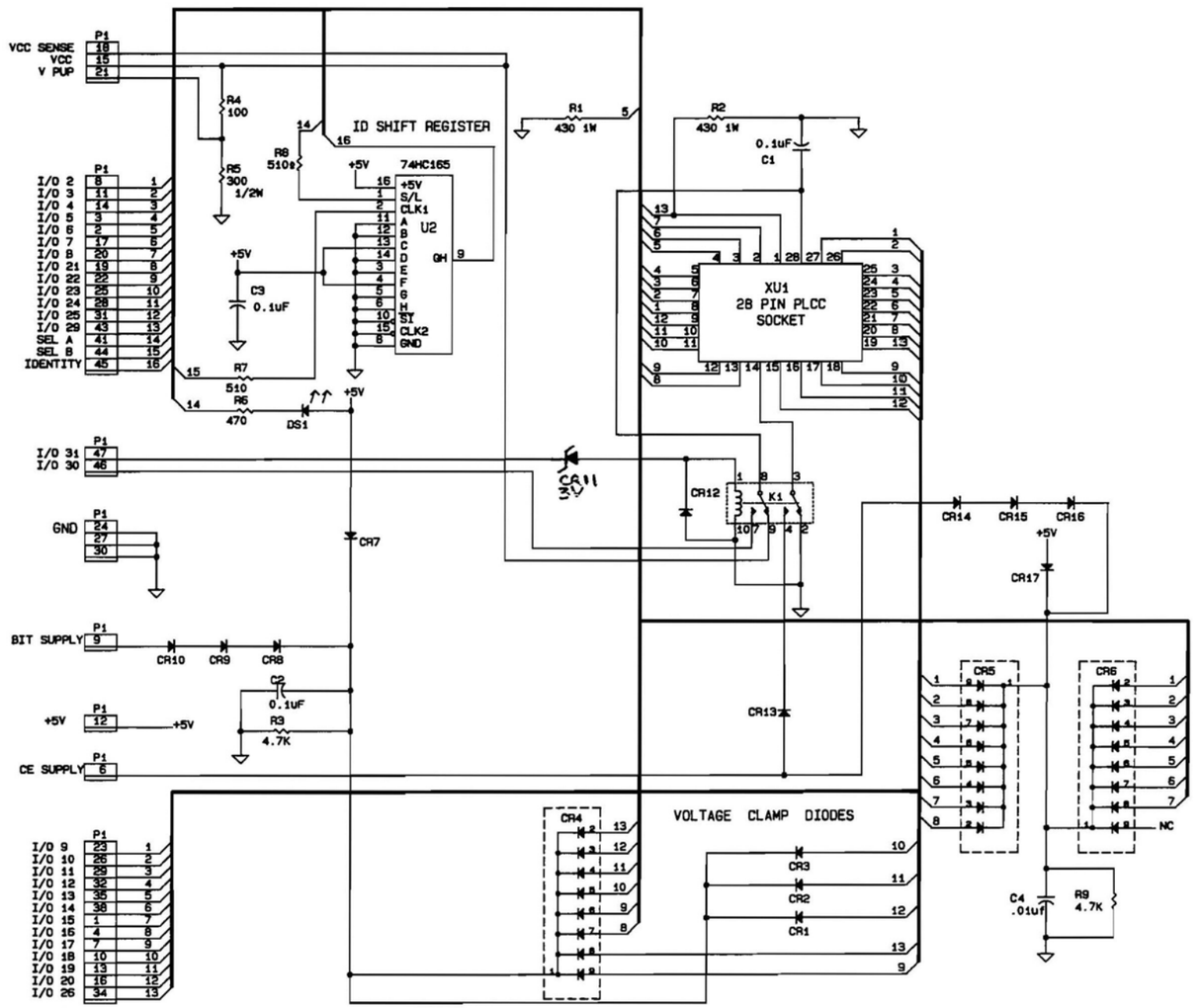
P/N 701-2143-001

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED:
   CR23, K6, XU1, J2, Q1, R8, C8, DS1

DRAWN M. Patten	DATE 3/27/87	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED Eric Fugate	4/6/87	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, EPROM DIP DAUGHTER BD.
ELEC ENG	4/6/87		
MECH ENG B. Valdivia	4/6/87		
MFG ENG	4/6/87	DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54193 · DRAWING NO. 30-701-2193
QUAL ASSUR	4/6/87		SCALE — · D.A.D · SHEET 1 OF 1
APPD	4/6/87		

FERGUSON & SONS 100867

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	BK	KM	4/88
B	INC A1 PER ECP0541	JH	RN	JH	7/88



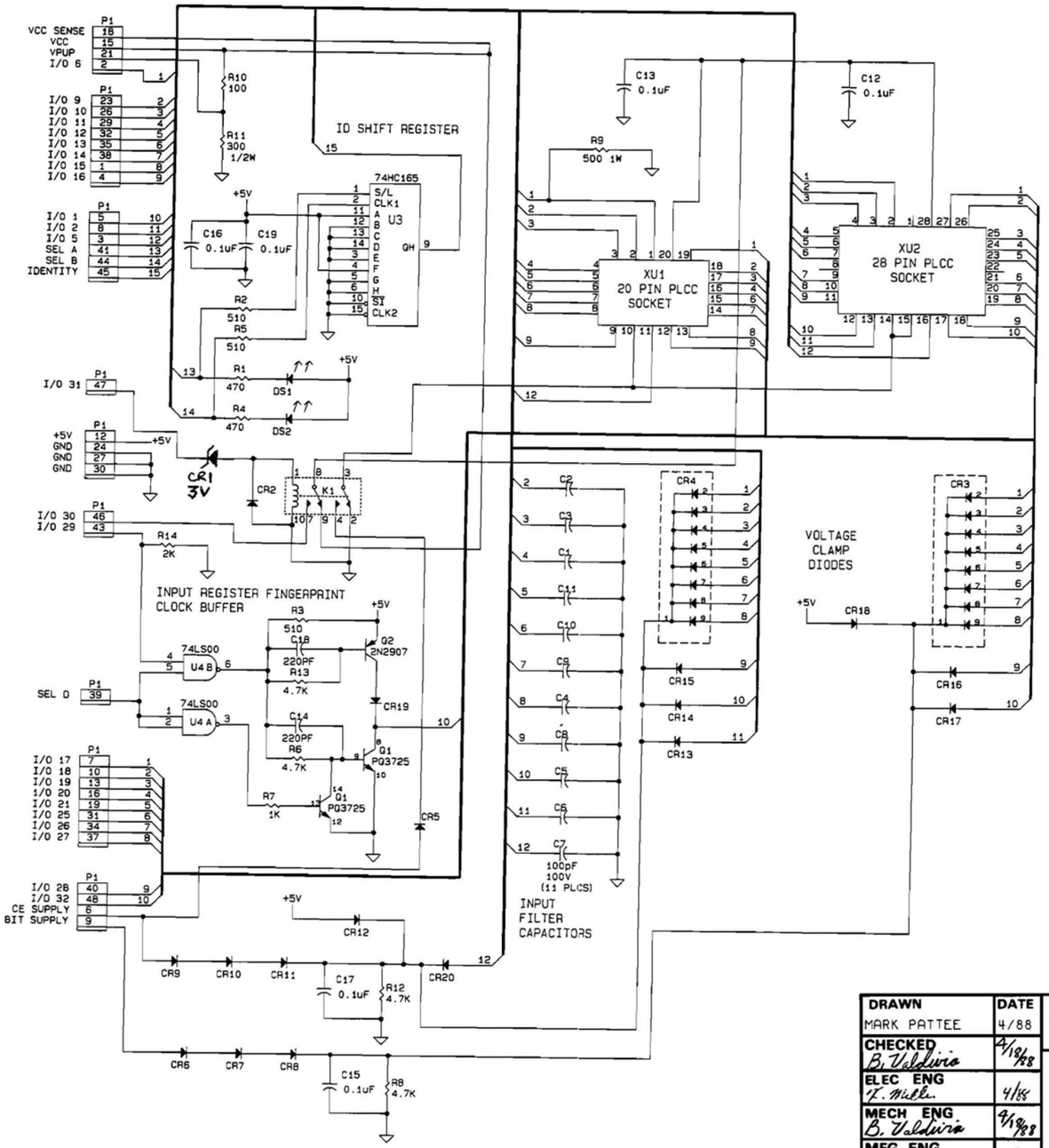
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W, 5% IN OHMS.
2. ALL CAPACITORS ARE 50V AND IN MICOFARADS.
3. ALL DIODES ARE 1N4148.
4. LAST REF DES USED: U2, R9, CR17, C4, DS1, P1

P/N: 701-2189-001

DRAWN MARK PATTEE	DATE 4/88	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED	5/4/88	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM 28 PIN IFL PLCC SKT ADPT
ELEC ENG	5/4/88		
MECH ENG B. Valdivia	5/4/88		
MFG ENG	5/4/88	DO NOT SCALE DRAWING	SIZE C / FSCM NO. 54193 / DRAWING NO. 30-701-2189
QUAL ASSUR	5/4/88		
APPD	5/4/88		SCALE 1/1 / D.A.D. / SHEET 1 OF 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	A RELEASE	MP			4/88
B	INCAI PER ECP 0541	JH	RN	JH	7/88



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED.
   R13, C19, CR20, DS2, P1, Q2, U4.
5. PWR & GND.

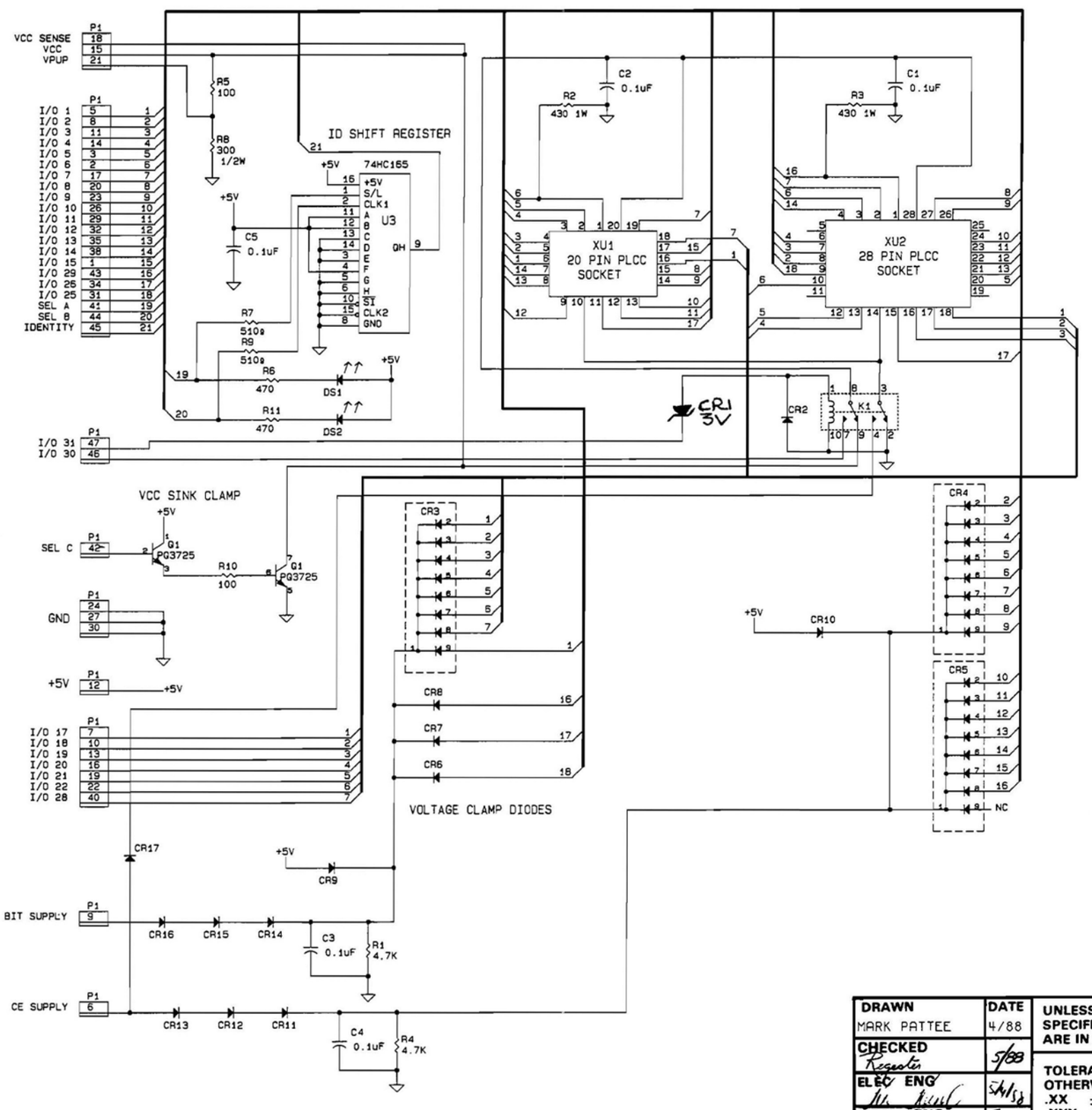
REF. DESIG.	+5V	GND
U3	16	8
U4	14	7

6. REFERENCE DESIGNATORS NOT USED:
   R7

P/N: 701-2190-001

DRAWN MARK PATTEE	DATE 4/88	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED B. Valdivia	4/18/88	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM 20/28 PIN JEDEC ADAPTER
ELEC ENG T. Mick	4/88		
MECH ENG B. Valdivia	4/18/88		
MFG ENG D. Beeson	4/13/88	DO NOT SCALE DRAWING	SIZE C · FSCM NO. 54193 · DRAWING NO. 30-701-2190
QUAL ASSUR Bright	4/13/88		SCALE 1/1 · D.A.D. · SHEET 1 OF 1
APPD T. Mick	4/18		

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	BF	KM	4/88
B	INC A1 PER ECP 0541	JH	RW	JM	7/88



NOTES: UNLESS OTHERWISE SPECIFIED

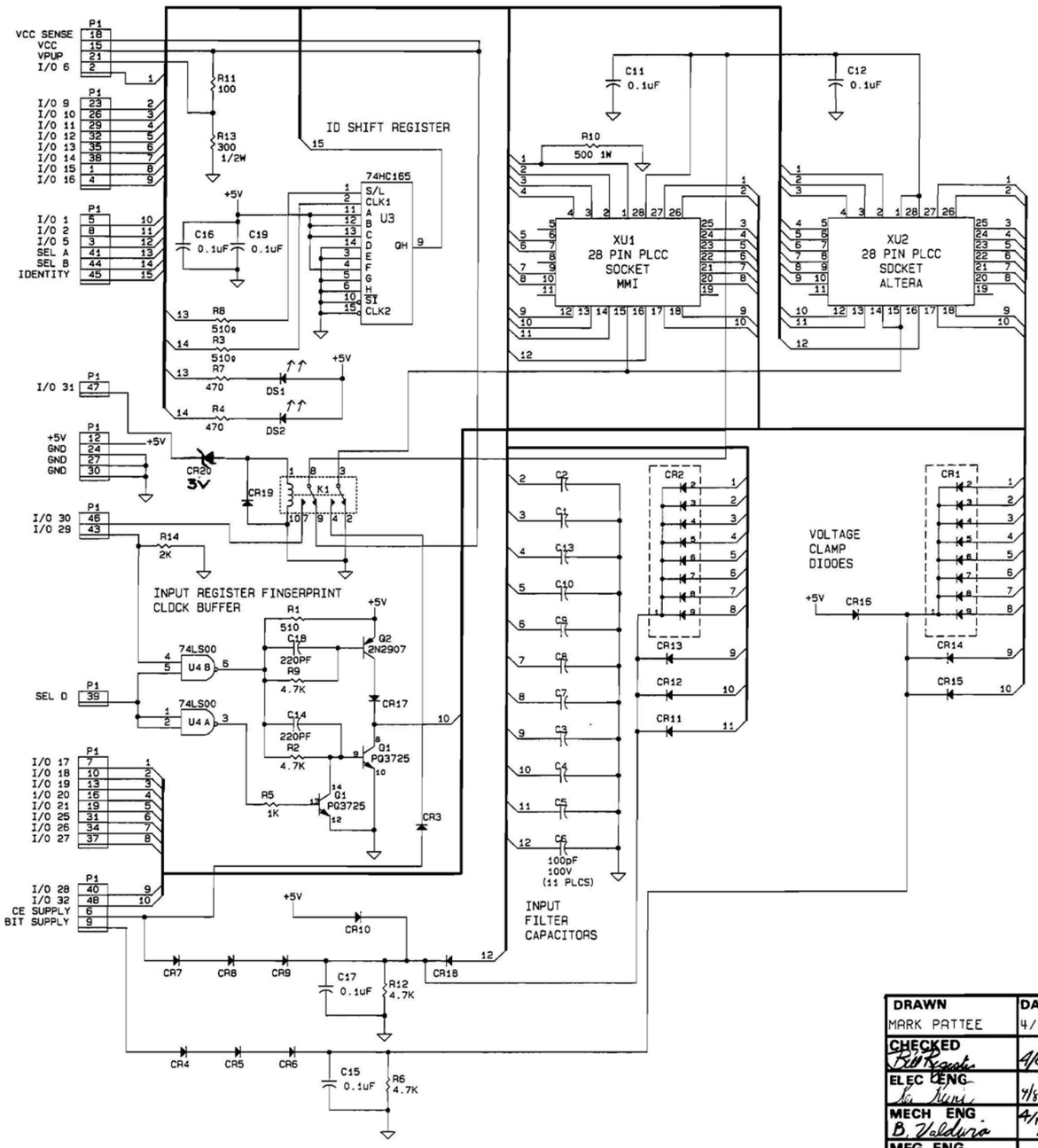
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATORS USED: U3, Q1, C5, CR17, P1, R11

P/N: 701-2191-001

DRAWN MARK PATTEE	DATE 4/88	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED Regnier	5/88	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM 20/28 PLCC IFL SKT ADPT
ELEC ENG	5/11/88	DO NOT SCALE DRAWING	SIZE C · FSCM NO. 54193 · DRAWING NO. 30-701-2191
MECH ENG B. Valdivia	5/4/88		SCALE 1/1 · D.A.D. · SHEET 1 OF 1
MFG ENG	5/4/88		
QUAL ASSUR	5/4/88		
APPD	5/11/88		

FERGUSON & SONS 100667

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	BP	[signature]	4/88
B	INC A1 PER ECP 0541	JH	RN	[signature]	7/88



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 1N4148.
4. LAST REFERENCE DESIGNATOR USED.
   R15, C19, CR20, DS2, P1, Q2, U4.
5. PWR & GND.

REF. DESIG.	+5V	GND
U3	16	8
U4	14	7

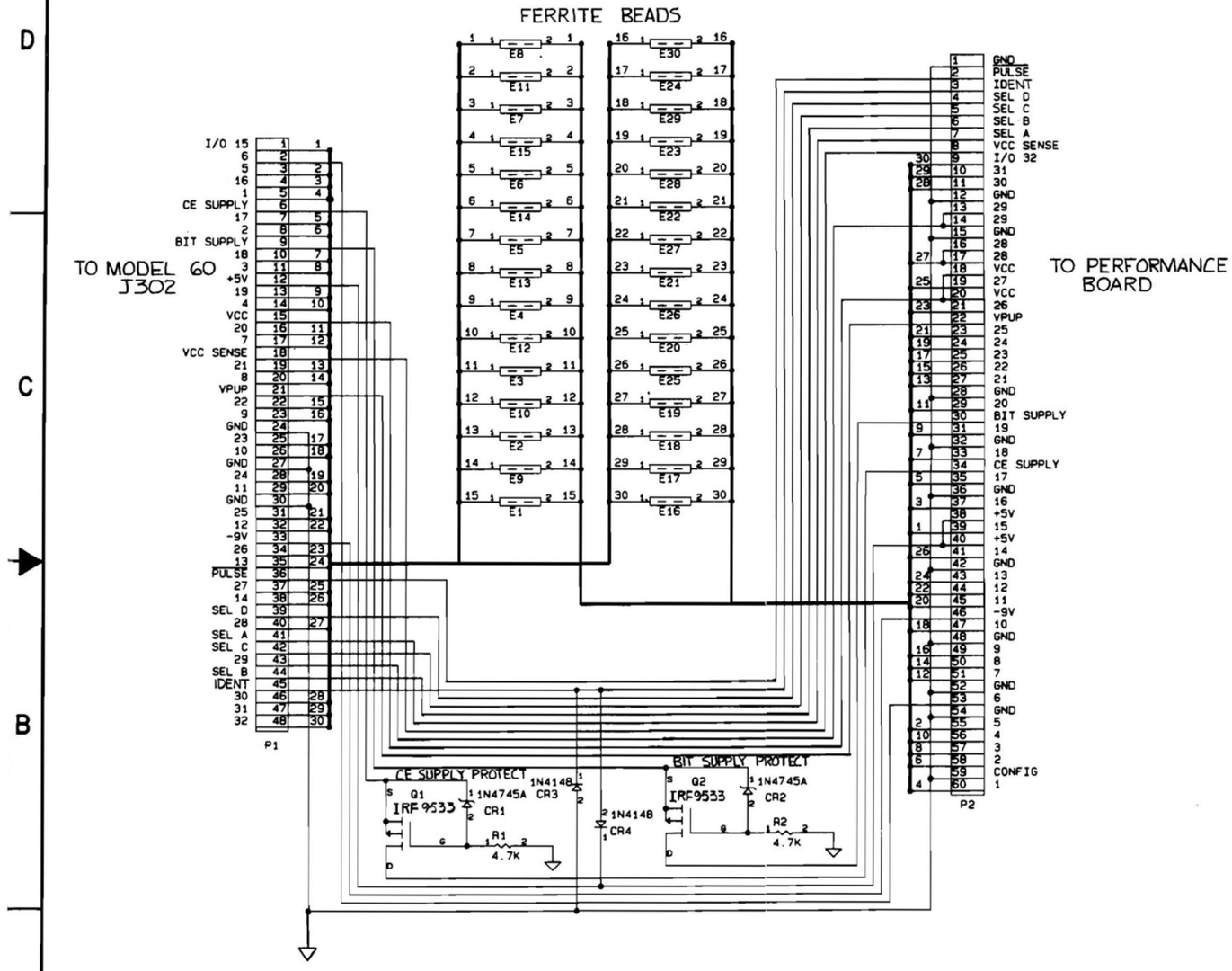
6. REFERENCE DESIGNATORS NOT USED:
   R7

P/N: 701-2192-001

DRAWN MARK PATTEE	DATE 4/88	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED [signature]	4/88	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM 28/28 MMI/ALTERA ADAPTER
ELEC ENG [signature]	4/88		
MECH ENG B. Valdivia	4/18/88	DO NOT SCALE DRAWING	SIZE C / FSCM NO. 54193 / DRAWING NO. 30-701-2192
MFG ENG [signature]	4/18/88		
QUAL ASSUR [signature]	4/18/8		SCALE 1/1 / D.A.D. / SHEET 1 OF 1
APPD [signature]	4/88		

FERGUSON & SONS 100667

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP	[illegible]	[illegible]	2-85



NOTES: UNLESS OTHERWISE SPECIFIED

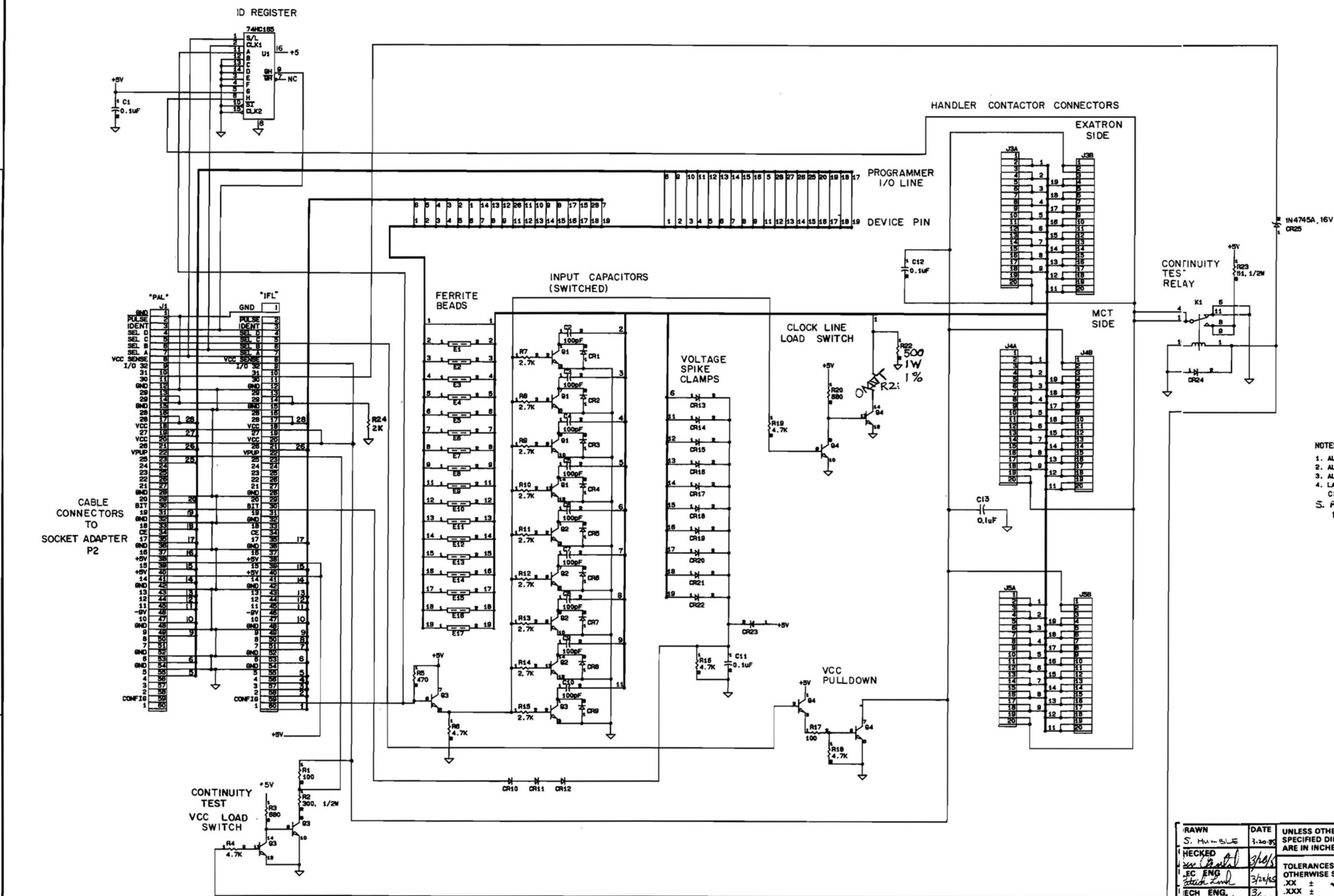
1. ALL RESISTORS ARE 1/4W 5% IN OHMS.
2. LAST REF DES USED: R2, Q2, CR4, P2, E30

P/N 701-0172-001

DRAWN M. Patten	DATE 2/85	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED Ben Patil	3/25/85	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM MODEL 60 LOGIC PROGRAMMER HANDLER ADAPTER
ELEC ENG Patrick Linh	3/28/85	DO NOT SCALE DRAWING	SIZE C; FSCM NO. 54193; DRAWING NO. 30-701-0172
MECH ENG Barry Valdivia	3/28/85		SCALE NONE; SHEET 1 OF 1
MFG ENG C Reuter	3/25/85		
QUAL ASSUR Ed Barlow	3/28/85		
APPD G. James	3/25/85		

BRUNING

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE		3/21/85	PL	3/25/85
B	INC ADCN AI PER EFP 0175	RN		KM	10/10/85



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL DIODES ARE 1N4148.
3. ALL TRANSISTORS ARE MPQ3725.
4. LAST REFERENCE DESIGNATOR USED: C13, CR25, R23, J5, K1, E17, Q4, U1.
5. REF DESIGNATORS NOT USED: R21

P/N 701-0196-002

DRAWN S. Humble	3-20-85	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED	3/20/85	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, M60H 20 PIN PERFORMANCE BD
ELEC ENG	3/25/85		
MECH ENG	3/29/85		
MFG ENG	3/25/85	DO NOT SCALE DRAWING	SIZE D FSCM NO. 54193 DRAWING NO. 30-701-0196
QUAL ASSUR	3/29/85		
APPD	3/29/85		SCALE — SHEET 1 OF 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE		[illegible]	[illegible]	3/28/85
B	INC ADCN A1 PER ECP0175	RN	[illegible]	[illegible]	4/4/85

ID REGISTER

74HC165 U1

PROGRAMMER I/O LINE

DEVICE PIN

INPUT CAPACITORS (SWITCHED)

FERRITE BEADS

VOLTAGE SPIKE CLAMPS

CLOCK LINE LOAD SWITCH

EXATRON SIDE

MCT SIDE

CONTINUITY TEST RELAY

PIN 14 CLOCK DRIVER

HANDLER CONTACTOR CONNECTORS

CABLE CONNECTORS TO SOCKET ADAPTER P2

CONTINUITY TEST VCC LOAD SWITCH

VCC PULLDOWN

BYPASS FOR U2

NOTES UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL TRANSISTORS ARE MPS3725.
3. ALL DIODES ARE 1N4148.
4. LAST REFERANCE DESIGNATOR USED: C19, CR39, J4, K1, Q6, R32, U2..
5. GND AND PWR

	GND	+5
U1	8	16
U2	7	14

6. REFERENCE DESIGNATORS NOT USED: R19

P/N 701-0197-002

DRAWN	S. Hubble	DATE	3.20.85
CHECKED	[illegible]		3/28/85
ELEC ENG	[illegible]		3/28/85
MECH ENG	[illegible]		3/28/85
MFG ENG	[illegible]		4/4/85
QUAL ASSUR	[illegible]		3/28/85
APPD	[illegible]		3/28/85

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE: SCHEMATIC DIAGRAM. M60H 24PIN PERFORMANCE BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-0197

SCALE — SHEET 1 OF 1

BRUNING 44 141

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				3/24/85
B	INCORP. ADCH A1 PER ECP 0155	SH			8/5/87

ID REGISTER

CABLE CONNECTOR TO SOCKET ADAPTER P2

FERRITE BEADS

VOLTAGE SPIKE CLAMPS

HANDLER CONTACTOR CONNECTORS

EXATRON SIDE

MCT SIDE

CONTINUITY TEST RELAY

IN4745A, 16V CR17

CONTINUITY TEST VCC LOAD SWITCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL DIODES ARE 1N4148.
3. LAST REFERENCE DESIGNATOR USED: C3, K1, J3, R8, CR17, Q1, U1.
4. UNUSED GATES:

Q1 MPQ 3725

P/N 701-0198-003

DRAWN	J. HUMBLE	DATE	3-20-85
CHECKED	Ben Cant		3/20/85
ELEC ENG	Patrick Smith		3/24/85
MECH ENG	Barry V.		3/28/85
MFG ENG	[illegible]		3/29/85
QUAL ASSUR	Ed Barnett		5/28/85
APPD	[illegible]		5/28/85

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.

TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

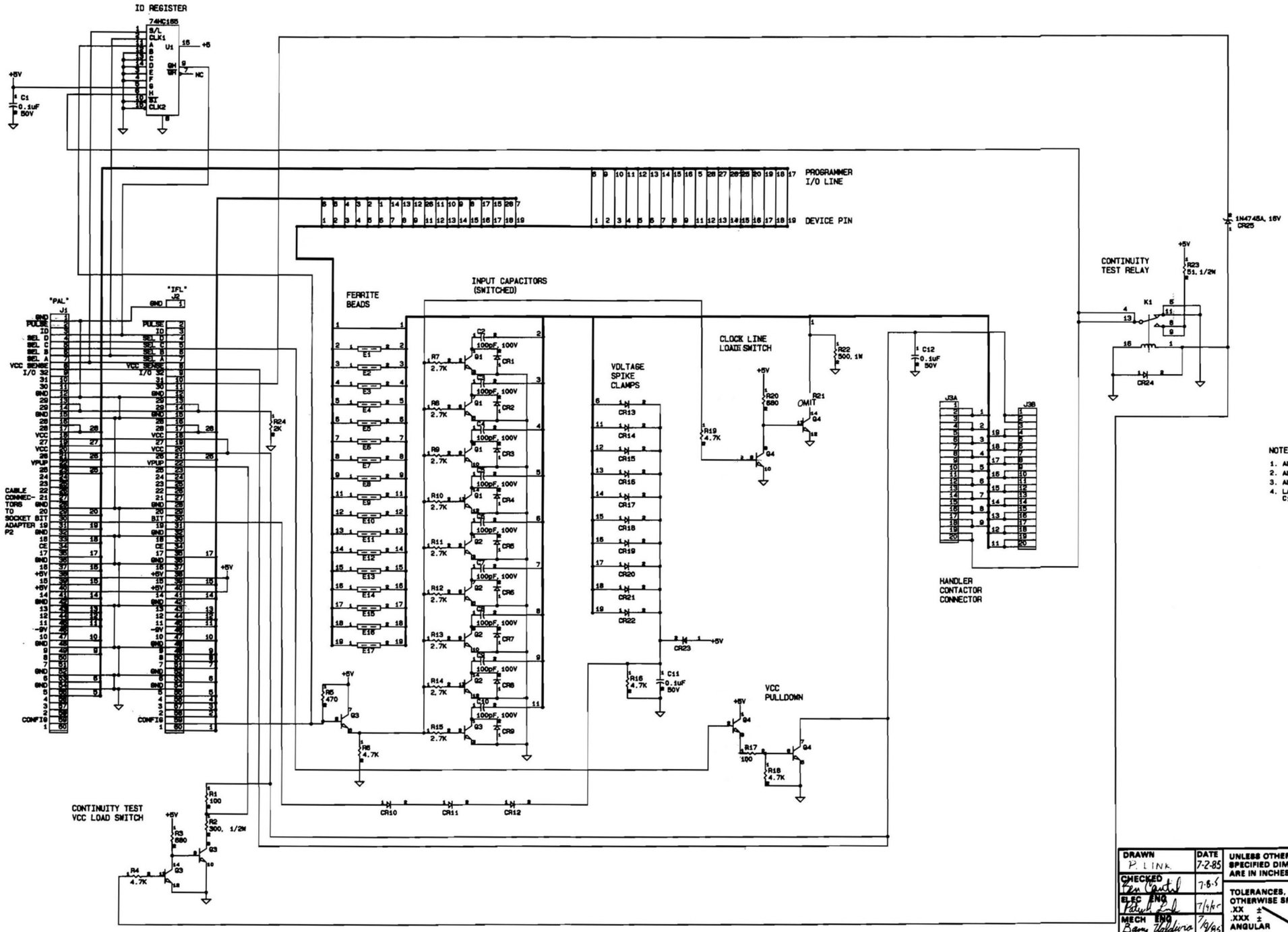
TITLE: SCHEMATIC DIAGRAM. M60H 28 PIN PERFORMANCE BD.

SIZE	FSCM NO.	DRAWING NO.
D	54193	30-701-0198

SCALE — SHEET 1 OF 1

BRUNING 44-141

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE				
B	INCA1 PER ECP 0196	JW	BV 8-2-86	GT	8/86



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL DIODES ARE 1N4148.
3. ALL TRANSISTORS ARE MPQ3725.
4. LAST REFERENCE DESIGNATOR USED: C12, CR25, R24, J3, K1, E17, Q4, U1

P/N 701-2007-002

DRAWN P. LINK	DATE 7-2-85	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED Ben Cantrell	7-8-85	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM HANDLER 300 20 PIN PERFORMANCE BOARD
ELEC ENG Peter Lee	7/9/85	DO NOT SCALE DRAWING	SIZE D · FSCM NO. 54183 · DRAWING NO. 30-701-2007
MECH ENG Barry Valdivia	7/9/85		SCALE NONE · D.A.D. · SHEET 1 OF 1
MFG ENG	7/8/85		
QUAL ASSUR Ed Bartley	7/9/85		
APPD	7/11/85		

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	[illegible]	[illegible]	[illegible]	7/9/85
B	INC A1 PER ECP0196	JW	BV 8-27-86	GS	8/86

ID REGISTER

74HC166

PROGRAMMER I/O LINE

INPUT CAPACITORS (SWITCHED)

FERRITE BEADS

VOLTAGE SPIKE CLAMPS

CLOCK LINE LOAD SWITCH

CONTINUITY TEST RELAY

HANDLER CONTACTOR CONNECTORS

PIN 14 CLOCK DRIVER

CONTINUITY TEST VCC LOAD SWITCH

VCC PULLDOWN

BYPASS FOR U2

NOTES UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL TRANSISTORS ARE MPS3725.
3. ALL DIODES ARE 1N4148.
4. LAST REFERANCE DESIGNATOR USED: C19, CR39, J4, K1, Q6, R32, U2.
5. PWR AND GND

	GND	+5
U1	8	16
U2	7	14

DRAWN P. LINK	DATE 7-2-85	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O REDMOND, WASH.
CHECKED [illegible]	7-8-85	TOLERANCES, UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM HANDLER 300 24 PIN PERFORMANCE BOARD
ELEC ENG [illegible]	7/16/85	DO NOT SCALE DRAWING	SIZE D FSCM NO. 54183 DRAWING NO. 30-701-2008
MECH ENG [illegible]	7/9/85		SCALE NONE D.A.D. SHEET 1 OF 1
MFG ENG [illegible]	7/3/85		
QUAL ASSUR Ed Barrett			
APPD [illegible]	7/16/85		

P/N 701-2008-002