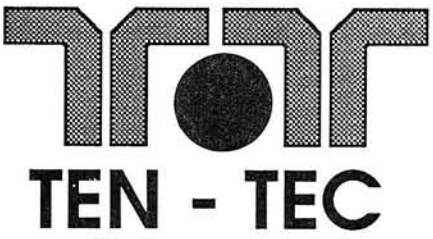

OWNER'S MANUAL

PARAGON

MODEL 585

ALL BAND HF
TRANSCEIVER

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INTRODUCTION

The PARAGON is a microprocessor controlled HF transceiver designed for the active, serious amateur. Incorporating the latest digital technology, the PARAGON features direct keypad frequency entry, dual digital VFOs, 62 memories (which store frequency, mode, VFO selection, I-F bandwidth, and a seven digit alphanumeric tag), memory scan (with channel lockout), memory tune via the main tuning knob, and all solid state design including the broadband "no tune" final power amplifier.

The PARAGON covers all amateur bands using CW (with full or semi break-in), SSB (with built-in speech processor), RTTY (true FSK or AFSK), and optional FM.

The general coverage receiver tunes from 100 kHz to 29.999 MHz and includes AM reception.

Chapters 1 and 2 of this manual cover installation and basic operation of the transceiver in order to quickly place the PARAGON into operation. Chapters 3 and 4 provide a more detailed description of the PARAGON's features, controls, and operation. Chapter 5 describes the options available for the PARAGON and how they should be installed. Chapter 6 is the technical reference section and contains detailed circuit descriptions, circuit board pictorials and schematic diagrams.

UNPACKING

Examine your Model 585 PARAGON for signs of shipping damage. Should any damage be apparent, notify the delivering carrier or dealer immediately, stating the full extent of the damage. Retain all damaged cartons. Liability for shipping damage rests with the carrier.

It is recommended that you keep the shipping carton and fillers in the event that storage, moving or reshipment becomes necessary. An accessory packet, warranty card, and manual are packed with the PARAGON. Make sure that you have not overlooked anything.

SPECIFICATIONS

GENERAL

FREQUENCY RANGE	Receive: 100 kHz to 29.9999 MHz Transmit: Standard Ham Bands 160M — 10M (Note: For operation outside Ham Bands contact factory.)
FREQUENCY CONTROL	Microprocessor controlled digital PLL synthesizer. 10 Hz resolution.
FREQUENCY READOUT	7 digit 10 Hz fluorescent readout.
FREQUENCY STABILITY	Worst case, 1 PPM per degree C. at 29.999MHz.
ANTENNA IMPEDANCE	50Ω unbalanced.
POWER REQUIRED	Receive = approx. 1.5A. Transmit = approx. 20 A. @ 13.8 VDC.
CONSTRUCTION	Rigid aluminum chassis. Extruded aluminum front panel. Textured top and bottom, snap up stainless steel bail.
DIMENSIONS	HWD 5-3/4" x 14-3/4" x 17"—14.6 x 37.4 x 43.2 cm.
NET WEIGHT	16 lbs.—7.25 kg.

TRANSMITTER

MODES	USB, LSB, CW, RTTY (FSK or AFSK), (FM optional).
DC POWER INPUT	Maximum 200 watts @ 14 VDC CW, SSB, (FM). 100% duty cycle for up to 20 minutes. Continuous with auxiliary air cooling.
RF POWER OUTPUT	25 to 100 watts adjustable with front panel RF PWR control.
MICROPHONE INPUT	High/Low impedance. Four pin, front panel connector accepts microphones with 5mV (-62 dB) output. Polarizing voltage is provided for electrets.
T/R SWITCHING	VOX or PTT on SSB. Switchable FAST or SLOW QSK on CW.
CW SIDETONE	Internally generated, adjustable tone and volume independant of AF GAIN control.
SSB GENERATION	9 MHz, 8-pole crystal ladder filter. Balanced modulator.
CARRIER SUPPRESSION	60 dB typical.
UNWANTED SIDEBAND SUPPRESSION	60 dB typical at 1.5 kHz tone.
SPURIOUS OUTPUT	More than 45 dB below peak power output.
METER	Switchable forward power, SWR, collector current, audio processing level.
CW OFFSET	750 Hz automatic.
FSK SHIFT	170 Hz.

RECEIVER

MODES — USB, LSB, CW, FSK/AFSK, AM, (FM optional).

SENSITIVITY

FREQUENCY MHz / MODE	.1 - 1.6	1.6 - 29.999	
SSB, CW, RTTY	.5 µV	.15 µV	10 db S/N @ 2.4 kHz
AM	3.5 µV	1.0 µV	10 db S/N @ 6.0 kHz
(FM)	1.0 µV	.30 µV	12 db SINAD @ 15 kHz

SELECTIVITY

SELECTIVITY / FILTER	-6 dB	-60 dB
STANDARD	2.40 kHz	3.36 kHz
AM	6.00 kHz	11.25 kHz
OPTIONAL	1.80 kHz	2.90 kHz
OPTIONAL	.50 kHz	1.40 kHz
OPTIONAL	.25 kHz	.85 kHz
(FM)	15 kHz	30 kHz

ATTENUATOR — Approx. -20 dB for 1.6 to 29.999 MHz, -10 dB for .1 to 1.6 MHz.

I-F FREQUENCIES — 1st = 75 MHz, 2nd = 9.0 MHz, 3rd = 6.3 MHz (FM 3rd = 455 kHz).

RX ANTENNA INPUT — Switchable 50Ω phono jack.

IMAGE REJECTION — > 80 dB.

I-F REJECTION — >70 dB.

NOISE BLANKER — Switchable on/off with adjustable width.

S - METER — Automatically switched on during receive. Calibrated to 50 µV at S9 .

DYNAMIC RANGE — 100 dB typical.

3 rd ORDER ICP — +18 dBm

SQUELCH SENSITIVITY — AM, CW, SSB, FSK (1.6 - 29.999 MHz) = Less than 1 µV. Optional FM (1.6 - 29.999 MHz) = Less than .4 µV.

PASS BAND TUNING — ± 1.2 kHz.

AUDIO OUTPUT — 1.5 watts @ 8Ω with less than 2% distortion.

NOTCH FILTER — 250 to 2.2 kHz, 50 dB notch typical.

AUDIO BANDPASS FILTER — 4 pole, variable center frequency 220 to 1.7 kHz, 35% bandwidth @ -6 dB. Variable fader control selects filtered or flat audio response.

TONE CONTROL — Variable 15 dB rolloff @ 5 kHz.

CHAPTER 1

INSTALLATION

1-1 INTRODUCTION When setting up the station, provide adequate ventilation for the heat sinks on the transceiver and the power supply. Do not confine the transceiver and power supply to a small volume without forced ventilation to circulate cool air around the heat sinks. Also try to select a location that allows comfortable access to the front panel controls and adequate clearance for rear panel connections.

When operating RTTY, SSTV, FM, or other high-duty modes, it is recommended that a small fan be directed on the heat sink. The sink temperature may reach as high as 200° Fahrenheit, which is still within the rating for the transistors, but certainly hot enough to cause a serious burn if touched.

1-2 FIXED STATION & MOBILE The PARAGON, with conventional antennas, will perform with distinction in any ham shack.

The PARAGON may be used for mobile operation in a car, boat, plane, or other vehicle. It operates directly from a 13.8 volt supply source and is self-contained except for key, microphone, and antenna. If desired, the Model 1140 Circuit Breaker may be installed in series with the +13.8 volt supply line. The circuit breaker will function as both an external on/off switch and an over-current protection device for the PARAGON.

NOTE: If the battery voltage drops below 12 volts, the PARAGON will not operate properly.

The SWR meter is especially useful in setting mobile whip antenna lengths to the operating frequency.

WHEN USING AN ALTERNATOR CHARGED BATTERY, **DO NOT** START AND STOP THE VEHICLE'S ENGINE WITH THE PARAGON TURNED ON. High voltage transients, caused by momentarily open regulator contacts, may cause serious damage to the transceiver circuits.

1-3 POWER SUPPLY Use a 12 to 14 VDC negative ground power source capable of delivering 22 amperes, well regulated. When powering from the Model 960 power supply, interconnect units with the cable attached to the power supply.

When other supplies or a battery are used, pin connections to the power socket are as shown in FIGURE 1-1.

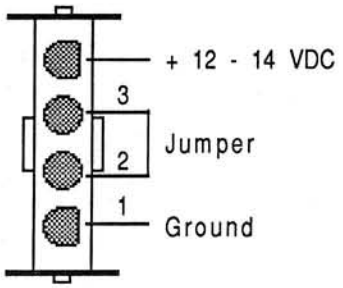


FIGURE 1-1. POWER SUPPLY CONNECTIONS

The front panel POWER switch controls a relay inside the transceiver that switches the high current 13.8 VDC to all circuits except the logic circuits. When using a TEN-TEC

power supply, a wire between pins 2 and 3 enables the primary AC circuit in the power supply when using the supplied cable. The power supply must be turned on BEFORE the PARAGON is turned on. The power supply should be left on at all times and the transceiver turned OFF and ON via the POWER switch in order to retain memories.

If making your own power cable, use number 12 or 14 gauge wire for the plus and minus (GND) leads, with the cable length as short as possible for minimum cable loss.

The PARAGON contains an internal fuse, located in the Lowpass Filter area, under the top shield. If this fuse needs replacing, be sure to use a 25 Amp. Fast Blow.

If additional protection is desired, a Model 1140 Circuit Breaker may be installed in series with the 13.8 VDC supply line.

1-4 ANTENNAS Any antenna presenting 50 to 75 Ω impedance will load satisfactorily. Random length and balanced antennas will require an antenna tuner. Most popular mobile antennas will operate at their resonant frequency without special matching. When they are used as portable antennas, a good ground system or counterpoise should be provided. The PARAGON is designed for use with an unbalanced feed system.

Although improper antennas will not damage the final output transistors, it is suggested that an SWR of 2 to 1 or less be achieved for maximum performance. In cases where the antenna cannot be matched to a better SWR, the PARAGON can be operated at reduced input power by adjusting the RF PWR control. Be sure to readjust the MIC control after reducing the RF PWR level.

1-5 MICROPHONE For SSB operation, plug a low impedance dynamic, or electret microphone into this jack. Amplified microphones can be used if the output level is adjusted to a low enough value to prevent the microphone circuit from overloading. High impedance mics (above 25KΩ) will not work.

1-6 KEY For CW operation, connect a straight key, bug, or electronic keyer to this jack. When using electronic keyers, they should be configured for positive keying, not "grid block" or negative. If configured for negative keying, no damage will occur, but the keying circuit will not operate.

1-7 GROUND In the interest of personal safety and to reduce the possibility of stray RF pickup on interconnecting cables which may cause parasitic oscillations, all station equipment should be well grounded to earth. It is also important to strap all equipment chassis together with short, heavy leads. The strap between the power supply and the transceiver also serves to reduce the voltage drop on the negative lead caused by wire and connector resistance. In mobile installations, connect a ground strap between the rear panel ground lug and the automobile chassis.

1-8 BATTERY BACKUP As long as the PARAGON is connected to a source of 13.8 VDC, the microprocessor and memory RAM circuits will retain all memories, last frequency used, and date & clock information. The front panel POWER switch does not remove power to the logic circuits.

To prevent loss of memory during power failures or while transporting the PARAGON, a backup battery (9 volt alkaline or Ni-Cad) can be installed in the PARAGON.

Refer to PARAGRAPH 5-1.1 for information on removing the top cover. Located in the center of the chassis is the battery holder. A battery clip is included in the packing kit shipped with the PARAGON. With the POWER switch in the ON position, and the PARAGON operating, install the battery in the holder and plug the battery cable into the +9V connector located on the left rear corner of the

large Logic Board. To verify correct installation, turn off the POWER switch and remove the power supply cable. After waiting a minute or two, reconnect the power supply and turn the POWER switch back on. The PARAGON should power up on the same frequency that it was on when you removed power and the clock should not have lost any time. If everything is correct, replace the top cover.

An alkaline battery will provide approximately 150 hours of backup if power is removed, otherwise the battery will last for it's shelf life. If the transceiver is not to be used for long periods of time, it is recommended that the battery be removed to prevent possible corro sion. When using a 9 volt Ni-Cad battery, the power supply should be turned on at least three to four hours per week to keep the battery trickle charged.

CHAPTER 2

CONDENSED OPERATING INSTRUCTIONS

2-1 INTRODUCTION The following instructions will enable the operator to quickly place the PARAGON into operation. Refer to CHAPTER 3 of this manual for more detailed descriptions of the controls and unique functions of the PARAGON.

Refer to CHAPTER 1 for information on connecting power supply, microphone, antenna, and other accessories.

2-2 SELECTING FREQUENCY There are two ways to select frequency, via the keypad and using the main tuning knob. With the keypad, the MHz portion of the frequency is entered first followed by the decimal point. If the frequency is less than 1 MHz, the decimal point is entered first.

After the decimal point, the remaining kHz portion of the frequency is entered and the transceiver will change to the new frequency by pressing the [ENTER] key. Zeros at the end of the frequency, if no more numerals are to follow, do not need to be entered. For whole MHz frequencies, you can simply enter the first one or two digits and then press [ENTER]. The following are examples of different frequencies and how to enter them. If an error is made during the entry procedure, press the [CLEAR] key, and repeat the entry.

Examples:

14.275 MHz:

[1] [4] [.] [2] [7] [5] [ENTER]

21.0 MHz:

[2] [1] [ENTER]

950 kHz:

[.] [9] [5] [ENTER]

2-3 INITIAL FRONT PANEL SETTINGS
Set the front panel controls as follows:

KEYPAD:

Select Mode, press CW,USB or LSB.
Select VFO A, press A/B until annunciator in display indicates "VFO A".
Select 2.4 kHz Bandwidth, press [2.4].

AF ---------- Adjust to suitable audio level
TONE --------- Midway
FADE --------- Max counter-clockwise
BP ---------- Max counter-clockwise
PBT---------- Midway
NOTCH------- Max counter-clockwise
MIC ---------- Max counter-clockwise
RF PWR ------ Max counter-clockwise
RF ---------- Max clockwise
SQL ---------- Max counter-clockwise
METER ------- FWD
NB ---------- OFF
VOX/PTT ---- PTT
QSK ---------- FAST
AGC---------- ON & SLOW
ATTN --------- OFF
PROC --------- OFF

2-4 TRANSMIT

CW --- Press TUNE key on keypad and adjust RF PWR control for desired output power as observed on meter. Press TUNE key again to return to transceive mode.

SSB --- Adjust RF PWR control as described above, then, using PTT, adjust MIC control until ALC LED just lights on voice peaks.

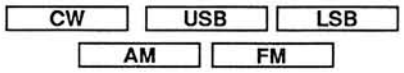
CHAPTER 3

DETAILED OPERATING INSTRUCTIONS

3-1 KEYPAD FUNCTIONS The keypad is used to enter frequency, to select VFO's, Mode, Bandwidth, alphanumeric tag, and to access microprocessor controlled functions. When a key is pressed, a "beep" will be heard from the speaker, indicating key closure. The beep level can be adjusted with the rear panel BEEP/VOICE control.

Some of the keys have two functions with the top functions accessed via the SHIFT key. After completing a multi-key function a double beep will be heard.

3-1.1 SELECTING MODE



Mode selection on the PARAGON is accomplished by pressing the desired mode key on the keypad. The corresponding LED will light indicating the chosen mode. When selecting AM, LSB, or USB modes, a typical crystal filter selection of either 6.0 or 2.4 kHz will automatically be chosen. This can be changed by pressing a different Filter key. See PARAGRAPH 4-1.3 for RTTY operation.

3-1.2 CRYSTAL FILTER SELECTION

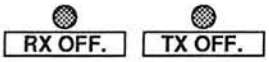
These keys select the desired IF bandwidth. In the standard configuration, the 6.0 and 2.4 kHz filters are installed. Optional filters may be installed for 1.8, .5, and .25 kHz. LEDs above the keys indicate the selected bandwidth.

Bandwidth selection is independant of the mode selected except in the optional FM mode. The IF bandwidth is automatically 15 kHz when this mode is selected.

3-1.3 TUNE

This key is used to place the transceiver in the transmit mode, or "key down". It is used when adjusting power output, and for system checks and SWR measurements. Pressing this key a second time returns the transceiver to the receive mode. NOTE: If TUNE is pressed when the transmit frequency is outside the ham bands, nothing will happen.

3-1.4 RECEIVE & TRANSMIT OFFSET



This function allows independent control of the receive and/or transmit frequencies with a range of ± 99.9 kHz. LEDs above the keys indicate the selected function, the OFF. annunciator lights, and the fluorescent display shows the frequency deviation ± in kHz.

In the RX OFFset mode, received stations may be "zeroed in" without affecting the transmit frequency. TX OFFset may be used, for example, to answer a station calling CQ and "listening 2 kHz up".

Only one OFFset function can be used at a time. Pressing the key a second time disables the selected offset function.

3-1.5 DISPLAY

DISP ➤

This key selects the time, date,or tag shown on the fluorescent display. Each time the key is pressed the display will toggle from DATE to TIME to TAG and the annunciators above the display will show the selection.

3-1.6 VOICE

VOICE

This key is used to activate the optional Model 257 Voice Readout.

3-1.7 SPOT

SPOT

This function, which is designed primarily for use in CW mode, allows the operator to listen to the frequency that he is transmitting on. Using this function, the transmitter frequency can be tuned to the incoming received signal by zero-beating with that signal. This is a momentary function and the transceiver will return to the previous receive frequency when the key is released. For best results, select a wide bandwidth filter when using this function.

3-1.8 VFO SELECTION

A = B A / B

These keys control the operation of the two VFOs. The A/B key toggles between VFO A & VFO B with the annunciators above the display indicating the selected VFO. When the A=B key is pressed, the frequency of the selected (and displayed) VFO is placed in the other undisplayed VFO.

SPLIT

The SPLIT key allows the receive and transmit frequencies to be assigned to each VFO. An annunciator above the display indicates that this function is enabled.

To receive on VFO A and transmit on VFO B, select VFO B with the A / B key and select the desired transmit frequency, then select VFO A and select the desired receive frequency. Then press the SPLIT key.

To transmit on VFO A and receive on VFO B, select VFO A and select the transmit frequency. Select VFO B and select the receive frequency, then press the SPLIT key.

Pressing the SPLIT key a second time disables this function. NOTE: When tuning with the SPLIT mode on, only the displayed VFO is changed!

3-1.9 TUNING RATES

FAST

The FAST key,with LED indicator, selects the tuning rate and resolution of the main tuning knob according to the following table.

	Normal	Normal Shifted
CW/USB/LSB/FSK	10 Hz	20 Hz
AM/FM	50 Hz	100 Hz
	Fast	**Fast Shifted**
CW/USB/LSB/FSK	20 Hz	50 Hz
AM/FM	100 Hz	500 Hz

TABLE 3-1. TUNING RATES

In addition, the tuning knob has a speed shift feature which increases the tuning rate automatically when the knob is spun at a fast rate.

3-1.10 TEN Hz DISPLAY

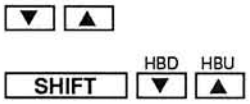
SHIFT 10 Hz MT

To display the 10 Hz digit of the frequency, press the SHIFT key followed by the MT key. Pressing theSHIFT and MT keys again will extinguish the 10 Hz digit.

3-1.11 TUNING KNOB LOCK

This key and its associated LED is used to lock out the main tuning knob to prevent accidental frequency change. All keyboard functions remain active.

3-1.12 DOWN / UP



These keys are used to quickly move up or down in either 100 kHz or 1 MHz steps. When the FAST tuning function is Off, the step size is 100 kHz. When the FAST tuning is On, the step size is 1 MHz.

When used with the SHIFT key, these keys are used to move up or down to the next amateur band. When the HBD or HBU key is held in there will be a short pause after which the ham bands will rapidly increment or decrement until the key is released.

3-2 MEMORIES

The PARAGON has 62 memory channels (00 to 61) which may be used to store favorite or often used frequencies. Each memory stores frequency, VFO in use, mode, filter selected, and the alphanumeric tag. Memory 00 also supplies the default tag (for example, your call) whenever the TAG is displayed but no memory has been selected.

Whenever a memory function is selected, the MEM annunciator will light.

3-2.1 MEMORY STORE

STO

Example: STO 1 4

To store information in a memory channel, first make sure that the frequency, mode, VFO, and filter selection are correct. Then press the STO key and the desired 2 digit memory channel number. The fluorescent display will show the memory channel selected. The STO function will NOT save the diplayed tag but instead will fill the TAG with blanks. To change the TAG see following instructions for TAG.

STO ENTER

A quick way of storing a memory without having to specify a channel number is to use the STO/ENTER method. The transceiver will automatically choose the next available memory channel. To use this function, press the STO key and then the ENTER key. The display will show the memory number used or if all the memory channels are full, the display will show "FULL".

3-2.2 MEMORY RECALL

RCL

To recall a memory channel,press the RCL key and then the desired 2 digit memory channel number. The display will show the recalled memory. If the tuning knob is adjusted or a frequency entered via the keypad, the transceiver will return to the non-memory mode.

RCL ENTER

To recall the last memory channel stored using STO/ENTER, press the RCL key and then the ENTER key.

3-2.3 TAG

Example: K4FW

The alphanumeric tag can store up to 7 characters of letters and/or numerals. To enter a tag into the display, select the TAG display using

the DISPlay key. Then press ENTER and the display will prompt you with underscores for each character position (_ _ _ _ _ _). Enter the numbers or letters located beneath the other keys on the keypad. If 7 characters are entered, the keypad returns to normal upon completion of the last digit. If less than 7 characters are entered, press theENTER key to complete the process.

If a memory has been recalled and the MEM indicator is on, the tag just entered will be stored automatically in the displayed memory channel. If the MEM indicator is initially off, it will be turned on and you will be prompted to enter the memory channel that the new tag should be stored in. If you enter a memory channel that is empty, the current Frequency, Mode, VFO and Filter information will also be automatically stored in that memory along with the tag. To exit the TAG entry mode at any time press the CLEAR key.

If the tuning knob is adjusted, this part of the display automatically returns to the Default TAG (filled with blanks) or the tag which has been stored in memory channel 00. Using this technique, you can set the Default TAG to be anything you want (your call sign, name, etc.).

3-2.4 MEMORY TUNE

[MT]

When this function is used, the main tuning knob will no longer tune the VFO but will tune through all of the programmed memories, including those that are locked out. The display will show a "T" to the right of the channel number indicating Memory Tune mode.

A locked location will display an "L" (Locked) in front of the memory number. Thus the Memory Tune function also provides a means of determining which memory locations are locked out when using memory scan.

3-2.5 SCRATCH PAD MEMORY

[STO] [STO]

[RCL] [RCL]

The scratch pad memory can be used to temporarily store and recall a single frequency without affecting the main memory locations. All of the information that is stored using the STO method is also stored in the Scratch Pad Memory. With the desired information selected, press the STO key twice. The display will show "SP" indicating that the displayed frequency is in scratch pad memory. The scratch pad memory may be recalled at any time by pressing the RCL key twice.

Each time a new frequency is entered into the scratch pad memory, the previous memorized frequency is erased.

3-2.6 MEMORY SCAN

[MS]

To use the memory scan mode press the MS key. The microprocessor will then scan through all of the programmed memories (except those that are locked out) stopping at each location for a period of time. The scan rate will be determined by the value selected using the RATE function (explained in PARAGRAPH 3-2.7).

To temporarily stop the scan function, press and HOLD the [ENTER] key until scanning stops, then to resume scan press [▼] or [▲] . The receiver will then resume scanning in the direction chosen by the keys. To exit the scan mode press the CLEAR key.

NOTE: In order to use Memory Scan, there must be more than 1 memory channel programmed and/or unlocked. If memory scan is attempted under these conditions the transceiver will appear to be malfunctioning as the keypad and main tuning knob will not respond. Pressing the CLEAR key will return the transceiver to normal.

3-2.7 RATE

SHIFT + RATE (MS)

The scan RATE is used in the memory scan mode and determines the speed or RATE at which the memory locations are scanned. To program the scan rate press the SHIFT and then the RATE keys. The word RATE and a number from 0 to 9 will appear in the display indicating the scan rate with 9 being the fastest. Press the UP/DOWN keys to select the desired rate and then press the ENTER key.

3-2.8 MEMORY LOCKOUT

ML

The Memory Lockout function causes selected memory locations to be bypassed during Memory Scan. The information in the locked out channel is retained and may be unlocked at any time. To lock out a location, recall the location to be locked out using either the RCL or the MT functions, and press the ML key. If the location to be locked out is already in the display, the recall procedure may be omitted. Then the location may be locked out by just pressing the ML key. If the locked out location is recalled or tuned via Memory Tune, the display will show "L" to the left of the memory channel number indicating that the location is locked out.

3-2.9 MEMORY LOCK CLEAR

MLC

The Memory Lock Clear key is used to unlock a selected memory location. This memory can be selected by using either the MEMORY RECALL function or by using the MEMORY TUNE function.

3-2.10 GLOBAL LOCKOUT

SHIFT + GL (STO)

TheGlobal Lockout key is used to lock out all of the memory locations. This is useful if you have a lot of programmed memories but only wish to listen to a few select memories by using the Memory Lock Clear key described above.

3-2.11 GLOBAL LOCK CLEAR

SHIFT + GLC (RCL)

The Global Lock Clear key is used to unlock all of the locked out memory locations.

3-2.12 MEMORY CLEAR

SHIFT + MC (ML)

This key will clear the currently displayed memory channel, returning it to an unprogrammed state. To select the desired memory you must first use the MEMORY RECALL or MEMORY TUNE functions. MEMORY CLEAR will only clear a recalled memory location. If you wish to clear all memories the best way is to press the RESET switch on the right side of the transceiver.

3-3 CLOCK-CALENDAR & SYSTEM FUNCTIONS The PARAGON has a built-in 24 hour, crystal controlled clock and calendar circuit. As long as power is supplied by the power supply or the internal 9 volt back-up battery (if installed), the clock will keep accurate time. The procedures for setting the clock and date functions are descibed below.

3-3.1 SET

SHIFT + SET (MLC)

The SET key is used to set the 24 hour clock and date.

3-3.2 CLOCK SET

DISP ➤ (until TIME is displayed)

SHIFT + SET (MLC)

To set the time in the 24 hour clock, first press the DISP key until TIME is displayed. Next press the SHIFT key, then the SET key and you will be prompted by four underscores for the time entry. Enter the hours and minutes digits as desired. If you enter less than four digits you must press the ENTER key again to exit the SET routine. When you exit via the ENTER key, all unfilled digits will be cleared to zero. The clock will begin running again upon pressing the ENTER key or entering the last of the four digits.

3-3.3 DATE SET

DISP ➤ (until DATE is displayed)

SHIFT SET MLC

To set the date, first press the DISP key until DATE is displayed. Then press the SHIFT key followed by the SET key and the day of the month will be blanked, leaving only the month. Use the UP or DOWN arrow keys to select the correct month, then press ENTER. Now only the day of the month will be displayed. Again use the UP or DOWN arrow keys to select the correct day. When you are finished press the ENTER key.

3-3.4 SYSTEM VERSION NUMBER

SHIFT ENTER

The instructions for the PARAGON microprocessor are contained in an EPROM. Because of this design, updates, improvements and new features may readily be implemented by simply changing the software. By pressing the SHIFT key and then holding down the ENTER key, the TAG display will show the version number for the software in your system. (EXAMPLE: VER 3-2)

3-3.5 SYSTEM RESET SWITCH The RESET switch is accessible through a hole located on the right side of the PARAGON. This switch is connected to the microprocessor and will cause a system reset when pressed. If the PARAGON ever malfunctions and the keypad and/or tuning knob no longer operate properly, pressing the RESET switch will usually correct the problem. **NOTE: Pressing the RESET switch will clear ALL MEMORIES and will also clear the clock and date information.**

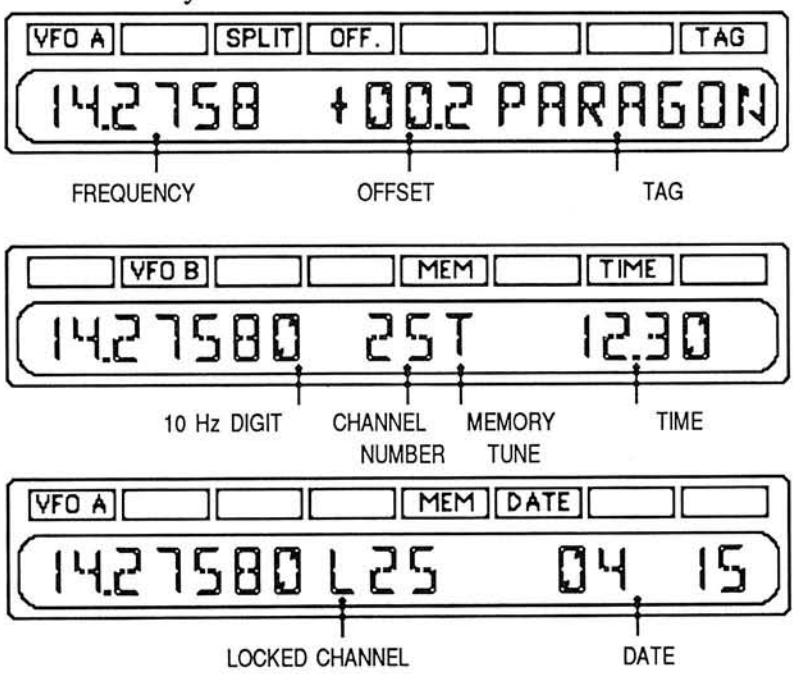


FIGURE 3-1. FRONT PANEL DISPLAY

3-4 FRONT PANEL FUNCTIONS The following sections describe the front panel displays and the controls which are not located on the keypad. Refer to FIGURE 3-3 to help locate each control.

3-4.1 DISPLAY AREA As shown in FIGURE 3-1, the vacuum fluorescent display shows the frequency, Rx/Tx Offset, memory status, the date, time, or tag, and other microprocessor controlled functions. The eight annunciators above show the VFO selection, OFFset or MEMory selection, and the DATE, TIME, or TAG selection.

3-4.2 AF GAIN/TONE The AF GAIN control varies the audio output of the transceiver. The TONE control is a low pass type with a rolloff of approximately 15 dB at 5 kHz.

3-4.3 METER & SWITCH In receive mode the meter will automatically read S units when the meter switch is in any position. The S meter will be accurate only when the RF control is fully clockwise. The meter is factory calibrated for a reading of S9 at 50 μV when operating at 15 MHz.

When transmitting, the meter indicates the following:

IC position measures the current drawn by the final amplifier module. Use the scale marked 0 to 20 amperes.

SWR position provides a reading of power reflected from the antenna. When the forward power is 100 watts, the standing wave ratio can be read from the scale marked SWR.

FWD position measures forward power to the antenna. Use the FWD scale marked 0 to 100 watts.

To determine SWR, place meter switch in FWD position, press TUNE and adjust RF PWR control for a reading of 100 watts. Then switch the meter switch to REF and use the scale marked SWR. Press the TUNE key again to return to transceive mode.

PROCESS position displays the level of compression applied to the MIC input when the PROCess control is turned on.

3-4.4 NOISE BLANKER The N.B. switch turns on the blanker circuit. The WIDTH control varies the blanking pulse width.

3-4.5 ATTENUATOR To reduce susceptability to receiver overload in the presence of extremely strong signals, the ATTN switch removes the front end RF amplifier from the receiver circuitry. The effect is a 20 dB reduction in signal level to the first mixer but with more dynamic range and greater sensitivity than would be the case with a simple attenuator. The LED below the switch indicates that the attenuator has been selected.

3-4.6 BPF / FADE This control fades from normally flat audio response to a bandpass filter variable from 220 to 1700 Hz with the BPF control. Various amounts of bandpass effect can be chosen by the degree of clockwise rotation. The filter width is 35% of the selected center frequency at the -6 dB points.

3-4.7 PBT / NOTCH The PBT control adjusts the position of the PBT IF crystal filter in relation to the fixed second IF filter. When the selected filter is wide, i.e. 2.4 or 1.8 kHz, the PBT control essentially becomes a variable bandwidth control. Counter-clockwise rotation shifts the passband towards the low side of the signal when in USB mode, clockwise rotation shifts the passband toward the high side of the signal. When in LSB mode, the above directions are reversed.

The PBT circuit in the PARAGON produces the effect of varying the frequency response of signals passing through the narrow filter, which enables you to separate signals which are close together. On RTTY it can place the narrow filter to pass only the 2295 and 2125 Hz tones for superior rejection of

adjacent signals. The PBT has no effect on the transmitter frequency or bandwidth.

The NOTCH control adjusts the center frequency of the audio notch across the passband. The notch depth is at least 40 dB and will reduce carrier interference by this amount or more. To use the NOTCH, rotate the control slowly until the unwanted signal is reduced. The notch circuit is effectively removed by turning the control fully counter-clockwise.

3-4.8 MIC / RF PWR The RF PWR control varies the amount of power output for all modes. This allows you to set your output power to any value from 25 to 100 Watts. The MIC control varies the amount of audio applied to the transmit balanced modulator.

To set these controls, place the METER switch in the FWD power position and place the transceiver in transmit using the TUNE function. Advance the RF PWR control to the desired power level. The CW level is now set. For SSB operation, continue by placing the transceiver in either the USB or LSB mode and while speaking into the microphone in a normal voice, advance the MIC control until the ALC LED lights on voice peaks. NOTE: The ALC LED will light at all RF PWR settings when operating in CW or TUNE modes.

Increasing the MIC setting over that required to just light the ALC LED will not result in any appreciable increase in power out. However, overdrive will produce SSB, AFSK, or SSTV distortion products.

The PARAGON uses a "current-limit" protection system where the drive level is automatically reduced to prevent the final transistors from drawing more than 20 amperes. If full power output can not be obtained, it is an indication that the antenna is not presenting a 50 Ω impedance. Refer to PARAGRAPH 4-1.4 for more information.

3-4.9 PROC The PROCess switch and control activates the speech processor and determines the processing level. The processor increases the average speech power and allows a greater range of voice levels to attain peak ALC level. An LED below the switch indicates when the processor has been selected.

The processing level will affect the MIC control to some extent. To set the processor, turn it off and adjust the RF PWR and MIC as described above. Turn the PROCess switch on and advance the control until the meter needle moves into the center of the black band (on the PROC scale) on voice peaks. More processing is available by further clockwise rotation of the control, but the MIC control must be reduced to keep the ALC action constant.

Severe distortion, objectionable background noise, and transmitted splatter will occur if the MIC control is not adjusted so that the ALC LED just lights on voice peaks. The processed audio may be monitored to prevent this distortion by using the MONITOR control on the rear panel. The use of headphones is recommended to prevent feedback from the speaker. See PARAGRAPH 3-5.7.

3-4.10 RF / SQL The RF gain control varies the gain of the I-F stages. The AGC is dependent on the setting of this control and therefore the S meter is calibrated only when the RF gain control is fully clockwise.

The SQL control sets the squelch threshold level. The squelch level is determined by the AGC circuits. To adjust the squelch, rotate the control clockwise until the received audio becomes quiet. To turn the squelch function off, rotate the control fully counter-clockwise.

3-4.11 AGC FAST / SLOW & ON / OFF These switches control the automatic gain control (AGC) system. In the FAST position, the recovery time of the AGC system is approximately .2 seconds and in the SLOW position approximately 2 seconds.

The ON/OFF switch defeats the AGC

system. When the AGC is turned OFF, the IF gain is controlled by the RF gain control and the S meter is inoperative.

It is sometimes useful, when extreme QRM is present, to turn the AGC off and control the audio volume with the RF gain control.

3-4.12 VOX/PTT This switch selects either the internal VOX (voice operated transmit) or manual PTT (push-to-talk) circuitry.

3-4.13 QSK FAST / SLOW The QSK switch controls the recovery time of the receiver after transmitting. Place in the FAST position for cw full break-in.

3-4.14 PWR This switch controls the main power to the transceiver via an internal relay which switches the high current 13.8 VDC. Power is connected to the logic circuits at all times.

3-4.15 PHONES This jack is designed to be used with a standard 1/4" plug. Headphones with an impedance of 4 to 16 ohms are recommended. Both the internal speaker and external speaker jacks are disabled when headphones are plugged in. The AF OUT jack is not affected by using the PHONES jack.

3-4.16 MIC The microphone circuit has been designed for high or low impedance microphones with a minimum 5 mV output. Transistorized microphones may also be used, providing their output level is adjusted so that the input stages are not overdriven. The cable, which preferably should provide shielding for all leads, is terminated with a standard 4 pin microphone plug. Failure to shield both microphone and PTT leads may result in RF getting into the audio circuits. Connections to the plug are as shown below in FIGURE 3-2.

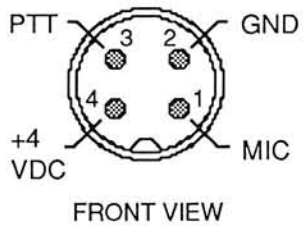


FIGURE 3-2. MIC CONNECTIONS

FIGURE 3-3. MODEL 585 FRONT PANEL

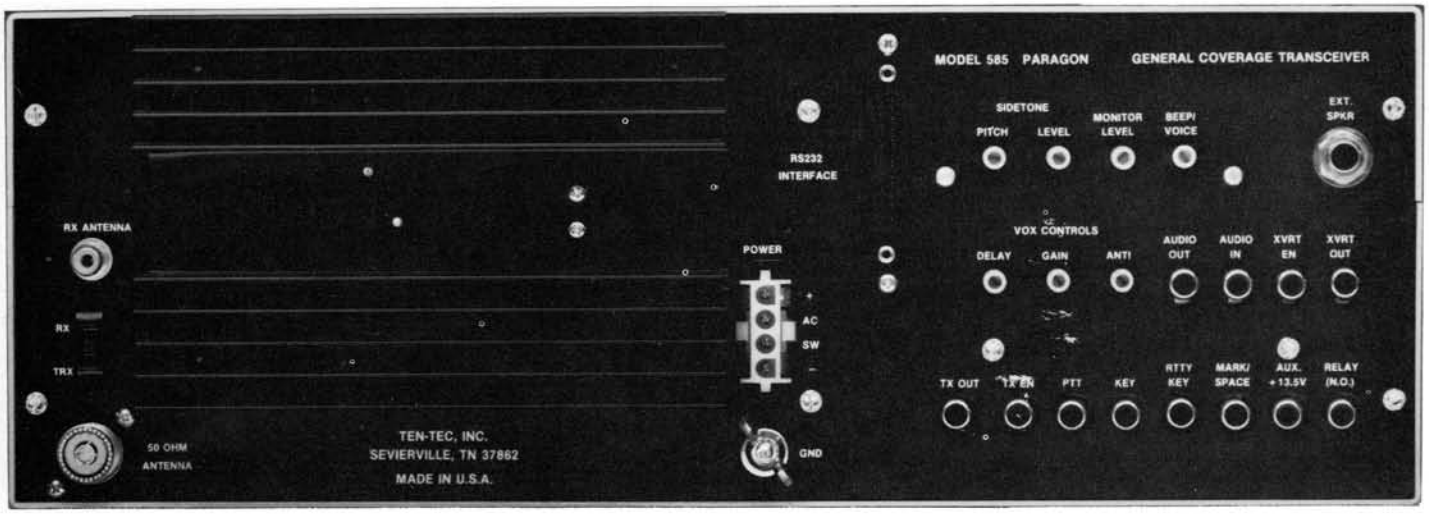


FIGURE 3-4. MODEL 585 REAR PANEL

3-5 REAR PANEL FUNCTIONS The following sections describe the rear panel connectors and controls. Refer to FIGURE 3-4 for the location of each connector or control.

3-5.1 POWER SOCKET This connector is used for the main DC power to the transceiver and for switching the power supply output on and off. Reverse polarity protection is provided via an internal reverse-biased diode and 25 ampere fast blow fuse.

Refer to PARAGRAPH 1-3 for connection details.

3-5.2 GROUND POST Used for the primary transceiver ground. To prevent personal injury, interference and other ground related problems, connect this terminal to a good earth ground using heavy gauge copper braid or wire and make the connection as short as possible.

3-5.3 ANTENNA This connector mates with the standard PL-259 plug for 50Ω coaxial antenna or external linear amplifier connections.

3-5.4 RECEIVE ANTENNA This jack provides a connection directly to the receiver front end at all times. When the RX-TRX switch is in the RX position, the SO-239 Antenna connector is disconnected from the receiver, and a receive-only antenna may be connected to the RX ANTENNA jack. This also permits use of a secondary receiver when the switch is placed in the TRX position and the secondary receiver antenna input is connected to the jack.

3-5.5 CW SIDETONE The LEVEL and PITCH controls adjust the internally generated sidetone during cw transmit. Adjust for desired volume and pitch.

3-5.6 VOX CONTROLS The rear panel GAIN, DELAY, and ANTI VOX controls can be adjusted to suit the individual operator's needs. To adjust, proceed as follows:

1) Adjust the front panel AF GAIN control to a comfortable level.
2) While speaking into the mic at normal level, adjust the GAIN for reliable VOX action.
3) Adjust the DELAY so that T/R switching does not occur between words when speaking into the microphone.
4) Set the ANTI VOX to the point where receiver audio does not trip the VOX circuit at moderate volumes.

3-5.7 SSB MONITOR LEVEL This control permits monitoring the SSB transmit audio thru the audio amplifier circuit of the transceiver. It is useful when adjusting the internal speech processor so that the processed audio has not been adjusted to the point where severe distortion occurs. Also, it is useful for checking AFSK and SSTV signals. Headphone use is recommended when using the SSB Monitor function to prevent feedback from speaker to microphone. During normal SSB operation this control should be left in the full counter-clockwise position.

3-5.8 BEEP / VOICE This control is used to set the level of the keypad "beep" and optional voice outputs. You can turn it off by rotating the control fully counter-clockwise.

3-5.9 KEY The transmitter can be keyed by a ground connection to the high impedance KEY input when the CW mode is selected. This line is compatible with open collector (positive) keyer outputs as well as bugs and straight keys. When the key is closed the antenna is electronically disconnected from the receiver and the receiver stages are disabled.

3-5.10 XVRT EN / XVRT OUT These jacks can be used in conjunction with an exter-

nal transverter for VHF/UHF operation. A closure to ground on the XVRT ENable jack switches the low level transmit carrier (approximately 0 dBm) to the rear panel XVRT OUT jack and disables the PARAGON final output amplifier.

The transverter receive output can be connected to the Receive Antenna jack described above.

3-5.11 AF OUT This jack provides a line level receiver audio output for use with an external RTTY demodulator or tape recorder. Level is not affected by the front panel AF gain control.

3-5.12 TX EN / TX OUT The TX ENable/ TX OUT jacks provide a keying loop for use with some types of external linear amplifiers. For normal operation these jacks are jumpered together. For more information refer to FIGURE 5-7 which shows the connections required for use with the TITAN amplifier.

TX ENable: A closure to ground places the transceiver into transmit mode regardless of mode selected.

TX OUT: Provides a closure to ground thru an open collector transistor to ground whenever the PARAGON is in transmit mode.

3-5.13 PTT This jack is in parallel with the push-to-talk line on the microphone front panel jack. It may be used with an external transmit/receive station switch, foot switch, etc. A closure to ground places the transceiver in transmit mode only in USB, LSB and FM modes.

3-5.14 AUX 13.8 This jack provides 13.8 VDC@ 2 amperes and may be used to power external equipment such as an electronic keyer. The AC power supply used to power the PARAGON must have enough current capacity to power both the transceiver and any accessories conected to the AUX 13.8 jack.

3-5.15 AUDIO IN Low level audio signals (500mV max.) such as an AFSK input, phone patch, etc. can be mixed together into the mic channel through this input. Typical input impedance is 2.2 KΩ.

Caution: Some AFSK equipment will output a signal even when not activated. If this signal is left connected to the AUDIO IN jack, it can interfer with normal SSB operation.

3-5.16 EXT. SPKR A standard 1/4" phone jack for connecting an external speaker. The internal speaker is disconnected whenever this jack is used. Any 4 to 16 ohm speaker may be used.

3-5.17 RELAY This jack provides a normally open relay contact which switches to ground during transmit. Since one side of this connector is grounded, DO NOT use it to switch AC lines.

When operating cw, a drop-out delay is incorporated in the relay circuit. The delay time is factory set to an average value and may be adjusted via a small trimmer poteniometer on the Control Board, located under the cover on the bottom side of the transceiver. There is no delay in the other modes. Setting this control for a longer delay will help reduce the noise caused by the relay during CW keying.

3-5.18 RTTY KEY This jack is in parallel with the KEY jack and can be used to control the PARAGON during RTTY operation. A closure to ground places the transceiver in transmit mode.

3-5.19 MARK / SPACE This is the input for RTTY keying. The RTTY MARK level can be 0 to -15 Vdc. The SPACE should be between +2.5 Vdc and +15 Vdc.

CHAPTER 4

OPERATING HINTS

4-1 INTRODUCTION The following paragraphs provide additional useful information for getting the best performance out of your PARAGON. Also included is TABLE 4-1, which provides trouble-shooting information if you should ever have a problem.

4-1.1 CW In the CW mode, the indicated frequency is the received frequency. To accurately read an incoming signal, therefore, it is necessary to "zero-beat" the signal, not peak it on the S meter. This holds true no matter where the OFFSET controls are set.

When transmitting cw, the actual transmitted frequency is 750 Hz higher than the displayed receive frequency. This is due to the BFO shift necessary to bring the oscillator into the filter passband. To accurately determine the transmitted frequency, add 750 Hz to the receive frequency, or if SPLIT VFO's are used, add 750 Hz to the programmed transmit frequency.

4-1.2 FM The PARAGON will operate transceive ± 5 kHz deviation FM with the optional Model 256 FM Adaptor.

The PBT, Crystal Filter selection keys, Noise Blanker, QSK and AGC switches do not function in this mode.

If split Rx / Tx is desired when operating thru repeaters, program the transmit and receive frequencies in VFO A and VFO B.

Set the MIC control midway, internal limiting circuitry prevents over-deviation in the FM mode, assuming that the microphone used has an output of 5 mV or less.

4-1.3 FSK (RTTY)

SHIFT CW

To enable the FSK mode, press the SHIFT key, then the CW key. All mode LED indicators will go out indicating this mode selection.

Required external equipment are a teletypewriter or keyboard and a demodulator (terminal unit) designed for 170 Hz shift with 2125/2295 Hz tones. Audio for the demodulator may be taken from the AF OUT jack on the rear panel.

The FSK keying should be connected to the MARK / SPACE jack (MARK: 0 to -15Vdc, SPACE: +2.5 to +15 Vdc) and a seperate T/R function is provided on the RTTY KEY jack (ground to transmit).

AFSK operation is also possible by using the AUDIO IN jack on the rear panel or the MIC connector on the front panel.

4-1.4 PROTECTIVE CIRCUITRY & ALC ALC serves three major functions: assures maximum power from the transmitter without critical adjustment of the input drive, prevents the amplifier from being overdriven into the non-linear, distortion-producing area, and serves as a power limiting device which protects the output transistors. It does the first two very well, but the third only partially. To protect the system, the PARAGON uses current limiting circuitry which automatically reduces the drive level if the current demand is

greater than 20 amperes. As an extra measure of protection, the TEN-TEC Model 960 power supply (or the Model 1140 magnetic circuit breaker) has a trip-out feature that prevents currents in excess of 20 amperes.

If the ALC LED lights at power outputs less than 100W, this is an indication that the current limiting circuits are reducing drive. This also occurs if the RF PWR control is turned down. Although the PARAGON will operate satisfactorily under these conditions, an improvement in the antenna system or matching network will provide maximum efficiency.

4-1.5 SOLID-STATE POWER AMPLIFIERS Although transistors and vacuum tubes both can be made to amplify RF power, there are some fundamental differences in how this is accomplished. A better understanding will aid in recognizing correct or incorrect performance.

Misconceptions sometimes arise from incomplete knowledge which results in erroneous conclusions being drawn that the equipment is faulty, erratic, or not performing to specifications. The purpose of the following information is to brief you on solid-state "no-tune" RF amplifiers so that you can knowledgeably approach and correct any apparent improper performance characteristic.

4-1.6 BROADBAND vs RESONANT TANKS Almost all tube circuits use resonant tanks in the plate circuit. The PARAGON uses a broadband system. In class AB operation, these two approaches act similarly without drive being applied. The idle current is relatively low and within the device dissipation rating, even with load impedance variations from open to short circuit.

However, with drive applied, the two act very differently. In the case of tubes, the dissipation within the tube depends on both the tuning of the tank and the load applied. If the tank is resonated and the load is very light, the internal power dissipated is quite small as indicated by the null which reduces plate current almost to the level with no drive. Out of resonance, the plate current, and hence dissipation, increases rapidly and may damage the tube from overheating. In resonance, as the load is increased, the null becomes more shallow at a higher plate current as a result of the power being delivered to the load. As the tank is tuned to resonance, the load impedance which is usually on the order of 50Ω is transformed to a relatively high impedance of several thousand ohms to match the plate circuit impedance. Small load reactive components, either capacitive or inductive, can usually be balanced out in the tank resonating function.

With transistors, drive applied and no load, there is no resonant high impedance to limit the collector current, and so power is poured into the circuit (much as the out-of-resonance tank condition). Since there is no load power, all has to be dissipated in the transistor. So even with no load, the ALC LED may light as the current limiting circuitry is automatically reducing drive level, or the power supply circuit breaker may trip. The broad-band transformer system used with transistors transforms the 50Ω load impedance not higher, but much lower (in the order of 4 or 5 Ω) to match the transistor output impedance. Since this transformation is fixed in design, any reactive component in the load impedance is applied in a transformed way to the collector circuit. Certain reactances at this point, especially inductive, give rise to parasitic oscillation. To correct for this, the antenna impedance should be changed to remove this reactance, or a matching network should be inserted between the antenna and transceiver. It is important to remember that any antenna changes its impedance with frequency, so that one that resonates well at one end of the band may well cause oscillations to activate the current limiting or trip the circuit

breaker on the other end of the band. If entire band operation is desired, especially on the lower bands, the adjustable matching network would be the better choice, rather than to try to make the antenna behave over the entire band on a cut-and-try basis.

A final point to bring out regarding broadband vs tank systems is that there is a limit to the amount of current that you can draw from an emitting filament, and this saturation current will limit the amount of power drawn from the supply. In the case of transistors, where the collector internal impedance is only a fraction of an ohm, extremely high currents can be demanded of the power supply, especially with mismatched loads well below 50 ohms. A fuse is provided in the PARAGON for protection when operating from a power source that is not limited.

4-1.7 SWR - Two Kinds The standing wave ratio is direct measure of the ratio between two impedances, i.e. a SWR of 3 to 1 indicates that one impedance is three times the other. Therefore, the unknown impedance can be either three times as large or three times as small as the known one. If the desired impedance that the transceiver wants to see is 50Ω, an SWR of 3 to 1 on the line may mean a load impedance of either 150 Ω or one of 17 Ω. If it is 150 Ω, the transmitter will act differently than if it is 17 Ω. In the first case, the power demanded from the power supply will be much lower, and not large enough to trip the circuit breaker. In the second case, even though the SWR reads the same, the breaker may repeatedly trip out. The SWR reading gives no indication of reactive components, nor can it separate the resistive from the reactive components. It is calibrated with a pure resistive load and therefore has its greatest accuracy with pure resistive loads. The SWR bridge should be used only as an indicator when attempting to adjust antenna systems to a pure 50 Ω resistive impedance at the transmitter output point.

4-1.8 EFFICIENCY Since transistor amplifiers have a very low value of output impedance, they act more or less as a constant voltage source. That is the RF output voltage tends to remain at a fixed value regardless of the load impedance. Hence, the output power will vary depending on the value of the load, and increases as the load impedance goes down. It can be seen that a 3 to 1 SWR on the low side of 50Ω will ask the amplifier to deliver much more power than a 3 to 1 SWR on the high side. Since the amplifier does have a finite value of output impedance, the amount of power delivered to the load with efficiency will change with load. Unless the load is near the design value, the transistors will heat up unnecessarily without delivering any more power to the antenna.

Recommended Reading: ARRL HANDBOOK

IF YOU HAVE TROUBLE

If the transceiver should fail to operate as normal, use the following chart as an aid in determining the problem. Often the cause of the problem is an overlooked switch/control or a mistake in entering information into the keypad.

SYMPTOM	POSSIBLE CAUSE
Transceiver dead, no meter illumination, no display.	Check power switch on transceiver and power supply. Check power cable. Check supply for correct voltage.
Receiver dead, meter and display on.	Check Squelch, and AF gain controls. Check Phones and Ext. Spkr jacks. Check Crystal Filter keys for selection of bandwidth with option not installed. Check if FM mode selected without option installed. Check RX/TRX switch.
Transmitter dead, meter and display on.	Check frequency for less than 1.75 MHz or for ouside Ham Bands. Check microphone, PTT switch, and microphone cable & connector Check if AM mode selected, or FM mode selected without option installed.
Received signal strength low.	Check ATTN switch and RF gain control.
Main tuning knob will not change frequency.	Check LOCK key and LED. Press CLEAR key.
Main tuning knob will not change frequency, keypad will not respond to input.	Microprocessor may be in process of a selected function routine. Memory Scan mode is selected with less than 2 memory channels programmed and/or unlocked. Press CLEAR key.
No readout, audio present. Readout present, connot enter commands.	Microprocessor may be locked up due to an incorrect keyboard entry or a power supply noise spike. Turn the POWER switch on the PARAGON off and then back on. If this does not clear the problem, the microprocessor will have to be reset. Press the RESET button located on the lower right side of the PARAGON. NOTE: PRESSING THE RESET SWITCH WILL **CLEAR ALL MEMORIES** AND RESET THE TIME AND DATE. Use this approach only as a last resort.
Display flashes message "PLL OUT OF LOCK".	Check several different frequencies on each band. If this message appears only when keying the PARAGON in SPLIT or OFFSET operation, one or more of the VCO's is probably slightly misaligned. If this message occurs on all bands there is something seriously wrong in the PLL synthesizer. In either case, it is recommended that you return the PARAGON to the factory for prompt repair.
When in SSB mode, transmitted audio is heard in speaker or headphones. (Talk-through)	Check SSB MONITOR LEVEL control on rear panel.

TABLE 4-1. TROUBLE SHOOTING CHART

CHAPTER 5

OPTIONS INSTALLATION

5-1 INTRODUCTION The following paragraphs describe how to remove the top and bottom covers of the PARAGON and the basic steps required to install the various optional accessories available for use in the PARAGON. Additional instructions and information may be supplied with each of the options.

5-1.1 REMOVAL OF TOP & BOTTOM COVER To remove the top cover, remove the upper two of the four large Phillips screws located on each side. Slide the top back and out from under the rear lip of the extruded front panel. *Caution:* Speaker wires will limit removal of the top cover. Unplug the speaker connector before completely removing the top cover.

To remove the bottom cover, remove the lower two large Phillips screws located on each side. With the transceiver upside down and the front panel facing forward, slide the bottom cover back and out from underneath the rear lip of the extruded front panel. Next remove the twelve screws securing the bottom shield and carefully remove the shield cover.

5-1.2 "MASS TERM" CONNECTORS

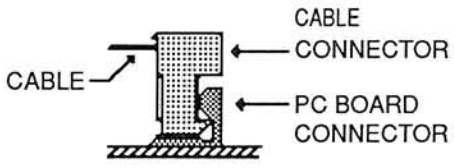


FIGURE 5-1. MASS TERM CONNECTOR

Some of the options require attachment of cables to the options pc board. The "mass term" type connectors have an identification number on the cable connector which matches the same number printed on the top of the pc board. The polarity of the connectors is as shown in the diagram.

5-1.3 CRYSTAL FILTERS

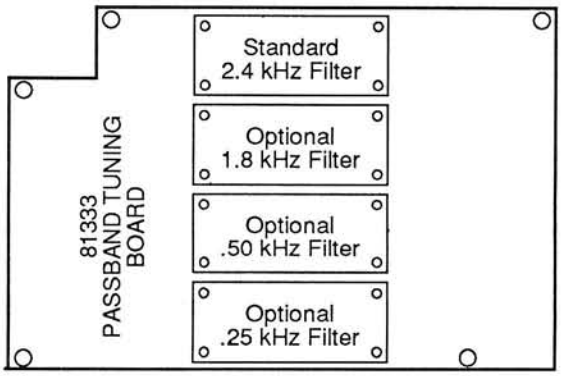


FIGURE 5-2. CRYSTAL FILTER LOCATIONS

There are three optional crystal filters which may be installed in the PARAGON, Model 288 (1.8 kHz), Model 285 (.5 kHz), and Model 282 (.25 kHz). These options plug into the Pass Band Tuning Board located on the bottom side of the transceiver. The inputs and outputs of these boards are the same and therefore they may be installed in either direction.

5-1.4 VOICE READOUT The Voice Readout option, Model 257, announces the displayed frequency whenever the VOICE key is pressed. The Voice Readout pc board

plugs into an edge card connector located on the Logic Board. Refer to FIGURE 5-3 for the location of the Logic Board and the Voice Readout edge card connector.

After installing the Voice Readout, press the VOICE key and adjust the speech level control, located on the Voice Readout pc board, to a suitable level.

For more detailed information on the use of the Voice Readout, refer to the instructions included with the Model 257.

5-1.5 RS232 INTERFACE The RS232 Interface option, Model 258, provides communication between the logic circuits of the PARAGON and an external computer with RS232 capability. All of the keypad functions and the main tuning circuitry can be controlled.

The option package includes a plug-in pc board that contains all of the required driver and interface circuitry, an RS232 connector to be mounted on the rear panel of the transceiver, a connecting cable, and information listing the command codes required to access the microprocessor.

To install the rear panel connector, remove the top cover of the transceiver and remove the two screws & nuts securing the connector cover plate. Using the two screws just removed, attach the RS232 connector to the rear panel. Plug the RS232 Interface Board, with the connecting cable attached, into the edge card connector on the Logic Board. Then plug the other end of the cable into the RS232 rear panel connector board.

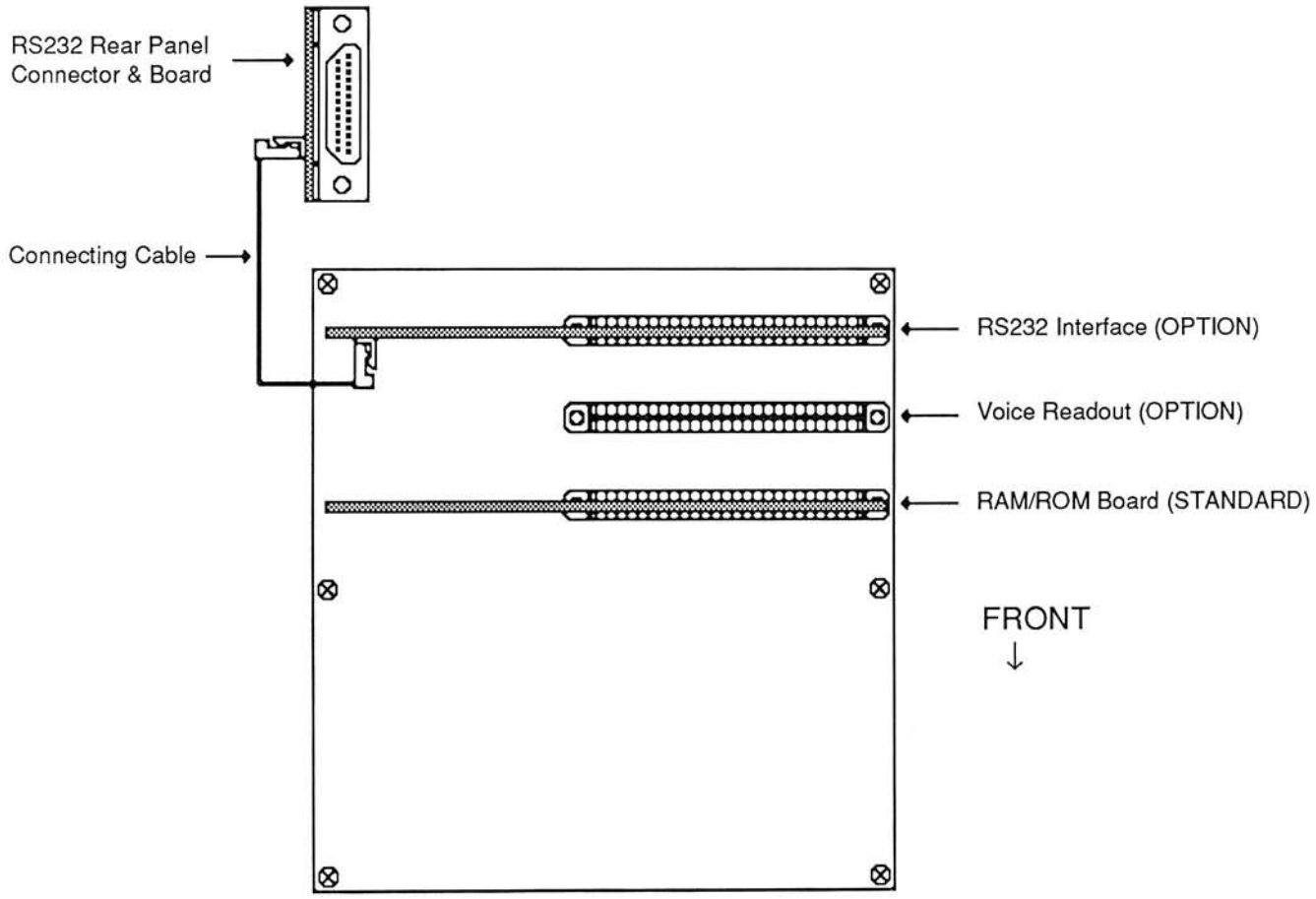


FIGURE 5-3. OPTIONS INSTALLATION DIAGRAM

5-1.6 FM ADAPTOR The optional Model 256 FM Adaptor enabl· s the PARAGON to transceive ± 5 kHz deviation FM. For information on operating FM with the PARAGON refer to PARAGRAPH 4-1.2 and to the instructions provided with the adaptor.

To install the FM Adaptor, remove the top cover and locate the synthesizer sub-chassis on the left side of the transceiver (with the front panel facing forward).
There are four mounting posts located on the topside of the sub-chassis where the FM board is mounted with the four screws supplied.

Refer to the detailed mounting and connection instructions provided with the Model 256 for the remaining installation steps.

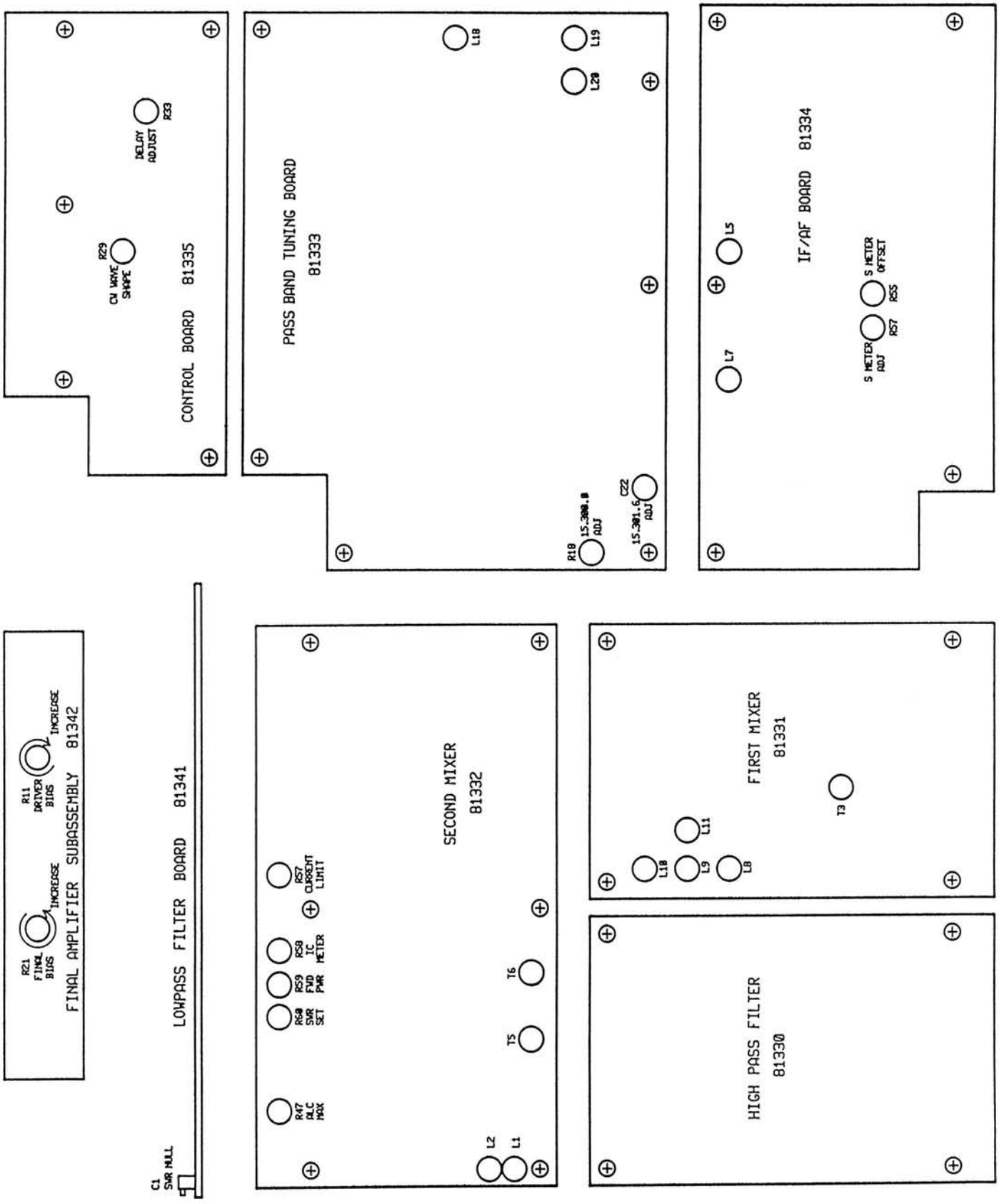


FIGURE 5-4. MODEL 585 ADJUSTMENTS (BOTTOM VIEW)

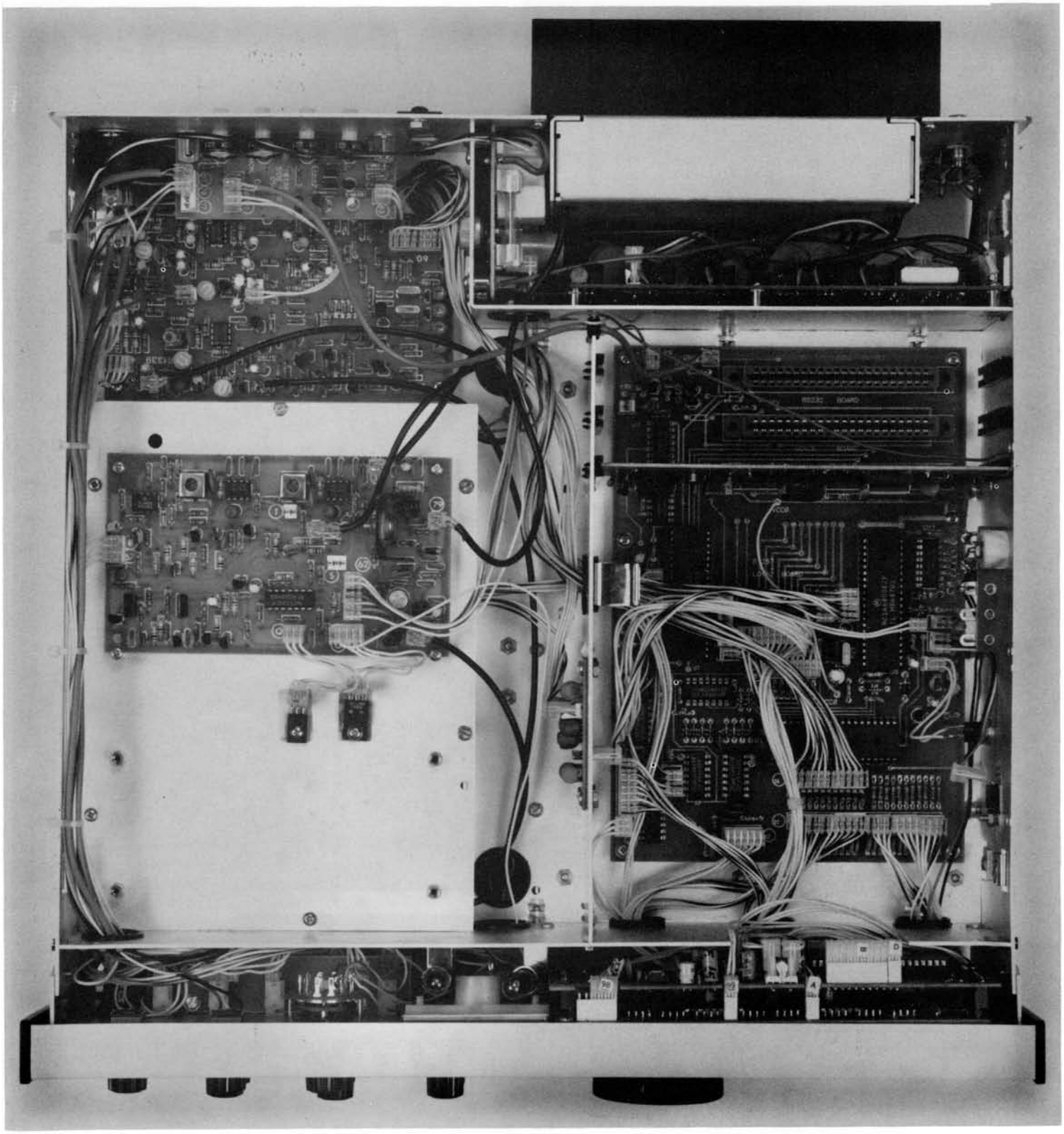


FIGURE 5-5. MODEL 585 TOP VIEW

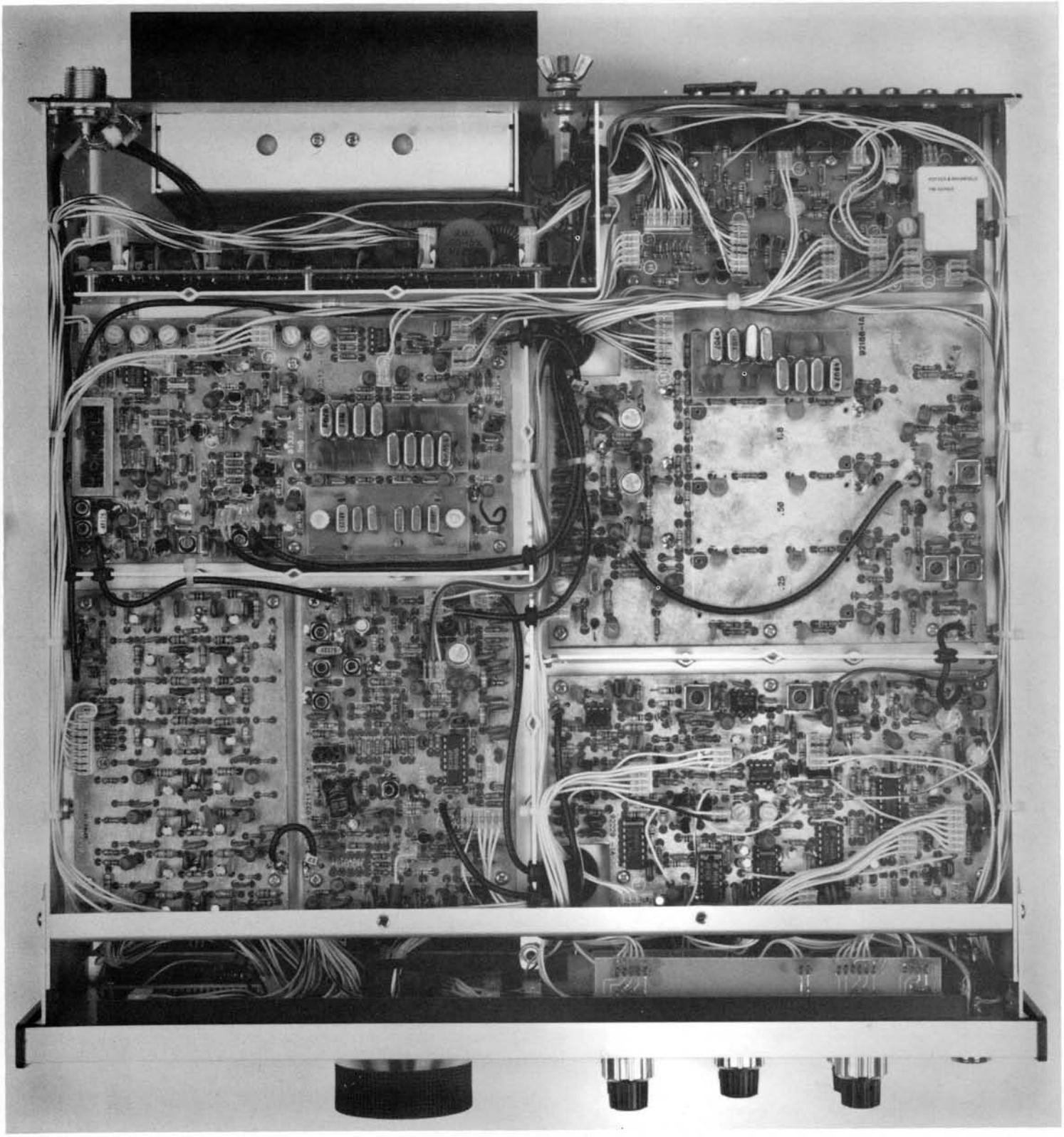


FIGURE 5-6. MODEL 585 BOTTOM VIEW

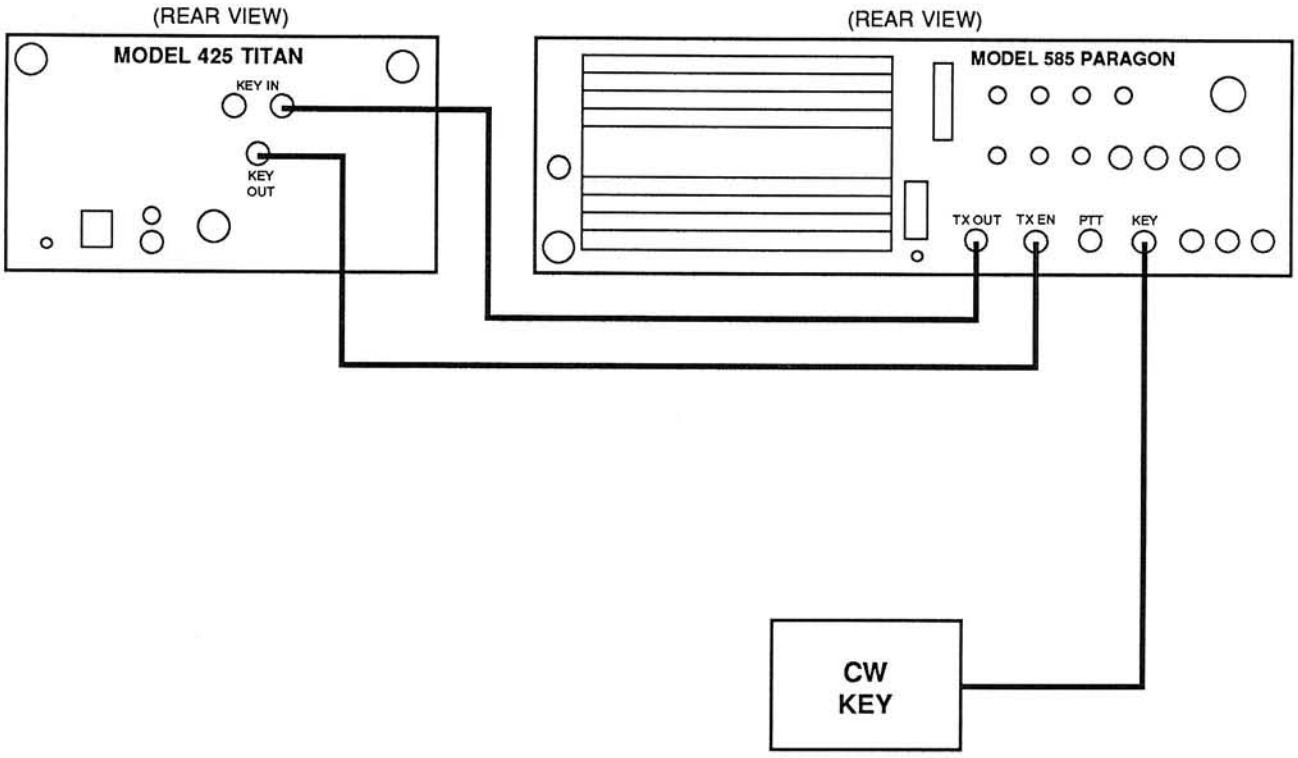
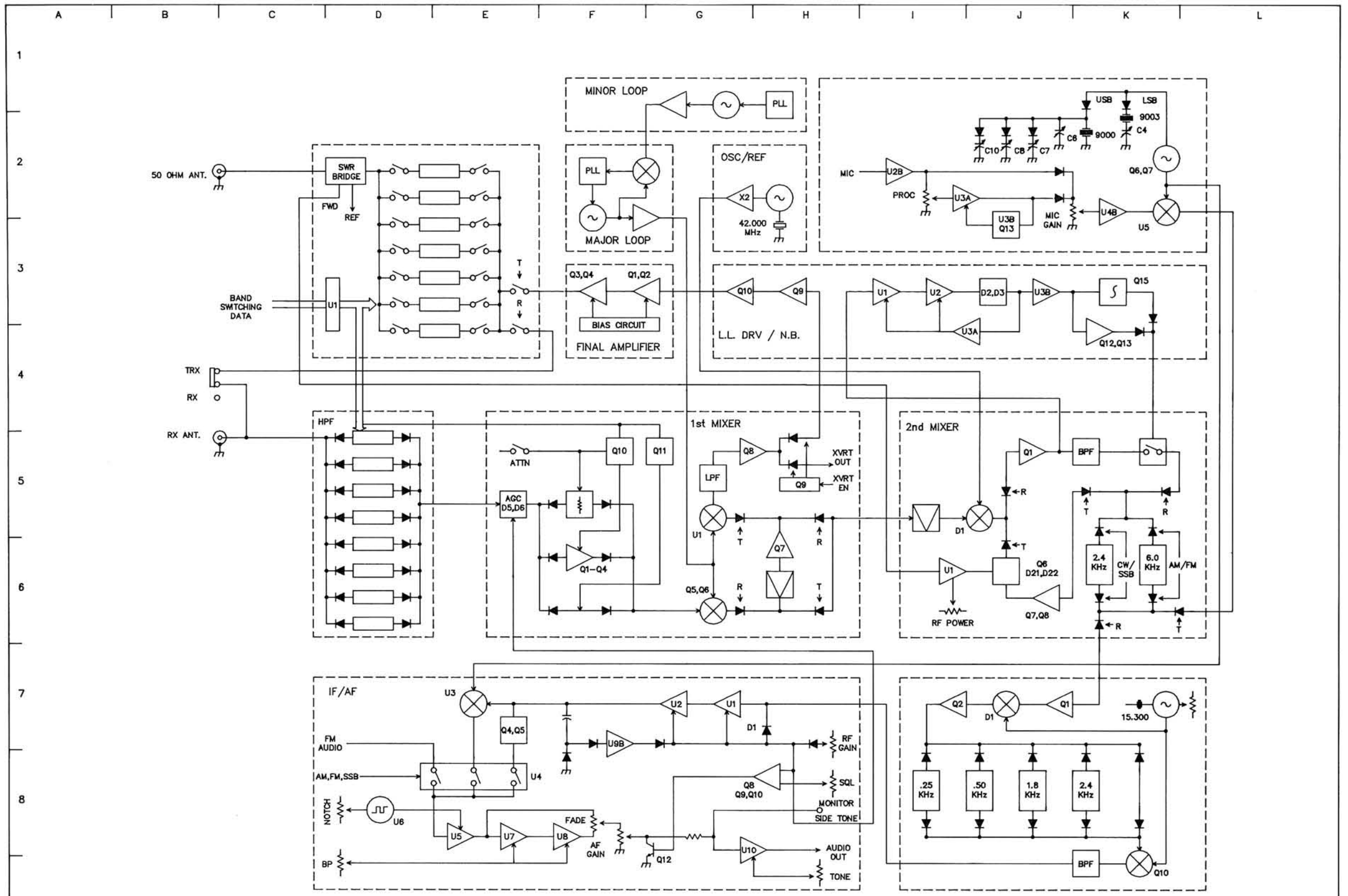


FIGURE 5-7. QSK HOOK-UP WITH TITAN AMPLIFIER

CHAPTER 6

CIRCUIT DESCRIPTIONS AND ILLUSTRATIONS

6-1 INTRODUCTION The following sections contain detailed circuit descriptions for all of the printed circuit board subassemblies used in the PARAGON. Also included are circuit trace drawings and detailed component layout diagrams. These drawings are followed by fold-out schematic diagrams for each circuit board subassembly.


MINOR LOOP
PLL
MAJOR LOOP
OSC/REF
X2
42.000 MHz
50 OHM ANT.
SWR BRIDGE
FWD
REF
BAND SWITCHING DATA
U1
T
R
Q3,Q4
Q1,Q2
BIAS CIRCUIT
FINAL AMPLIFIER
Q10
Q9
L.L. DRV / N.B.
USB
LSB
9003
C4
C10
C8
C7
C6
9000
MIC
U2B
PROC
U3A
U3B Q13
MIC GAIN
U4B
Q6,Q7
U5
U1
U2
D2,D3
U3B
Q15
Q12,Q13
TRX
RX
RX ANT.
HPF
ATTN
Q10
Q11
AGC D5,D6
Q1–Q4
1st MIXER
Q8
XVRT OUT
XVRT EN
Q9
LPF
U1
T
R
Q7
Q5,Q6
2nd MIXER
Q1
BPF
D1
R
T
Q6 D21,D22
U1
RF POWER
Q7,Q8
2.4 KHz
CW/ SSB
6.0 KHz
AM/FM
IF/AF
U3
Q4,Q5
U2
U1
D1
U9B
RF GAIN
FM AUDIO
AM,FM,SSB
U4
Q8 Q9,Q10
SQL
MONITOR
SIDE TONE
NOTCH
U6
U5
U7
U8
FADE
AF GAIN
Q12
U10
AUDIO OUT
TONE
BP
Q2
D1
Q1
15.300
.25 KHz
.50 KHz
1.8 KHz
2.4 KHz
BPF
Q10

6-2 TRANSMIT LOW PASS FILTER (81341)

This board contains an array of seven 5-pole lowpass output filters, the T/R switching relays, and a directional coupler for forward power and SWR detection.

Eight band lines from the control filter board enter at connector 8 where they are buffered by relay driver U1 and pass through connectors 14 and N to energize filter select relays K3-K16. The buffered band lines also exit connector 14 to the receive high pass filter board for simultaneous selection of receive filters. One of the eight lines is high at any one time based on the operating frequency of the transceiver.

The 100 Watt RF output of the PA is connected through the contacts of K1, which is energized by "T" voltage, and proceeds through the selected filter and the primary of SWR bridge transformer T1 to the rear panel antenna connector. Based on operating frequency, the proper lowpass filter is automatically selected to attenuate harmonics of the RF PA output signal to an acceptable level before radiation by the station antenna. Bridge transformer T1 and associated circuitry discriminate between forward and reflected power to develop drive voltages at connector 12 for the ALC and RF metering circuits on the 2nd mixer board.

On receive, K1 is open and K2 is energized by "R" voltage, connecting the lowpass filtered antenna to the receiver input at connector 13. From connector 13 the receive signal passes through the receive highpass filter board (by way of the rear panel RX/TRX switch) before entering the 1st mixer board. The combination of transmit lowpass filter and receive highpass filter produces an overall bandpass response which determines the front end bandwidth of the receiver.

Connector 9 brings "T" and "R" voltages from the control board to the T/R relays K1 and K2. "T" voltage is supplied to the PA through connector 11 and relay driver U1 is powered by 13.5 Volts from connector 4.

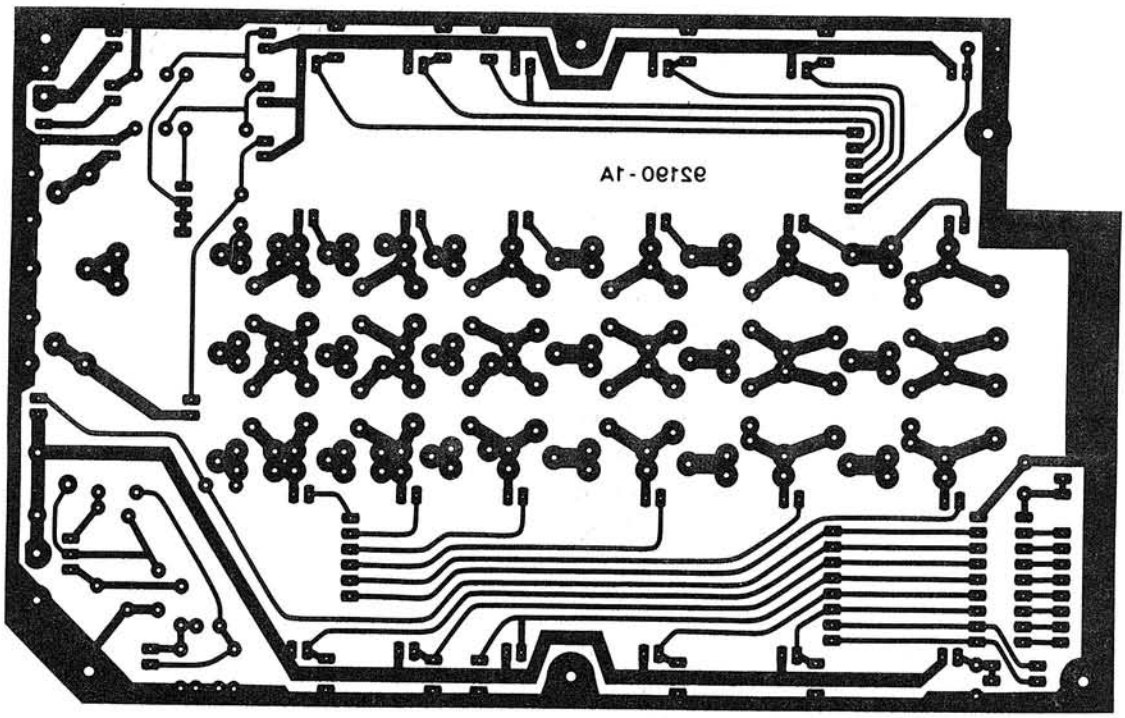


FIGURE 6-2. 81341 TRANSMIT LOW PASS FILTER CIRCUIT TRACE

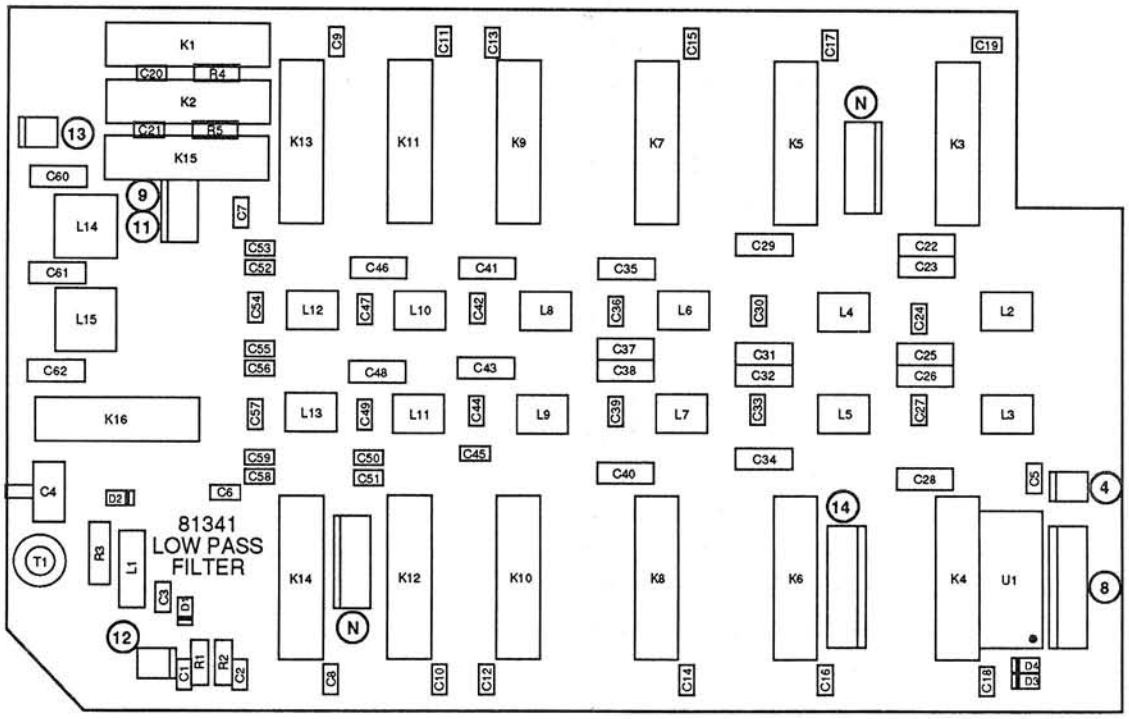
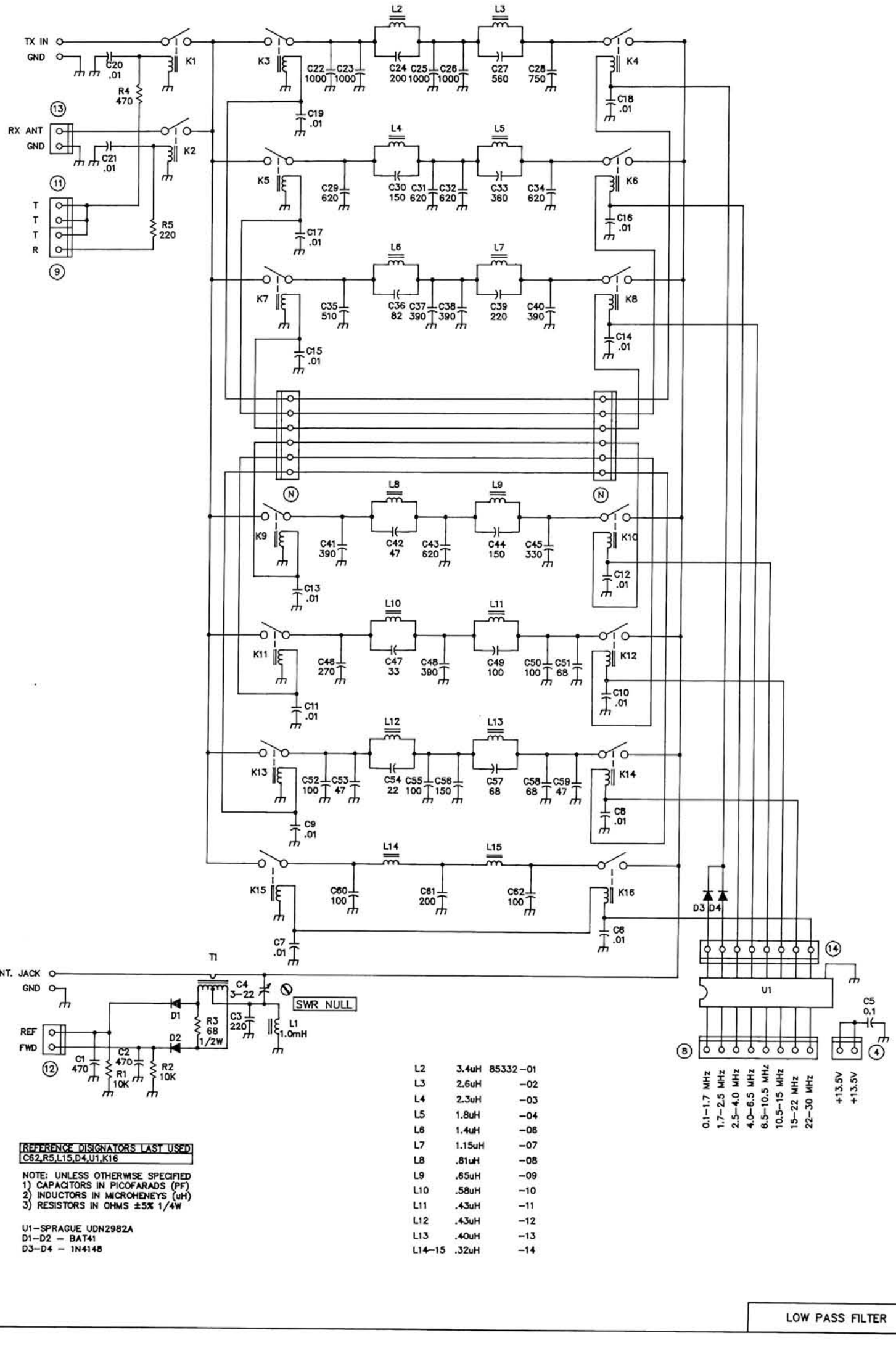


FIGURE 6-3. 81341 TRANSMIT LOW PASS FILTER COMPONENT LAYOUT



L2	3.4uH	85332-01
L3	2.6uH	-02
L4	2.3uH	-03
L5	1.8uH	-04
L6	1.4uH	-06
L7	1.15uH	-07
L8	.81uH	-08
L9	.65uH	-09
L10	.58uH	-10
L11	.43uH	-11
L12	.43uH	-12
L13	.40uH	-13
L14-15	.32uH	-14

REFERENCE DISIGNATORS LAST USED
C62,R5,L15,D4,U1,K16

NOTE: UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENEYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1-SPRAGUE UDN2982A
D1-D2 - BAT41
D3-D4 - 1N4148

LOW PASS FILTER | 81341

6-3 RX HIGH PASS FILTER (81330)

This assembly contains the band selected high pass filters which, in conjunction with the transmit low pass filters, determine the front end bandwidth of the receiver. The filters are 5th order elliptical designs with the exception of the 0.1-1.6 Mhz band which is a 5 pole lowpass. Connector 15 is the input to this board and connector 17 is the output. A 30 MHz low pass filter at the input improves the image rejection and the 75 Mhz IF rejection of the receiver.

PIN diodes D1-D16 select a high pass filter based on band information from connector 14. One of the eight lines from connector 14 is driven high (approximately 12 Volts) by a relay driver on the transmit low pass filter board, providing forward current to the input and output PIN diodes for the selected band. The diode forward currents return through resistors R19 and R20 providing a reverse bias voltage for the diodes of the deselected bands. Connector 16 supplies 0.1-1.6 Mhz band information to the 1st mixer board to disable the RF amplifier on that band.

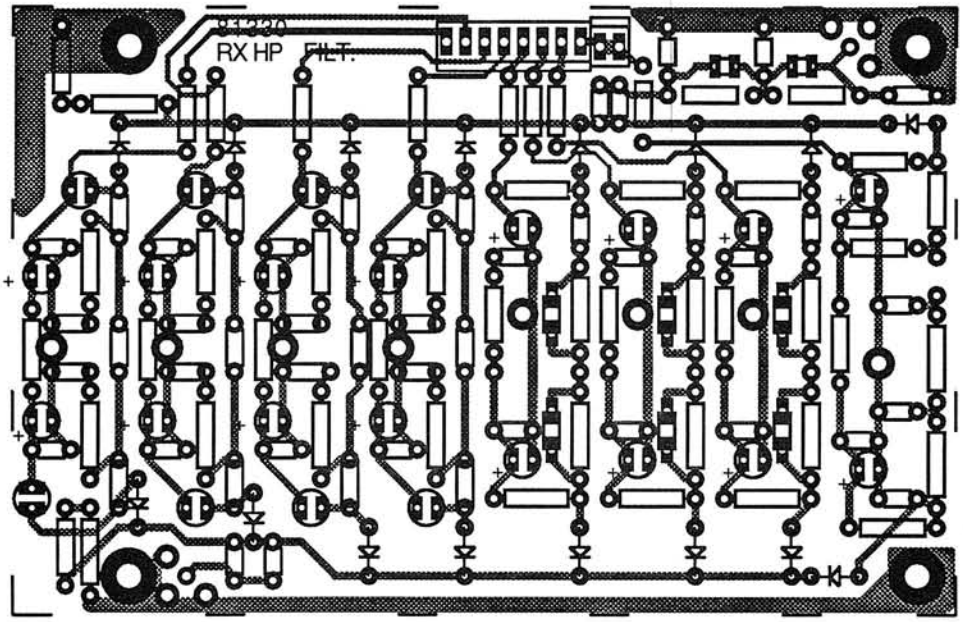


FIGURE 6-5. 81330 RX HIGH PASS FILTER CIRCUIT TRACE

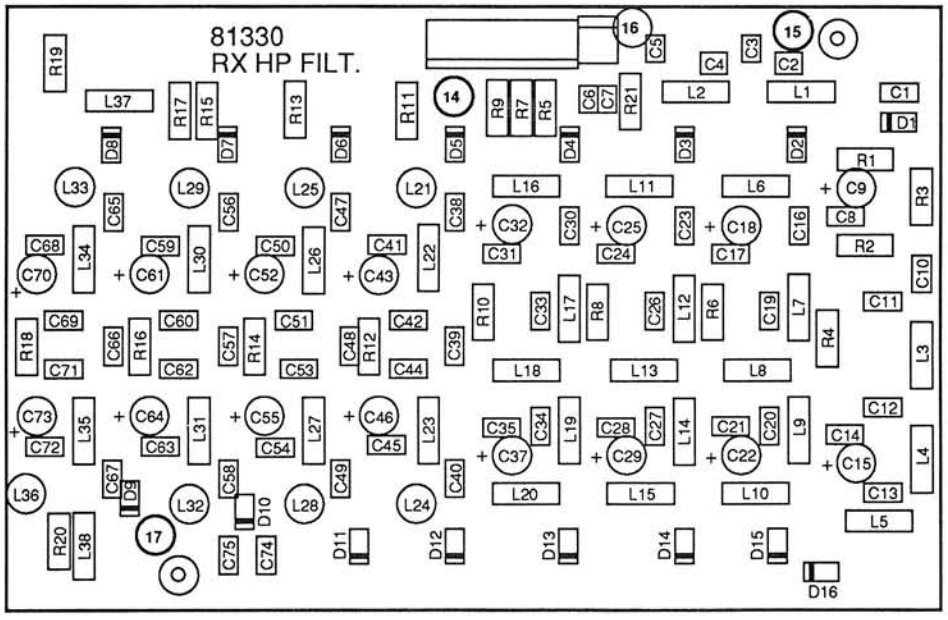


FIGURE 6-6. 81330 RX HIGH PASS FILTER COMPONENT LAYOUT

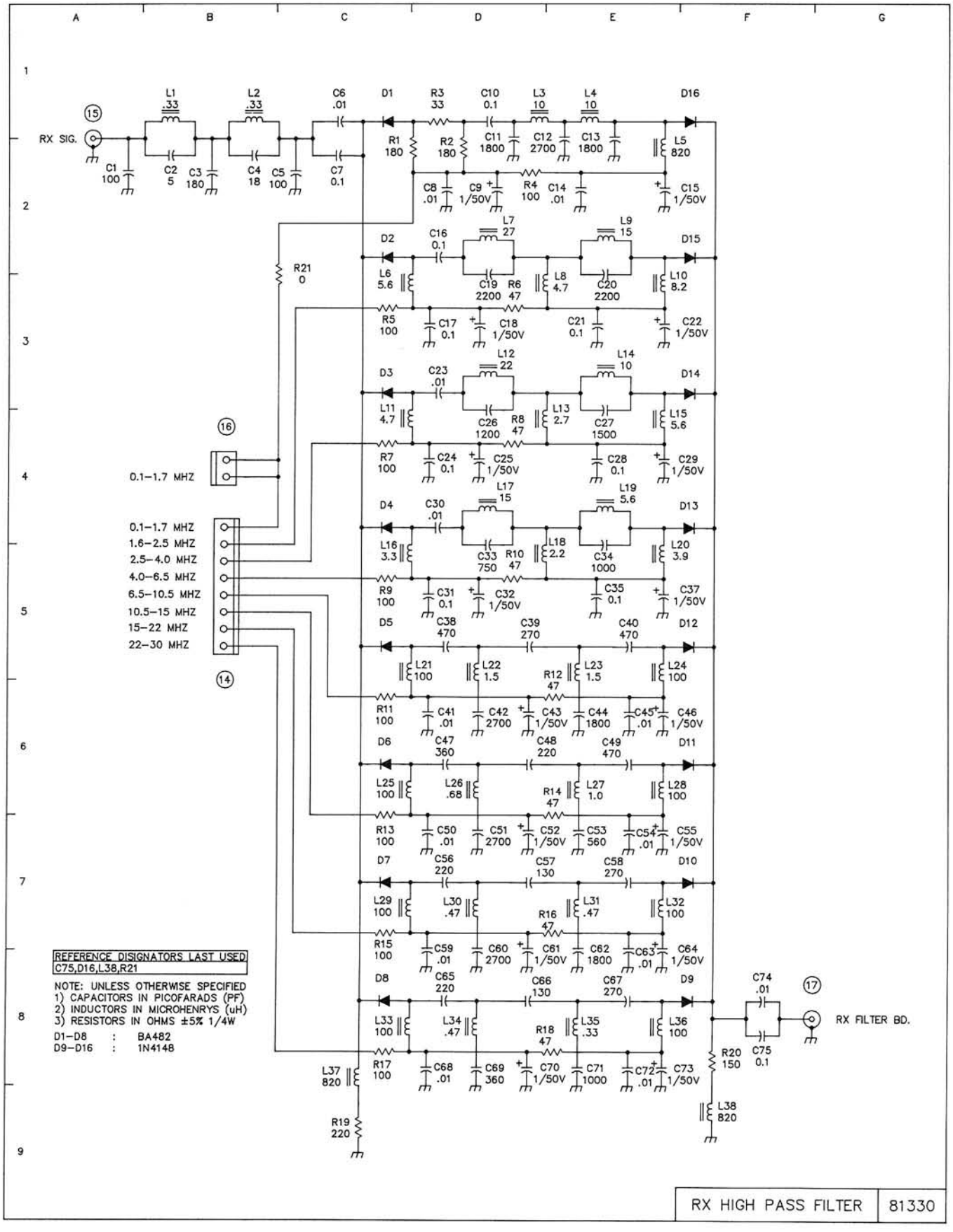


FIGURE 6-7. 81330 RX HIGH PASS FILTER SCHEMATIC

6-4 FIRST MIXER (81331)

This board contains the receiver functions of RF amplifier and receive attenuator, 1st mixer, monolithic filter, and filter post amplifier. It also performs the transmit functions of transmit mixer and low level preamplifier. It accepts receiver input from the receive high pass filter board at connector 17 and produces a 75 MHz IF output to the second mixer board at connector 25. On transmit, the 75 MHz transmit IF from the 2nd mixer board is accepted at connector 25 and a transmit signal on the operating frequency is output to the low level driver board on connector 24.

The receive input at connector 17 passes through PIN attenuator diode D5 and diode switch D7 to the RF amplifier Q1-Q4. D5 is normally forward biased by the two diode drops across D1 and D2, but this bias can be overcome by forward current through PIN diode D6 produced by large signal AGC voltage from the IF/AF board on connector 19. Four junction FETs are paralleled in the broadband RF amplifier stage to provide high dynamic range, greatly reducing the level of interfering intermodulation products from nearby large signals in the band. Diode switch D12 connects the RF amplifier output to the input of the high level single balanced 1st mixer Q5-Q6.

Transistors Q10 and Q11 and diode switches D8-D11 provide a means for bypassing the RF amplifier with either a direct path or a -20dB pad depending on the front panel ATTN switch setting and the band of operation. The front panel ATTN switch, through connector 18, normally feeds 13.5 Volts to the emitter of Q10. On bands other than .1-1.6 MHz, the base of Q10 is pulled low by D3 and R56 via connector 16. The forward biased Q10 then supplies power to the RF amplifier through L23, forward biasing diode switches D7 and D12 and reverse biasing diodes D8-D11. When the .1-1.6 MHz band is selected, with the ATTN switch still in the normal position, connector 16 supplies 12.5 Volts to emitter follower Q11 which forward biases diodes D9 and D11, reverse biasing D8, D10, D7, D12, and Q10. This removes power from the RF amplifier and bypasses it with a direct connection through D9 and D11. Switching the front panel ATTN switch to the -20dB position removes voltage from the emitter of Q10 and applies 13.5 Volts to R53, forward biasing diodes D8 and D10, and reverse biasing D9, D11, D7, D12, Q10, and Q11, regardless of the band of operation. This inserts -10dB pad resistors R48, R50, and R99 in place of the RF amplifier producing a net gain reduction of -20dB on bands above 1.6 MHz.

First mixer transistors Q5 and Q6 mix the receive signal in the .1-30 MHz range with the synthesizer 1st LO output of 75.1-105 MHz to produce the first IF at 75 MHz. Tuned transformer T3 couples the 75 MHz mixer output through 3dB pad R17-R19 to diode switch D13 which is forward biased in receive by "R" voltage from connector 20. The 3dB pad serves to stabilize impedance variations and terminate mixer products at the mixer output port, improving the distortion performance of the mixer and the match to the crystal filter. Tuned matching networks C18-C22 and L8-L10 couple the 75 MHz IF signal through a 15 KHz wide 2 pole monolithic crystal filter and into the 1st IF amplifier stage Q7. Tuned circuit C25, C26 and L11 matches the output of Q1 to 50 Ohms and diode D15 routes the signal to the 2nd mixer board via connector 25.

In transmit, "T" voltage from connector 20 powers transmit mixer U1 and forward biases diode switches D14, D16, and D17, reverse biasing D13 and D15. The monolithic filter and IF amplifier now process the 75 MHz transmit IF signal from the 2nd mixer board at connector 25 and feed it to one input of transmit double balanced mixer U1. U1 mixes the 75 MHz IF with the synthesizer output of 76.7-

105 MHz to produce an output on the operating frequency in the range of 1.7-30 MHz. This signal passes through 30 MHz lowpass filter C36-C38, L19-20 to the input of broadband amplifier Q8. The output of Q8 is matched to 50 Ohms by T7 and normally passes through diode switch D17 to the transmit low level amplifier board via connector 24. However, when the transverter enable pin of connector 22 is pulled low by grounding the center pin of the rear panel XVRT EN connector, transistor switch Q9 supplies a forward current to D18 which reverse biases D17 so that the output of Q8 is diverted through 3dB pad R43-R45 to the rear panel XVRT OUT connector via connector 23. This output is useful for driving transmitting frequency converters which require an input level of approximately +5dBm in the 1.7-30 MHz band.

To ensure that no stray signals leak in from the receiver input connector 17 during transmit, diode D4 is included to bias up the AGC attenuator diodes D5 and D6 while "T" voltage is high.

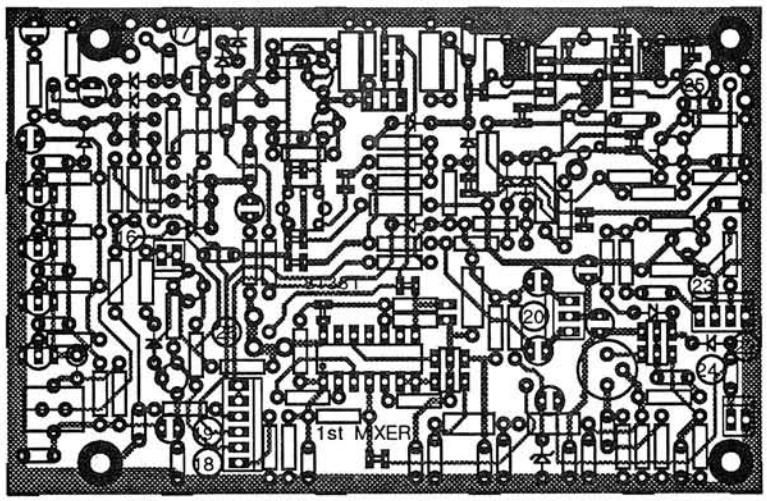


FIGURE 6-8. 81331 FIRST MIXER CIRCUIT TRACE

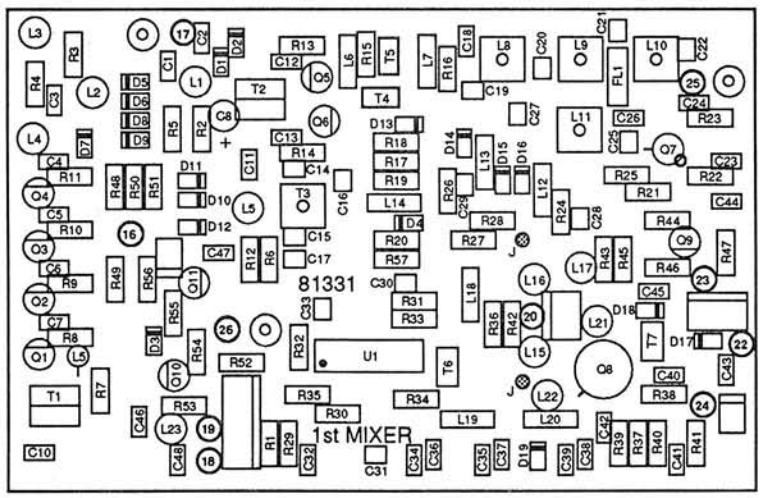
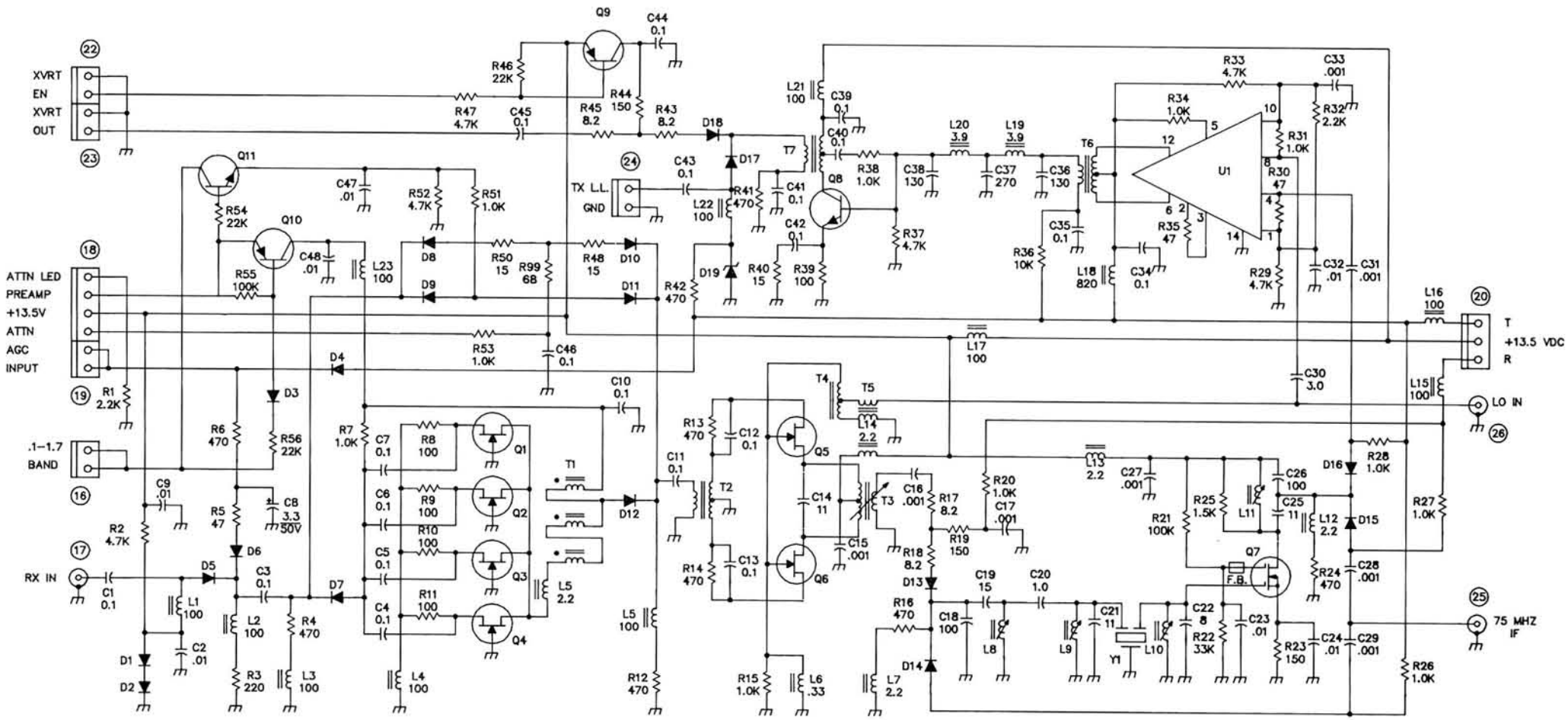


FIGURE 6-9. 81331 FIRST MIXER COMPONENT LAYOUT



U1	MC1496P
Q1–Q6	J310
Q7	JN201
Q8	2N3866
Q9	2N5087
Q10	MPSA64
Q11,Q12	MPS6514
D1–D4	1N4148
D7–D18	BA482
D19	1N751A, 5.1V
D5,D6	HP 3379 / 1N5767

REFERENCE DISIGNATORS LAST USED
C46,L23,D19,Q12,U1,T7

NOTE: UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

6 - 15 / 6 - 16 blank

FIRST MIXER	81331

6-5 SECOND MIXER (81332)

The second mixer board uses the 84 MHz second LO (from oscillator reference connector 27) to perform the frequency conversion between the 75 MHz 1st IF at connector 25 (from the 1st mixer board) and the 9 MHz 2nd IF at connector 38 in receive, or at connector 37 in transmit. It also performs the noise blanker sampling and gating functions for receive, and the ALC function for transmit. Connections to the noise blanker circuit on the low level amplifier board are through connectors 31 and 32. The inputs to the ALC circuit are connectors 29 from the front panel RF PWR control, 12 from the lowpass filter board (FWD), and 7 from the DC power board (ISENSE). This board also contains a 75 MHz 2-pole monolithic crystal filter and 9 MHz AM and SSB 8-pole crystal filters to provide part of the selectivity on receive and the sideband rejection on transmit.

84 MHz from the PLL oscillator reference board drives the LO port of double balanced diode mixer D1. On receive, a 75 Mhz 1st IF signal enters the RF port of the mixer through 15 KHz wide 2-pole monolithic filter Y1. Diode switch D2 is forward biased by "R" voltage from control board connector 35, passing the mixer output to grounded gate amplifier Q1. The 9 MHz output of Q1 is selected by tuned transformers T5 and T6 and coupled to emitter follower Q2 and noise blanker gate circuit T7-T8, D4-D7. Connector 31 carries the output of Q2 to the noise blanker circuit on the low level amplifier board which, when activated, develops a blanking pulse on connector 32. When a blanking pulse drives clamp transistor Q3 into conduction, gate diodes D4-D7 which are normally forward biased by R11 and R12, are reverse biased by the voltage across C14, blocking passage of the noise pulse to T8. Unblanked signals proceed through T8, T9, and forward biased diode D8 to whichever 9 MHz 8-pole crystal filter is selected by the control board via connector 34. "R" voltage forward biases D18 and reverse biases D16-17 to connect the 9 MHz filter output to the passband tuning board via T10 and connector 38.

In transmit, Diodes D16 and D17 are forward biased by a DC voltage from the TX Audio board on connector 37, connecting the 9 MHz double sideband output of the balanced modulator (or an unbalanced carrier in CW/RTTY) through T10 and D12-D13 to 2.4 KHz sideband filter Y3. The desired sideband is selected by Y3 and passed through D11 and D9, which is forward biased by "T" voltage from control board connector 35, to amplifier and follower Q6 and Q7. The output of emitter follower Q6 drives ALC PIN attenuator diodes D21 and D22. PIN diode D21 is normally biased on in transmit by voltage across zener diode D20, providing a direct path through C34, attenuator R33-R35, and D3 to mixer D1. Mixer D1 converts the signal up to 75 MHz and passes it through T1 and 2-pole filter Y1 to the 1st mixer board on connector 25. ALC voltage from the emitter of Q5 forward biases PIN diode D22, shunting part of the 9 MHz transmit signal from Q6 to ground through C36. Also, the forward current of D22 reduces the forward bias of D12, reducing the portion of the signal flowing to C34 and mixer D1.

ALC voltage is developed by U1 and U2 based on samples of RF output and PA collector current, and the setting of the front panel RF PWR control. At connector 12, the forward power sample of the SWR bridge on the transmit lowpass filter board passes through R49 and D30 to U1b, where it is compared to a voltage reference set by the RF PWR control through connector 29 and R44. When the forward power sample exceeds the reference voltage, the output of U1b goes up, charging capacitor C37 through D23 and R39, establishing an ALC voltage at the base of Q5. The emitter of Q5 follows this ALC voltage to control the attenuation through PIN diodes

D22 and D21 as explained above.

Voltage dropped across the PA current sampling resistor on the DC input board is cabled to connector 7 of this board. U2a level shifts this PA current sample and applies it to the input of DC amplifier U2b which drives the board mounted current limit adjustment R57. When the output of R57 exceeds the reference voltage set by the RF PWR control (factory adjusted to 22 amps with RF PWR fully clockwise), diode D25 is forward biased, and ALC action results similar to the forward power case above.

The reflected (reverse) power sample of the SWR bridge from connector 12 is sent to the front panel meter switch through calibration resistor R60, D29, and connector 30. The forward power sample is buffered by U1a to drive peak holding capacitor C39, calibration R59, and meter connector 30. The Ic function of the meter is driven by U2b through calibration R58, D27, and connector 30.

All active stages on this board are powered by "+REG", "R", or "T" from control board connector 36 except for U2 which receives +13.5 Volts from the DC input board at connector 7.

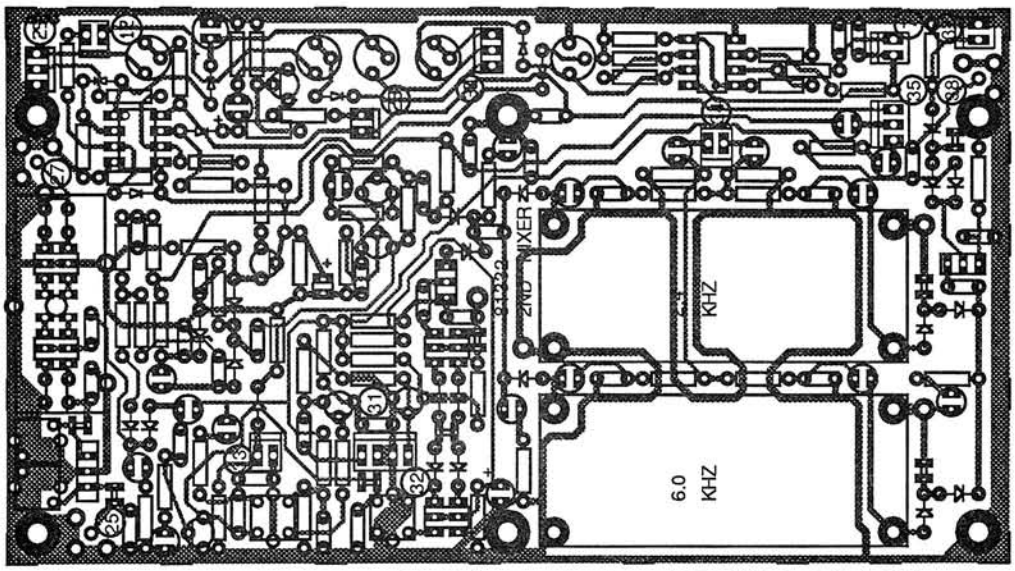


FIGURE 6-11. 81332 SECOND MIXER CIRCUIT TRACE

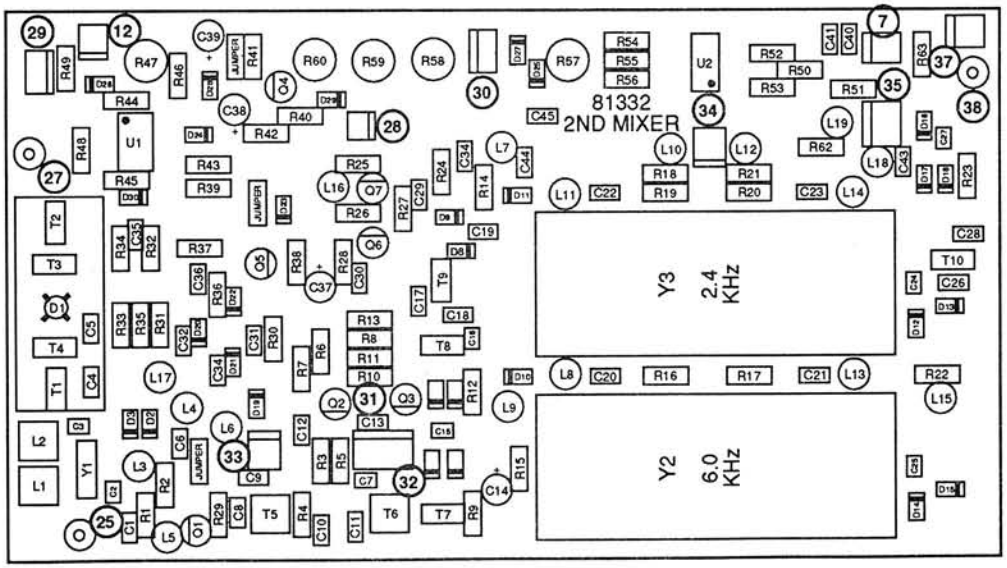
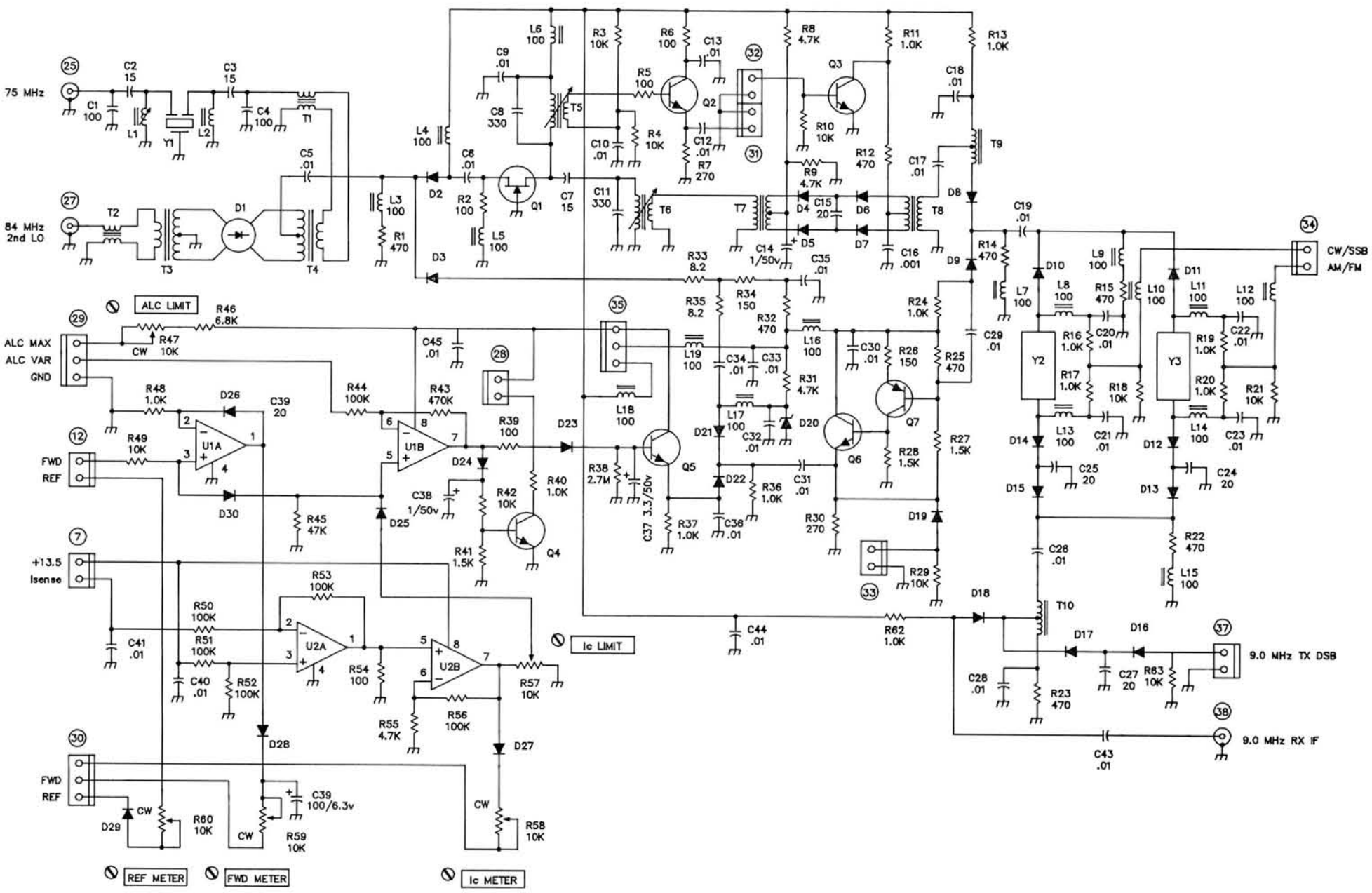


FIGURE 6-12. 81332 SECOND MIXER COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
C45,R63,Q7,D30,Y3

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

Q1	J310	D1	ND487C2-3R
Q2	MPS5179	D2-D19	BA482
Q3,Q4	MPS6514	D20	1N751A
Q5	MPSA14	D21-D22	IN5767
Q6	MPS3693	D23-D29	IN4148
Q7	2N5087	D30	BAT41
U1,U2	LM358N		
Y1	75 MHZ 2 POLE, 15KHZ BW		
Y2	9.0 MHZ 8 POLE, 2.4 KHZ BW (48058)		
Y3	9.0 MHZ 8 POLE, 6.0 KHZ BW (48127)		

6 - 19 / 6 - 20 blank

SECOND MIXER	81332

6-6 PASSBAND TUNING BOARD (81333)

The passband tuning board accepts a 9 MHz receive IF signal from the 2nd mixer board at connector 38, converts it down to approximately 6.3 MHz and passes it through one of four crystal filters (the 2.4 KHz filter is standard). Filter select lines from logic board connector 41 determine which filter is selected. After filtering, the signal is converted back to 9 MHz and sent to the IF/AF board via connector 43. The exact frequency of the signal before filtering is set by the front panel PBT control through connector 42.

The 9 MHz IF signal from the 2nd Mixer at connector 38 occupies a 2.4 KHz wide band (9.0003-9.0027 MHz) on SSB/CW and RTTY, and a 6 KHz band (8.997-9.003 MHz) on AM/FM. This signal is amplified by low noise amplifier Q1 and input to the RF port of mixer D1. The LO port of this mixer is driven with approximately 15.3 MHz from VCXO Q4 through buffer Q5 and LO amplifier Q3. The exact frequency of the LO signal is determined by the bias on tuning diode D19 which is set by the front panel PBT control through connector 42. The output of the VCXO is also buffered by Q6 and Q7 and used as the LO signal to the output mixer Q10. This arrangement insures that the IF signal exits the PBT board on exactly the same frequency as it entered, regardless of the VCXO frequency.

As an example of passband tuning board operation, it will be assumed that the receiver is operating in USB mode with the 2.4 KHz filter selected. With the PBT control centered, Q4 oscillates at 15.3 MHz, producing an output of 6.2973-6.2997 MHz from mixer D1. This matches exactly the passband of the 2.4 KHz sideband filter which is selected by diode switches D3, D13 and D14. In this condition the 8-pole response of the 2.4 KHz filter on this board is combined with the 8-pole response of the 2.4 KHz filter on the 2nd mixer board to produce an overall 16-pole IF filter response of 2.4 KHz bandwidth for the receiver. If the PBT control is rotated counter-clockwise, the frequency of the VCXO goes down (as much as 1.6 KHz for fully CCW), moving the output frequencies of mixer D1 down in relation to the passband of the 2.4 KHz filter on this board, filtering out some of the lower frequencies in the 2.4 KHz bandwidth mixer output signal. This effectively reduces the IF bandwidth of the receiver by the amount of the frequency shift of the VCXO. This reduced bandwidth signal is now mixed again with the VCXO in Q10 to return the remaining signals to their original frequencies. The end effect of this is that, as the PBT control is rotated counter-clockwise, the original 2.4 KHz USB passband is progressively reduced by as much as 1.6 KHz, and the reduction is accomplished by moving the upper edge of the passband downward, reducing the higher frequency audio tones of the received signal. Rotating the PBT control clockwise from center again reduces the passband, but this time the reduction is accomplished by shifting the lower passband edge upward, reducing the lower frequency audio tones.

The operation of passband tuning with other modes or filters selected is similar to the above except that in LSB the direction of control rotation is reversed with respect to audio frequency response (to preserve the correspondence of control movement to the frequency location of the received signals), and narrow filters have less useable range of shift. In AM/FM mode, an attenuator is selected by D2, D15 and D16 instead of a filter, so passband tuning has no effect.

Power to the output mixer Q10 is supplied through Q9 which is forward biased during receive by Q8. The input preamplifier Q1 and bias to VCXO Q4 are supplied by "R" voltage from control board connector 39. Regulated "+REG" voltage supplies the VCXO and buffers Q3 and Q5. The remaining stages are powered by 13.5 Volts from connector 39.

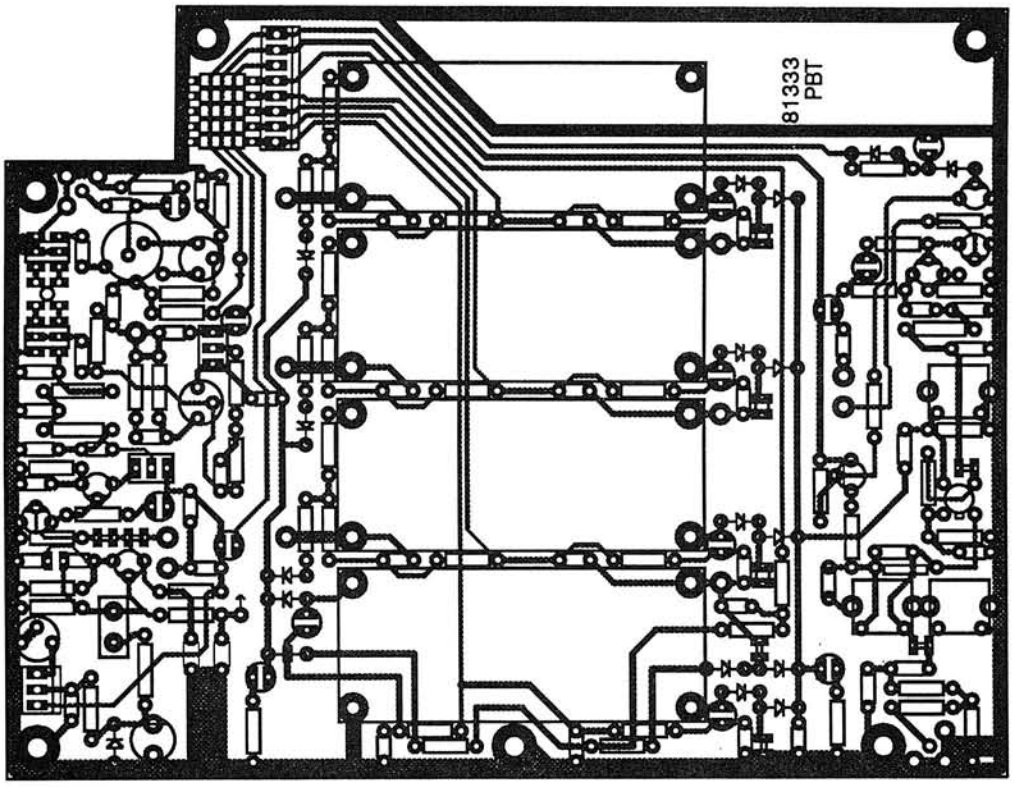


FIGURE 6-14. 81333 PASS BAND TUNING BOARD CIRCUIT TRACE

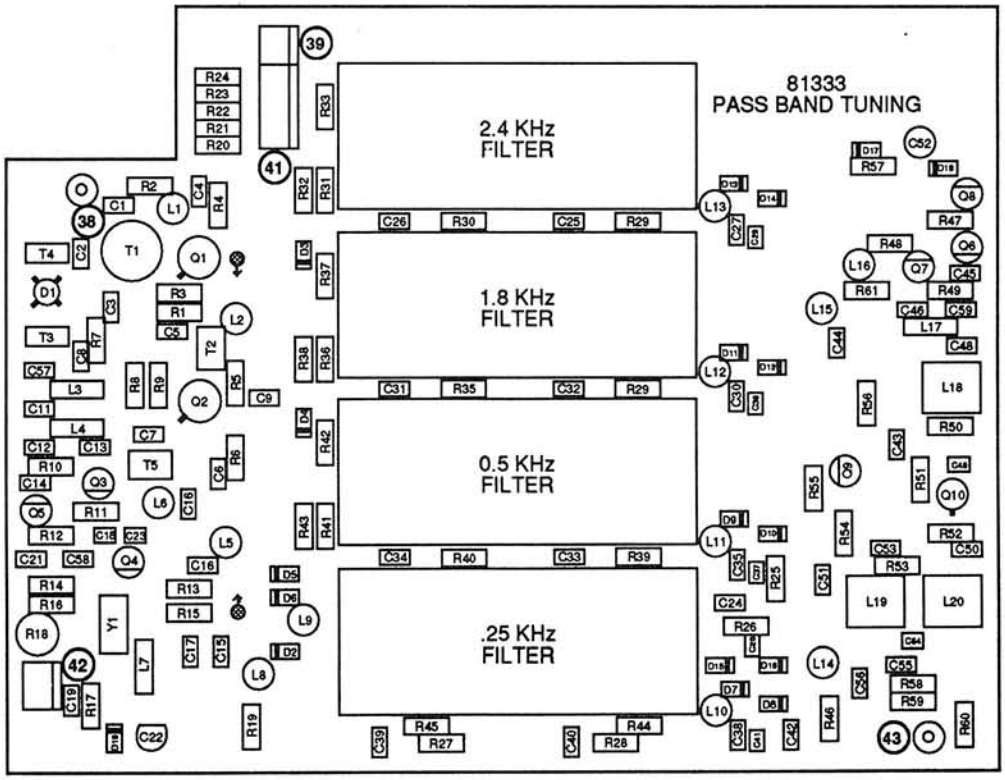
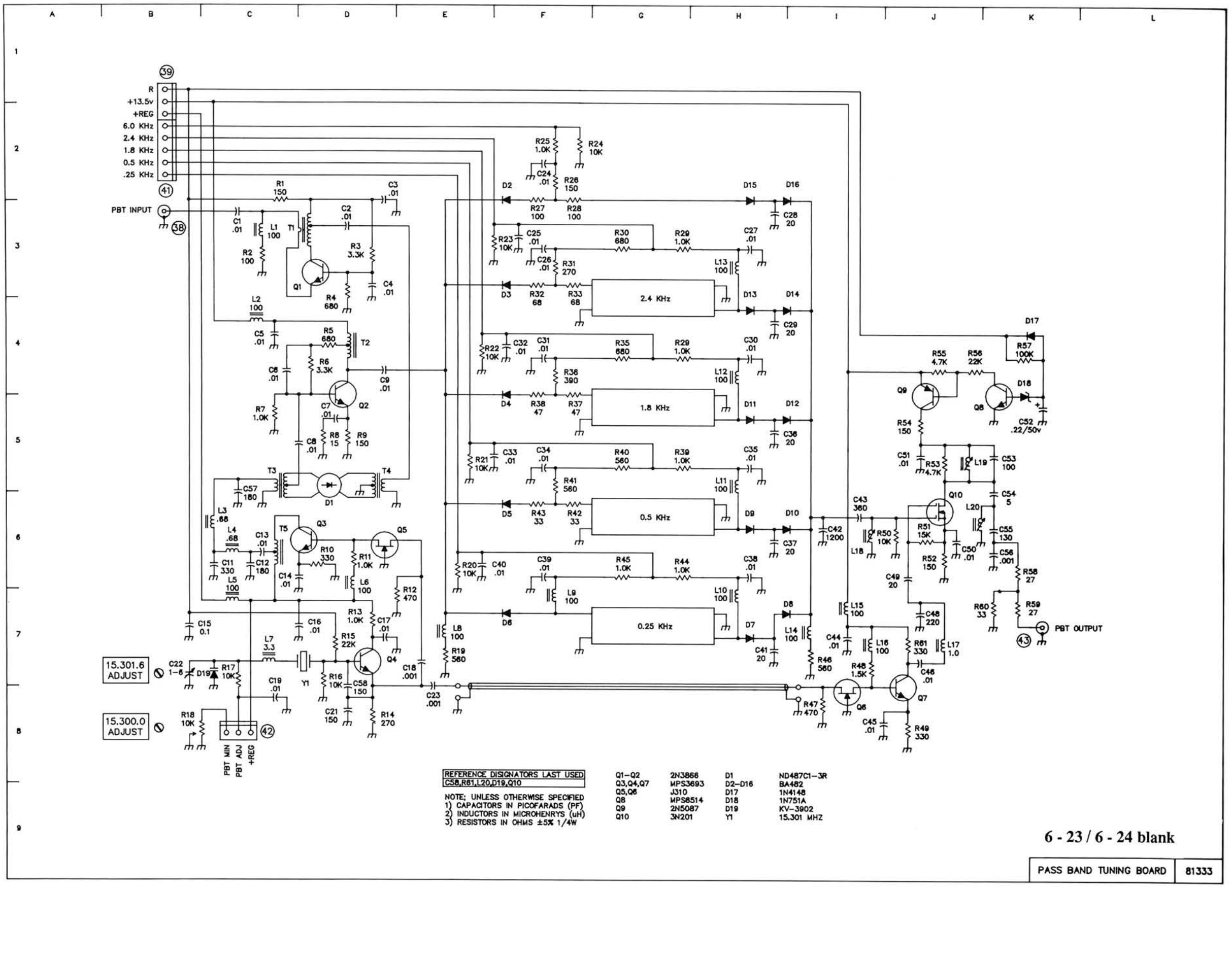


FIGURE 6-15. 81333 PASS BAND TUNING BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
C58,R61,L20,D19,Q10

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

Q1-Q2	2N3866	D1	ND487C1-3R
Q3,Q4,Q7	MPS3693	D2-D16	BA482
Q5,Q6	J310	D17	1N4148
Q8	MPS8514	D18	1N751A
Q9	2N5087	D19	KV-3902
Q10	3N201	Y1	15.301 MHZ

6 - 23 / 6 - 24 blank

PASS BAND TUNING BOARD | 81333

6-7 IF / AF BOARD (81334)

The IF/AF board contains the 9 MHz IF amplifier stages that contribute the major portion of the receiver gain. It also contains the SSB/CW and AM detectors, AGC circuits, audio notch and bandpass filters, audio amplifier, and speaker driver.

The 9 MHz IF signal from the passband tuning board enters at connector 43 and is amplified by grounded gate FET Q1, integrated circuit IF amplifiers U1 and U2, and emitter follower Q3. The output of Q3 splits three ways. One output drives AGC detector D4-D6, to develop an AGC voltage across capacitor C45. Through connector 49, the front panel AGC FAST/SLOW switch connects additional AGC holding capacitor C46 in parallel with C45 in the SLOW position, and the AGC ON/OFF switch shorts the AGC voltage to ground in the OFF position. U9b amplifies and level shifts the AGC voltage and, through D8, applies it to the gain control pins of U1 and U2 and the base of PIN diode driver Q2. Shunt PIN diode D1 attenuates the IF signal at the input to U1 when the amplified AGC voltage exceeds the threshold set by zener diode D2. The front panel RF GAIN control at connector 50 can reduce receiver gain by raising the AGC control line voltage through Q7 and D12.

The AGC voltage across C45 is also amplified and level shifted by S-meter amplifier U9a and split three ways: to the S-meter through D11 and R57, to front end AGC diodes on the 1st mixer board via connector 19, and to the squelch circuit Q8-Q10. In the squelch circuit, the output of U9a is compared to the voltage across the front panel SQUELCH control at connector 50. When the output of U9a is less than the voltage set by the SQUELCH control at the base of Q8, Q10 and D9 are forward biased, saturating audio clamp transistor Q12, and muting the receiver audio. A mute voltage from control board connector 44 also saturates Q12 during transmit and for a short period after transmit as determined by C64-C65-R89 and the front panel QSK switch at connector 48.

Another output from emitter follower Q3 drives AM IF amplifier Q5 and AM detector Q4. The detected AM output of Q4 is filtered by C33, C34, and R32 and applied to one section of audio switch U4.

The last output from Q3 is via C20 to product detector U3. The approximately 9 MHz BFO input to the product detector comes from the transmit audio/BFO board via connector 46. The detected SSB/CW/RTTY output from the product detector is filtered by C26, C27, and R17 and applied to a section of audio switch U4.

Based on inputs from the control board on connector 51, audio switch U4 selects an audio signal from the product detector in SSB/CW/RTTY mode, the AM detector in AM mode, or the FM option board at connector U in FM mode. The output of U4 drives notch filter circuit U5. The frequency of the audio notch is determined by the clock frequency input to U5 which is developed by notch clock circuit U6. The frequency of notch clock U6 is set by the front panel NOTCH control via connector 53. The frequency range of the notch clock is approximately 27-210 KHz resulting in an audio notch frequency range of 540-4200 Hz. The output of notch filter U5 drives the audio bandpass filter circuits U7 and U8 through C42, and one side of the front panel FADE control through C43 and connector 55. Q11 samples a portion of this "flat" audio and outputs it to the rear panel AUDIO OUT jack via connector 56 and the transmit audio board.

The center frequency of the audio bandpass filter is determined by the voltage applied to R71 and R84 by the front panel BP control via connector 54. The center frequency range of the bandpass filter is approximately 220-1700 Hz, and the 6 dB bandwidth is always 35% of the center frequency. Bandpass fil-

tered audio output from U8 is routed to one side of the front panel FADE control through C52 and connector 55.

On the upper pot board, the unfiltered (flat) audio from C43 and the bandpass filtered audio from C52 are combined in proportions determined by the setting of the front panel FADE control. Clockwise rotation of the control increases the filtered portion and decreases the unfiltered portion of audio delivered to audio amplifier U10a through connector 55, R91 and C57. When the squelch is "closed", clamp transistor Q12 is saturated, shunting all receiver audio to ground. Unsquelched receive audio (or transmit audio from sidetone connector 57) is amplified by U10a and applied to the clockwise end of the front panel TONE control vi connector 55. The counter-clockwise end of the control returns through connector 55 to the input of speaker driver U10b. C54 shunts the wiper of the control to ground, forming a "high-cut" tone control. Cable 47 connects the speaker driver output to the front panel PHONES jack and the rear panel EXT SPKR jack. Cable 76 carries it from there to the sidetone board, cable 77, and the internal speaker.

Cable 55/45 from the control board supplies +13.5 Volt power to U10 and "+REG" to all remaining circuitry.

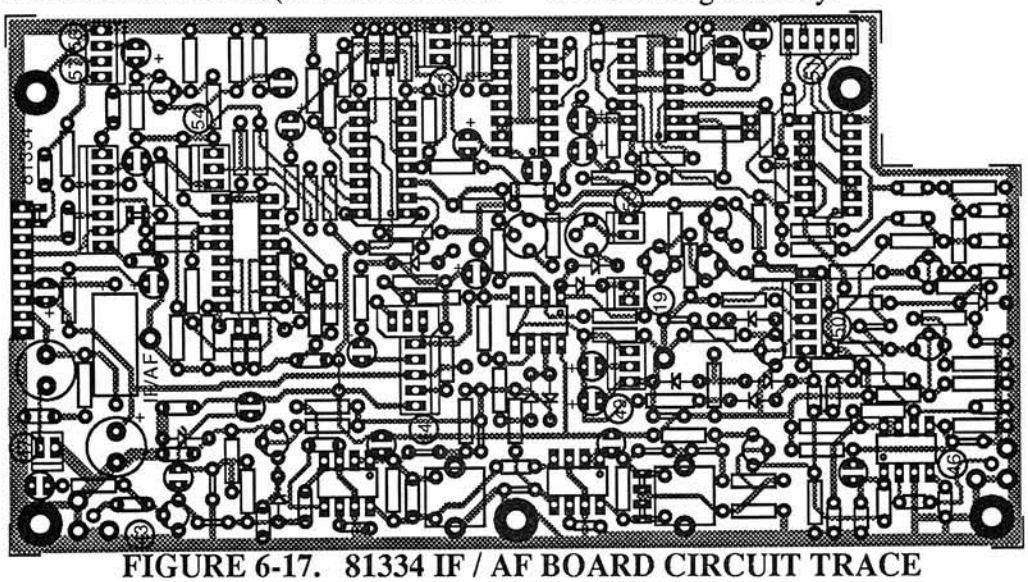


FIGURE 6-17. 81334 IF / AF BOARD CIRCUIT TRACE

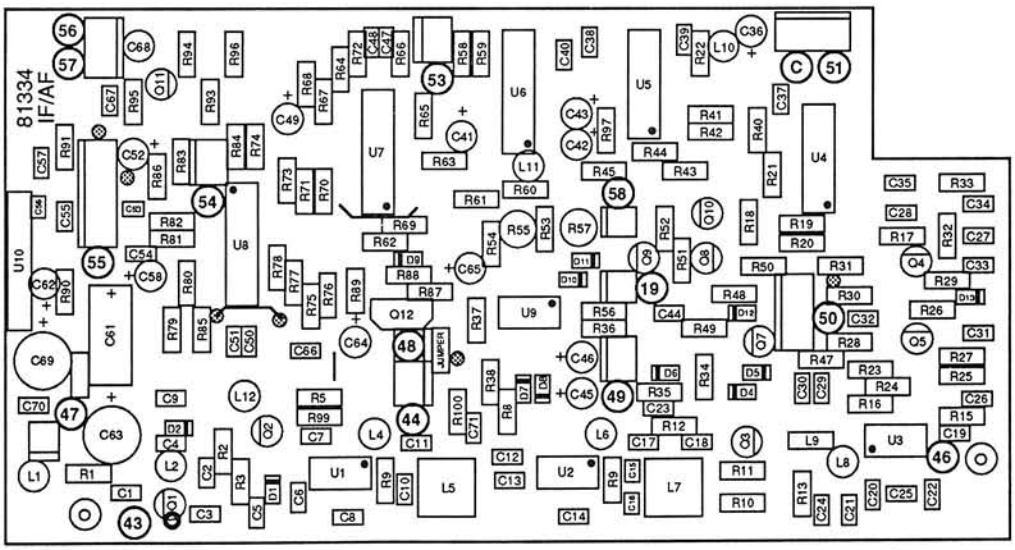
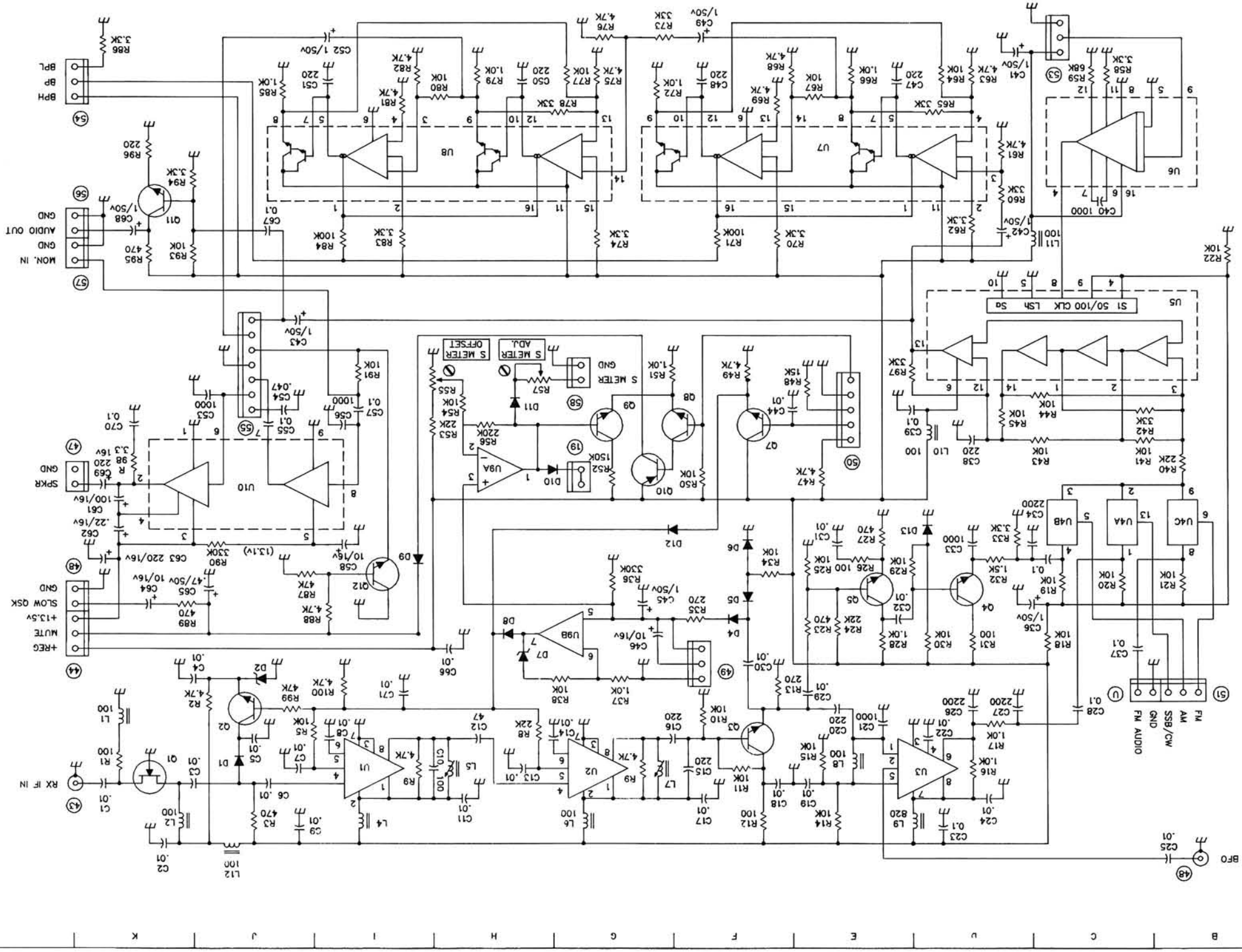


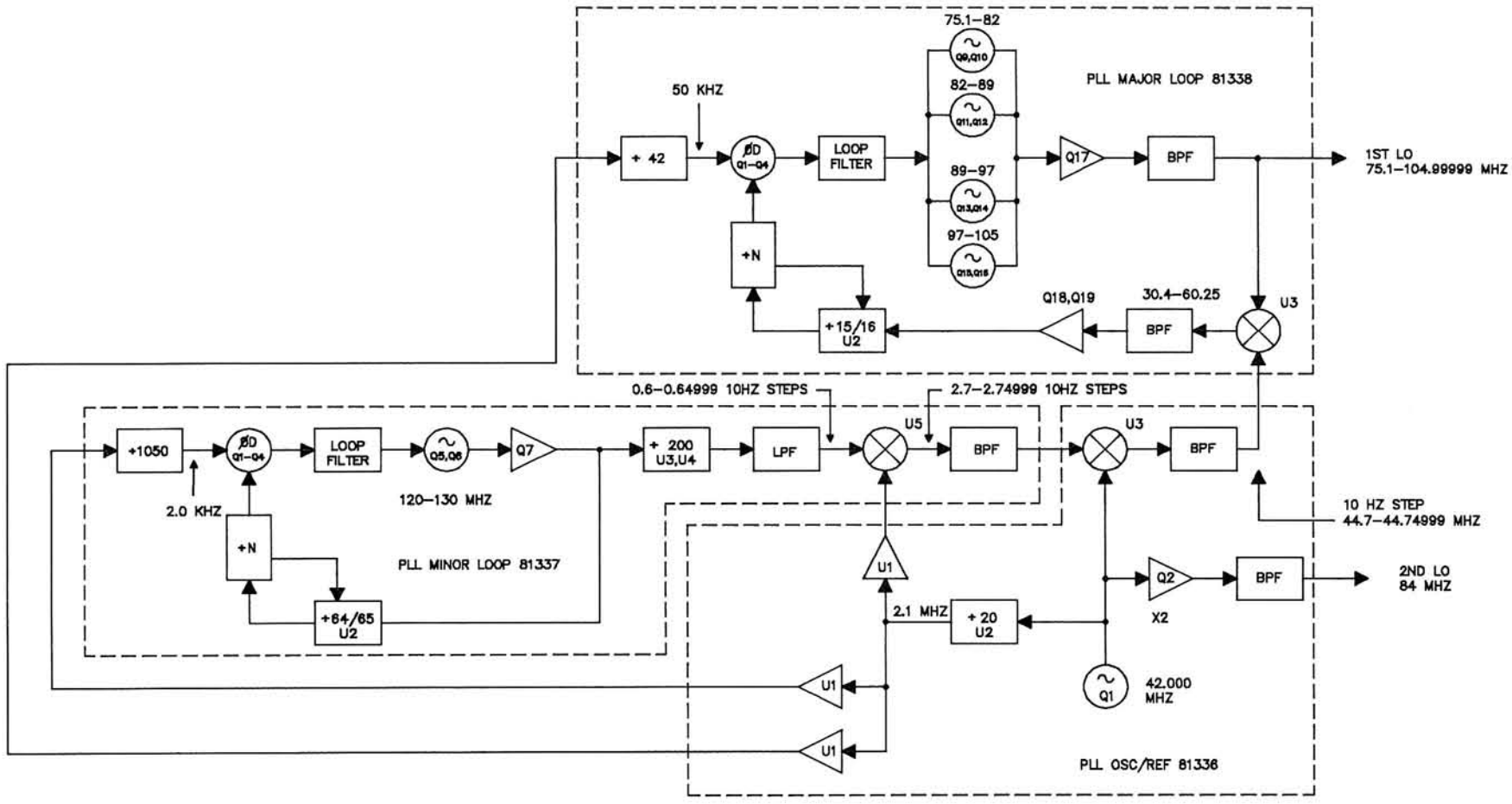
FIGURE 6-18. 81334 IF / AF BOARD COMPONENT LAYOUT

NOTE: UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (UH)
3) RESISTORS IN OHMS ±5% 1/4W

REFERENCE DISIGNATORS LAST USED
R100,C71,L12,D13,Q12,U10

U1,U2	MC1350P	Q1	J310	D1	HP 3379
U3	CA3053E	Q2,Q4,Q5	MPS6514	D2-D7	1N748A
U4	CD4066BE	Q7,Q9,Q11	MPS6514	D4,D5	1N4148
U5	MFSCN	Q3	MPS3693	D8-D13	1N4148
U6	CD4046BE	Q10	2N5087	D6	BAT41
U7,U8	LM1360N	Q12	MPSU01		
U9	LM358N				
U10	TDA1015				





PLL BLOCK DIAGRAM

6-8 PHASE LOCKED LOOP BLOCK DIAGRAM

The phase locked loop subsystem is responsible for generating the variable first local oscillator injection frequency of 75.1-105 MHz in 10 Hz steps, and the fixed second local oscillator signal of 84 MHz. The frequency accuracy of these signals is determined by a crystal controlled 42 MHz master oscillator on the PLL reference oscillator board.

The fine resolution steps of 10 Hz for the 1st LO are developed by the minor loop board. In the minor loop, a VCO covering the frequency range of 120-130 MHz is phase locked to a 2 KHz reference obtained by dividing a 2.1 MHz output of the reference oscillator board by 1050. This produces an output of 120-130 MHz with 2 KHz resolution, which is then divided by 200 to produce 0.6-0.65 MHz in 10 Hz steps. This 0.6-0.65 MHz signal is mixed with another 2.1 MHz output from the reference oscillator board to produce the 2.7-2.75 MHz minor loop output with 10 Hz resolution.

The 2.7-2.75 MHz output from the minor loop board is translated again on the reference oscillator board by mixing with the 42 MHz master oscillator signal to produce an output to the PLL major loop board of 44.7-44.75 MHz in 10 Hz steps.

The PLL major loop board is a mixing loop in which the difference between a VCO operating in the range of 75.1-105 MHz and the 44.7-44.75 MHz output from the reference oscillator board is phase locked to a 50 KHz reference. The 50 KHz reference is developed by dividing a 2.1 MHz output from the reference oscillator board by 42. Although the major loop step size is 50 KHz as set by the 50 KHz reference, the final major loop output of 75.1-105 MHz moves in 10 Hz steps as determined by the 44.7 to 44.75 MHz from the minor loop. Four VCOs are used to cover the 75.1-105 MHz range to keep noise and microphonics to acceptable levels.

On the reference oscillator board, the 42 MHz master oscillator signal is passed through a frequency doubler and filter to form the second LO injection of 84 MHz.

6-9 REFERENCE OSCILLATOR (81336)

This board contains the 42 MHz master oscillator that determines the accuracy of the 1st and 2nd local oscillator injection frequencies. The 42 MHz oscillator output is divided by 20 to form a 2.1 Mhz reference signal which is used by the PLL boards to develop the 1st LO. The 42 MHz signal is doubled to produce the 84 MHz 2nd LO. This board also contains a mixer and filter circuit which converts the PLL minor loop signal of 2.7-2.75 MHz up to 44.7-44.75 MHz for use by the PLL major loop.

Q1 and third overtone crystal Y1 form a crystal controlled Colpitts oscillator stage. Trimmer C1 is provided for setting the oscillator output frequency to exactly 42 MHz. Center tapped transformer T2, diodes D1-D2, and Q2 form a push-push doubler and amplifier chain which develops the 84 MHz 2nd LO frequency. L6-L8 and C13-C17 form a triple-tuned band pass filter which cleans up the 84 MHz signal before it is sent to the 2nd mixer via connector 27.

C8 and L5 form a low pass network which couples some of the 42 MHz oscillator output into frequency divider U2 and double balanced mixer U3 while rejecting any 84 MHz second harmonic produced in the doubler diodes D1 and D2. U2 divides this 42 MHz input by 20 to form a 2.1 MHz reference signal which is distributed to the PLL boards by buffers U1 via connectors 85, 86 and 88.

U3 mixes its 42 MHz input with the PLL minor loop input of 2.7-2.75 MHz from connector 87 to produce an output of 44.7-44.75 MHz. This signal is filtered by the triple-tuned network of L10-L12 and C33-C37 before being sent to the PLL major loop via connector 89.

13.5 Vdc power from connector 3 is regulated to 10.4 Volts for the voltage sensitive oscillator and balanced mixer stages by U4 and Q3. Dropping resistor R13 and Zener Diode D3 provide 5 Volts power to U1 and U2.

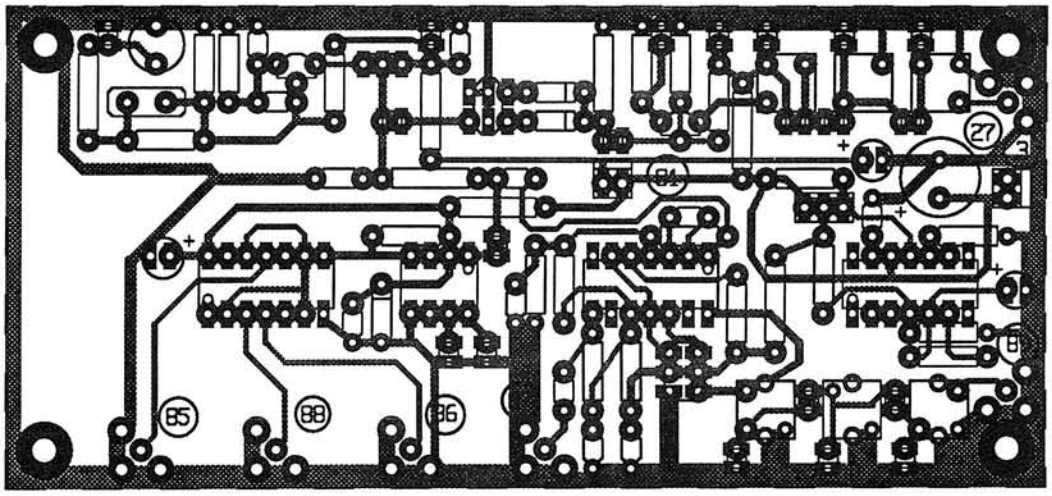


FIGURE 6-21. 81336 REFERENCE OSCILLATOR CIRCUIT TRACE

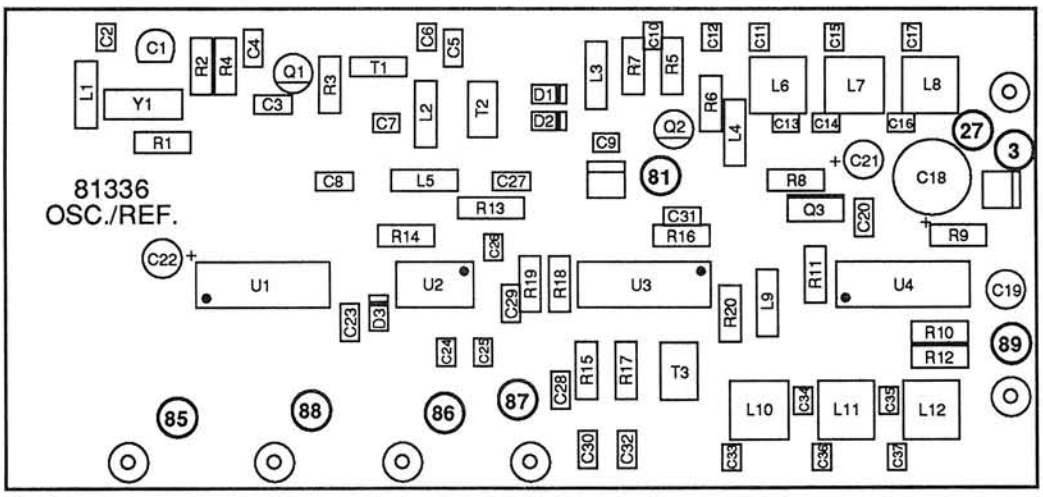
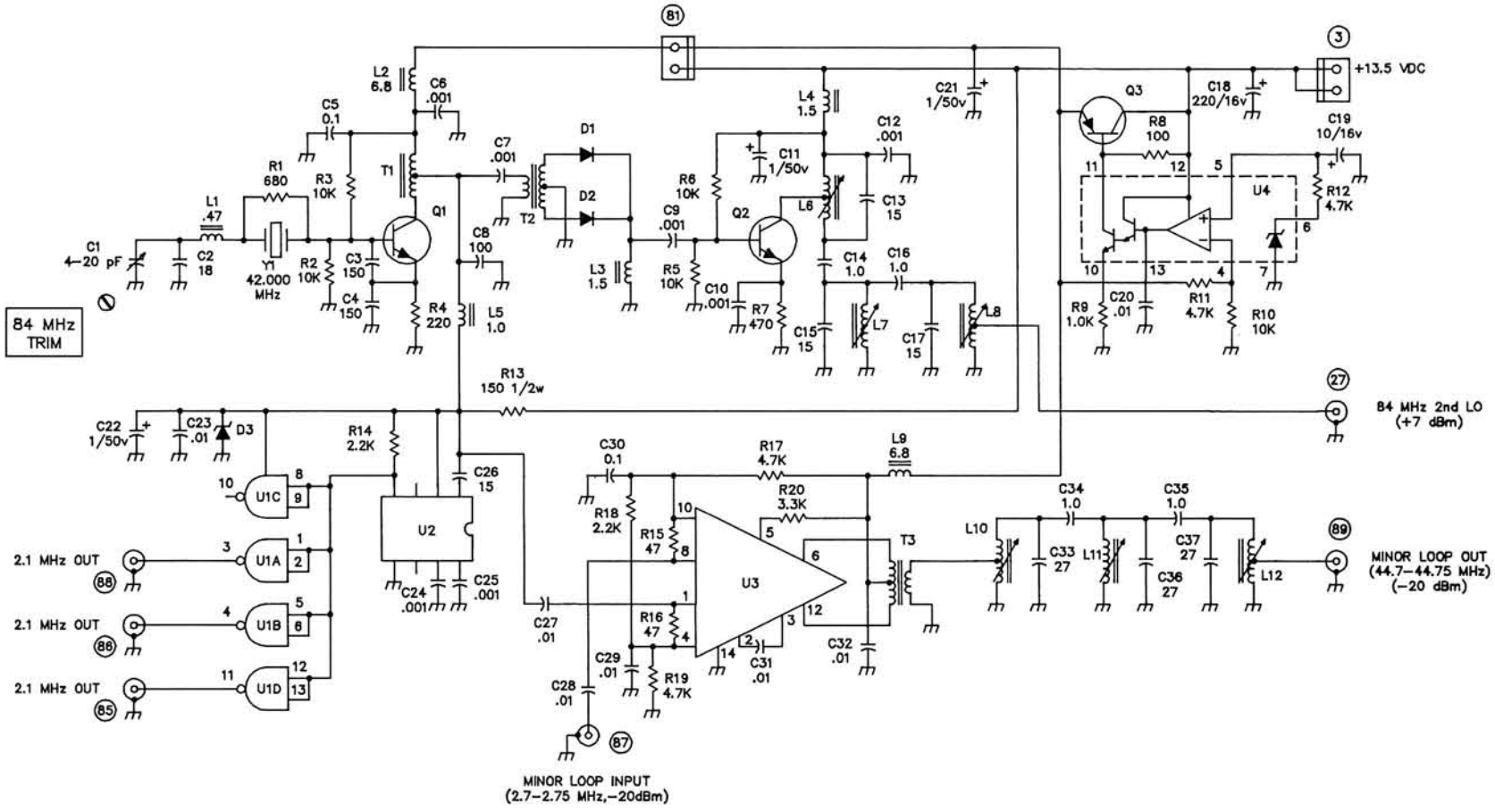


FIGURE 6-22. 81336 REFERENCE OSCILLATOR COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R20,C37,L12,Q3,U4,Y1

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1	MC14011BPC
U2	MC3396P
U3	MC1496P
U4	MC1723P
Q1-Q2	MPS5179
Q3	MJE370
D1-D2	IN4148
D3	IN751A

6 - 33 / 6 - 34 blank

PLL OSCILLATOR/REFERENCE	81336

6-10 PLL MAJOR LOOP BOARD (81338)

The PLL major loop board is a mixing loop in which the difference between a VCO operating in the range of 75.1-105 MHz and the 44.7-44.75 MHz minor loop output is phase locked to a 50 KHz reference. Although the major loop step size is 50 KHz as set by the 50 KHz reference, the final major loop output of 75.1-105 MHz moves in 10 Hz steps as determined by the 44.7 to 44.75 MHz from the minor loop. Four VCOs are used to cover the 75.1-105 MHz range to keep noise and microphonics to acceptable levels. Serial programming from the logic board (by way of the minor loop board) and VCO select lines from the control filter board are received on connectors 83 and 90 respectively. Power inputs and loop unlock output connect to the minor loop board through connector 82. The 2.1 MHz reference signal and the 44.7-44.75 MHz minor loop signal come from the reference oscillator board on connectors 88 and 89 respectively. The 75.1-105 MHz 1st LO signal is output to the first mixer board on connector 26.

PLL circuit U1 performs the functions of reference divider, programmable counter, and phase detector. The reference divider is programmed by the microprocessor to a fixed divide ratio of 42 which, assuming 2.1 MHz input from the reference oscillator board at connector 88, results in a 50 KHz reference to the phase detector. The programmable counter is programmed to a number based on the operating frequency which, in conjunction with prescaler U2, results in dividing the mixer output from Q19 down to 50 KHz for the other phase detector input. U2 is a dual modulus prescaler which extends the frequency range and resolution of the programmable counter in U1. Based on the phase and frequency difference between the divided down signals from reference connector 88 and the mixer output from Q19, the phase detector in U1 drives charge pump circuit Q1-Q4 to add or subtract charge from the loop filter capacitors C9-C11. A low voltage on one of four VCO select lines at connector 90 activates a VCO which operates on a frequency determined by the loop filter voltage across tuning diodes D10-D13. The selected VCO forward biases one of the diode switches D6-D9 to drive buffer amplifier Q17. The output of Q17 in the frequency range of 75.1-105 MHz is cleaned up by bandpass filter C31-C35, L20-L24 and becomes the 1st LO injection to the first mixer board at connector 26. A sample of this output is mixed with the minor loop output at connector 89 by double balanced mixer U3 and the difference frequency output is selected by bandpass filter C42-C46, L6-L10. This difference frequency of 30.4-60.25 MHz passes through broad band amplifiers Q18 and Q19 to drive prescaler U2, thus closing the loop.

13.5 Volt power from minor loop connector 82 is reduced to 5 Volts by R7 and D1 to supply U1 and U2. A voltage regulator on the reference oscillator board supplies 10.4 Volts regulated via minor loop connectors 81 and 82 for the remaining circuitry on this board.

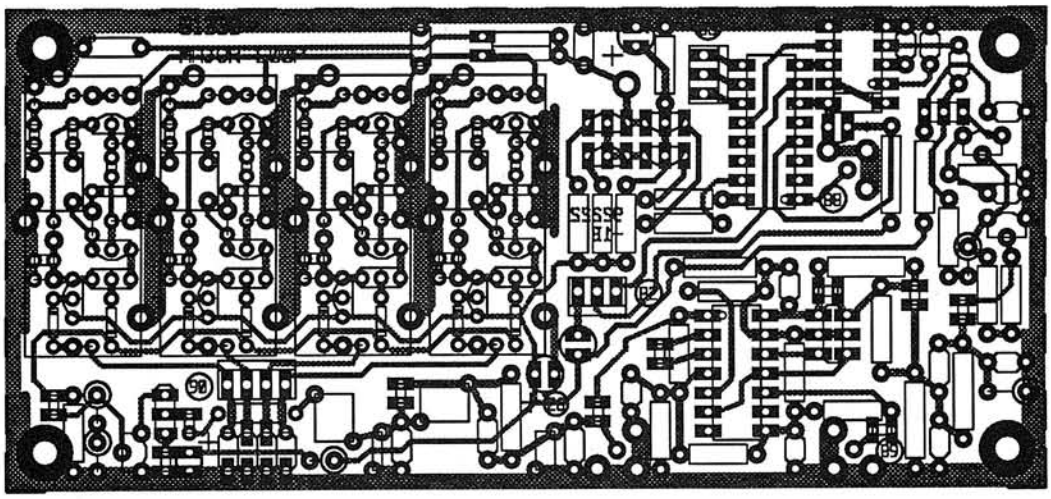


FIGURE 6-24. 81338 MAJOR LOOP BOARD CIRCUIT TRACE

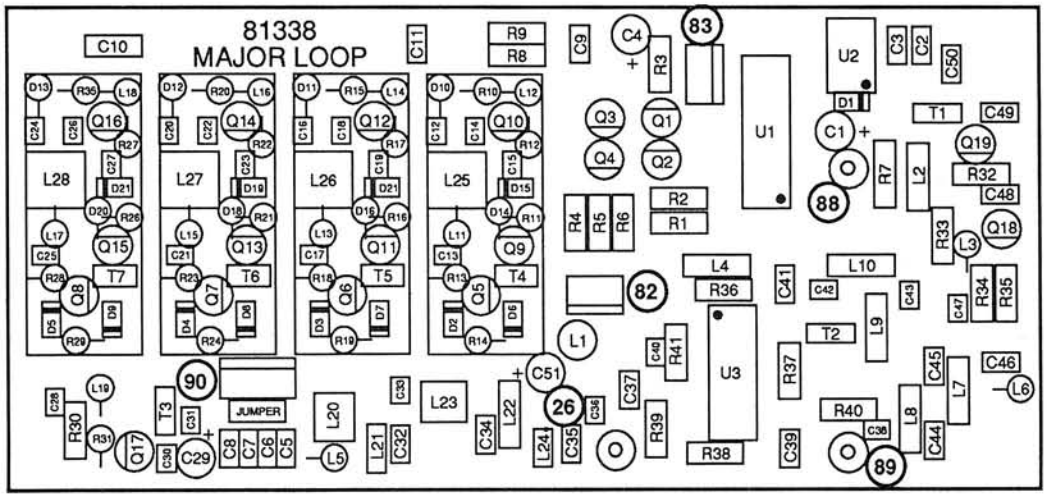
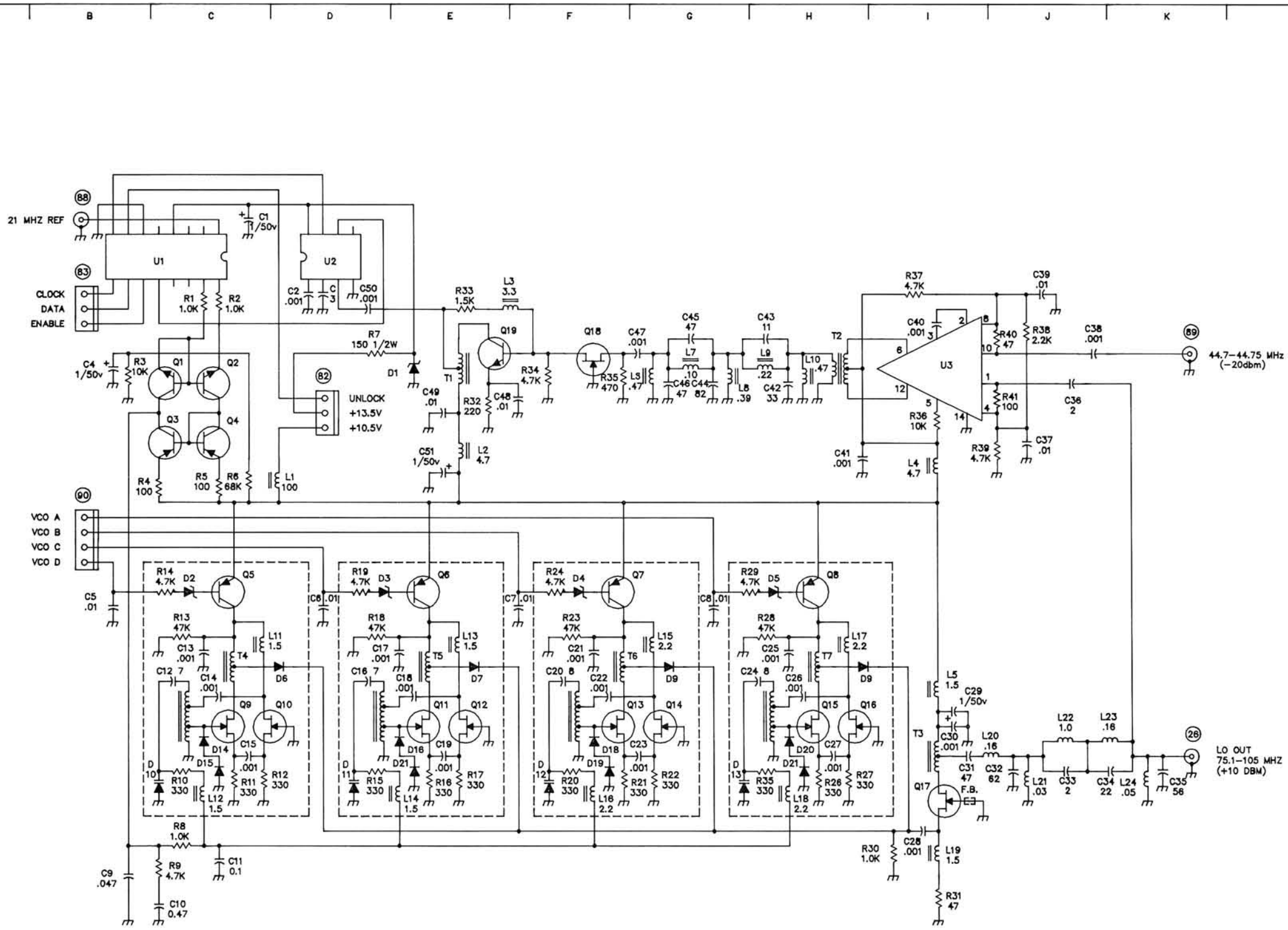


FIGURE 6-25. 81338 MAJOR LOOP BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R41,C51,L24,Q19,U3,D21

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1	:	MC145158P	D2-D5	:	1N754A	Q1,Q2	:	MPS6514
U2	:	MC3393P	D6-D9	:	BAT41	Q3-Q8	:	2N5087
U3	:	MC1496P	D10-D13	:	KV-3902	Q9-Q18	:	J310
D1	:	1N751A	D14-D21	:	1N4148	Q19	:	MPS5179

6 - 37 / 6 - 38 blank

MAJOR LOOP	81338

6-11 PLL MINOR LOOP BOARD (81337)

The minor loop develops the fine resolution 10 Hz steps of the synthesizer by dividing the output of a 2 KHz resolution phase locked loop by 200. The 2 KHz minor loop VCO operates in the frequency range of 120-130 MHz resulting in a divided down output range of 600-650 KHz. This 50 KHz range fills in the gaps between the 50 KHz steps of the major loop providing an overall resolution of 10 Hz for the synthesizer. The 600-650 KHz signal is translated upward twice by mixing first with 2.1 MHz from connector 86 and then (via connector 87) with 42 MHz on the reference oscillator board to become the 44.7-44.75 MHz minor loop input to major loop board connector 89.

PLL circuit U1 performs the functions of reference divider, programmable counter, and phase detector. The reference divider is programmed by the microprocessor to a fixed divide ratio of 1050 which, assuming 2.1 MHz input from the reference oscillator board at connector 85, results in a 2 KHz reference to the phase detector. The programmable counter is programmed to a number based on the operating frequency which, in conjunction with prescaler U2, results in dividing the VCO output from Q7 down to 2 KHz for the other phase detector input. U2 is a dual modulus prescaler which extends the frequency range and resolution of the programmable counter in U1. Based on the phase and frequency difference between the divided down signals from reference connector 85 and VCO output from Q7, the phase detector in U1 drives charge pump circuit Q1-Q4 to add or subtract charge from loop filter capacitors C1 and C2, determining the voltage across tuning diode D1 and the operating frequency of the VCO, Q5-Q6. VCO buffer Q7 drives two prescalers through lowpass network C10-C11 and L11: U2 which closes the phase locked loop, and the U3-U4 combination which performs a fixed division by 200.

The output of U4, after lowpass filtering by C20-24, L9-10, has a step size of 10 Hz, but at 600-650 KHz its frequency is too low to be easily mixed with the major loop output of 75-105 MHz. It is therefore translated up in frequency by mixing with 2.1 MHz from the reference oscillator board connector 86 in double balanced mixer U5. The sum frequency output of U5 at 2.7-2.75 MHz is selected by bandpass filter C32-38, L11-13 and sent to the reference oscillator board via connector 87 for further translation to 44.7-44.75 MHz. This signal, still with 10 Hz resolution, is finally routed to the minor loop input of the major loop board at connector 89.

PLL circuit U1 provides an active low out of lock signal through R22 to out of lock detector circuit Q8-10. When the base of Q1 is pulsed low, Q10 is forward biased producing an active low synthesizer out of lock signal to the logic board via connector 84. Similar circuitry around Q9 conditions out of lock pulses from the major loop at connector 82, again forward biasing Q10 during an out of lock condition.

13.5 Volts from connector 81 is reduced to 5 Volts power for U1-U4 by shunt regulator R13-14 and D2. A regulator on the reference oscillator board provides 10.5 Volts power to the remaining circuitry and to the major loop board via connectors 81 and 82.

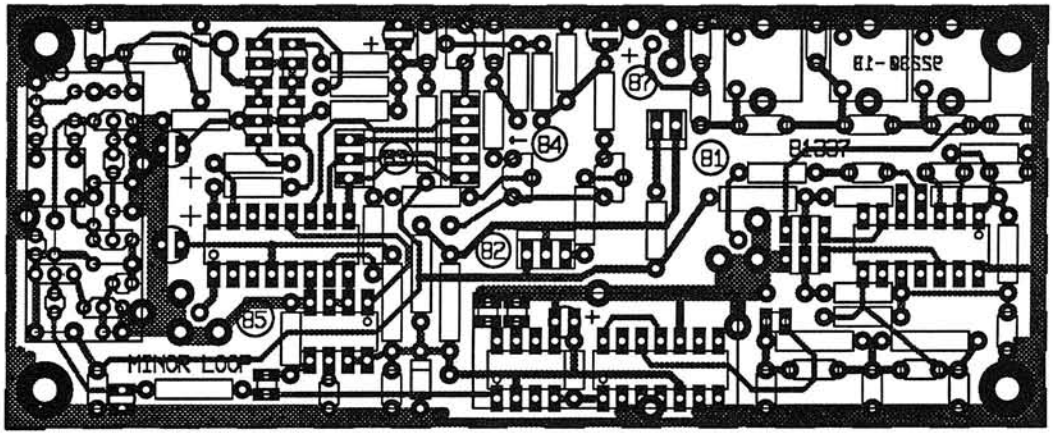


FIGURE 6-27. 81337 MINOR LOOP BOARD CIRCUIT TRACE

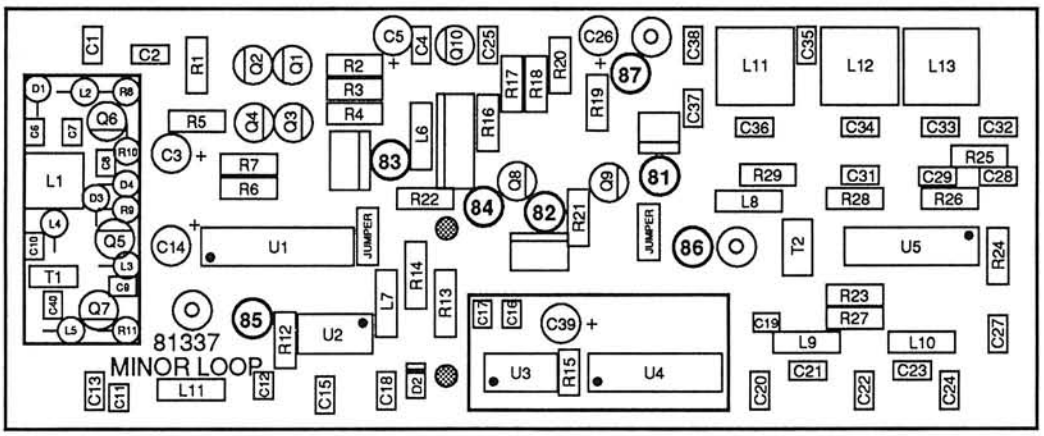
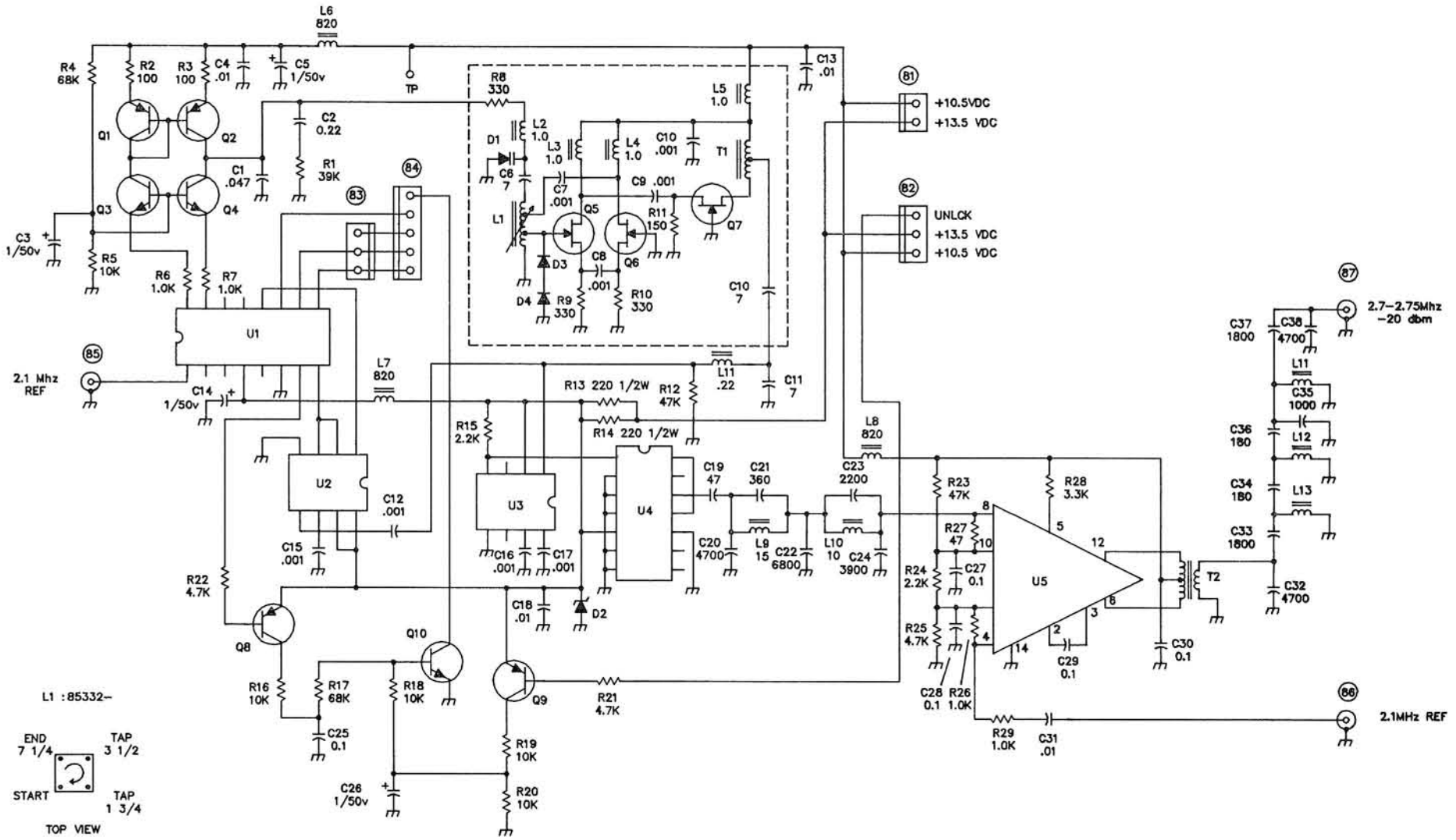


FIGURE 6-28. 81337 MINOR LOOP BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R28,C38,L13,Q10,U5,D4

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1 – MC145158P
U2 – MC12017P
CA3232E
U4 – 74LS90
U5 – MC1496P

D1 – KV3902
D2 –1N751A
D3,D4– 1N4148

Q1,Q2,Q8,Q9 – 2N5087
Q3,Q4,Q10 – MPS6514
Q5,Q6,Q7 – J310

6 - 41 / 6 - 42 blank

MINOR LOOP	81337

6-12 CONTROL BOARD (81335)

This board contains diode and transistor logic circuitry to develop control voltages based on inputs from the logic board, rear panel control jacks, or front panel switches, that determine the mode of operation (SSB, CW, transmit, receive, etc.) of the various circuits in the transceiver. It also contains the adjustable CW wave shaping circuit that sets the rise and fall times of the transmitted CW envelope, and the hold-in adjustment for the auxiliary T/R relay.

The main mode information from the microprocessor enters at connector 59. "T" voltage (indicating transmit mode) enters at connector 61 from the low level amplifier board. These inputs are combined in diode-transistor logic circuits D1-D15 and Q3-Q9 to form mode outputs to the IF/AF, second mixer, and transmit audio boards via connectors 51, 34, and 60.

A request to key the transmitter is generated by grounding the PTT (rear panel or microphone/VOX via switch board connector 65) or CW KEY lines, or a TUNE output from the logic board, which forward biases Q1, Q2, or D22, sending a high level to the microprocessor via connector 66 and, via D30 to the mute pin of IF/AF connector 45. The microprocessor buffers the transmit request and drives Q13, pulling the center pin of the rear panel TX OUT connector to ground. Normally the TX OUT connector is jumpered to the TX ENable connector and the low level from Q13 is passed directly to keying waveshape circuit Q14-Q17. An external keying interlock loop may be substituted for the jumper between TX OUT and TX ENable. Such an interlock may be used to prevent "hot switching" of a QSK linear amplifier, for example.

The keying waveshape circuit Q14-Q17 is an adjustable integrator that slows down the rise and fall times of the keying voltage "TD" which is sent to the T/R generator on the low level amplifier board via connector 61, and to the balanced modulator on the TX audio board via connector 60. CW waveshape adjustment R29 sets the keying rise and fall times in the range of 1-5 mS. This waveshaping has little effect on the T/R generator since its switching threshold is below 1 Volt. The balanced modulator, however, has a more gradual increase in gain as "TD" goes high, thus transferring the slowed rise and fall times to the transmitted keying waveform.

The buffered transmit request signal from the microprocessor at connector 66 also drives control relay RLY 1 via D24 and Q18 to provide a ground at the center pin of the rear panel RLY OUT connector during transmit. In CW mode, Q12 connects C8 into the circuit to hold Q18 and RLY 1 on between dits. This hold-in time is adjusted by the board mounted DELAY ADJUST pot R33.

An output from the collector of CW/RTTY keying transistor Q2 passes through R18, R19 and connector 63 to activate the CW sidetone oscillator on the sidetone board. Transistor Q10 clamps this output to ground to prevent sidetone generation in RTTY mode.

Cables 61/62, 40/39, 10/9, 21/20, 36/35, 45/44, and 5 distribute T, R, +REG, and +13.5 Volts to several boards. Wires in these cables are color coded as follows: T - blue, R - yellow, +REG - orange, +13.5 - red .

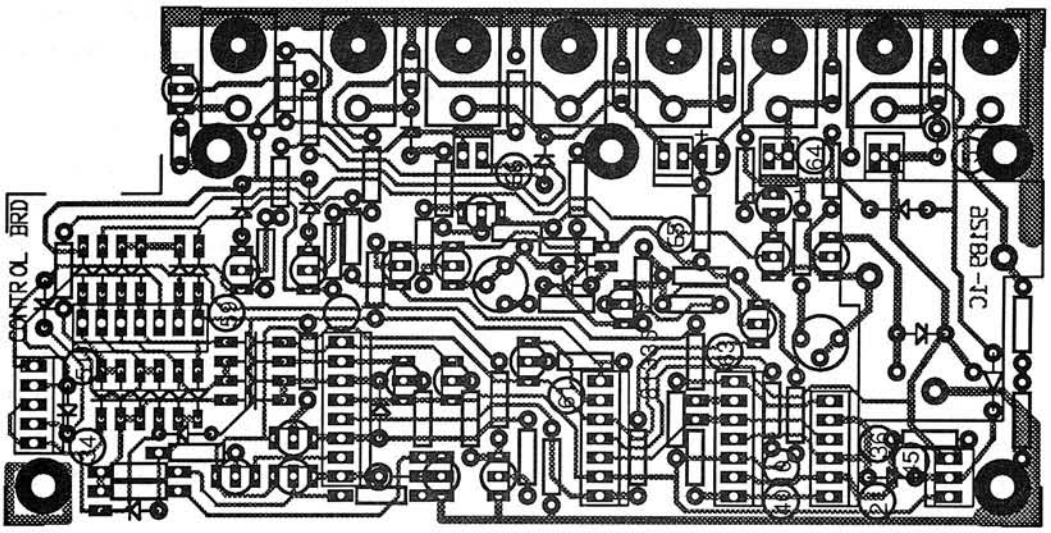


FIGURE 6-30. 81335 CONTROL BOARD CIRCUIT TRACE

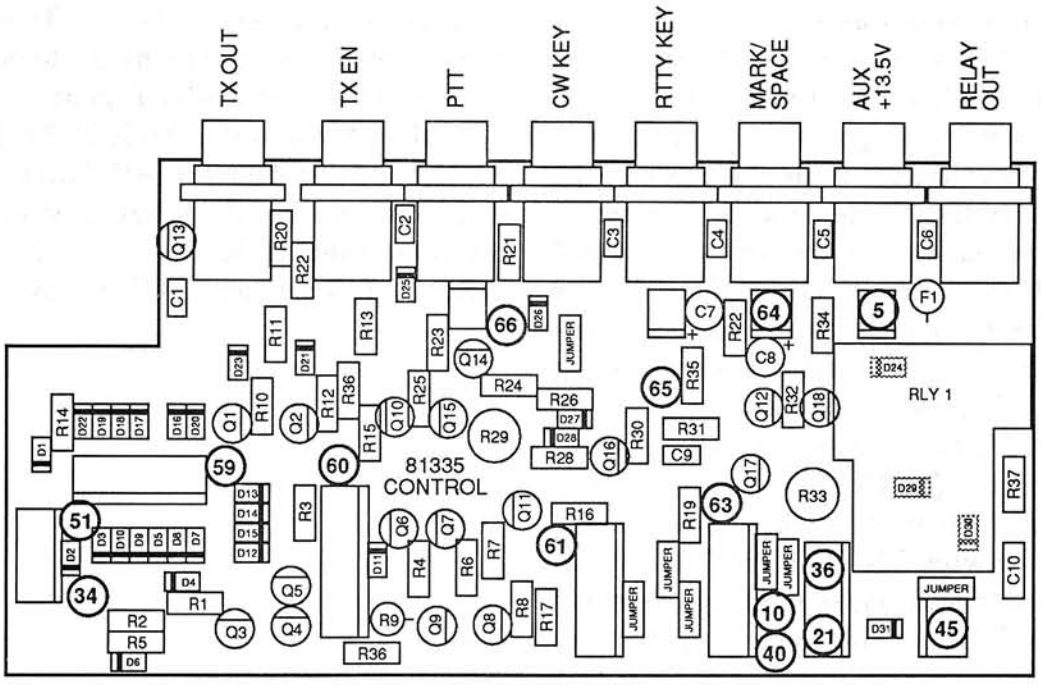
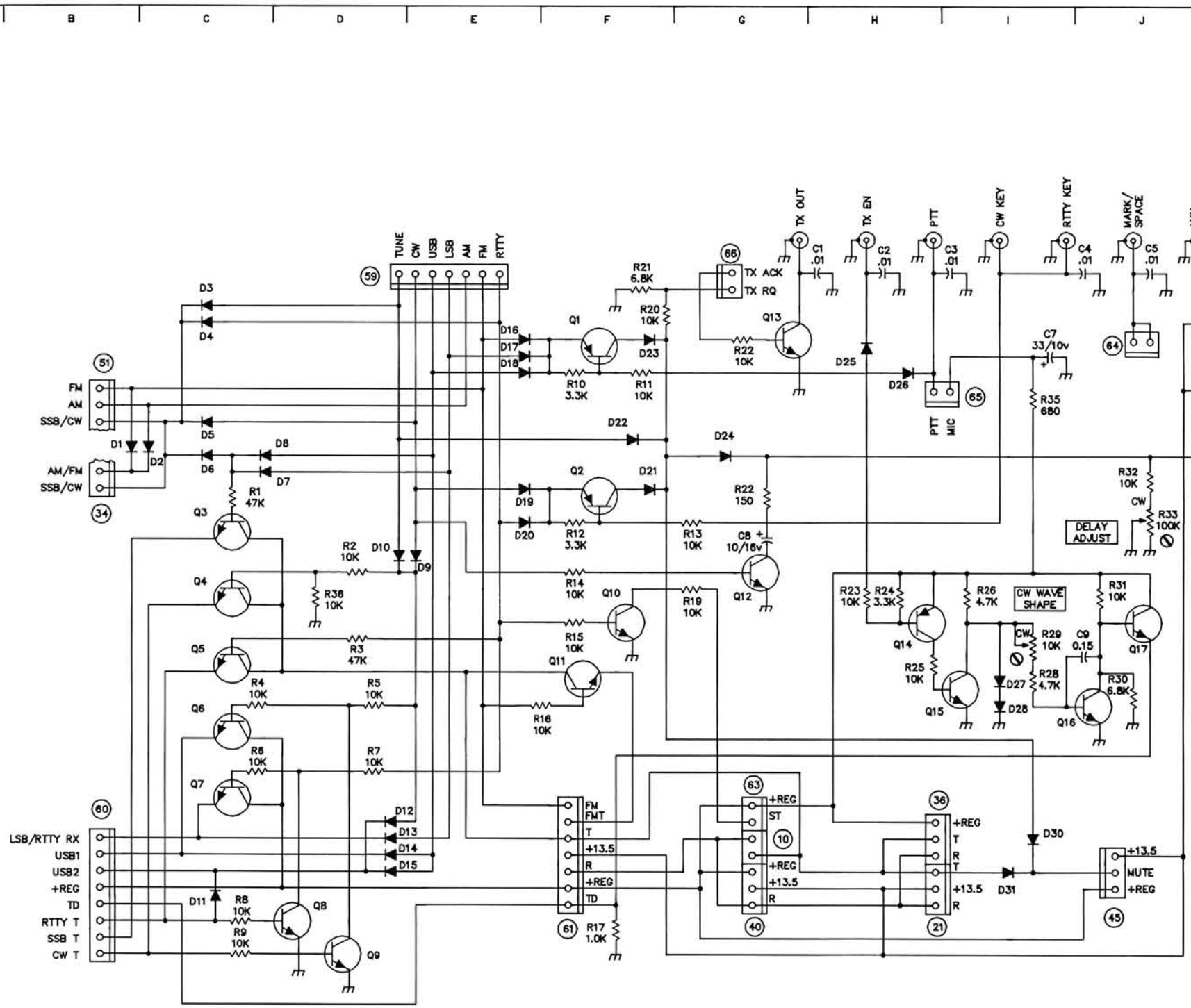


FIGURE 6-31. 81335 CONTROL BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R37,C10,D29,Q18

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

Q1,Q2,Q14	2N5087
Q3–Q13,Q15–Q17	MPS6514
Q18	MPSA13
D1–D29	1N4148
F1	2 AMP F.B.

6 - 45 / 6 - 46 blank

CONTROL BOARD	81335

6-13 SWITCH BOARD (81327)

The switch board contains five latching pushbutton switches which control the functions of Noise Blanker, VOX/PTT, QSK slow/fast, AGC on/off, and AGC fast/slow. This assembly is mounted on the left front subpanel just inboard of the main power switch.

Through connector 67, NB switch S1 feeds regulated voltage to the noise blanker pulse amplifier on the low level amplifier board enabling the noise blanker function.

VOX/PTT switch S2 selects the keying source to be sent to the control board via connector 65. Connector 69 carries the push to talk line and microphone polarizing voltage from the front panel MIC connector. The polarizing voltage loops directly to the control board connector 65, and the PTT line is switched to the control board when S2 is in the PTT position. When S2 is in the VOX position, the VOX output from the TX audio/BFO board at connector 68 is switched to connector 65 and the control board keying circuit.

In the slow position, QSK fast/slow switch S3 increases the recovery time of the mute circuit on the IF/AF board by connecting in additional capacitance via connector 48.

AGC off/on switch S4 disables the AGC circuit on the IF/AF board by grounding the AGC amplifier input through connector 49.

AGC fast/slow switch S5 increases the AGC decay time in the slow position by grounding the bottom end of an additional integrating capacitor in the AGC circuit.

FIGURE 6-33. 81327 SWITCH BOARD CIRCUIT TRACE

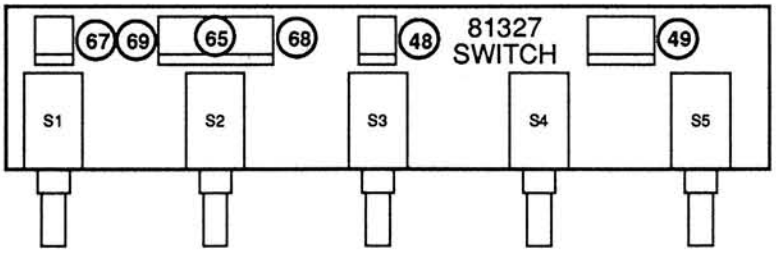


FIGURE 6-34. 81327 SWITCH BOARD COMPONENT LAYOUT

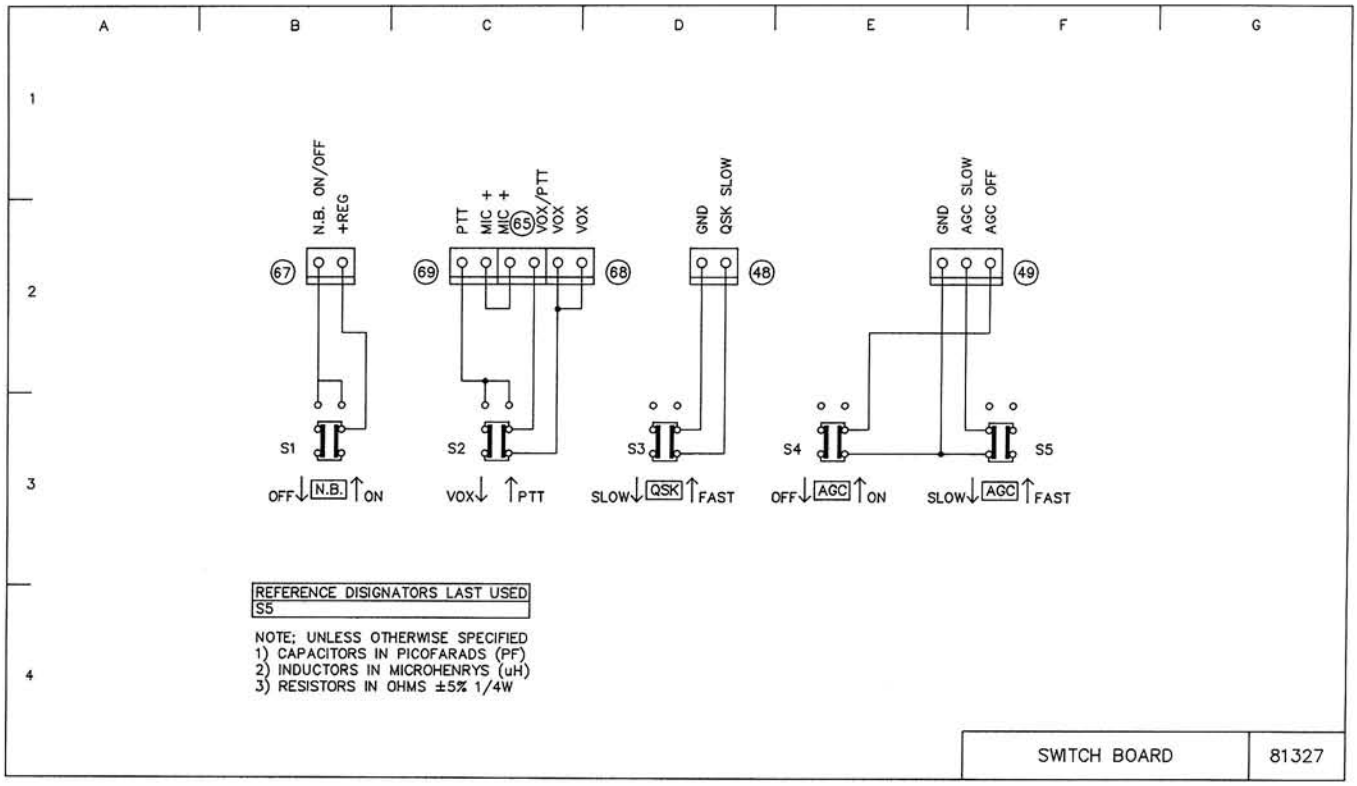


FIGURE 6-35. 81327 SWITCH BOARD SCHEMATIC

6-14 UPPER POT BOARD (81326)

This assembly contains three dual concentric controls, a latching pushbutton switch and a LED indicator. The board mounts on the left front subpanel at the control positions of AF GAIN and TONE, FADE and BP FILTER, PBT and NOTCH, and the ATTN switch.

The ATTN switch S1 is wired to the 1st mixer board by connector 18 where it controls the insertion of the receiver attenuator pad. When the pad is inserted, S1 applies 13.5 Volts to the anode of -20 dB indicator LED D1 which supplies a forward current through connector 18 to a dropping resistor on the 1st mixer board.

The AF GAIN control R5 forms a voltage divider at the output of fader network R1-R4 and R7 to select a controlled amount of audio signal for input to the audio amplifier on the IF/AF board via connector 55.

Unfiltered and filtered audio from the IF/AF board and connector 55 drive fader network resistors R1 and R2 respectively. The wiper of FADE control R7 is grounded through the center pin of connector 55 forming proportional voltage dividers with R1 and R2. The filtered and unfiltered portions are added together at the AF GAIN control R5 by summing resistors R3 and R4. Clockwise rotation of R7 increases the filtered portion and decreases the unfiltered portion of audio delivered to R5.

BP FILTER control R8 sets a dc voltage which determines the center frequency of the audio bandpass filter on the IF/AF board via connector 54. Clockwise rotation of the control increases the voltage at the center pin of connector 54 and increases the center frequency of the filter.

TONE control R6 is part of a "high cut" filter circuit between audio stages on the IF/AF board. Clockwise rotation of R6 reduces the amount of high frequency rolloff in the receive audio path.

NOTCH control R10, through connector 53 to the IF/AF board, varies a dc voltage to a clock oscillator which determines the frequency of the audio notch filter. Clockwise rotation of R10 increases the voltage at the center pin of connector 53, increasing the notch frequency.

The PBT control R9 connects to the passband tuning board through connector 42 where it controls the dc bias to the 15.3 MHz passband tuning VCXO. Clockwise rotation of R9 increases the voltage on the center pin of connector 42, increasing the frequency of the VCXO.

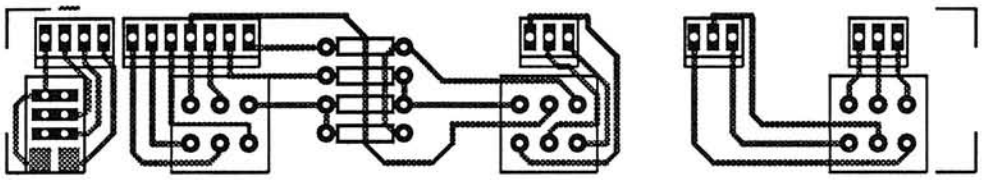


FIGURE 6-36. 81326 UPPER POT BOARD CIRCUIT TRACE

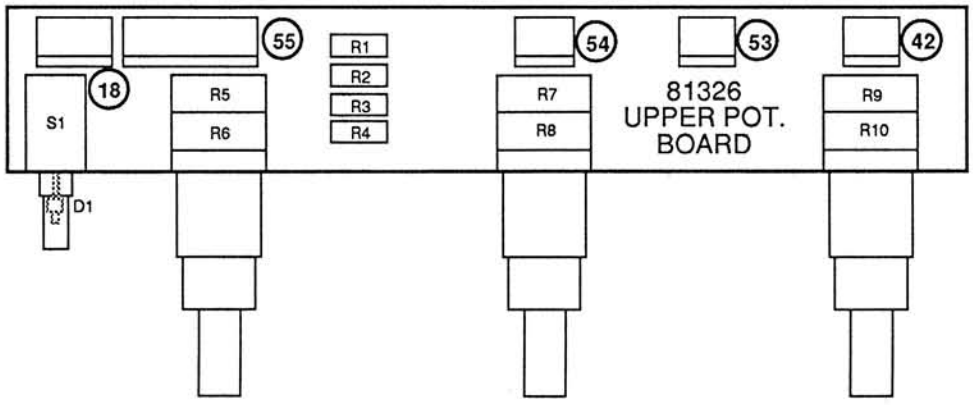


FIGURE 6-37. 81326 UPPER POT BOARD COMPONENT LAYOUT

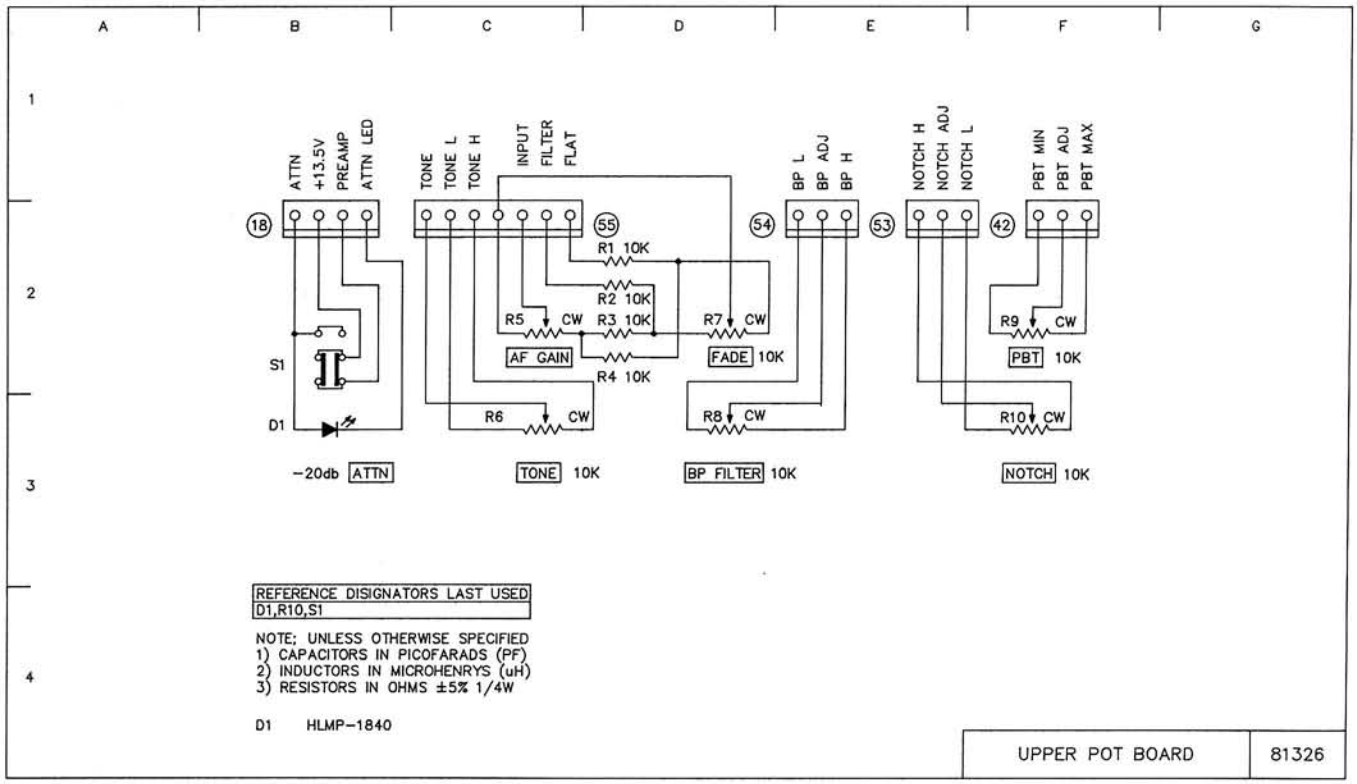


FIGURE 6-38. 81326 UPPER POT BOARD SCHEMATIC

6-15 LOWER POT BOARD (81325)

This board contains two dual concentric controls, a latching pushbutton switch, and two LED indicators. The board mounts on the left front panel at the control positions of MIC/ RF PWR, RF gain/SQUelch, ALC indicator, and the PROCessor on/off switch and indicator.

When PROCessor on/off switch S1 is in the "on" position, "+REG" voltage is applied to the anode of LED D1 and , through connector 70, to a diode on the transmit audio board which routes processed audio to MIC gain control R1 via cable 71. R1 sets the level of the signal returning on cable 71 to the balanced modulator. When S1 is in the "off" position, indicator D1 is extinguished, and unprocessed transmit audio is routed through R1 to the balanced modulator.

Through connector 29 to the 2nd mixer board, RF PWR control R2 forms a voltage divider which sets the ALC threshold. ALC action develops a current through connector 28 which illuminates ALC indicator D2.

Through connector 50 to the IF/AF board, RF gain and SQUelch controls R3 and R4 form voltage dividers which determine respectively AGC resting voltage and squelch threshold.

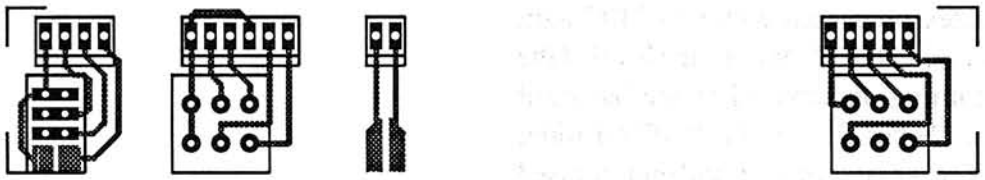


FIGURE 6-39. 81325 LOWER POT BOARD CIRCUIT TRACE

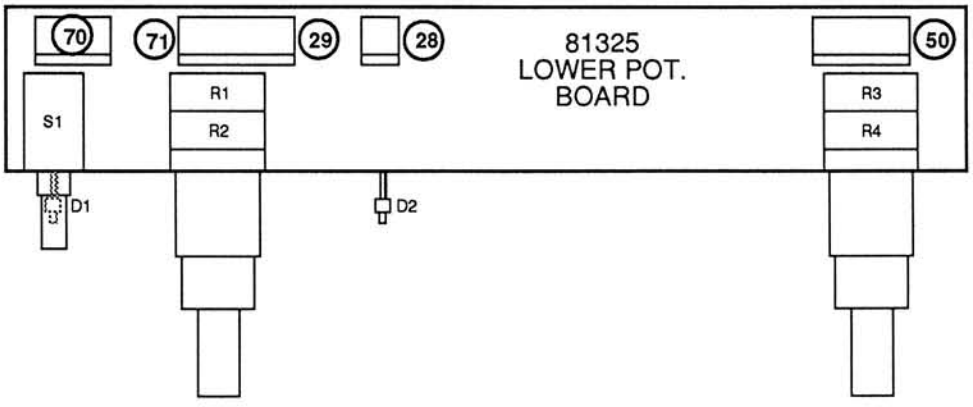


FIGURE 6-40. 81325 LOWER POT BOARD COMPONENT LAYOUT

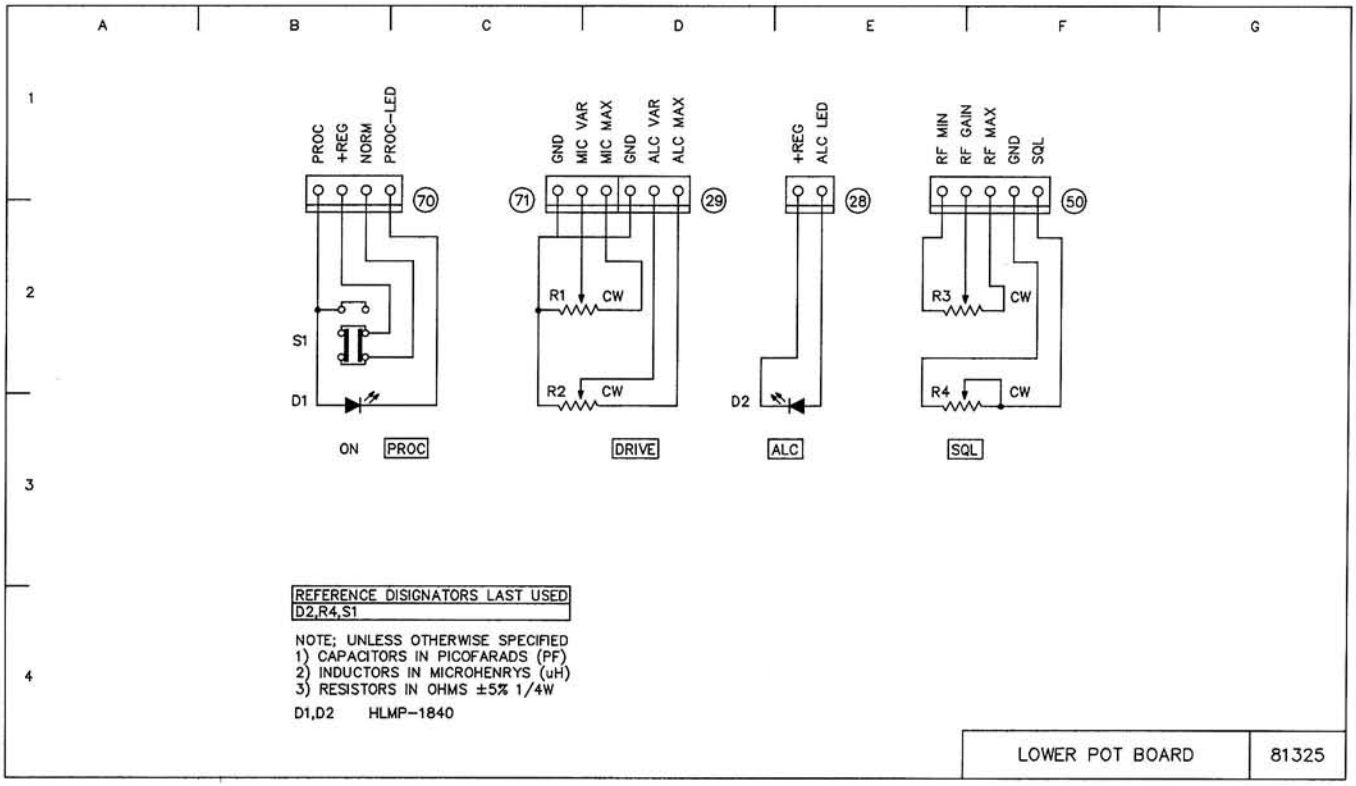


FIGURE 6-41. 81325 LOWER POT BOARD SCHEMATIC

6-16 SIDETONE BOARD (81362)

The sidetone board is mounted on the left rear panel with four controls accessible from the rear. The controls are user adjustable CW sidetone PITCH and LEVEL, transmit audio MONITOR level, and keypad BEEP/VOICE synthesizer level.

Transistor Q2 and associated components form a twin-tee audio oscillator with frequency of oscillation determined by PITCH control R7 and output level set by LEVEL control R10. The oscillator is enabled by transistor Q1 switching emitter bypass capacitor C1 to ground when the sidetone pin of connector 63 from the control board goes high.

MONITOR control R12 receives a sample of the transmit audio signal from the TX Audio/BFO board on connector 72. The BEEP/VOICE control R14 receives keyboard beep and optional voice synthesizer signals from the digital board via connector 80. The outputs from the three level controls are summed by resistors R11, R13, and R15 into an audio amplifier on the IF/AF board via connector 57.

Anti-vox and speaker connections jumper through this board from the external speaker jack at connector 76 to the TX Audio/BFO board via connector 72 and the internal speaker via connector 77.

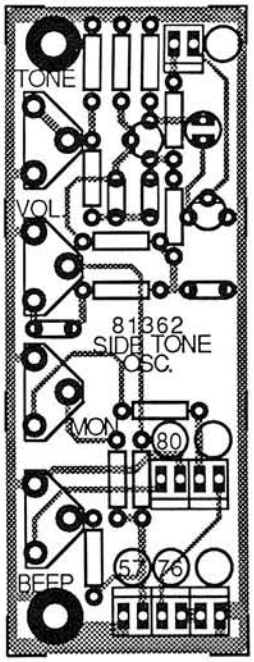


FIGURE 6-42. 81362 SIDETONE BOARD CIRCUIT TRACE

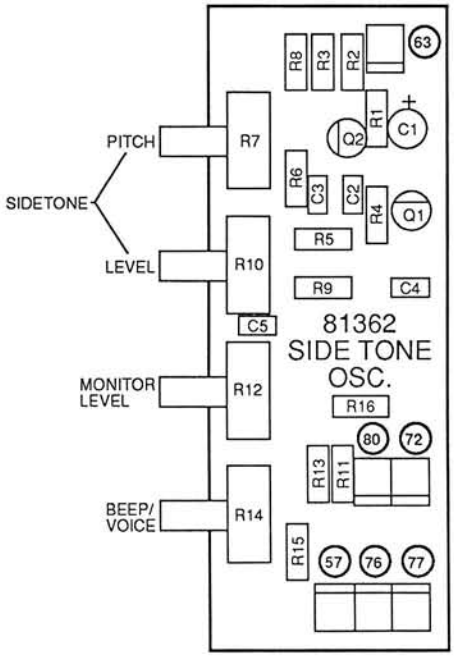


FIGURE 6-43. 81362 SIDETONE BOARD COMPONENT LAYOUT

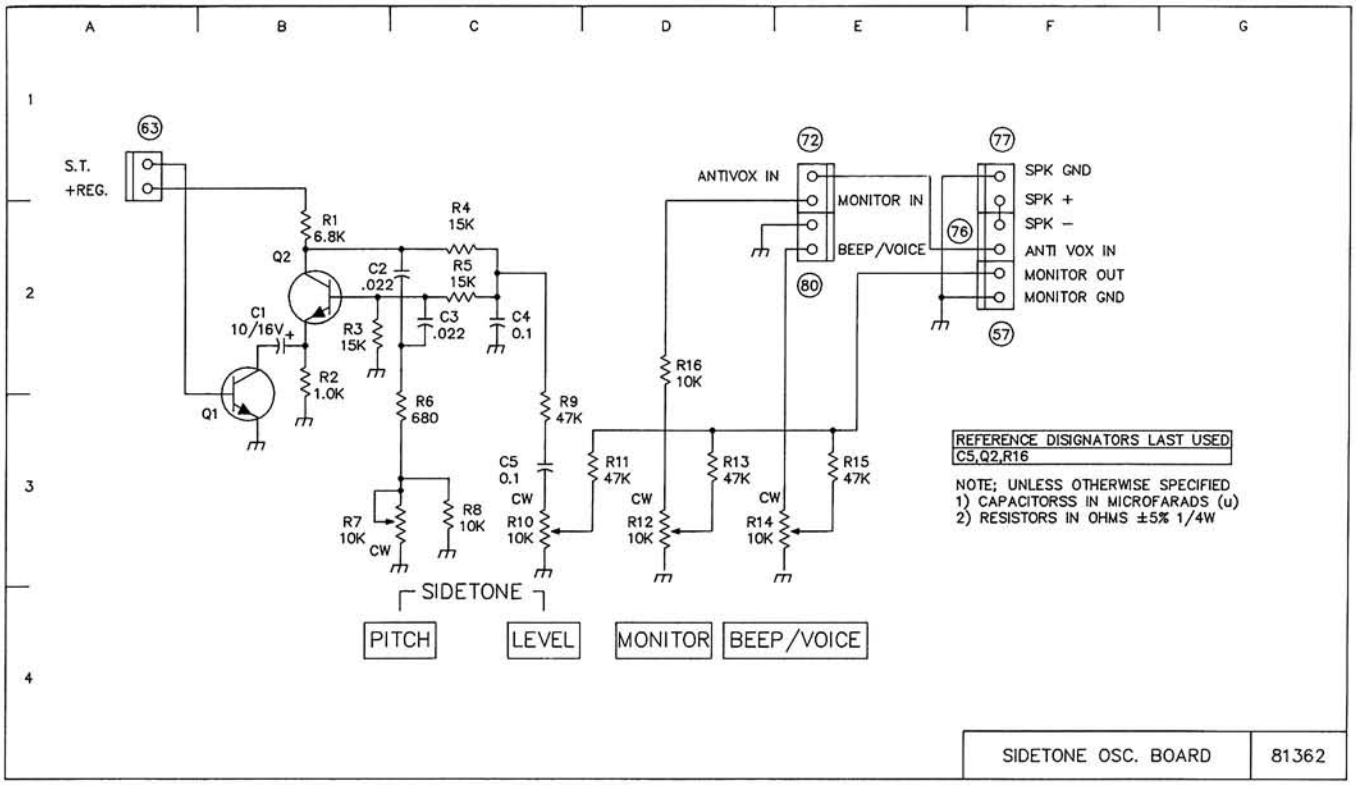


FIGURE 6-44. 81362 SIDETONE BOARD SCHEMATIC

6-17 TRANSMIT AUDIO/BFO BOARD (81339)

This board contains the transmit audio amplifiers, speech processor and VOX circuit, the 9 MHz BFO and balanced modulator. It is located at the left rear of the chassis, on top of the chassis deck behind the PLL shield box. Board mounted controls for VOX DELAY, VOX GAIN, and ANTI-VOX, and phono connectors for AUDIO IN and OUT and XVRT ENable and OUT are accessible through the rear panel.

Microphone audio from connector 73 or transmit audio from the rear panel AUDIO IN jack is amplified by U2B. The output of U2B splits four ways to drive the anode of diode switch D18, FM audio output connector 75, the speech PROCESSOR control pot at connector 74, and the VOX GAIN control R64. Diode D18 is normally forward biased through connector 70 when the PROCessor switch on the lower pot board is in the off position, connecting the amplified audio signal to the MIC gain control at connector 71.

The speech processor input at connector 74 is amplified to a nominal 1.2 Volts peak by U3A and again by U3B to approximately 1.8 Volts peak. One output of U3B drives rectifier D15 and compressor transistor Q13. Q13 clamps part of the original input to ground, effectively maintaining a constant audio level at the output of U3A. Another output of U3B drives the processor level meter through emitter follower Q12 and connector 78.

Half the output of U3A appears across clipper diodes D16 and D17, but no clipping occurs at the normal level of 0.6 volts. The clipper diodes limit fast audio transients, for which the compressor circuit is less effective, to 0.65-0.7 Volts. The compressed and limited speech processor output level is set by R81, and U4A buffers the output to the anode of diode switch D19. When the PROCessor switch is in the ON position, D18 is reverse biased, D19 is forward biased, and processed audio is passed to the MIC gain control via connector 71. R18 is adjusted so that the peak levels of the processed and the unprocessed audio signals at connector 71 remain equal as the PROCessor switch is toggled between OFF and ON.

The output of the MIC gain control at the center pin of connector 70 is buffered by U4B and output to the balanced modulator U5 and to the MONITOR level control on the sidetone board via connector 72. The balanced modulator mixes the transmit audio signal from U4B with the BFO carrier to produce a 9MHz double sideband suppressed carrier output. U4B is enabled on pin 7 by "TD" voltage from the control board connector 60. The balanced modulator gain is increased in SSB mode by grounding bypass capacitor C24 through Q9. Q10 unbalances the modulator in CW and RTTY modes. Tuned transformer T1 performs the match to the 50 Ohm DSB input of the 2nd mixer board at connector 37. R38 and R39 trim the AC and DC balance of U5 for maximum carrier null.

The VOX circuit is formed by U1, U2A, and Q11. Transmit audio from U2B is divided by VOX GAIN control R64 and amplified by U1B to drive positive voltage doubler D9-D10. Likewise anti-VOX input (speaker audio) on connector 72 is divided by ANTI VOX control R66 and amplified by U2A to drive negative voltage doubler D11-D12. The voltage doubler outputs are summed into comparator U1A by resistors R73 and R74. Whenever the sum at U1A pin 3 is more positive than the reference voltage at U1A pin 2, the comparator output goes high, charging C57 and saturating VOX keying transistor Q11. When the PTT/VOX switch on the switch board is in the VOX position, Q11 keys the transmitter via switch board connector 68 and control board connector 65. VOX DELAY control R79 sets the hold-in time of the VOX circuit by determining the discharge rate of C57.

The BFO oscillator/amplifier is formed by transistors Q6-Q8, and its frequency of operation is determined by crystals Y1-Y2, diode switches D20-D24, and capacitors C3-C10. Based on the mode of operation, transistor switches Q1-Q5 drive the diodes which select trimmer capacitors to set the BFO frequency at the proper place with respect to the IF filter response. Mode information from the control board enters at connector 60. The trimmers can be set with a high resolution counter at connector 46 by switching modes in the order listed below and adjusting the corresponding trimmer for the frequency indicated:

RTTY(shift CW) transmit, with MARK/SPACE low, adjust C6 for 9.000875 MHz.

RTTY transmit, with MARK/SPACE high, adjust C10 for 9.000705 MHz.

RTTY receive or LSB, adjust C4 for 9.003000 MHz.

USB, adjust C7 for 9.000000 MHz.

CW transmit or TUNE, adjust C9 for 9.000750 MHz.

NOTE: RTTY MARK input voltage can be in the range of 0 to -15 Vdc. RTTY SPACE input voltage should be in the range of +2.5 to +15 Vdc for proper operation.

Because of a slight interaction between the trimmers, these adjustments should be repeated at least once.

The BFO output from Q7 splits three ways. One output drives ALC transistor Q8 which controls the bias of oscillator transistor Q6 to maintain a constant output level. Another output serves as the carrier input to the balanced modulator U5. The third BFO output drives the product detector on the IF/AF board through connector 46.

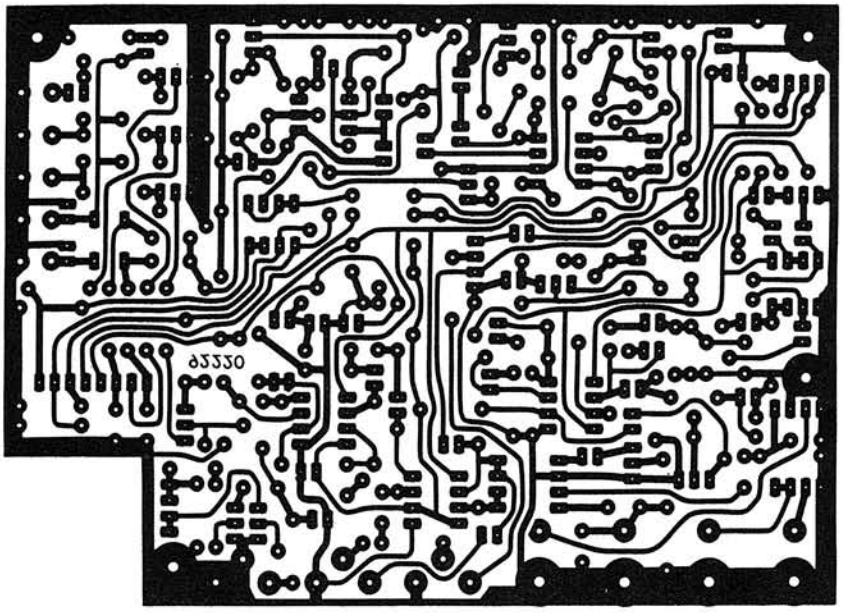


FIGURE 6-45. 81339 TRANSMIT AUDIO/BFO BOARD CIRCUIT TRACE

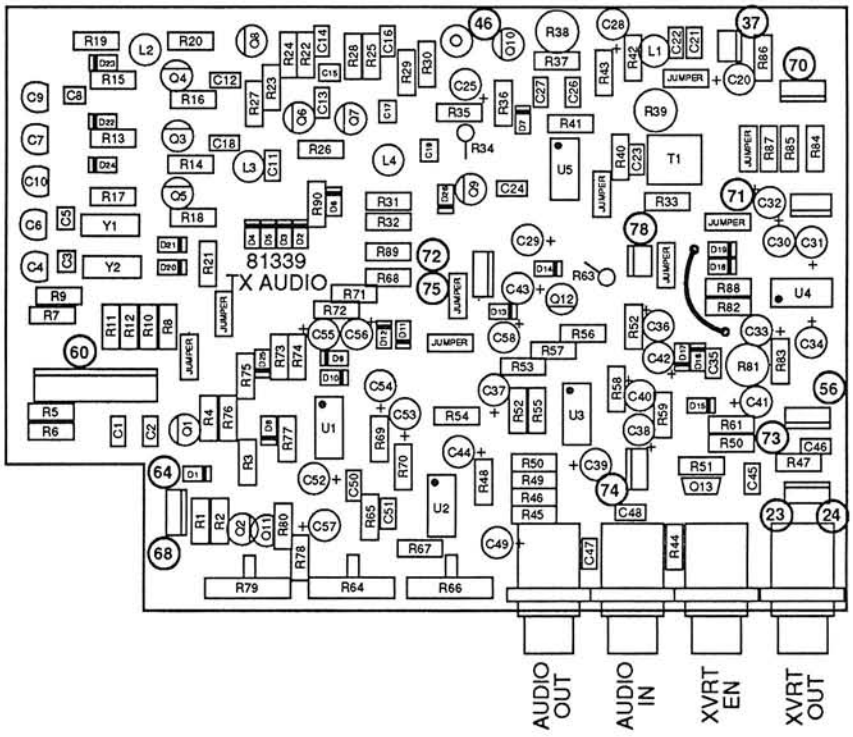
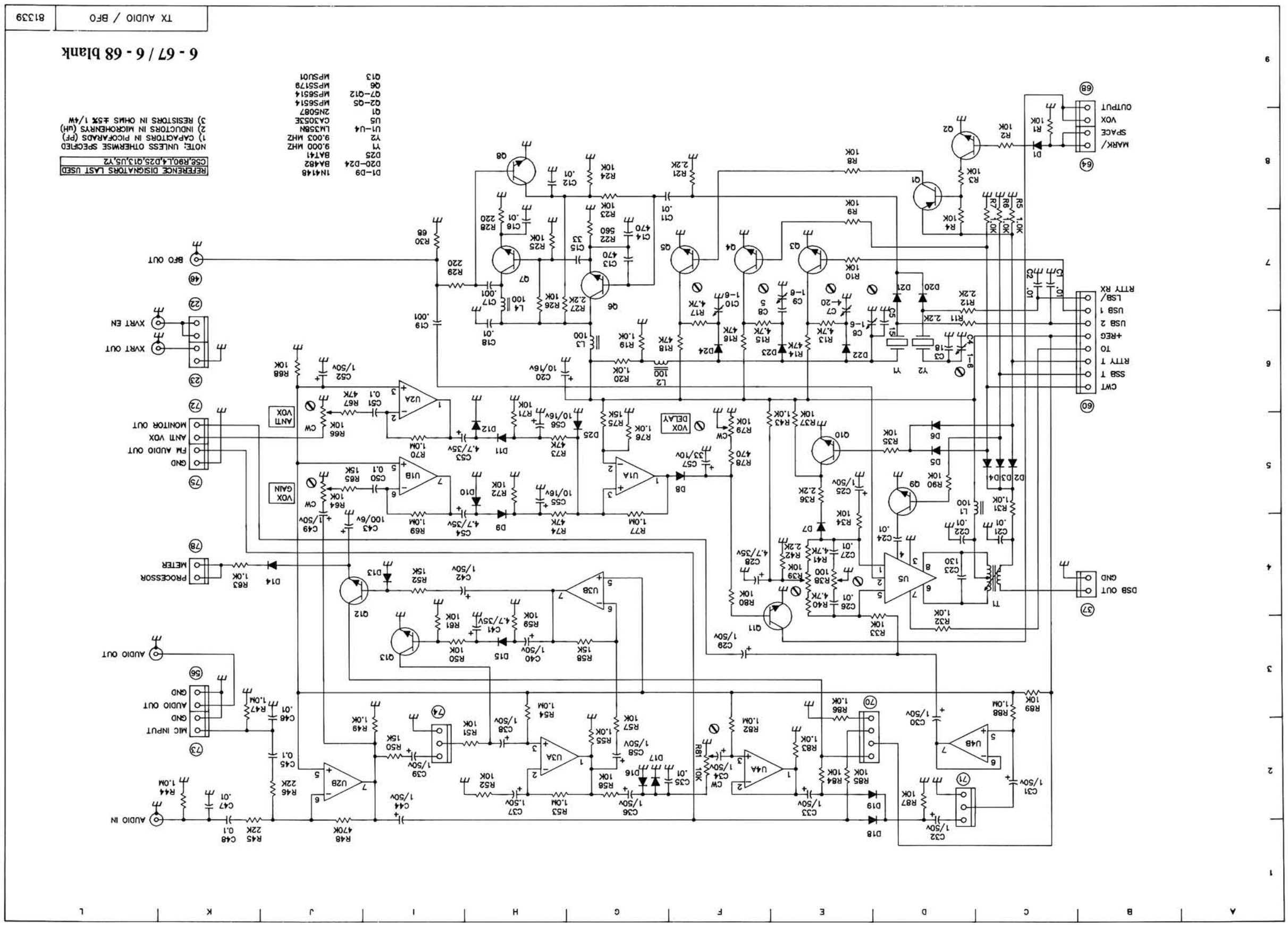


FIGURE 6-46. 81339 TRANSMIT AUDIO/BFO BOARD COMPONENT LAYOUT



6 - 67 / 6 - 68 blank

6-18 LOW LEVEL AMPLIFIER/NOISE BLANKER (81340)

This board contains the low level wide-band amplifier for the transmitter, the receiver noise blanker, "T" and "R" voltage generator, and the "+REG" and meter lamp regulators. It is located on the left upper chassis on top of the PLL shield.

The operating frequency transmit signal from the first mixer board enters on connector 24, is amplified by class A amplifier transistors Q9 and Q10, and exits to the final power amplifier at connector 79. During transmit, "T" voltage supplies bias to both stages through R14 and R20.

"T" and "R" voltages are developed by Q1-Q8 based on the level of the "TD" pin from control board connector 62. In transmit "TD" is high and Q4 sources approximately 12.5 Volts to the "T" line through R8, while Q8 holds the "R" line low. In receive "TD" is low and Q7 sources approximately 8.5 Volts to the "R" line through R13, while Q5 holds the "T" line low.

At connector 31, a sample of the 9 MHz receive IF signal from the second mixer board is input to noise blanker amplifiers U2 and U3. Part of the output of U2 is sent to the FM option connector. The output of U3 drives detector diodes D2 and D3 to produce a noise envelope signal across C30. U1A buffers this signal and charges AGC capacitor C20 through R39 and discharges it through R38 to determine the critical noise blanker AGC time constants. U1B amplifies the noise envelope to drive the base of noise threshold transistor Q12. The emitter of Q12 is biased with a variable voltage from the noise blanker LEVEL control at connector R. Noise pulses which overcome this bias voltage are amplified by Q12 and sent to the pulse amplifier stages Q13-Q17. The leading edge of a noise pulse is applied directly to the NB Pulse pin of connector 32 via R55 and D5. The trailing edge is delayed by integrator Q15 and applied in parallel with the leading edge signal to form a complete blanking pulse. Connector 32 carries the blanking pulse to the noise gate on the second mixer board. Power for the pulse amplifier stages is through connector 67 and the N.B. switch on the front panel switch board.

A regulator composed of U4 and Q11 supplies 8.5 Volts "+REG" voltage to all boards via connector 62 and the control board. Q11 is mounted on the PLL shield plate and connected with cable Q. Meter lamp regulator U5 is likewise mounted to the PLL shield and connected with cable P. Regulated 6 Volts is supplied to the meter lamps through connector O.

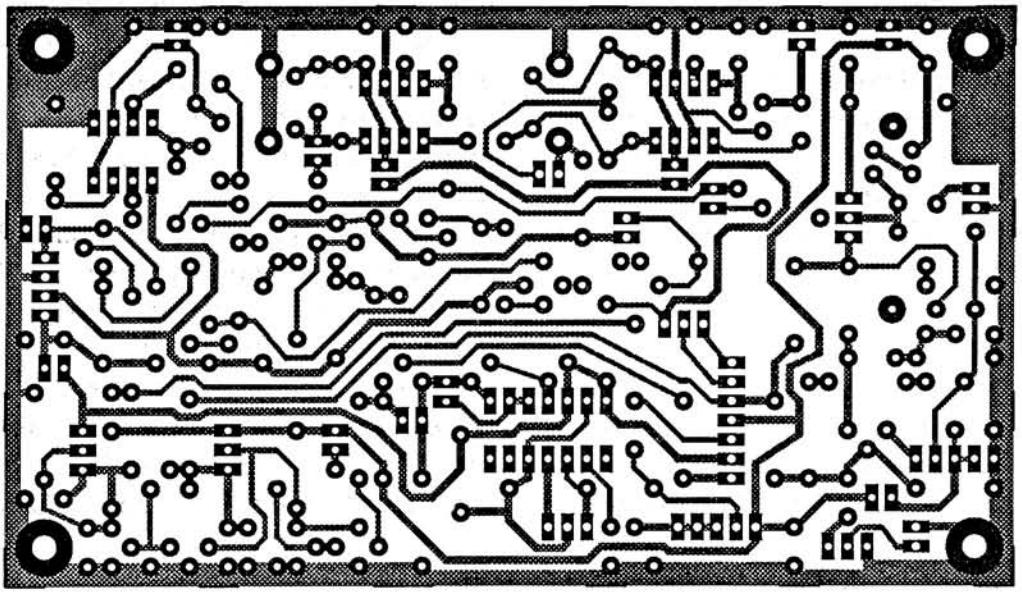


FIGURE 6-48. 81340 L. L. AMPLIFIER / NOISE BLANKER CIRCUIT TRACE

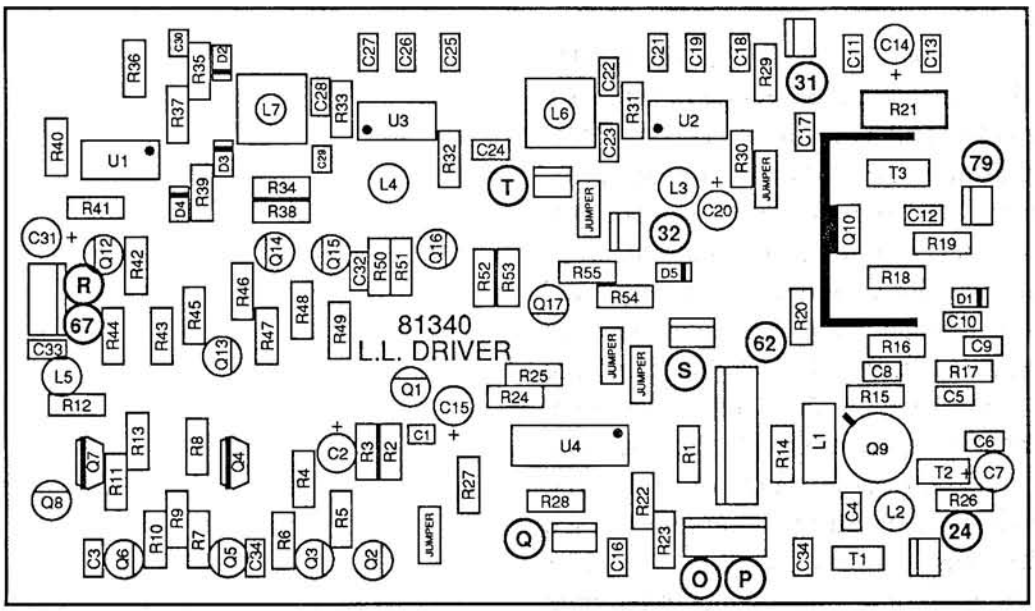
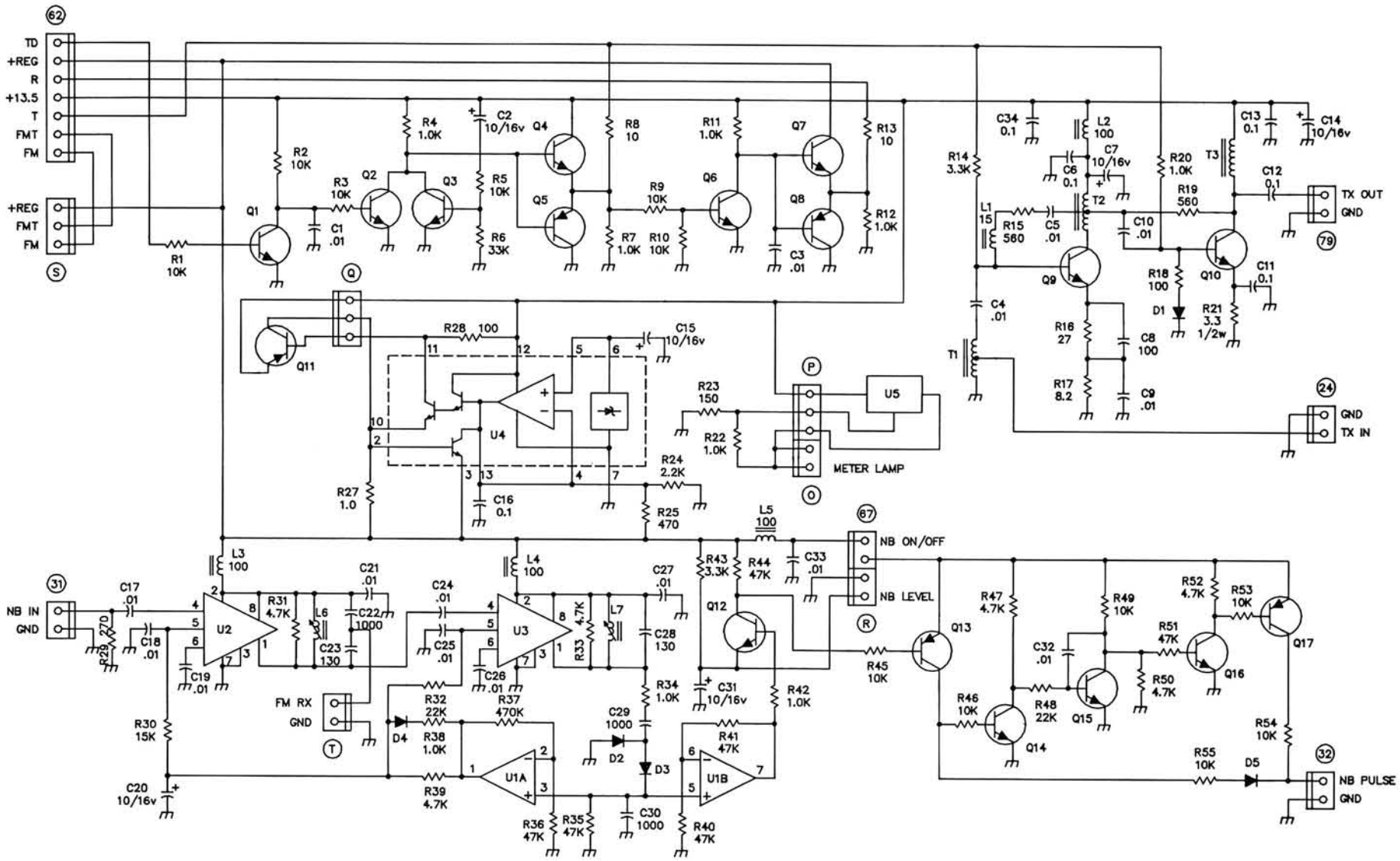


FIGURE 6-49. 81340 L. L. AMP. / NOISE BLANKER COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R55,C33,L7,U5,D5,Q17,T3

NOTE: UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1	LM358N	Q6,Q12	MPS6514
U2–U3	MC1350	Q14–Q16	MPS6514
U4	MC1723C	Q4–Q7	MPSU01
U5	MC7805CT	Q5,Q8	2N5087
D1	1N4002	Q13,Q17	2N5087
D2–D4	BAT41	Q9	2N3866
D5	1N4148	Q10	MRF476
Q1–Q3	MPS6514	Q11	MJE370

6 - 71 / 6 - 72 blank

LOW LEVEL AMP	81340

6-19 RF POWER AMPLIFIER (81342) and PA BIAS BOARD (81343)

The high power RF amplifier, its push-pull driver stage, and the PA bias board are housed in a metal box which is an integral part of the heatsink assembly. The unit is attached to the rear panel with four hex head screws. Input is received through connector 79 on the low level amplifier board, and the 100 Watt output is through a miniature coaxial cable soldered to pins on the lowpass filter board. "T" voltage enters the unit on the small blue wire from connector 11 on the lowpass filter board, and 13.5 Volts dc enters on the large red wire from the dc power board.

Q1 and Q2 form a wideband class AB linear driver stage with input and output impedance matching accomplished by broadband transformers T1 and T3. RC networks R1-C1 and R6-C2, in conjunction with feedback networks R3-L3-C5, R8-L4-C6, and emitter networks R4-R5-C3 and R9-R10-C4, control the input impedance and flatten the gain variation of the transistors over the frequency range of 1.6-30 MHz. Regulated bias is fed to this stage by the green wire from connector M on the PA bias board.

Q3 and Q4 form the high power broadband output stage of the transmitter. This stage is also biased to linear class AB operation by a regulator on the PA bias board. Input impedance and gain variation with frequency are controlled by RC input networks and RF feedback similar to the driver stage. Broadband transformer T4 matches the output stage to 50 Ohms for driving the transmit lowpass filters. Regulated bias for the output stage arrives on the brown wire from connector M on the PA bias board.

Bias for both stages is temperature compensated to maintain a relatively constant operating point by mounting the bias reference diodes D2 and D3 in thermal contact to the heatsink. The temperature dependant voltage across each reference diode is added to a portion of the "T" voltage and the sum is used as a reference voltage for the respective bias regulator U1B-Q1 or U1A-Q2 on the PA bias board. In receive, "T" voltage is low and both regulators are cut off, removing bias from both PA stages. When "T" goes high, capacitor C27 delays the rise of the bias reference voltages, reducing the gain of the PA until the rest of the transceiver settles into a stable transmit mode.

The bias adjustment pots R11 and R21 are accessible through the bottom shield of the transceiver. To adjust PA bias, an dc amp meter must be inserted in series with the large red 13.5 Vdc lead to the dc power board. Unplug connector 79 from the low level amplifier board to remove drive from the PA. Key the transmitter in USB mode. While watching the meter, rotate first the final bias pot R21 and then the driver bias pot R11 to produce minimum current. Now rotate the driver bias pot R11 to increase the meter reading by 50 milliamps. Next rotate the final bias pot R21 to produce an additional increase of 500 milliamps on the meter. Remove the meter and reconnect the red wire to the dc power board and connector 79 to the low level amplifier board.

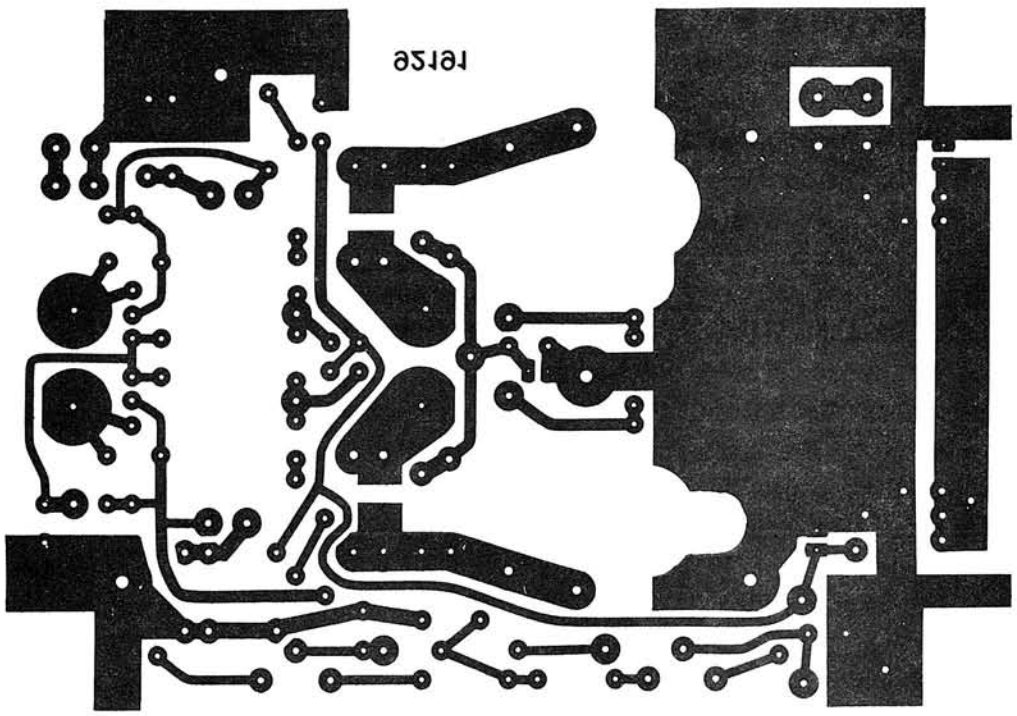


FIGURE 6 - 51. 81342 RF POWER AMPLIFIER CIRCUIT TRACE

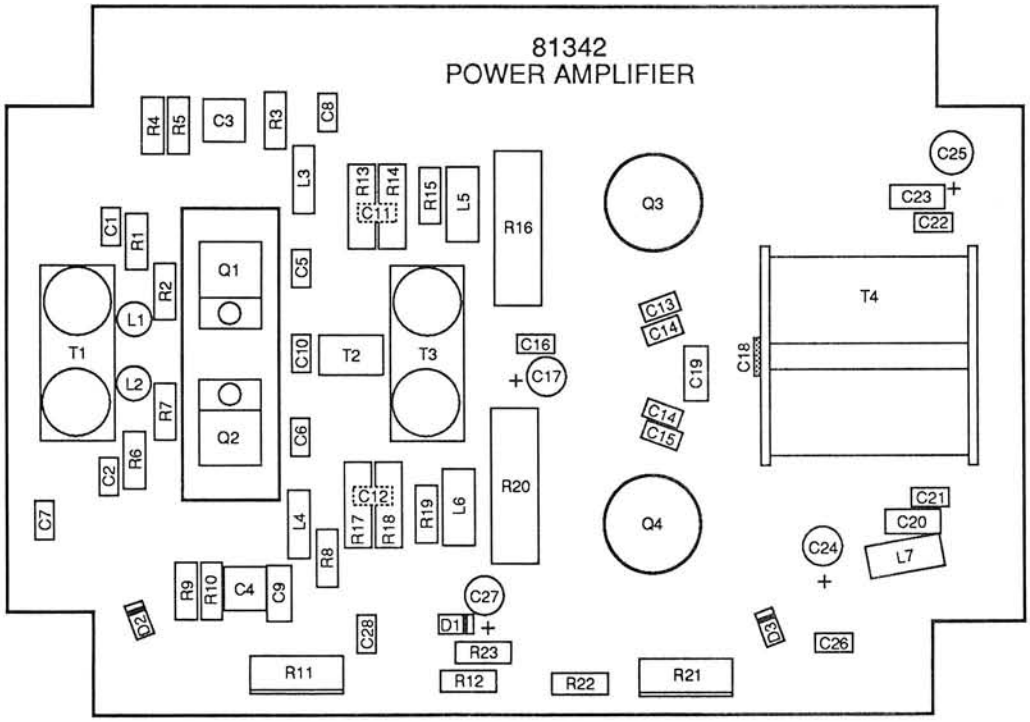


FIGURE 6 - 52. 81342 RF POWER AMPLIFIER COMPONENT LAYOUT

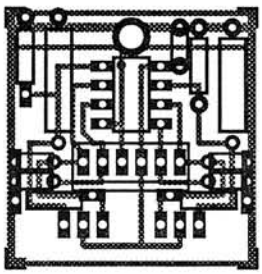


FIGURE 6 - 53. 81343 PA BIAS BOARD CIRCUIT TRACE

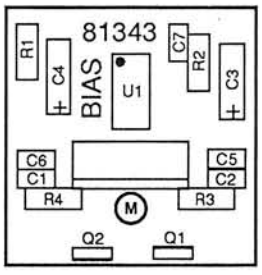


FIGURE 6 - 54. 81343 PA BIAS BOARD COMPONENT LAYOUT

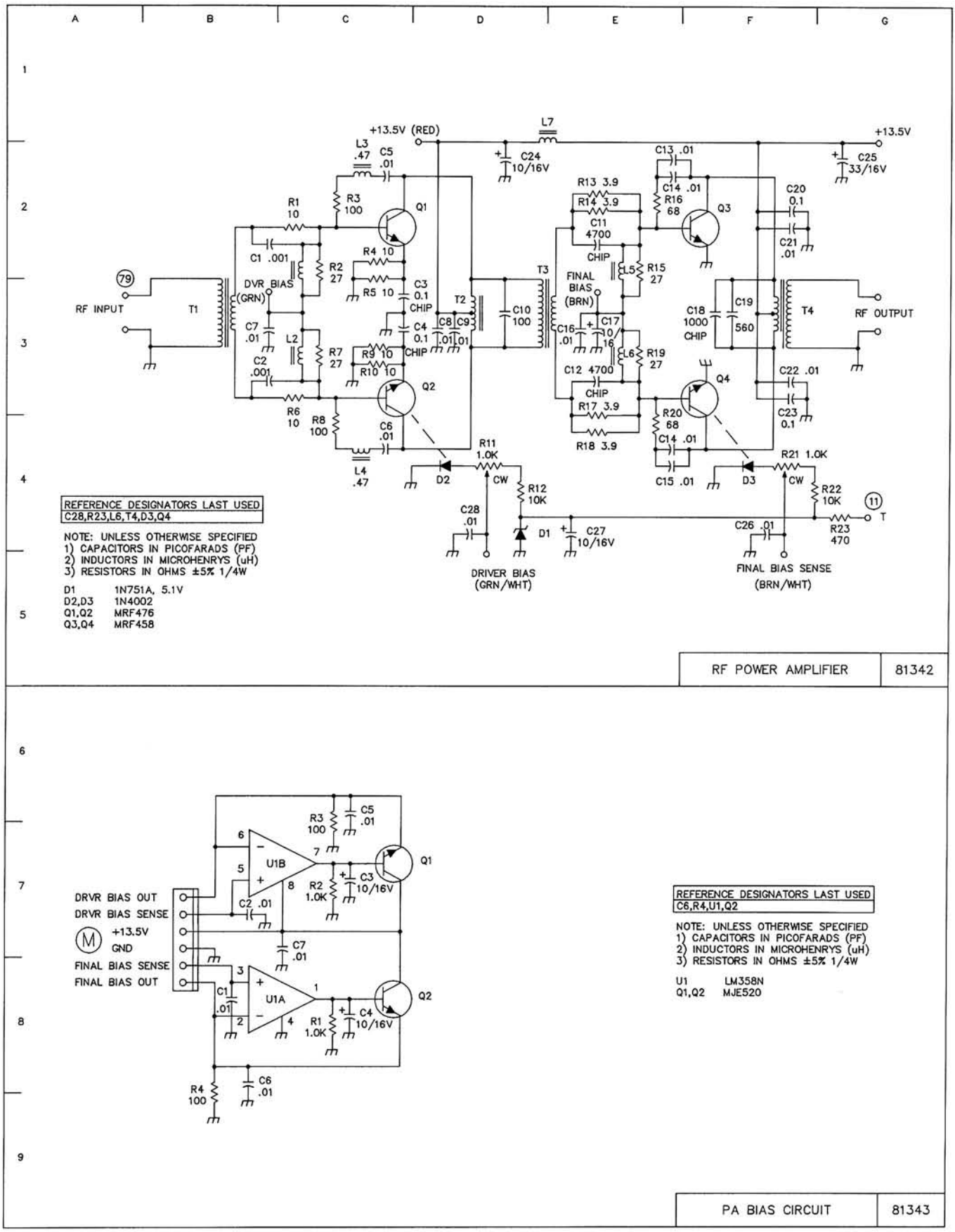


FIGURE 6-55. 81342 RF POWER AMP. and 81343 PA BIAS BOARD SCHEMATIC

6-20 LOGIC BOARD (81267)

This board contains the main system microprocessor, several I/O driver integrated circuits, address decoders and latches, three edge card connectors for expansion boards, and the rotary encoder circuitry.

The main microprocessor, U8, is the heart of the system. This is an 8-bit CMOS microprocessor with sixteen I/O lines and a multiplexed address/data bus (B0-B7 and A8-A12) capable of addressing up to 8K of external memory. This microprocessor contains an internal oscillator whose frequency is controlled by Y1. The I/O lines going to connector 84 are used to control the PLL synthesizer circuits. The SOL line is monitored by U8 to determine if an out of lock condition exists in the PLL synthesizer. If the SOL line goes low for more than about 100 mS, U8 will send a "PLL OUT OF LOCK" message to U1 on the VF Display Control Board and also disable the transmitter of the PARAGON. When the SOL line returns high, the display and transceiver are returned to normal. Connector 1 is used to select the correct VCO in the PLL synthesizer, depending on the operating frequency of the PARAGON. On connector 66, U8 monitors the KEY IN line to tell when it should go into the transmit mode. When KEY IN goes high, U8 will compute the correct transmit frequency and insert any needed timing delays before enabling the transmitter output by setting TX EN high. Connector J provides access to the RESET line of U8. This is connected to a push button switch located on the right side of the PARAGON and is used to force a RESET of U8 in the event that the system malfunctions and cannot be cleared by simply turning the POWER switch off and back on. Pin PA1 of U8 is used to monitor the power supply line (+13.5V) in order to detect when the POWER switch has been turned off. When this happens, U8 is placed into a "sleep" mode to conserve power but still retain its memory. When power is turned on, with U8 in the "sleep" mode, transistors Q3 and Q4 generate a negative going pulse on the IRQ line of U8. This wakes the microprocessor up and restores it to normal operation. The IRQ line is also used by the Real Time Clock circuit located on the Ram-Rom-Rtc Board, and by the encoder circuits to tell the microprocessor to change frequency. The clock pulse from the encoder circuits is coupled by C13 to the IRQ pin. Pin PA0 of U8 is used to tell whether the encoder is tuning up(high) or down(low).

Additional I/O is provided by U7 which has twenty-four I/O lines directly controlled by the main microprocessor. Whenever the CE (pin 21) of U7 goes low, U7 is enabled by the main microprocessor. This signal is generated by the address decoder on the Ram-Rom-Rtc Board whenever the microprocessor addresses memory locations C2H - C8H. The I/O lines going to connector 91 are used as input lines from the key matrix of the Keypad. The lines going to connector D are used to interface with the microprocessor on the VF Display Control Board. Pin PE4 of U7 is used to select the type and frequencies of operation allowed on the PARAGON. When this line is jumpered to ground, the PARAGON will transmit only on the Ham Bands. If this jumper is removed, the PARAGON will transmit on any frequency from 1.7 MHz to 30 MHz. Pin PC7 of U7 is used to handshake with the optional Model 257 Voice Readout. The outputs at connector F go to U6 and are used to select a column during the keypad scanning routine.

U6 is a 1 of ten decoder which is used to scan the columns of the Keypad matrix. It is controlled by the signals coming from U7 via a jumper cable at connector F. The outputs of U6 go to connectors 94 and 97, which in turn go to the Keypad. Whenever a particular column is selected during the scan, that output goes low, while all others remain high.

Pins PB0-PB2 of U8 are used to send

serial data to U1, a 32 bit latched driver. The outputs of U1 at connector K are used to select the correct low pass filter circuits, depending on the operating frequency of the PARAGON. Output lines going to connector 59 are used to select the desired operating mode on the Control Board. Outputs from connector 92 drive the corresponding LEDs on the Keypad. Outputs from connector 41 are used to select the desired crystal filter position while the corresponding LEDs are driven by the lines going to connector 95. Outputs from connector 96 are used to drive additional LEDs on the Keypad. The outputs at connectors 98, 99, and A are used to drive the LEDs on the VF Display Board.

U12 and diodes D1-D7 are used as an address decoder whose outputs go to the Ram-Rom-Rtc Board.

U10 and U11 form another address decoder used to generate the DISP IRQ (enable) signal for U1 on the VF Display Control Board. The output of U10C goes low whenever U8 addresses A0H and the data strobe (DS) is high. In addition, the output of U11C goes high and serves to latch the required data into U9 (an 8 bit latch) which sends it to the display controller.

The encoder circuitry consists of an optical rotary encoder and hex schmitt trigger located on the Keypad Board. This circuit generates quadrature signals (each signal being 90° out of phase). The rotary encoder produces 120 pulses per revolution of the Main Tuning Knob. The four quadrature signals are sent via connector 93 to U2 and U3. These gates detect the leading and trailing edges of the signals and generate an output pulse for each edge, thus multiplying the number of pulses by four. The pulses are summed by diodes D8-D15 and applied to U4A and U4B which are connected as a flip-flop to detect the direction of the encoder. The UP/DOWN output of U4 goes to PA0 of U8. The summed pulses are applied through D16 and D17 to U4C and U4D. The clock pulses thus generated (480 per revolution of the encoder) are applied via C13 to the IRQ line of U8. They are also sent to U5 which buffers the signal and then integrates it to develop a tuning rate detector. When the number of pulses exceeds a predetermined threshold, the output of U5D goes high. This signal is connected to PE3 of U7 and is monitored by U8. When U8 sees the SHIFT line go high, it changes the tuning step size of the synthesizer to a larger value.

Transistors Q1, Q2, and Q5 comprise a low current regulator used to supply standby power when the POWER switch is turned off and U8 is in the "sleep" mode. Power is supplied either by the +13.5V line from the non-switched power supply on connector 2 or from an internal 9 Volt battery.

Connector 80 supplies the audio signal from the RTC (beep) and the optional Voice Readout to the audio circuits of the PARAGON.

Connector G goes to an externally mounted high current +5.6 Volt regulator mounted on the right side panel of the PARAGON.

Connector I supplies +13.5 Volts primary power for the externally mounted +5.6 Volt regulator and for U1, the 32 bit serial driver.

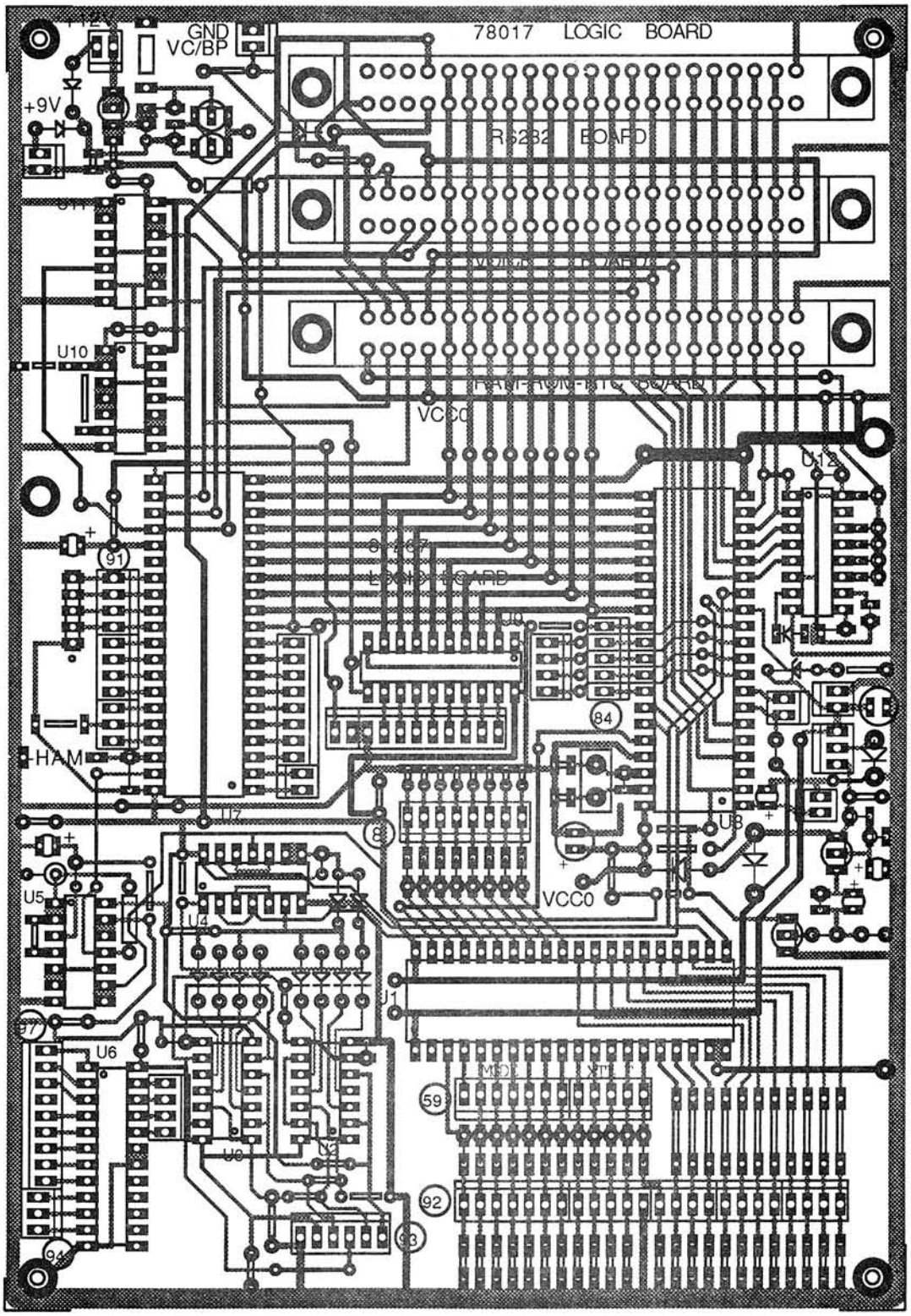


FIGURE 6-56. 81267 LOGIC BOARD CIRCUIT TRACE

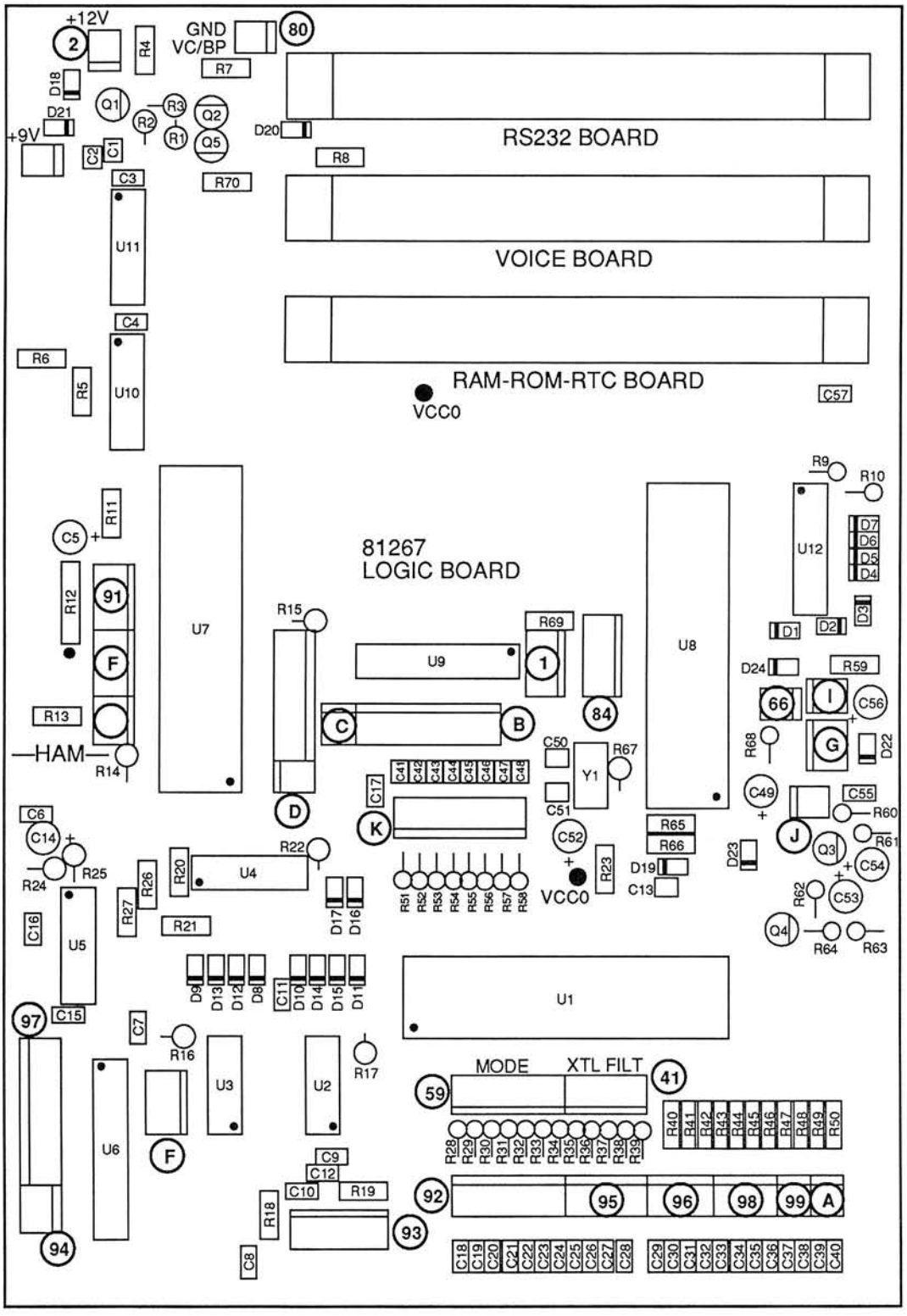
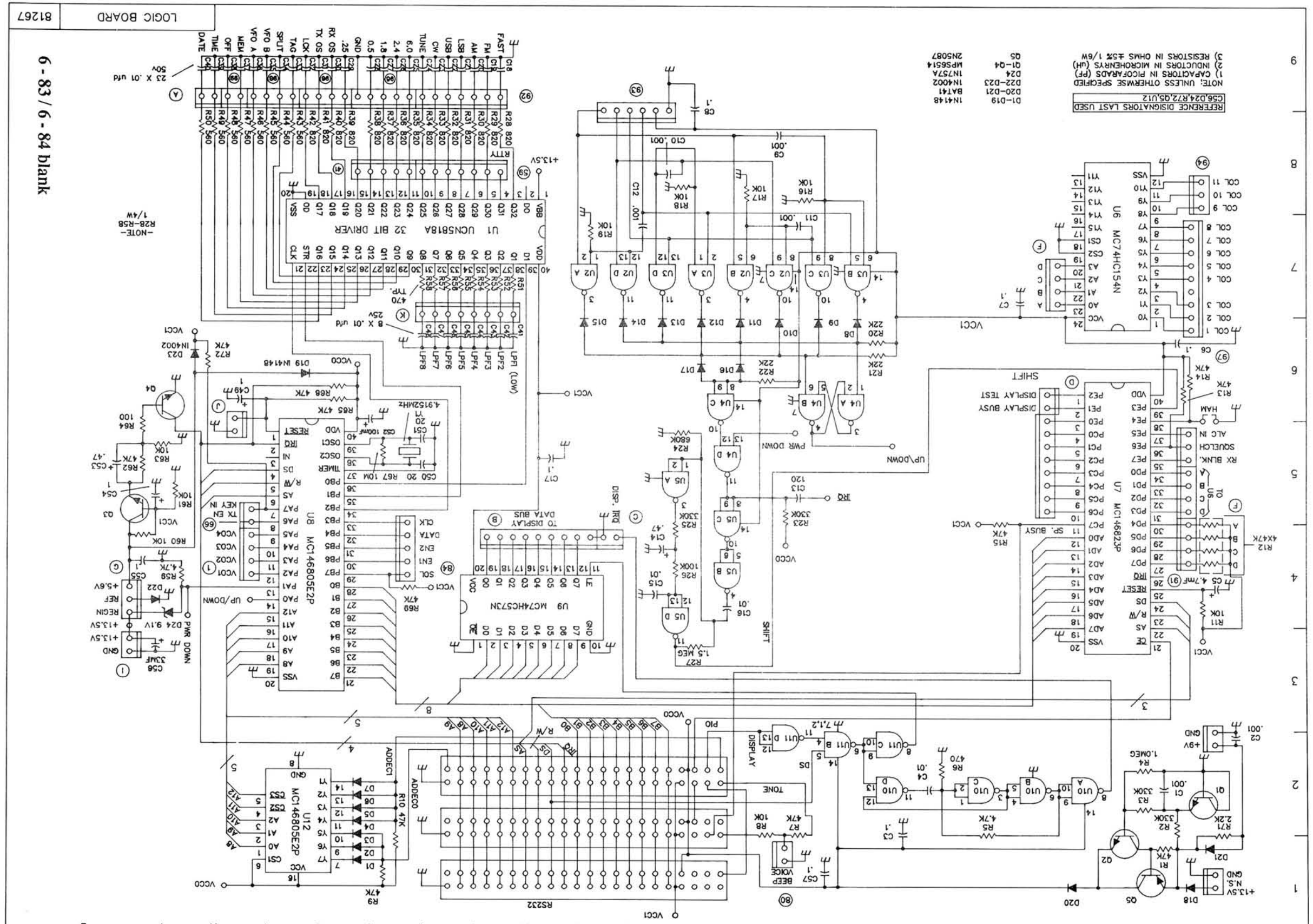


FIGURE 6-57. 81267 LOGIC BOARD COMPONENT LAYOUT



6 - 83 / 6 - 84 blank

6-21 CONTROL FILTER BOARD (81377)

The control filter board is mounted on the center chassis shield partition and contains 12 pi-section LC lowpass networks to filter sensitive control lines leading to the synthesizer and lowpass filter boards.

Eight band lines from the digital board enter at connector K and are filtered before exiting to the low pass filter board via connector 8. Four VCO select lines from the digital board enter at connector l, are filtered, and exit to the synthesizer major loop board via connector 90.

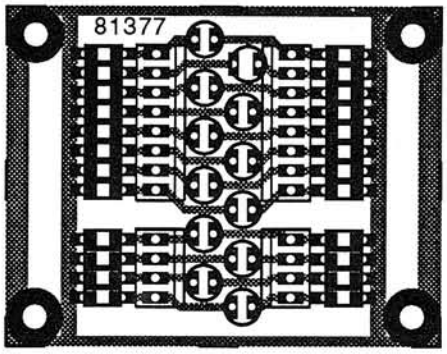


FIGURE 6-59. 81377 CONTROL FILTER BOARD CIRCUIT TRACE

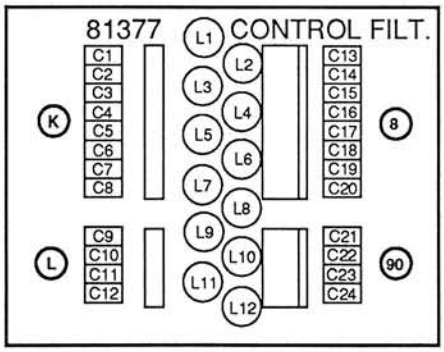


FIGURE 6-60. 81377 CONTROL FILTER BOARD COMPONENT LAYOUT

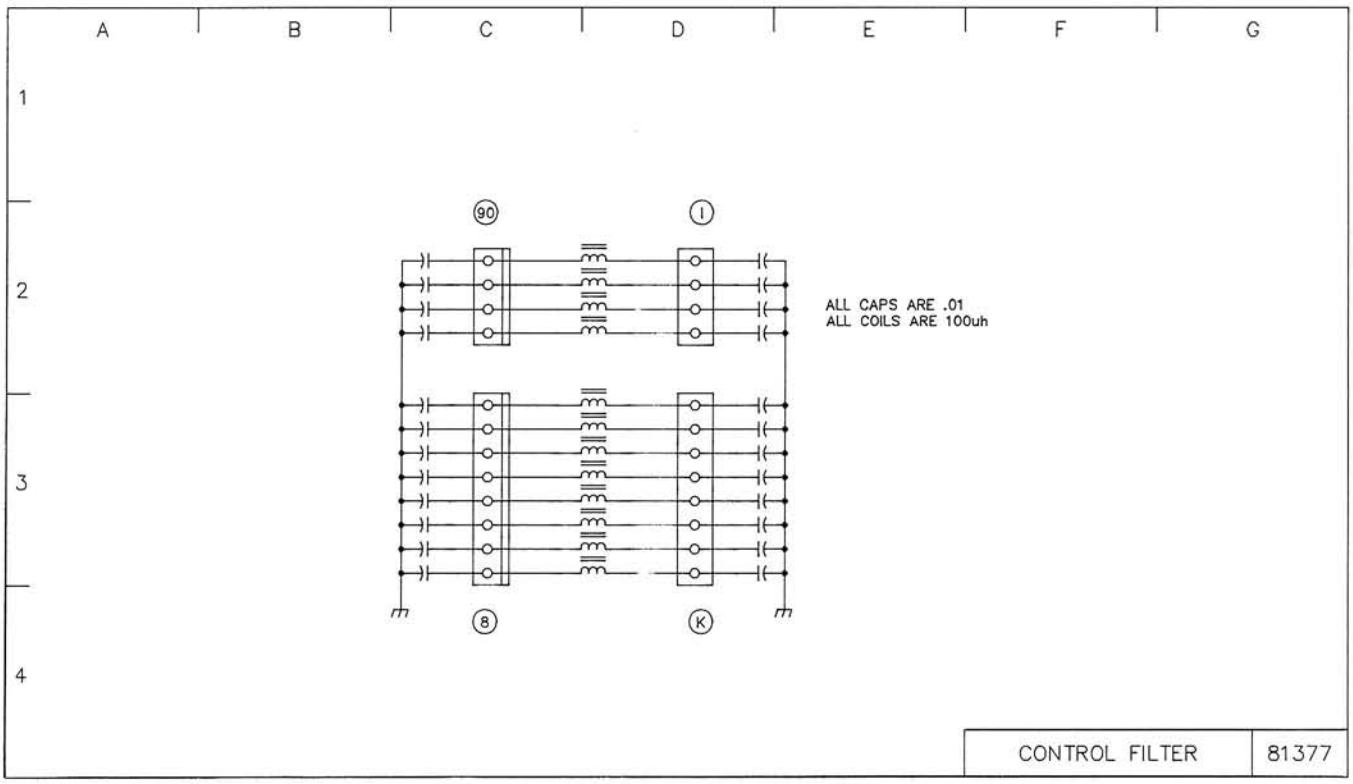


FIGURE 6-61. 81377 CONTROL FILTER BOARD SCHEMATIC

6-22 RAM-ROM-RTC BOARD (81360)

This board contains a Real Time Clock, CMOS Ram and Eprom, and address decoding circuits. The Real Time Clock, U3, keeps track of the time (24 Hour Format) and the date. Timing is crystal controlled by Y1 and adjustable by means of C5. U3 also has a built-in programmable square wave generator which is used to generate the "beep" tone for keypad feedback. This tone is output on the SQW pin of U3 and sent to transistor Q1 which amplifies the signal to a useful level. The output of Q1 is fed through a low pass filter, consisting of R7, R8, C6, and C7, to clean up the waveform. This signal is then fed to the edge card connector and eventually to connector 80 on the Logic Board.

U7 and U8 form an address decoder which provides several enable signals to the various memory mapped devices tied to the multiplexed address/data bus system. The output from Y0 of U8 is enabled for memory addresses 80H-8FH, which is reserved for U3, the Real Time Clock. Output Y1 of U8 is enabled for addresses 90H-93H, which is reserved for the optional Model 258 RS232 Interface. Output Y2 of U8 is enabled for address A0H, which is the VF Display Controller. Output Y3 is enabled for address B0H, which is for the Model 257 Voice Readout Option. Output Y4 of U8 is enabled for addresses C2H-C8H, which is reserved for the I/O expander, U7 on the Logic Board. Whenever any of the above outputs is enabled, the line goes low, at all other times it remains high.

U5 is another address decoder which is used to enable U2, a 2K x 8 CMOS Ram, for addresses 100H through 4FFH. When enabled, the CS pin of U2 is set low. This device contains the Memory and VFO information saved by the operator. Because of memory map limitations, only the first 1024 bytes of U2 are available for storing Memory information.

U6 and diode D2 form another address decoder designed to enable U1 for addresses 500H through 1FFFH. When enabled, the E pin of U1 is set low. U1 is an 8K x 8 CMOS, U.V. erasable EPROM, which contains the operating instructions for the main microprocessor system. Because of memory map restrictions, only the top 6,912 bytes of U1 are available for use by the main microprocessor.

U4 is an 8 bit latch which is used to latch the lower 8 bits of the address (A0-A7) from the multiplexed address/data bus coming from the main microprocessor on the Logic Board. This latch is enabled on the rising edge of the Address Strobe (AS).

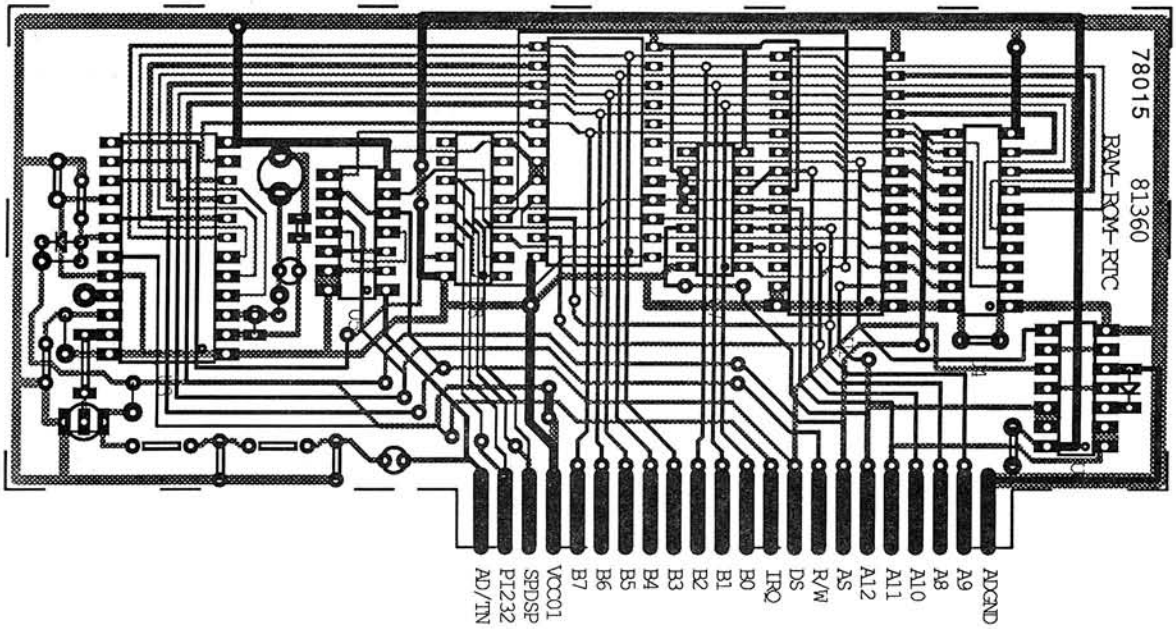


FIGURE 6-62. 81360 RAM-ROM-RTC BOARD CIRCUIT TRACE

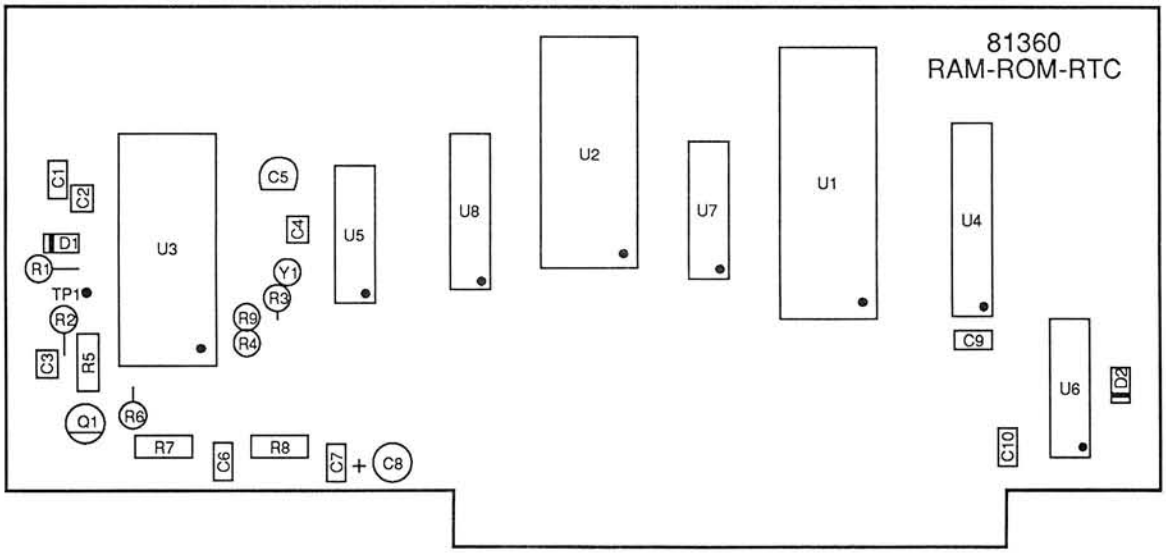
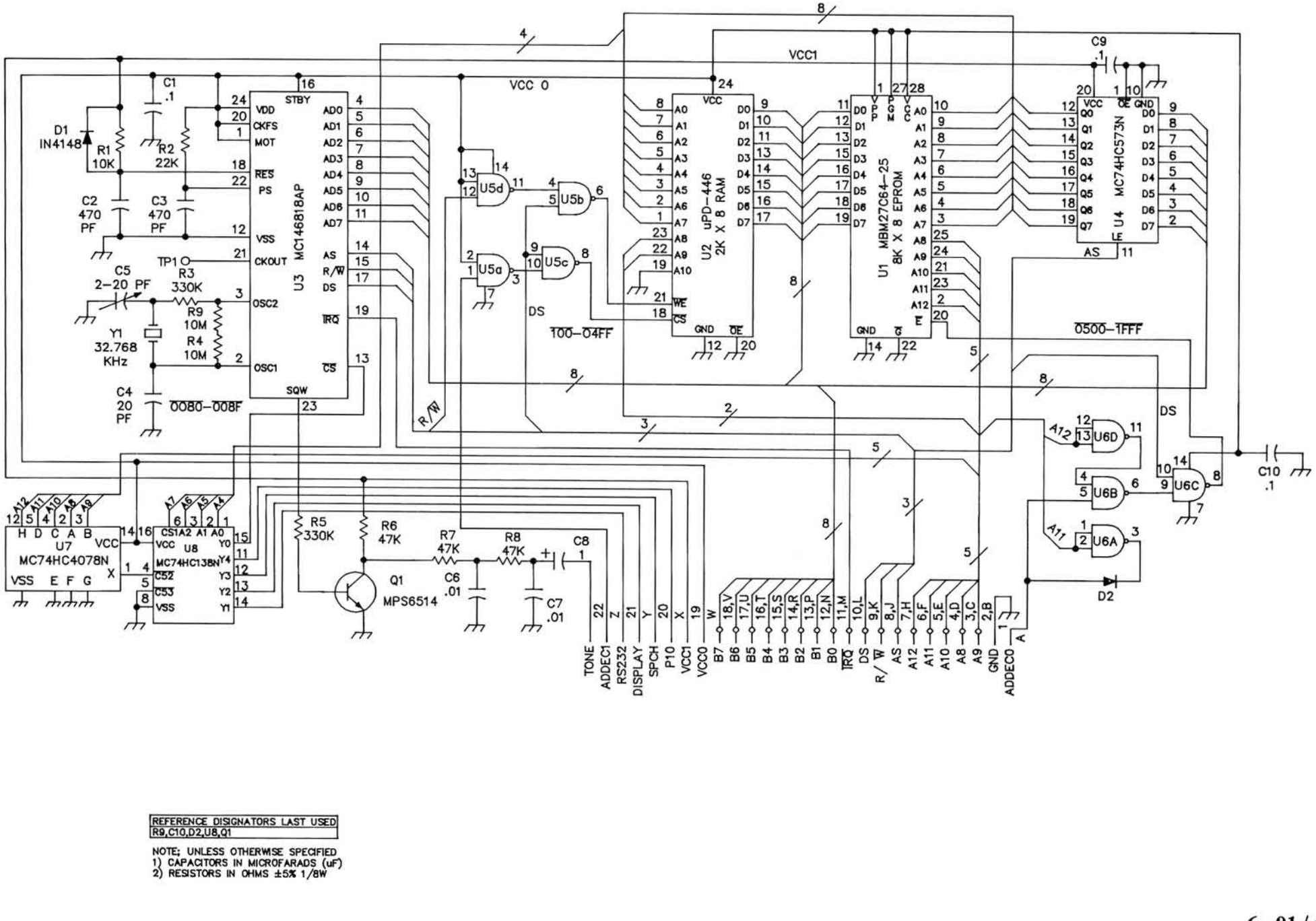


FIGURE 6-63. 81360 RAM-ROM-RTC BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
R9,C10,D2,U8,Q1

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN MICROFARADS (uF)
2) RESISTORS IN OHMS ±5% 1/8W

6 - 91 / 6 - 92 blank

RAM/ROM/RTC BOARD	81360

6-23 KEYPAD BOARD (81268)

The keypad board contains an array of 43 key switches, 15 LED indicators, a rotary shaft encoder and encoder buffer. The circuit board is mounted to the rear of the front panel keypad bezel and is connected to the digital board through six connectors which are accessible through the sub panel at the rear of the fold down front panel assembly.

The keypad switches are arranged electrically in an array of eleven columns and four rows. The columns are scanned through connectors 94 and 97, and the rows are sensed through connector 91. The microprocessor detects a key closure by strobing each column line low in sequence, while watching for a low to appear on any of the row lines. The location of the closure is defined by the intersection of the column and row lines that are simultaneously low.

The digital board drives the indicator LEDs through connectors 92, 95, and 96. The diodes are illuminated by positive voltage drive and all diode cathodes return to ground through connector 95.

Output pulses from the shaft encoder are buffered and inverted by U1 and output to the digital board on connector 93. Connector 93 also supplies 5 Volt power to the encoder.

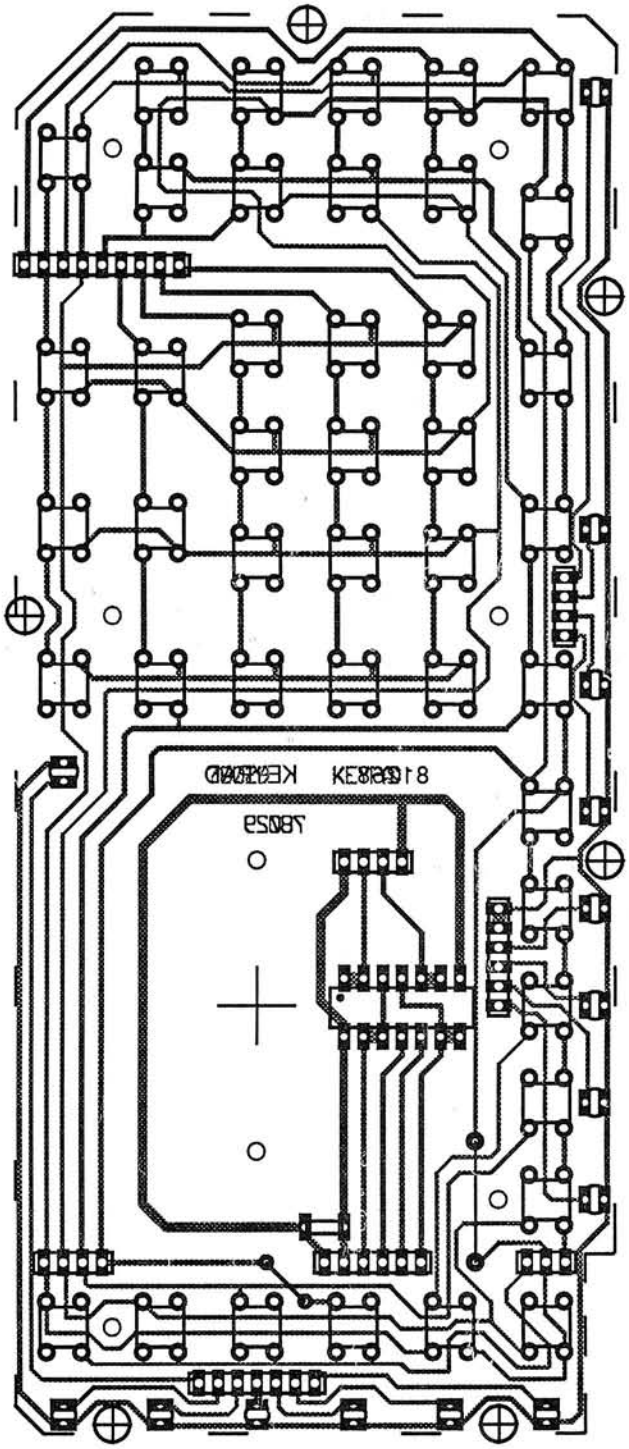


FIGURE 6-65. KEYPAD BOARD CIRCUIT TRACE

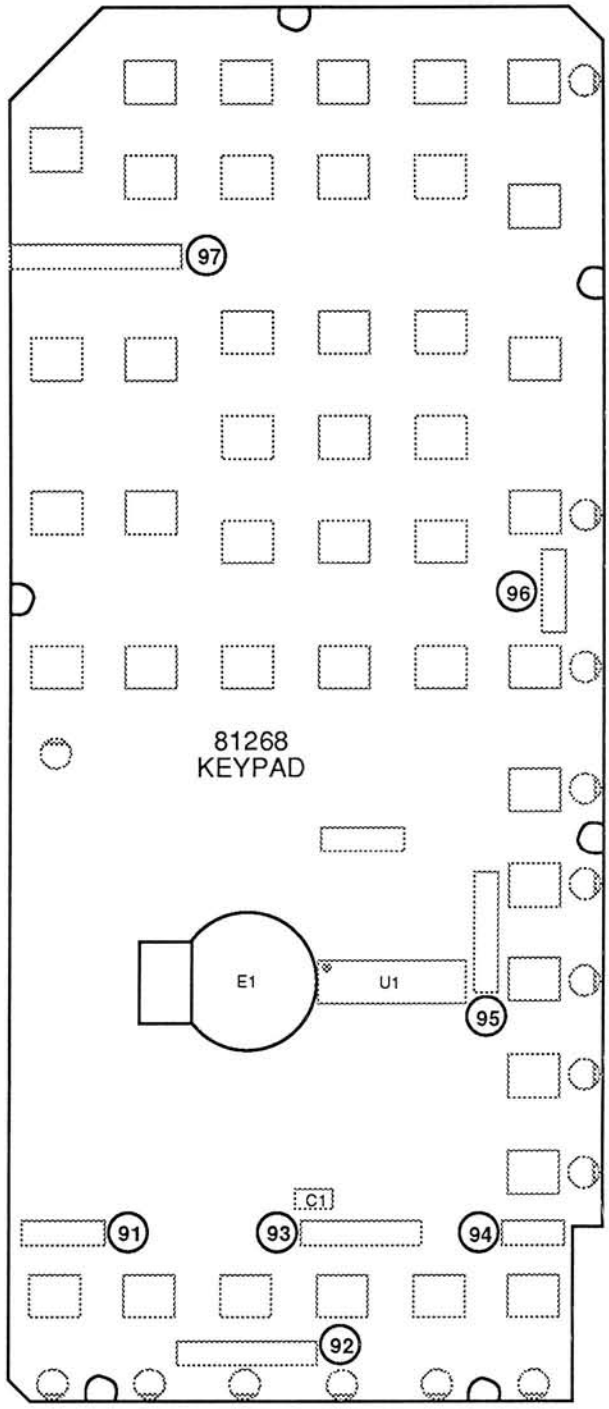
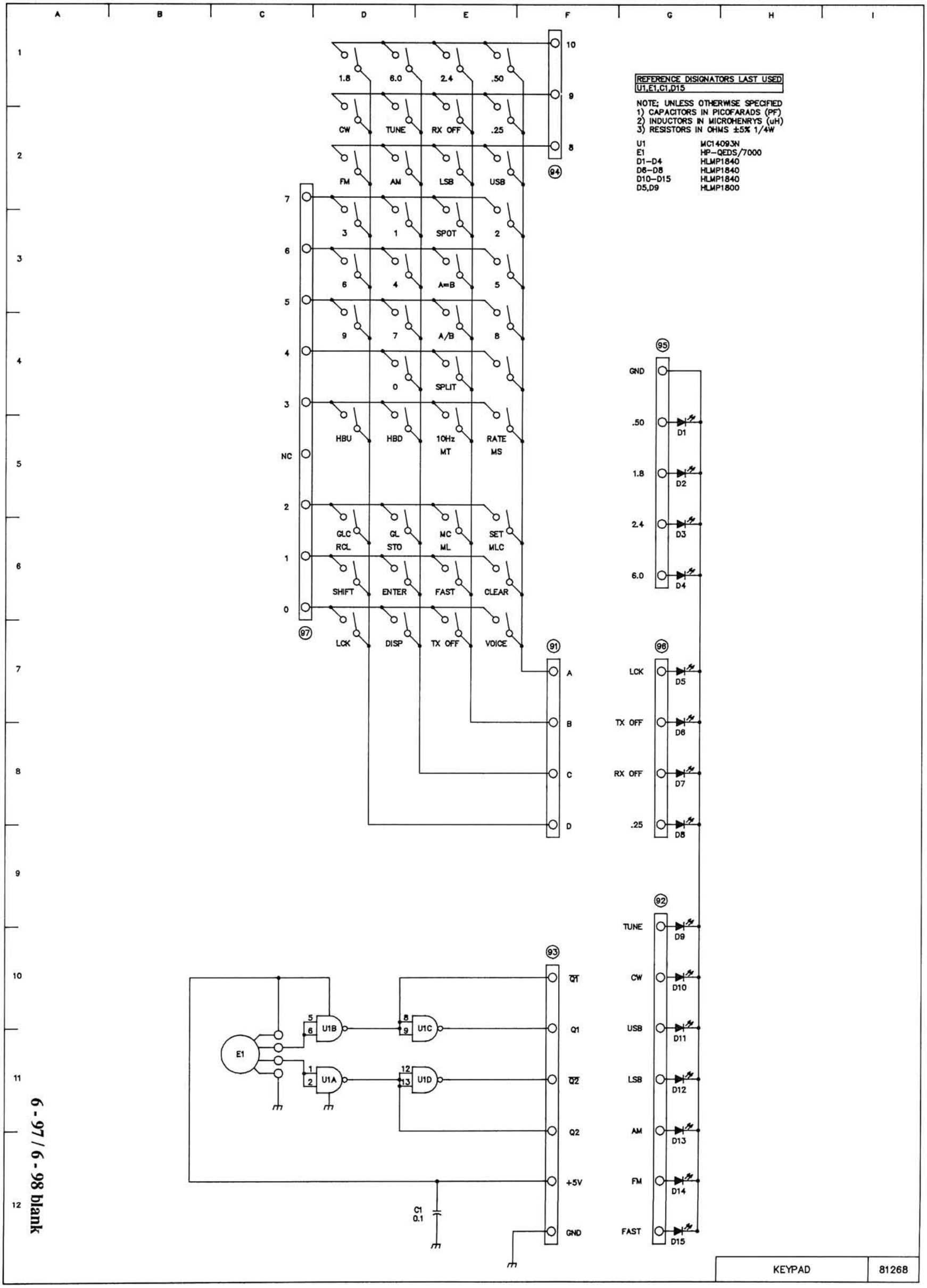


FIGURE 6-66. 81268 KEYPAD BOARD COMPONENT LAYOUT



6 - 97 / 6 - 98 blank

KEYPAD	81268

6-24 VF DISPLAY CONTROL BOARD (81359)

This board contains a microprocessor, U1, which is used the control all operations of the vacuum fluorescent display system. Also on this board is a DC-to-DC converter used to generate the +30 volts required to drive the display. There is also a low current +5 volt regulator, U3, which provides power for U1 and the digit drivers on the VF Display Board.

Microprocessor U1 receives information from the main microprocessor, located on the Logic Board, via the 8-bit data bus DD0-DD7. When the main microprocessor wishes to update the display, it latches the data on the DD0-DD7 bus and then pulses the IRQ line (on connector C) low. This tells U1 that it has data on the bus to be processed. At this time, U1 sets the BUSY line (on connector D) high to tell the main microprocessor that it is busy processing the data. After it has finished processing the data byte, U1 sets the BUSY line low again and the main microprocessor continues sending the next byte of information. This back and forth exchange continues until U1 has received information for all twenty digits in the display. When it is not processing data from the main microprocessor, U1 is generating the required scanning signals for the drivers on the VF Display Board. The speed at which U1 operates is controlled by crystal Y1 (5.99 MHz). This clock signal is internally divided by four to yield an internal bus frequency of approximately 1.5 MHz and an execution cycle time of about .66 μS.

The DC-to-DC converter consists of U2, a free running oscillator, and a voltage tripler circuit consisting of diodes D2-D6 and capacitors C9-C14. In addition, D1, a 9.1 volt zener diode, helps provide some degree of voltage regulation. The frequency of oscillation of U2 is conrolled by C1 and the combination of R1 and R2. The ratio of R1 and R2 is selected so that the output signal appearing at pin 3 of U2 is a square wave of 50% duty cycle. There are two output voltage levels available from the DC-to-DC converter. The normal output is about +30VDC, but a lower value of about +20VDC is also available for providing a dimmer display if desired. These are selected by the jumper plug connected to the mass term connector with +VEE on it.

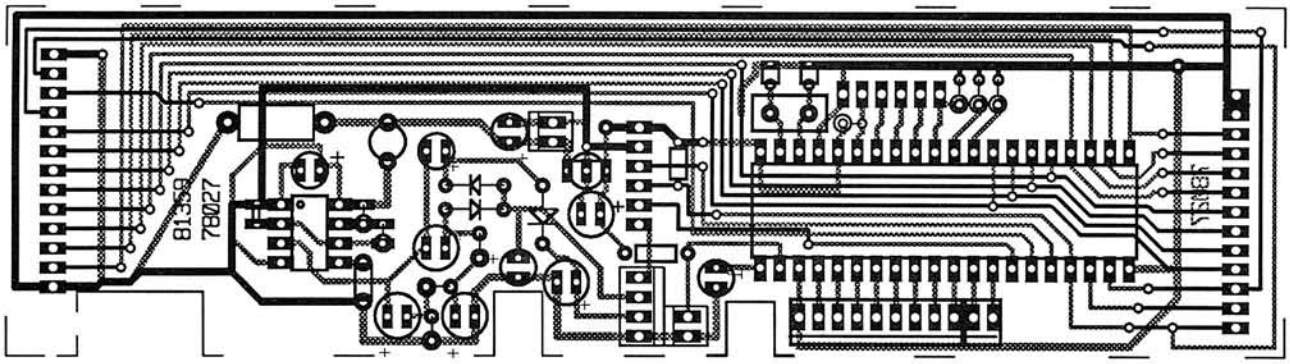


FIGURE 6-68. 81359 VF DISPLAY CONTROL BOARD CIRCUIT TRACE

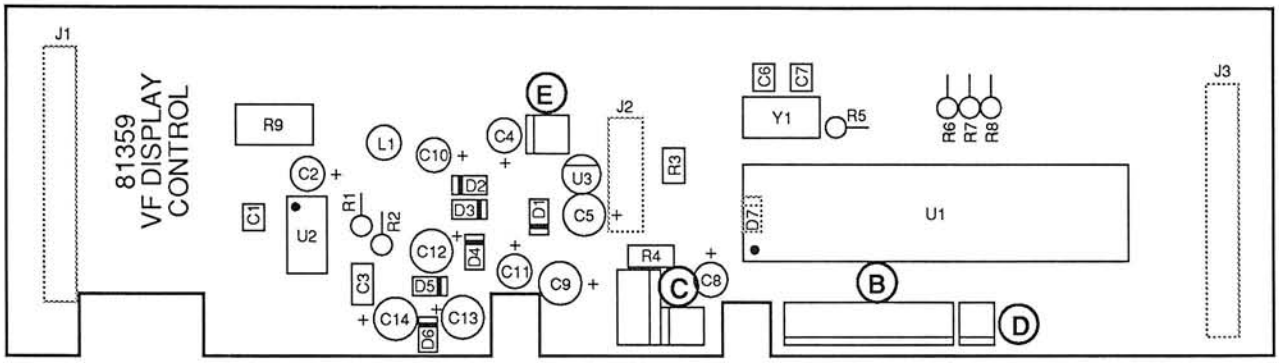
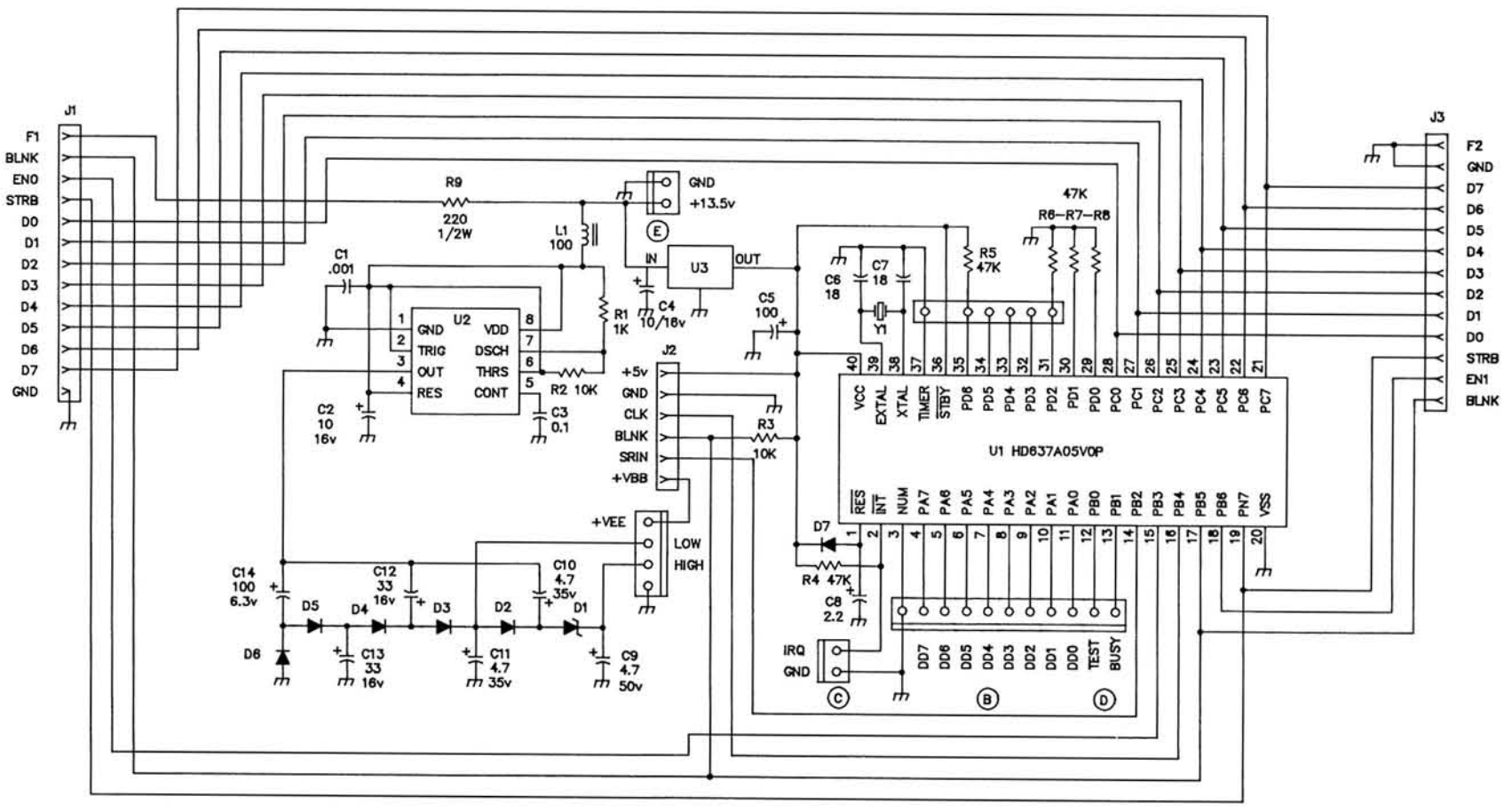


FIGURE 6-69. 81359 VF DISPLAY CONTROL BOARD COMPONENT LAYOUT



REFERENCE DISIGNATORS LAST USED
C14,D7,L1,R9,J3

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

U1	–	HD637A05V0P
U2	–	NE555N
U3	–	LM2931Z5P
D1	–	1N751,9.1 Volts
D2–D7	–	1N4148
Y1	–	5.9904 Mhz

6 - 101 / 6 - 102 blank

DISPLAY CONTROL	81359

6-25 VF DISPLAY BOARD (81269)

This board contains the twenty character alphanumeric vacuum fluorescent display, DISP1, and the segment and digit driver integrated circuits required to drive the display. Also on this board is an array of 8 LEDs used to annunciate the various display modes currently in use.

The display segments (SGA - SGO, PNT) are driven by integrated circuits U1 and U2, which are latched 8-bit parallel high voltage drivers. The data for each of these devices is provided by the microprocessor on the VF Display Control Board via the 8-bit data bus (D0-D7). When the EN0 line of P1 goes high, U1 is enabled. The STRB line is then pulsed high to load the data for U1 into the latches. Likewise, when EN1 goes high, U2 is enabled and when STRB is pulsed high its data is latched.

The display digits (DG1-DG10) are driven by U3, while digits (DG11-DG20) are driven by U4. These are both 10-bit, serial input, latched high voltage drivers. Data for each device is sent by the microprocessor on the VF Display Control Board via the SRIN line of P2. This data is clocked into each device by a low to high logic transition on the CLK line of P2. These two drivers are connected in cascade such that the serial output data (SDO) of U3 is connected to the serial data input (SDI) of U4. Therefore, all twenty bits are loaded serially by the microprocessor.

Since this is a multiplexed display system (only one digit is turned on at a time), the display must be blanked while data is being loaded and latched. When the BLNK line goes high, all drivers are turned off causing the display to be blanked. For best viewing contrast and minimum ghosting, the digits are turned on for approximately 500 µS, and blanked for 100 µS. The digits are scanned from left to right (DG1 to DG20).

Power for the display drivers is provided by the +5V pin on P2. Pin +VBB provides the high voltage (+30 VDC) required to drive the vacuum fluorescent display DISP1.

Connector 98 provides signals for the LEDs used to annunciate VFO A, VFO B, SPLIT, and TAG. Connector 99 provides signals for OFF. and MEM. LEDs. Connector A provides signals for DATE and TIME LEDs.

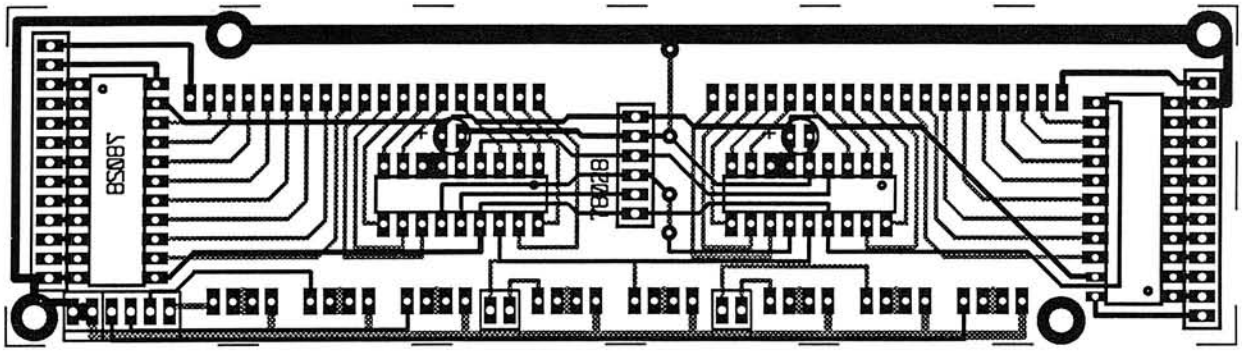


FIGURE 6-71. 81269 VF DISPLAY BOARD CIRCUIT TRACE

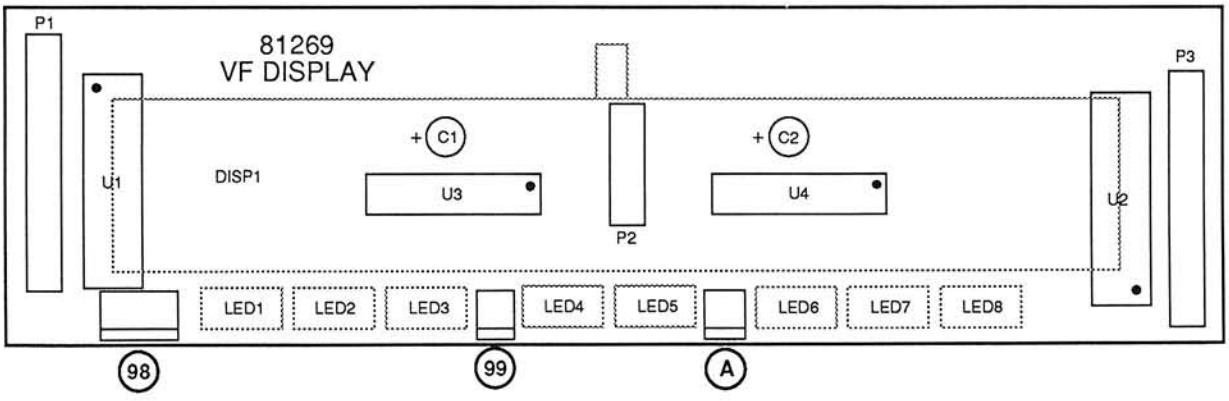
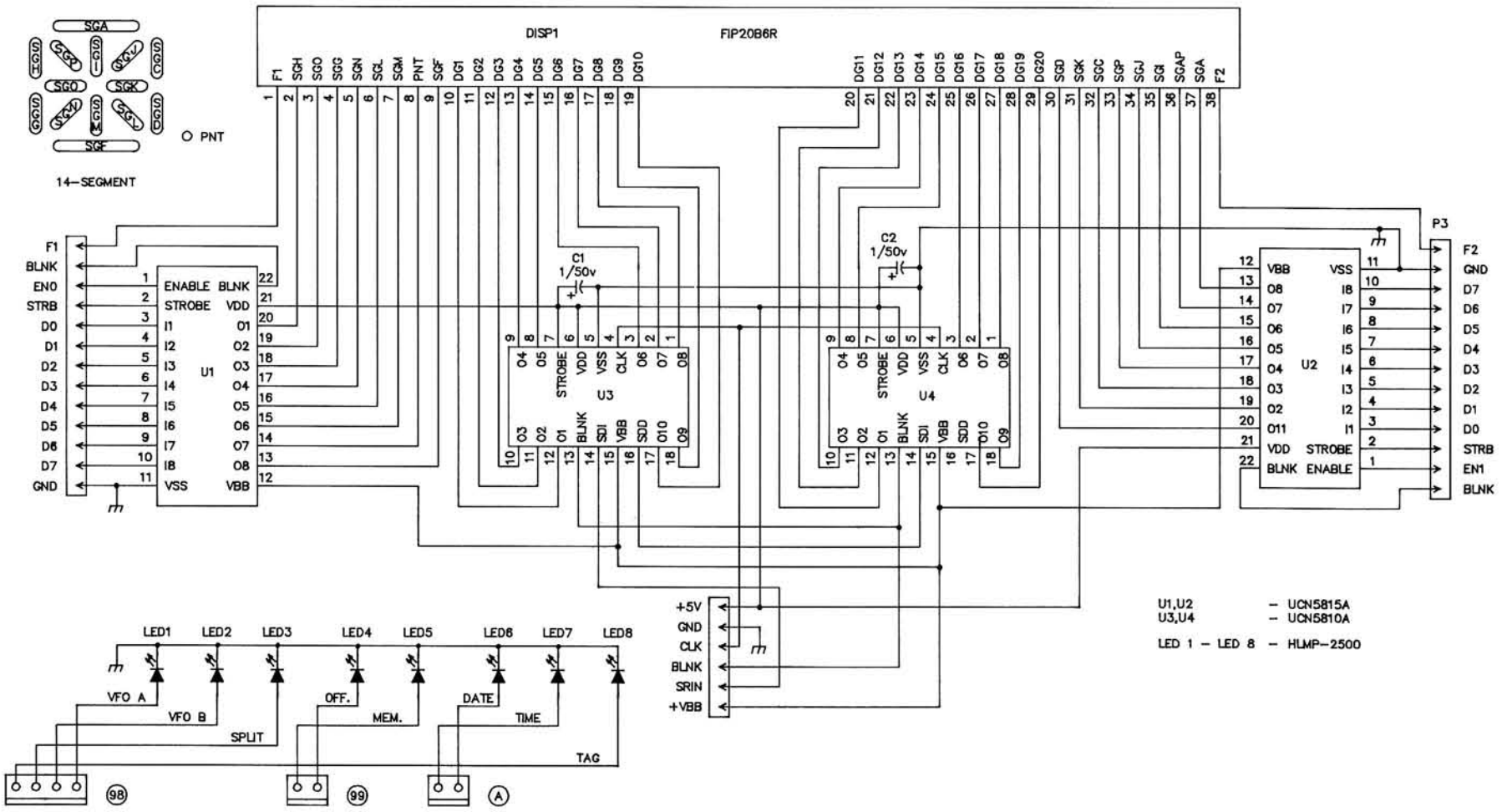


FIGURE 6-72. 81269 VF DISPLAY BOARD COMPONENT LAYOUT



6 - 105 / 6 - 106 blank

VF DISPLAY	81269

6-26 DC POWER BOARD (81328)

This assembly contains a DC power relay, controlled by the front panel POWER switch, which connects 13.5 Volts DC from the external power supply to the main 13.5 Vdc power buss in the transceiver. This board has a fuse (AGC 25 Fast Blow) which provides short circuit and reverse polarity protection, and also contains the current shunt resistor which is used to sample the final amplifier collector current.

A pin on connector 2 carries a continuous 13.5 Volts to the logic board memory keep alive circuitry to retain microprocessor memory when the front panel POWER switch is turned off. (A 9 Volt battery can be installed on the logic board to retain memory when the external 13.5 Volt source is removed.)

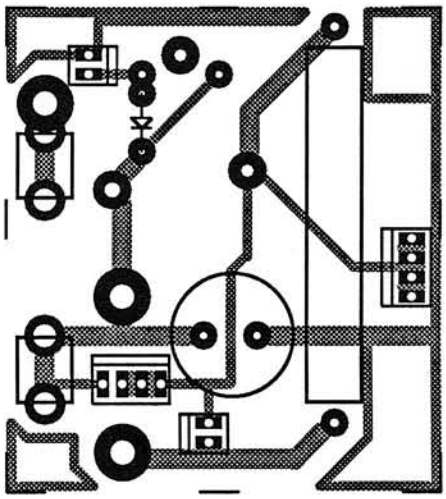


FIGURE 6-74. 81328 DC POWER BOARD CIRCUIT TRACE

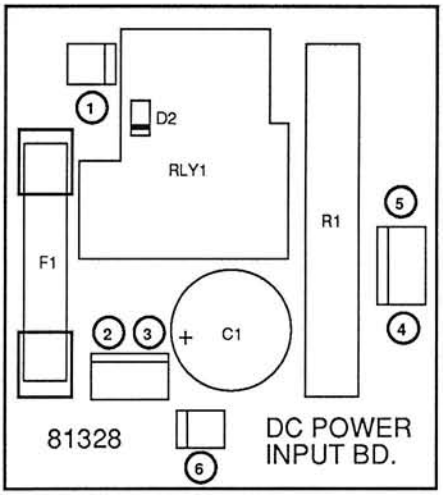


FIGURE 6-75. 81328 DC POWER BOARD COMPONENT LAYOUT

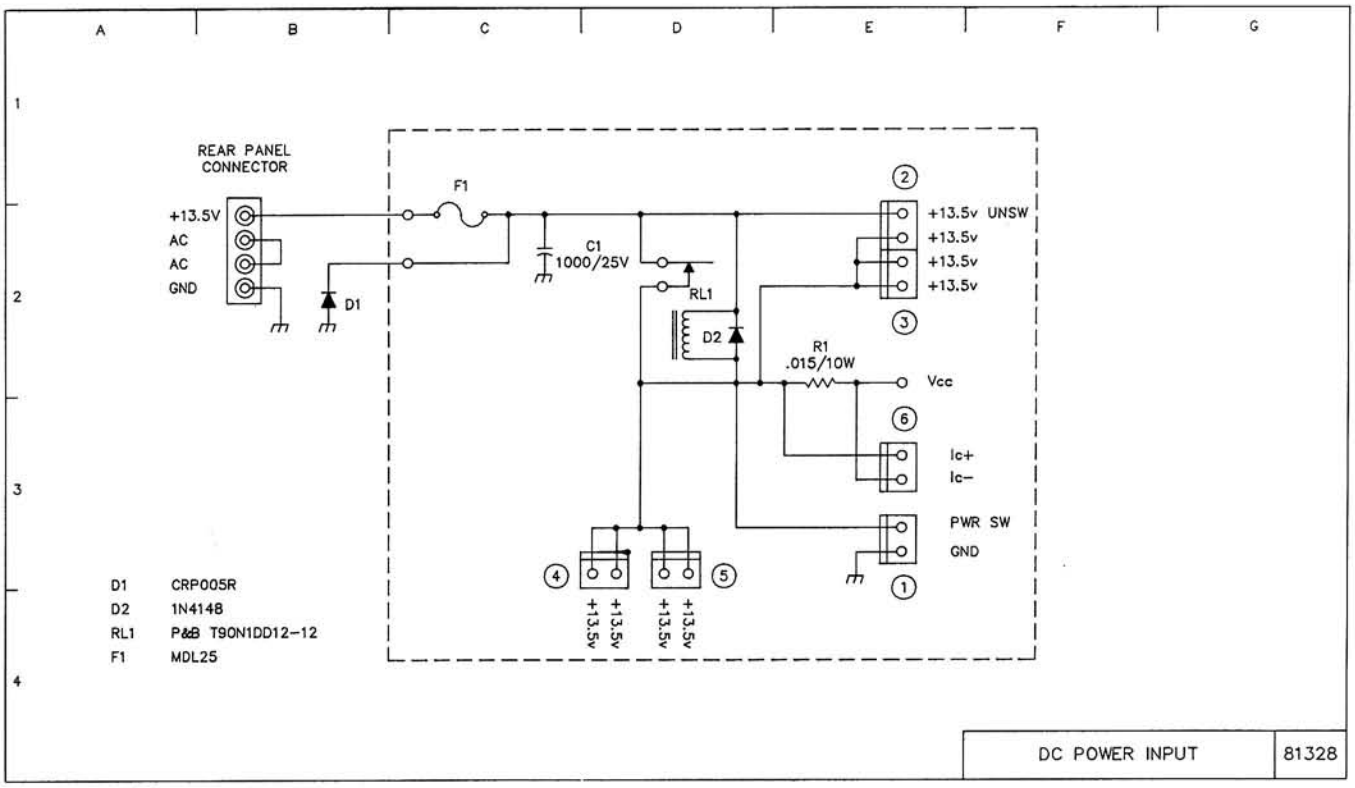


FIGURE 6-76. 81328 DC POWER BOARD SCHEMATIC

PARAGON

MANUAL ADDENDUM

SOFTWARE VERSION DISPLAY

Transceiver control software versions 3.4 dated Mar 30, and later do not have the version display feature activated by pressing "SHIFT-ENTER." This feature was deleted to make room for the "VOICE" and "RS-232" accessory board interface programs. If your version display feature is operational, you do not have the accessory interface programs and if either of the accessory boards are added the software chip must be changed.

There two ways to determine the software version in your Paragon.

1. Press the "DISPLAY" button to show the "date" display. If the date has not been programed the "default" date will be displayed. If the date has been programed it will be necessary to press the "re-set" button on the right side of the cabinet. (NOTE: PRESSING THE RE-SET BUTTON DUMPS ALL INFORMATION THAT YOU HAVE STORED IN THE MEMORIES.) The current program, as of July 13 1988, is dated June 15 and is version 3.7.

2. Remove the top cover and read the version number on the program chip. (The first vertical board on the right side of the chassis.)

CW "SPOT" FUNCTION

Effective with software version 3.4 dated MAR 30, the "SPOT" button works as a "REVERSE" button. The 750 Hz offset in the original program has been deleted. When "SPOT" is pressed the receiver monitors the frequency programed into the opposite VFO or offset. If you are operating simplex, pressing "SPOT" has no effect. For normal CW operation zero beating a signal is not necessary. If you do want to zero beat the incoming signal, press the USB or LSB mode and the 2.4 kHz filter. Tune the signal to zero beat. Press the CW mode button. You are exactly on the frequency.

VFO MEMORIES

Also effective with version 3.4, mode and filter selected are stored in the VFO A/B memories. This is useful if, for example, you are tracking a pileup on CW and one on SSB. One caution, the Paragon will not operate "SPLIT" unless both VFO's are in the same mode. You cannot use "SPLIT" to operate cross-modes. To restore "SPLIT" operation select the desired VFO and press "A=B".

"FAST" TUNING

The original scheme was to have the tuning rate increase as the tuning knob speed was increased. This proved to be annoying because of the resulting "over-shoot" problem. When fast tuning the band you would pass a signal of interest by a half-turn of the knob. By nature, you would tune back at a slow rate and it would take two revolutions of the knob to find the signal. The tuning rate in "FAST" is in 20 Hz increments and the normal rate, 10 Hz.

NICAD BATTERY MEMORY POWER

When you purchase a new nicad battery it is not charged. If you have an appropriate charger, use it to charge the battery. If you install the battery in your Paragon without pre-charging, leave the Paragon power supply turned on for at least 48 hours.

MODE/FILTER SELECT

Effective with Version 3.7 dated June 15, the filter selected does not change when the mode is changed.

CHANNEL SCANNING RATES

Version 3.7 dated June 15 has selectable scanning rates from 4 channels per second to one channel every 9 seconds with a total of ten rates.

CW OFFSET

CW operation uses USB on all bands. With version 3.4 dated March 30, the frequency display is offset 700 Hz. The display reads the carrier frequency when you are listening at a 700 Hz tone. This eliminates the risk of out of band operation while the display is telling you that you are in the band.

TROUBLE SHOOTING

1. If the control line voltage for a linear amplifier exceeds 15 volts, we recommend the use of an external relay. The external relay can be controlled by the N/O relay built into the Paragon. The transients induced by keying higher voltages with the internal relay can cause the Paragon micro-processor to lock-up.

2. No output on SSB can be caused by having the speech processor turned on and the processor gain control turned down.

3. If the microprocessor locks up it may be necessary to disconnect the internal memory back-up battery to enable the reset button.

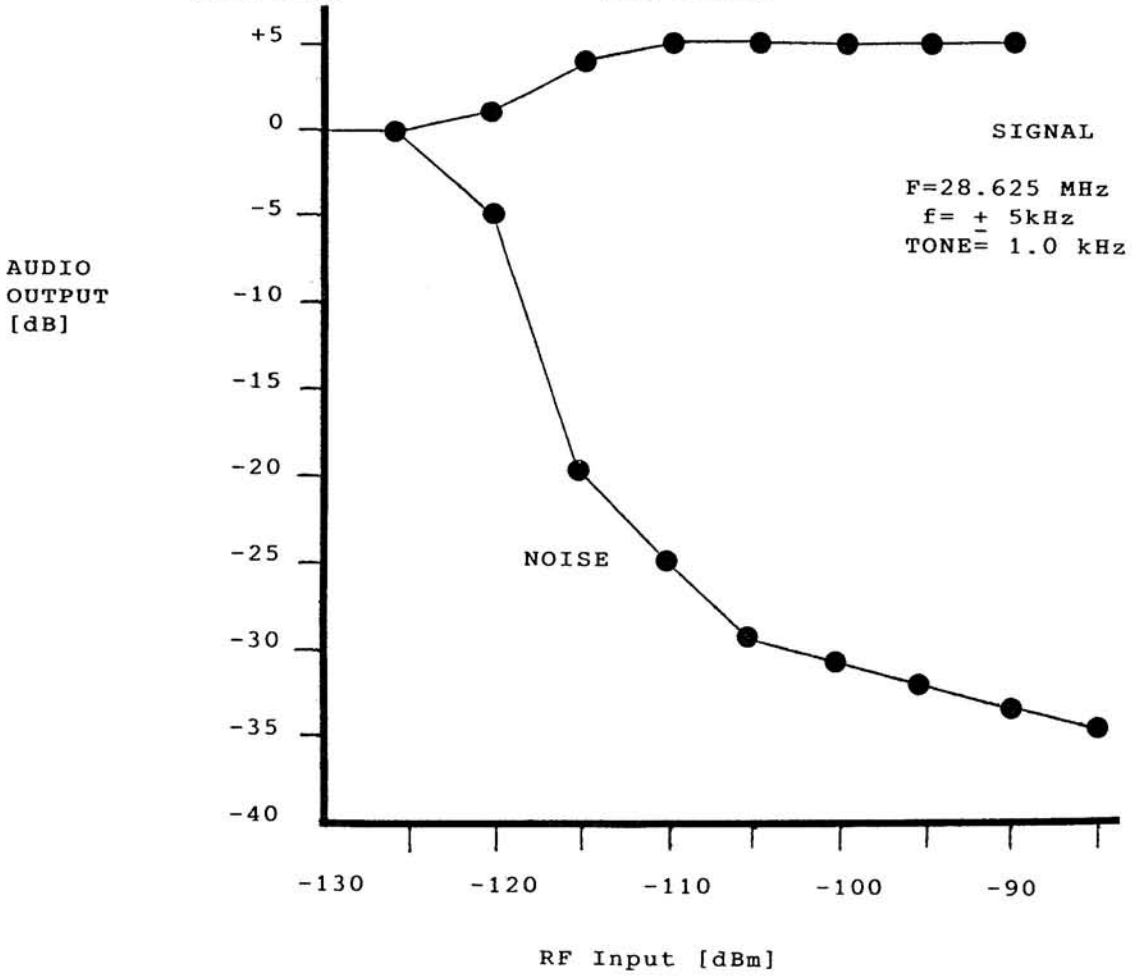
MODEL 256 FM OPTION

Introduction:

The Model 256 FM Option board allows Ten-Tec Paragon owners to transmit and receive narrow band FM (F3E) signals. The easily installed circuit board hooks to the Paragon circuitry through five cables which carry power, audio and RF signals to and from the FM option.

Specifications:

Sensitivity	0.3 mV for 12 dB SINAD (1.0 kHz tone @ 5 kHz dev.)
Receive Bandwidth	15 kHz
Quieting	See Below



Transmit carrier	Adjustable 15W to 100W with ALC
Transmit deviation	Limited to +/- 5 kHz

Installation:

Step One: Check your parts. The FM Option kit includes the circuit board assembly, four 4-40 x 3/8" phillips head screws and five cable assemblies.

Step Two: Begin by removing the top and bottom covers of the Paragon and then remove the lower shield on the bottom of the unit.

Step Three: Orient and screw down the FM Option board as shown in Figure One. Attach cables (S) and (T) from the FM board to the L.L. DRVR/N.B. board. Note that these and the other three cables are symetrical and either end can be plugged into either connector.

Step Four: Install cable (75) from the TX Audio/BFO board to the FM Option. Now connect cable (U) to the FM Option and feed the loose end through the large grommet as shown. Turn to the bottom of the radio and plug the loose end into the IF/AF board adjacent to connector (51).

Step Five: Run cable (33) from the FM Option through the grommet and along the center partition in the bottom of the radio. About half way back, bend the cable leftward and through a slot into the 2nd mixer compartment. Plug the cable into connector (33) on the second mixer board.

Step Six: This completes the installation, but before attaching the shield and top and bottom covers, power up the Paragon. Verify that in receive the Paragon now has FM type white noise hiss with the FM mode selected. Also verify that FM transmit generates a CW carrier which can be controlled by the ALC adjustment.

Step Seven: If everything is in order, reattach the bottom shield. Watch carefully that all wires and cables are seated in their slots along the various partitions. Replace the top and bottom covers and the Paragon is ready to put on the air.

Operation:

F3E narrow band FM is authorized for use in the same spectrum authorized for SSB. The operation of the Paragon on FM is much the same as SSB except the front panel mic gain adjustment is not used. To operate FM, select the desired frequency, select the FM mode and adjust the RF output level for 50 to 75 watts out. FM is a "key down" mode and if you operate at higher power levels, some auxiliary cooling air on the power amplifier heat sink is recommended.

On the 10 meter band there are some FM repeater operations that are interesting. These repeaters normally operate above 29.6 MHz. Your transmit frequency will normally be 100 KHz below the receive frequency. You use VFO A and VFO B to set up the desired frequency pair and operate in the SPLIT mode. Be sure that both VFOs are set up for FM operation.

In the FM mode, transmit audio levels and frequency deviation are factory preset with internal adjustments.

Circuit Description:

The Model 256 FM Option board consists of two signal paths. On trasmit the board receives audio from the TX Audio/BFO board through connector 75. After processing the audio, the board generates a 9.000 MHz FM carrier for the transmitter at connector 33. On receive a 9.000 MHz IF signal is extracted from the noise blanker at connector T and demodulated into an audio signal at connector U.

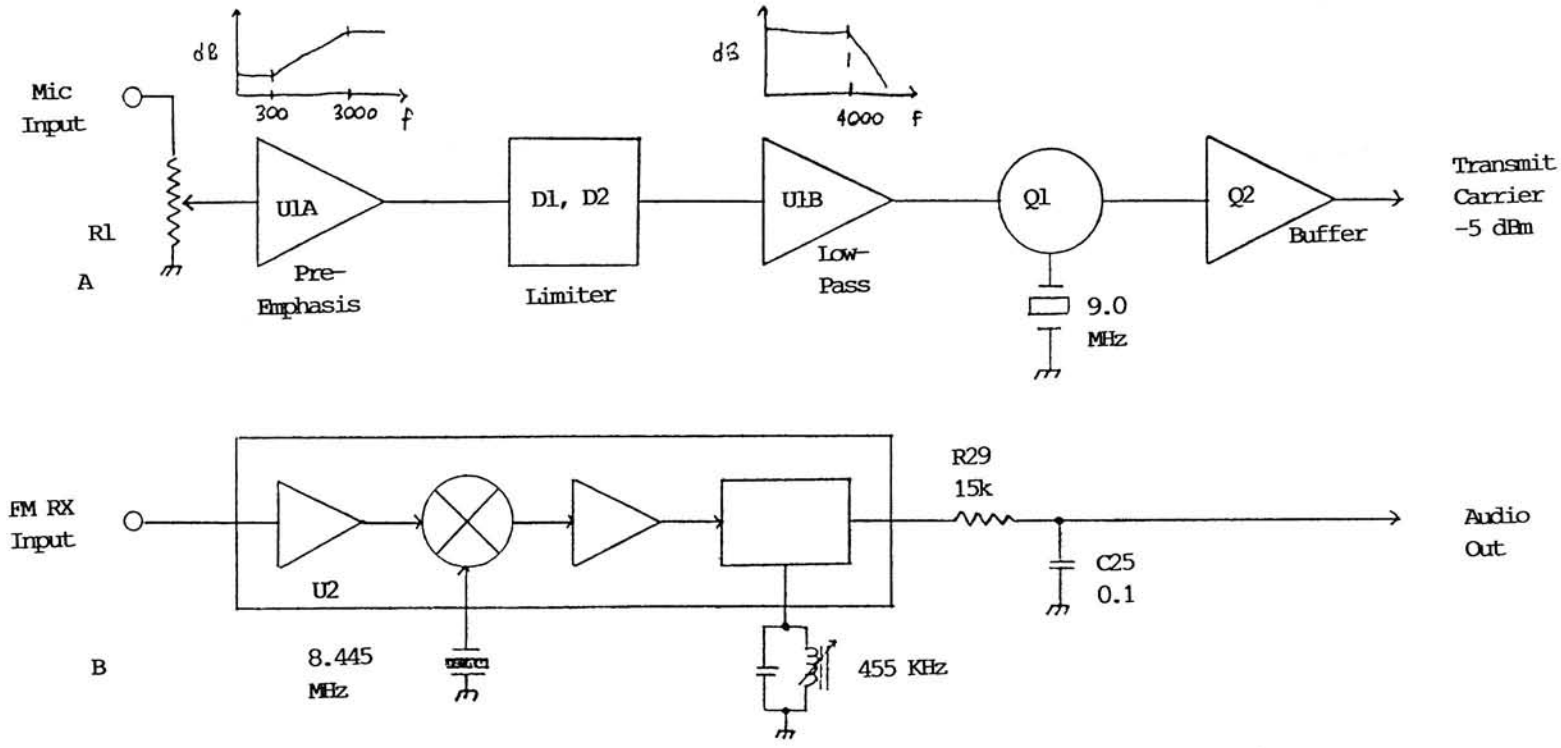


FIGURE TWO: Block diagram of the FM transmit functions (A) and single chip receiver (B) on the Model 256.

Figure 2A illustrates the transmit functions. Connector 75 receives an amplified microphone signal from the TX Audio/BFO board. Trimmer R1 adjusts the level of the mic signal into the preemphasis network around U1A. The preemphasis provides a high-pass type response of +6 dB/octave over the 300 to 3000 Hz audio range. Analysis of the FM reception of speech signals shows that processing of this type on the transmit end and a reciprocal de-emphasis at the receiver can improve noise performance several dB.

Diodes D1 and D2 limit the peak-to-peak amplitude of the processed audio to prevent over deviation of the FM carrier. In practice R1 is adjusted for a particular microphone so that limiting occurs only occasionally.

Lowpass filter U1B filters harmonic distortion from the limiter and adjusts the amplitude of the audio for varactor D3. The varactor performs the voltage to frequency conversion in the Colpitts oscillator Q1. The reactive network between D3 and the 9.000 MHz crystal Y1 lets the oscillator swing symmetrically about a 9.000 MHz center frequency. L1 is adjusted to center the oscillator at 9.000 MHz with no audio bias. Buffer transistor Q2 isolates the oscillator and provides about -5 dBm carrier to the next transmitter stage on the second mixer board. At this point the transmitter treats the FM carrier as if it were CW.

Figure 2B shows the receive path through U2. The FM receive signal is tapped off of the noise blanker 9.000 MHz IF and enters the FM Option board at connector T. The signal feeds an LM3361N receiver chip which converts down to a 455 KHz IF. Cermanic filter CF1 sets the receive bandwidth for the on-chip quadrature detector. T1, the quadrature coil, is adjusted for maximum recovered audio and minimum distortion. The audio signal is de-emphasized by the lowpass network of R29 and C25 and is carried on to the IF/AF board through connector U.

The S-meter, squelch function, tone control and other operations are still accomplished by the IF/AF board where the SSB/CW IF system operates concurrently and in parallel with the FM receiver chip on the option board.

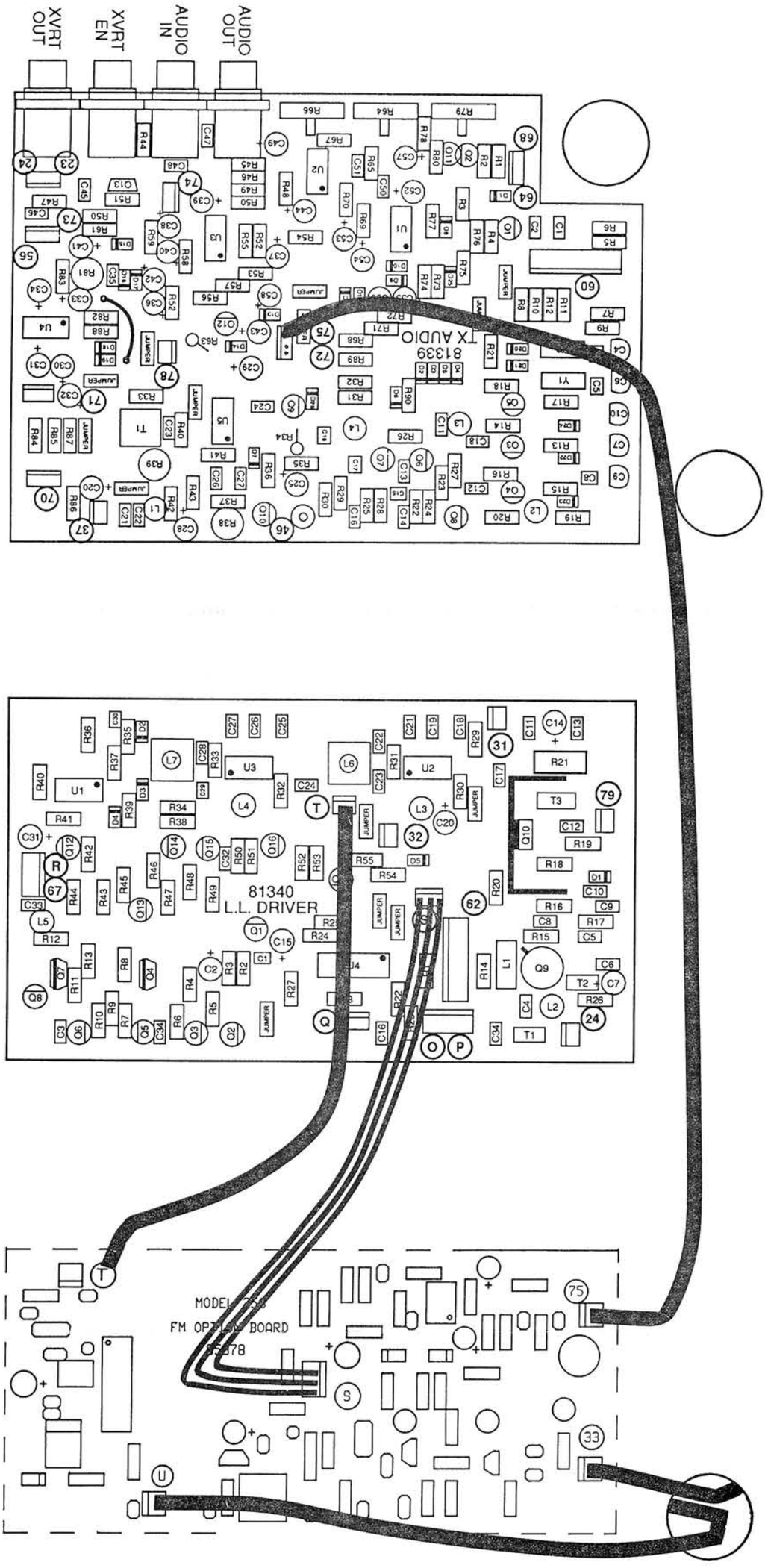
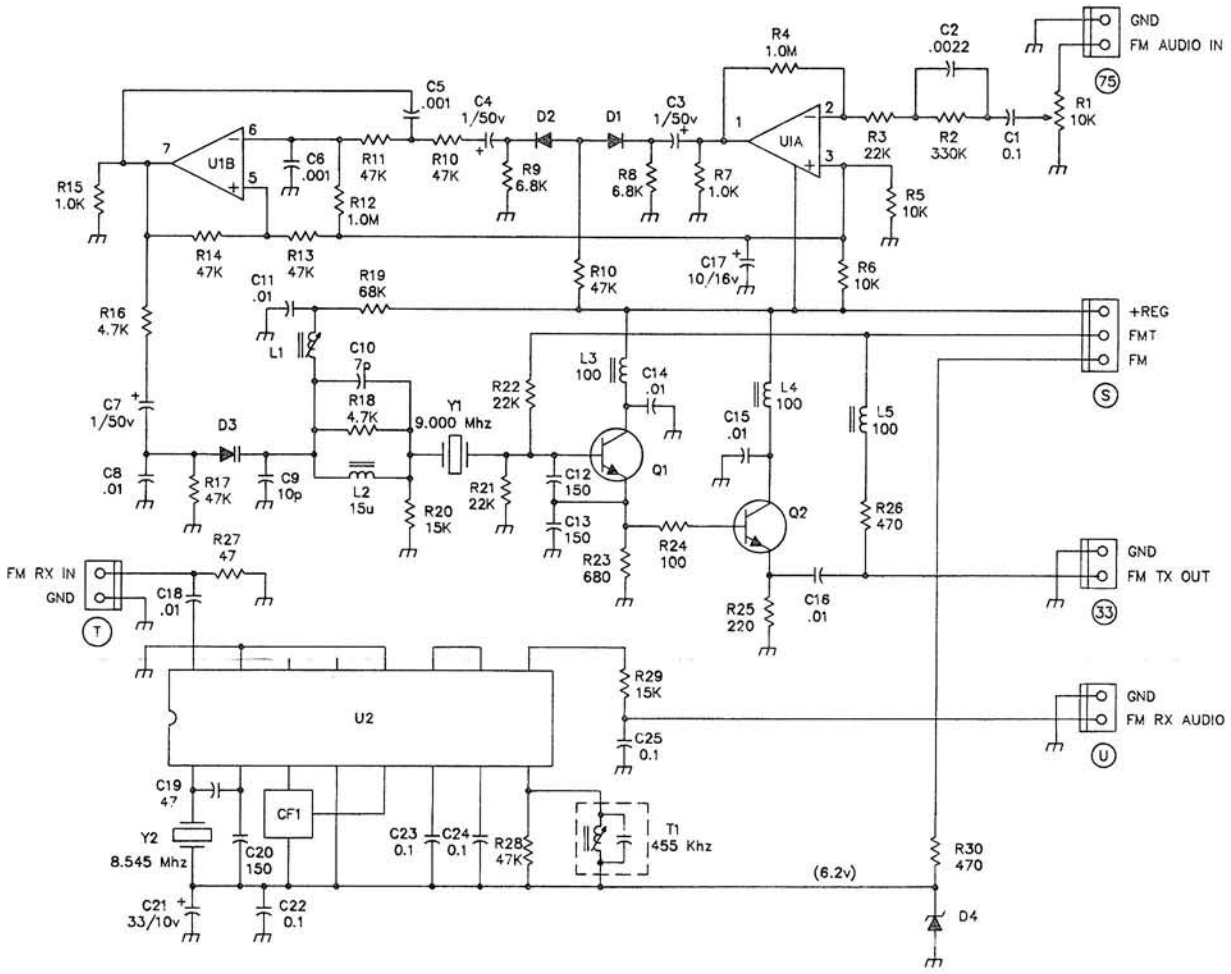


Figure One: Pictorial view of the top left-hand interior of the Paragon. The FM Option board screws down to four pressed in standoffs on the PLL cage cover.



U1: LM358N
U2: LM3361N
Q1-Q2: MPS-3693
D1-D2: 1N4148
D3: MV209
D4: 1N753A
Y1: 9.000 Mhz
Y2: 8.545 Hhz
CF1: CFU455E

REFERENCE DISIGNATORS LAST USED
C25, R30, L5, D3, Q2, U2

NOTE; UNLESS OTHERWISE SPECIFIED
1) CAPACITORS IN PICOFARADS (PF)
2) INDUCTORS IN MICROHENRYS (uH)
3) RESISTORS IN OHMS ±5% 1/4W

FM OPTION BOARD	81404

TEN-TEC MODEL 960 POWER SUPPLY/SPEAKER

GENERAL

The Model 960 Power Supply is designed to power the TEN-TEC models 560/561 and 585 transceivers. The supply delivers 20 Amps at 13.5 Vdc from a 115/230 Vac 50-60 Hz source. Circuit features include an electronic over-current sensor which shuts off the output if the current demand exceeds 22 Amps. The over-current shut down condition is reset by cycling the POWER switch from ON to OFF and back to ON. Output over-voltage protection is also included to prevent the output voltage from exceeding 16.0 Vdc.

The output voltage is available through a heavy duty 3 foot cable and connector. The cable carries +13.5 Vdc, ground and the "hot" side of the ac primary and mates directly to the POWER jack on the 560/561 and 585 transceivers. Two RCA phono jacks on the back of the supply also provide +13.5 Vdc for low current (2 or 3 amps) auxiliary applications.

INSTALLATION

Any high current loads should be drawn from the 4 pin connector at the end of the output cable. Pin 1 (black wire) is the chassis ground and high current return. It is identified by a rib on the plastic shell of the connector. Pins 2 and 3 (white wires) are connected in series with the front panel POWER switch and carry the "hot" side of the the 115/230 Vac line. These two lines facilitate remote ON/OFF switching of the power supply. Pin 4 (red wire) is the +13.5 Vdc output.

If the supply is to be used with equipment other than TEN-TEC transceivers, pins 2 and 3 must be connected together to turn on the supply. These two pins are at 115/230 Vac and carry up to 3 Amps under full load. If the cable length must be extended for some application, a heavy gauge wire, at least #14, must be used. Significant voltage drops can occur even in heavy cable with a 20 Amp load. Maximum length should be 4 feet. When using the supply with the 560/561 or 585, provide a good interchassis connection by running a separate heavy braid or wire between the ground posts on the rear panels. In rf communication systems, a connection from chassis to earth ground is simply good practice.

The phone jacks marked AUX +13.5 V are connected in parallel with the high current output cable. Each may be used to power auxiliary equipment that does not draw more than 3 Amps. The center terminal is positive, the shell is ground.

If you wish to use the built-in speaker, insert the 1/4" phone plug, cabled through the back of the supply, into the EXT SPKR jack of the transceiver.

230 Vac OPERATION

Before operating the supply from 230 Vac, the line voltage selector switch on the bottom of the supply must be moved with a screwdriver blade to display "230". Next replace the back panel line fuse with the MDL 2 type fuse contained in the packing kit.

If the ac line plug is to be replaced for 230 Vac operation, please preserve the original line, neutral and ground connections. In the line cord itself, the center green conductor is chassis ground and should be wired to pick up ground in the house wiring. The neutral side of the ac is carried on the side of the line cord which has small grooves along the length of the outer insulation. The "hot" ac line is carried in the conductor covered by the smooth insulation.

CAUTION

NEVER operate the power supply from 230 Vac when the line voltage selector switch is in the 115 position or visa versa.

OPERATING HINTS

1) Connect the line cord to a proper source of voltage. This is a three wire plug and is intended to pick up the ground of the ac house wiring. Do not defeat the ground connection by using an adapter plug.

2) Connect the load to the 4 pin connector as described above.

3) Turn on the unit and check that the front panel indicator lights. This LED is powered directly from the regulated output and will always indicate the over-current shut down condition by going out.

4) To reset the over-current trip out, turn off the unit with the front panel POWER switch, then turn it back on. If the over-current condition remains, the supply will again shut down and the LED indicator will stay out. Remove the source of the overload and reset the supply as before.

5) If the over-voltage protection circuit detects an output over-voltage condition, it will short the output to ground. If the condition was caused by noise on the ac line (near-by lighting strike, etc.) the over-voltage circuit will trigger the over-current shut down and the supply must be reset as before. If, however, the over-voltage condition is the result of a component failure in the supply, the over-voltage circuit will blow the 25 Amp fuse mounted internally on the pass transistor board. If this fuse is blown, it indicates that possibly some internal part has failed and service may be required.

6) FUSES: If the line fuse or internal 25A fuse must be replaced use the identical type fuse.

   Internal 25 A Fuse - AGC 25
   115 Vac line fuse - MDL 4
   230 Vac line fuse - MDL 2

7) HIGH CURRENT OPERATION: Do not place the power supply in a closed area or small space where air cannot circulate freely around the heat sink on the rear panel. This heat sink should have free access to normal air convection currents. Never set anything, books, magazines and so forth, on top of the heat sink or where they can cover the ventilation slots in the side of the supply.

With 20 Amp loads, some voltage drop at the load is unavoidable. The three foot cable and connector to connector interface can account for up to 0.30 Vdc of loss. If pilot lamps in the driver equipment appear to dim or if excessive voltage drop at the load is indicated, the connector should be inspected for dirty contacts and wear. After years of use, the contacts in the connector tend to spread and tarnish and may require cleaning or replacement.

SPECIFICATIONS

Input Voltage: 109-125 Vac or 218-250 Vac, 50-60 Hz.

Output Voltage: 13.8 Vdc, internally adjustable from 11.5 to 15.0 Vdc.

Output Current: 20 Amps full load, 22 Amps maximum for 5 minutes.

Current Limiting: Electronically disables output. Factory set threshold at 22A.

Regulation: - 3% at output connector for no load to 20 A full load.

Ripple: 20 mV peak to peak at 20A.

Speaker Impedance: 8 ohms.

CIRCUIT DESCRIPTION

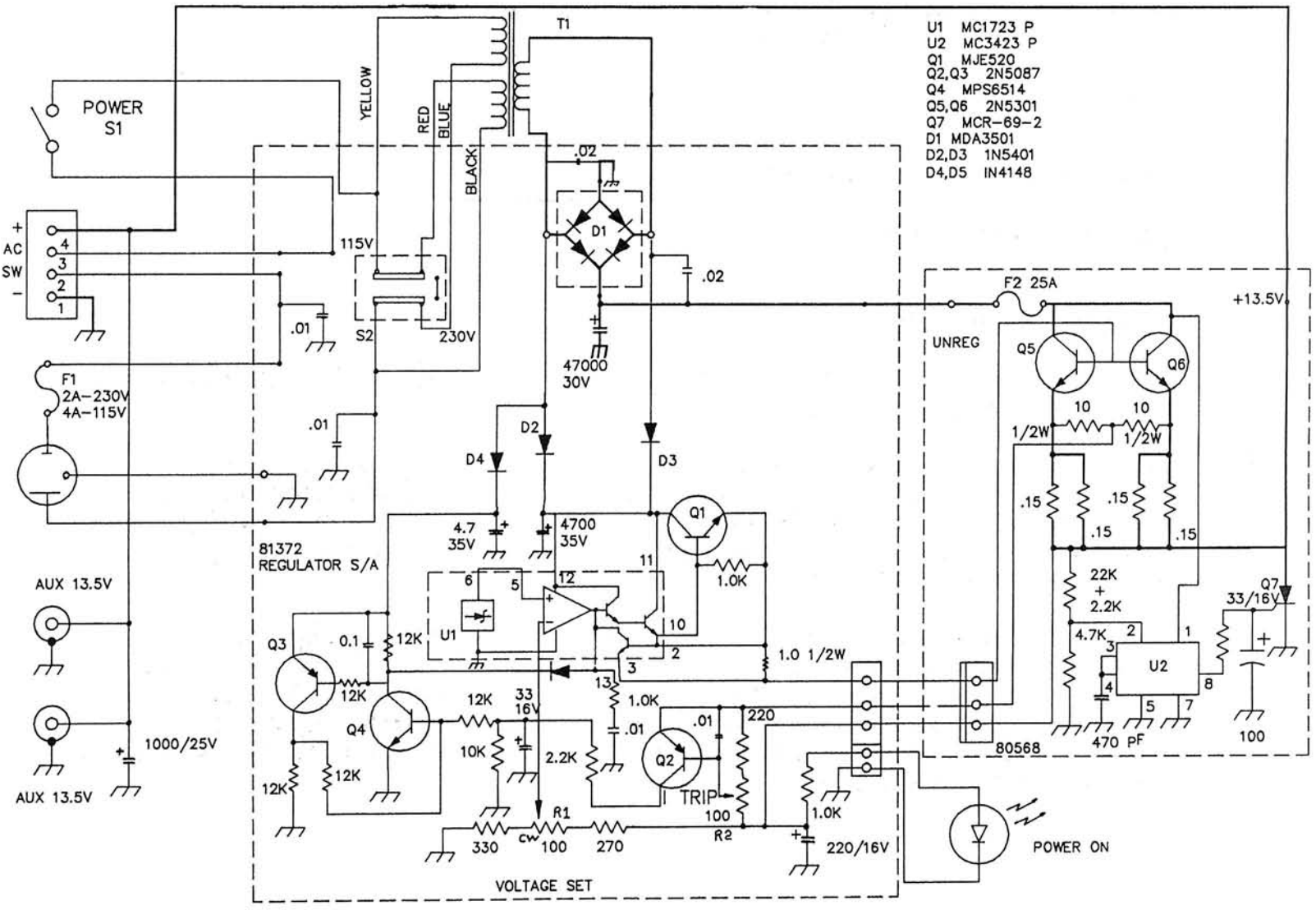
The Model 960 uses a linear series regulator type circuit based on the '723 regulator chip and two 2N5301 pass transistors.

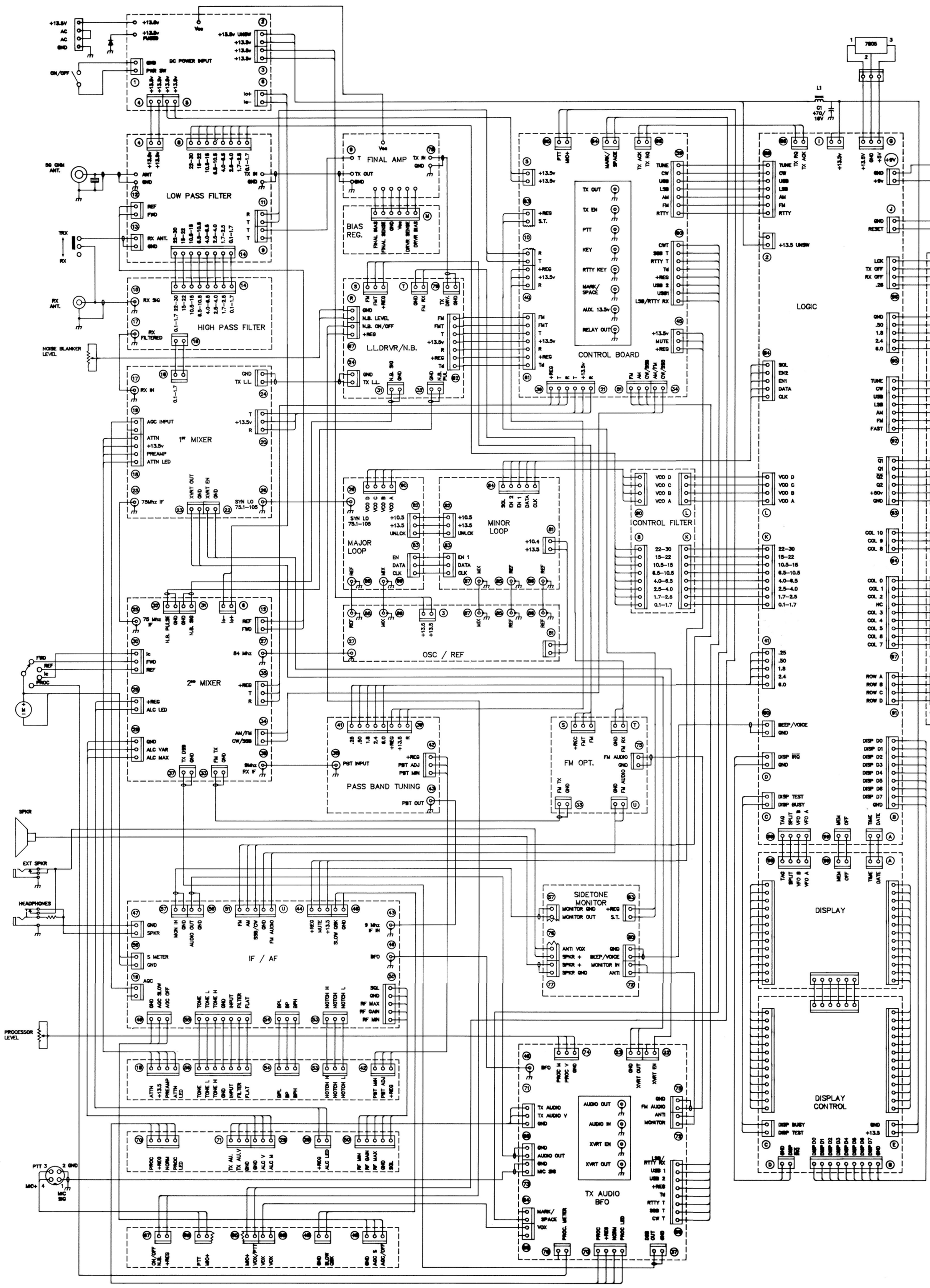
The "hot" side of the ac is fused by the rear panel line fuse F1 then sent down the heavy 4 conductor cable where a jumper or switch at the load end of the cable connects pins 2 and 3. Pin 3 leads back to the POWER switch S1 on the 960 and on to the dual primaries of transformer T1. The voltage selector switch S2 on the bottom of the 960 configures the transformer primary windings for either 115 or 230 Vac.

The secondary of T1 feeds high current bridge rectifier D1 which develops unregulated dc for the pass transistors. Seperate rectifiers D2 and D3 provide dc power for the regulator circuit. Regulator chip U1 compares a sample of the output voltage from R1, the output voltage trimmer, to an on-chip reference voltage. Any difference between the output and reference voltages is amplified and used to correct the bias on transistor Q1. Q1 then drives the bases of pass transistors Q5 and Q6.

The over-current shut-down circuit consists of transistors Q3 and Q4 which form an SCR type latch. Q2 acts as the trigger. Output current is sampled across the 0.15 ohm ballast resistors at the emitters of Q5 and Q6. This voltage drop appears across resistor R2, the over-current set trimmer, and biases Q2. Excessive current drain will develop sufficient voltage across the ballast resistors to turn on Q2 and fire the over-current SCR circuit Q3 and Q4. With Q4 turned on, and latched by Q3, the drive from regulator U1 is shunted to ground through D5. The latching action of Q3 keeps the supply disabled until the over-current circuit is reset by cycling the POWER switch.

Over-voltage protection is provided by U2 and SCR "crowbar" Q7. If the output voltage exceeds the factory set threshold of 15.9 Vdc, U2 will trigger Q7 into conduction and either trip the over-current circuit or blow the internal 25 Amp fuse F2.




DC POWER INPUT
LOW PASS FILTER
HIGH PASS FILTER
1ST MIXER
2ND MIXER
FINAL AMP
BIAS REG.
L.L.DRVR/N.B.
CONTROL BOARD
CONTROL FILTER
MAJOR LOOP
MINOR LOOP
OSC / REF
PASS BAND TUNING
FM OPT.
IF / AF
SIDETONE MONITOR
TX AUDIO BFO
LOGIC
KEYPAD
DISPLAY
DISPLAY CONTROL
AUX 9v BATTERY
MASTER RESET
NOISE BLANKER LEVEL
PROCESSOR LEVEL
SPKR
EXT SPKR
HEADPHONES
PTT 3
MIC+ 4
2 GND
1 MIC SIG