SM-Z-89/90

Computer System

Service Manual

585-7

ZENITH DATA SYSTEMS
SAINT JOSEPH, MICHIGAN 49085

The Z-89/90 Computer System

This Z-89/90 Computer System Service Manual contains service information for the following six Zenith Data Systems products:

1. The Z-89/90 Computers.
2. The Z-89-37 Double-Density Disk Controller.
3. The H-88-1 Single-Density Disk Controller.
4. The H-17-1 Floppy Disk Drive.
5. The H-17-4 Floppy Disk Drive.
6. The WH-88-16 Memory Expansion.

Z-89/90

Computers

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Specifications

CPU AND MEMORY

Processor	Z-80.
Clock	2.048 MHz.
Memory	48K bytes user RAM (expandable to 64K), Z-89 series 64K bytes user RAM, Z-90 series 8K System for ROM and RAM. 8K reserved.

DISPLAY

CRT	12″ diagonal — green phosphor.
Display Format	24 lines of 80 characters (with access to 25th line).
Display Size	6.5″ high × 8.5″ wide.
Character Size	0.2″ high × 0.1″ wide (approximate).
Character Type	5 × 7 dot matrix (upper case); 5 × 9 dot matrix (lower case with descenders); 8 × 10 dot matrix (graphics).
Keyboard	84 keys (60 alphanumeric, 12 function/control) plus a 12-key numeric/control pad.
Cursor	Blinking, nondestructive, underline, block, or disabled (DIP switch selectable).
Cursor Controls	Up, down, left, right, home, CR, LF, back space, tab, and cursor off.
Cursor Addressing	Relative and direct.
Tab	Standard 8-column tab.
Refresh Rate	60 Hz at 60 Hz/50 Hz at 50 Hz line frequency.
Edit Functions	Insert and delete character or line.
Erase Functions	Erase page, erase to end of line, and erase to end of page.
Bell	Audible alarm on receipt of ASCII BEL.
Video	Normal and reverse by character.

SERIAL INTERFACE

Channels	3 EIA RS-232C. Each channel provides serial data and primary RS-232C handshake.
Output Levels	RS-232C.
Input Levels	RS-232C compatible.
Character Length	5, 6, 7, or 8 bits.
Parity	Even, odd, stick, or none.
Stop Bits	1, 1-1/2 or 2.
Baud Rates	All standard rates to 57,600 baud.

GENERAL

Power Requirements	115/230 volts at 90 watts max.
Size	13″ high × 17″ wide × 20″ deep (33 × 43.2 × 50.8 cm).
Weight	46 lbs. (20.7 kg).
Operating Temperature	10° to 35° Celsius.
Storage Temperature	0° to 50° Celsius.

CPU BOARDS Z-89/90

The CPU boards for the Z-89 (HE 181-3396) and the Z-90 (HE 181-3615) are basically the same, with the following exceptions:

	IC U516	IC U518	IC U549	IC U557	IC U558
Z-89	HE 444-41	HE 444-62	HE 443-904	HE 443-912	HE 443-754
Z-90	HE 444-83	HE 444-84	See note 1.	See note 2.	HE 100-1817

NOTE 1: The memory chip is left out to receive the cable from the 16K Memory Expansion Board.

NOTE 2: U557 is left open to receive the interface cable from the Z-89-37 Controller Board.

The Z-90 CPU board has the JJ505 jumper plug removed. Cable (HE 134-1159) is connected from JJ505 to Pin 14 of P508, to enable the 4K ROM at U518.

JJ501 must be jumpered for correct memory size (48K or 64K).

These boards may be interchanged if the above modifications are made. The Z-90 CPU board may be used as a direct replacement if the proper IC's are inserted at U549, U557, and U558. U516 and U518 do not have to be changed.

Setup and Testing

POWER LINE CONSIDERATIONS

If you need to change the position of the 115/230 switch (located on the bottom of the Computer), be sure you change rear panel fuse F1 to the proper value as follows:

> For 115 VAC, use a 1.5-ampere, 125-volt, slow-blow fuse.
> For 230 VAC, use a 1-ampere, 250-volt, slow-blow fuse.

The plug on the power cord is for standard 115 VAC outlets. For 230 VAC operation in the U.S.A., cut off and replace in a manner such that your power connection conforms with section 210-21 (b) of the National Electric Code, which reads, in part:

> "Receptacles connected to circuits having different voltages, frequencies, or types of current (AC or DC) on the same premises shall be of such design that attachment plugs used on such circuits are not interchangeable."

When you install the new plug, make sure it is connected according to your local electrical code. Units with three-wire line cords must always have the green wire connected to chassis ground.

Be sure the NORM/LOW switch (on the bottom of the Computer) is set in its proper position to match your line voltage as follows:

> NORM range — 110 V to 130 V rms or 220 V to 260 V rms.
> LOW range — 100 V to 120 V rms or 200 V to 240 V rms.

NOTE: If you do not know the value of the line voltage in your area, set the NORM/LOW switch to NORM.

CABINET REMOVAL

Whenever you need to remove the cabinet top:

- Refer to the inset drawing on Figure 2-1, insert the blade of a small screwdriver into the notch in the latch plate, and then, as you lift upward on the front, slide the latch plate toward the front of the Computer about 1/4".
- Likewise, open the latch plate on the other side of the cabinet top.
- **WARNING:** When the line cord is connected to an AC outlet, hazardous voltages can be present inside your Computer. See Figure 2-1.
- Carefully tilt the cabinet top back.
- Unplug the fan.
- When the top is tilted straight up, carefully lift the hinges out of the rear panel.

Simply reverse this procedure to close and lock the cabinet top back on the Computer.

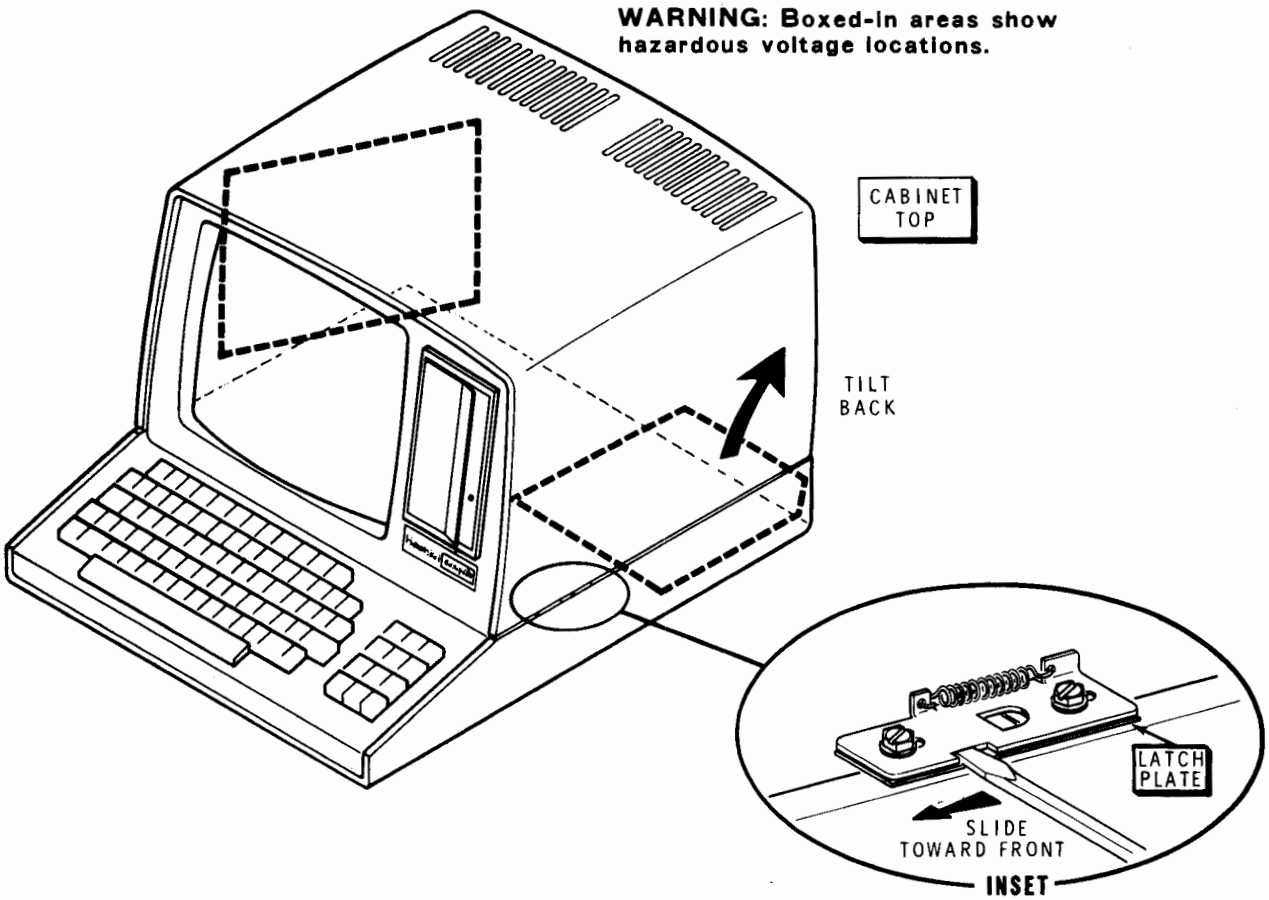


Figure 2-1

ZDS System Configuration

This section of the Manual shows you the normal switch and jumper positions. Check them to be sure they are in their proper positions, or set them (as explained) for the operation that is desired.

The Computer communicates with the peripherals at RS-232C signal levels. 25-pin "D" connectors on the rear panel conform to RS-232C standards and mate with most equipment that conforms to this standard.

Refer to the following sections that pertain to your Computer.

TERMINAL LOGIC CIRCUIT BOARD

Carefully tilt back the cabinet top. See Figure 2-1.

Be sure the POWER switch is off. Then remove the screws that hold the terminal logic circuit board (the rear circuit board). Remove the two screws that hold the top of the CPU logic circuit board. Disconnect the cables, as necessary, and lift the circuit boards up out of the Computer.

SWITCH S402 (Secondary power-up configuration)

Push all of the switches on S402 up (0) as shown in Figure 3-1 on Page 3-2.

If you ever want to change these switch positions, they are defined as follows:

SWITCH SECTION	DESCRIPTION
0	0 = underscore cursor; 1 = block cursor
1	0 = key click; 1 = no key click
2	0 = discard past end of line; 1 = wrap around
3	0 = no auto LF on CR; 1 = auto LF on CR
4	0 = no auto CR on LF; 1 = auto CR on LF
5	0 = ZDS mode; 1 = ANSI mode
6	0 = keypad normal; 1 = keypad shifted
7	0 = 60 Hz refresh; 1 = 50 Hz refresh

SWITCH S401 (Primary power-up configuration)

Refer to Figure 3-1 for the following steps.

This switch (located on the terminal logic circuit board) sets the following power-up and reset modes:

SWITCH SECTION	DESCRIPTION
0-3	Baud Rate
4	Parity Enable
5	Odd/Even Parity
6	Normal/Stick Parity
7	Half/Full Duplex

The particular configuration that you select is initialized when you power-up the Computer or when you perform a Computer Reset. Figure 3-1 shows the location of switch S401. Remember that, as you look at switch S401 from the front of the Computer, you select the one (1) positions of the switch by pushing the switches down, and you select the zero (0) positions by pushing the switches up.

Set switch S401 for:

MODE	SWITCH SECTION 0	1	2	3	4	5	6	7
9600 Baud	0	0	1	1				
No Parity					0			
Odd Parity						0		
Normal Parity							0	
Full Duplex								1

When no parity is selected, you can set the even and normal parity switch sections to either position since they will be ignored.

Each function of switch S401 is explained in the following text.

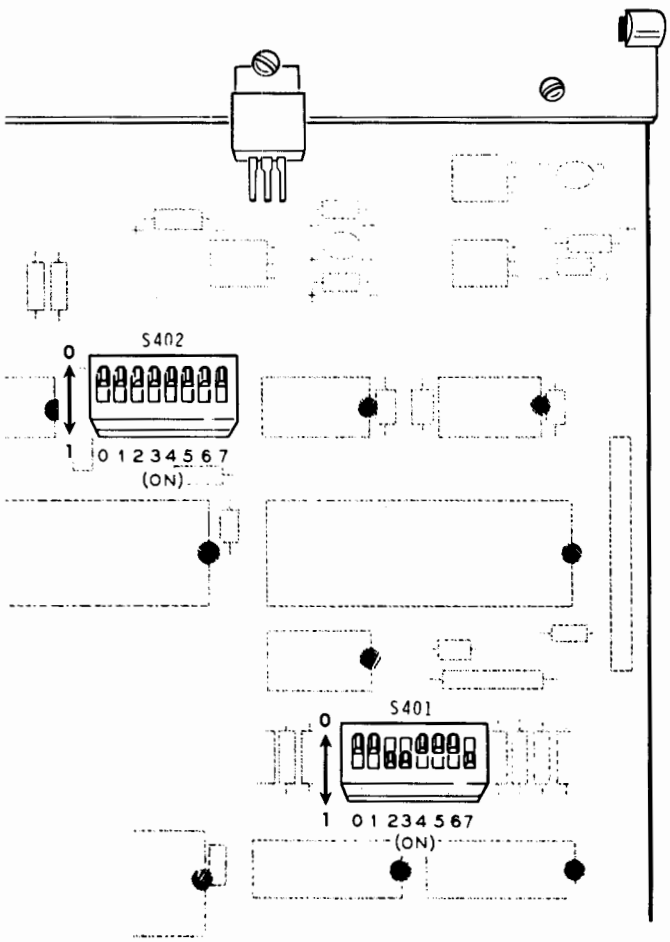


Figure 3-1

Baud Rate

When used as a Computer, the baud rate must be set to 9600. If you use your Computer as a terminal, you can reset the baud rate as explained below.

You can select any of 12 different baud rates (110-9600). To do this, place sections 0, 1, 2, and 3 of switch S401 to the proper positions as shown below. The baud rate will be initialized (or updated) upon Reset or during power-up.

BAUD RATE	SWITCH SECTION 0	1	2	3
N/A	0	0	0	0
110	1	0	0	0
150	0	1	0	0
300	1	1	0	0
600	0	0	1	0
1200	1	0	1	0
1800	0	1	1	0
2000	1	1	1	0
2400	0	0	0	1
3600	1	0	0	1
4800	0	1	0	1
7200	1	1	0	1
9600	0	0	1	1
19200*	1	0	1	1

Parity

You can program the ACE (Asynchronous Communication Element) to either generate or eliminate the parity bit. Section 4 of switch S401 selects the parity bit.

Down (1) = Parity
Up (0) = No Parity

ZDS Software does not check parity.

Odd/Even Parity

If section 4 = 1, then section 5 of switch S401 selects odd or even parity.

Down (1) = Even Parity
Up (0) = Odd Parity

Normal/Stick Parity

If section 4 = 1, then section 6 of switch S401 sets the ACE to transmit and receive either stick or normal parity.

Down (1) = Stick Parity
Up (0) = Normal

Half/Full Duplex

Section 7 of switch S401 selects either full or half duplex communications between the Computer and the terminal sections.

Down (1) = Full Duplex
Up (0) = Half Duplex

ZDS Software supports full duplex operation. Set section 7 to 1 for full duplex operation.

Replace the circuit boards and reconnect their cables.

* Not currently supported (may drop characters)

CPU LOGIC CIRCUIT BOARD

Switch SW501

The functions that switch SW501 selects are determined by integrated circuit U518. See Figure 3-2.

5-1/4" HARD-SECTORED FLOPPY USAGE

When you use a 5-1/4" hard-sectored floppy disk, integrated circuits part numbers HE 444-40, HE 444-62, or HE 444-84 must be installed at U518. Set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers." See Figure 3-2.

Set SW501 section 5 to "1."

Set the remaining seven SW501 sections to "0."

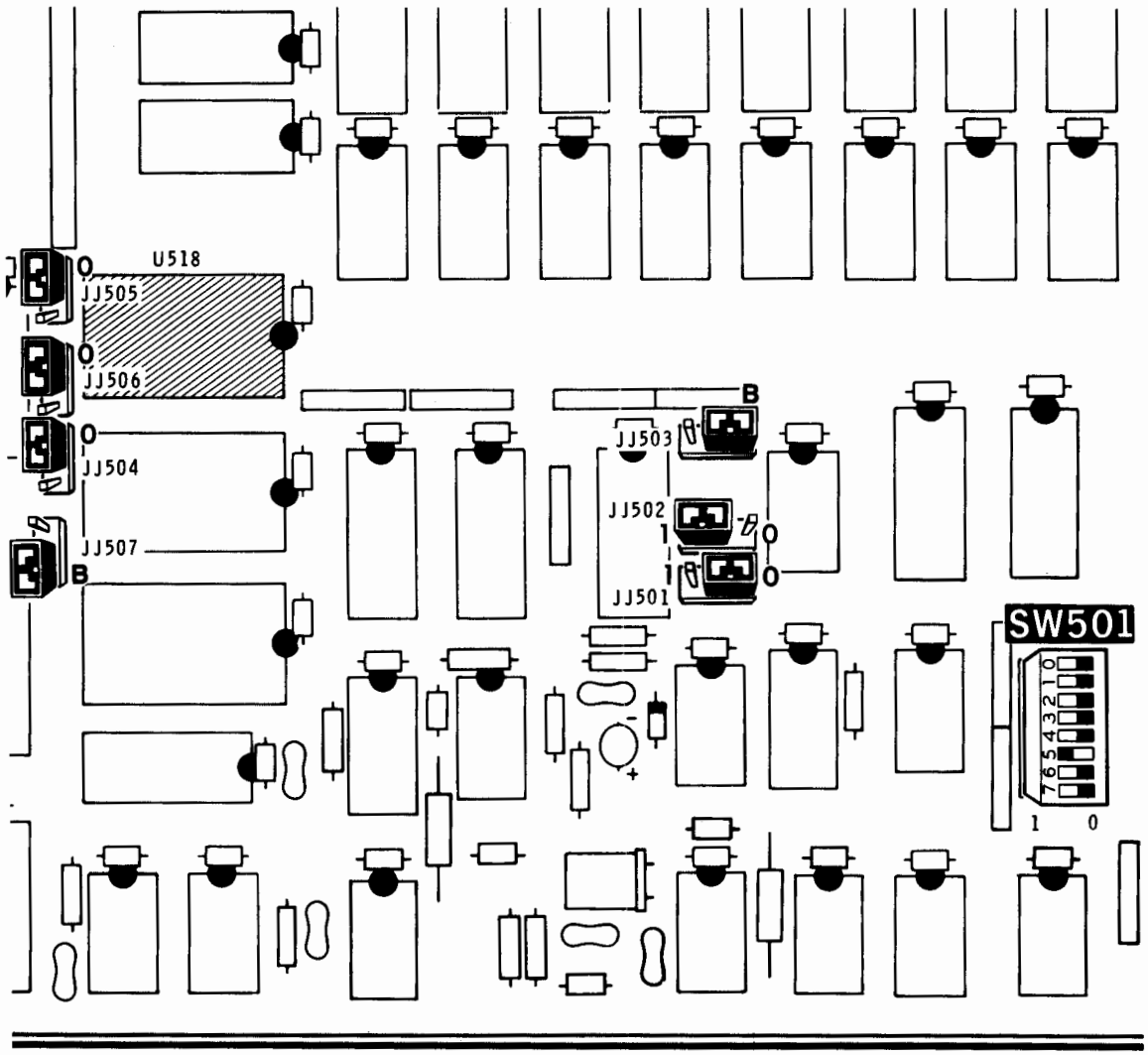


Figure 3-2
CPU board.

8″ FLOPPY DISK (Z-47) USAGE

When you use an 8″ floppy disk (Z-47), integrated circuit part numbers HE 444-62 or HE 444-84 must be installed at U518.

- When you boot up from a 5-1/4″ hard-sectored floppy disk to enable your 8″ floppy disk, set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers." See Figure 3-2.

Set SW501 switch sections 2 and 5 to "1."

Set the remaining six SW501 sections to "0."

- When you boot up from the left-hand 8″ floppy disk drive, set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers."

Set SW501 switch sections 2, 4, and 5 to "1."

Set the remaining five SW501 switch sections to "0."

8″ FLOPPY DISK (Z-67) USAGE

There are four ways of installing the Interface Board. How you install yours depends on what equipment you already have. If you have:

1. A **Z-89-37 Double-Density Controller**, you must install your Interface Board as shown in Figure 3-3 on Page 3-6. Switch SW501 on the CPU Board must be set as shown in inset drawing #1. The jumpers on the Interface Board must be set as shown in inset drawing #2.

2. An **H-88-1 Disk Controller**, you must install your Z-89-67 Interface Board as shown in Figure 3-4 on Page 3-7. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

3. A **Z-89-47 Interface Board**, you must install your Z-89-67 Interface Board as shown in Figure 3-5 on Page 3-8. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

4. **None of the Above**, install your Interface Board as shown in Figure 3-6 on Page 3-9. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

You may set the DIP switches on the Interface Board in any position when you are using Zenith software.

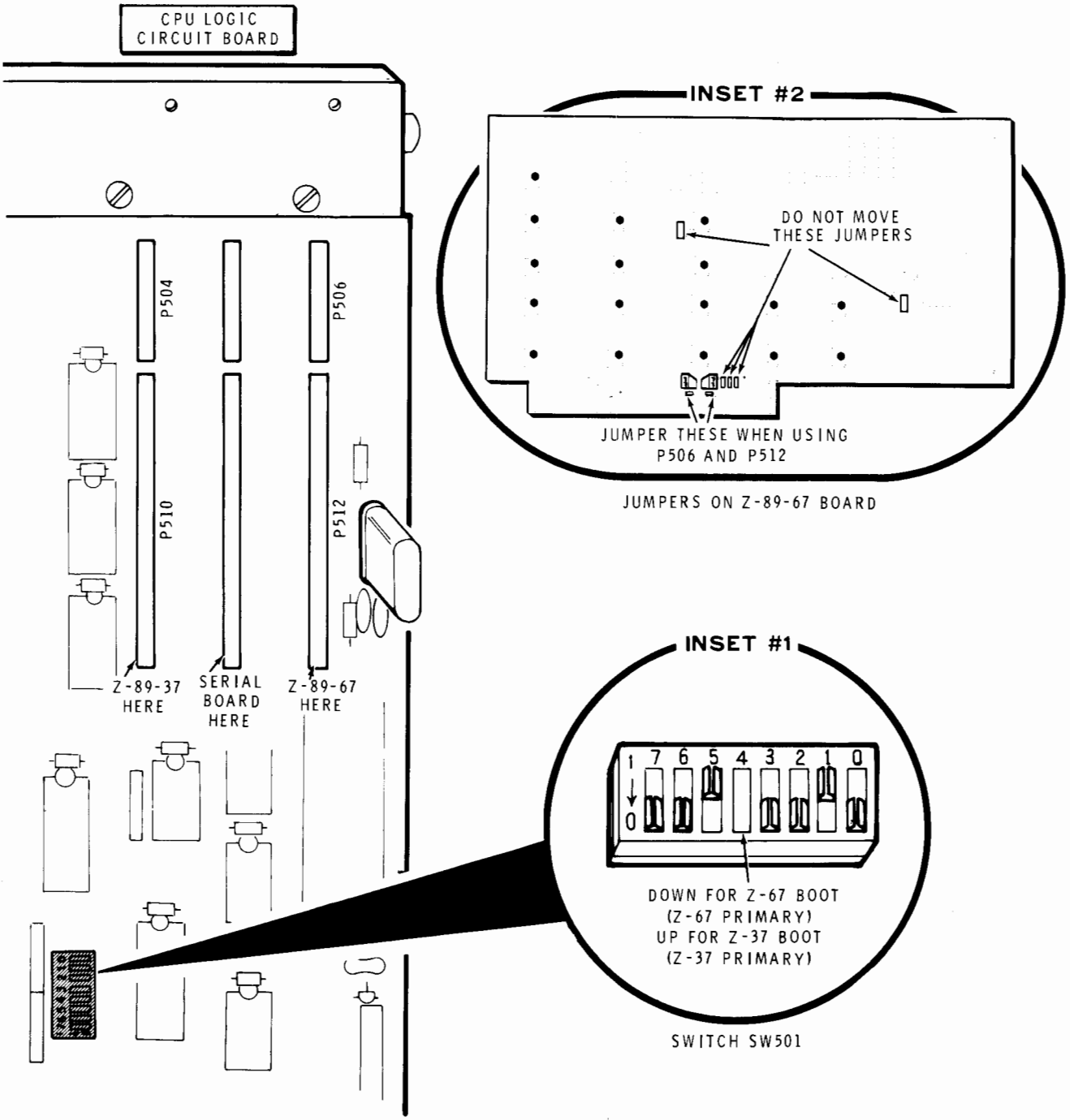

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-37
HERE
SERIAL
BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
DOWN FOR Z-67 BOOT
(Z-67 PRIMARY)
UP FOR Z-37 BOOT
(Z-37 PRIMARY)
SWITCH SW501

Figure 3-3

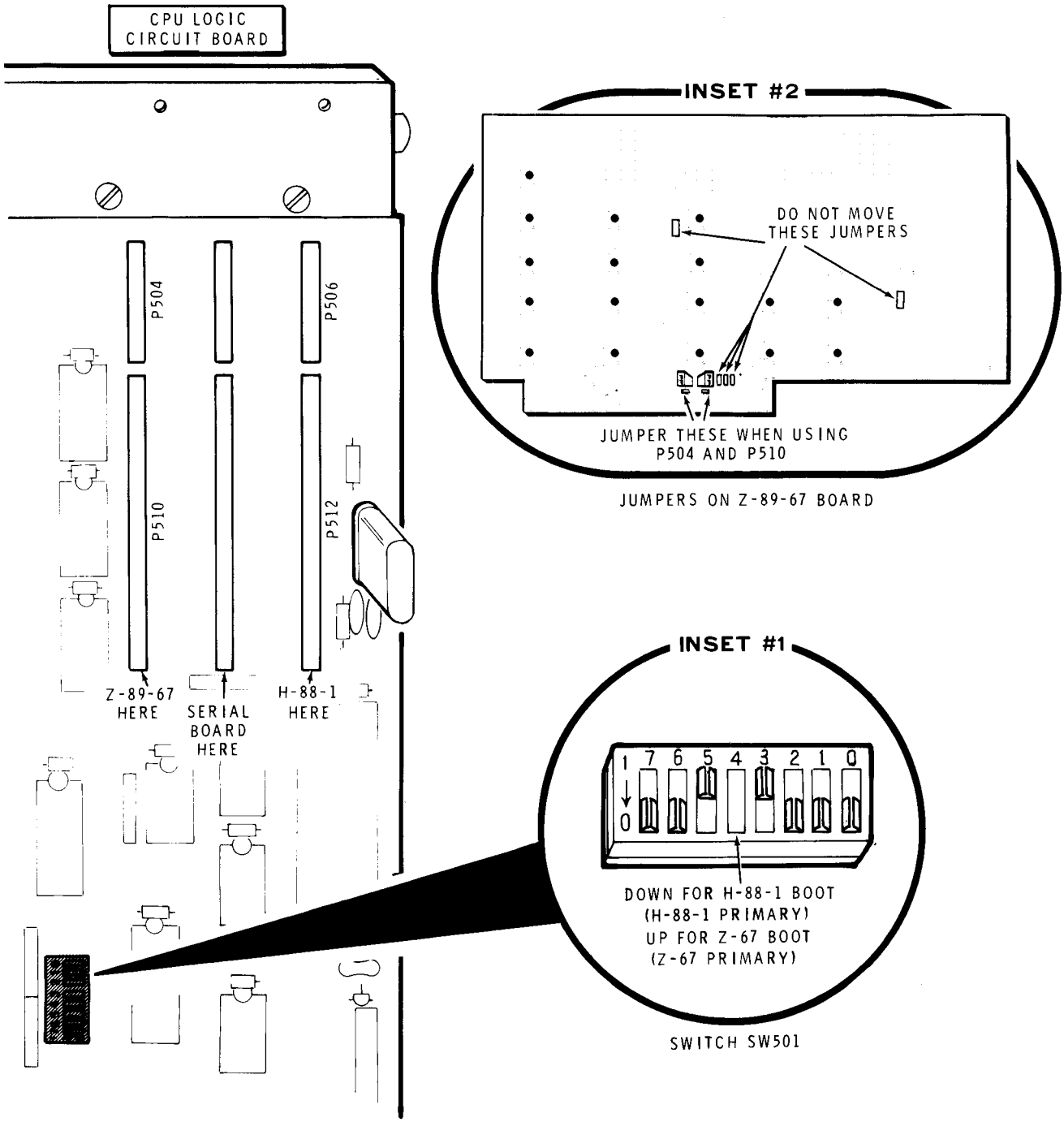

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-67
HERE
SERIAL
BOARD
HERE
H-88-1
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P504 AND P510
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
DOWN FOR H-88-1 BOOT
(H-88-1 PRIMARY)
UP FOR Z-67 BOOT
(Z-67 PRIMARY)
SWITCH SW501

Figure 3-4

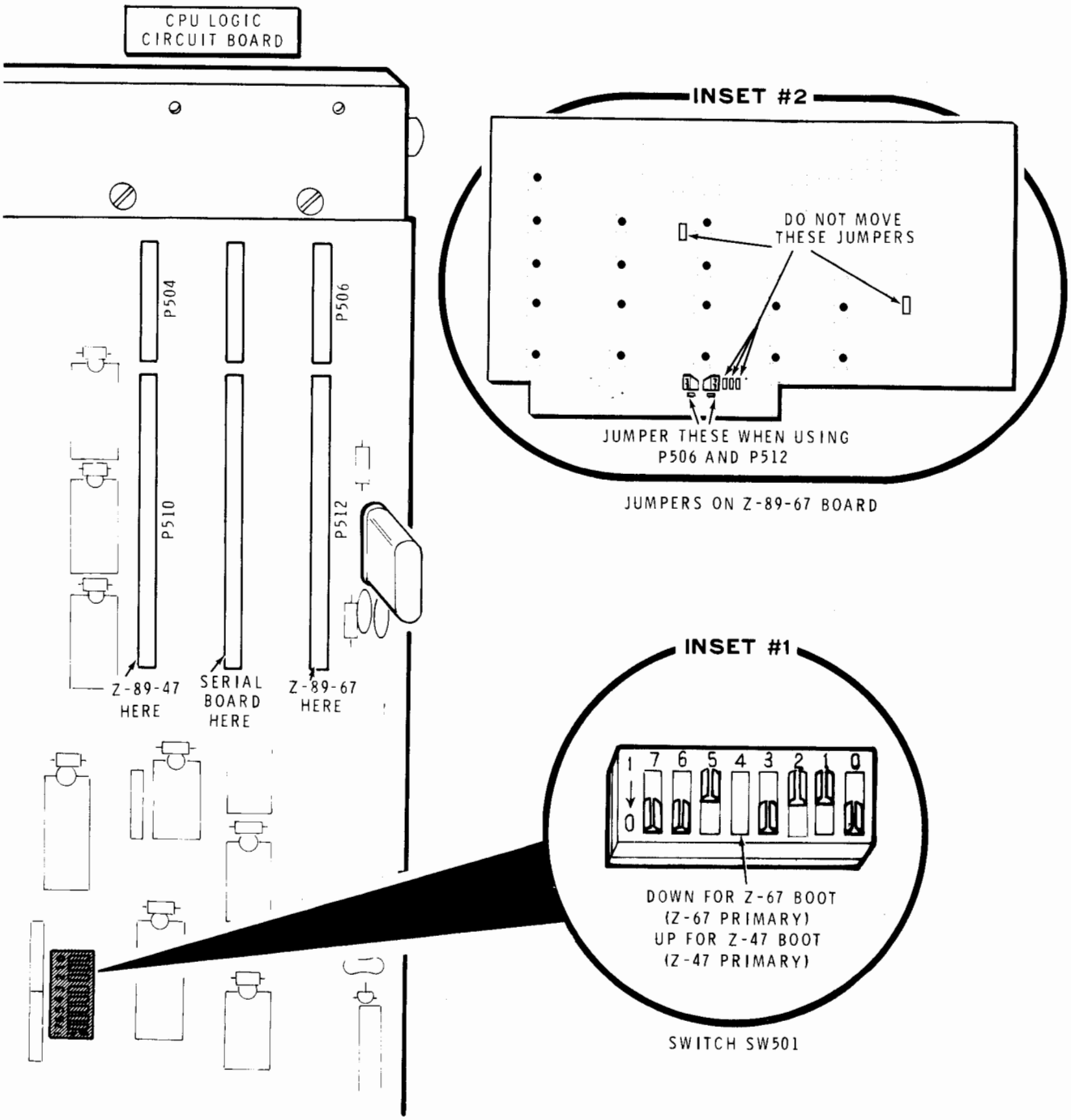

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-47
HERE
SERIAL
BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
DOWN FOR Z-67 BOOT
(Z-67 PRIMARY)
UP FOR Z-47 BOOT
(Z-47 PRIMARY)
SWITCH SW501

Figure 3-5

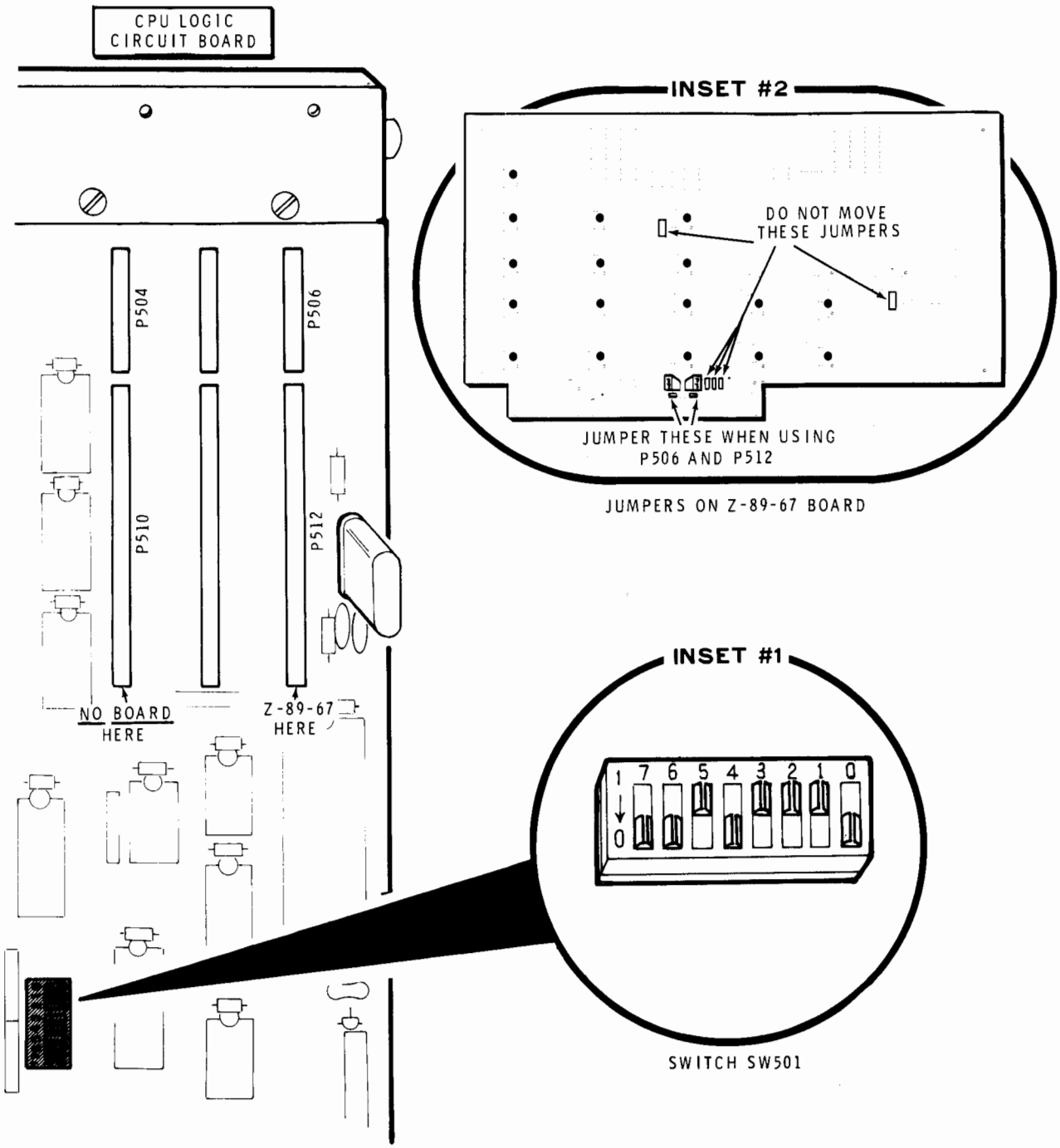

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
NO BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
SWITCH SW501

Figure 3-6

Z-89-37 INTERFACE BOARD USAGE

Z-89-47

For a system to operate properly with the Z-89-37, the Z-89-47 I/O board should be installed at plugs P506 and P512. However, before the Z-89-47 will operate properly when plugged into plugs P506 and P512, a resistor must be added to the Z-89-47 circuit board.

To make the modification use a 4700 Ω, 1/4-watt resistor, HE-6-472 (yellow-violet-red), slide a length of sleeving over the resistor and solder the resistor between pins 1 and 12 of plug P2 on the foil side (not the component side) of the Z-89-47 circuit board. Refer to Figure 3-7.

Set the 170/174 programming plug to 174.

Install the Z-89-47 board at plugs P506 and P512.

NOTE: If you ever move this board to another set of plugs, be sure to remove the 4700 Ω resistor that you just installed.

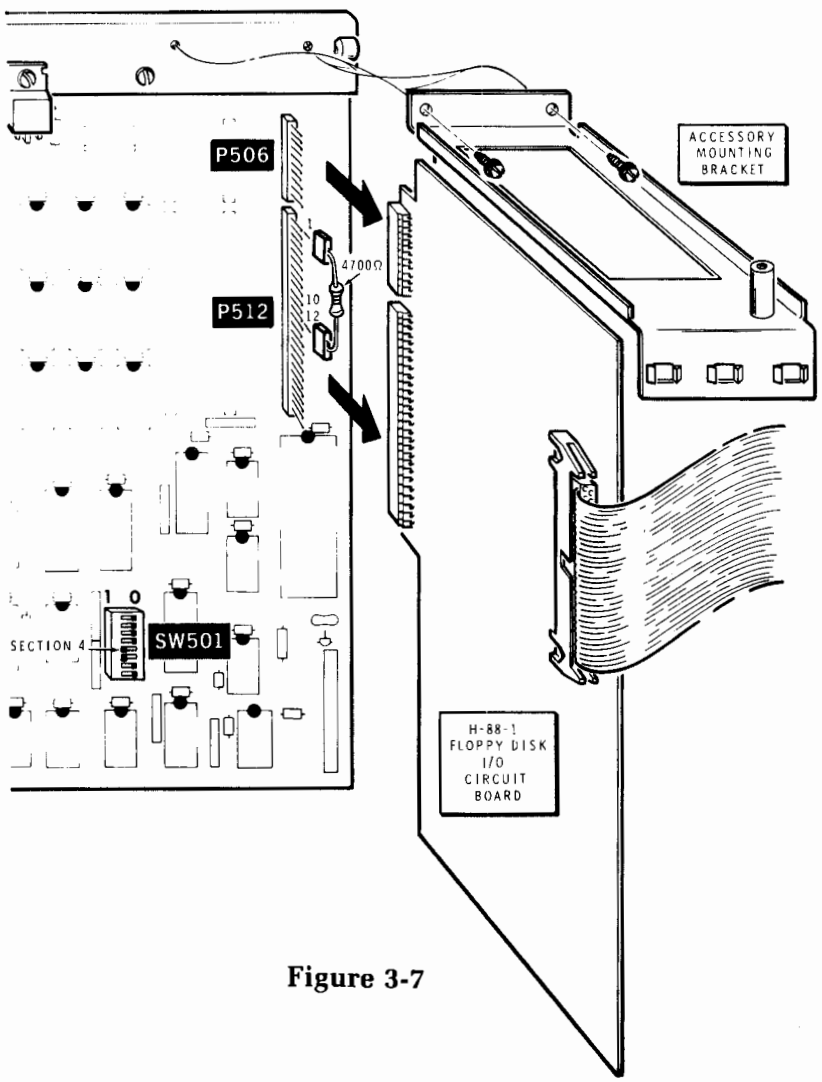


Figure 3-7

PROGRAMMING MODULES

Refer to Figure 3-8 on Page 3-12 as you read the following information.

Use the following information for any special configurations that you may want.

Programming modules:

J1 & J2 — Select port 170 or 174. (Both jumpers must be at 170, or both jumpers must be at 174. 170 is normal.)

J3 — 1 = No precompensation; 0 = precompensation. (1 position is normal.) Use "0" if any of your drives are 48 TPI Wangco Model 82 (HE 150-71) drives. Otherwise, use "1."

We recommend that you do not use both 48 and 96 TPI drives in the same system, since the precompensation will be wrong for at least one of the drives. This can result in reduced data reliability. When precompensation is selected, it is factory pre-set to 300 nanoseconds.

J4 — J7 — Selects which drive is connected to plug P3. (Drive numbers are determined by how the drive programming modules are cut. See Figure 3-8.)

J4 = DS1
J5 = DS2
J6 = DS3
J7 = DS4 (presently not supported)

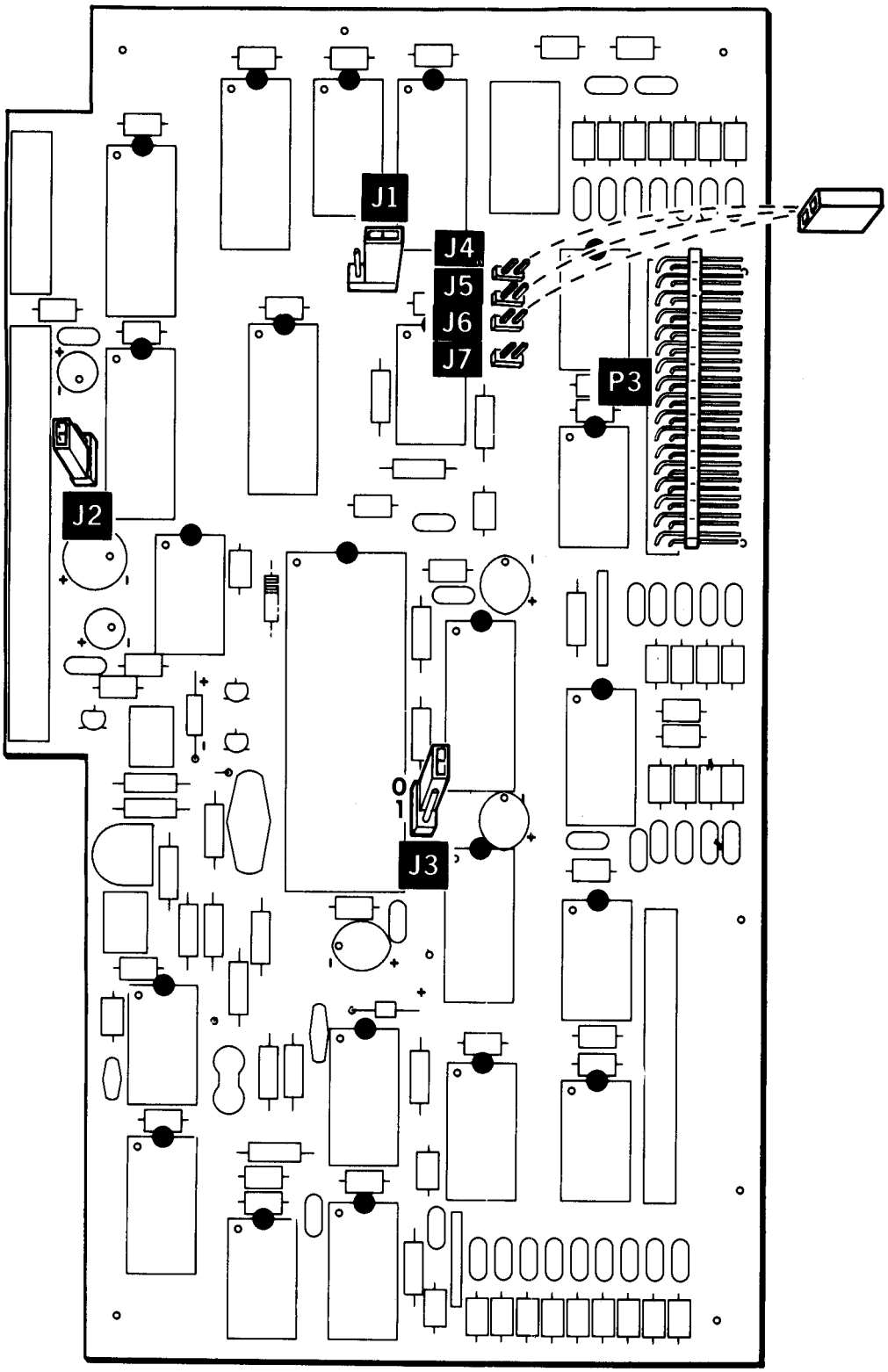


Figure 3-8
Z-89-37 Interface Board

TO REARRANGE THE DRIVE NUMBERS . . . .

Refer to the following chart and Figure 3-9, and select the configuration that fits your situation. Configuration E is normally used for transferring data and programs from hard-sectored disks to soft-sectored disks.

After you select the configuration you want, refer to Figure 3-10 on Page 3-14 to program any 48 TPI (H-17-1) drives, or Figure 3-11 on Page 3-15 to program any 96 TPI drives. [Figure 3-12 on Page 3-16 shows single-sided drives (H-17-1) programmed for connection to an H-88-1 Controller.] You can do this programming by physically interchanging preprogrammed drives, interchanging the programming modules, cutting the programming modules (if presently uncut); or by replacing the programming module with a properly set dip switch.

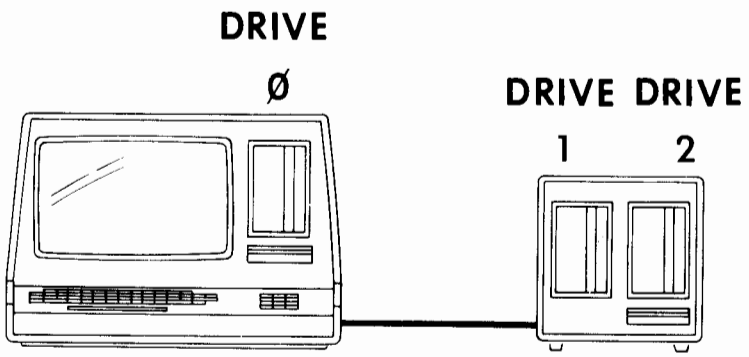


Figure 3-9

FLOPPY DISK CONTROLLER BOARD(S)		TYPES OF DRIVES: • 48 TPI (H-17-1) • 96 TPI (H-17-4)	Drive 0	Drive 1	Drive 2
A	H-88-1	48 TPI (H-17-1) only. Internal drive present	DS3	DS2	DS1
B	H-88-1	48 TPI (H-17-1) Internal drive absent	No drive installed	DS3	DS2
C	Z-89-37	Either* Internal drive present	DS1 (Z-89-37 jumper installed at J4)	DS2	DS3
D	Z-89-37	Either* Internal drive absent	No drive installed (Z-89-37 jumper installed at J7)	DS1	DS2
E	H-88-1 & Z-89-37	Either* Internal drive present	DS3 [Drive 0 is 48 TPI (H-17-1) drive connected to H-88-1. Z-89-37 jumper installed at J6.]	DS1 (Drive 0 connected to Z-89-37)	DS2 (Drive connected Z-89-37)

* All drives connected to the Z-89-37 should be of the same type, either 48 TPI (H-17-1) or 96 TPI (H-17-4).

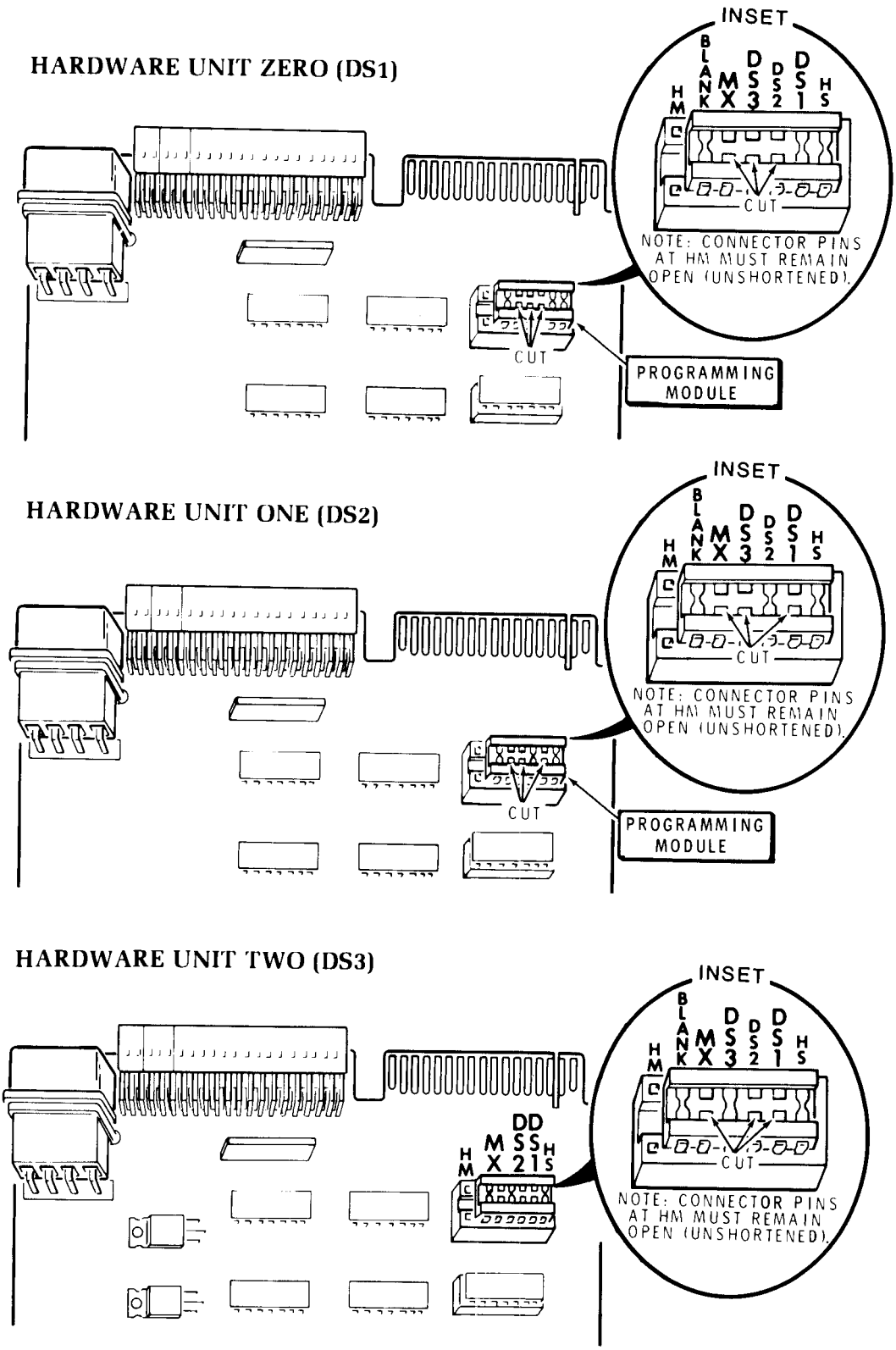
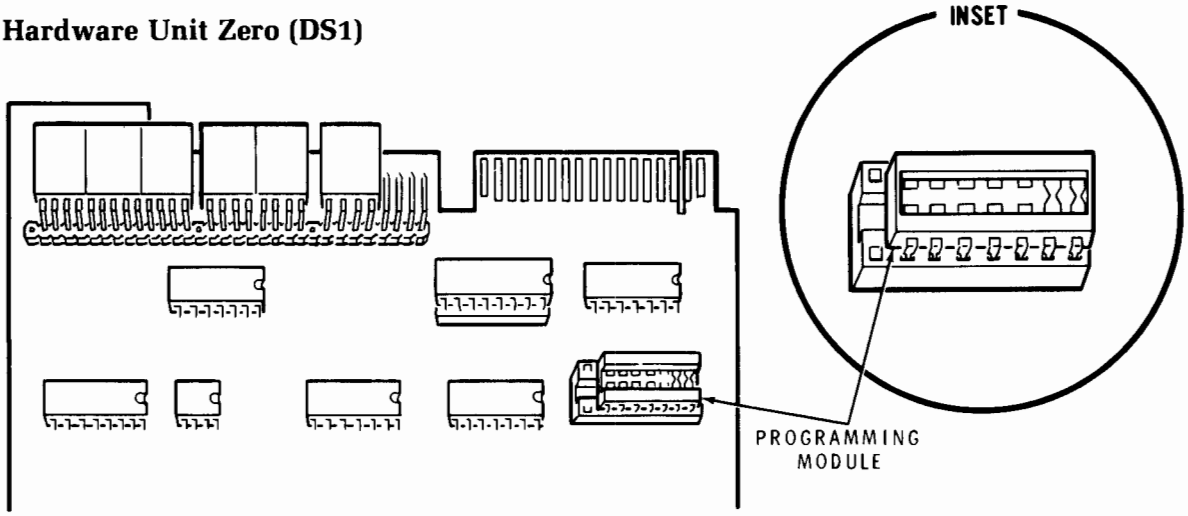


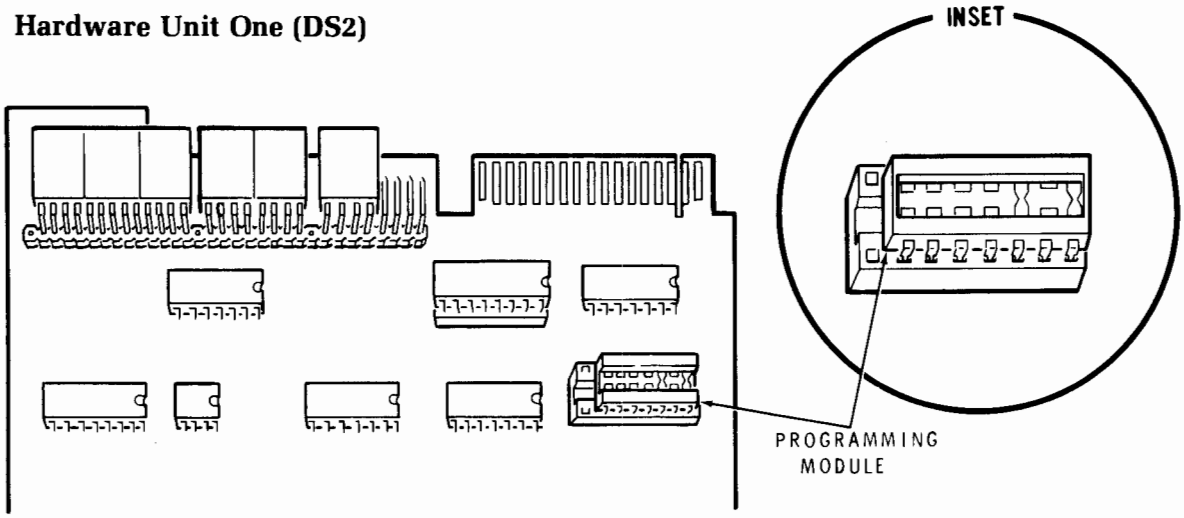
Figure 3-10

Single-sided drives (H-17-1) programmed for Z-89-37 Controller.

Hardware Unit Zero (DS1)



Hardware Unit One (DS2)



Hardware Unit Two (DS3)

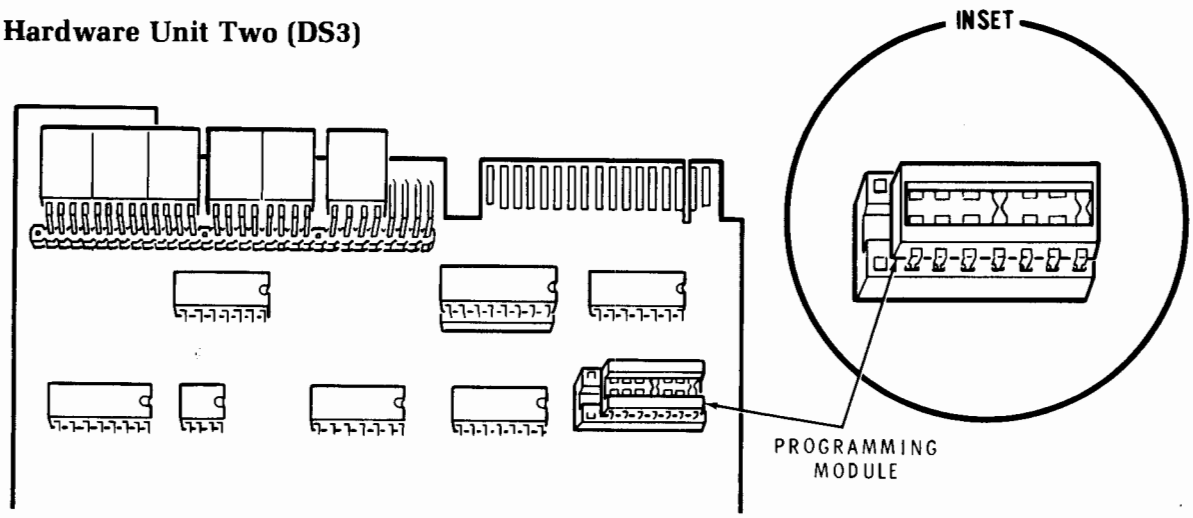
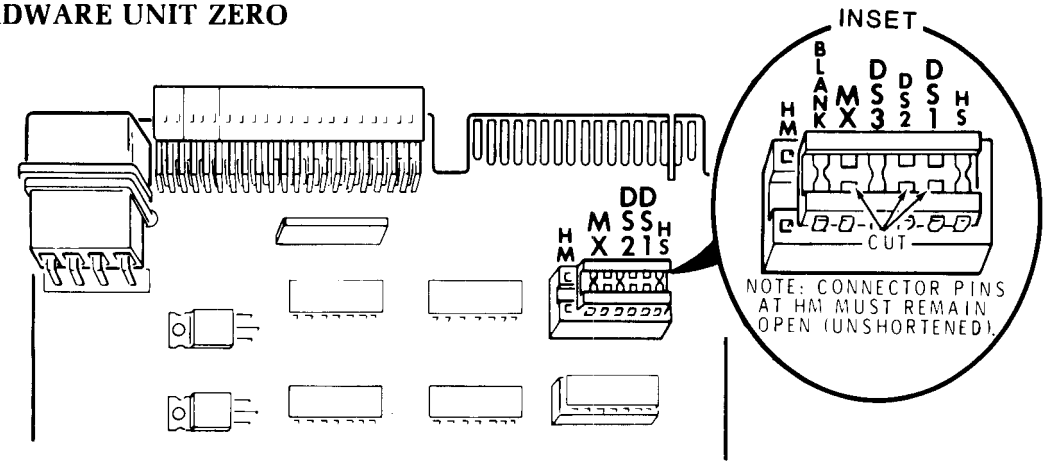


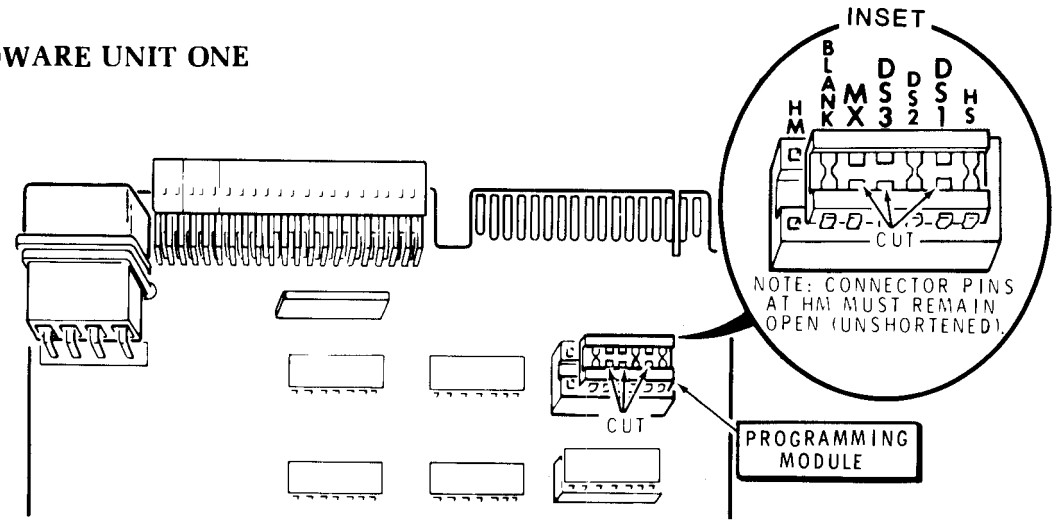
Figure 3-11

Double-sided drives (H-17-4) programmed for Z-89-37 Controller.

HARDWARE UNIT ZERO



HARDWARE UNIT ONE



HARDWARE UNIT TWO

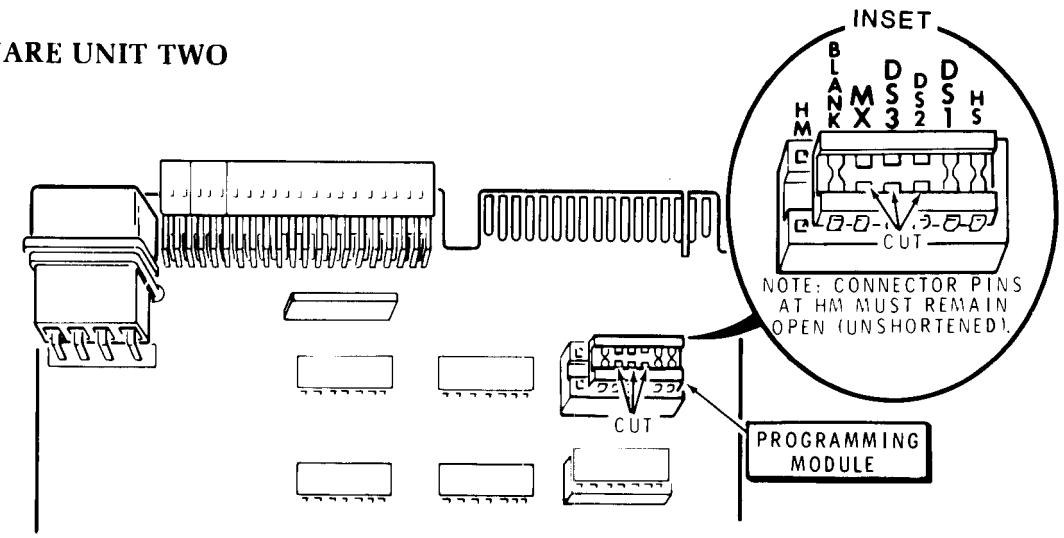


Figure 3-12
Single-sided drives (H-17-1) programmed for H-88-1 Controller.

Definitions of SW501 with MTR-89 (HE 444-62)

When IC part number HE 444-62 is installed at U518, the following table describes the functions of each SW501 switch section.

SWITCH SECTIONS	SETTING*	DESCRIPTION
1 and 0	00	Port 174/177Q (7CH-7FH) has a 5-1/4" hard-sectored floppy disk (normal).
	01	Port 174/177Q has a Z-47, 8" floppy disk.
	10	Undefined.
	11	Undefined.
3 and 2	00	Port 170/173Q (78H-7BH) is not in use (normal with Z-47, 8" floppy disk).
	01	Port 170/173Q has a 8" floppy disk (normal with Z-47).
	10	Undefined.
	11	Undefined.
4	0	Boots from device at port 174/177Q (7CH-7FH) (5-1/4" hard-sectored floppy disk).
	1	Boots from device at port 170/173Q (78H-7BH) (Z-47, 8" floppy disk).
5	0	Performs memory test upon power-up or SHIFT-RESET.
	1	Does not perform memory test (normal).
6	0	Sets console to 9600 baud (normal).
	1	Sets console to 19200 baud (not currently supported).
7	0	Normal boot (normal).
	1	Auto boot on power-up or SHIFT-RESET (not recommended).

* Right-hand value is for switch section 0 or 2, depending on respective Switch Section column.

Definition of SW501 with MTR-90 (HE 444-84)

When IC part number HE 444-84 is installed at U518, set the sections of SW501 as described in "Definition of SW501 with MTR-89," except for sections 0, 1, 2, and 3, which are defined as follows:

SWITCH SECTIONS	SETTING*	DESCRIPTION
1 and 0	00	Port 174/177Q (7CH-7FH) is 5-1/4" hard-sectored floppy disk.
	01	Port 174/177Q is Z-47, 8" floppy disk.
	10	Port 174/177Q is Z-67, 8" hard disk.
	11	Undefined.
3 and 2	00	Port 170/173Q (78H-7BH) is Z-37 soft-sectored disk.
	01	Port 170/173Q is Z-47, 8" floppy disk.
	10	Port 170/173Q is Z-67, 8" hard disk.
	11	Undefined.

* Right-hand value is for switch section 0 or 2, depending on respective Switch Section column.

Memory Decode ROM

The memory decode ROM is located at U517 on the CPU board. Two ROMs have been used. Part number HE 444-42 was originally used. This ROM precluded the use of more than 48K of memory or CP/M. It has been superseded in all production units by HE 444-66, which allows the ROM based 48K mode, the ROM based 56K mode, and an all RAM 64K mode. **All** users should upgrade to this part regardless of configuration. There are **no** negative consequences connected with this upgrade.

Associated with this ROM are three or four jumpers, JJ501 thru JJ504. Older CPU boards have all four jumpers; they should be set as follows:

When using the Old ROM (HE 444-42)

	JJ501	JJ502	JJ503	JJ504
16K	0	0	0	0 (or B)
32K	1	0	0	0 (or B)
48K	0	1	0	0 (or B)

When using the New ROM (HE 444-66)

	JJ501	JJ502	JJ503	JJ504
16K	0	0	**	0 (or B)
32K	1	0	**	0 (or B)
48K	0	1	**	0 (or B)
64K*	1	1	**	0 (or B)

Newer CPU boards (which only have three jumpers, JJ501 through JJ503) are supplied with the new decode ROM (HE 444-66) already installed and the jumper wire incorporated directly into the PC board foil. These boards should not be used with the old ROM (HE 444-42). These jumpers should be set as follows:

	JJ501	JJ502	JJ503
16K	0	0	0 (or B)
32K	1	0	0 (or B)
48K	0	1	0 (or B)
64K*	1	1	0 (or B)

These are four jumper wires associated with the code ROM and the secondary address decoder. These are either JJ505, JJ506, JJ507 and JJ508 (on older units) or JJ504, JJ505, JJ506 and JJ507 (on newer units). These should be set as follows:

Older Units: Newer Units:	JJ505 JJ504	JJ506 JJ505	JJ507 JJ506	JJ508 JJ507
MTR-88, MTR-89	0	0	0	1 (or B)
MTR-90	1	*	1	1 (or B)

* Requires the WH-88-16 accessory PC board.

** A jumper is required between the center pin of JJ503 and pin 17 of P509, or P4 of WH-88-16 (which connects to pin 17 of P509). This jumper may have been soldered on the back of the CPU board during manufacture (for Z-89-FA and some other models), or it may be ordered as part number HE 134-1120 and installed by the user. Neither tools nor soldering are required.

HARD-SECTORED 5-1/4" SINGLE-DENSITY FLOPPY DISK

The single-density floppy disk interface circuit board is installed at P506 and P512 on the CPU circuit board.

SERIAL INTERFACE

Refer to Figure 3-13 on Page 3-21 and set all three programming jumpers to OFF if this has not already been done.

NOTE: These jumpers determine the interrupt priority of the ports. When a jumper is in the "OFF" position, no interrupt exists for that port. When you install the jumper at 3, 4, or 5, an RST 3, an RST 4, or an RST 5 (respectively) instruction is executed when the interrupt for that port occurs.

The first port on the circuit board is located at address 340/347Q (0E0H-0E7H) and is normally used as the line printer port. However, it is not restricted only to that use, as it is a standard RS-232C interface with a "DCE" connector.

The second port on the circuit board is located at address 320/327Q (0D0H-0D7H) and is a general purpose port. It is a standard RS-232C interface with a "DCE" connector.

The third port on the circuit board is located at address 330/337Q (0D8H-0DFH) and is a general purpose port. It is a standard RS-232C interface with a "DTE" connector, suitable for use with a MODEM.

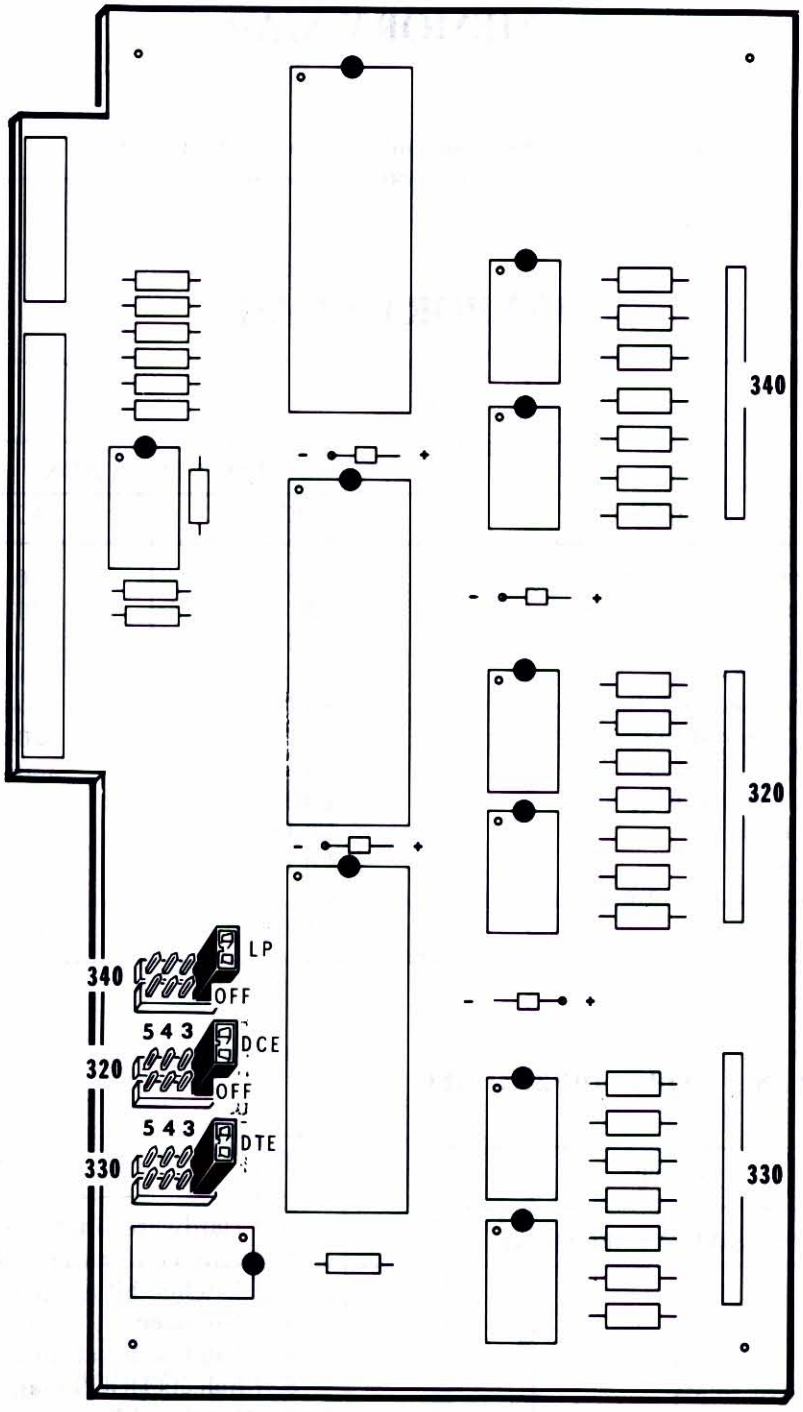
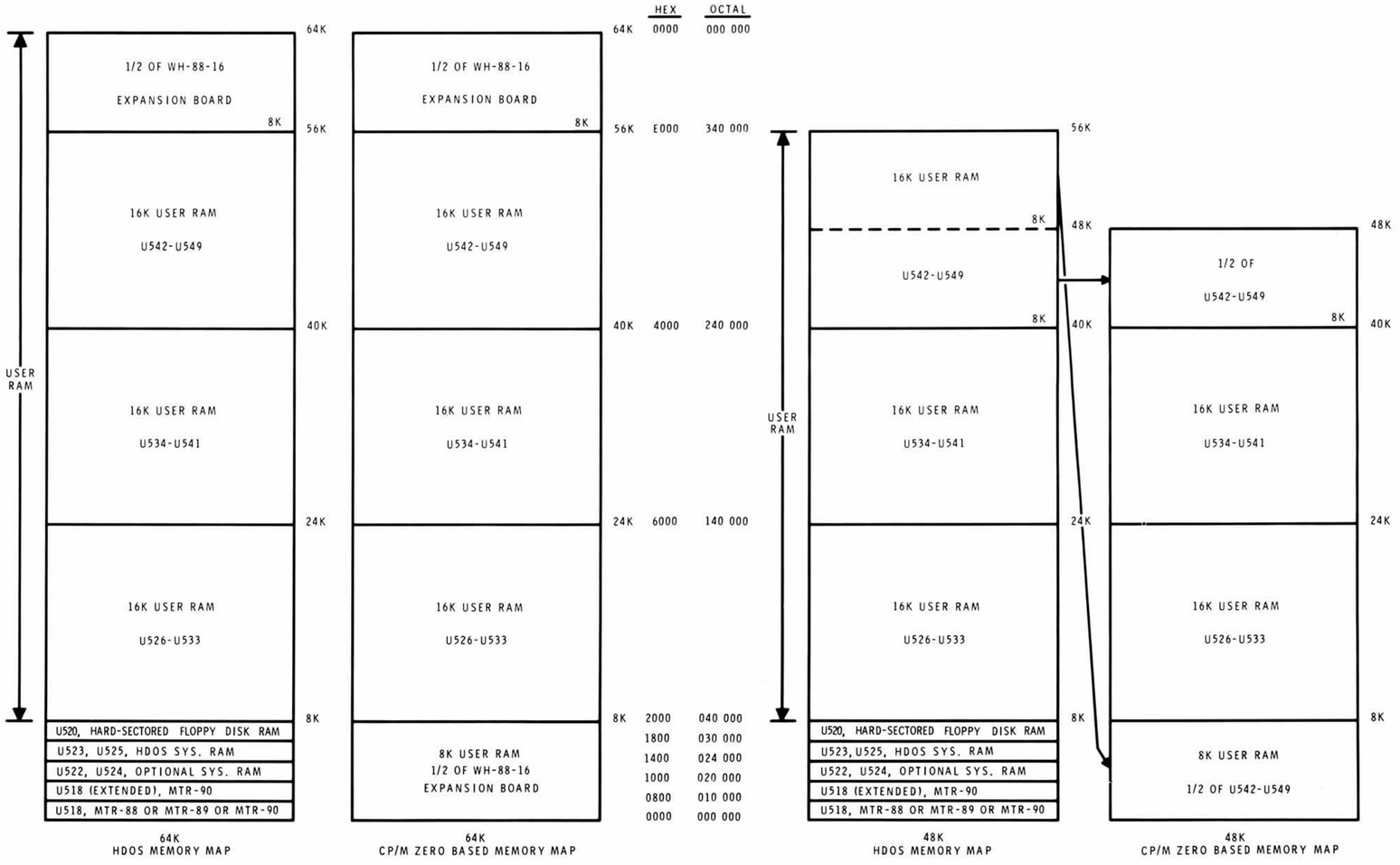


Figure 3-13

Serial interface board.



MEMORY MAP

MEMORY MAP

The Memory Map (fold-out from this page) illustrates the use of the specified memory locations.

I/O PORT USAGE

USE	PORT LOCATION	
	HEX	OCTAL
Not specified, available	0-77	0-167
Cassette I/O (if used)	78-79	170-171
Disk I/O #1	78-7B	170-173
Disk I/O #2	7C-7F	174-177
Not specified, reserved	80-C7	200-317
DCE Serial I/O	D0-D7	320-327
DTE Serial I/O	D8-DF	330-337
DCE Serial I/O	E0-E7	340-347
Console I/O	E8-EF	350-357
NMI*	F0-F1	360-361
General purpose port	F2	362
NMI*	FA-FB	372-373

GENERAL PURPOSE PORT (0F2H) BIT DEFINITIONS

BIT	INPUT
	(SW501 SWITCH SECTION)
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7

BIT	OUTPUT
0	Hardware single step enable
1	2 mSec clock enable
2	Latched bit at memory expansion connector
3	Not used
4	Latched bit at memory expansion connector
5	Selects HDOS map or CP/M map
6	Latched bit at I/O expansion connector
7	Latched bit at I/O expansion connector

* Ports labeled "NMI" are not used. Rather, an NMI is generated if the port is accessed for either input or output. This is done for compatibility with earlier computer products, specifically the Heathkit Model H-8.

Operation

COMMAND SUMMARY

Care of Your Floppy Diskette — Do not turn the Computer on or off when a floppy disk is installed in the disk drive with its door closed. Errant power signals can cause the disk head to bounce. If the drive door is closed, the drive head is engaged on the diskette and can possibly damage the diskette.

If your Computer uses the MTR-89 or the MTR-90 monitor, you will find a couple of differences in the commands.

T(est Memory)

The MTR-90 uses a shorter command for T(est Memory). By typing T, the RAM memory test is initiated. The test references memory locations in the current radix. Error messages report the address of any bad memory locations.

You may also use the same command for Test Memory as used for the MTR-89, which is (H: Go 7375 ㊐).

R(adix)

The R(adix) command sets the current working radix for all other commands.

Valid arguments to radix are O(ctal) and H(exadecimal). The default current radix on power up is octal. Typing R and RETURN with no argument displays the current radix.

EXAMPLE: Set the current radix to hexadecimal and then check it.

```
   H: R(adix) H(exadecimal)
   H: R(adix)    ㊐
Hexadecimal
   H:
```

This summary is a list of the commands that the Computer will respond to and the responses that it will make. **You may enter commands in either upper or lower case characters**. In all cases, pushing the DELETE key prior to pushing the RETURN key (which terminates the command) will cancel the current command and cause the Computer to respond with the prompt (H:). **All byte entries are in octal, and all address entries are in split octal**. NOTE: Split octal is two 3-bit bytes as shown in Figure 4-1.

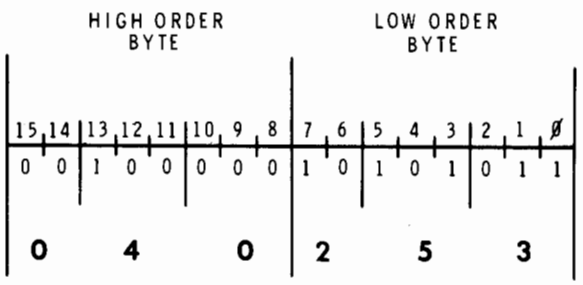


Figure 4-1

1. Turn on the Computer power. Then wait a few seconds until the CRT becomes illuminated.

2. Boot:

   After you see the prompt (H:), enter "B." The Computer will complete the "Boot" message and then wait for a Carriage Return.

   Insert a diskette in the floppy disk drive and close the door.

   Now press the RETURN key and the system should begin booting up. If the system seems to stop after a second or two of disk activity, depress the space bar two or three times. (You may be directed to do this by a message on the screen, depending on the firmware installed.)

3. Go to the user routine: (G) or (G ADDR)

   A. After the prompt, enter "G." The Computer will complete the "Go" message.

   B. Enter either a Carriage Return or a new address and a Carriage Return.

   C. If you did not enter a new address above (in Step B), control will be given to the routine at the address specified by the user program counter. However, if you entered a new address and a Carriage Return, control will be given to the address you specified.

4. Set the user Program Counter values: (P) or (P ADDR)

   After the prompt, enter "P." The Computer will complete the "Program Counter" message. Now you may enter a new program counter value (in split octal) and terminate it with a Carriage Return. If no new value is entered and you enter a Carriage Return, the current contents of the user Program Counter will be displayed. Again, a new value may be entered and terminated with a Carriage Return, or just entering a Carriage Return will cause a return to the prompt and the current value to be unaltered.

5. Substitute memory: (S) or (S ADDR)

   After the prompt, enter "S." The Computer will complete the "Substitute" message and wait for an address to be specified (in split octal notation) and ended with a Carriage Return. The address specified will then be displayed, followed by its contents. At this point, you can change the contents by entering the octal value to be placed into memory. If you do not want a change, or after you have entered the new value, there are three options.

   A. To view the contents of the next address; enter a SPACE.

   B. To view the contents of the previous address; enter the minus sign (−).

   C. To exit the Substitute mode; enter a Carriage Return.

KEYBOARD OPERATION

Figure 4-2 shows the keyboard of the Computer. The power ON/OFF switch is located on the right rear corner of the back panel. Whenever you turn on the Computer, allow the tube about 30 seconds to warm up. You should then see a flashing line (cursor) or block cursor (if it was selected) in the upper left-hand corner of the screen.

The keyboard allows you to send data to the Computer of the screen. Most of the keys are the same as they are on most typewriters; they type the same alphanumeric characters. A clicking sound tells you that each keystroke has been processed. You cannot damage the Computer by typing on the keys.

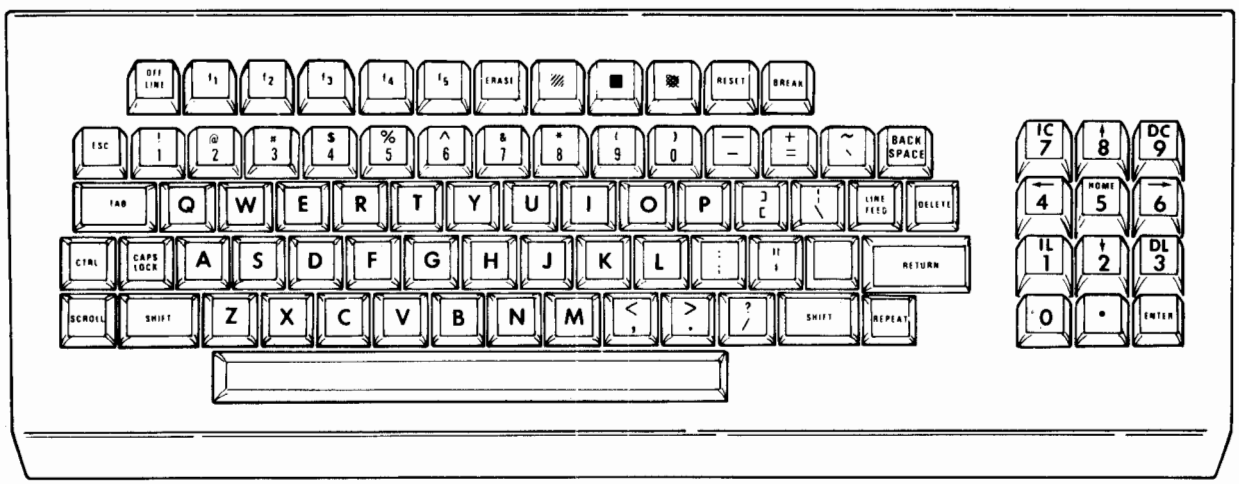


Figure 4-2

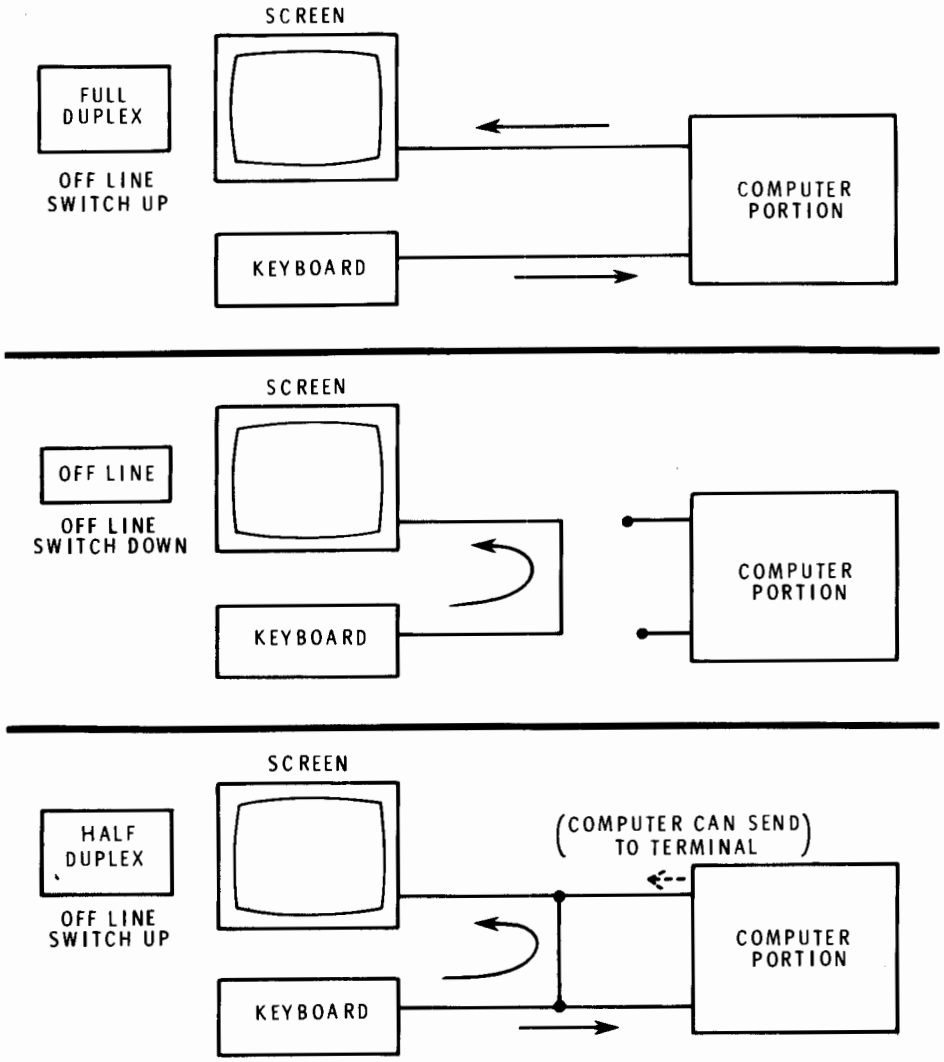


Figure 4-3

The screen contains 2000 normal character positions; 25 lines of 80 characters. Only one character can occupy a character position at any given time and it will remain there until it is erased or replaced.

When the Computer is initially turned on, it clears the screen by placing spaces in all character positions. The cursor is the blinking horizontal line that appears at the home position. It underlines the character position where the next character will be written. (The block cursor will fill the character position.)

As shown in Figure 4-3, you can use the Computer in any one of three different modes; full duplex, off line, or half duplex. (However, half duplex is not a normal ZDS mode.)

When the Computer is on line, the keyboard can transmit any one of the 128_{10} ASCII characters to the computer section. However, some of these characters will not be displayed if the Computer sends them back to the Terminal section.

In the off line mode, the terminal is effectively disconnected from the Computer and the keyboard controls the screen directly. This way, you can position the cursor (↑, ↓, →, ←, and HOME), insert or delete characters or lines (IC, DC, IL, and DL), or erase (ERASE), without sending the codes to the Computer — which could otherwise disrupt a program, etc.

Another way of controlling the screen without sending code to the Computer is to use the CTRL key. Example: you want to erase the screen, but you do **not** want to transmit a code to the Computer. Press and hold the CTRL key and then type SHIFT ERASE. This tells the terminal section to erase the screen, but not to send the code to the Computer section. Again, you can use this procedure with the cursor keys (↑, ↓, →, ←, and HOME), the Insert Line, Delete Line, Insert Character, and Delete Character keys, and ERASE.

Whenever you use the special escape codes to enter and exit the special modes, make sure you enter the lower-case and upper-case letters. For instance, type ESC p (not ESC P) to enter the reverse video mode.

The "ASCII Characters" and "Escape Sequences" show the commands and special escape sequences that the terminal section sends and responds to. Your Computer **must** contain the proper software for it to respond to and generate the codes that use these special features. Different versions of software may support different features.

The Computer has a 128 character input FIFO (first in, first out) buffer for receiving and holding characters until the terminal section can process them. In some cases (such as when the terminal section is operating at 9600 baud in the "insert character" mode), the FIFO can be filled faster than the terminal section can process the characters. In this case, the terminal section will send X OFF (control S) when the FIFO has received 112 characters. After the terminal section has processed enough characters so that only 96 characters remain in FIFO, it will send X ON (control Q) to the Computer section to indicate that it is ready to accept more characters.

When the terminal section sends X OFF, this is only an indication that the buffer is nearly full. Characters will not be lost until after the FIFO has received a full 128 characters. At this point more incoming characters will be lost and the bell will sound.

NORMAL MODES AND KEYS

The following descriptions are for switch S402 set to all zeros.

ALPHABETIC KEYS

The Computer has the standard 26 letters of the alphabet. These keys can transmit either lower-case or upper-case codes as well as display them on the screen. You can either hold the SHIFT key down or you can push the CAPS LOCK key to obtain upper-case letters.

NONALPHABETIC KEYS

The nonalphabetic keys are those with double markings. These include the numbers 0 through 9, punctuation marks, and special characters. The lower marking is generated when both of the SHIFT keys are released, while the upper marking is generated when either (or both) SHIFT key is held down. The CAPS LOCK key will not shift these keys.

MISCELLANEOUS

The characteristics in the following description apply only to the terminal's internal key handling of the listed codes, which can be overridden by the software.

RETURN — Moves the cursor to the first character position of the line that it is currently in. If the cursor is already at the first character position, it remains there. RETURN is a nondisplayable character. Normally, there is no automatic line feed.

LINE FEED — Moves the cursor down one line. LINE FEED is a nondisplayable character. If the cursor is at the bottom line, a LINE FEED causes it to remain there, but all of the data on the screen moves up one line. Data on the top line is lost as it is scrolled up and off the screen. Normally, there is no CR.

SPACE BAR — Causes the cursor to move one character position to the right. A Space is a nondisplayable character. If you type the Space Bar when the cursor is positioned below a displayed character, the character is replaced by a space and the cursor moves one character position to the right. If you type the Space Bar when the cursor is at the right end of a line, the cursor will remain there since neither a carriage return nor a line feed is generated.

BACK SPACE — Moves the cursor one space to the left. If the cursor is at the start (left end) of a line, it will not move when you type a BACK SPACE. ZDS software uses this key to delete the last input character.

DELETE (Rubout) — Transmits the ASCII code 177Q (7FH). It is a nondisplayable character. ZDS software uses this key to cancel the last character that was input.

TAB — When typed on the keyboard, it transmits the ASCII code 011Q (09H). When received by the terminal, it moves the cursor to the next tab stop (eight character spaces) to the right. The tab stops are fixed at 9, 17, 25, 33, 41, 49, 57, 65, and 73 (columns are numbered 1 through 80). If the cursor is at character position 73 through 79, it will only move one character position to the right each time you type the TAB key. If the cursor is at character position 80, it will not move when you type the TAB key (unless the wraparound feature has been selected).

ESC (Escape) — A nondisplayable character that transmits the ASCII code 033Q (1BH). This key is used in combination with other keys to enter and exit special modes.

REPEAT — When you hold this key in, along with another key, it will repeat the function of the other key as long as both keys are held down. **The repeat rate is approximately 8 characters per second**. However, if the baud rate that has been selected is less than the repeat rate, the repeat function will operate at the slower rate.

SHIFT — When you use this key in conjunction with another key, the character printed on the upper portion of that key will be displayed. When you use the SHIFT keys in conjunction with the alphabetic keys, the upper-case character is displayed.

CAPS LOCK — When this latching key is down, the terminal section will transmit the ASCII code for, and display, upper-case (capital) alphabetic letters. It does not shift the keys with the double markings. This is **not** a shift lock.

OFF LINE — When this latching key is down, the terminal section is inhibited from transmitting or receiving data. However, any displayable characters that you type on the keyboard will appear on the screen and any local control codes will be responded to.

BREAK — When you type this key, it generates a **continuous space** at the output of the terminal section. It is generally used to tell the computer that you wish to interrupt execution.

RESET — Allows you to reset the Computer to its preset condition; **it exits all escape modes and resets the baud rate to the rate selected by the switches on the logic circuit board. To use this key, you must press only the right-hand SHIFT key and the RESET key at the same time.** This two-key combination prevents you from inadvertently resetting the Terminal.

SCROLL — When this is used with ZDS software, when in the Hold Screen Mode, you can type the SCROLL key to instruct the Terminal to display another line of information onto the screen. You can simultaneously press the SHIFT and SCROLL keys to display another 24 lines of information onto the screen.

SCROLL (line)	SCROLL
SCROLL (page)	SHIFT/SCROLL

CONTROL KEY

The CTRL key is held down while you push one of the other keys to send the 32 ASCII control codes to the Computer. These are nondisplayable characters. The Terminal responds to only seven of the control characters from the keyboard or from the serial input port. These seven characters are:

Bell (BEL or CTRL G) — Causes the Terminal to sound an audible tone through an internal speaker.

Back Space (BS or CTRL H) — Duplicates the BACK SPACE key.

Horizontal Tab (HT or CTRL I) — Duplicates the TAB key.

Line Feed (LF or CTRL J) — Duplicates the LINE FEED key.

Carriage Return (CR or CTRL M) — Duplicates the RETURN key.

Escape (ESC or CTRL [ ) — Duplicates the ESC key.

Cancel (CTRL X) — Cancels the current escape sequence.

Circuit Description

To help you locate parts in the Computer or on the Schematic, the circuit component numbers (R1, C101, L301, etc.) for resistors, capacitors, coils, transistors, and integrated circuits are in the following groups.

0- 99	Parts mounted on the molded cabinet base or front panel.
100-199	Parts mounted on the power supply circuit board.
200-299	Parts mounted on the video circuit board.
300-399	Parts mounted on the keyboard circuit board.
400-499	Parts mounted on the terminal logic circuit board.
500-599	Parts mounted on the CPU logic circuit board.
600-699	Parts mounted on the serial interface circuit board.
700-799	Parts mounted on the cassette interface circuit board.
800-899	Parts mounted on the hard-sectored floppy disk interface circuit board.
900-999	Parts mounted on the video driver circuit board.

POWER SUPPLY CIRCUIT BOARD

Refer to the Schematic Diagram (part 3 of 3) (fold-in) as you read the power supply circuit description.

The primary circuit of the power supply consists of slow-blow fuse F1, ON/OFF switch SW3, 115/230-volt switch SW1, NORM/LOW line switch SW2, and the primary windings of transformer T1.

The red secondary windings of transformer T1 supply AC to diode bridge rectifier D109-D112. The 65-volt rectified output of the bridge is filtered by capacitor C1. It is used to power the video circuits.

The yellow secondary windings of T1 supply AC to the diode bridge rectifier BR1. The rectified output of the bridge (approximately 9 VDC) is filtered by capacitors C101 and C103 and is used on the logic circuit board.

The green secondary windings supply center-tapped 30 VAC to diode bridge rectifier D101-D104. The rectified output of the bridge (±18 VDC) is filtered by capacitors C102 and C104. This output is used on the logic circuit board.

INTERCONNECTION AND GROUNDING

The three power supplies (+65, +8.5, and ±18) are not interconnected on the power supply circuit board. Instead, they pick up their appropriate grounds at the circuit boards they power. The +65-volt video supply connects to + and ground points on the video circuit board. The external conductive coating of the CRT and the CRT socket arc-ring both connect directly to the video circuit board ground.

The +8.5-volt and ±18-volt supplies connect directly to the logic circuit boards with no common grounds until they meet at the terminal logic circuit boards.

This grounding method produces two independent operating systems that do not interact with each other except through the signal ground and sync/video inputs. In the event of a CRT arc, the arc discharge current is confined to the video circuit board and it does not induce transients into the logic circuits.

The logic/video system is also floating with respect to the ground wire of the power cord. The protective ground input (pin 1) of the EIA RS-232 connector connects to the power cord ground, along with all the exposed metal surfaces.

The signal ground input (pin 7) of the EIA RS-232 connector connects to the terminal logic circuit board ground.

VIDEO DEFLECTION CIRCUIT BOARD

Refer to the Schematic Diagram (part 1 of 3), and the Block Diagram (fold-out from Page 5-15) as you read the video circuit description.

POWER SUPPLY

The unregulated 65 volts DC from the power supply circuit board enters the video circuit board at plug P202, pins 2 and 3. Assume that the Computer has just been turned on and the output of the +53-volt regulator is at zero volts. The base current of Q201 is supplied through resistors R201, R202, and R203. The collector current of Q201 causes Q202 to turn on and supply current to the base of Q204. As the output voltage at the emitter of Q204 rises, D202 begins to supply current to zener diode D201 through resistor R202. D201 stabilizes at 12.8 volts and provides a reference for the output voltage. The divider formed by resistors R207 and R208 samples the output voltage as it continues to rise, and applies a fraction of the voltage to the emitter of Q201. When the emitter voltage of Q201 reaches 12.15 volts (12.8-.65), its collector current is reduced to a value that keeps the output voltage stabilized at +53 volts.

The current through R211, supplied to the load by Q204, generates a voltage that is applied through current limiting resistor R209 to the base of Q203. If the current thus developed exceeds about 1.1 amperes, Q203 turns on and shunts current from the base of Q202, which, in turn, prevents the output current from exceeding 1.1 amperes.

D203 and R212 form another zener regulator that supplies 6.2 volts DC to the video driver circuit board and 6 volts DC to the horizontal section through R213.

VERTICAL SECTION

The vertical portion of the video circuit board consists of two sections, a sweep generator and an amplifier.

The sweep (or ramp) generator consists of C208, C209, R221, and Q205. Capacitors C208 and C209 charge to +53 volts through resistor R221 to generate the ramp. This ramp voltage is applied to the anode of Q205, a programmable unijunction transistor. The gate of the unijunction is biased at a voltage determined by R215, R216, D204, and R217. When the anode voltage charges to the gate voltage, Q205 conducts and dicharges C208 to ground through L201. As the discharge current decreases to zero, the unijunction stops conducting and the capacitors start to charge again through R221.

The ramp voltage is applied to the base of Darlington voltage follower Q206. The emitter voltage of Q206 is fed back to the junction of C208 and C209 to linearize the exponential ramp. Resistor R222 and Vert Linearity control R223 determine the amount of correction applied to the ramp. The amplitude of the ramp is determined by R218 and the Vert Size control, R219.

The free-running frequency of the oscillator is slightly less than 60 Hz, the normal sweep rate. Vertical sync pulses, which enter the circuit board at plug P202, pin 6, are coupled through C206 and D204 to the gate of transistor Q205. The negative-going pulse lowers the gate voltage below the anode voltage and Q205 immediately conducts, discharging C208 and C209 before the free-running trip point is reached. This increases the oscillator frequency to 60 Hz (or 50 Hz if you set section 7 of switch S402 to its "1" position). Each succeeding sync pulse keeps the oscillator synchronized with the vertical sync signal generated by the CRT controller on the logic circuit board.

The amplifier portion of the vertical circuitry is composed of Q207, Q208, Q209, Q210, Q211, and Q212.

Under steady-state conditions, with no ramp signal applied to the base of transistor Q208, the collector currents of Q207 and Q208 are determined by bias string R225, R226, R227, R228 and emitter resistors R229 and R231. The collector current of Q207 is nominally 3 milliamperes, and the collector current of Q208 is nominally 2 milliamperes. The difference (1 milliampere) between the two, supplies base current to driver transistor Q209, which drives output transistors Q211 and Q212. Diode D205 and resistor R237 bias transistors Q211 and Q212 so that there is enough idle current to eliminate crossover distorsion. Transistor Q210 is a current source that provides base current for Q212 and the bias network, D205 and R237. The output voltage at the junction of R239 and R241 is fed back to the bias string through R234 to keep the output stable at about 25 volts.

When the ramp signal is applied to the input of the amplifier through C211, the collector current of Q208 is varied as a function of the amplitude of the ramp voltage. The difference between the currents of Q207 and Q208 drives the outputs through Q209. The output voltage is fed through C216 to the vertical deflection yoke. Resistor R242, which is in series with the yoke, generates a voltage proportional to the yoke current. This voltage is fed back to the base of Q207 (negative feedback), which changes its collector current to keep the yoke current directly proportional to the input ramp voltage.

HORIZONTAL SECTION

The horizontal portion of the video circuit board consists of three sections:

Time delay and pulse shaping.

Horizontal deflection.

High voltage supplies.

The time delay and pulse shaping circuits are triggered by the horizontal sync pulses that come from the logic circuit board. They generate a time delay that provides horizontal centering and a pulse of the proper width to drive the horizontal sweep system.

The horizontal deflection system transfers energy from the power supply to the yoke in order to sweep the beam across the face of the CRT. The high voltage supplies generate the anode and grid voltages that operate the CRT.

TIME DELAY AND PULSE SHAPING

The horizontal sync pulses enter the circuit board at plug P202, pin 1. These pulses are then coupled through R243, C217, and D206 to U201. The trailing edge of each pulse triggers U201, a timer used as a monostable multivibrator, causing the output (pin 3), to go high. The width of the output pulse is determined by C221, R247 and Horizontal Centering control R246. When the output pulse from U201 goes low, it triggers another timer used as a monostable multivibrator, U202. The 20 microsecond output pulse of U202 (pin 3) is determined by C223 and R249. This pulse drives horizontal driver transistor Q213.

HORIZONTAL SWEEP AND HIGH VOLTAGE

Transistor Q213 and driver transformer T201 drive horizontal output transistor Q214, which, in turn, drives the horizontal output transformer (flyback transformer) and the yoke. The positive-going pulse from U202 is coupled through the parallel combination of R251 and C224 to the base of Q213. During the time the pulse is high, the collector current of Q213 flows through the primary of T201. The phasing of the transformer is such that the secondary output voltage during this time is negative and keeps Q214 turned off. While Q213 is turned on and current flows through the primary, energy is stored in T201.

When the output pulse from U202 returns to zero volts, Q213 turns off, its collector current decreases to zero, the secondary voltage of T201 goes positive, and Q214 starts to conduct. The energy stored in the transformer is converted to base current and keeps Q214 turned on for the rest of the cycle. The transformer inductance, R254, R255, C226, and L202 control the base current decay and insure the best efficiency of the output transistor.

Transistor Q214 is a switch that controls the flow of energy through the deflection components. When Q214 is turned on, current flows from the power supply through the primary of horizontal output transformer T202 and through the horizontal yoke, L203, L204, and C232 to ground. During this time, the yoke current increases linearly and the beam is deflected to the right of the screen. When it reaches the right edge, driver transistor Q213 turns on and output transistor Q214 turns off. The energy that was stored in the yoke (along with the energy stored in the primary of T202) is transferred to C228 in the form of a half-wave voltage pulse with an amplitude of 550 volts. During this cycle, the current through the yoke goes to zero and the beam returns to the center of the screen.

Capacitor C228 now discharges into the yoke, inducting a current in the opposite direction, deflecting the beam to the left side of the screen. As the voltage across C228 decreases to zero volts, the resonant circuit of C228, the yoke, and the primary of T202 try to oscillate in a negative direction. The energy transferred to the yoke by C228 now provides the sweep current for the first half of the scan and charges C232 via damper diode, D208.

Shortly before the beam reaches the center (before the yoke current reaches zero), transistor Q213 is turned off by U202 and Q214 is turned on. For a brief period, both D208 and Q214 are conducting in opposite directions. D208 is conducting the yoke current and Q214 is conducting the primary current of T202. Transistor Q214 turns on early to guarantee a smooth transition from negative to positive yoke current.

The value of C232 is chosen to provide "S" shaping of the current waveform through the yoke. This compensates for stretching at the left and right edges of the screen. Since the deflected beam sweeps a wider area at the edges than it does at the center for a given deflection angle, the current is decreased slightly at the left and right edges.

Width coil L203 is in series with the yoke and its reactance can be adjusted to change the total current through the yoke. If its reactance is high, the yoke current is slightly decreased and the scan width is reduced. If its reactance is low, the scan width is increased.

Horizontal linearity coil L204 is a nonlinear inductor that provides further linearity correction that cannot be provided by C232 alone.

HIGH VOLTAGE SUPPLIES

The flyback voltage pulse developed at the collector of Q214 during the horizontal retrace is rectified by D211 and C231 to provide approximately 500 volts DC. This voltage, which is filtered further by R266, C235, C236, and C237 is coupled through R909, on the driver circuit board, to the CRT grid 2 (G2).

The same flyback pulse is transformer coupled to the secondary of T202 and rectified by D207 and C229 to generate a −100-volt DC supply.

Resistor R265 and Focus control R264 form a voltage divider between the +500-volt and the −100-volt supplies to provide a bias voltage for grid 4 (the focus grid). This voltage is coupled through R267 and R908, on the driver board, to G4 on the CRT.

Another voltage divider consisting of D209, R261, and G1 control R262, between the +55-volt and −100-volt supplies, provides a bias for grid 1 of the CRT.

The flyback pulse is also coupled to another secondary of transformer T202, the high voltage winding. The output pulse from this winding is about +15,000 volts. It is rectified by D1 (in the anode lead) and filtered by the internal capacitance of the CRT to provide the anode (or accelerator) voltage for the CRT.

Occasionally, the voltage stored in the internal capacitance of the CRT arcs over to the other electrodes. An arc ring built into the tube socket, and C233 (a capacitor with a parallel spark gap), in conjunction with driver circuit board series resistors R904, R907, R908, and R909, limit the amount of the arc energy on the video circuit board to a safe value.

Flyback transformer T202 also has a filament winding that supplies 6.3 volts AC at 450 milliamperes to power the CRT filament.

VIDEO DRIVER CIRCUIT BOARD

Refer to the Schematic Diagram (part 1 of 3), and the Block Diagram (fold-out from Page 5-15) as you read the video driver circuit description.

The voltages for the CRT, except for the anode supply and deflection voltages, are either generated on or pass through the video driver circuit board. The CRT 6.3 VAC voltage originates on the video circuit board and passes directly through the video driver circuit board to the CRT. The filament voltage is RF-bypassed to ground on the driver board by capacitors C907 and C908. A common ground also is routed from the video board through the driver board, and forms an arc-ground to the cathode and grid circuits of the CRT.

The video amplifier is a conventional cascade amplifier. The video signal is routed onto the board from rear panel Brightness control R1 and through resistor R905 to the base of transistor Q902. The base of transistor Q901 is biased by the 6.2-volt supply coming from the video circuit board. The signal at the collector of Q901 is coupled through resistor R904 to the cathode of the CRT. Choke L901, in series with collector load resistor R903, provides high frequency compensation.

Grid voltages for the CRT are routed through three, series-connected, current-limiting resistors on the driver board, R907 to grid 1, R908 to grid 4, and R909 to grid 2.

TERMINAL LOGIC CIRCUIT BOARD

Refer to the Schematic Diagram (part 2 of 3), and the Block Diagram (fold-out from Page 5-15) as you read the terminal logic board circuit description.

The terminal logic board consists of seven functional blocks:

1. Power supplies.
2. Keyboard encoder and configuration logic.
3. Processor/CPU.
4. Master block and system logic.
5. Communications.
6. CRT and memory control.
7. Display memory, character generator, and video control logic.

The integrated circuits in each block are numbered as follows:

U401-U405	Power supplies.
U426, U427, U429, U431, U434, U435, U440-U442	Master clock and system logic.
U413, U428, U430, U432, U433, U436-U439	Processor, ROM, RAM, processor control logic.
U443-U450	Keyboard encoder and configuration logic.
U452-U454	Communications and I/O drivers.
U414-U418	CRT and memory control.
U406-U411, U419-U425	Display memory, character generator, and video control logic.

POWER SUPPLIES

Integrated circuits U401 and U402 provide two regulated 5-volt supplies. U401 supplies 5 volts DC for the left half of the circuit board, while U402 supplies the right half of the circuit board. U403 supplies +12 volts DC, U404 supplies −12 volts DC, and U405 supplies −5.2 volts DC. These integrated circuits are internally protected against short circuits, overloads, and high temperatures. Capacitors C402, C404, C407, and C411 at the inputs of the regulators stabilize the supplies, while capacitors C403, C405, C408, C412, and C413 improve the transient response of the regulators. C412 serves as the input stability capacitor for U405 and as the output capacitor for U404.

MASTER CLOCK AND SYSTEM LOGIC

Clock And Scalers

The master clock is a 12.288 MHz crystal-controlled oscillator. Crystal Y401, with C419, C421, and U426E form the oscillator. The series combination of C419 and C421 serve as the load capacitance for the crystal. U426E is the gain stage. Resistors R408 and R409 bias U426E into its linear region, while C418 bypasses any AC feedback through the two resistors. The output of the oscillator is buffered by U426D to prevent loading on the output from changing the oscillator frequency. This output is the "dot clock" and it is used by the shift register to shift dot information to the screen.

The dot clock also drives divide-by-sixteen counter U427, which generates 1.536 MHz pulses. This is called the character clock. Each pulse corresponds to one character on the screen. U427 is a synchronous presettable counter that is loaded with a binary eight (1000). It counts dot clock pulses until its output reaches binary fifteen (1111). During the fifteenth count, the ripple carry output (pin 15) goes low. This pulse, which is inverted by U426F, puts a logic one on the load input (pin 9). The next positive-going clock cycle reloads a binary eight back into the counter and the cycle repeats. The Q_C output (pin 12) generates a 1.536 MHz pulse that serves as the clock for CRT controller U417 (pin 21). It is inverted by U412D. These two signals are referred to on the Schematic as $\overline{C}$ and C. The Q_B (pin 13) output generates a 3.072 MHz signal that drives the clock input (pin 16) of the ACE (U452).

The dot clock also drives U429. U429 is a divide-by-six and divide-by-two scaler. The clock drives the B input (pin 1), and the Q_D output (pin 8) generates a 2.048 MHz clock signal for CPU (U430). The Q_D output (pin 8) also drives the A input (pin 14). The Q_A output (pin 12) in turn drives the input of binary scaler U440.

The output of U440 provides a 128 kHz clock (pin 6) for the keyboard encoder, U444 and a 1 kHz signal (pin 14) for the audible bell signal.

System Control Logic

The system control logic consists of I/O and memory decoding, power-up and manual reset circuits, and the bell and key clock circuits.

I/O and memory decoding are accomplished by three-to-eight line decoders U442 and U435, respectively. U442 decodes address bits A5, A6, and A7, to generate eight I/O addresses:

1. Keyboard encoder ..... 200 (80_H)
2. Keyboard status ..... 240 ($A0_H$)
3. CRT controller ..... 140 (60_H)
4. Power-up configuration (primary) ..... 000 (00_H)
5. Power-up configuration (secondary) ..... 040 (20_H)
6. ACE (communications) ..... 100 (40_H)
7. Bell enable ..... 340 ($E0_H$)
8. Key click enable ..... 300 ($C0_H$)

Decoder U442 is enabled only during an I/O read or write operation to eliminate the possibility of false decoding on a refresh address coming from the Z80.

U435 decodes address bits 14 and 15 to generate three memory addresses:

1. Program ROM ..... 000.000 (00 00_H)
2. Scratchpad RAM ..... 100.000 (40 00_H)
3. Display memory ..... 370.000 (F8 00_H)

Whenever the Z80 performs a read or a write operation it will either write to or read from one of these memory or I/O addresses.

When the Computer is first turned on, the CPU, CRT controller, ACE, and keyboard control logic are cleared by the master reset signal. U431A, R412, C422, and D401 form the power-up reset circuit. When power is first turned on, C422 has no charge and temporarily holds pin 2 of U431A at logic zero. The output of U431 goes high and is inverted by U431B. The two outputs are the true and the complimented reset pulses. As C422 charges through R412, it pulls the input of U431 high, turning off the reset pulses.

A manual reset can also be accomplished if you simultaneously press the Reset and right-hand Shift keys on the keyboard. U446E and U446B are connected to those keys and they drive the inputs of U431D. The output of U431D (pin 11) is coupled through R413 to pin 1 of U431A. R413 and C423 form a de-bounce circuit for the Shift and Reset keys. When the output of U431D goes low, the input of U431A is also pulled low. This generates a reset pulse.

The CPU, under the control of the ROM program, can cause a bell tone or a key click to sound through the speaker. When the CPU addresses I/O port 340, pin 7 of U442 triggers one-half of monostable U441. Its output goes low for about 200 milliseconds, causing the output of U431C to go high. This logic 1 is NANDed in U434C with the 1000 Hz signal coming from U422. The output of U434C drives speaker SP1. Diode D402 keeps the output of U434C from being driven above 5 volts at turn-off by the inductive reactance of the speaker.

When the CPU addresses I/O port 300, pin 9 of U442 triggers the other half of U441. Its output (pin 7) goes low for about six milliseconds and turns on the 1000 Hz tone. This short duration causes the tone to sound like a click.

PROCESSOR

The processor section of the Terminal consists of the Z80 processor, U430, the CPU (central processing unit), ROM (read only memory), RAM (random access memory), and processor control logic.

Processor/CPU

The heart of the terminal logic circuit board is the Z80 CPU. It acts as a scheduling or dispatching service for the data coming into or originating from the Terminal. It examines the data it receives and determines what, if anything, it should do with it. If the data comes from the ACE (U452), for example, the Z80 will compare the ASCII word with a set of conditions determined by the ROM program, and then write the word into the appropriate memory or I/O port. If the ASCII word is a bell signal, the CPU addresses I/O port 340, and the bell tone sounds through the speaker. If the word is the letter "B," the CPU performs a memory write to the current cursor position in the display memory. If the data from the ACE is a nonvalid character or a string of characters, the CPU simply ignores the data and does nothing.

The ROM program that directs the CPU is rather long and complex, but the mechanics of the process are easy to follow. The 2.048 MHz clock signal drives the clock input (pin 6) of the CPU through U426A. This steps the CPU through an internal "Machine" cycle that starts with a fetch instruction. It executes the remainder of its instructions by stepping through a precise set of a few basic instructions. These include memory read, memory write, I/O read, I/O write, and interrupt acknowledge. The basic thing to remember is that the ROM program directs the Z80 to make decisions and move data from place to place within the circuit board. Without the CPU and ROM, the decisions and data movement would have to be accomplished with hard-wired logic packages.

ROM

The read only memory, U437, is a pair of 4K × 8-bit (32768 bit) ROMs. Its twelve address inputs connect to A0 through A11 of the address bus and its eight data outputs connect to D0 through D7 of the data bus. U413A, U413B, and U434D decode the ROM select line coming from memory decoder U435.

RAM

The random access memory for the Z80 scratchpad consists of U438 and U439, 256 × 4-bit RAMs. This scratchpad RAM provides temporary data storage for the Z80. The address inputs to each IC connect to A0 through A7 on the address bus. The lower four bits of data (D0-D3) are provided by U438; the upper four bits (D4-D7) are provided by U439. The select signal comes from U435.

Processor Control Logic

The processor for the Terminal requires some additional circuitry to control the interrupt process, and to provide a wait cycle for keyboard encoder U444, which is slow in responding to a read cycle.

U432C is a 2-input NOR gate that monitors the INTRPT output of the ACE (U452) and pin 6 of U447B (the keyboard INTRPT). When either INTRPT output goes high, the output of U432C goes low and signals the INT input (pin 16) of the Z80 that data is available from the ACE or keyboard.

U433, U432A, and U432B form a counter that drives the $\overline{\text{WAIT}}$ input (pin 24) of the Z80. Whenever the Z80 performs an I/O read at the keyboard encoder, pin 11 of U442 drives the "reset to zero" inputs (pins 12 and 13) of U433. The Q_A and Q_B outputs (pins 9 and 5) of U433 drive the inputs of U432B, a 2-input NOR gate. The output of U432B holds the Z80 $\overline{\text{WAIT}}$ input low whenever the Q_A or Q_B outputs of the counter are high. This generates a total wait of four clock cycles (one wait cycle is automatically inserted by the Z80 on an I/O instruction) to allow the output buffer of U444 to turn on. When the Q_C output (pin 4) of counter U433 goes high, it drives the input of U432A high. This forces the output low and turns off the A input (pin 10) of U433. The Q_A and Q_B outputs now go low and the wait signal is no longer present. The Z80 then finishes up the I/O read cycle (pin 11 of U442 goes high) and the counter is reset to zero and held there until the next keyboard read.

U428 provides a nonmaskable-interrupt (NMI) that operates under the control of the ROM program. The NMI routine is used when the program wants to read something into the CRT Controller (or CRTC) during the vertical blanking period. The data input of U428A is driven by A2 of the address bus. The T, or clock, input is driven by the complemented CRT controller I/O select that comes from pin 12 of I/O decoder U442 through U412C, which provides the complement of the signal. When the program wants to write during vertical retrace, it addresses the CRT controller while holding A2 high. The Q output of U428A is clocked high and drives the reset input of U428B high. The vertical sync signal from U417 drives the T input of U428B and clocks the Q output low as soon as the sync signal begins. The NMI input of the Z80 goes low and the program immediately jumps to the "update CRTC" routine. Part of that routine will write a zero to the data input of U428A to clear the NMI signal.

KEYBOARD ENCODER AND CONFIGURATION LOGIC

Keyboard Encoder

The keyboard of the Terminal consists of single-pole, single-throw switches in a matrix that is scanned by keyboard encoder U444. Outputs X1 through X9 go high, in sequence, and drive one of the Y1 through Y10 inputs if one of the switches is depressed. The encoder uses the X and Y information to generate a

unique binary code for each matrix intersection, and this code is latched internally when a key is depressed. The encoder generates a data strobe (DS), which comes from pin 13 of U444, for each key closure. DS clocks the T input (pin 3) of U448A and the $\overline{Q}$ output of U448A goes low. The $\overline{Q}$ output drives an input of U447B. The output of U447B, an $\overline{INT}$ signal, is coupled to Z80, pin 16. When the Z80 services the interrupt at I/O port 200, pin 11 of U442 clears U448A (through U447C and U446A) and the $\overline{INT}$ signal is removed. Pin 36 of U444 is also a binary data output and it is latched in U448B by the I/O read at 80H (200Q). The keyboard interrupt routine also checks the keyboard status in another I/O read operation. The keyboard status check reads the state of the following:

1. Control key.
2. Shift keys.
3. Repeat key.
4. Break key.
5. Off-line key.
6. Caps Lock key.
7. Data Strobe.
8. Data bit latched in U448B.

The ROM program uses this information in conjunction with the encoder data to determine the routing of the data within the Terminal. Pin 10 of I/O decoder U442 drives enable inputs (pin 19) of buffers U449 and U450 to put the status information on the bus. The Caps Lock, Break, Off Line, Control, Repeat, and Shift (left) keys are connected directly to the inputs of these buffers. The outputs of U448A and U448B are also connected to the inputs of the buffers.

The binary data outputs of the keyboard encoder drive the address inputs (A0-A7) of ROM U445. U445 converts the binary data from the keyboard encoder to ASCII data. The data outputs of U445 drive the D0-D7 bits of the data bus. The chip select input (pin 18) of U445 is driven by pin 11 of U442 (the I/O decoder).

When the Repeat key is held down, the input of U446D is low and its output is high. This enables the repeat rate oscillator, U447A, R437, C481, and Q402. The repeat frequency, approximately 15 Hz, is determined by R437 and C481. When the Repeat key is released, the output of U446D goes low, forcing the output of U447A high and disabling the repeat function.

The two shift keys are NORed together in U447D. Its output drives the shift input (pin 21) of U444. When the Control key is typed, the output of U446F is forced high, which drives the control input (pin 19) of keyboard encoder U444.

Configuration (Power-up) Logic

When the system is first turned on, the ROM program must program the ACE (U452) for the baud rate and parity that you selected on switches S401 and S402. The program addresses I/O port 00H (000Q). Pin 15 of I/O decoder U442 drives enable inputs of U449 and U450 to put the information selected by the switches on the bus. The program then interprets the data and configures the ACE accordingly. I/O address 20H (040Q) is used in a similar manner. Pin 14 of the I/O decoder U442 enables buffer U443 and puts the data from S402 on the bus.

COMMUNICATIONS AND I/O DRIVERS

The Terminal talks to the outside world through an Asynchronous Communications Element (ACE) and EIA RS-232C compatible line drivers and receivers. The ACE (U452) converts parallel ASCII data to serial data and drives the communications line through line driver U453. The ACE also converts serial data coming from line receiver U454 into parallel ASCII data. The ACE puts this data on the bus when the ROM program requests it.

ACE/UART

Refer to the (ACE) Block Diagram (fold-out from this page) as you read this circuit description.

U451 is an Asynchronous Communications Element that performs the following functions:

1. Converts data from parallel to serial and vice versa.
2. Divides a master clock frequency by a programmed divisor to generate a desired baud rate.
3. Programs the data characteristics, parity, stop bits, and character length.

The characteristics of the ACE must be programmed into the internal registers of U452 by the ROM program through the address and data busses. Bidirectional data bits (pins 1-8) of U452 connect to the system data bus. The address inputs (pins 28, 27, and 26) connect to the system address bits A0, A1, and A2. When the ROM program addresses I/O port 40H (100Q), pin 13 of I/O decoder U442 selects the $\overline{CS2}$ input (pin 14) of the ACE. The Z80 can then read or write data by enabling the data input and data output strobes at pins 21 and 18 ($\overline{DISTR}$ and $\overline{DOSTR}$) of U452.

When the ACE receives a complete serial word from the EIA interface, it signals the Z80 that there is data available by pulling the Z80 $\overline{INT}$ input (pin 16) low. The Z80 then examines the internal status and data registers of the ACE, reads the data word, and routes it to the proper device within the Computer.

I/O Drivers

The standard EIA interface communicates by means of a serial stream of voltage levels that correspond to logic ones and zeros. A logic one (or mark) on the data lines is a voltage between −5 and −15 volts. A logic zero on the data lines is a voltage between +5 and +15 volts. On the control lines ($\overline{DTR}$, $\overline{RTS}$, $\overline{RLSD}$, $\overline{DSR}$, CTS), a voltage between +5 and +15 volts is considered to be ON, and a voltage between −5 and −15 volts is considered to be OFF.

U453 is a standard EIA line driver. A logic one on the input of U453C drives the serial data outline to an EIA logic one, or "mark." A zero on the input forces the line to an EIA zero, or "space." U453B and U453D drive control lines DTR (Data Terminal Ready) and RTS (Ready to Send) in a similar manner.

U454 is a standard EIA line receiver. The serial data in line drives the input of U454A, which converts the EIA voltages to TTL levels and drives the serial input of the ACE. Likewise, the RLSD, DSR, and CRS line signals drive the inputs of U454B, U454D, and U454C, respectively. The outputs drive the appropriate control inputs of the ACE.

The I/O connector on the back panel of the Computer is a standard 25-pin D-type plug with the data and signal line connected as follows:

1. Protective or chassis ground.
2. Serial Data Out.
3. Serial Data In.
4. Request To Send (RTS).
5. Clear To Send (CTS).
6. Data Set Ready (DSR).
7. Signal ground.
8. Received Line Signal Detector In (RLSD).
20. Data Terminal Ready (DTR).

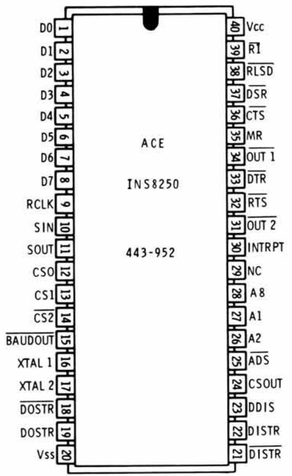
CRT AND DISPLAY MEMORY CONTROL

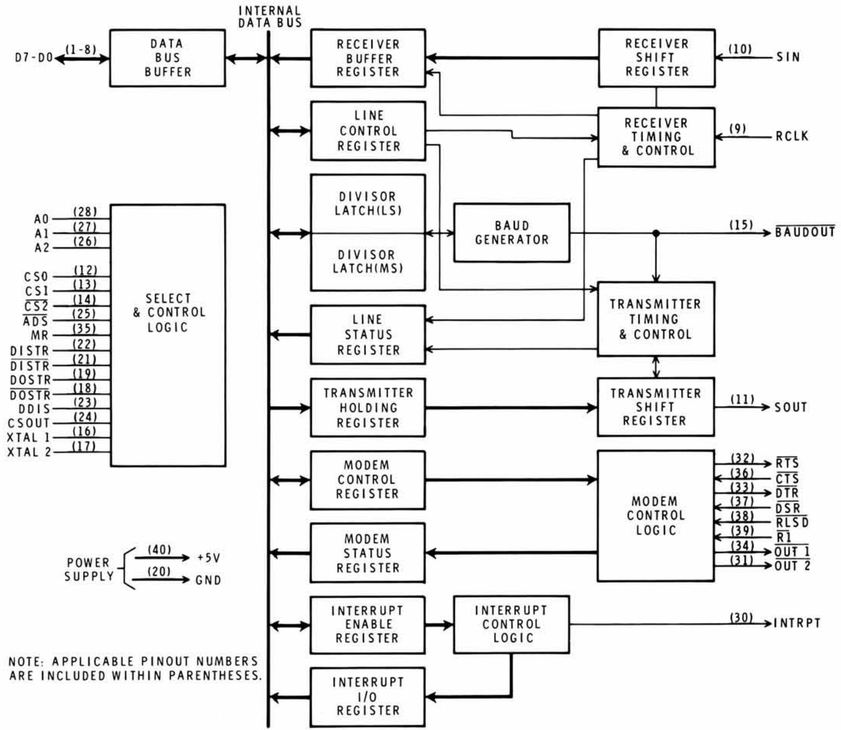
The heart of the video logic system is the CRT controller. This device generates all of the sync and blanking signals and display memory addresses for the video system, The memory control is used to select either the address coming from the CRT controller or the address bus, and to synchronize read and write pulses.

CRT Controller

The CRT controller, U417, is a fully programmable device that is set up by the ROM program during power-up. Its didirectional data bits (pins 33-26) connect to system data bits D0-D7. Its address or programming inputs come from the following four input pins:

Pin 22. Read/Write (R/$\overline{W}$) — Determines whether the controller's internal register file is to be written to or read from. A write is a logic zero.





ASYNCHRONOUS COMMUNICATIONS ELEMENT (ACE) BLOCK DIAGRAM

Pin 24. Register Select (RS) — Selects either the address register (RS=0) or one of the data registers (RS=1) of the internal register file.

Pin 25. Chip Select ($\overline{CS}$) — A zero sets the CRT controller to read or write the internal memory file.

Pin 23. Enable (E) — Enables the I/O buffers and clocks data to and from the CRT controller. Data is clocked on the falling edge of the enable signal.

The internal registers are written to or from by means of the address register. The Z80 sets up the programmable registers by first writing a register number into the address register when the register select input is low. It then performs a write operation when the register select input goes high.

Each of the CRT controller's registers is programmed at power-up with appropriate data to generate the SYNC, timing, and refresh signals. The memory address outputs (MA0-MA10) drive the address inputs of the display RAM through multiplexers U414, U415, and U416. The scan row address outputs (RA0-RA3) drive the address inputs of character generator U420. The display enable output (DISPLAY) is a logic one whenever the CRT controller, U417, is addressing a port of the RAM during the time it should be displayed. This serves as a blanking output whenever it is a logic zero. The cursor output goes to a logic one when the RAM location being addressed is equal to the address stored in the cursor address registers.

Controller Read/Write Logic

The $\overline{CS}$ and E inputs of the CRT controller must be selected in a particular sequence to perform read and write operations to and from the controller. The enable input pulse (pin 23) must always be inside the $\overline{CS}$ pulse. When the I/O request for address 140 appears at pin 12 of U442, the clear input of U418A goes low, and the Q output immediately drives the $\overline{CS}$ input low. The Q output drives the data input of U418B to a logic one. At the same time, U412C puts the Clear input of U418B at a logic one.

The next CPU clock pulse at pin 11 of U418B clocks the logic one at the data input through to the Q output. This delays the leading edge of the enable pulse until approximately one clock cycle after the leading edge of the $\overline{CS}$ pulse. When the I/O request at address 140 goes away (returns to logic one), the output of U412C immediately clears U418B. U418B's Q output (pin 9) drives the E input of the CRT controller to zero. The clear input of U418A goes high at the same time, but the Q output remains low until the next CPU clock pulse at U418A's clock (pin 3) clocks the logic one at the data input through to the output, terminating the $\overline{CS}$. This delays the trailing edge of the $\overline{CS}$ pulse until after the trailing edge of the E pulse.

Display Memory Control

The display memory control consists of an address bus multiplexer, a bidirectional bus buffer, and some gates that control the display memory write enable (WE) and chip select ($\overline{CS}$) inputs.

The address bus multiplexer consists of quad 2-input multiplexers U414, U415, and U416. Their select inputs are tied together and controlled by memory decoder U435. When no read or write operations are being performed on the display memory, the select inputs are at a logic one, and the memory addresses (MA0-MA9) generated by the CRT controller drive the address inputs (A0-A9) of RAMs U408-U411. Memory address MA10, generated by the CRT controller, is used to select either the upper or the lower 1K bank of video RAM. When the Z80 addresses the memory, pin 9 of U435 pulls the select input to a logic zero, CRT controller memory addresses MA0-MA9 are disconnected from the display RAM, and address bus bits A0-A9 are connected to the RAM address inputs. The Z80 can then read from or write into the display RAM.

Bus buffer U407 isolates the main data bus from the secondary or refresh bus. During the screen refresh period, the data outputs of the display RAM drive the data inputs of the character generator continuously. This would prevent the processor from having access to the bus except during retrace times. However, by isolating the refresh bus from the main bus, the Z80 can have continuous access to the main bus, and the display RAM and character generator can have continuous access to the secondary bus (refresh bus). When the Z80 needs access to the display RAM, it addresses the memory, which enables U407 through pin 9 of U435, and connects the main bus directly to the secondary bus.

U412A and U412B provide the $\overline{CS}$ signals for the display RAMs. During the screen refresh cycle, pin 11 of U414 is driven by A10 and pins 1 and 4 of U412 are logic one. The output of U412A provides the $\overline{CS}$ for RAMs U408 and U409 and drives input pin 5 of U412B. The output of U412B is the complement of the $\overline{CS}$ signal and it drives the $\overline{CS}$ input of RAMs U410 and U411. During a display RAM read or write cycle, pins 1 and 4 of U412 are driven by the RD + WR signal coming (indirectly) from pin 3 of U434A. This eliminates the possibility of a contention problem on the secondary (refresh) bus between the display RAMs and buffer U407.

The write (WE) inputs of the RAMs are connected together and they are controlled by U413C. The WE (pin 8 of U413C) cannot go low unless pin 9 of U435 is low (memory is selected), the signal is delayed slightly to avoid a timing race with memory selection, and the Z80 WR output is low.

DISPLAY MEMORY, CHARACTER GENERATOR, AND VIDEO CONTROL LOGIC

This section of the terminal logic circuit board essentially runs by itself (in conjunction with the CRT controller) after being programmed by the Z80. The CRT controller continually provides refresh addresses for the display RAM, while the output of the RAM continually provides data for the character generator and the video shift register.

Character Generator

Character generator U420 is a 2048 × 8 (16384 bit) read only memory (ROM) that converts the ASCII data stored in the display memory into dot information for the video shift register. Address inputs A0-A3 (pins 5-8) are driven by the scan row address outputs of the CRT controller (RA0-RA3) to select a particular row of dots within a character space. Address inputs A4-A10 connect to the secondary data bus through 8-bit latch U419. These inputs use ASCII data to address the dot data stored in the ROM. The data outputs (01-08) of U420 supply video dot data to the parallel inputs of video shift register U421.

The inputs of 8-bit latch U419 connect to the secondary data bus. Data bits D0-D6 are latched into U419A-G and drive the character generator. Data bit D7 is the reverse video bit. It is latched in U419H and drives an input of U423A.

Video shift register U421 latches parallel dot data from the character generator at inputs A-H and shifts it out of output Q_H in synchronism with the dot clock (the dot clock drives the clock input, pin 7). The shift register is loaded (the dot data is latched) on a positive-going transition of the dot clock while the shift/load input is held low by the ripple carry coming from pin 12 of U426F. The dot data at input H appears immediately at output Q_H. The next leading edge of the dot clock shifts the data that was latched at Q_G. The next edge of the dot clock will shift the data that was latched in Q_F, and so on. After the data from Q_A is shifted to the Q_H output, the load input goes low, and the next character cycle begins.

Video Control Logic

The video control logic consists of two sections: a series, or chain, of gates and latches associated with video cursor, and reverse video data; and a chain of gates and latches associated with blanking data.

The display enable (blanking) and cursor data from pins 18 and 19 of the CRT controller is coincident with MA0-MA10, which address the display RAM. The display enable bit is latched in U424F (after passing through AND gate U423C) by the complemented character clock pulse coming from pin 11 of U412D. The cursor bit is latched in U424F. This delays the two signals by one character time. They are delayed for one more character time by being latched in U424E and U424G, respectively. The two character delays are necessary to compensate for the delays in the display RAM/character generator "pipeline."

When MA0-MA10 address the RAM, it takes approximately 450 nS for the data to be valid at the outputs. Once it settles down, the next character clock latches it in U419. The data at the output of U419 then addresses character generator U420. The data at the output takes another 450 nS to settle, and it is latched in the shift register by the following clock pulse. (Since the character clock pulses are 650 nS apart, the RAM and character generator outputs have plenty of time to settle.) This two-character delay matches the delays for the cursor and display enable, so that everything is synchronized.

The reverse video bit (D7) in the display RAM is latched first in U419, and then in U424H (after passing through AND gate U423A), so that it too arrives coincident with the video, blanking, and

cursor data. The video dot data from pin 13 of video shift register U421 and the cursor data coming from pin 16 of U424G are exclusive-ORed in U425A. This causes the cursor dots to reverse when the cursor happens to be coincident with video information, and keeps the cursor from disappearing when it occupies the same space as a character.

The video/cursor information coming from pin 3 of U425A is then exclusive-ORed in U425B with the reverse video data coming from pin 19 of U424H. When pin 19 is logic zero, the video/cursor data passes through U425B just as it is entered. If pin 19 of U424H is logic one, the data is reversed, and the character appears on the screen as black dots on a white background. The reverse video function can be disabled under the control of the ROM program when a logic zero is written into latch U422B via the address bus. Address bit A3 drives the data input of U422D, and its clock input is clocked when the CRT controller is addressed (I/O address 140). If the reverse video is to be ignored, the Q output (pin 9) of U422B puts pin 1 of AND gate U423A at a logic 0 and disables the reverse video bit coming from pin 19 of latch U424H.

The video/cursor/reverse data coming from pin 6 of U425B is ANDed in U423D with the display enable data coming from pin 12 of U424E. If the display enable is logic 1, the video data goes to the video circuit board; if it is a logic zero, the video is blanked.

When the Z80 performs a read or write operation on the display RAM, it disturbs the pipeline, and the data on the secondary (refresh) bus does not coincide with what should be written on the screen. Consequently, the video is blanked during a read or write. When pin 9 of memory decoder U435 goes low to select the display RAM, it also drives the clear input (pin 1) of U424. The Q output (pin 6) of U424C drives pin 9 of AND gate U423C to a logic zero and disables the display enable. At the same time, the Q output (pin 12) of U424E drives pin 12 of AND gate U423D to a logic zero, blanking the video information coming from the video chain. The screen will blank as long as the RAM is selected.

When pin 9 of U435 goes high to deselect the RAM, U424 is no longer held cleared. The logic one at the D input of U424C is clocked through to its Q output on the next character clock pulse, and it is clocked through U424D and U424E on the next two pulses. This three-character delay gives the pipeline time to reload with valid information before the video is enabled.

The propagation delays through the various gates and latches (U421, U425A, U425B, and U424) from the edge of the character and dot clocks to their various outputs is not always constant, so another delay is used. Latch U422A acts as a mini-pipeline, clocked at the dot rate. The data input to U422A is the composite video/cursor/reverse/blanking data, and its T input is clocked by the dot clock. This 80 nS delay lets all data settle to valid states before it is sent to the video circuit board.

The sync and video signals are buffered before they leave the terminal logic circuit board. U406A inverts and buffers the video data. U406C inverts and buffers the vertical sync signal coming from pin 40 of the CRT controller. U406D buffers the horizontal sync signal coming from pin 39 of the CRT controller.

CPU LOGIC CIRCUIT BOARD

Refer to the Schematic Diagram (part 3 of 3), and the Block Diagram (fold-out from Page 5-21) as you read the CPU logic circuit description.

SYSTEM CLOCK

Crystal X501, in conjunction with U501A, forms a crystal oscillator which operates at 12.288 MHz. Capacitors C501 and C503 provide the load for the crystal, while R501 and R502 force U501A to operate in its linear mode. C502 acts as a low-pass filter to insure that the crystal will determine the operating frequency of the circuit rather than the delay time of U501A.

U502 operates both as a divide-by-6 scaler, resulting in a 2.048 MHz clock signal, and as a divide-by-two scaler acting on the 2.048 MHz signal to provide U503's clock. U503 operates as a divide-by-1024 scaler and provides the 2 mS clock signal.

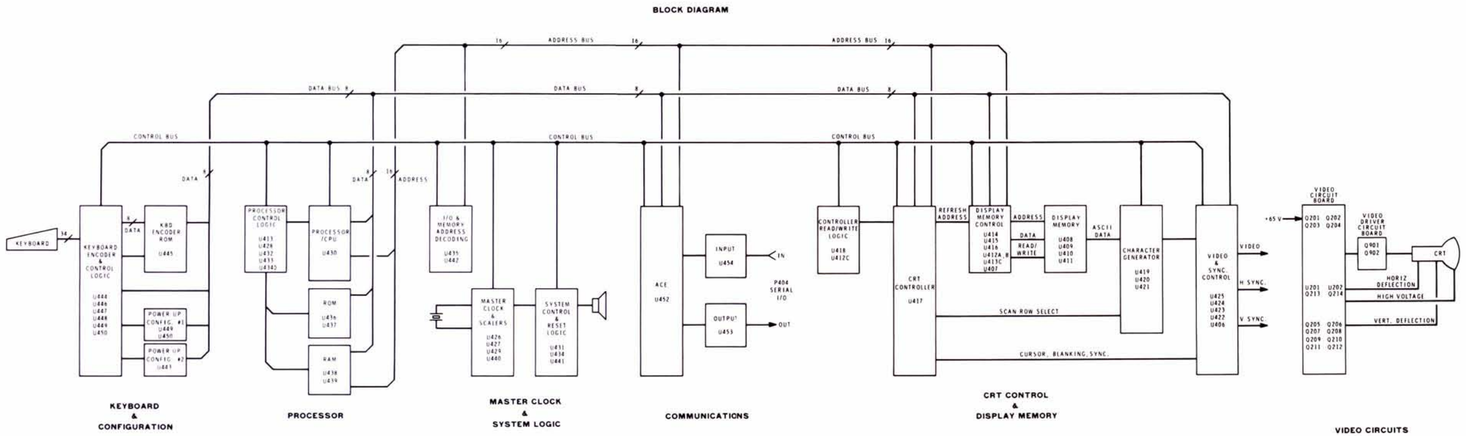
POWER-UP AND RESET

When power is first applied, capacitor C507 is discharged. As the +5 V source becomes active, C507 begins to charge. Approximately 150 mS after the +5 V source reaches +5 volts, pin 6 of U508B goes low and pin 8 of U501D goes high and terminates the power-up reset operation.

As long as the reset and shift keys are held down on the keyboard, pin 3 of U506A is held low and the display electronics are continuously reset. However, the Computer is not reset until the keys are released. This insures that the display will complete its reset function before the Computer resets; thus resulting in a proper indication on the display.

The rising edge of the KBRST L signal toggles U506A and causes its Q output (pin 5) to go high. This signal is coupled to a 50 μS one-shot (U507A) by U508A, and is the trigger signal for the one-shot. U507A's output is the reset signal used by the Computer and is coupled to the Computer by U508B and U501D.

U508A and U508D form an R-S flip-flop which guarantees that a keyboard reset will occur only during the op code fetch portion of an M1 cycle. Therefore, the refresh for dynamic memories will not be disturbed and no information will be lost.



TERMINAL LOGIC AND VIDEO CIRCUITS BLOCK DIAGRAM

CENTRAL PROCESSING UNIT (CPU)

The CPU is a Z80 microprocessor which runs at 2.048 MHz. Figure 5-1 shows the timing during an M1 cycle (instruction fetch). Notice that signal $\overline{M1}$ occurs prior to the refresh signal during the instruction fetch.

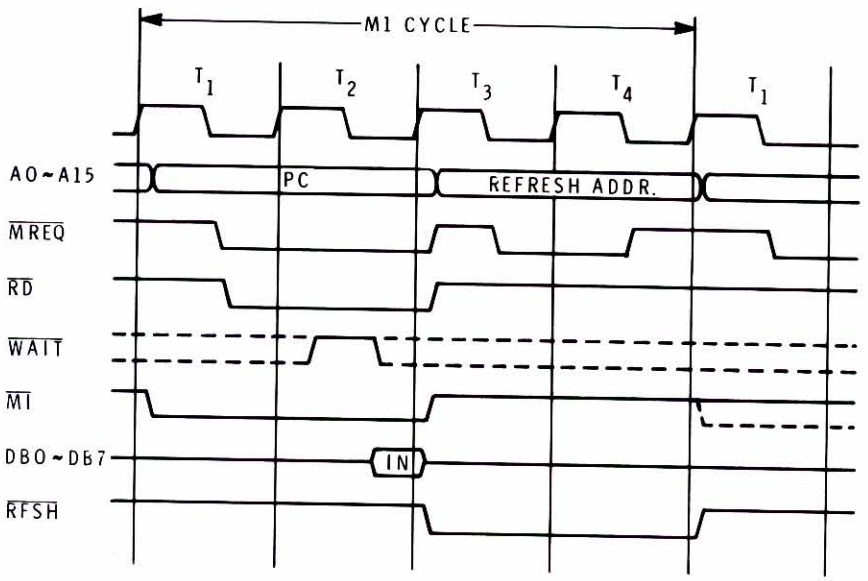


Figure 5-1

Figure 5-2 shows the timing of a memory read and memory write cycle.

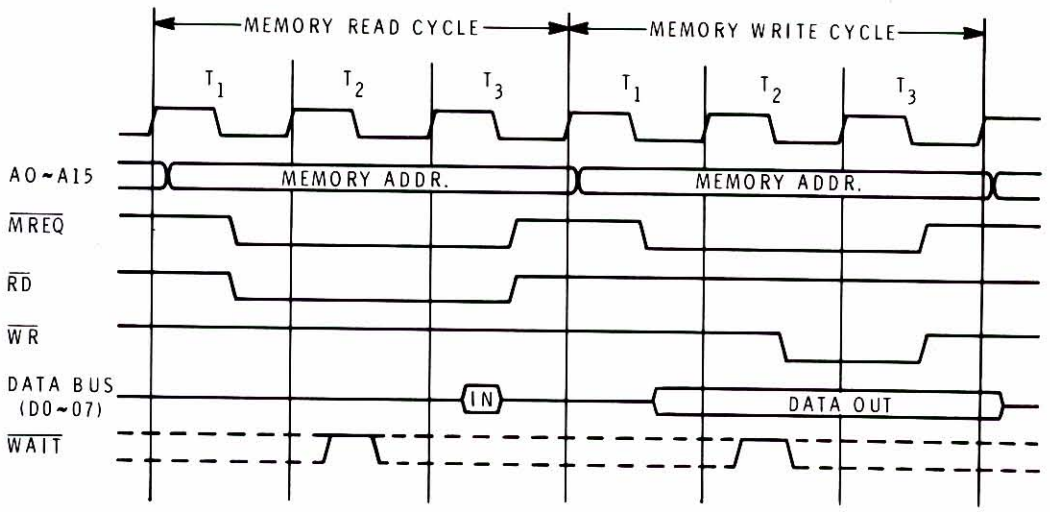


Figure 5-2

Figure 5-3 shows the timing during an I/O cycle.

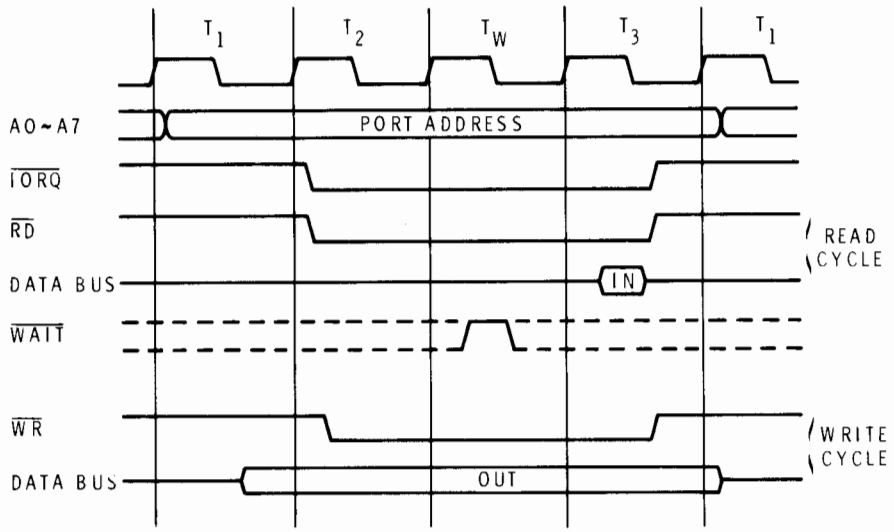


Figure 5-3

Figure 5-4 occurs only at the end of an instruction cycle that both an $\overline{M1}$ and an $\overline{IORQ}$ are generated.

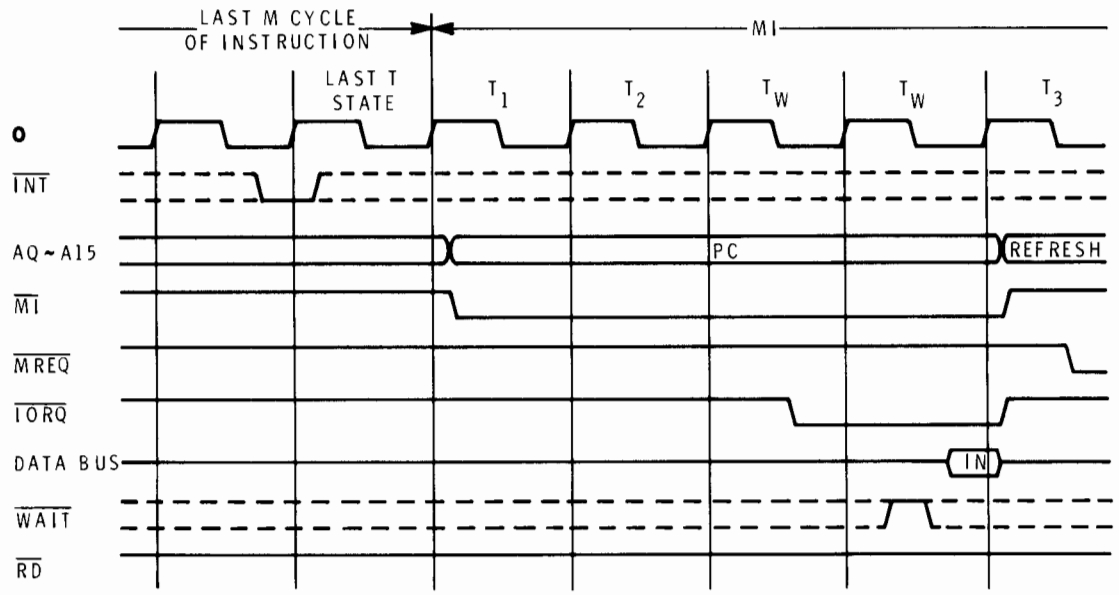


Figure 5-4

CONTROL LOGIC

U509 is a non-inverting buffer, while U562D complements BM1 L to produce BM1 H. U515A OR's the I/O request and memory request signals to produce the latch address signal (LA L). U562A and U562B form a 100 nS delay for the memory request signal; thus DMERQ L is the delayed memory request. This delay occurs only on the leading edge and not the trailing edge of the signal.

ADDRESS LATCH

U510 and U511 are transparent latches. Any data at their inputs is transferred to their outputs when LA L is high. When LA L is low, the last data pattern to occur just before the LA L high-to-low transition is retained at their outputs.

MEMORY MAP DECODER

U517 and U516 are PROMs which decode the latched address lines and determine which memory chips are to be enabled. Specifically, U517 determines which of the eight 8K banks is to be enabled, and U516 determines which of the 1K pages within bank 0 is to be enabled. However, the address lines are not the only criteria used to determine memory selection.

Jumpers JJ501, JJ502, and JJ503 select various memory configurations. That is, if only 48K of user RAM is installed, then JJ501 is jumpered for "0," JJ502 is jumpered for "1," and JJ503 is jumpered for "B." As a result, RAS0 L, RAS1 L, or RAS2 L, will be selected (coincident with the selected address being within banks 1 and 2, 3 and 4, or 5 and 6). In addition, NOMEM L will be asserted low whenever bank 7 is accessed. This results in U521 being enabled and all 0's being forced onto the data bus (required by some software memory sizing routines). If , however, 64K of user memory is installed, JJ501 and JJ502 will be jumpered for "1," and JJ503 is again a "B." Now, when bank 7 is addressed, RAS3 L will be asserted instead of NOMEM L. Access to 64K of RAM requires setting the CP/M ORG 0 latch in the software to configure bank 0 as RAM.

The write enable line (WE L) will be asserted low whenever there is no read (BRD L is high), no refresh (BRSH L is high), memory is selected (DMERQ L is low), and the bank selected contains writeable memory. Thus, since NOMEM L contains no writeable memory, WE L cannot be asserted if NOMEM L is asserted. However, bank 0 contains both writeable and non-writeable memory. Therefore, WE L will be asserted for bank 0 if the first three conditions are met regardless of the fourth condition. It is up to U516 to either enable or not enable the page select lines (MC5001 L, MC5023 L, MC505 L, and MC5067 L), depending on whether the memory addressed is writeable or not.

Write enable line 0 (WE 0 L) is used with the 1K of RAM associated with the floppy disk. It is only asserted when WE L is asserted, MC505 L is asserted, and FMWEN H is asserted. It is controlled by bit 7 of I/O port 177.

If the refresh line (BRFSH L) is asserted low, then WE L is not asserted. In addition, RAS0 L, RAS1 L, and RAS2 L will be asserted (consistent with the position of jumpers JJ501, JJ502, and JJ503) regardless of the bank address. This insures that all applicable dynamic RAM will be refreshed.

DYNANIC RAM MULTIPLEXER

U513 and U514 multiplex the 14 address lines required for 16K of memory into the 7 lines available on the memory chips. U512A is used to clock the row and column addresses into the memory chips in the proper sequence and at the proper time. Assume that a memory cycle has just begun (DMERQ H is high). At this time, the row addresses are multiplexed onto the memory address lines (A0-6 L) and the applicable RAS line (RAS0-2 L) is asserted low; thus, latching the row address into the memory chips. One half clock cycle later, U512A is toggled. This causes the row addresses to be removed from the memory address lines (A0-6 L) and the column addresses (A7-13) to be multiplexed in. A short delay later (determined by R514 and C522), the CAS L line is asserted and the column address is latched into the memory.

The multiplexer will be returned to its normal state (RAS address selected) when either a refresh cycle is initiated (clears U512A) or after the first clock cycle following the memory cycle (DMERQ H is low, causing the Q output of U512A to go low).

SYSTEM ROM

U518 is the system ROM which resides in the bottom 2 pages of memory (0, 1). An additional 2K of ROM can be added to the system at Pages 2 and 3 by installing jumper JJ507 at "A." Jumpers JJ504, JJ505, and JJ506 are used to switch between the 3-voltage EPROMs and the single voltage ROMs. When the jumpers are installed in their 0 locations, then the 3-voltage EPROMs are used.

FLOPPY DISK ROM

U520 is the floppy disk ROM which resides in the address map at Pages 6 and 7. It is restricted to a single voltage ROM. However, by moving jumper JJ507 to "B," U519 will serve as the floppy ROM and a 3-voltage EPROM can be installed. It is now no longer possible to use 4K of system ROM.

FLOPPY DISK RAM

U523 and U525 are used by the floppy disk and reside in Page 5 of bank 0 of the memory map. They are organized as 1K × 4 static RAMs. Provisions are made for an additional 1K of static memory at Page 4. However, it cannot be write protected as the memory at Page 5 can.

SYSTEM RAM

The system RAM is organized as 16K × 1 dynamic RAMs and resides in banks 1, 2, 3, 4, 5, 6, and 7. U526 through U533 comprise banks 1 and 2, U534 through U541 comprise banks 3 and 4, and U542 through U549 comprise banks 5 and 6. Bank 7 is accessible when the memory expansion board is installed and JJ501 through JJ503 are properly positioned.

INTERRUPT LOGIC

U557 detects that an interrupt request has occurred. It transmits this information to the processor by the INT L line. The interrupt priority is also determined by U557, and is available on output pins 6, 7, and 9. This information is transmitted to the data bus during the interrupt acknowledge cycle by U558.

The highest priority is interrupt level 5, while the lowest priority is the 2 mS clock at level 1. In processing the interrupt, the CPU is operating in the 8080 mode. Therefore, the data on the data bus at acknowledge time is an instruction (U558 encodes the data from priority encoder U557 such that the processor sees a restart instruction). This instruction directs the processor to execute the instruction at ROM address 10 for the 2 mS clock, at address 20 for the single step, at address 30 for the INT 3L, etc.

I/O MAP DECODER

U550 is a 256 × 8 PROM, and decodes the various I/O ports required by the Computer. I/O F2H (362Q) is the general purpose port and I/O 362L is its enable signal. I/O NMI L is generated by the system whenever accesses to ports 0F0H (360Q), 0F1H (361Q), 0FAH (372Q), 0FBH (373Q) occur. Interrupt acknowledge is generated by the Z80 via a simultaneous M1 L and IORQ L. The BM1 L is used to deselect U550 and terminate the interrupt request. This enables the system to run software previously developed for the H-8 Computer. That is, accesses to the H-8 front panel are rerouted to the system console.

Since the interrupt acknowledge generates a BIORQ L signal, this could cause an I/O request to I/O 362 or I/O NMI. The effect would be to either cancel the interrupt before it could be processed or to generate an NMI request. In either case, the Computer will get lost. Therefore, since the interrupt acknowledge also generates an M1 signal, M1 is used to deselect U550 during the interrupt acknowledge cycle.

SINGLE STEP AND 2 mS CLOCK

The 2 mS clock is controlled by U506B. It is enabled by writing a "1" on data line D1 H at I/O port 0F2H (362Q). Once enabled, the next positive transition of the 2 mS clock will trigger U506B and cause its output (pin 8) to go low; thus enabling interrupt level 1. The clock handler must, as part of its routine, disable the clock interrupt (clear U506). Otherwise, another interrupt will be generated as soon as an EI instruction is executed. This occurs because U506B is operating as a latch. It will be cleared whenever a write to I/O port 0F2H (362Q) occurs. If D1 H is low when this write occurs, then the 2 mS clock will be disabled. If D1 H is high when the write occurs, then U506B will only be cleared and the 2 mS clock will still be enabled; thus allowing another interrupt to occur at the end of the next 2 mS period. At power-up or keyboard reset, U506B is enabled. Consequently, a 2 mS clock interrupt will occur immediately after an EI instruction has been executed.

The single step is enabled by D0 H and I/O port 0F2H (362Q). With bit 0 of port 0F2H (362Q) low, U555A and U555B are held in their initialized state. When bit 0 of port 0F2H (362Q) is high, the single step is enabled.

U556A synchronizes the 2.048 MHz clock with the M1 cycle and valid data on the data lines. U515B and U554 decode the EI instruction for U555A. Thus, an EI instruction causes the D input of U555A (pin 2) to be asserted low. U555A is then toggled by U556A: thus, setting the T input of U555B (pin 11) low. At the end of the next M1 cycle, U555B is toggled, which latches its output (pin 0) low. Another M1 cycle is executed, which now toggles U556's output (pin 8) high. This generates the interrupt at level 2 (restart 2). The software sequence is:

1. Enable single step
2. Wait for keyboard
3. EI instruction
4. RTI instruction
5. Execute single program instruction
6. Interrupt out of program
7. Disable single step
8. Enable single step (steps 7 and 8 are required to reinitialize single step logic)
9. Wait for keyboard
10. Etc.

GENERAL PURPOSE PORT

The general purpose port is located at I/O address 0F2H (362Q), and is comprised of U551, U552, U553B, and switch SW501. A read from this port puts the DIP switch (SW501) status on the data lines. A write to this port controls the single step and 2 mS interrupt logic. In addition, 4 other lines (MEM0 H, MEM1 H, IO0 H, and IO1 H) are available. These lines are routed to the accessory connectors on the CPU logic circuit board and are not presently used. BANK SEL H controls the selection of bank 7 on the 16K memory expansion board.

CONSOLE SERIAL PORT

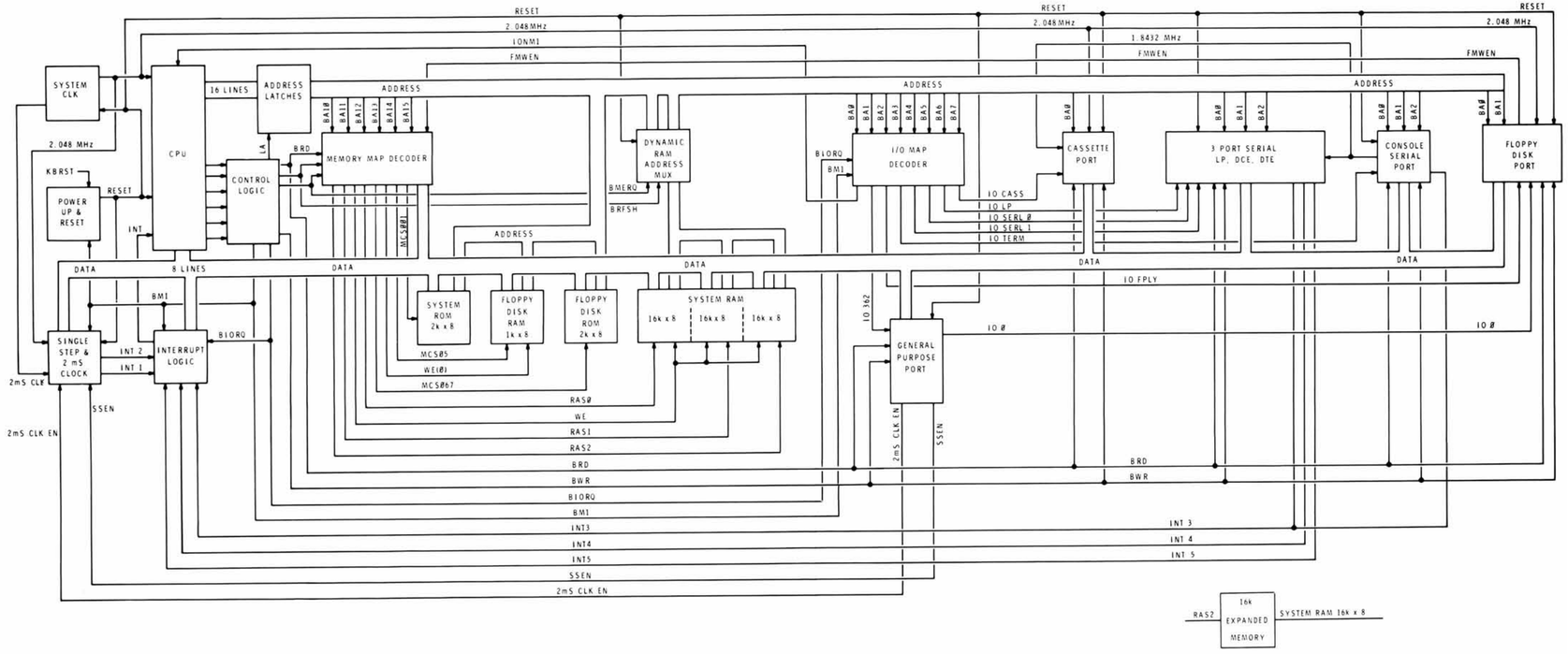
This port, at I/O locations 0E0H-0E7H (350Q-357Q), is used to communicate with the console terminal. U559 and U560 convert the TTL levels from and to the ACE (U561) into standard EIA signals. U515D acts only as an inverter for the reset line, and Q1 provides both inversion and the WIRED-OR function for interrupt level 3 (restart 3).

The clock for the ACE is supplied by logic inside U561, and is crystal controlled by X502. C525 and C526 provide the load for the crystal, and R515 and R516 provide the proper bias for the internal devices. The clock thus generated is routed to the I/O accessory connectors (through buffer U564D) for use by the Serial Interface Accessory circuit board.

SERIAL INTERFACE I/O CIRCUIT BOARD

The first port on this circuit board is located at I/O 0E0H-0E7H (340Q-347Q) and is used as the line printer port. Its output is standard EIA with a DCE connector. The second port is located at I/O 0D8H-0DFH (330Q-337Q) and, again, is used as the standard EIA output. However, this port is terminated with a DTE connector for communication with a MODEM. The third port is located at I/O 0D0H-0D7H (320Q-327Q) and is configured for EIA with a DCE connector. All three ports can be jumpered for interrupt levels, 3, 4, or 5 and use the 1.8432 MHz clock generated by the console serial port.

The main logic device for each port is the 8250 ACE.



CPU LOGIC AND SERIAL INTERFACE I/O BLOCK DIAGRAM

Service

QUICK CHECKS

- Check to see that the power cord is plugged into the receptacle, and the proper voltage is present.
- Check and verify that all switches and jumpers are in the correct positions for the equipment being used.
- With the Computer on, verify the presence of high voltage by checking the CRT filament.
- With the Computer in the OFF LINE mode, type some letters on the upper and lower portion of the screen to verify the proper character generation.
- Hard reset the Computer by depressing the right shift key and reset key simultaneously. This will cause the MTR prompt (H:) to appear in the upper left-hand corner of the screen.
- Verify the communication in and out of the ACE port on the terminal logic board by placing a jumper wire between pins 3 and 5 on J404 of the terminal logic board.
- Hard reset the Computer; the MTR prompt (H:) will appear.
- Check Dynamic RAM Test with MTR-90 by typing the letter (T).
- Check Dynamic RAM Test with MTR-89 by typing the letter (G) or (g). The Computer will respond with the word Go.
- Type 7375 followed by the RETURN key. The Computer will execute the Dynamic RAM Test which takes about ten minutes. If no failures are detected, the CPU, RAM memory, and the decoders are operational. If an error is detected, it will be printed on the screen. Refer to memory testing on Page 6-11.
- Hard reset the Computer. Insert a blank disk into the on-board drive.
- Check the disk rotational speed by typing the letter (G) or (g). The Computer will respond with Go. Then type 7372, followed by the RETURN key. The output on the CRT will be a number in Base 8 (octal) ranging from 177-201. The optimum reading should be at 200 (octal).

CRT ADJUSTMENT

This section contains several adjustments that you may need to make to properly maintain your Computer. You will have to remove or tilt back the cabinet top in order to reach the controls, coils, and adjustments called for in this section.

On the terminal logic circuit board set section 2 of switch S402 down to its 1 position. This enables the wraparound. See Figure 6-1.

NOTE: When power is turned on, do not touch the flyback transformer, the high voltage lead, or the anode socket at the back of the CRT, as it is possible to receive an electrical shock from these areas. Also, to lessen the chances of an electrical shock while you are making adjustments, keep your other hand away from this unit and all other metallic objects.

Plug in the line cord and set the POWER switch to ON.

After a short warm-up time, a light raster should appear on the screen. If it does not, adjust G1 control R262 counterclockwise (as viewed from the left side), to cause the raster to appear.

If the display is slanted, loosen the yoke clamp screw slightly and slowly turn the yoke to properly line up the raster on the screen. See Figure 6-2 on Page 6-3.

Adjust VERT SIZE control R219 (on the video circuit board) so the raster is approximately 6" high.

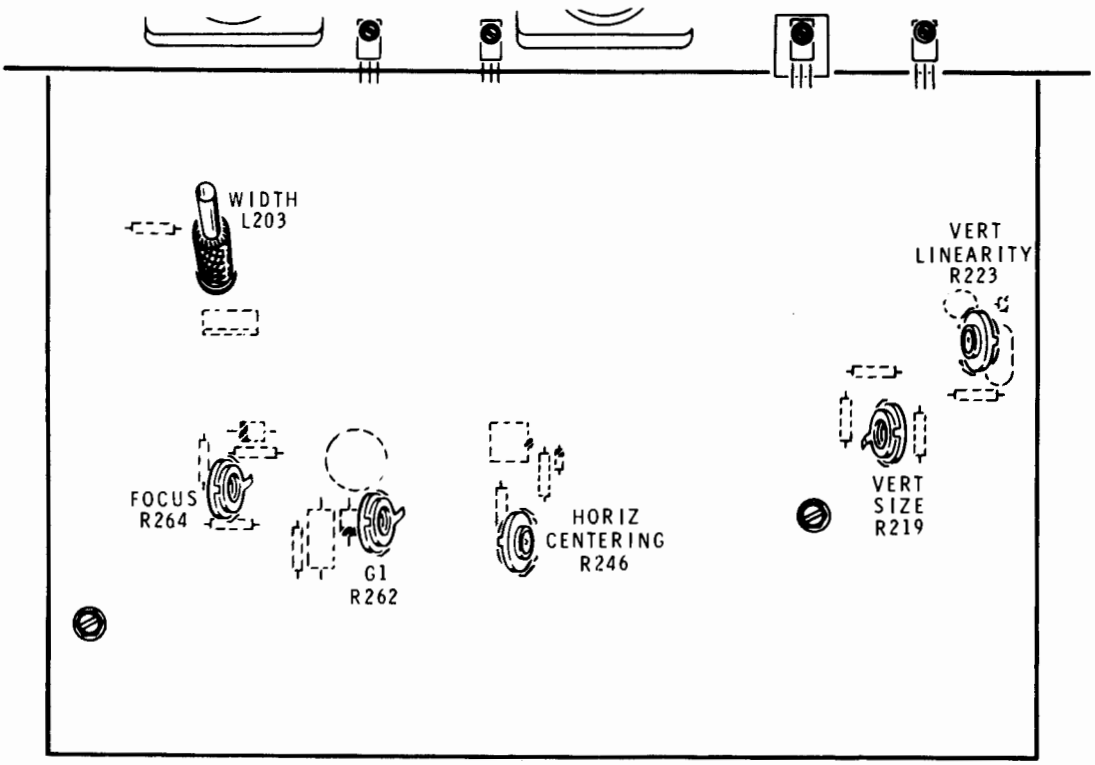


Figure 6-1
Video deflection circuit board.

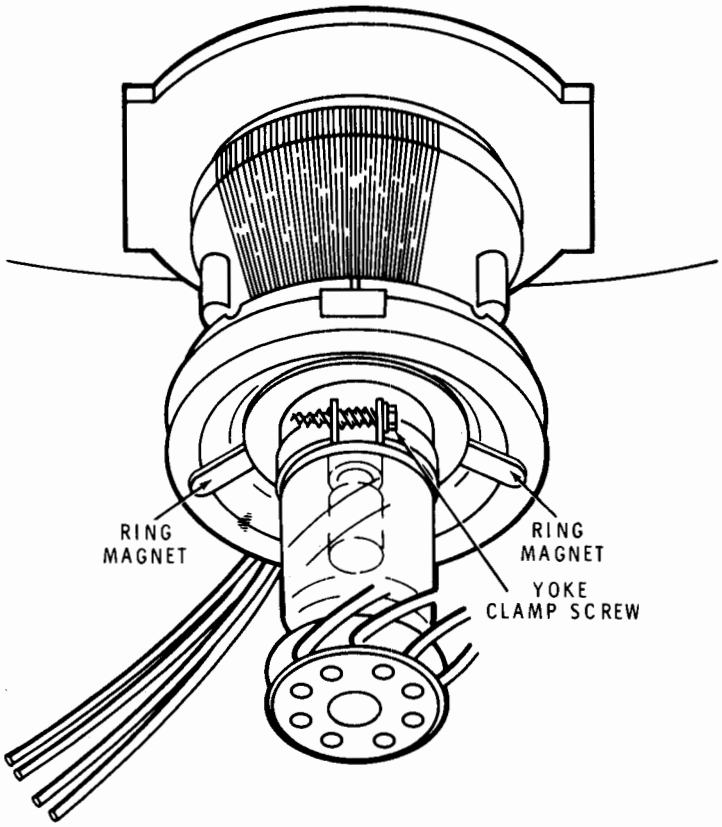


Figure 6-2
CRT-yoke.

Refer to Figure 6-2 and rotate the ring magnets on the back of the yoke to center the display on the screen.

Adjust rear panel BRIGHTNESS control R1 until a blinking cursor (underline) appears at the top corner of the screen.

Set the OFF LINE and CAPS LOCK keys to their down positions.

Hold the "Z" key and the REPEAT key down and fill the screen with characters.

Adjust HORIZ CENTERING control R246 to center the display horizontally within the raster.

Adjust VERT LINEARITY control R223 so that the top and bottom rows of characters are of uniform size.

NOTE: You should make the next adjustment in a darkened room.

Turn G1 control R262 clockwise (as viewed from the left) until the raster just disappears.

If the display width is not approximately 8-1/2", adjust WIDTH coil L203 to correct the width size.

Adjust BRIGHTNESS control R1 to obtain the brightness that is most suitable to you.

Adjust FOCUS control R264 for the best focus.

Recheck the display for proper alignment of the screen. If necessary, rotate the yoke a small amount. Then tighten the yoke clamp screw only enough to hold the yoke from turning.

Set the POWER switch to OFF and disconnect the line cord.

Set section 2 of switch S402 (on the terminal logic circuit board) up to its 0 position.

Resecure all parts in your Computer and replace the cabinet top.

SWITCH CONFIGURATIONS

Terminal Logic Board

For the switch locations refer to Figure 6-3.

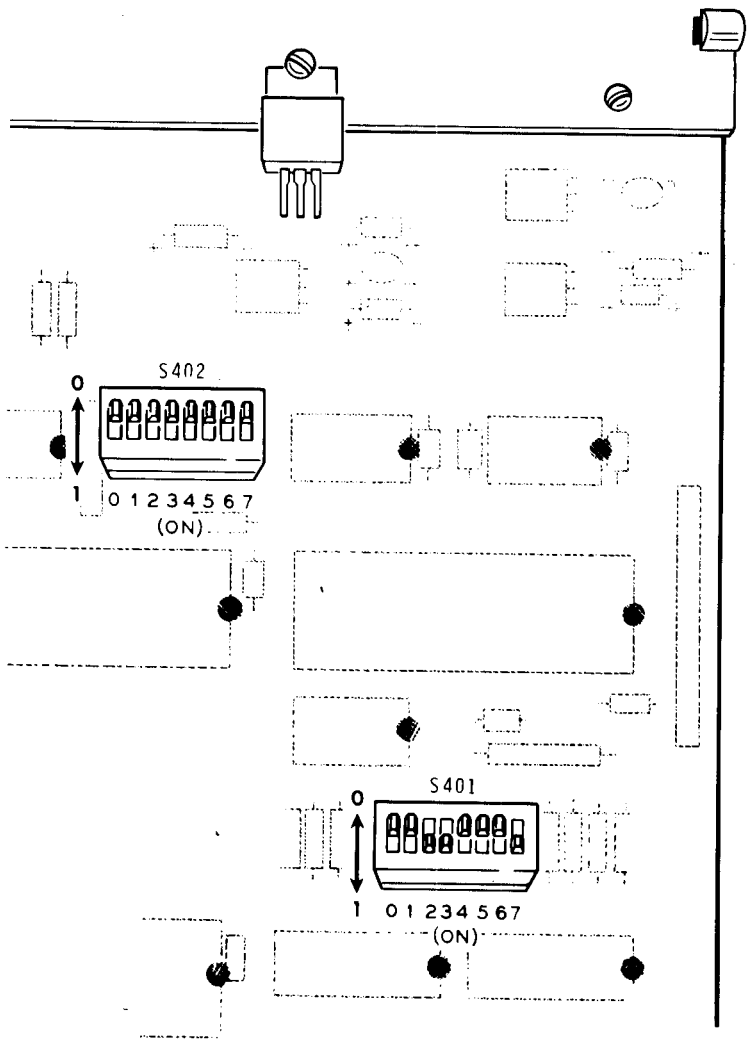


Figure 6-3
Terminal logic board.

SWITCH S402

SWITCH SECTION	DESCRIPTION
0	0 = underscore cursor; 1 = block cursor
1	0 = key click; 1 = no key click
2	0 = discard past end of line; 1 = wrap around
3	0 = no auto LF on CR; 1 = auto LF on CR
4	0 = no auto CR on LF; 1 = auto CR on LF
5	0 = ZDS mode; 1 = ANSI mode
6	0 = keypad normal; 1 = keypad shifted
7	0 = 60 Hz refresh; 1 = 50 Hz refresh

SWITCH S401

SWITCH SECTION	DESCRIPTION
0-3	Baud Rate
4	Parity Enable
5	Odd/Even Parity
6	Normal/Stick Parity
7	Half/Full Duplex

MODE	SWITCH SECTION 0	1	2	3	4	5	6	7
9600 Baud	0	0	1	1				
No Parity					0			
Odd Parity						0		
Normal Parity							0	
Full Duplex								1

BAUD RATE	SWITCH SECTION 0	1	2	3
N/A	0	0	0	0
110	1	0	0	0
150	0	1	0	0
300	1	1	0	0
600	0	0	1	0
1200	1	0	1	0
1800	0	1	1	0
2000	1	1	1	0
2400	0	0	0	1
3600	1	0	0	1
4800	0	1	0	1
7200	1	1	0	1
9600	0	0	1	1
19200*	1	0	1	1

*Not currently supported (may drop characters)

CPU LOGIC CIRCUIT BOARD

Switch SW501

The functions that switch SW501 selects are determined by integrated circuit U518. See Figure 6-4.

5-1/4" HARD-SECTORED FLOPPY USAGE

When you use a 5-1/4" hard-sectored floppy disk, integrated circuit part numbers HE 444-40, HE 444-62, or HE 444-84 must be installed at U518. Set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers." See Figure 6-4.

Set SW501 section 5 to "1."

Set the remaining seven SW501 sections to "0."

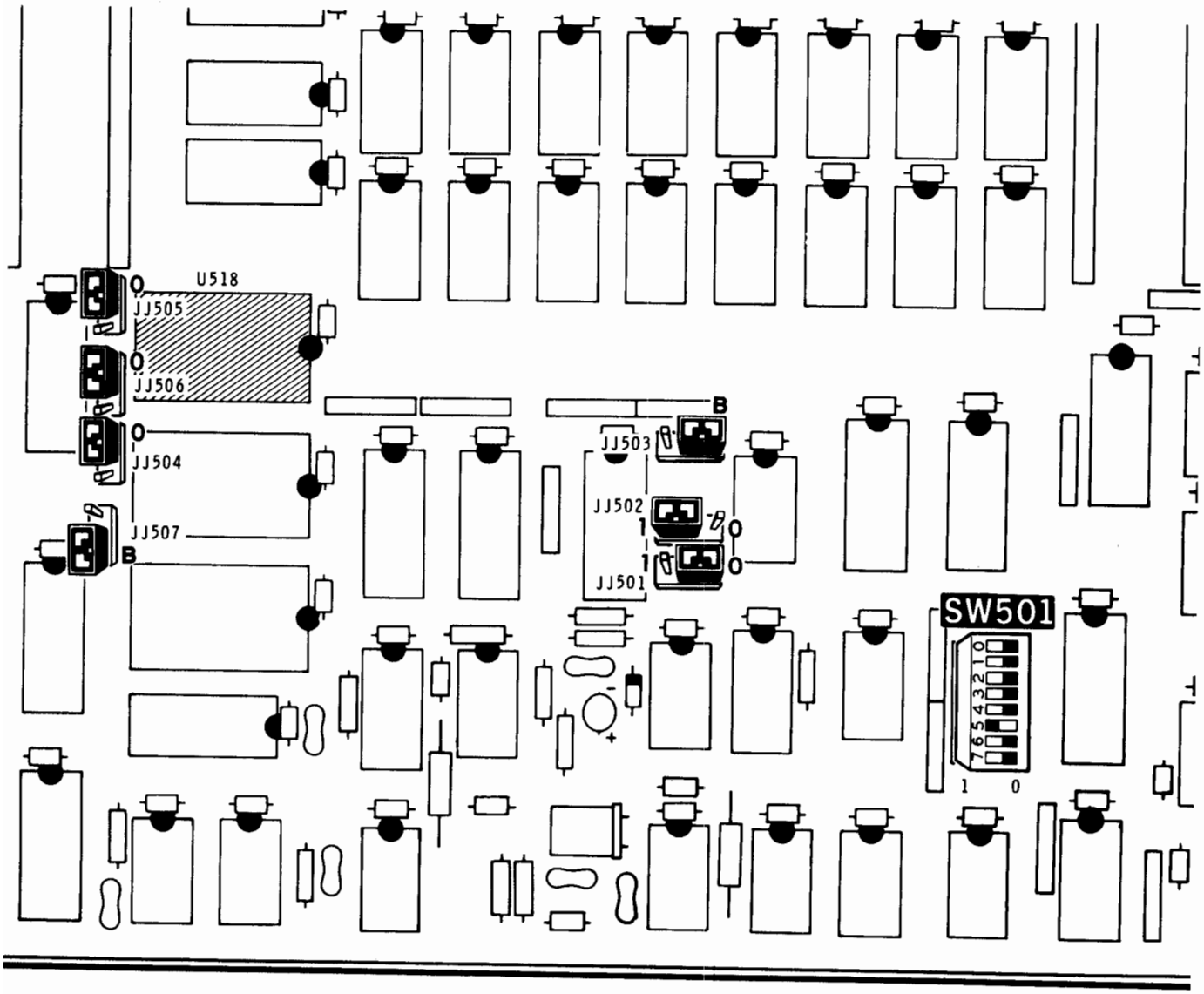


Figure 6-4
CPU board.

8″ FLOPPY DISK (Z-47) USAGE

When you use an 8″ floppy disk (Z-47), integrated circuit part numbers HE 444-62 or HE 444-84 must be installed at U518.

- When you boot up from a 5-1/4″ hard-sectored floppy disk to enable your 8″ floppy disk, set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers." See Figure 6-4.

Set SW501 switch sections 2 and 5 to "1."

Set the remaining six SW501 sections to "0."

- When you boot up from the left-hand 8″ floppy disk drive, set SW501 switch sections as directed in the next two steps. Then proceed directly to "Programming Jumpers."

Set SW501 switch sections 2, 4, and 5 to "1."

Set the remaining five SW501 switch sections to "0."

8″ FLOPPY DISK (Z-67) USAGE

There are four ways of installing the Interface Board. How you install yours depends on what equipment you already have. If you have:

1. A **Z-89-37 Double-Density Controller**, you must install your Interface Board as shown in Figure 6-5 on Page 6-8. Switch SW501 on the CPU Board must be set as shown in inset drawing #1. The jumpers on the Interface Board must be set as shown in inset drawing #2.

2. An **H-88-1 Disk Controller**, you must install your Z-89-67 Interface Board as shown in Figure 6-6 on Page 6-9. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

3. A **Z-89-47 Interface Board**, you must install your Z-89-67 Interface Board as shown in Figure 6-7 on Page 6-10. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

4. **None of the Above**, install your Interface Board as shown in Figure 6-8 on Page 6-11. Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

You may set the DIP switches on the Interface Board in any position when you are using Zenith software.

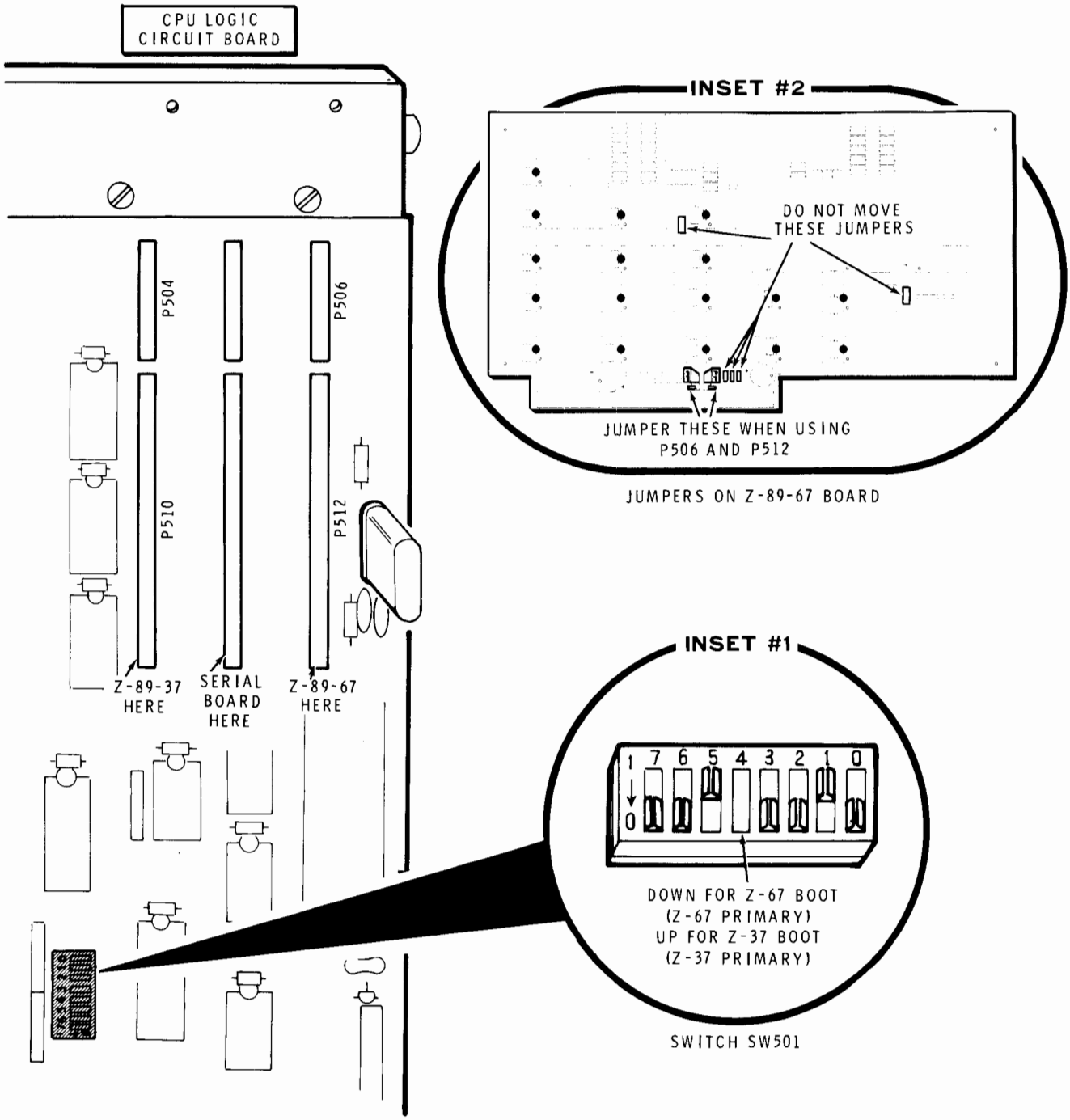

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-37
HERE
SERIAL
BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1
0
7 6 5 4 3 2 1 0
DOWN FOR Z-67 BOOT
(Z-67 PRIMARY)
UP FOR Z-37 BOOT
(Z-37 PRIMARY)
SWITCH SW501

Figure 6-5

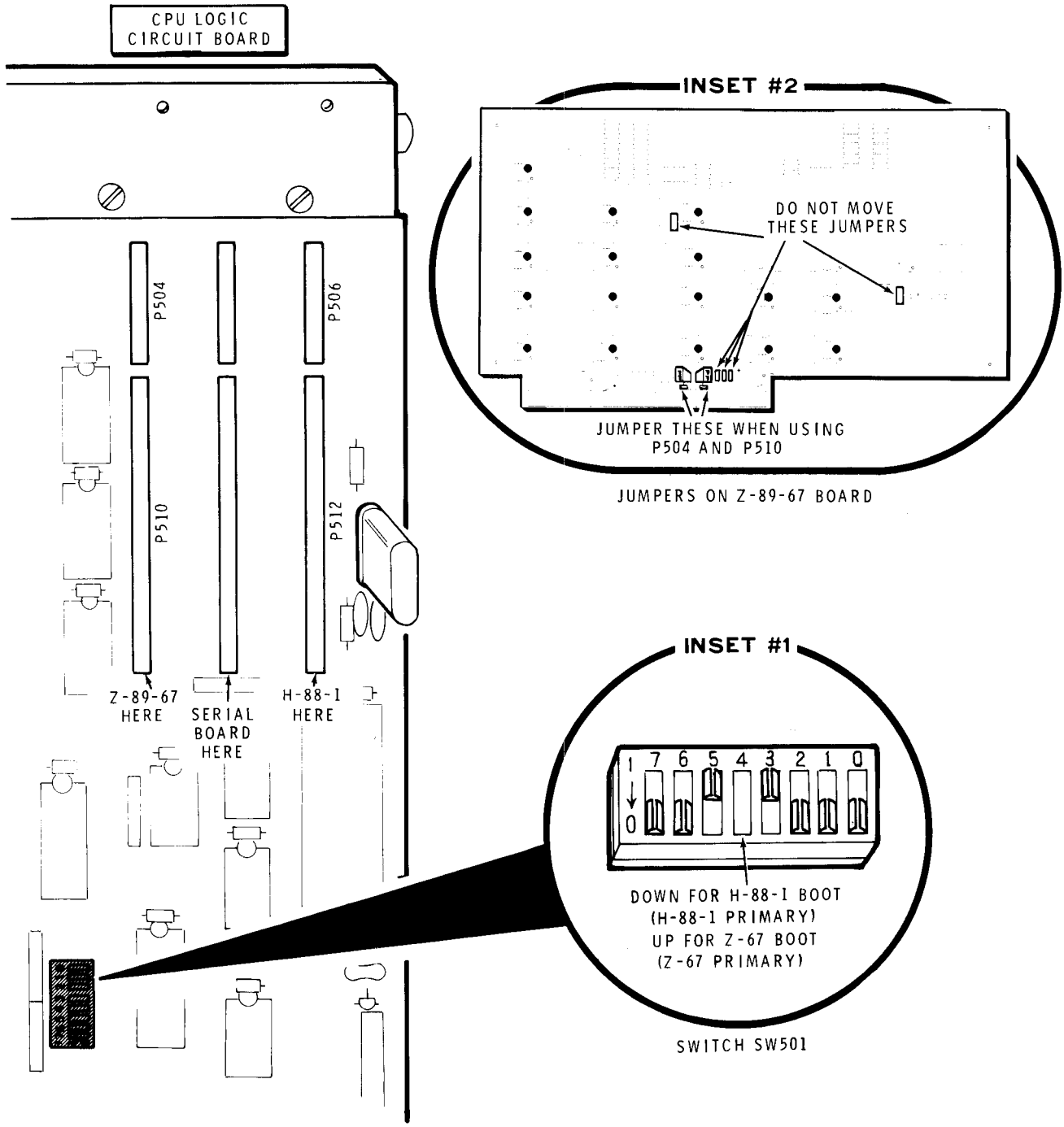

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-67
HERE
SERIAL
BOARD
HERE
H-88-1
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P504 AND P510
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
DOWN FOR H-88-1 BOOT
(H-88-1 PRIMARY)
UP FOR Z-67 BOOT
(Z-67 PRIMARY)
SWITCH SW501

Figure 6-6

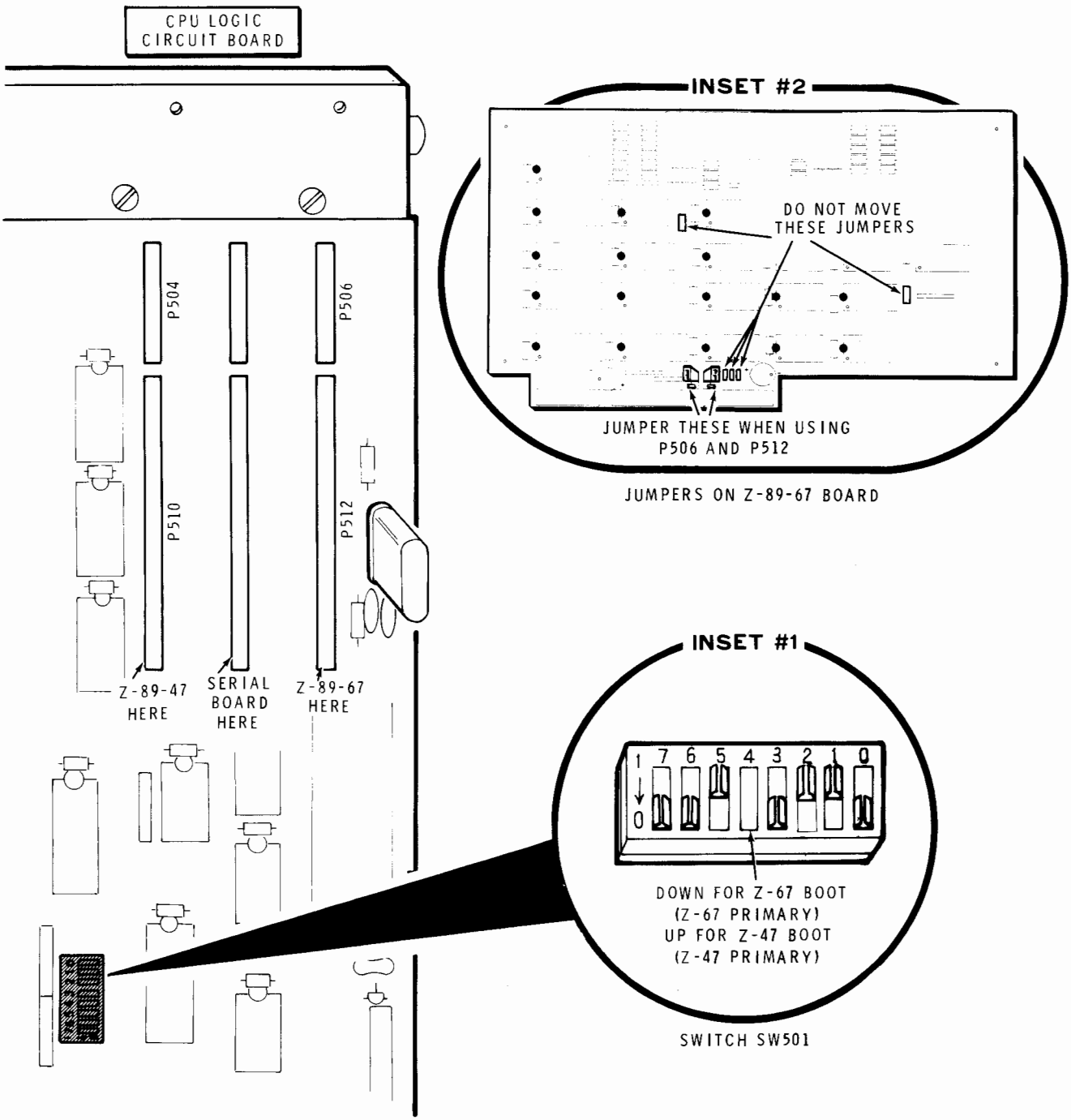

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
Z-89-47
HERE
SERIAL
BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
DOWN FOR Z-67 BOOT
(Z-67 PRIMARY)
UP FOR Z-47 BOOT
(Z-47 PRIMARY)
SWITCH SW501

Figure 6-7

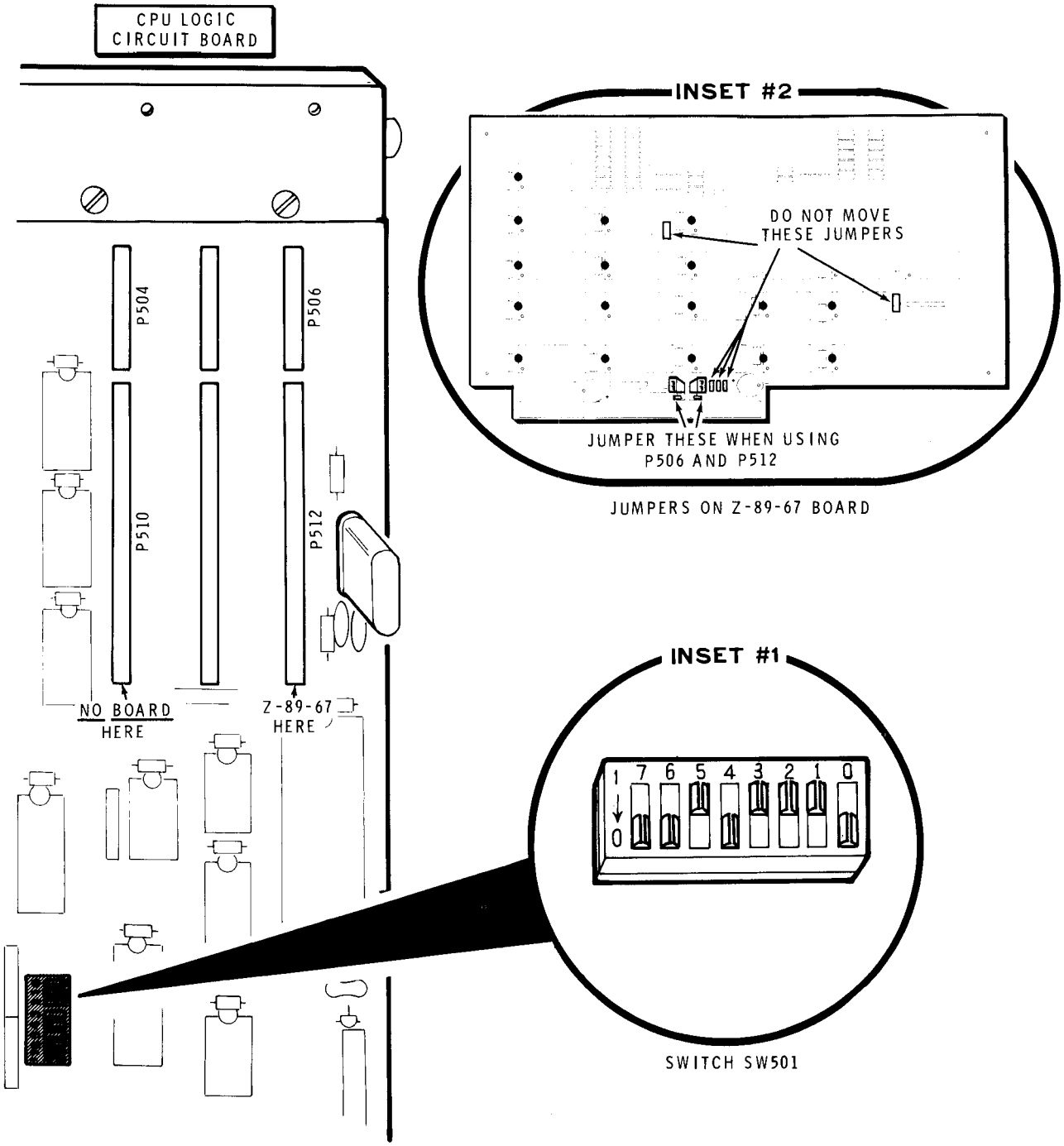

CPU LOGIC
CIRCUIT BOARD
P504
P506
P510
P512
NO BOARD
HERE
Z-89-67
HERE
INSET #2
DO NOT MOVE
THESE JUMPERS
JUMPER THESE WHEN USING
P506 AND P512
JUMPERS ON Z-89-67 BOARD
INSET #1
1 7 6 5 4 3 2 1 0
0
SWITCH SW501

Figure 6-8

Z-89-37 INTERFACE BOARD USAGE

Z-89-47

For a system to operate properly with the Z-89-37, the Z-89-47 I/O Board should be installed at plugs P506 and P512. However, before the Z-89-47 will operate properly when plugged into plugs P506 and P512, a resistor must be added to the Z-89-47 circuit board.

To make the modification, use a 4700 Ω, 1/4-watt resistor, HE 6-472 (yellow-violet-red), slide a length of sleeving over the resistor, and solder the resistor between pins 1 and 12 of plug P2 on the foil side (not the component side) of the Z-89-47 circuit board. Refer to Figure 6-9.

Set the 170/174 programming plug to 174.

Install the Z-89-47 board at plugs P506 and P512.

NOTE: If you ever move this board to another set of plugs, be sure to remove the 4700 Ω resistor that you just installed.

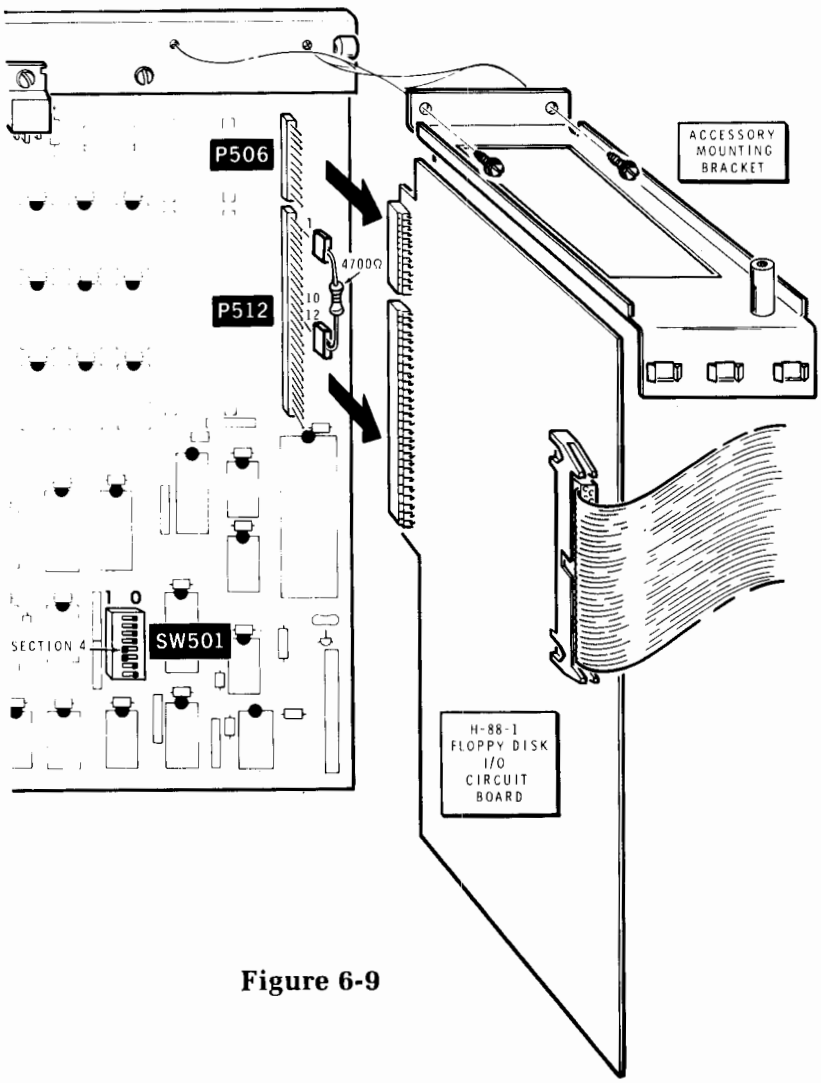


Figure 6-9

PROGRAMMING MODULES

Refer to Figure 6-10 on Page 6-14 as you read the following information.

Use the following information for any special configurations that you may want.

Programming modules:

J1 & J2 — Select port 170 or 174. (Both jumpers must be at 170, or both jumpers must be at 174. 170 is normal.)

J3 — 1 = No precompensation; 0 = precompensation. (1 position is normal.) Use "0" if any of your drives are 48 TPI Wangco Model 82 (HE 150-71) drives. Otherwise, use "1."

We recommend that you do not use both 48 and 96 TPI drives in the same system, since the precompensation will be wrong for at least one of the drives. This can result in reduced data reliability. When precompensation is selected, it is factory pre-set to 300 nanoseconds.

J4 — J7 — Selects which drive is connected to plug P3. (Drive numbers are determined by how the drive programming modules are cut. See Figure 6-10.)

J4 = DS1
J5 = DS2
J6 = DS3
J7 = DS4 (presently not supported)

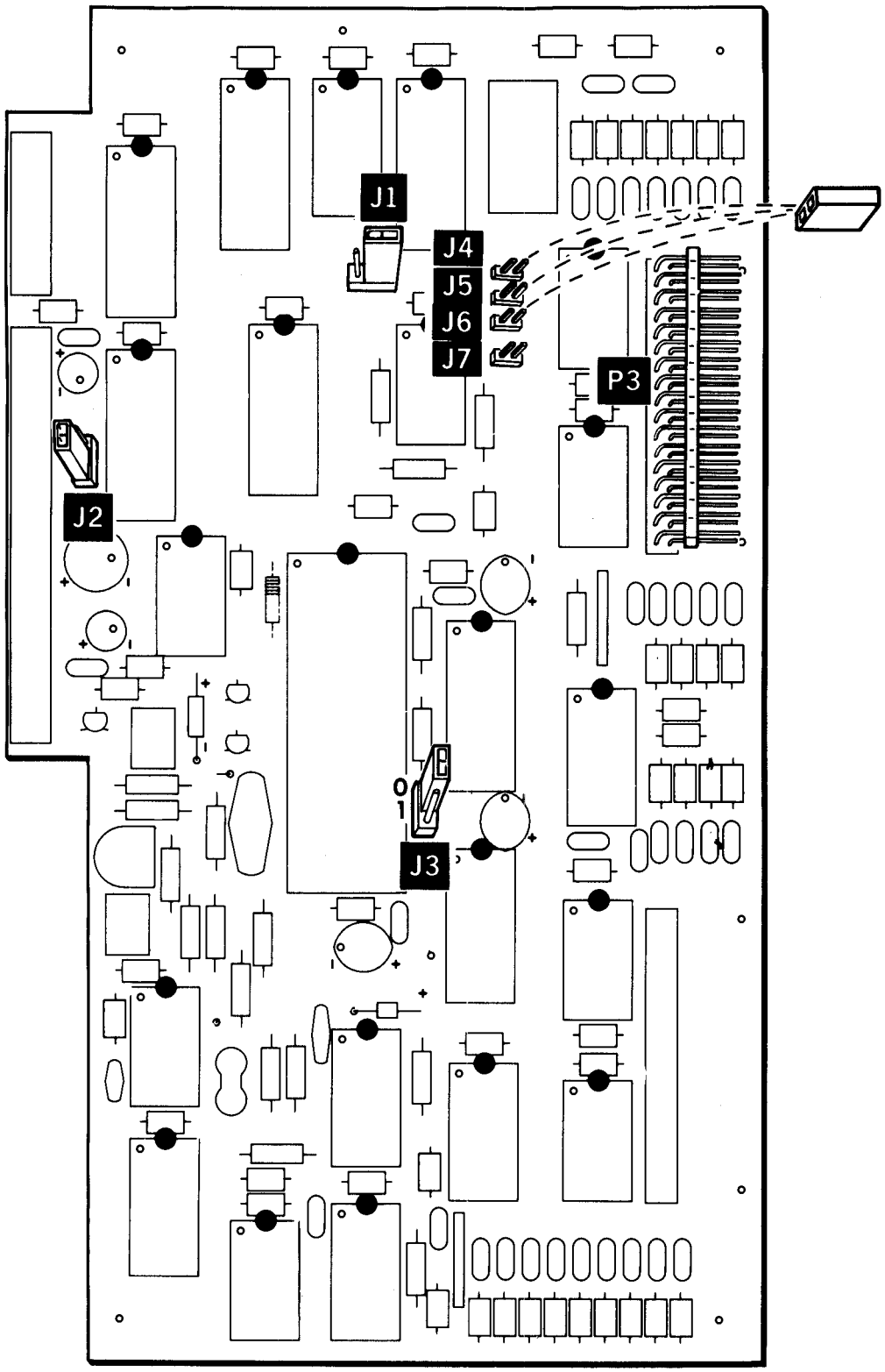


Figure 6-10

TO REARRANGE THE DRIVE NUMBERS . . . .

Refer to the following chart and Figure 6-11, and select the configuration that fits your situation. Configuration E is normally used for transferring data and programs from hard-sectored disks to soft-sectored disks.

After you select the configuration you want, refer to Figure 6-12 on Page 6-16 to program any 48 TPI (H-17-1) drives, or Figure 6-13 on Page 6-17 to program any 96 TPI drives. [Figure 6-14 on Page 6-18 shows single-sided drives (H-17-1) programmed for connection to an H-88-1 Controller.] You can do this programming by physically interchanging the programming modules, cutting the programming modules (if presently uncut); or by replacing the programming module with a properly set dip switch.

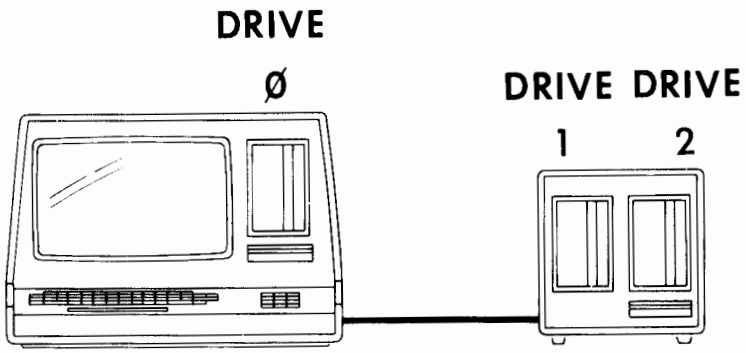


Figure 6-11

FLOPPY DISK CONTROLLER BOARD(S)		TYPES OF DRIVES: • 48 TPI (H-17-1) • 96 TPI (H-17-4)	Drive 0	Drive 1	Drive 2
A	H-88-1	48 TPI (H-17-1) only. Internal drive present	DS3	DS2	DS1
B	H-88-1	48 TPI (H-17-1) Internal drive absent	No drive installed	DS3	DS2
C	Z-89-37	Either* Internal drive present	DS1 (Z-89-37 jumper installed at J4)	DS2	DS3
D	Z-89-37	Either* Internal drive absent	No drive installed (Z-89-37 jumper installed at J7)	DS1	DS2
E	H-88-1 & Z-89-37	Either* Internal drive present	DS3 [Drive 0 is 48 TPI (H-17-1) drive connected to H-88-1. Z-89-37 jumper installed at J6.]	DS1 (Drive 0 connected to Z-89-37)	DS2 (Drive connected Z-89-37)

* All drives connected to the Z-89-37 should be of the same type, either 48 TPI (H-17-1) or 96 TPI (H-17-4).

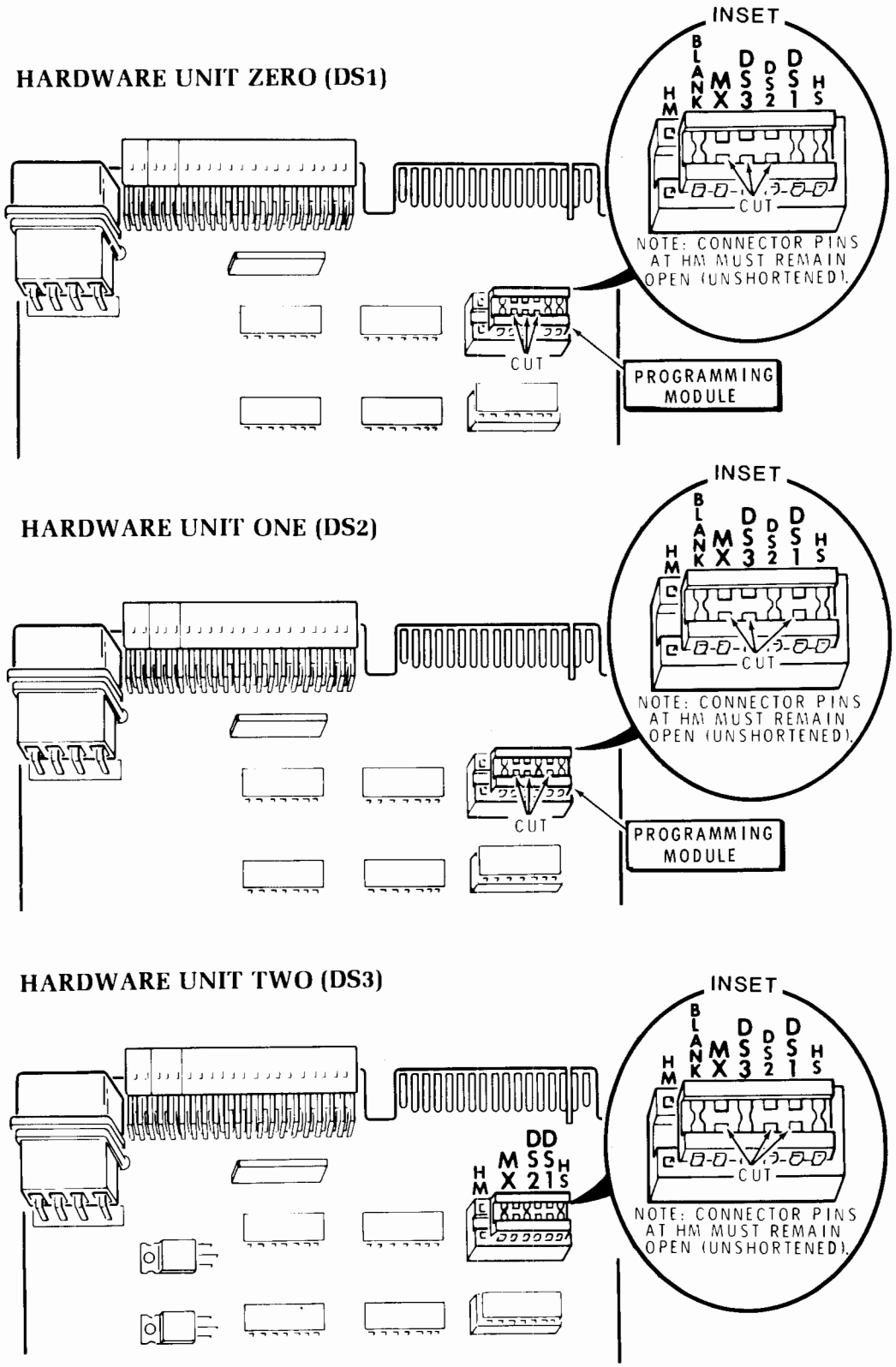
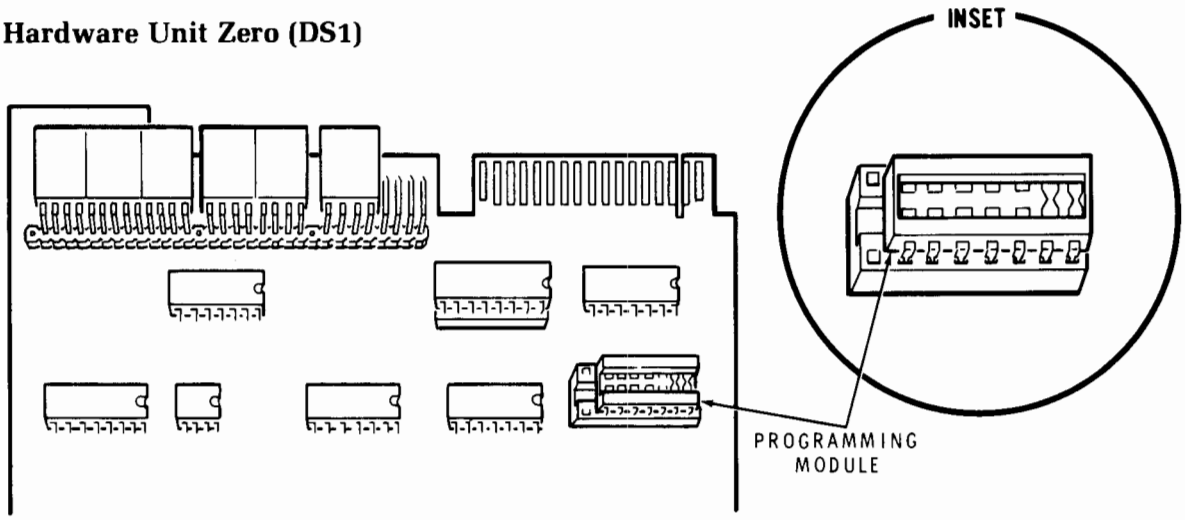


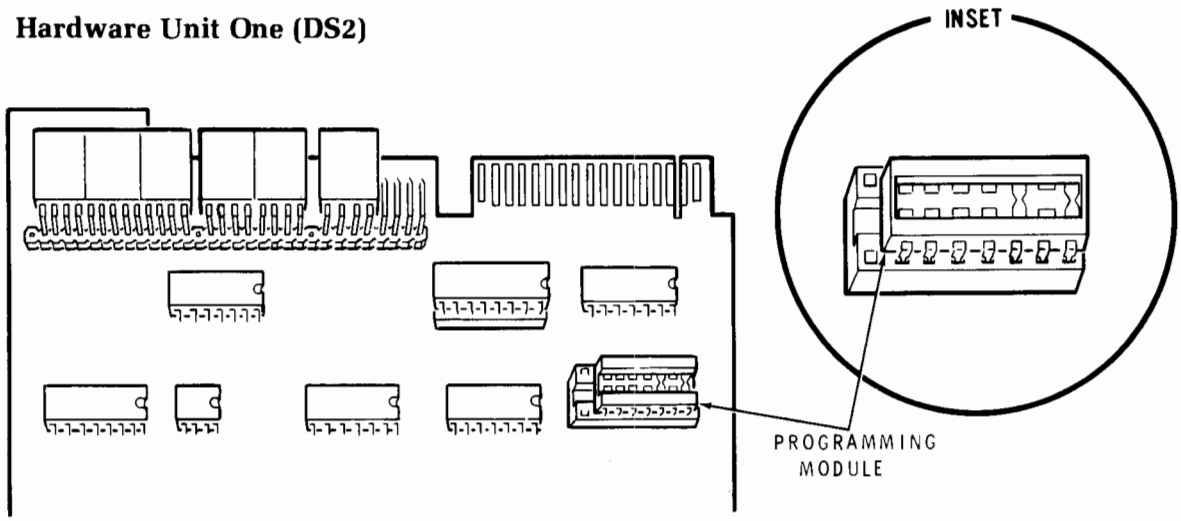
Figure 6-12

Single-sided drives (H-17-1) programmed for Z-89-37 Controller.

Hardware Unit Zero (DS1)



Hardware Unit One (DS2)



Hardware Unit Two (DS3)

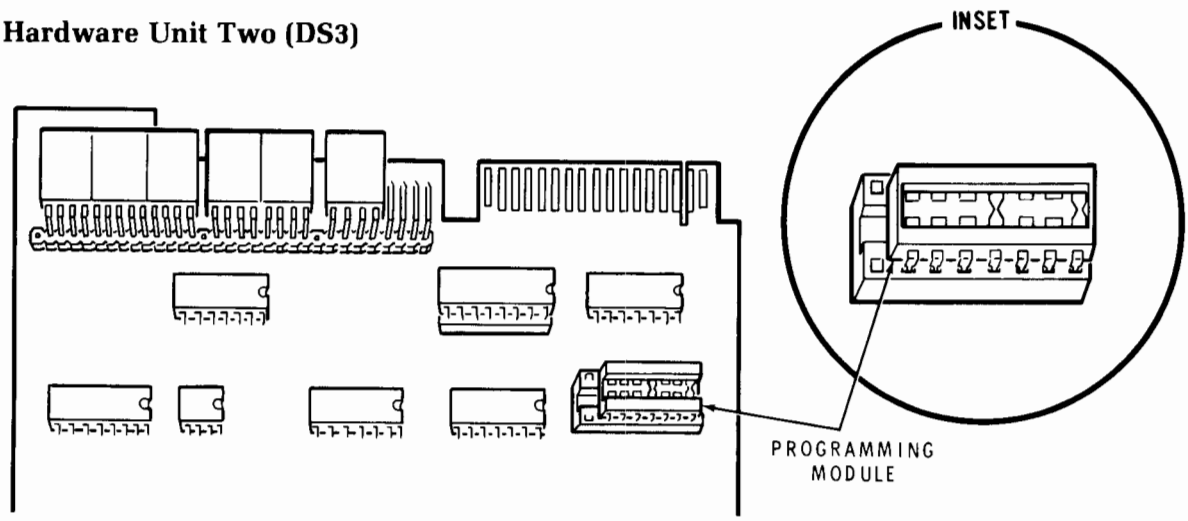
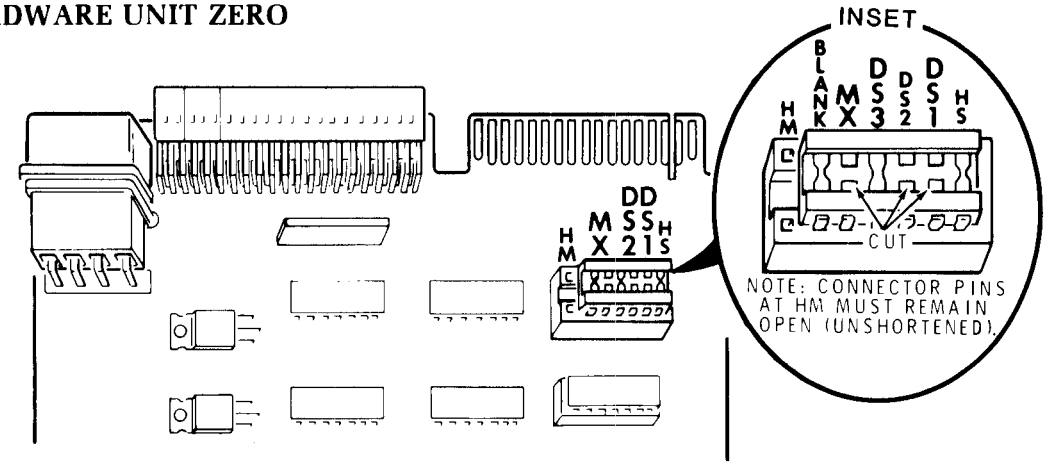


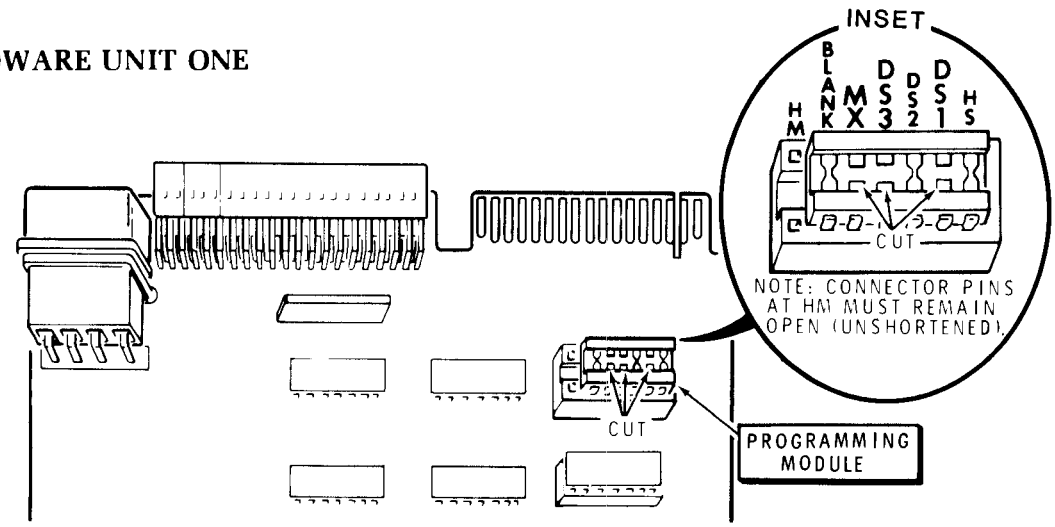
Figure 6-13

Double-sided drives (H-17-4) programmed for Z-89-37 Controller.

HARDWARE UNIT ZERO



HARDWARE UNIT ONE



HARDWARE UNIT TWO

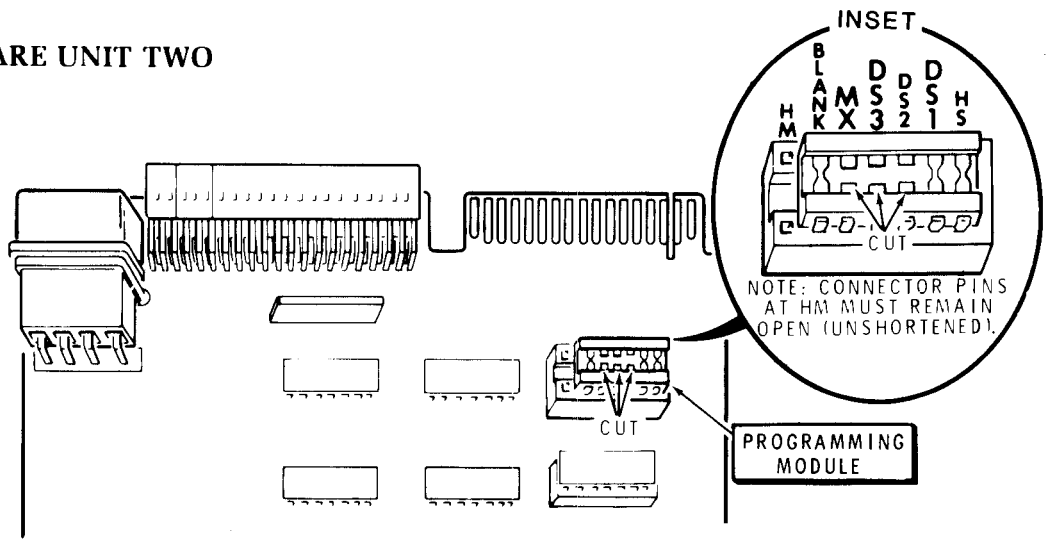


Figure 6-14

Single-sided drives (H-17-1) programmed for H-88-1 Controller.

Definitions of SW501 with MTR-89 (HE 444-62)

When IC part number HE 444-62 is installed at U518, the following table describes the functions of each SW501 switch section.

SWITCH SECTIONS	SETTING*	DESCRIPTION
1 and 0	00	Port 174/177Q (7CH-7FH) has a 5-1/4" hard-sectored floppy disk (normal).
	01	Port 174/177Q has a Z-47, 8" floppy disk.
	10	Undefined.
	11	Undefined.
3 and 2	00	Port 170/173Q (78H-7BH) is not in use (normal with Z-47, 8" floppy disk).
	01	Port 170/173Q has a 8" floppy disk (normal with Z-47).
	10	Undefined.
	11	Undefined.
4	0	Boots from device at port 174/177Q (7CH-7FH) (5-1/4" hard-sectored floppy disk).
	1	Boots from device at port 170/173Q (78H-7BH) (Z-47, 8" floppy disk)
5	0	Performs memory test upon power-up or SHIFT-RESET.
	1	Does not perform memory test (normal).
6	0	Sets console to 9600 baud (normal).
	1	Sets console to 19200 baud (not currently supported).
7	0	Normal boot (normal).
	1	Auto boot on power-up or SHIFT-RESET (not recommended).

* Right-hand value is for switch section 0 or 2, depending on respective Switch Section column.

Definition of SW501 with MTR-90 (HE 444-84)

When IC part number HE 444-84 is installed at U518, set the sections of SW501 as described in "Definition of SW501 with MTR-89," except for sections 0, 1, 2, and 3, which are defined as follows:

SWITCH SECTIONS	SETTING*	DESCRIPTION
1 and 0	00	Port 174/177Q (7CH-7FH) is 5-1/4" hard-sectored floppy disk.
	01	Port 174/177Q is Z-47, 8" floppy disk.
	10	Port 174/177Q is Z-67, 8" hard disk.
	11	Undefined.
3 and 2	00	Port 170/173Q (78H-7BH) is Z-37 soft-sectored disk.
	01	Port 170/173Q is Z-47, 8" floppy disk.
	10	Port 170/173Q is Z-67, 8" hard disk.
	11	Undefined.

Memory Decode ROM

The memory decode ROM is located at U517 on the CPU board. Two ROMs have been used. Part number HE 444-42 was originally used. This ROM precluded the use of more than 48K of memory or CP/M. It has been superseded in all production units by HE 444-66, which allows the ROM based 48K mode, the ROM based 56K mode, and an all RAM 64K mode. **All** users should upgrade to this part regardless of configuration. There are **no** negative consequences connected with this upgrade.

Associated with this ROM are three or four jumpers, JJ501 thru JJ504. Older CPU boards have all four jumpers; they should be set as follows:

When using the Old ROM (HE 444-42)

	JJ501	JJ502	JJ503	JJ504
16K	0	0	0	0 (or B)
32K	1	0	0	0 (or B)
48K	0	1	0	0 (or B)

When using the New ROM (HE 444-66)

	JJ501	JJ502	JJ503	JJ504
16K	0	0	**	0 (or B)
32K	1	0	**	0 (or B)
48K	0	1	**	0 (or B)
64K*	1	1	**	0 (or B)

Newer CPU boards (which only have three jumpers, JJ501 through JJ503) are supplied with the new decode ROM (HE 444-66) already installed and the jumper wire incorporated directly into the PC board foil. These boards should not be used with the old ROM (HE 444-42). These jumpers should be set as follows:

	JJ501	JJ502	JJ503
16K	0	0	0 (or B)
32K	1	0	0 (or B)
48K	0	1	0 (or B)
64K*	1	1	0 (or B)

These are four jumper wires associated with the code ROM and the secondary address decoder. These are either JJ505, JJ506, JJ507 and JJ508 (on older units) or JJ504, JJ505, JJ506 and JJ507 (on newer units). These should be set as follows:

Older Units: Newer Units:	JJ505 JJ504	JJ506 JJ505	JJ507 JJ506	JJ508 JJ507
MTR-88, MTR-89	0	0	0	1 (or B)
MTR-90	1	*	1	1 (or B)

* Requires the WH-88-16 accessory PC board.

** A jumper is required between the center pin of JJ503 and pin 17 of P509, or P4 of WH-88-16 (which connects to pin 17 of P509). This jumper may have been soldered on the back of the CPU board during manufacture (for Z-89-FA and some other models), or it may be ordered as part number HE 131-1120 and installed by the user. Neither tools nor soldering are required.

ROTATIONAL SPEED TEST

This test will check the rotational speed of the floppy disk drive for the Z-89 and Z-90 Computers. After the test starts, it will display the disk drive speed test message and a "speed equals" message as follows:

Disk drive rotational speed test

Drive speed =

The word "Working" will be flashed on and off at the home position and a drive speed number (in octal), which should be as close to 200 as possible, will update with each flash on the screen. The rotational speed tolerance is one percent. The displayed value should be between 166 and 212 (remember, octal numbers jump from 177 to 200). Do not adjust the speed unless it is out of tolerance.

Your drive unit has a control labeled R30 or R7 which is used to vary the drive speed. The location for this control for various drives is shown in Figure 6-15.

This adjustment may be extremely sensitive so if an adjustment is necessary, do not turn it far in either direction. Less than one degree of rotation in either direction should bring the drive speed into tolerance. Turn the control clockwise to decrease the speed or counterclockwise to increase it.

As the drive bearings wear, the speed may change slightly. Fluctuations within the tolerance are normal and may be attributed to variations in temperature and humidity.

To begin the test, be sure the OFF LINE key is up (out). Then obtain the "H:" prompt. (Simultaneously push the right-hand SHIFT and RESET keys if necessary.)

Type G7372CR. The total entry will be:

H: **Go 7372CR**

and the test will start.

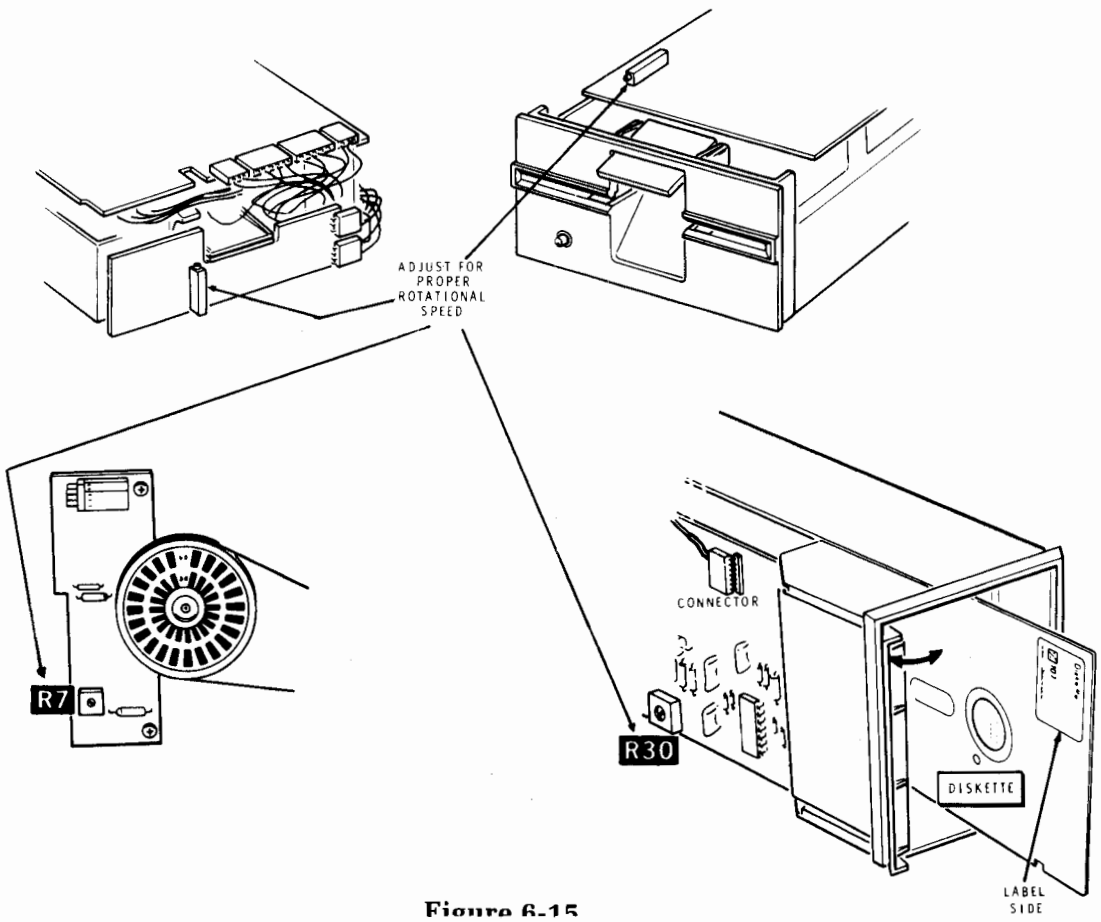


Figure 6-15

MEMORY TESTING

It is usually easier to test and locate a bad memory IC using diagnostic programs rather than with test equipment. The system monitor has a built-in memory test you can use to locate a faulty bit. This memory test is for the Z-89 and Z-90 Computers.

The memory test uses the Z80 registers as its scratch pad and will check all user memory from 040000A on up to the top end of the supplied memory. You can start it either by setting section 5 of SW501 to its zero position and resetting the Computer, or by entering:

H: Go 7375 CR

The Computer will then load 000Q into each byte of memory, go back and compare each location to zero, increment each location until it again reaches the end of memory, and then repeat the operation. It will do this until every bit pattern from 000Q to 377Q has been tested in every memory location. It will then go back to zero and start over.

Due to the way the program is written, the first value to be displayed is as shown below (48K system):

Dynamic RAM test
LWA = 337377
Pass = 002

Depending on the amount of RAM installed, the last working address (LWA) will normally indicate one of the following three numbers:

Amount of RAM Installed	LWA (Offset Octal)	LWA (Decimal)
16K	137377	24575 (24K-1)
32K	237377	40959 (40K-1)
48K	337377	57343 (56K-1)

The *Pass* number indicates the data byte that the program is checking for. If the location being checked were not this value, then an error message similar to the following would occur:

Dynamic RAM test
LWA = 337377
Pass = 002
Error @ 040100 = 006

And the speaker will continuously beep. This indicates that the program expected to see a binary 00000010 at address 040100A, but got a binary 00000110 instead. In other words, data bit D_2 is stuck to a logic one.

You can determine which IC has failed by converting the Pass Number and Error Number from their octal form to binary form. Then locate the mismatch in the numbers as in the following example.

Dynamic RAM test
LWA = 337377
Pass = 002
Error = 006

$D_7D_6D_5D_4D_3D_2D_1D_0$
002 octal = 0 0 0 0 0 0 1 0 binary
006 octal = 0 0 0 0 0 1 1 0 binary

Data bit D_2 is a mismatch. In this case the defective IC is in the top row (48K = top row, 32K = middle row, 16K = bottom row). Since LWA = 337377 is greater than 32K, its location is in the top row. D_2 is the defective IC, so the third IC in the top row is defective.

You can use the table below to cross-reference the address and faulty bit location to the IC causing the failure.

Since the faulty bit was D_2 at address 040100A, then U544 should be replaced. (Refer to the table below.)

Note that the dynamic RAMs are laid out on the CPU board as shown in the table. Once you become familiar with this test, you should be able to locate most memory data failures without having to refer to the Schematic.

MTR-89

48K LWA = 337.377	U549	U548	U547	U546	U545	U544	U543	U542
32K LWA = 237.377	U541	U540	U539	U538	U537	U536	U535	U534
16K LWA = 137.377	U533	U532	U531	U530	U529	U528	U527	U526
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MTR-90 with 16K expansion

64K LWA = 337.377	U5	U6	U4	U7	U3	U8	U2	U9
48K LWA = 337.377		U548	U547	U546	U545	U544	U543	U542
32K LWA = 237.377	U541	U540	U539	U538	U537	U536	U535	U534
16K LWA = 137.377	U533	U532	U531	U530	U529	U528	U527	U526
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

TROUBLESHOOTING CHARTS

The following charts list conditions and possible causes of several specific malfunctions. If a particular part is mentioned (F1 or example) as a possible cause, check that part and other components connected to that part to see that they are in good working order.

WARNING: Measure the anode voltage only with an approved high voltage probe.

CAUTION: Never operate the Computer unless the short black ground wire coming from the corner of the video board is connected to the CRT ground.

POWER SUPPLY PROBLEMS

CONDITION	POSSIBLE CAUSE
Nothing happens at turn on.	1. Not plugged in. 2. Fuse F1 blown. 3. Switch SW1 wiring. 4. Fuseholder wiring. 5. Capacitor C1.
Fuse blows.	1. Check primary wiring. 2. Short circuit on power supply circuit board. 3. Short circuit across transformer secondary. 4. Diodes D101-D112, and BR1. 5. Capacitors C1, C102-C104. 6. IC's U401-U405. 7. Short between collector of transistor Q204 and video board heat sink. 8. Incorrect fuse. 9. Power transformer T1.
No output from 5 V supplies, or voltage(s) too high or too low.	1. IC's U401, U402. 2. Diodes D105-D107. 3. Capacitor C103.
No +12 V, or is too high or too low.	1. IC U403. 2. Diodes D101-D104. 3. Capacitor C102.
No −12 V, or is too high or too low.	1. IC U404. 2. Diodes D101-D104. 3. Capacitor C104.
No −5 V, or is too high or too low.	1. IC U405. 2. IC U404 (−12 V source supplies −5 V regulator). 3. Diodes D101-D104. 4. Capacitor C104.
No +53 V, or is too high or too low.	1. Transistors Q201, Q202, Q204. 2. Diodes D201, D202.
No unregulated voltages (+65, +8.5, +/−16) on power supply board.	1. Check appropriate secondary of T1, diode bridges or filter capacitor.
No anode voltage when other voltages are OK.	1. No sync pulses coming from terminal logic board. 2. Transistors Q213, Q214. 3. Deflection yoke. 4. Coils L203, L204. 5. Capacitors C228, C232. 6. Diode D208. 7. IC's U201, U202.
+500 V supply is too high or too low.	1. Diode D211. 2. Capacitor C231.
−90 V supply is too high or too low.	1. Diode D207. 2. Resistor R259. 3. Capacitor C229.
−6 V supply is too high or too low.	1. Diode D203. 2. Resistor R212.

DISPLAY PROBLEMS

CONDITION	POSSIBLE CAUSE
No video (blank screen).	1. Brightness control (R1) turned down. 2. Anode voltage incorrect. 3. Grid voltages incorrect (G1, G2, G4). 4. No cathode drive. 5. Transistors Q901, Q902. 6. No video signal coming from terminal logic board. 7. IC U406. 8. Video circuits on logic board. 9. Diode D901. 10. No sync pulses coming from logic board. 11. Diode D209.
Screen all white (raster).	1. Grid voltages. 2. Transistors Q901, Q902. 3. Video circuits on terminal logic board. 4. Anode voltage incorrect.
Insufficient brightness.	1. Transistors Q901, Q902. 2. Diode D902. 3. Capacitors C901-C905. 4. Brightness control, R1, Resistors R901-R904, R214, R218, R219, R217. 5. Grid voltages.
One bright horizontal line on screen.	1. Vertical amplifier transistors Q207-Q212. 2. Diode D205. 3. Deflection yoke (vertical). 4. Vertical sweep generator transistors Q205, Q206. 5. Diode D204. 6. No vertical sync pulses coming from logic board. 7. IC U406.
Too much or too little height.	1. Vertical amplifier or sweep generator. 2. Capacitor C213. 3. Resistor R242. 4. Vertical size control R219. 5. Capacitor C211.
Too much or too little width.	1. Adjust width coil L203. 2. Capacitors C228, C232. 3. Deflection yoke (horizontal). 4. Coils L203, L204. 5. +53 V supply not correct. 6. Flyback transformer T202. 7. Transistor Q214.

Display Problems (Cont'd.)

CONDITION	POSSIBLE CAUSE
Picture tube filament does not glow.	1. No horizontal sync pulse coming from logic board. 2. Filament winding of T202 (brown wires). 3. Resistor R257.
Horizontal centering does not work.	1. IC U201. 2. Horizontal centering control R246. 3. Capacitor C221.
No horizontal sweep, but sync pulses are present at P202-1.	1. Diode D206. 2. IC's U201, U202. 3. Transistors Q213, Q214. 4. Transformer T201. 5. +6 V supply not correct. 6. Capacitor C226. 7. Diode D208. 8. +53 V supply not correct. 9. Deflection yoke. 10. Coils L203, L204.

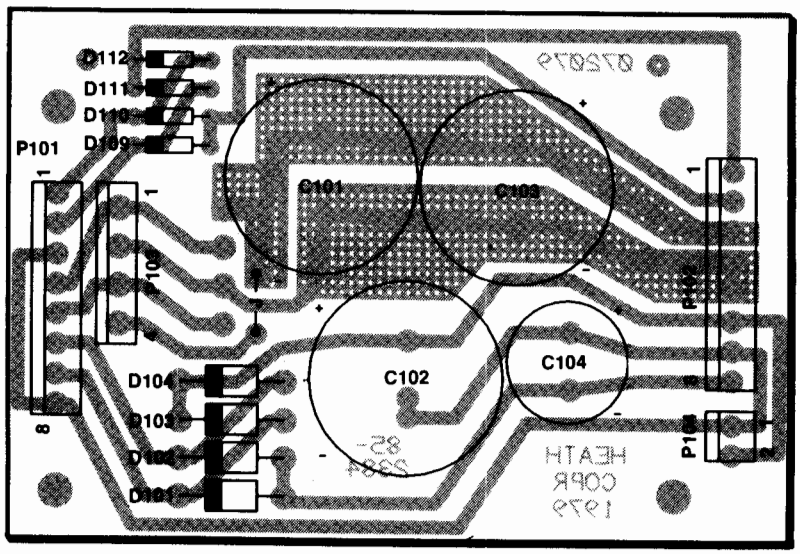
Circuit Board X-Ray Views

NOTE: To find the PART NUMBER of a component for the purpose of ordering a replacement part:

A. Find the circuit component number (R5, C3, etc.) on the "X-Ray View."

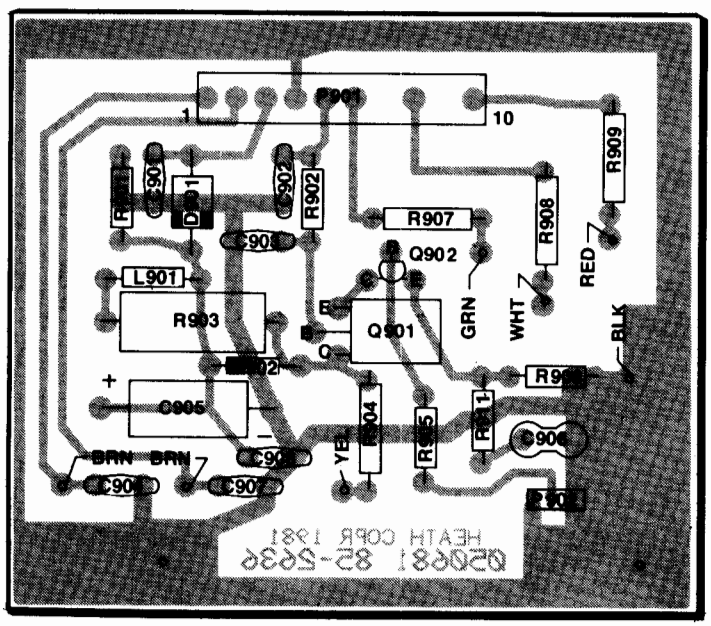
B. Locate this same number in the "Circuit Component Number" column of the "Replacement Parts List."

C. Adjacent to the circuit component number, you will find the ZDS PART NUMBER and DESCRIPTION which must be supplied when you order a replacement part.



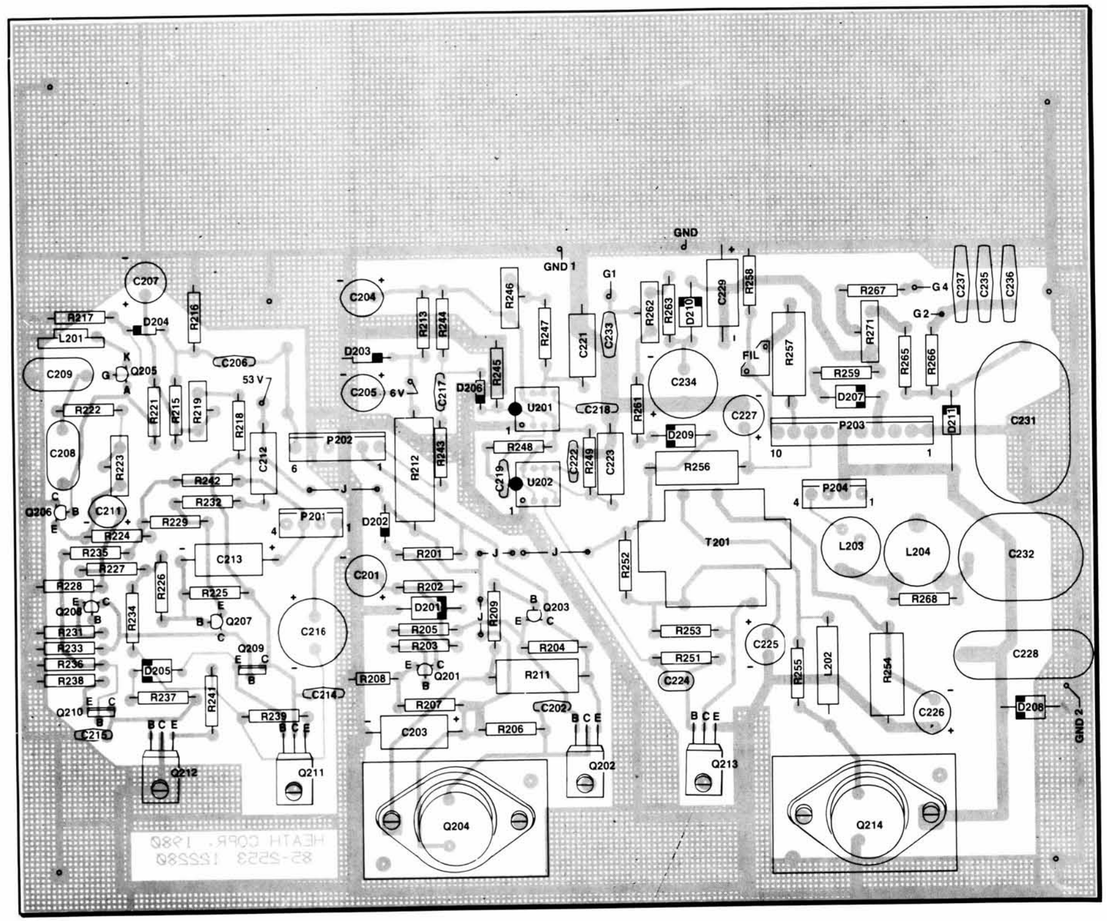
Z-89 AND Z-90 POWER SUPPLY CIRCUIT BOARD

Part number HE 181-3244. Shown from the component side.



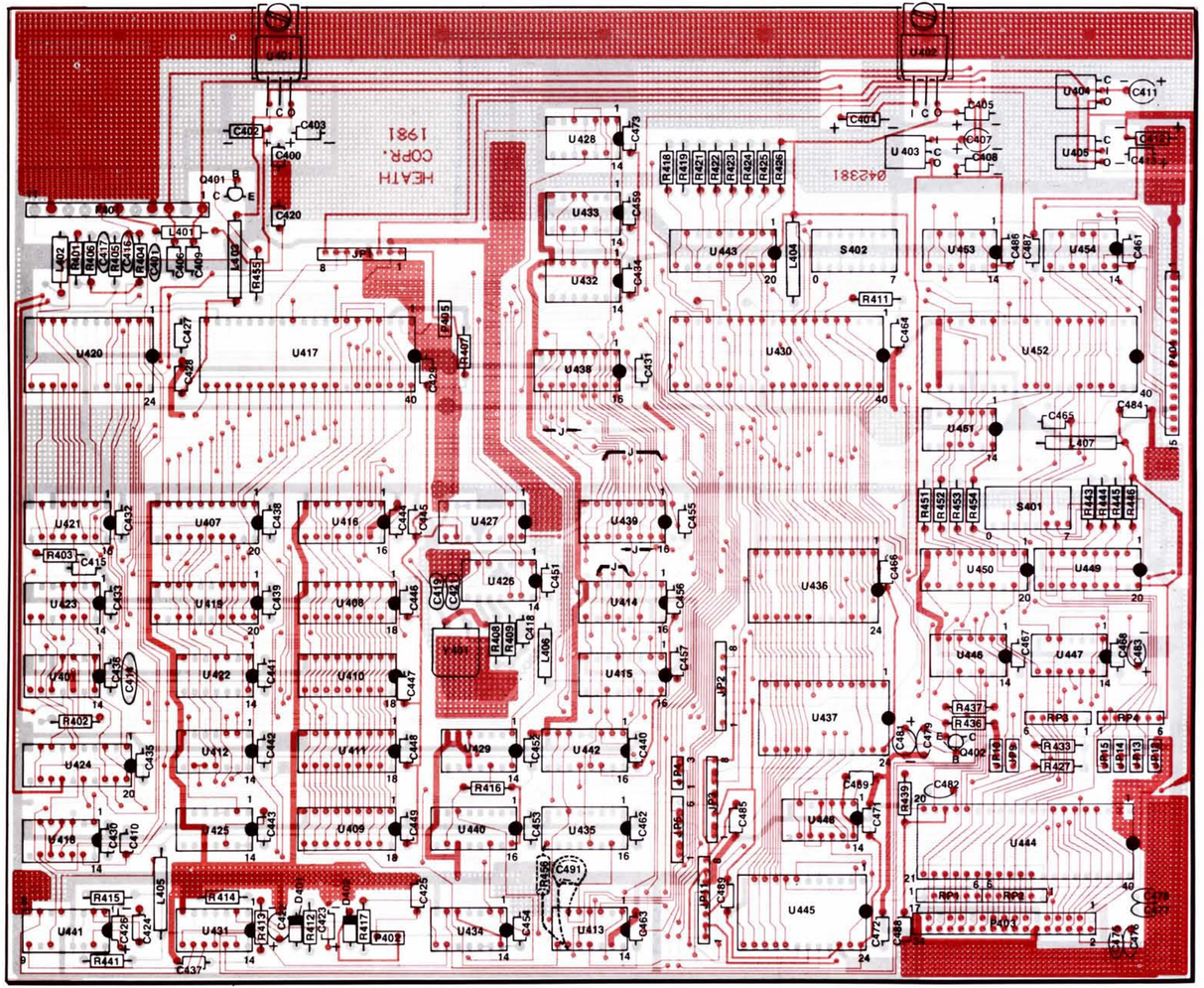
Z-89 AND Z-90 VIDEO DRIVER CIRCUIT BOARD

Part number HE 181-3387. Shown from the component side.



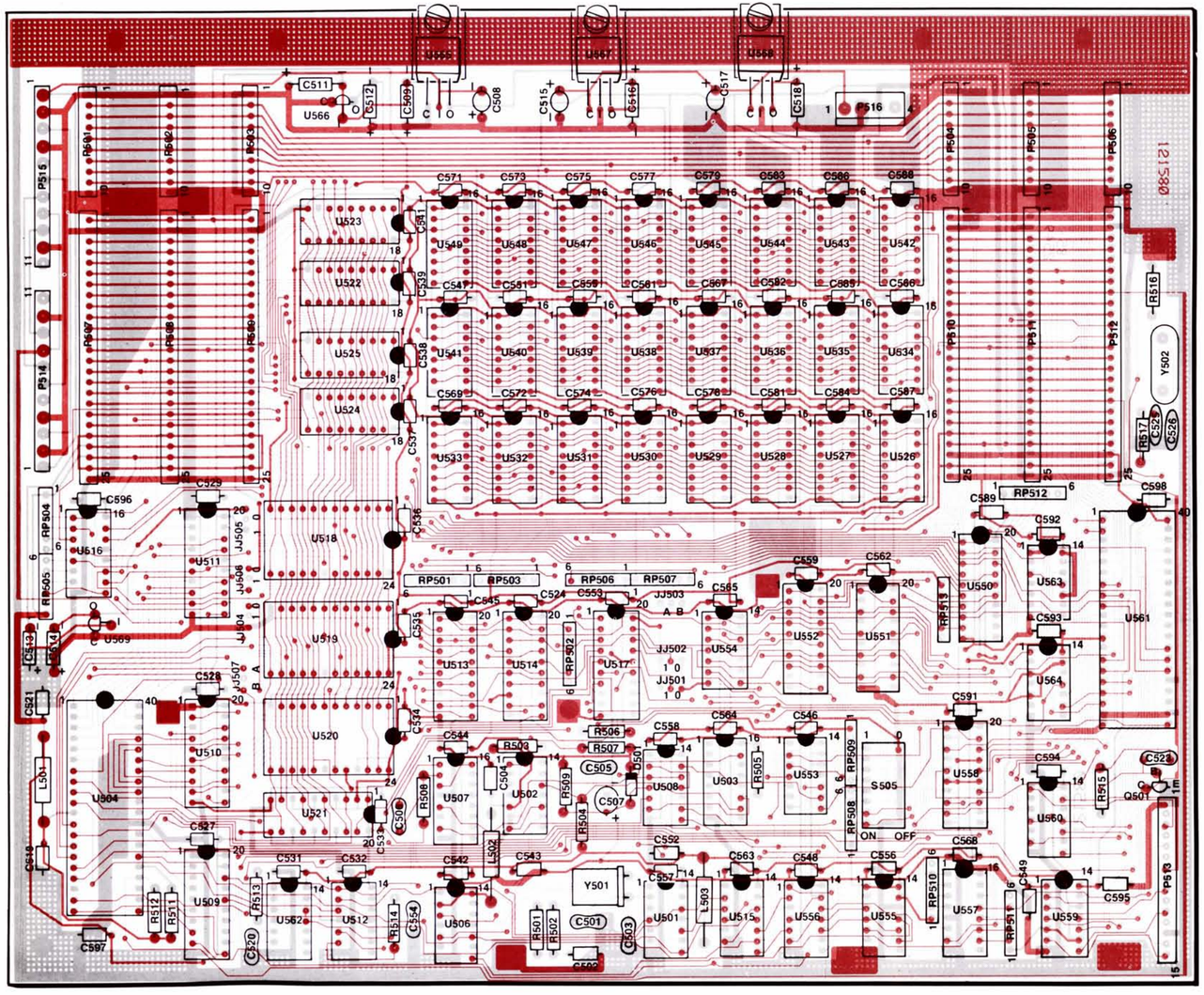
Z-89 AND Z-90 VIDEO DEFLECTION CIRCUIT BOARD

Part number HE 181-3400. Shown from the component side.



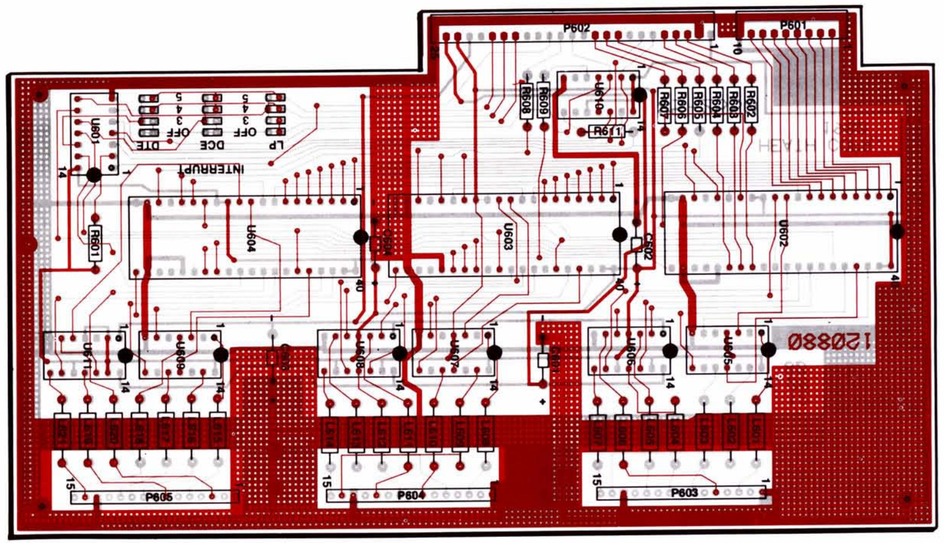
Z-89 AND Z-90 TERMINAL LOGIC CIRCUIT BOARD

Part number HE 181-3383. Shown from the component side.



Z-89 AND Z-90 CPU LOGIC CIRCUIT BOARD

Z-89 Part number HE 181-3396. Z-90 Part number HE 181-3615. Shown from the component side.



Z-89 AND Z-90 SERIAL INTERFACE I/O CIRCUIT BOARD

Part number HE 181-3389. Shown from the component side.

Semiconductor Identification Charts

This section is divided into two parts: "Component Number Index" and "Part Number Index." The first section provides a cross-reference between semiconductor Component Numbers and their respecitive Part Numbers. The Component Numbers are listed in numerical order. The second section provides a lead configuration detail (basing diagram) for each semiconductor Part Number. The Part Numbers in the second section are also listed in numerical order.

COMPONENT NUMBER INDEX

This index shows the Part Number of each semiconductor in the Computer.

POWER SUPPLY CIRCUIT BOARD

CIRCUIT COMPONENT NUMBER	PART NUMBER
BR1	HE 57-67
D101	HE 57-42
D102	HE 57-42
D103	HE 57-42
D104	HE 57-42
D109	HE 57-65
D110	HE 57-65
D111	HE 57-65
D112	HE 57-65
U101	HE 442-30
U102	HE 442-30
U103	HE 442-650

VIDEO CIRCUIT BOARD

Diodes

CIRCUIT COMPONENT NUMBER	PART NUMBER
D201	HE 56-94
D202	HE 56-56
D203	HE 56-58
D204	HE 56-56
D205	HE 56-73
D206	HE 56-56
D207	HE 57-27
D208	HE 57-614
D209	HE 57-27
D210	HE 57-27
D211	HE 57-64

Transistors

CIRCUIT COMPONENT NUMBER	PART NUMBER
Q201	HE 417-811
Q202	HE 417-924
Q203	HE 417-874
Q204	HE 417-282
Q205	HE 417-823
Q206	HE 417-885
Q207	HE 417-822
Q208	HE 417-821
Q209	HE 417-926
Q210	HE 417-926
Q211	HE 417-264
Q212	HE 417-263
Q213	HE 417-195
Q214	HE 417-923

Integrated Circuits

CIRCUIT COMPONENT NUMBER	PART NUMBER
U201	HE 442-53
U202	HE 442-53

VIDEO DRIVER CIRCUIT BOARD

Diodes

CIRCUIT COMPONENT NUMBER	PART NUMBER
D901	HE 57-27
D902	HE 56-93

Transistors

CIRCUIT COMPONENT NUMBER	PART NUMBER
Q901	HE 417-834
Q902	HE 417-875

TERMINAL LOGIC CIRCUIT BOARD

Diodes

CIRCUIT COMPONENT NUMBER	PART NUMBER
D401	HE 56-56
D402	HE 56-56

Transistors

CIRCUIT COMPONENT NUMBER	PART NUMBER
Q401	HE 417-937
Q402	HE 417-937

Terminal Logic Board (Cont'd.)

Integrated Circuits

CIRCUIT COMPONENT NUMBER	PART NUMBER
U401	HE 442-54
U402	HE 442-54
U403	HE 442-663
U404	HE 442-664
U405	HE 442-630
U406	HE 443-891
U407	HE 443-885
U408	HE 443-764
U409	HE 443-764
U410	HE 443-764
U411	HE 443-764
U412	HE 443-728
U413	HE 443-875
U414	HE 443-799
U415	HE 443-799
U416	HE 443-799
U417	HE 443-906
U418	HE 443-730
U419	HE 443-805
U420	HE 444-29
U421	HE 443-892
U422	HE 443-900
U423	HE 443-780
U424	HE 443-805
U425	HE 443-915
U426	HE 443-18
U427	HE 443-757
U428	HE 443-730
U429	HE 443-34
U430	HE 443-881
U431	HE 443-792
U432	HE 443-779
U433	HE 443-733
U434	HE 443-228
U435	HE 443-877
U436	Not used
U437	HE 444-46
U438	HE 443-721
U439	HE 443-721
U440	HE 443-760
U441	HE 443-727
U442	HE 443-877
U443	HE 443-791
U444	HE 443-913
U445	HE 444-37
U446	HE 443-18
U447	HE 443-792
U448	HE 443-792
U449	HE 443-791
U450	HE 443-791
U451	HE 443-730
U452	HE 443-952
U453	HE 443-794
U454	HE 443-795

Resistor Packs

CIRCUIT COMPONENT NUMBER	PART NUMBER
RP1	HE 9-98
RP2	HE 9-98

CPU LOGIC CIRCUIT BOARD

Diode

CIRCUIT COMPONENT NUMBER	PART NUMBER
D501	HE 56-56

Transistor

CIRCUIT COMPONENT NUMBER	PART NUMBER
Q501	HE 417-821

Integrated Circuits

CIRCUIT COMPONENT NUMBER	PART NUMBER
U501	HE 443-18
U502	HE 443-34
U503	HE 443-760
U504	HE 443-881
U506	HE 443-730
U507	HE 443-727
U508	HE 443-792
U509	HE 443-824
U510	HE 443-837
U511	HE 443-837
U512	HE 443-730
U513	HE 443-824
U514	HE 443-824
U515	HE 443-779
U516	HE 444-41 or 444-83
U517	HE 444-66
U518	HE 444-62* or 444-84**
U519	Not Used
U520	HE 444-19
U521	HE 443-754
U522	Not Used
U523	HE 443-764
U524	Not Used
U525	HE 443-764
U526-U549	HE 443-904
U550	HE 444-61
U551	HE 443-791
U552	HE 443-805
U553	HE 443-875
U554	HE 443-732
U555	HE 443-730
U556	HE 443-730
U557	HE 443-912
U558	HE 443-754
U559	HE 443-794
U560	HE 443-795
U561	HE 443-952
U562	HE 443-792
U565	HE 442-664
U566	HE 442-665
U567	HE 442-663
U568	HE 442-663
U569	HE 442-665

SERIAL INTERFACE CIRCUIT BOARD

Integrated Circuits

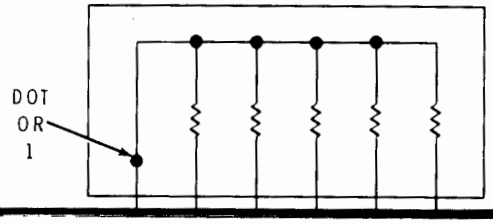
CIRCUIT COMPONENT NUMBER	PART NUMBER
U601	HE 443-818
U602	HE 443-952
U603	HE 443-874
U604	HE 443-952
U605	HE 443-795
U606	HE 443-794
U607	HE 443-795
U608	HE 443-794
U609	HE 443-795
U610	HE 443-730

* Used for MTR-89
** Used for MTR-90

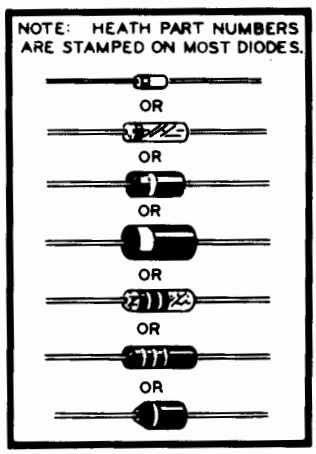
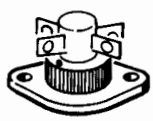
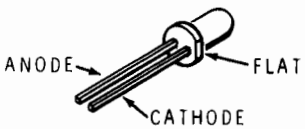
PART NUMBER INDEX

This index shows a lead configuration detail (basing diagram) of each semiconductor part number.

RESISTOR PACK

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 9-98		220 kΩ resistor network	

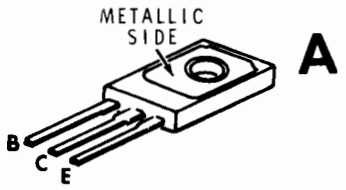
DIODES

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 56-56	1N4149	10 mA, 75 V	
HE 56-58	1N709A	Zener, 6.2 V, 25 mA	
HE 56-73	MZ2360	Compensation	
HE 56-93	FD333	225 mA, 125 V	
HE 56-94		Zener, 12.8 V, 12 mA	
HE 57-27	1N2071	SI Rect 1 A, 600 V	
HE 57-42	3A1	SI Rect 3 A, 100 V	
HE 57-64	DRS-110	SI Rect 1 A, 1000 V	
HE 57-65	1N4002	SI Rect 1 A, 100 V	
HE 57-614	MR-508	SI Rect 3 A, 800 V	
HE 57-67	10A20	Diode Bridge	
HE 412-640		Light-emitting Diode	

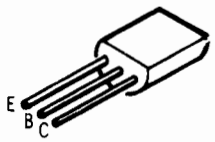
TRANSISTORS

PART NUMBER	MAY BE REPLACED WITH	BASING DIAGRAM
HE 417-195	MJE340	A
HE 417-282	MJ2841	E
HE 417-811	MPSL01	B
HE 417-821	MPSA06	B
HE 417-822	MPSA56	B
HE 417-823	MPU131	C
HE 417-834	MPSU10	D
HE 417-874	2N3906	B
HE 417-875	2N3904	B
HE 417-885	MPSA65	B
HE 417-923	BU500	E
HE 417-924	MJE172	A
HE 417-926	MPSU06	D
HE 417-927	MPSA93	B
HE 417-932	MJE182	A
HE 417-937	MPS2369	B

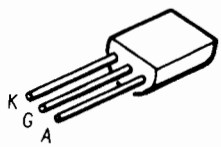
LEAD CONFIGURATION (TOP VIEW)



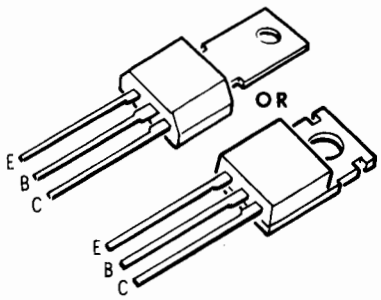
A



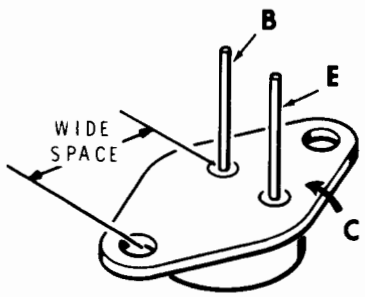
B



C

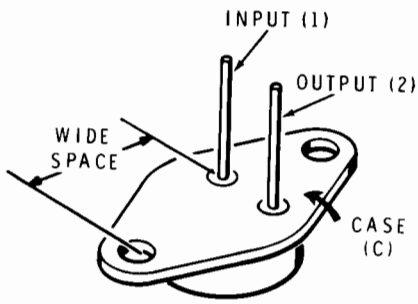
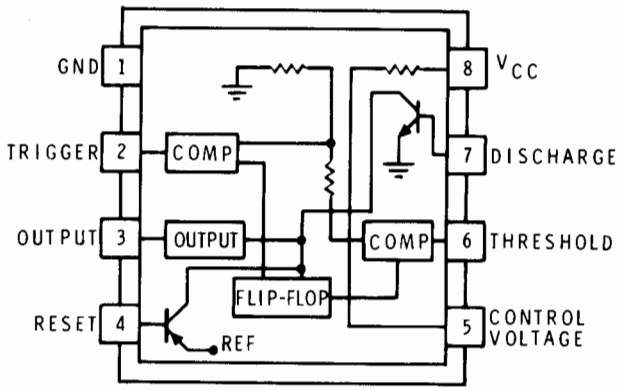
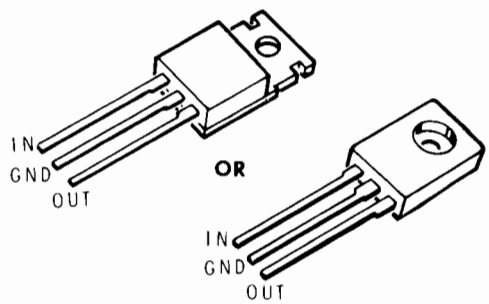
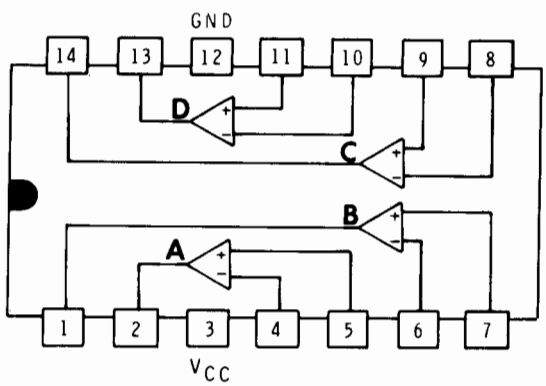


D

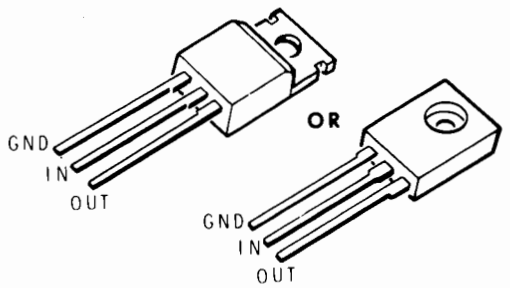
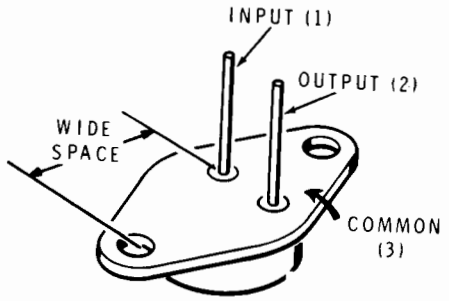
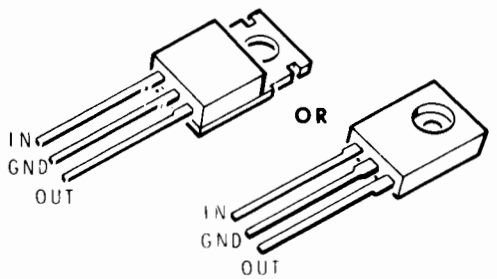
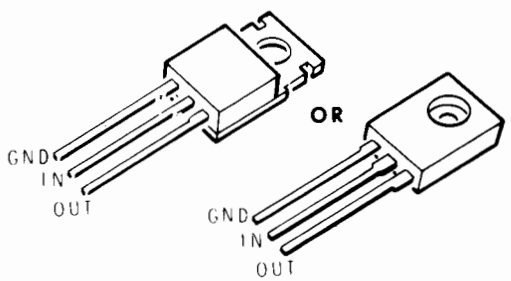
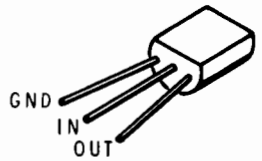


E

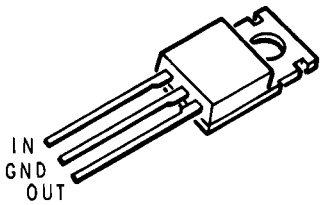
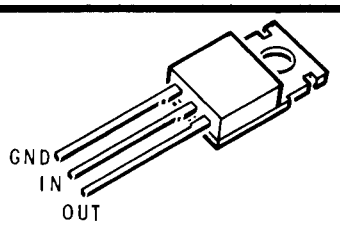
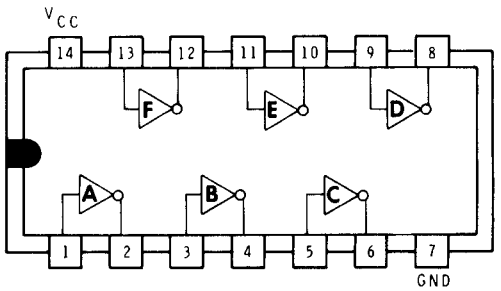
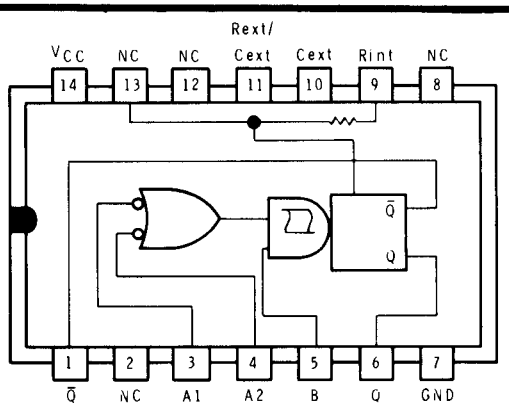
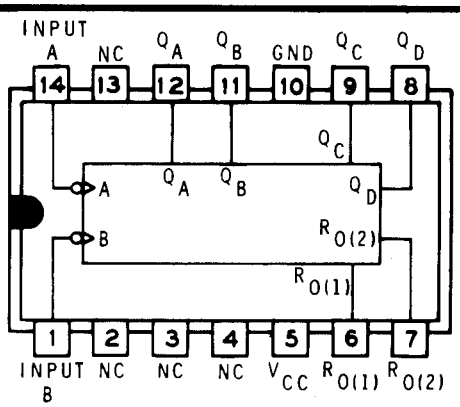
INTEGRATED CIRCUITS

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 442-30	μA309K LM309	5-volt Regulator	
HE 442-53	555	Timer	
HE 442-54	7805	+5 V Regulator	
HE 442-616	LM3302N, LM2901, or μA775 (selected)	Quad Operational Amplifier	

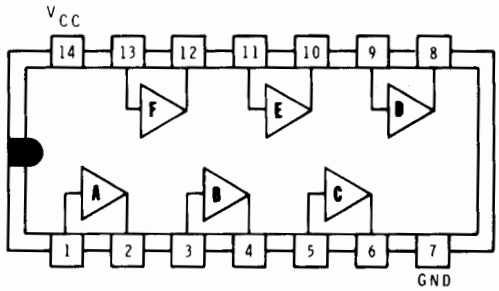
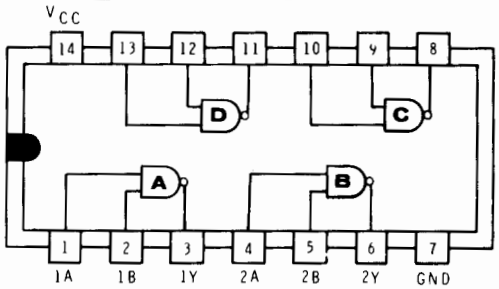
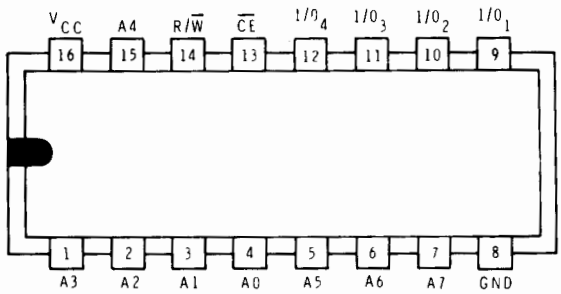
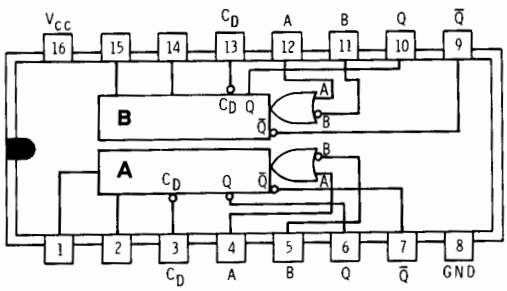
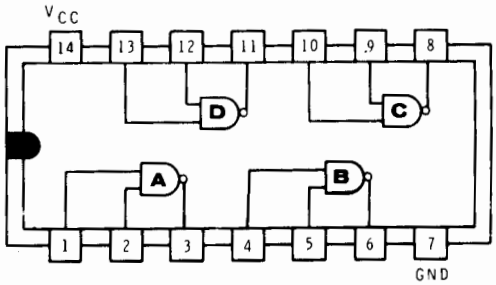
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 442-630	7905.2	−5.2 V Regulator	
HE 442-650	78H12	+12 V, 5 A Regulator	
HE 442-663	78M12CKC	+12 V Regulator	
HE 442-664	79M12CKC	−12 V Regulator	
HE 442-665	79L05AC	−5 V Regulator	

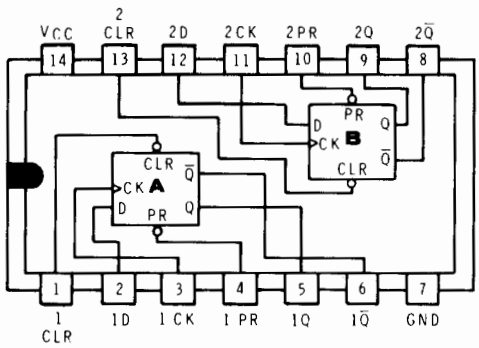
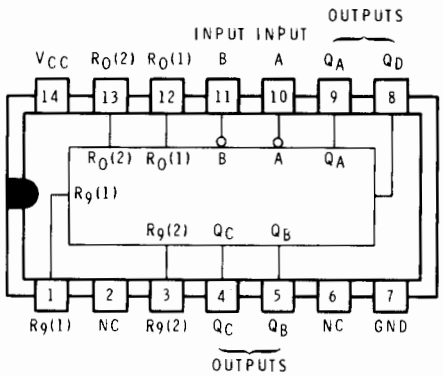
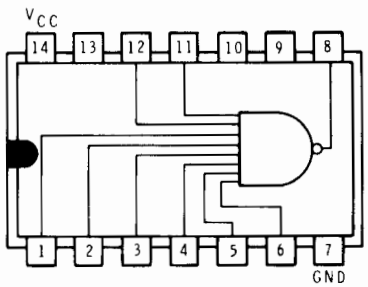
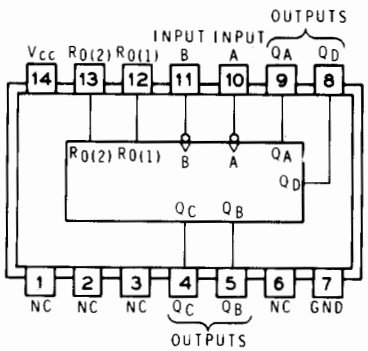
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 442-674	UA7812	+12 V Regulator	
HE 442-683	79M05	−5 V Regulator	
HE 443-18	7404	Hex Inverter	
HE 443-22	74121	Monostable Multivibrator	
HE 443-34	7492	Divide-By-Twelve Counter	

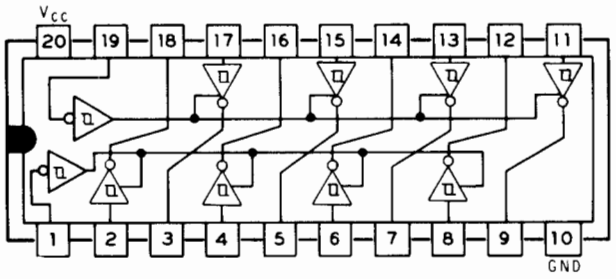
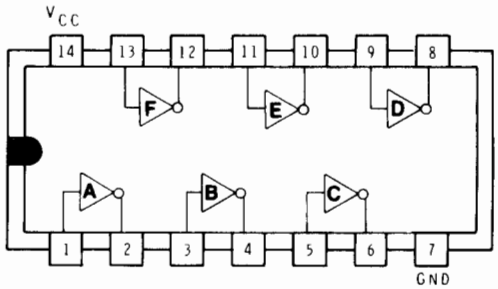
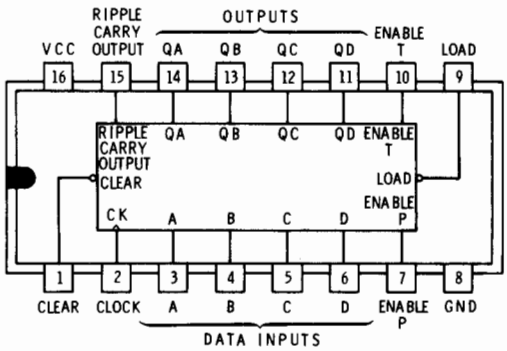
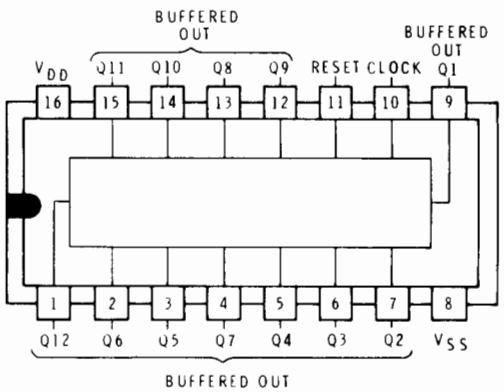
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-73	7416	Line Driver	
HE 443-77	7438	Quadruple 2-Input Positive-NAND Buffers With Open-collector Outputs	
HE 443-721	2112-2	256 × 4 RAM	
HE 443-727	96L02	Dual Monostable	
HE 443-728	74LS00	Quad 2-input NAND	

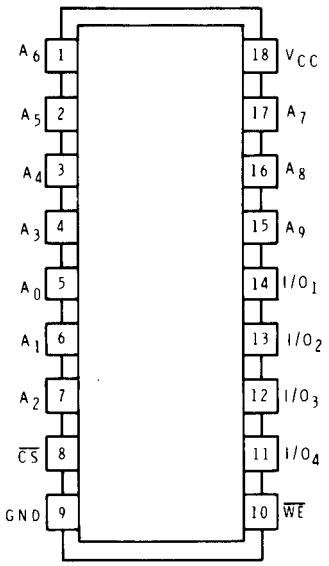
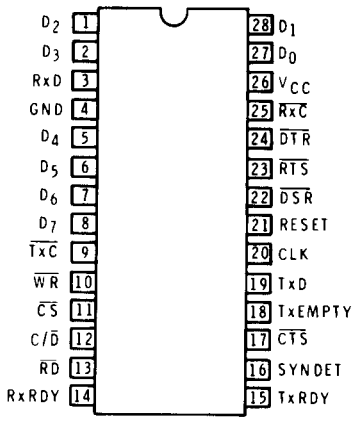
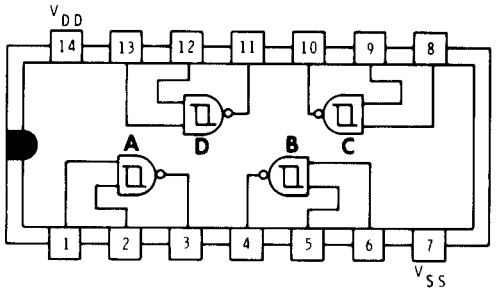
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-730	74LS74	Dual D Flip-flop	
HE 443-731	SN74LS290	BCD Counter	
HE 443-732	SN74LS30	8-input NAND	
HE 443-733	74LS293	4-Bit Binary Counter	

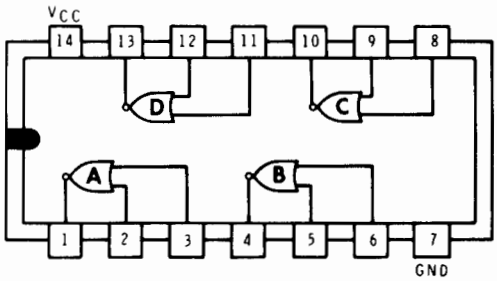
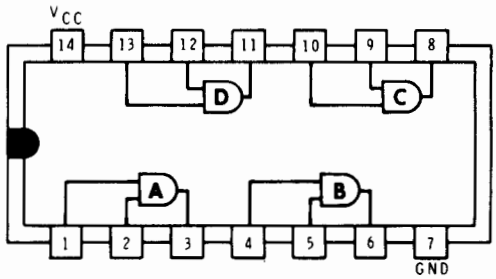
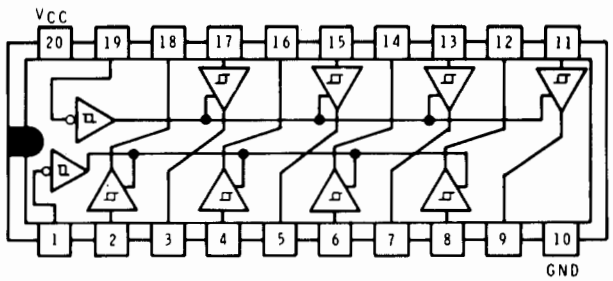
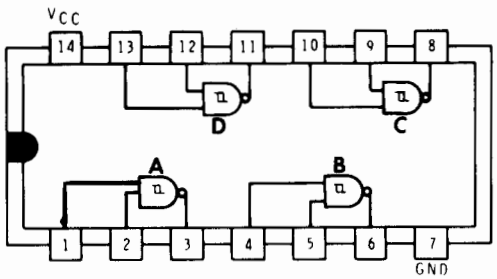
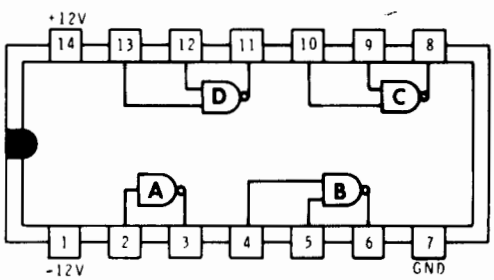
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-754	74LS240	Octal buffer, 3-state outputs	
HE 443-755	74LS04	Hex Buffer	
HE 443-757	74LS161	4-Bit Binary Counter	
HE 443-760	4040	12-Bit Binary	

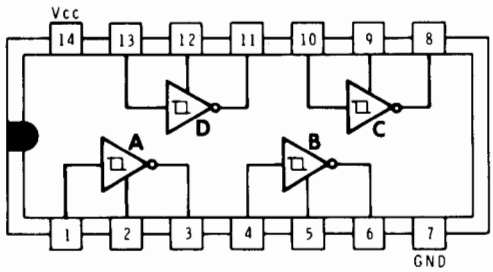
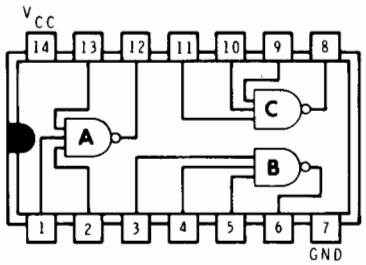
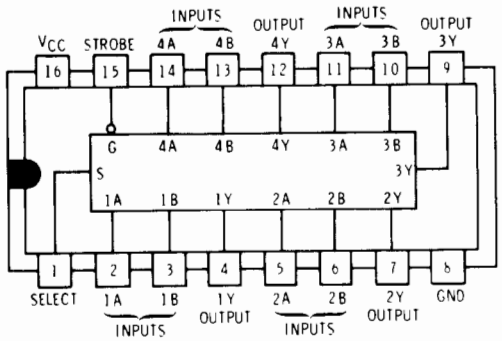
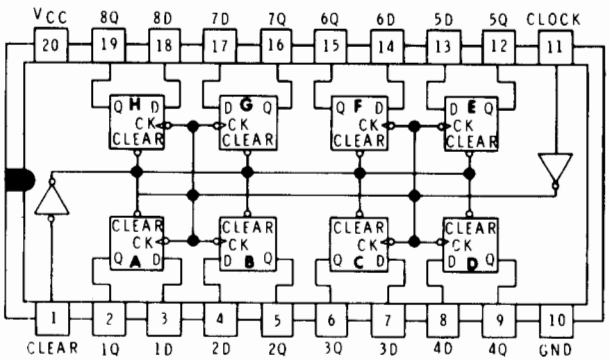
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-764	2114	1K × 4 RAM	
HE 443-776	8251	USART	
HE 443-778	4093	Quad 2-input NAND SCHMITT Trigger	

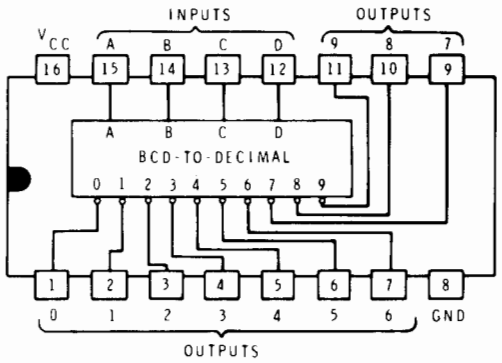
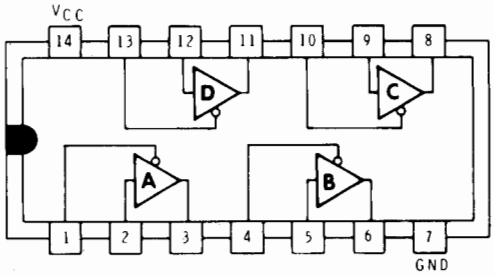
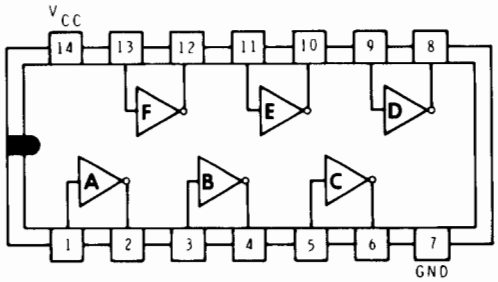
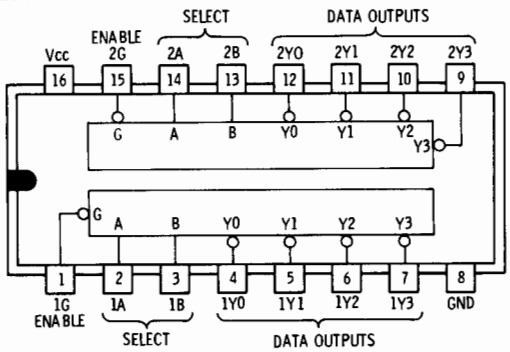
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-779	74LS02	Quad 2-input Positive-NOR gates	
HE 443-780	74LS08	Quad 2-input Positive-AND Gates	
HE 443-791	74LS244	Noninverting 3-state output octal buffers	
HE 443-792	74LS132	Quad 2-input Positive-NAND Schmitt Triggers	
HE 443-794	75188 or 1488	EIA Driver	

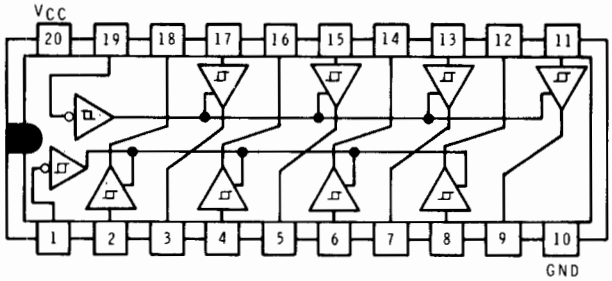
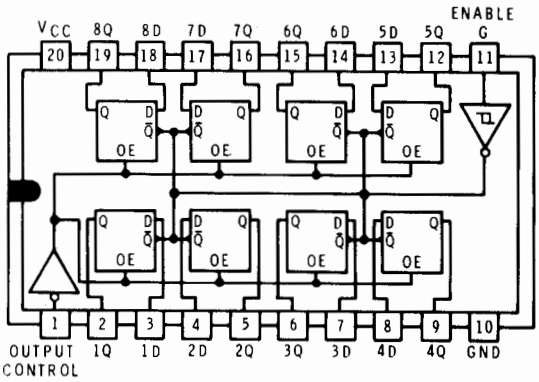
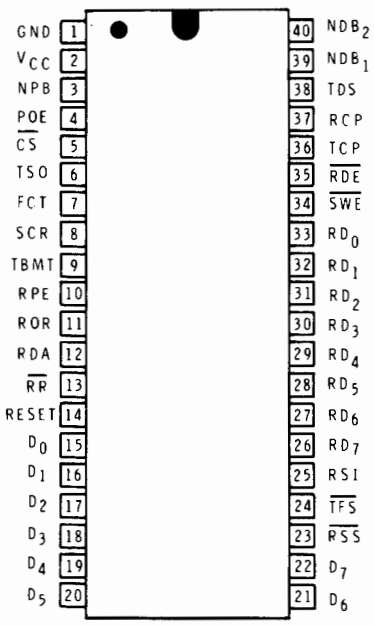
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-795	75189 or 1489	EIA Receiver	
HE 443-797	74LS10	Triple 3-input Positive-NAND Gate	
HE 443-799	74LS157	Quad 2-line-to-1-line Multipliers	
HE 443-805	74LS273	Octal D Flip-flop with clear	

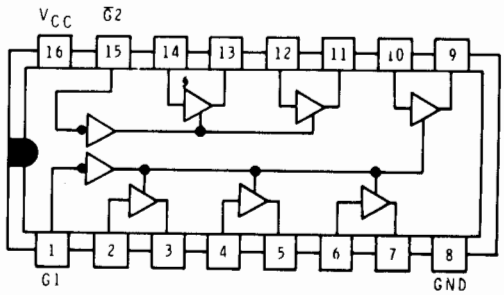
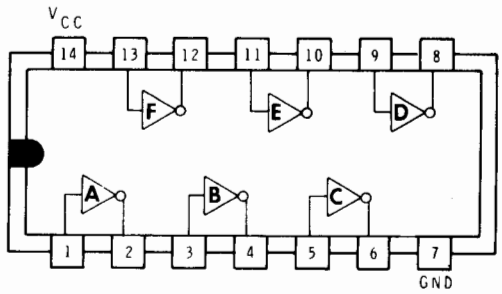
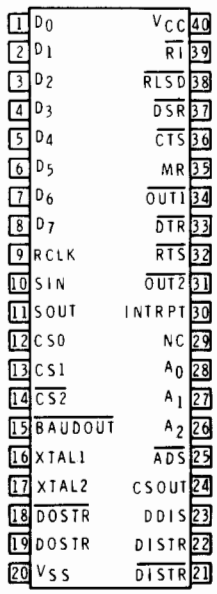
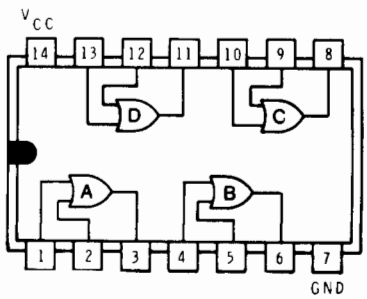
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-807	74LS42	BCD-to-Decimal Decoder	
HE 443-811	74LS125	Quad bus buffer gate with 3-state outputs	
HE 443-818	74LS05	Hex Inverter	
HE 443-822	74LS139	Dual 2-to-4-line decoder	

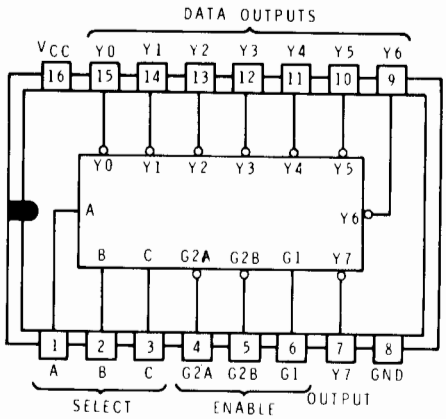
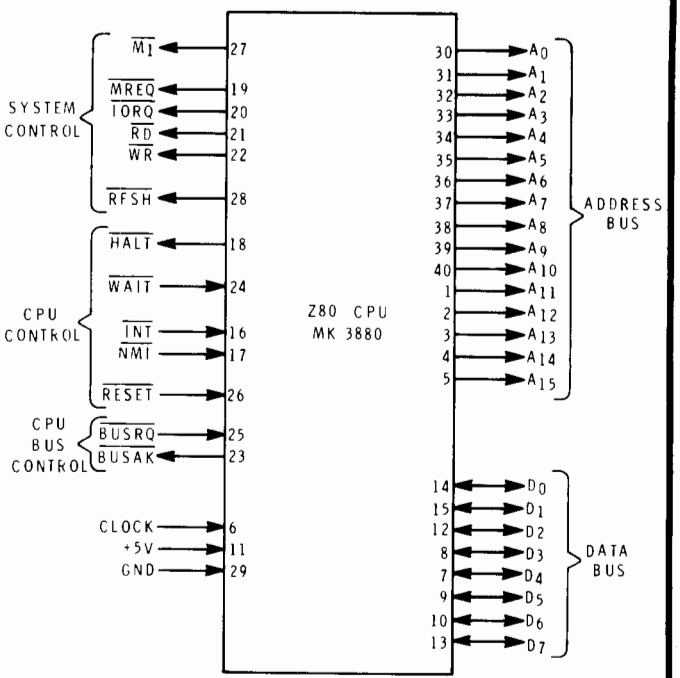
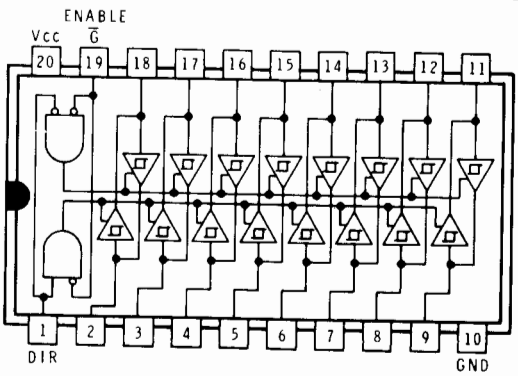
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-824	74LS241	Octal buffer	
HE 443-837	74LS373	Octal D latch	
HE 443-856	S2350	Universal Synchronous Receiver/ Transmitter (USRT)	

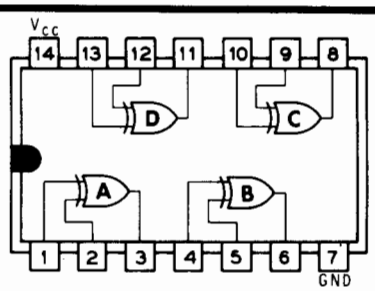
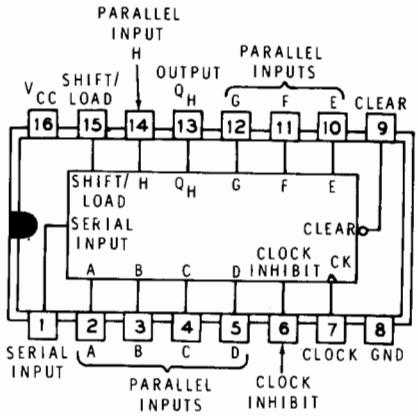
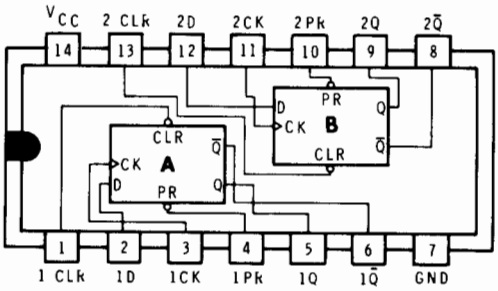
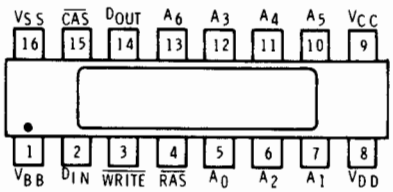
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-857	74LS367	Hex Bus Drivers	
HE 443-872	74LS14	Hex SCHMITT-Trigger Inverters	
HE 443-952	8250B	ACE	
HE 443-875	74LS32	Quad 2-input Positive OR Gates	

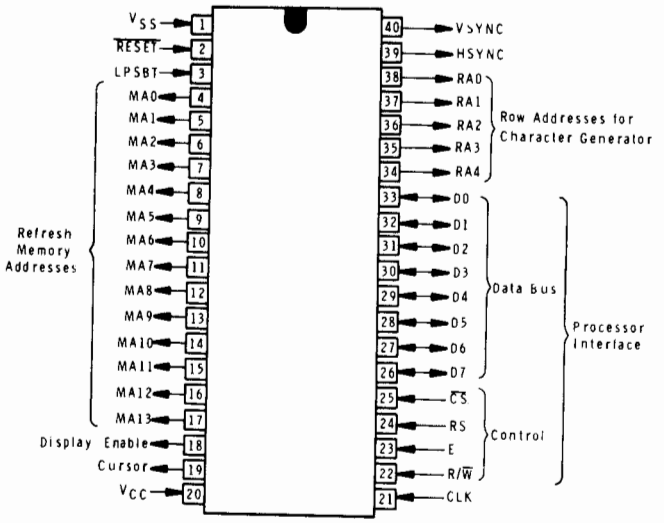
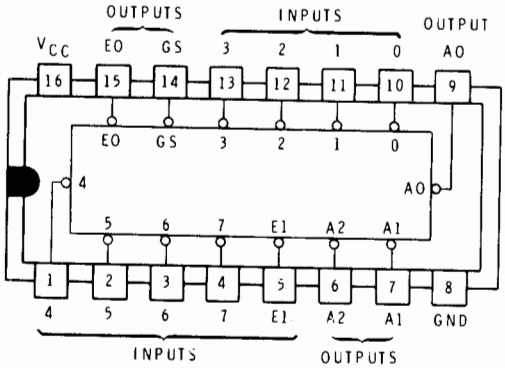
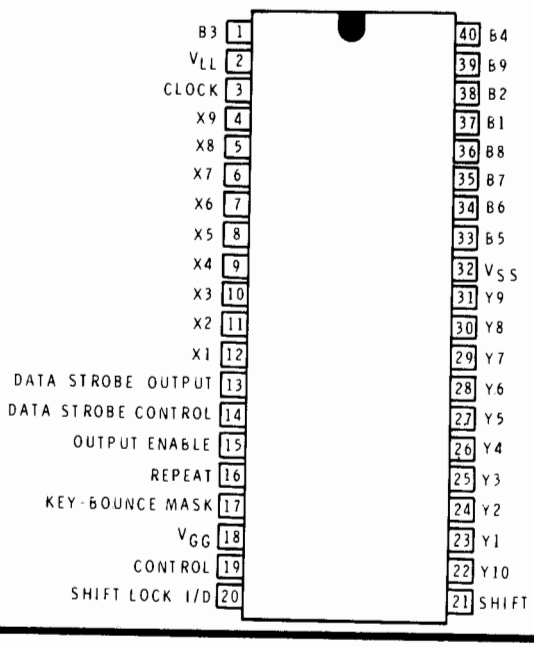
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-877	74LS138	3-to-8-line Decoder	
HE 443-881	Z 80	Microprocessor	
HE 443-885	74LS245	Octal bus transceiver	

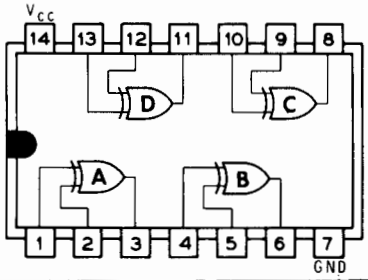
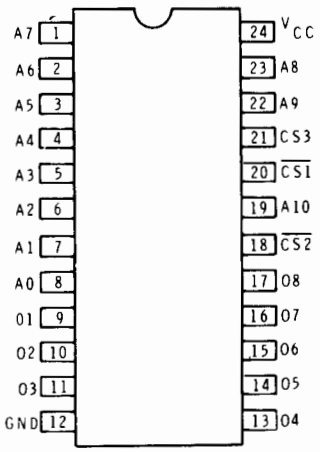
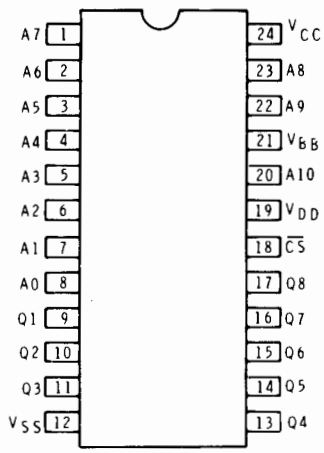
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-891	74LS86	Quad 2-input Exclusive — OR	
HE 443-892	74LS166	8-bit shift register	
HE 443-900	74S74	Dual-D Flip-flop	
HE 443-904	MK4116-4	16K × 1 RAM	

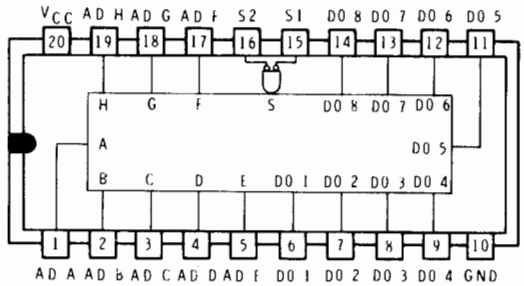
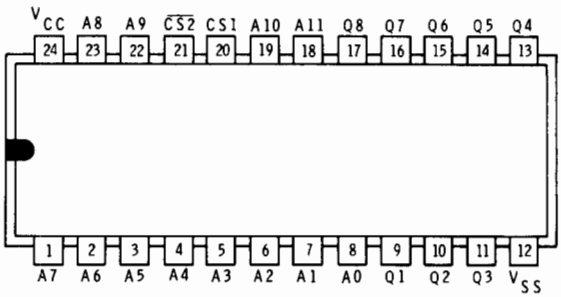
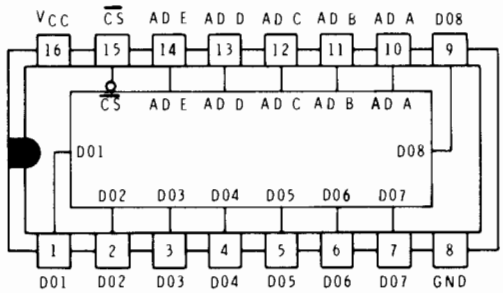
Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-906	6845	CRT Controller	
HE 443-912	74LS148	8-line-to-3-line Priority encoder	
HE 443-913	S740	Keyboard Encoder	

Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-915	74S86	Quad 2-input Exclusive — OR	
HE 444-19 HE 444-29 HE 444-37	2316 or 8316	2K × 8-bit ROM (Available only from Heath Co.)	
HE 444-62 or HE 444-84	2716	PROM (Available only from Heath Co.)	

Integrated Circuits (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 444-66 HE 444-61	SN74S47D	256 × 8-bit PROM (Available only from Heath Co.)	
HE 444-46	8332A	4K × 8-bit PROM (Available only from Heath Co.)	
HE 444-41 or HE 444-83	SN74S188A	32K × 8-bit ROM (Available only from Heath Co.)	

Replacement Parts List

POWER SUPPLY

(Z-89 and Z-90 part number HE 181-3244.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
CAPACITORS, Electrolytic		
C101	HE 25-902	10,000 μF
C102	HE 25-906	4700 μF
C103	HE 25-902	10,000 μF
C104	HE 25-891	470 μF
DIODES		
BR1	HE 56-67	Bridge rectifier
D101	HE 57-42	3A1
Diodes (cont'd.)		
D102	HE 57-42	3A1
D103	HE 57-42	3A1
D104	HE 57-42	3A1
D109	HE 57-27	1N2071
D110	HE 57-27	1N2071
D111	HE 57-27	1N2071
D112	HE 57-27	1N2071
INTEGRATED CIRCUIT		
See "Semiconductor Identification."		

VIDEO DEFLECTION CIRCUIT BOARD

(Z-89 and Z-90 part number HE 181-3400.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
NOTE: The following resistors are 5%, 1/2-watt unless otherwise specified.		
R201	HE 6-105	1 MΩ
R202	HE 6-472	4700 Ω
R203	HE 6-102	1000 Ω
R204	HE 6-682	6800 Ω
R205	HE 6-472	4700 Ω
R206	HE 6-101	100 Ω
R207	HE 6-6491	6490 Ω, 1%
R208	HE 6-1871-12	1870 Ω, 1/4-watt, 1%
R209	HE 6-102	1000 Ω
R210	Not used	
R211	HE 3-6-2	.51 Ω, 2-watt
Resistors (cont'd.)		
R212	HE 3-57-5	1500 Ω, 5-watt, 10%
R213	HE 6-470	47 Ω
R214	Not used	
R215	HE 6-152	1500 Ω
R216	HE 6-332	3300 Ω
R217	HE 6-104	100 kΩ
R218	HE 6-223	22 kΩ
R219	HE 10-390	20 kΩ control
R220	Not used	
R221	HE 6-224	220 kΩ
R222	HE 6-273	27 kΩ
R223	HE 10-390	20 kΩ control
R224	HE 6-822	8200 Ω
R225	HE 6-103	10 kΩ
R226	HE 6-623	62 kΩ

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION

Resistors (cont'd.)

R227	HE 6-473	47 kΩ
R228	HE 6-103	10 kΩ
R229	HE 6-122	1200 Ω
R230	Not used	
R231	HE 6-182	1800 Ω
R232	HE 6-101	100 Ω
R233	HE 6-105	1 MΩ
R234	HE 6-103	10 kΩ
R235	HE 6-273	27 kΩ
R236	HE 6-222	2200 Ω
R237	HE 6-150	15 Ω
R238	HE 6-471	470 Ω
R239	HE 6-279	2.7 Ω
R240	Not used	
R241	HE 6-279	2.7 Ω
R242	HE 6-479	4.7 Ω
R243	HE 6-102	1000 Ω
R244	HE 6-223	22 kΩ
R245	HE 6-273	27 kΩ
R246	HE 10-311	5000 Ω control
R247	HE 6-6491	6490 Ω, 1%
R248	HE 6-273	27 kΩ
R249	HE 6-392	3900 Ω
R250	Not used	
R251	HE 6-201	200 Ω
R252	HE 6-470	47 Ω
R253	HE 6-392	3900 Ω
R254	HE 3-22-2	1.2 Ω, 2-watt
R255	HE 6-101	100 Ω
R256	HE 3-22-2	1.2 Ω, 2-watt
R257	HE 3-22-2	1.2 Ω, 2-watt
R258	HE 6-104	100 kΩ
R259	HE 6-331	330 Ω
R260	Not used	
R261	HE 6-473	47 kΩ
R262	HE 6-104	100 kΩ
R263	HE 6-823	82 kΩ
R264	HE 6-225	2 MΩ
R265	HE 6-394	390 kΩ
R266	HE 6-335	3.3 MΩ
R267	HE 6-335	3.3 MΩ
R268	HE 6-102	1000 Ω

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION

CAPACITORS

C201	HE 25-911	22 μF, 25 V
C202	HE 21-140	.001 μF ceramic
C203	HE 25-865	10 μF electrolytic
C204	HE 25-220	10 μF tantalum
C205	HE 25-220	10 μF tantalum
C206	HE 21-176	.01 μF ceramic
C207	HE 25-883	47 μF electrolytic
C208	HE 27-145	.22 μF Mylar
C209	HE 27-145	.22 μF Mylar
C210	Not used	
C211	HE 27-841	4.7 μF tantalum
C212	HE 29-32	.0068 μF polystyrene
C213	HE 25-865	10 μF electrolytic
C214	HE 21-176	.01 μF ceramic
C215	HE 21-140	.001 μF ceramic
C216	HE 25-890	330 μF electrolytic
C217	HE 21-75	100 pF ceramic
C218	HE 21-176	.01 μF ceramic
C219	HE 21-75	100 pF ceramic
C220	Not used	
C221	HE 29-22	.0047 μF polystyrene
C222	HE 21-176	.01 μF ceramic
C223	HE 29-22	.0047 μF polystyrene
C224	HE 27-73	.047 μF Mylar
C225	HE 25-882	22 μF electrolytic
C226	HE 25-220	10 μF tantalum
C227	HE 25-882	22 μF electrolytic
C228	HE 29-56	.006 μF polypropylene
C229	HE 25-299	1.5 μF electrolytic
C230	Not used	
C231	HE 29-57	.22 μF polypropylene
C232	HE 27-206	1 μF polycarbonate
C233	HE 21-193	.005 μF spark gap
C234	HE 25-883	.47 μF electrolytic
C235	HE 21-122	.02 μF ceramic
C236	HE 21-122	.02 μF ceramic
C237	HE 21-122	.02 μF ceramic

DIODES — TRANSISTORS – IC's

See "Semiconductor Identification."

INDUCTORS – CHOKES – TRANSFORMERS

L201	HE 40-581	620 μH inductor
L202	HE 45-42	8.75 μH choke
L203	HE 40-1947	19 μH inductor
L204	HE 40-1948	52 μH inductor
T201	HE 51-197	Driver transformer
T202	HE 51-200	Flyback transformer

VIDEO DRIVER CIRCUIT BOARD

(Z-89 and Z-90 part number HE 181-3387.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
R901	HE 6-105-12	1 MΩ, 1/4-watt, 5%
R902	HE 6-102-12	1000 Ω, 1/4-watt, 5%
R903	HE 1-50-2	820 Ω, 2-watt
R904	HE 1-45	220 Ω, 1/2-watt, 10%
R905	HE 6-750-12	75 Ω, 1/4-watt, 5%
R906	HE 6-220-12	22 Ω, 1/4-watt, 5%
R907	HE 1-9	1000 Ω, 1/2-watt, 10%
R908	HE 1-25	47 kΩ, 1/2-watt, 10%
R909	HE 1-25	47 kΩ, 1/2-watt, 10%
R910	Not used	
R911	HE 6-370-12	33 Ω, 1/4-watt, 5%
CAPACITORS		
C901	HE 21-176	.01 μF ceramic
C902	HE 21-176	.01 μF ceramic
Capacitors (cont'd.)		
C903	HE 21-176	.01 μF ceramic
C904	HE 21-176	.01 μF ceramic
C905	HE 25-865	10 μF electrolytic
C906	HE 20-106	390 pF mica
C907	HE 21-176	.01 μF ceramic
C908	HE 21-176	.01 μF ceramic
DIODES — TRANSISTORS		
See "Semiconductor Identification."		
CHOKE		
L901	HE 45-39	4.65 μH choke

TERMINAL LOGIC CIRCUIT BOARD

(Z-89 and Z-90 part number HE 181-3383.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
NOTE: All resistors are 1/4-watt, 5%.		
R401	HE 6-222-12	2200 Ω
R402	HE 6-470-12	47 Ω
R403	HE 6-101-12	100 Ω
R404	HE 6-222-12	2200 Ω
R405	HE 6-101-12	100 Ω
R406	HE 6-102-12	1000 Ω
R407	HE 6-102-12	1000 Ω
R408	HE 6-561-12	560 Ω
R409	HE 6-561-12	560 Ω
R410	Not used	
R411	HE 6-331-12	330 Ω
R412	HE 6-103-12	10 kΩ
R413	HE 6-102-12	1000 Ω
R414	HE 6-103-12	10 kΩ
R415	HE 6-224-12	220 kΩ
R416	HE 6-102-12	1000 Ω
R417	HE 6-100-12	10 Ω
R420	Not used	
R418-R426	HE 6-103-12	10 kΩ
R427-R435	HE 6-103-12	10 kΩ
Resistors (cont'd.)		
R430	Not used	
R436	HE 6-102-12	1000 Ω
R437	HE 6-472-12	4700 Ω
R438	HE 6-272-12	2700 Ω
R439	HE 6-103-12	10 kΩ
R440	Not used	
R441	HE 6-224-12	220 kΩ
R442-R454	HE 6-103-12	10 kΩ
R450	Not used	
R455	HE 6-102-12	1000 Ω
R456	HE 6-101-12	100 Ω
R457	HE 6-102-12	1000 Ω
RP1	HE 9-98	220 kΩ resistor network
RP2	HE 9-98	220 kΩ resistor network
CAPACITORS		
C400	HE 21-176	.01 μF ceramic
C401	HE 21-46	.005 μF ceramic
C402	HE 25-221	2.2 μF tantalum
C403	HE 25-221	2.2 μF tantalum
C404	HE 25-221	2.2 μF tantalum
C405	HE 25-221	2.2 μF tantalum
C406	HE 21-176	.01 μF ceramic

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
Capacitors (cont'd.)		
C407	HE 25-276	4.7 μF tantalum
C408	HE 25-221	2.2 μF tantalum
C409	HE 21-176	.01 μF ceramic
C410	HE 21-176	.01 μF ceramic
C411	HE 25-276	4.7 μF tantalum
C412	HE 25-221	2.2 μF tantalum
C413	HE 25-221	2.2 μF tantalum
C414	HE 21-167	39 pF ceramic
C415	HE 21-176	.01 μF ceramic
C416	HE 21-711	470 pF ceramic
C417	HE 21-140	.001 μF ceramic
C418	HE 21-176	.01 μF ceramic
C419	HE 20-101	47 pF mica
C420	HE 21-176	.01 μF ceramic
C421	HE 20-103	150 pF mica
C422	HE 25-223	47 μF tantalum
C423	HE 25-221	2.2 μF tantalum
C424	HE 21-95	.1 μF ceramic
C425	HE 21-95	.1 μF ceramic
C426	HE 25-221	2.2 μF tantalum
C427-C457	HE 21-95	.1 μF ceramic
C458	HE 21-176	.01 μF ceramic
C459-C474	HE 21-95	.1 μF ceramic
C475-C478	HE 21-711	470 pF ceramic
C479	HE 21-140	.001 μF ceramic
C480	Not used	
C481	HE 25-220	10 μF tantalum
C482	HE 21-46	.005 μF ceramic
C483	HE 25-223	47 μF tantalum
C484	HE 21-176	.01 μF ceramic
C485	HE 21-176	.01 μF ceramic
C486	HE 21-176	.01 μF ceramic
C487	HE 21-176	.01 μF ceramic
C488	HE 21-176	.01 μF ceramic
C489	HE 21-176	.01 μF ceramic
C490	Not used	
C491	HE 21-711	470 pF ceramic
MISCELLANEOUS		
S401	HE 60-621	DIP switch
S402	HE 60-621	DIP switch
Y401	HE 404-613	12.288 MHz crystal

DIODES – TRANSISTORS – IC's

See "Semiconductor Identification."

CPU LOGIC CIRCUIT BOARD

(Z-89 part number HE 181-3396 — Z-90 part number HE 181-3615.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
NOTE: All resistors are 1/4-watt, 5%.		
R501	HE 6-561-12	560 Ω
R502	HE 6-561-12	560 Ω
R503	HE 6-331-12	330 Ω
R504	HE 6-102-12	1000 Ω
R505	HE 6-102-12	1000 Ω
R506	HE 6-471-12	470 Ω
R507	HE 6-103-12	10 kΩ
R508	HE 6-184-12	180 kΩ
R509	HE 6-103-12	10 kΩ
R510	Not used	
R511	HE 6-102-12	1000 Ω
R512	HE 6-102-12	1000 Ω
R513	HE 6-151-12	150 Ω
R514	HE 6-151-12	150 Ω
R515	HE 6-472-12	4700 Ω
R516	HE 6-152-12	1500 Ω
R517	HE 6-105-12	1 MΩ
CAPACITORS		
C501	HE 20-103	150 pF mica
C502	HE 21-185	.01 μF ceramic
C503	HE 20-101	47 pF mica
C504	HE 21-186	.01 μF ceramic
C505	HE 20-106	390 pF mica
C506	HE 20-171	820 pF mica
C507	HE 25-282	68 μF tantalum
C508	HE 25-221	2.2 μF tantalum
C509	HE 25-197	1.0 μF
C510	Not used	
C511	HE 25-195	2.2 μF tantalum
C512	HE 25-197	1.0 μF tantalum
C513	HE 25-195	2.2 μF tantalum
C514	HE 25-197	1.0 μF tantalum
C515	HE 25-221	2.2 μF tantalum
C516	HE 25-197	1.0 μF tantalum
C517	HE 25-221	2.2 μF tantalum
C518	HE 25-197	1.0 μF tantalum
C519	HE 21-185	.01 μF ceramic
C520	Not used	
C521	HE 21-185	.01 μF ceramic
C522	HE 21-114	270 pF ceramic

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
Capacitors (cont'd.)		
C523	HE 21-22	220 pF ceramic
C524	HE 21-185	.01 μF ceramic
C525	HE 21-3	10 pF ceramic
C526	HE 21-5	20 pF ceramic
C527-C597	HE 21-185	.01 μF ceramic

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
MISCELLANEOUS		
SW501	HE 60-621	8-section switch
Y501	HE 404-613	12.288 MHz crystal
Y502	HE 404-608	1.843 MHz crystal
DIODE — TRANSISTOR — IC's		
See "Semiconductor Identification."		

CHASSIS PARTS

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
R1	HE 10-1178	500 Ω control
C1	HE 25-857	1500 μF electrolytic capacitor
T1	HE 54-969	Power transformer
T2	HE 181-3152	Yoke assembly
SW1	HE 60-642	115/230 switch
SW2	HE 60-643	NORM/LOW switch
SW3	HE 61-43	Power switch
F1	HE 421-23	1-ampere fuse
F1	HE 421-25	1.5-ampere fuse
—	HE 401-163	Speaker
V1	HE 411-838	White CRT
	OR	
—	HE 411-851	White anti-glare CRT
	OR	
—	HE 411-852	Green anti-glare CRT
—	HE 950-3	Top cover - assembly
—	HE 90-1263-1	Top cover
—	HE 90-725	Brass inserts
—	HE 352-33	Vibra-tite sealant
—	HE 950-2	Base cabinet - assembly
—	HE 90-1262-1	Terminal base
—	HE 90-725	Brass inserts
—	HE 352-33	Vibra-tite sealant
—	HE 950-6	Bezel cover - assembly
—	HE 90-1244-1	Bezel cover
—	HE 90-725	Brass inserts
—	HE 90-352-33	Vibra-tite sealant
—	HE 90-1239-1	Front panel
—	HE 95-646	Disk box
—	HE 391-635	ZDS nameplate
—	HE 64-864	12-key keypad
—	HE 64-865	4-key keypad (off line, f_1, f_2, f_3)
—	HE 64-866	4-key keypad (f_4, f_5, ERASE, BLUE)
—	HE 64-872	4-key keypad (RED, WHITE, RESET, BREAK)
—	HE 90-1238-1	Keyboard cover

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SERIAL INTERFACE I/O CIRCUIT BOARD

(Z-89 and Z-90 part number HE 181-3389.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
R601	HE 6-102-12	1000 Ω
R602	HE 6-181-12	180 Ω
R603	HE 6-181-12	180 Ω
R604	HE 6-181-12	180 Ω
R605	HE 6-181-12	180 Ω
R606	HE 6-181-12	180 Ω
R607	HE 6-181-12	180 Ω
R608	HE 6-181-12	180 Ω
R609	HE 6-181-12	180 Ω
R610	HE 6-181-12	180 Ω
R611	HE 6-181-12	180 Ω

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
CAPACITORS		
C601	HE 25-221	1.0 μF tantalum
C602	HE 25-221	1.0 μF tantalum
C603	HE 25-221	1.0 μF tantalum
C604	HE 25-221	1.0 μF tantalum
COILS		
(21) L601-L621	HE 45-614	10 μH
INTEGRATED CIRCUITS		
See "Semiconductor Identification."		

CABLES

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
PERIPHERAL CABLES		
Model Z-25		
—	HE 134-1115	20 conductor head to PCB
—	HE 134-1134	6 conductor head sensor
—	HE 134-1135	6 conductor paper sensor
—	HE 134-1155	5 conductor 2 D-connector
Model Z-47		
—	HE 134-1101	AC power
—	HE 134-1102	35 conductor power supply
—	HE 134-1103	25 conductor DC
—	HE 134-1104	34 conductor controller
—	HE 134-1105	26 conductor slave drive
—	HE 134-1106	4 conductor write protect
Model Z-67 and Z-87		
—	HE 134-1167	40 conductor SH/INT/CON
—	HE 134-1168	50 conductor RDG/DISK A1
—	HE 134-1169	50 conductor RDG/DISK A2
—	HE 134-1170	20 conductor RDG/DSK DAT AB
—	HE 134-1172	50 conductor host interface
—	HE 134-1174	10 conductor AC
—	HE 134-1175	18 conductor DC
—	HE 134-1178	7 conductor w/plug

CIRCUIT Comp. No.	PART NUMBER	MODEL
CABLES		
I/O Cables		
—	HE 134-1114	Z-25
—	HE 134-1166	Z-37
—	HE 134-1108	Z-47
—	HE 134-1216	Z-67
—	HE 134-1216	Z-87

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
Z-89/90 INTERNAL CABLES		
—	HE 134-1066	Keyboard to TLB
—	HE 134-1163	89/37 I/O to backplate
—	HE 134-1073	Serial I/O to backplate
—	HE 134-1100	H-88-1 extention cable
—	HE 134-1107	89-47 to backplate
—	HE 134-1216	89-67 to backplate
—	HE 134-1075	CPU P513 to TLB P404
—	HE 347-83	CPU P515 to TLB P401