H/Z-100 COMPUTER SERVICE DATA MANUAL; ADDITIONAL AND UPDATE MATERIAL

DIRECTIONS:

REPLACE the following pages with the accompanying updated pages:

Pages 3-21 through 3-28,

Pages 3-67/3-68,

Pages 3-141 through 3-144,

First two pages in Section 5, Disk Controller and Drives.

ADD Part II to Section 5. This is new data for the H-207 Floppy Disk Controller Board.

CHANGE the following:

Page 2-99, Parts Required,

Part number of the programming plug...

from: HE 969-18 to: HE 432-1168.

Page 3-159, Connectors and Sockets,

Part number of the 4-pin right-angle connector...

from: HE 432-363 to HE 434-363.

UPDATE the Motherboard schematics (refer to the enclosed schematic revision sheet).

INITIAL SETUP

INTRODUCTION

The H/Z-100 is easy to disassemble; even an all-in-one unit requires only about 15 minutes to remove the motherboard.

However, due to the way the unit is packaged, there are very few test points that you can reach while the unit is assembled and operating. To get around this, you should build the following extender cables.

These extender cables allow you to spread out the H/Z-100 over a 29" x 46" surface. This permits you to easily reach every IC while the unit is operating.

PARTS REQUIRED

Qty.	Description	Part No.
2	40-pin ribbon cable w/connectors	HE 134-1108
1	34-pin ribbon cable w/connectors	HE 134-1025
4	Small alligator clips for jumper wire construction	HE 260-16
20 ft.	#18 stranded wire	HE 344-155
20	Large spring connector	HE 432-753
1	10-pin adapter plug	HE 432-788
2	10-hole socket shell	HE 432-1061
1	Programming plug	HE-432-1168

$\overline{\text{TEST}}$, Pin 23 Test Input: This input is examined by the "wait for test" software instruction. If pin 23 is low, execution continues, otherwise the processor waits in an idle state.

MN/$\overline{\text{MX}}$, Pin 33 Minimum/Maximum: Logic one on this pin places the 8088 in the minimum mode, the mode used by the H/Z-100. When placed in the maximum mode, some of the pin functions change. Usually, the maximum mode is used for larger systems and multi-processing systems.

RESET, Pin 21 Reset: Goes high to reset the 8088. The interrupts are disabled, certain registers in the 8088 are set or cleared, and the instruction pointer (program counter) points to the memory address 16 bytes below the top end of the 1 megabyte range (FFFF0H).

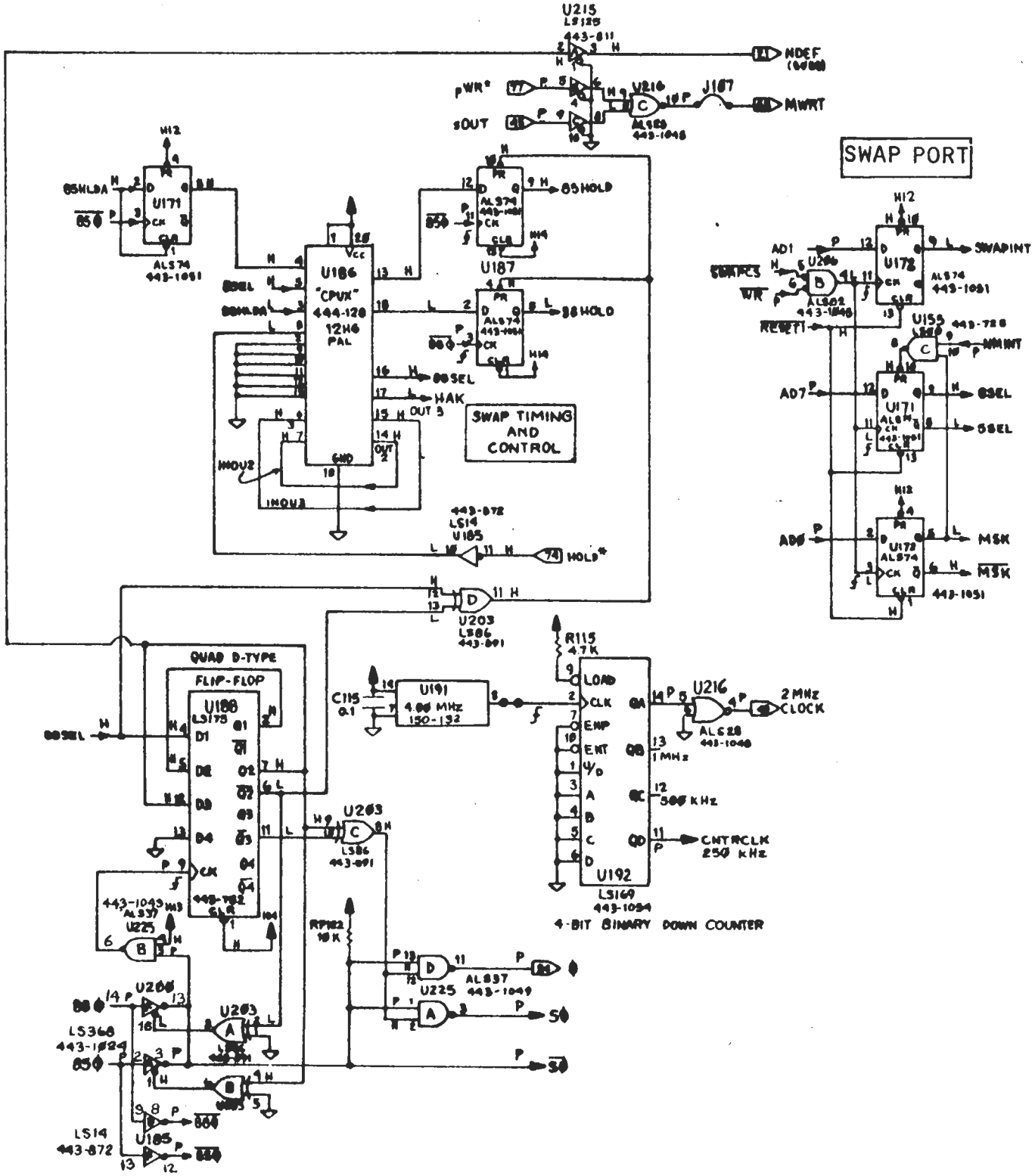
This line is asserted when the $\overline{\text{RESET}}$ line at U236-11 is pulled low. A Schmitt trigger shapes this signal and the clock circuits retimes it before applying it to the 8088.

READY, Pin 22 Ready: This is an acknowledgement signal from the addressed memory or I/O port that it is ready to transfer data. When this line is low, the CPU goes into a wait state until the addressed device brings it high. This allows using the 8088 with slow memory or I/O devices.

The READY signal is generated when U205-9 places a logic one on U236-4. U236 synchronizes this signal with the 8088 clock to ensure correct set up and hold times.

CLK, Pin 19 8088 Clock Input. Five-megahertz clock to provide timing to the 8088.

This signal comes from U236-8 which derives it from the 15-MHz crystal at Y103. Duty cycle is about 33% for optimized timing inside the 8088. When the 8088 is the active processor, this line also goes to the processor swap port as 880 to provide system timing.



PROCESSOR SWAP PORT (MB1)

PROCESSOR SWAP PORT

OVERVIEW

The processor swap port controls which CPU is to be active, handles interrupt routing, and ensures proper timing of the clock circuits during the swap. To access the swap port, the CPU writes a control byte to port 0FEH. Only three bits of the byte are used: AD0 controls the interrupt mask, AD1 controls the swap interrupt line, and AD7 performs the processor swap.

PROCESSOR SWAP

Refer to schematic MB1 as you read the following.

At power up, the reset circuits clear U171-9 to logic zero. This pin, 8SEL, connects to U186-5, a 12H6 PAL. This IC responds by placing a logic zero on U187-12 and a logic one on U187-2. On the first positive transition of $\overline{85\phi}$, the 85HOLD line will go low, enabling the 8085 CPU. On the first positive transition of $\overline{88\phi}$, the 88HOLD line will go high, disabling the 8088 CPU.

The 8085, while executing the code in the monitor ROM, soon transfers control to the 8088. It does this by setting bit 7 of the processor swap port control byte to logic one. Here's how...

The CPU addresses port 0FEH to assert $\overline{\text{SWAPCS}}$ (from the I/O decoder) at U206-5. It then sets AD7 to logic one at U171-12. Finally, it asserts the write line at U206-6. As a result, U171-11 goes high and latches U171-9 to logic one. The 8SEL line is now asserted.

The values at U172-12 and U172-2 are also latched to their respective outputs, but these will be covered later.

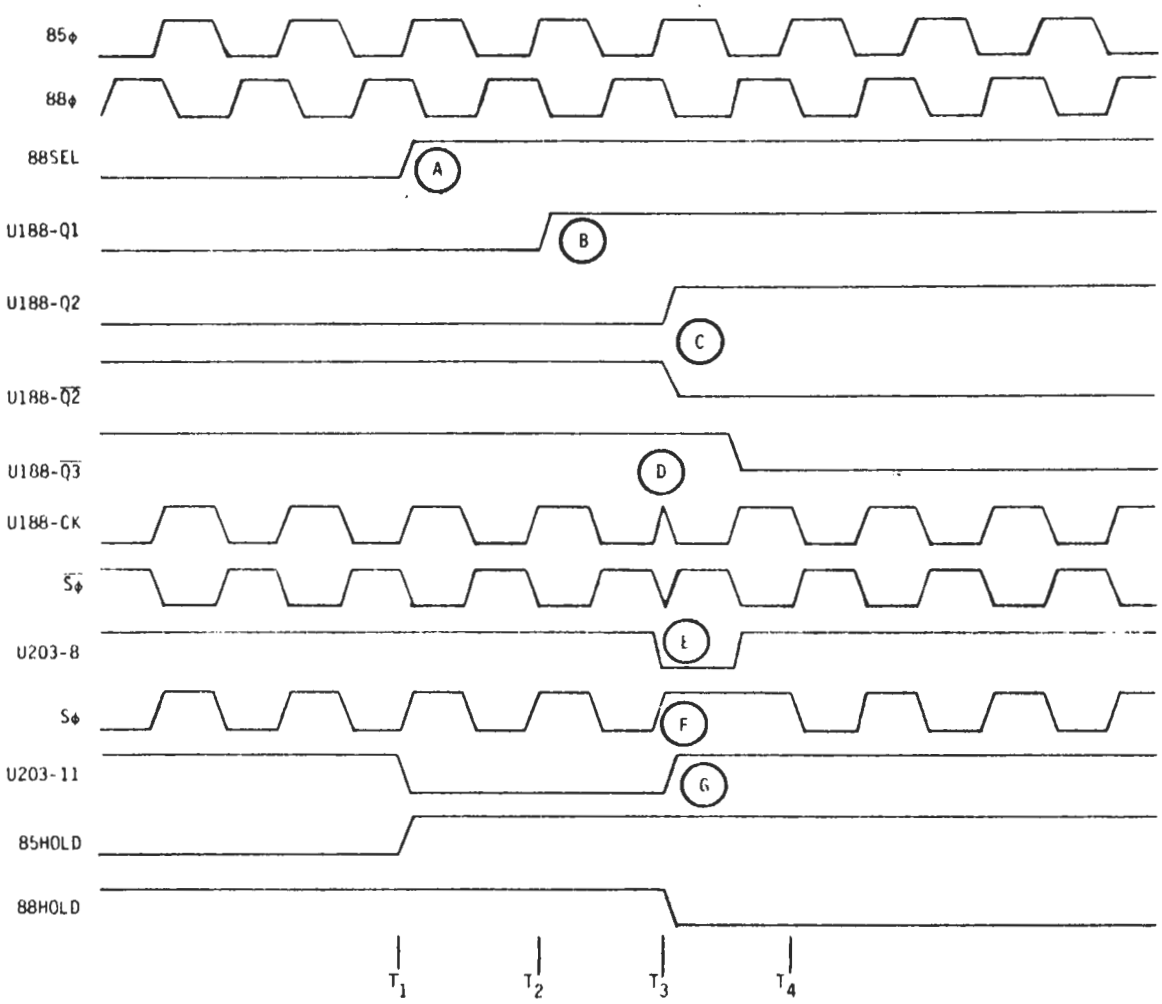
The 8SEL line, now logic one, causes U186-13 to change to logic one, U186-18 to change to logic zero, and U186-16 to change to logic one.

The HOLD* line at U185-11 asserts whenever a board on the S-100 bus takes control of the H/Z-100. This causes U186 to disable both the 8085 and the 8088 through U187. Both CPUs respond by returning their hold-acknowledge signals; the 8088 at U186-3 and the 8085 at U171-2. When this happens, U186 asserts the HAK line at pin 17. This, in turn, raises the S-100 pHLDA line to logic one at U180-9. The board that generated the HOLD* request can now take control of the H/Z-100.

SWAP TIMING

The 88SEL line also goes to U188-4, a quad D-type latch. This circuit is designed to suppress any glitches on the system clock line when the H/Z-100 switches from one CPU to the other. It also ensures that the CPU being disabled is no longer active when the other CPU is enabled.

The 8085 and the 8088 run on separate crystal-controlled clocks; the 8085 from Y101 and the 8088 from Y103. Although these clocks are stable, they aren't in phase. Switching from one clock to another can cause a glitch on the system clock line, Sϕ, which can upset the timing in other circuits.



SWITCHING FROM 8085 to 8088

To see how U188 and its associated circuits block this spike, refer to the waveforms on the previous page.

The two top waveforms are the respective clocks for the 8085 and 8088 CPUs. These are present at the inputs of inverters U200-2 and U200-14. Assuming that the 8085 is the active processor, then U200-1 is low and 85ϕ couples through the inverter to form $\overline{S\phi}$. It also couples through U225B to clock U188.

At time T1, the 8088 is selected; the 88SEL line goes to logic one as shown at A on the waveforms illustration. The next clock pulse at U188-9 latches this logic one into U188-2, the Q1 output at B.

The next clock pulse causes the Q2 output to latch high, shown at C. This tri-states U200 through the exclusive-OR gate at U203B. At the same time, $\overline{Q2}$ goes low to couple the 88ϕ clock to the $\overline{S\phi}$ line. Since, in this example, the two clocks are nearly 180-degrees out of phase, the clock immediately returns to zero, causing the spike at D in the waveforms illustration.

Up until this time, the output of U203-8, another exclusive-OR gate, has been logic one. This is because its inputs Q2 and $\overline{Q3}$ of U188 have been in opposite states. However, since Q2 went low at time T3, both inputs to U203C are the same, causing U203-8 to go to logic zero (waveform E). This forces the system clock output at U225-3 to logic one until time T4 (waveform F).

At time T4, the first positive-going edge of the 8088 clock causes the $\overline{Q3}$ output of U188 to go high. This opens the gate at U225A to pass the system clock, which is now the 8088 signal.

As mentioned earlier, the other function that 88SEL and U188 perform is to ensure that the CPU being disabled is completely disabled before the other CPU is activated. To see how this is done, again refer to the waveforms illustration.

Once again, assume that the H/Z-100 is switching from the 8085 to the 8088. At time T1, the 88SEL line goes high, which is coupled to U203-11. The other input of this exclusive-OR gate is the Q2 line from U188. Since both inputs are now the same state, U203-11 goes to logic zero to preset both HOLD latches at U187.

Both CPUs respond by going into a HOLD state and sending hold-acknowledge signals to U186; the 8088 to pin 3 and the 8085 to pin 4 through U171. This asserts HAK at pin 17 which drives the S-100 pHLDA line at U180-9.

At time T3, the $\overline{Q2}$ line goes low and U203-11 returns to logic one, thus releasing the latches at U187 from their preset states. The next $\overline{88\Phi}$ clock pulse latches the logic zero at U187-2 into U187-5, removing the 8088 from the hold state.

Also at this time, U188-7 goes high to drive U215-3 high. This last IC connects to pin 21 of the S-100 bus to form the NDEF (8088) line. This line is a "not-to-be-defined" line that can be used for any function by the computer manufacturer. For the H/Z-100, this line asserts when the 8088 is active.

INTERRUPT MASK

The interrupt mask circuits ensure that interrupt requests are sent to the currently active CPU. The mask bit, MSK, is set or cleared by setting or clearing bit 0 of the processor swap port. If set, and the 8085 is active, the 8085 gets all interrupt requests. If cleared, and the 8085 is active, the interrupt request is blocked. However, the swap port will disable the 8085 and enable the 8088. If the 8088 is active, all interrupt requests are sent to the 8088 regardless of the mask bit. Here's how it's done...

Immediately after reset, the 8085 CPU is the active processor. Control lines 5SEL at U171-8 and MSK at U172-6 are logic one. These two lines connect to U225-9 and U225-10, shown near the 8085 IC on the schematic. U220-2 inverts the resulting logic zero to enable U189A and U189D. So all interrupts are sent to the 8085; maskable through U189A, non-maskable through U189D.

The 8SEL line, which is the complement of 5SEL, disables U189B and U189C, the AND gates to the 8088. Later, when the 8085 hands control to the 8088 CPU, 8SEL will go high and 5SEL will go low.

If, while the 8085 is selected, the $\overline{\text{MSK}}$ line is set to logic zero, U220-2 disables U189A and U189D. This blocks the interrupt request from both the 8085 and the 8088. However, if an interrupt request should occur, either standard or NMI, U156-6 will go high to assert the NMINT line.

The NMINT line connects to U155-9 in the processor swap port. The other input is the MSK line which is also high. As a result, U155-8 goes low to assert the 8SEL line. The H/Z-100 swaps to the 8088 processor as described previously.

When the 8088 CPU is active, 8SEL is high to enable U189B and U189C. U189A and U189D are disabled because 5SEL is logic zero at U225-9. So, no matter what the setting of the $\overline{\text{MSK}}$ bit at U225-10, all interrupt requests will be routed to the 8088 processor.

MAP SELECTING

Map selecting takes place at pins 1 and 15 of U111. These two lines, MAPSEL0 and MAPSEL1, also go to U173-7 and -8; but currently are not used by this IC. Depending on the logic state of U111-1 and U111-15, plus the address on lines BA12-BA15, the memory map will appear to be in one of the four configurations shown in the illustration:

Configuration #1: MAPSEL1 = 0 MAPSEL0 = 0

This is the default configuration, memory is contiguous from 0 to 192K.

Configuration #2: MAPSEL1 = 0 MAPSEL0 = 1

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 1. The two 16K areas and the rest of RAM are unchanged. This configuration may be used for MP/M while running the 8085 CPU.

Configuration #3: MAPSEL1 = 1 MAPSEL0 = 0

In this configuration, the first 48K of bank zero appears to be swapped with the first 48K of bank 2. The two 16K areas and the middle 64K of RAM are unchanged. This configuration may also be used for MP/M while running the 8085 CPU.

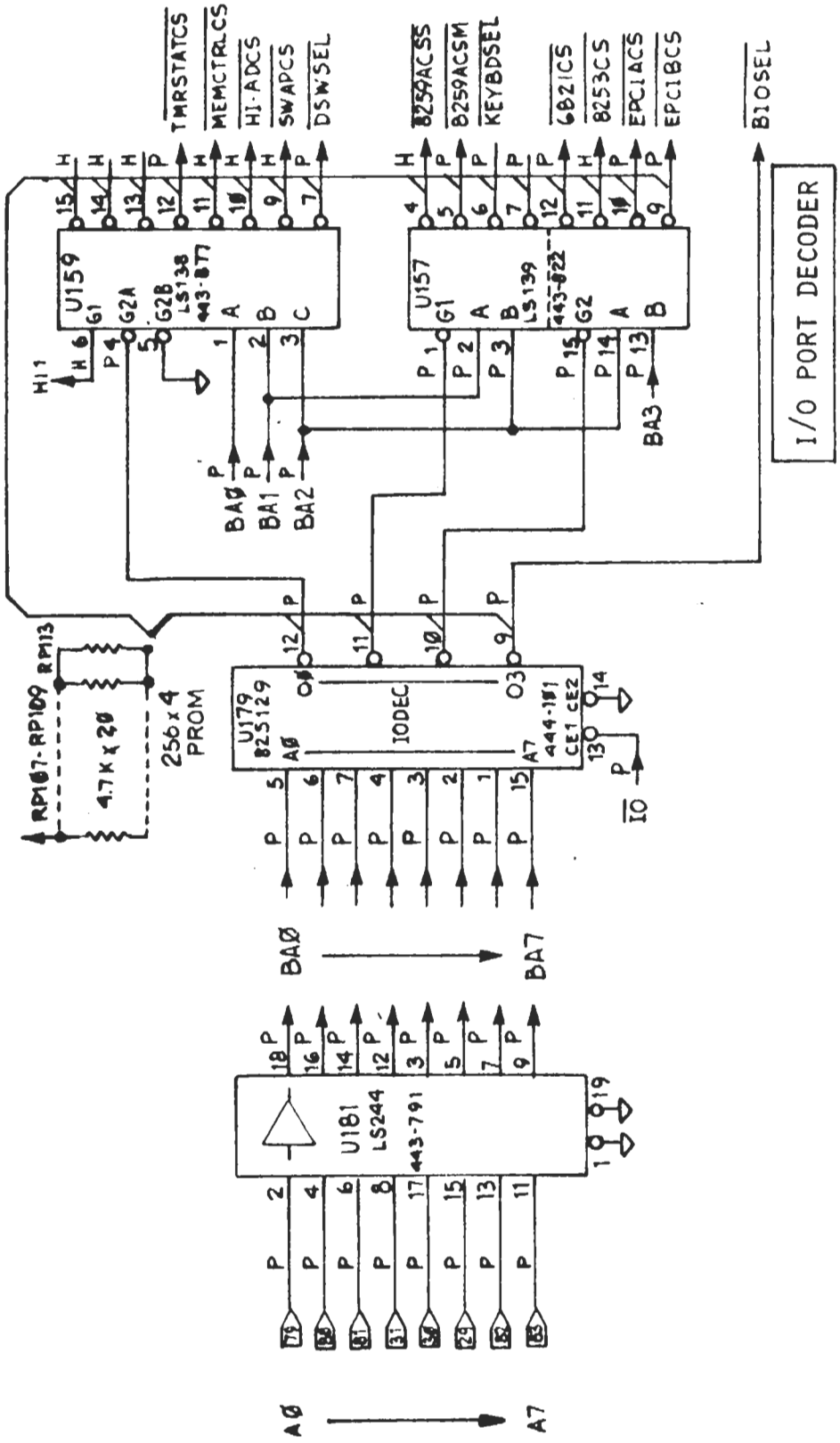
Configuration #4: MAPSEL1 = 1 MAPSEL0 = 1

In this configuration, 56K in bank 0 appears to be swapped with 56K in bank 1. Four kilobyte buffers above and below each 56K area remain unchanged, as does the top 64K bank. This configuration would permit using an extended BIOS when running CP/M-85.

Note that, in all cases, the memory only appears to be swapped from the memory's point of view. When the CPU addresses the swapped memory, the memory map decoder merely asserts a different RAS line than it normally would.

For example, assume that the H/Z-100 is operating in Configuration #4. If the CPU should write to the byte at the 6K location, U111 would assert $\overline{\text{REN1}}$ instead of $\overline{\text{REN0}}$. The memory at the 70K location will be written to. Bear in mind, however, that as far as the CPU (and the programmer) is concerned, the byte at 6K was written to.

Address lines BA12-BA15 allow the memory map decoder to keep some sections of memory in place--down to 4K increments.



I/O PORT DECODER (MB2)

PROCESSOR SWAP TESTS

SWAP TEST #1

1. Lift pin 5 of U186 (MB1).
2. Jumper U186-5 to ground.
3. Apply power and perform the following steps:

CHECK			IF NOT OKAY, CHECK
*S100-21	= L	(MB1)	U215-3
*U180-9	= L	(MB1)	U180-10
*U186-3	= H	(MB1)	U211-30
*U186-4	= L	(MB1)	U171-5

Go to Swap Test #2

U171-1	= L	(MB1)	U210-38
U171-5	= L	(MB1)	U171-1
U180-10	= L	(MB1)	U186-17
U186-3	= H	(MB1)	U211-30
U186-4	= L	(MB1)	U171-5
U186-16	= L	(MB1)	U186-3
U186-17	= L	(MB1)	U186-4
U186-18	= H	(MB1)	U186 is defective.
U187-2	= H	(MB1)	U186-18
U187-3	= P	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-5	= H	(MB1)	U187-2, U187-3
U187-9	= L	(MB1)	U187-10, U187-11, U187-12
U187-10	= H	(MB1)	U203-11
U187-11	= P	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12	= L	(MB1)	U186-3
U203-11	= H	(MB1)	U203-12, U203-13
U203-12	= L	(MB1)	U186-16
U203-13	= H	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.

U210-38 = L	(MB1)	U210-39
U210-39 = L	(MB1)	U187-9
U211-30 = H	(MB1)	U211-31
U211-31 = H	(MB1)	U187-5
U215-2 = L	(MB1)	Restore U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3 = L	(MB1)	U215-2

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SWAP TEST #2

1. Lift pins 4 and 5 of U186.
2. Jumper U186-4 and U186-5 to 5 volts.
3. Apply power and perform the following tests:

CHECK		IF NOT OKAY, CHECK
*S100-21 = H	(MB1)	U215-3
*U171-5 = H	(MB1)	U171-3, U171-2, U171-1
*U180-9 = L	(MB1)	U180-10

Go to Swap Test #3.

U171-1 = H	(MB1)	U210-38
U171-2 = H	(MB1)	U210-38
U171-3 = P	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U180-10 = L	(MB1)	U186-17
U186-3 = L	(MB1)	U211-30
U186-13 = H	(MB1)	U186-3
U186-16 = H	(MB1)	U186-3
U186-17 = L	(MB1)	U186-3
U186-18 = L	(MB1)	U186 is defective.

U187-2	= L	(MB1)	U186-18
U187-3	= P	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-4	= H	(MB1)	U203-11
U187-5	= L	(MB1)	U187-2, U187-3, U187-4
U187-9	= H	(MB1)	U187-11, U187-12
U187-11	= P	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U187-12	= H	(MB1)	U186-13
U203-11	= H	(MB1)	U203-13, U203-12
U203-12	= H	(MB1)	U186-16
U203-13	= L	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U210-38	= H	(MB1)	U210-39
U210-39	= H	(MB1)	U187-9
U211-30	= L	(MB1)	U211-31
U211-31	= L	(MB1)	U187-5
U215-2	= H	(MB1)	Restore U186-4 and U186-5 and go to CLOCK CIRCUITS TESTS.
U215-3	= L	(MB1)	U215-2

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SWAP TEST #3

1. Restore pin 4 of U186; leave pin 5 lifted.
2. Jumper U186-5 to ground.
3. Turn on the H/Z-100.
4. Connect a jumper wire from ground to pin 74 of the S-100 bus (HOLD*).
5. Perform the following tests:

CHECK			IF NOT OKAY, CHECK
*U180-9	= H	(MB1)	U180-10

Go to Swap Test #4.

U180-10 = H	(MB1)	U186-17
U186-13 = H	(MB1)	U186 is defective.†
U186-16 = H	(MB1)	U186 is defective.†
U186-17 = H	(MB1)	U186-13, U186-18

†NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

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SWAP TEST #4

1. Remove the jumper between ground and pin 5.
2. Connect the jumper from pin 5 to +5 volts.

CHECK		IF NOT OKAY, CHECK
*U180-9 = H	(MB1)	U180-10

End of tests.

U180-10 = H	(MB1)	U180-17
U186-13 = H	(MB1)	U186 is defective.†
U186-17 = H	(MB1)	U186-13, U186-18
U186-18 = H	(MB1)	U186 is defective.†

†NOTE: Before replacing U186, check the continuity between pins 6 and 15, and between pins 7 and 14. Also check for ground at pins 2, 8, 9, 10, 11, 12, and 19.

PARTS LIST

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U170	74ALS1020	HE 443-1081
U171	74ALS74	HE 443-1051
U172	74ALS74	HE 443-1051
U173	HAL14L4	HE 444-130
U174	74LS32	HE 443-875
U175	74LS10	HE 443-797
U176	74LS174	HE 443-879
U177	74LS240	HE 443-754
U178	74LS244	HE 443-791
U179	82S129 PROM	HE 444-101
U180	74LS367	HE 443-857
U181	74LS244	HE 443-791
U182	74LS14	HE 443-872
U183	74LS02	HE 443-779
U184	74LS156	HE 443-1036
U185	74LS14	HE 443-872
U186	HAL12H6	HE 444-128
U187	74ALS74	HE 443-1051
U188	74LS175	HE 443-752
U189	74LS08	HE 443-780
U190	2764 ROM	HE 444-87
U191	4.000 MHz oscillator	HE 150-132
U192	74LS169	HE 443-1054
U193	74LS367	HE 443-857
U194	7417	HE 443-72
U195	74LS240	HE 443-754
U196	74LS373	HE 443-837
U197	74LS373	HE 443-837
U198	74LS373	HE 443-837
U199	74LS156	HE 443-1036
U200	74LS368	HE 443-1024
U201	74LS125	HE 443-811
U202	74ALS74	HE 443-1051
U203	74LS86	HE 443-891
U204	8741A	HE 444-141
U205	74S74	HE 443-900
U206	74ALS02	HE 443-1045
U207	74LS14	HE 443-872
U208	8259A	HE 443-1012
U209	8259A	HE 443-1012

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS (CONTINUED)		
U210	8085A	HE 443-1010
U211	8088	HE 443-1009
U212	74LS273	HE 443-805
U213	74LS373	HE 443-837
U214	74LS244	HE 443-791
U215	74LS125	HE 443-811
U216	74ALS28	HE 443-1048
U217	74LS244	HE 443-791
U218	96LS02	HE 443-1040
U219	74ALS74	HE 443-1051
U220	74LS04	HE 443-755
U221	74LS32	HE 443-875
U222	74LS00	HE 443-728
U223	74LS244	HE 443-791
U224	74ALS28	HE 443-1048
U225	74ALS37	HE 443-1049
U226	74S288 PROM	HE 444-105
U227	74LS373	HE 443-837
U228	78L12 +12V regulator	HE 442-644
U229	79L12 -12V regulator	HE 442-646
U230	75189	HE 443-795
U231	75452	HE 443-74
U232	555 timer	HE 442-53
U233	74ALS74	HE 443-1051
U234	74ALS74	HE 443-1051
U235	74ALS10	HE 443-1047
U236	8284A	HE 443-1011
U237	74LS125	HE 443-811
U238	74ALS74	HE 443-1051
U239	74LS244	HE 443-791
U240	4.9152 MHz oscillator	HE 150-133
U241	74LS244	HE 443-791
U242	2661-2	HE 443-1061
U243	2661-2	HE 443-1061
U244	74LS244	HE 443-791
U245	75188	HE 443-794
U246	75189	HE 443-795
U247	75189	HE 443-795
U248	75188	HE 443-794

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CRYSTALS		
Y101	10.000 MHz crystal	HE 404-645
Y102	6.000 MHz crystal	HE 404-647
Y103	15.000 MHz crystal	HE 404-644
CONNECTORS - SOCKETS		
	8-pin IC socket	HE 434-230
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	24-pin IC socket	HE 434-307
	28-pin IC socket	HE 434-310
	40-pin IC socket	HE 434-253
	2-pin connector	HE 432-1171
	3-pin connector	HE 432-1102
	4-pin right-angle connector	HE 434-363
	9-pin right-angle molex connector	HE 432-1202
	10-pin connector	HE 432-903
	20-pin connector	HE 432-1227
	25-pin F right-angle "D" connector	HE 432-1195
	25-pin M right-angle "D" connector	HE 432-1194
	40-pin connector	HE 432-1062
	Jumper	HE 432-1041
	S-100 board edge connector	HE 432-1193
HARDWARE		
	#4 lockwasher	HE 254-9
	#4 nut	HE 252-15
	4-40 x 5/16" hex "D" spacer	HE 255-757
	4-40 x 5/16" black phillips-head screw	HE 250-1469
MISCELLANEOUS		
	PC board	HE 85-2653-1
	Wire, bare	HE 340-8
	Wire, blue wirewrap	HE 344-189
D101	1N5817 diode	HE 57-507
D102	1N4149 diode	HE 56-56
D103	1N4149 diode	HE 56-56
D104	1N4149 diode	HE 56-56
SW101	8-section slide switch	HE 60-621
X101	Audio transducer	HE 473-29

DISK CONTROLLER AND DRIVES

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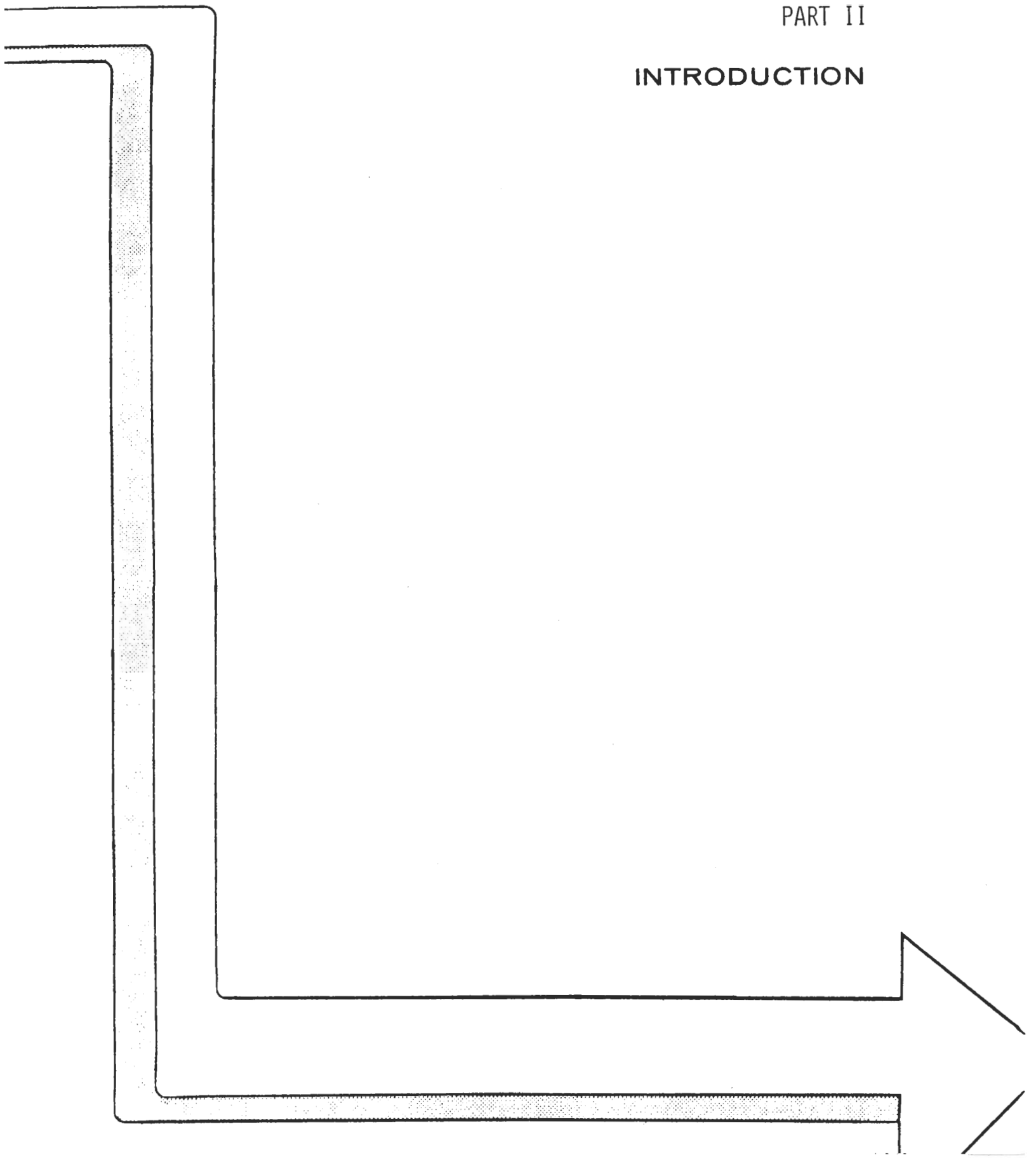
PART I

INTRODUCTION

PART II

INTRODUCTION



The H-207 is a floppy disk controller board. It functions as an intelligent interface between the CPU and the disk drives. The H-207 selects the correct drive in a multi-drive system and properly handles data transfer to and from the disk drives.

The H-207 operates as a slave processor. This means the disk controller board contains its own processor which is controlled by the master CPU. Thus, the disk controller board takes commands from the master CPU and converts them into the necessary signals required to control the drives. This type of system allows the master CPU to do other tasks while the disk controller board processor actually does the work of controlling the disk drives.

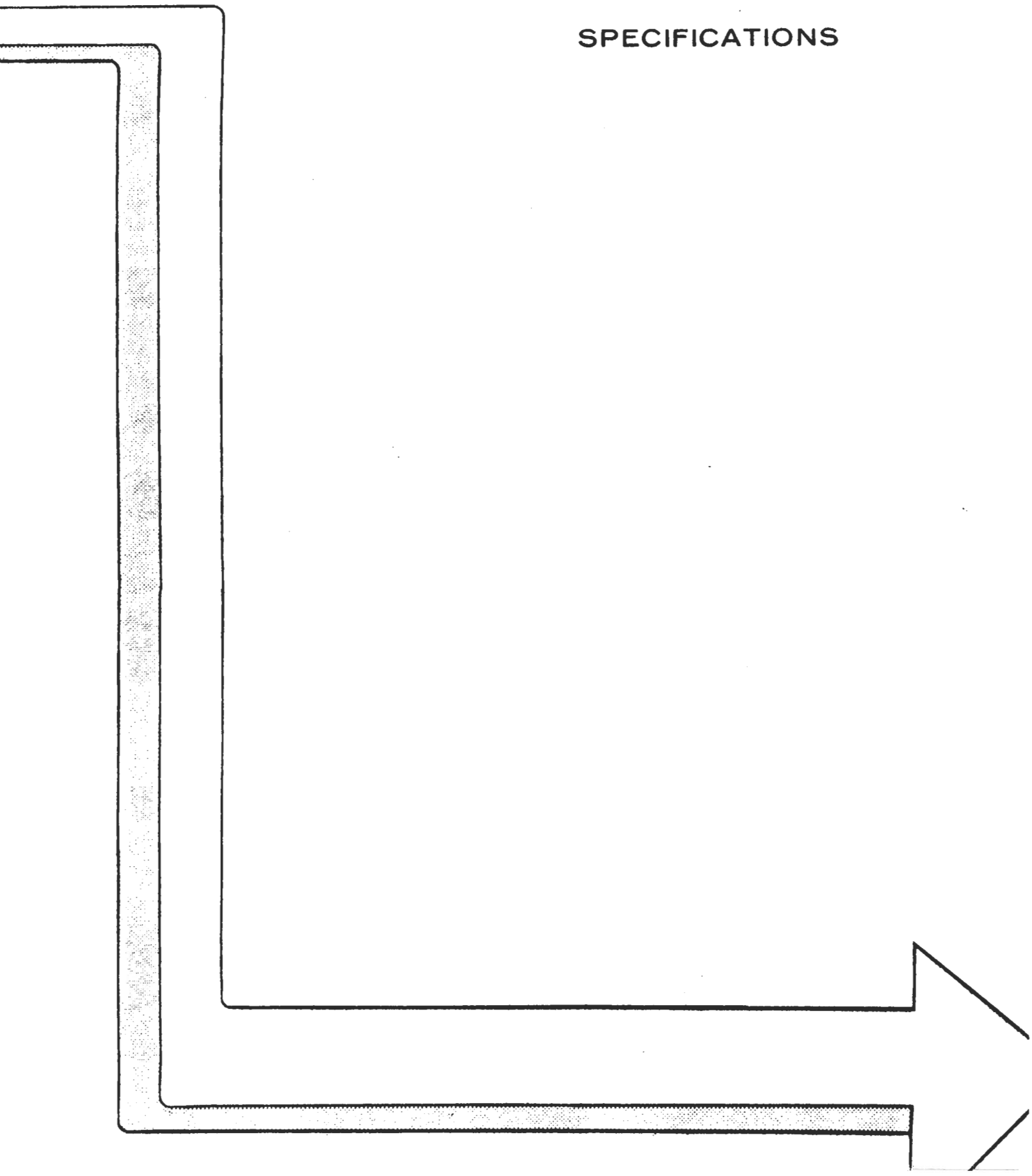
The H-207 is versatile. It can support up to four 5-1/4" and four 8" disk drives. User software selects the type of drive used and the density of the media. However, present Heath Company software limits the number of drives to three.

The H-207 can be operated in three different modes; Wait State, Polled I/O, or Interrupt. This allows the disk controller board to support almost all available soft-sectored disk formats. By using the Wait State mode, the board can be jumpered to operate at speeds up to 6 MHz.

Because the H-207 is a IEEE 696 Standard S-100 compatible card, it can be installed in other makes of computers using the IEEE Standard. Additional features that make the controller board acceptable to other computers are: user selectable addressing, software controllable formatting, Shugart compatible 8" interface, and adjustable precompensation.

The information provided in this section of the manual will familiarize you with the operation and troubleshooting of the H-207. Using this information, you will be able to troubleshoot the disk controller board to the component level.

SPECIFICATIONS



Type	WD1797.
Drives Supported	Up to four each.
5-1/4"	Single/double-sided, 48/96 TPI, single/double density.
Capacity (formatted) ...	80K, 160K, 320K, or 640K; depending on the number of sides and density.
Track Format	4K, eight sectors of 512 bytes each.
Stepping Speed	6 milliseconds per track or faster.
8"	Single/double-sided, single/double density.
Interface type	Shugart 850 or equivalent.
Data Separator	Phase-locked loop.
Precompensation	Variable independently for both 5-1/4" and 8" sizes.
Data Transfer	Programmed using wait states, interrupt or polling.

OPERATION

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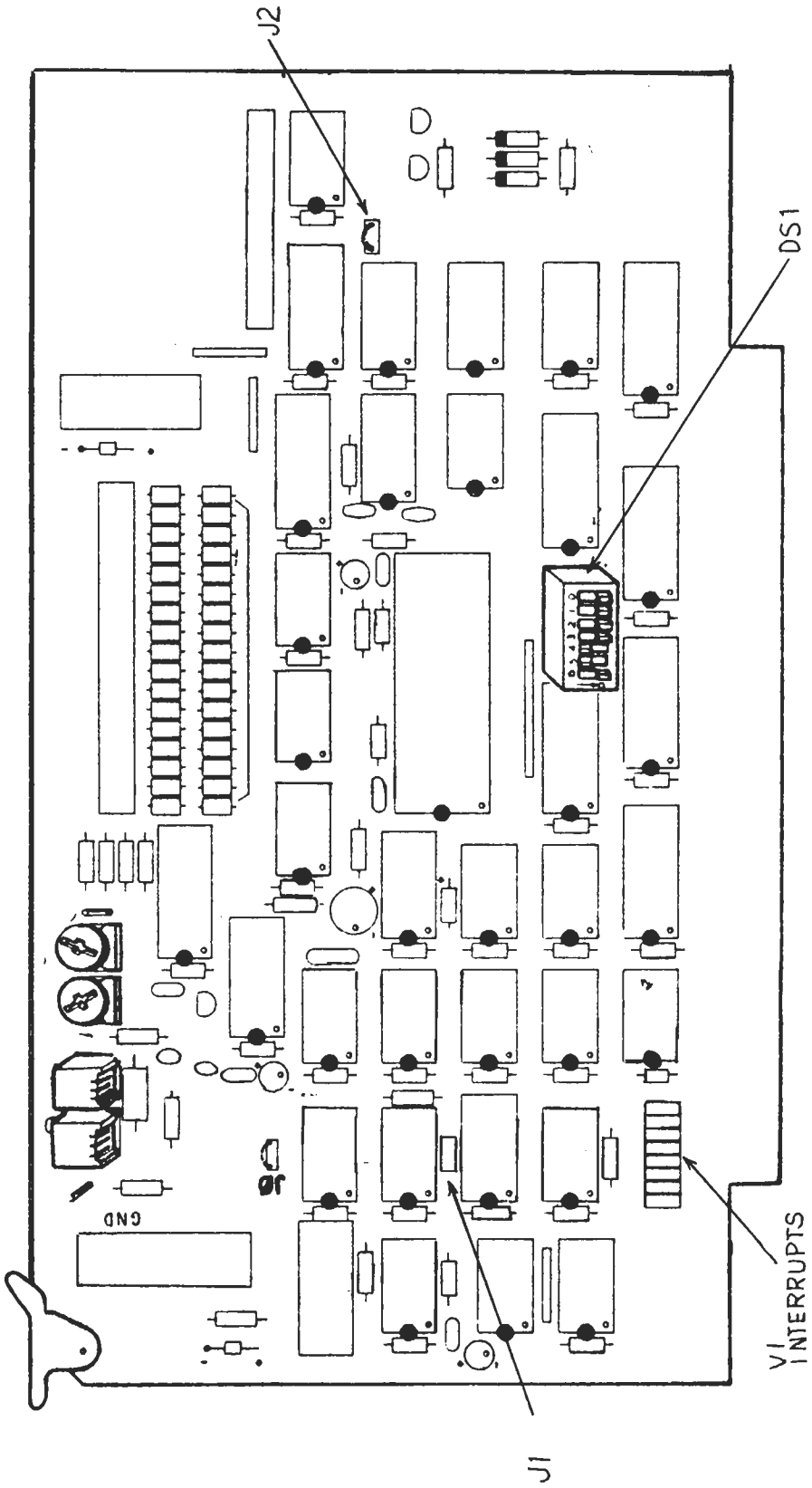


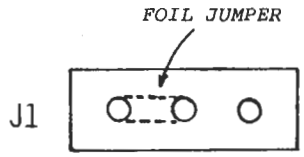
H-207 CONTROLLER BOARD
JUMPER AND SWITCH LOCATIONS

INTRODUCTION

To permit the H-207 to operate in many different types of computers, a number of jumpers and a slide switch are incorporated into the design of the board. These devices permit configuring the controller board for the computer environment in which the H-207 is installed. There are three main areas of concern: clock speed jumpering, selection of interrupt jumpers and the setting of the slide switch, DS1. Refer to the pictorial on the adjacent page for the location of the jumpers and the slide switch.

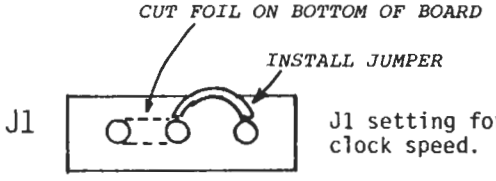
CLOCK SPEED

The host computer clock speed that the H-207 will operate with is determined by the jumpering at J1. As received, J1 is jumpered by a foil run on the bottom of the board. (See illustration below.) This jumpering enables the H-207 to operate in computers that have a CPU clock speed faster than 3 MHz. This jumpering is normal when the H-207 is installed in a H/Z-100.



J1 set for H/Z-100 Computer operation or for CPU clock speeds faster than 3 MHz.

For the H-207 to operate in a computer that has a CPU clock speed at or slower than 3 MHz, the jumpering of J1 must be altered. This is accomplished by cutting the foil jumper on the bottom of the circuit board and installing a 1" wire jumper from the middle hole of J1 to the rightmost hole. Refer to the illustration below when performing this alteration.



J1 setting for 3 MHz or slower CPU clock speed.

INTERRUPT JUMPERS

The Vectored Interrupt jumper locations, VI, are located on the lower left-hand corner of the controller board. The data request line, DRQ, from the 1797 is connected to holes J3 through J10 shown in the illustration below. The center row of holes numerically correspond with the S-100 interrupt lines VI0 through VI7. The interrupt request line, IRQ, from the 1797 is connected to holes 0 through 7. When jumpered, these locations route IRQ and/or DRQ from the 1797 controller to the S-100 interrupt lines.

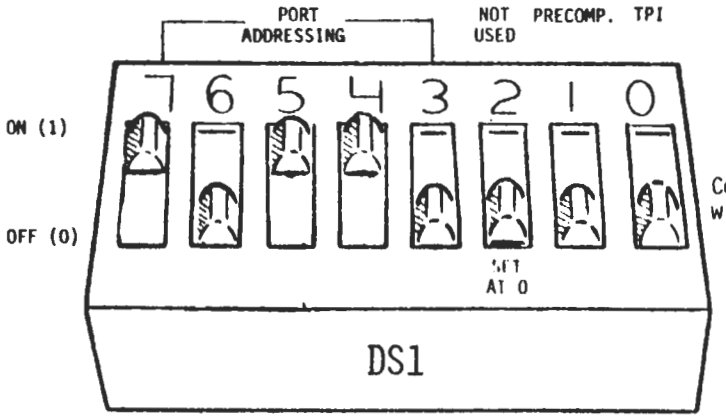
No jumpers are installed in these locations when the H-207 is used in a H/Z-100. These jumper locations are only used when the H-207 is installed in computers that require interrupt protocol. The configuration of the jumpers is determined by the customer's computer documentation.

VI

VECTOR INTERRUPT JUMPER LOCATIONS
(No jumpers are installed for H/Z-100 operation.)

SLIDE SWITCH (DS1)

DS1, an 8-section slide switch, determines the port address and the condition of bits 3 and 4 of the status port. The sections of DS1 are defined as follows:



Configured for an H/Z-100 Computer with 48 TPI, 5-1/4" Drives

DS1

HEATH SOFTWARE DEFINED		HARDWARE DEFINED	
Section	Definition	Section	Definition
0	This bit determines the TPI of the 5-1/4" disk drive. 0 = 48 TPI. 1 = 96 TPI.	0	Status port bit 4.
		1	Status port bit 3.
		2	Not used. Leave at 0.
		3-4-5-6-7	Port addressing (MSB).
1	This bit determines whether precomp is on or off. 0 = precomp off. 1 = precomp on.		
2	Not used.		
3-4-5-6-7	Port addressing.		

The H-207 occupies a block of eight contiguous I/O port addresses. The three low-order bits in this block select 1797 registers, the control latch, or the status port. The H/Z-100 computer series place the H-207 at port address B0H. A map of the I/O port is shown below.

I/O ADDR. (Binary)	READ	WRITE	PORT DESIGNATION
SSSSS000*	•		1797 Status Register
SSSSS000		•	1797 Command Register
SSSSS001	•	•	1797 Track Register
SSSSS010	•	•	1797 Sector Register
SSSSS011	•	•	1797 Data Register
SSSSS100		•	Control Latch
SSSSS101	•		Status Port

* S = dip switch bit

The dip switch bits are simply defined from the binary equivalent of the switches. For example, the port address for the H/Z-100 is shown below.

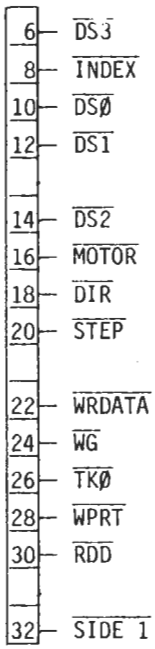
SSSSSXXX** = 10110XXX = Port B0 - B7.

** X = 1797 register, control latch, or status port.

OUTPUT CONNECTORS

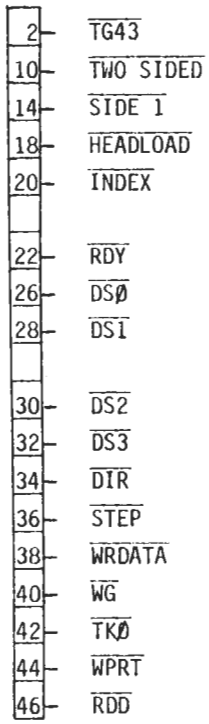
5" DISK DRIVE CONNECTOR (P2)

This 34-pin connector provides the necessary signals to drive a 5-1/4" disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All numbered pins are grounded.



8" DISK DRIVE CONNECTOR (P1)

This 50-pin connector provides the necessary signals to drive an 8" Shugart compatible disk drive. Refer to the pictorial at the left for a description of the pinouts of this connector. All odd numbers pins are grounded.



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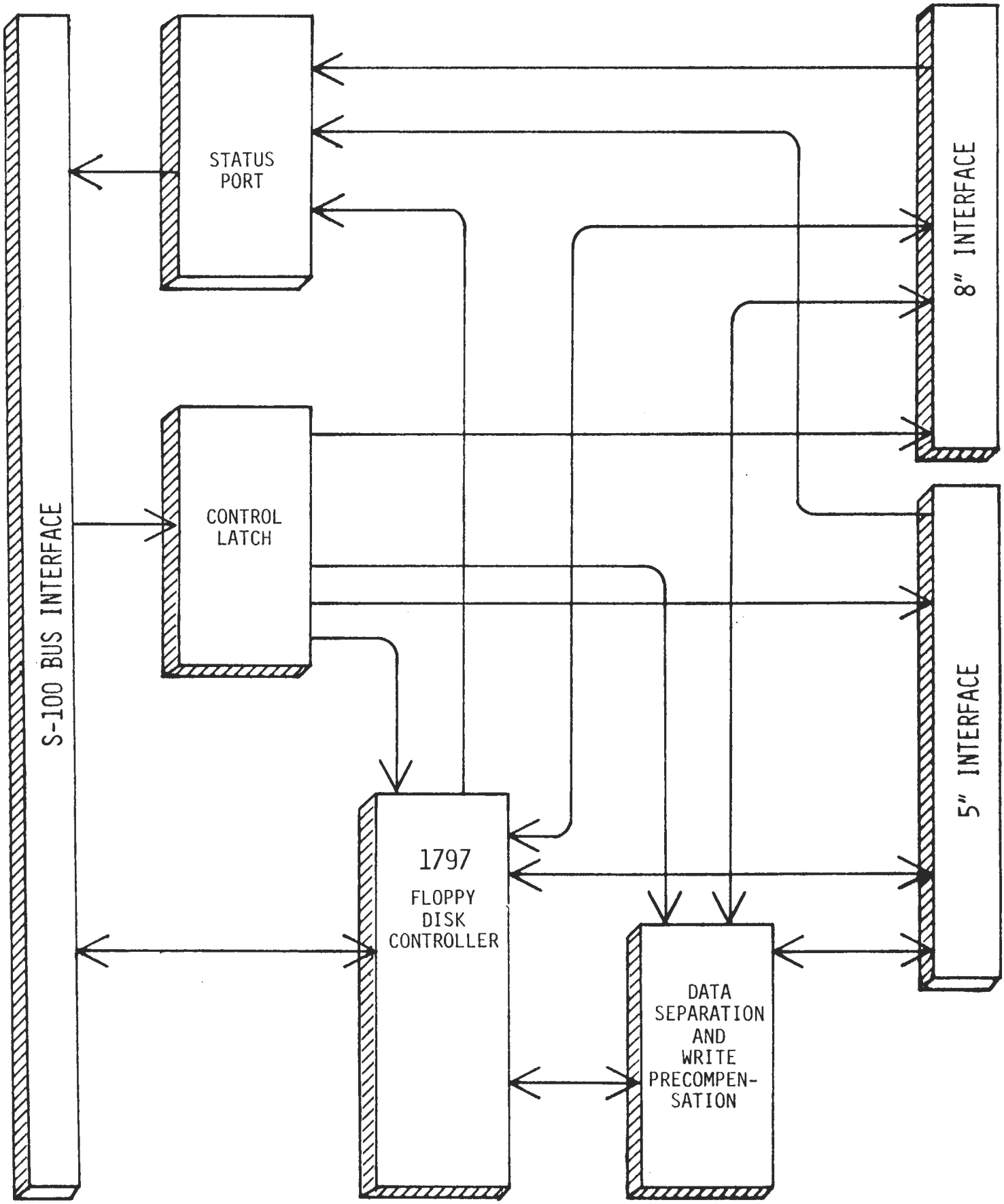

H-207 BLOCK DIAGRAM

BLOCK DIAGRAM DESCRIPTION

Refer to the H-207 block diagram as you read the following.

The H-207 Floppy Disk controller board consists of seven major sections: the bus interface, the status port, the control latch, the 1797 floppy disk controller, the data separation & write precompensation circuits, and the two drive interfaces.

The bus interface is made up of two octal bus buffers, an octal tri-state latch, an address comparator, and some miscellaneous enabling circuitry. These components interface the H-207 to the S-100 bus in the H/Z-100.

The status port is a read-only device that tells the CPU the status of the disk drives and the controller. This includes track density, number of recording sides to the disk, and if precompensation is being used.

The control latch accepts commands to the disk drives such as DRIVE SELECT, 5" FASTEP, and others that have to do with the selection and mode of the drives.

The 1797 controller controls the placement of information on the diskette. That is, the movement of the drive head, the formation of written data, and the separation of the read data is controlled by the 1797.

The data separation and write precompensation circuitry control how the data is read to or written from the diskette. It does this by separating the data from the clock signal during read operations and precompensating data during the double-density write operations.

The 8" and 5.25" drive interfaces include buffers and filter circuitry. Up to four drives can be connected to each interface.

DETAILED CIRCUIT DESCRIPTION

S-100 BUS INTERFACE

The S-100 Bus Interface is compatible with any IEEE 696-standard S-100 Bus. See the S-100 specification sheets in the appendices of this manual for definitions of the lines.

DATA IN

Data into the bus (out from the controller board) travels through signal lines 91-95 and signal lines 41-43 on the bus interface. These pins are used in read operations from the status latch or from the 1797 controller. The data is buffered from the board's internal data bus to the S-100 bus by means of U36, a 74LS244 buffer.

DATA OUT

Data out from the bus (into the controller board) travels through pins 35, 36, 38, 39, 40, 88, 89, and 90 on the bus interface plug. This data is latched by tri-state latch U35. The latch is used because data on the S-100 bus is not present long enough for the 1797 to receive properly. The tri-state latch holds the data on the board's internal data bus so that the 1797 can read it. Valid data is latched in U35 on every write cycle. The latch is enabled through pin 1 when the ALE (Address Latch Enable) signal latches an asserted sOUT (Status Out) signal via U20.

ADDRESS LINES

The address lines from the bus enter the board through pins 29, 30, 31, 79, and 80 through 83 of the bus interface. They are buffered by the 74LS244 chip, U34.

CONTROL LINES

The control lines from the S-100 bus enter the board through pins 24, 25, 45, 46, and 75 through 78 of the bus interface. These lines are buffered by U33.

VECTOR INTERRUPT LINES

The vector interrupt lines from the bus enter the board at pins 4 through 11 of the bus interface. They may be driven by U32.

READY LINE

The ready line, RDY, enters through pin 72 of the bus interface. It is driven by U32. The controller board uses this line to put the CPU in a wait state during some operations to give the controller time to finish the operation.

RESET CIRCUITS

POWER-UP/RESET

On power up, the CPU sends RESET* through the S-100 bus to the H-207 board. This places the 1797 controller, the control latch, the write precompensation control, and the U26 flip-flops in a known state before the CPU accesses the board.

In the 1797, the reset line sets the command register at 03H, the sector register to 01H, and bit 7 of the status register (Not Ready bit) to logic zero.

After the reset line goes high, the 1797 executes the restore command. The drive read/write head seeks track 0 and sends an interrupt to the computer once the track is found. See the 1797 IC data sheets for more details.

The reset line connects to pin 1 of the control latch, U30, to clear all of the outputs.

The reset state of the phase lock loop control, U1, makes the phase four (ø4) input equal to 0 (see the 1691 IC data sheets).

Finally, the U26 Q-outputs are made equal to 1; pin 9 sends an RDY (ready) signal to the CPU and pin 5 provides part of the qualification needed for read/write enabling through U27-11.

POWER-UP WRITE PROTECTION

On power up, the TTL circuits will be at an undefined state until the power supply voltage rises above 4 volts. This could generate a write command in the drives and damage any disks that may be installed.

To protect the disk, the WG (write gate) output from the 1797 is coupled to the 5" and 8" drives through Q3 and Q2. These transistors are biased by R25, D3-D1, and R24 to remain cut off until the power supply voltage is at or above 4 volts. When the supply reaches this value, Q2 and Q3 are biased near their operating region and will conduct whenever WG is asserted.

CPU/CONTROLLER LOGIC

Reading and writing in the H-207 board involves three types of information: data which can be read or written, status signals, and control signals. Status signals can only be read and control signals can only be written.

READ STATUS LATCH (U31)

Assume a status signal needs to be read. There are two sources of status information for the S-100 bus, the status port at U31 and the 1797 status register in U22.

To read from the status port, the CPU selects the H-207 by placing the address of the board on the address lines, A0-A7. Lines A3-A7 are checked by the address comparator, U29, for the proper address. The proper address is defined by the user by setting DIP switch DS1. If the address is correct, the EOUT signal pin 19 asserts.

The EOUT signal is gated through U28-13 by I/O at pin 12. I/O asserts on a data transfer between the CPU and an I/O port. If I/O is low, indicating that the sINP signal or sOUT signal is asserted, then the simultaneous assertion of EOUT and I/O signals sends a logic one to U20-2. This logic one is latched onto pin 5 when ALE (address latch enable) asserts. ALE, derived from pSTVAL* and pSYNC, goes high when the H-207 port address is stable.

The Q output of U20 is NANDed with pDBIN from the S-100 bus to form $\overline{\text{RDME}}$ at U27-8. This line goes low to indicate that the H-207 board is being read by the CPU, and activates the status latch, U31-1.

The status latch still can not be read until the status port select line (STPS) is asserted at pin 15 of U31. This line comes from U17-14, the I/O address decoder.

The I/O address decoder activates STPS by decoding the address lines A0, A1, and A2. If A0 and A1 are low and A2 is high, and if BDSEL or board select is active, then U17's Y1 line goes low. This causes U31 to place the status word onto the board's internal data bus, where it is buffered by U36 to the S-100 bus.

The organization of the status latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0	INTRQ	0 = no interrupt request	1 = interrupt request from 1797
1	MOTORON (5")	0 = spindle motor not running	1 = spindle motor running
3	96TP1	0 = 5.25" drives are 48 TPI	1 = 5.25" drives are 96 TP1
4	PRECOMP	0 = 5.25" drives do not need precomp	1 = 5.25" drives need precomp
6	TWOSIDED	0 = 8" diskette not two sided	1 = 8" diskette two sided
7	DRQ	0 = not ready for data transfer	1 = ready for data transfer

READ STATUS REGISTER OF 1797 (U22)

Assume now that the 1797's status register is to be read. The procedure is the same as described previously, except that address lines A0, A1, and A2 are low. Because the address bits A0-A2 are different, the I/O address decoder, U17, does not enable the status latch, U31. Instead the status register of the 1797 is selected and read onto the data bus.

WRITE CONTROL LATCH (U30)

The control latch, U30, is written at the falling edge of CLEN, which is the simultaneous assertion of pWR and the Y0 output of the I/O address decoder. The pWR signal comes directly from the CPU, and the Y0 signal occurs when A0, A1, and A2 are high, low, and high, respectively. The Y0 and pWR signals are ORed at U21-6 to form CLEN.

The organization of each bit in the control latch is as follows:

BIT	SIGNAL NAME	FUNCTION	
0,1	DSA, DSB	00 = select drive 1 01 = select drive 2	10 = select drive 3 11 = select drive 4
2	8"/5"	0 = select 5.25"	1 = select 8"
3	DSEN	0 = deselect all drives	1 = select drive specified by bits 0, 1, and 2
4	PRECOMP*		
	5.25" DDEN	0 = precomp all tracks	1 = disable precomp
	8" DDEN	0 = precomp all tracks	1 = precomp tracks 44-76
5	5" FASTEP	0 = 1797 operates as specified by bit 2	1 = 1797 operates in 8" mode
6	WAITEN	0 = wait state enable	1 = wait state enable
7	SDEN	0 = double density	1 = single density

*(Note: Precomp is disabled in single density.)

When the WAITEN bit in the control latch is asserted, a wait state is intitiated on the next read or write of the data register. WAITEN couples through U23, U26, and U32 to the S-100 RDY line. RDY goes low to put the CPU in a wait state until the disk controller asserts DRQ at U22-38.

Upon DRQ becoming active, an additional delay is needed to fulfill the access time requirements of the 1797 Controller. The access delay and synchronization to the S-100 Bus are both accomplished by counting system clocks. An on-board jumper selects whether one system clock is counted (for systems with clocks up to 3 MHz) or two system clocks are counted (for systems with clocks up to 6 MHz). For operation at less than 3 MHz, jumper J1 (near U19) should be jumpered between F and G. For operation between 3 and 6 MHz, this jumper should be between F and E (normal position for the H/Z-100).

At the completion of the access delay, the wait state is cleared. RDY is asserted, and the CPU completes the read or write of the data register in the 1797. A RESET or an INTRQ signal also clears the wait state, so that the CPU does not hang up after an error during a disk access.

WRITE COMMAND REGISTER IN THE 1797 (U22)

The command register in the 1797 can be written when A0, A1, and A2 are all low. The FDWR signal at U22-2 is asserted when both FDEN and pWR* are logic zero. The signal pWR comes directly from the CPU, while FDEN is a composite signal made up of FDSEL and U26-5. The output of U26-5 is the signal that starts the access of the 1797 controller at the end of the wait state.

DATA READ/WRITE OPERATIONS

During a data write operation, the controller board is enabled by the proper address and by pWR*. After the proper control words are sent to select the proper drive, address lines A0 and A1 are made high and A2 is made low. This connects the data register of the 1797 to the internal data bus. As long as A0 and A1 are high and A2 and FDWR are low, the data from the S-100 bus will go to the 1797 data register and be shifted out serially on pin 31, the write output line. Also, on pin 31, clock pulses are inserted between each bit.

The track and sector registers in the 1797 determine where the data is to be written to on the disk. Whenever a sector is filled with data, software determines the next sector to be written to by making the A0 and A1 signals equal to 0 and 1, A2 equal to 0. Software then writes the sector number to the sector register and the track number to the track register.

The 1797 translates the track numbers into the proper step and direction commands to the drive.

A read operation requires the board to be enabled as described earlier. However, the I/O address decoder does not enable the status latch because the address provided by the CPU is not correct for a status read from the latch. Instead, the address lines causes the 1797 to dump the bits in its data register onto the internal data bus of the H-207, which connects to the U36 buffer and the S-100 bus.

The 1797 fills its data register from the data shift register, which fills serially from the RAWREAD data stream at U22-27. See "Data Separation and Precompensation" for a discussion on RAWREAD data processing.

RDY DELAY

U19 is a quad flip-flop that acts as a delay line for the DRQ signal from the 1797 to the S-100 RDY line. The input at U19-4, D1, is output at Q1 after one clock cycle. Q1 is tied to D2 and is output to Q2 after another clock cycle. Q2 is also tied to U25-1 and D3.

From U25-12, the D2 signal presets flip-flop U26. Flip-flop U26 qualifies the FDSEL signal to enable read/write operations in anticipation of the RDY line being made active.

From D3 of U19, the delayed DRQ signal is output to Q3, which is connected to D4 and to jumper J1, post G. Post G is connected to post F in 3 MHz operations, which do not need additional delay of the DRQ signal. Instead, the output of Q4, which contains the DRQ signal delayed by three to four clock cycles, is connected to jumper J1, post E. For 6 MHz operation, J1 is connected between post E and post F.

INTERRUPTS

There are two interrupts that the H-207 board can make. They are the interrupt request (INTRQ) and the data request (DRQ). Both of these interrupts originate from the 1797. The INTRQ signal is sent to indicate a command completion or an error. The DRQ signal is sent to indicate data will be accepted in response to a disk read or write command.

The interrupts can be detected two ways, as either a vectored interrupt on any of the bus interface pins from 4 to 11, or as a bit set in the status port, U31, which can then be polled by the CPU.

The INTRQ signal pulls the bus out of a wait state caused by a logic zero at U26-9. When pin 39 of the 1797 asserts, it is inverted at U25-6 to set pin 9 of U26.

CONTROLLER/DISK-DRIVE LOGIC

DATA SHAPING

Data pulses to the drive are reshaped by U16, a one-shot multivibrator, to 400 ns. Raw data from the drive are reshaped to 250 ns.

DATA SEPARATION AND PRECOMPENSATION

Data separation and precompensation are performed primarily by U1, U3, U4, U5, and U22. The data separation circuits are used when the controller is receiving data from the disk drive, while the precompensation circuits are used when the controller is writing data to the disk.

DATA SEPARATION

$\overline{\text{READDATA}}$ ($\overline{\text{RDD}}$) from the drive couples through U9 and U16 to U1-11 and U22-27 ($\overline{\text{RAWREAD}}$). $\overline{\text{RDD}}$ contains both data bits and clock bits. U1 extracts the clock bits and sends them to U22-26 as RCLK. These pulses are synchronized with RDD. The 1797 uses the RCLK signal to extract the data bits from the $\overline{\text{RAWREAD}}$ stream. U22 then formats the data and sends it to the CPU.

U1 uses a phase-locked loop to keep RCLK in phase with the incoming data stream. The phase-locked loop consists of U5, U4, U13, and U1. U5 is a 4-MHz voltage-controlled oscillator that drives U4 and U13. U4 and U13 select either 4 MHz or 2 MHz, depending on the disk size. If a 5-1/4" disk is being read, U4-9 is low. This couples the 2-MHz signal to U1-16. Four megahertz is coupled to U1 for 8" drives.

If the phase of RCLK should drift with respect to the incoming $\overline{RDD}$ signal, U1 will send feedback pulses from U1-13 or U1-14 to the VCO at U5. These pulses will increase or lower the VCO frequency. In turn, the VCO frequency will increase or decrease the RCLK frequency until it again in phase with RDD. Here's how:

> If the frequency of $\overline{RDD}$ is higher than RCLK, then $\overline{RDD}$ will go low at the beginning of RCLK. The pump-up output (PU) at U1-13 will go from a high-impedance state to a logic one. This increases the VCO frequency which increases frequency of RCLK.
>
> If the frequency of $\overline{RDD}$ is lower than RCLK, then $\overline{RDD}$ will go low at the end of RCLK. The pump-down output ($\overline{PD}$) responds by going from a high-impedance state to logic zero. This decreases the VCO frequency and thus decreases the frequency of RCLK.
>
> If RCLK and $\overline{RDD}$ are in phase, then PU and $\overline{PD}$ are in a high-impedance state and the VCO frequency remains constant.

Pins 5, 7, and 8 of U1 allow the 1797 to control clock separation and data recovery. When pins 7 and 8 are low, the data recovery circuits are enabled. If pin 7 is high, which happens during a write operation, then the data recovery circuits are disabled.

Pin 15, DDEN, controls the frequency of RCLK. When pin 15 is logic one, the frequency of RCLK is equal to the VCO frequency divided by 16. When pin 15 is logic zero, RCLK is equal to the VCO frequency divided by 8.

DATA PRECOMPENSATION

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. Error is introduced by the shifting of old data that is adjacent to new data being written. This shifting is due to the nature of the magnetic fields on the disk (like fields repel).

The precompensation circuits consist of U22, U1, and U3. U22 sends the write data from pin 31 to U1-1. U3 provides delay timing for the write data in U1. U22 selects the amount of precompensation by setting the logic levels on pin 18 (LATE) and pin 17 (EARLY).

Here's what happens...

When the 1797 sends a data bit to U1-1, the strobe line at U1-5 latches high. This triggers U3-11 and causes a negative-going pulse to ripple through $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, and $\overline{\phi 4}$. R3 sets the pulse width of these signals and, therefore, the amount of precompensation.

With no precompensation (EARLY = LATE = 0), the data pulse is coupled to U1-6 at $\overline{\phi 2}$ time. If LATE precompensation is selected, the data bit leaves U1-6 at $\overline{\phi 3}$ time. EARLY precompensation synchronizes the data bit to $\overline{\phi 1}$.

When $\overline{\phi 4}$ pulses low, it couples through U7 to U1-19 to clear the strobe at U1-5 in anticipation of the next write data pulse.

Precompensation must be enabled for double-density operation. The CPU does this by setting U30-19 to logic one and sending it to the DDEN input at U1-15. The CPU also asserts the $\overline{\text{PRECOMP}}$ line at U30-12. This couples through U6-8 to TG43 at U1-9. TG43 must be high before precompensation can take place.

Even if $\overline{\text{PRECOMP}}$ isn't asserted, the write data should be precompensated on the inner tracks, where the data is packed closer together. This condition is taken care of by U22-29, which asserts on tracks greater than 43. The TG43 signal couples through U6-8 to the TG43 input of U1.

HEAD LOAD TIMING

The single-shot multivibrator at U15 provides read/write head-load timing. When the 1797 sends a head-load command, pin 28 goes high to load the drive head and to trigger U15.

U15-7 goes low for about 50 mS. This signal couples to U22-23 to prevent a data read or write until U15 times out. This delay compensates for bounce when the read/write head contacts the disk surface.

1797 TIMING

U18, U12, U14, and U30 provide timing and control of timing to the 1797. Depending on the state of U14, the clock frequency to U22-24 will be either 1 MHz or 2 MHz.

The operating frequency of the 1797 is automatically switched from 1 MHz to 2 MHz when changing from 5-1/4" drives to 8" drives. This is done by U30-6 and is coupled through U7-11 to the latch at U14.

One drawback of the 1797 is that it won't allow 5-1/4" drives to step at a 3-mS rate during track seek. To circumvent this problem, U30-15 sets the 5" FASTSTEP signal. This signal couples through U7-12 to U14. U14 increases the operating frequency to 2 MHz to speed up the step rate. At the end of the track-seek function, the clock frequency is reduced to 1 MHz again for normal 5-1/4" operation.

8" DRIVE INTERFACE

The 8" drive interface is through P1. All output signals to the drives are buffered through U8 and U10 except WG and HLD. The WG signal is sent through transistor Q2, as described previously. The HLD signal is inverted by U7-10 before being transmitted to the drives.

All input signals except READY and TWOSIDED are buffered through the upper section of U9 when enabled by a high on the 8"/$\overline{5}$" line. The READY signal is inverted at U6-6, while the TWOSIDED signal is inverted at U6-11.

5" DRIVE INTERFACE

The 5" drive interface is through P2. All output signals to the drives are buffered through U10 and U11 except WG and MOTOR. The WG signal is sent through transistor Q3, as described previously. The MOTOR signal turns on the disk drive motor whenever a logic zero is present at pins 9, 10, 12, and 13 of U23. The single-shot at U15 keeps the drive motor on for about 20 seconds after the disk access is complete. This provides a proper turn-off delay.

All input signals are buffered through the lower section of U9, which is enabled by a low on the 8"/$\overline{5}$" line.

CALIBRATION CIRCUIT BOARD

The calibration circuit compares the end of the write pulse with a narrow pulse of a known delay. When the two happen simultaneously, the LED on the calibration board is latched on. This indicates that the length of the write pulse is properly adjusted.

The write pulse coming from CP3 is applied to NAND gate U501D. U501D inverts the pulse and applies it to inverter U501C and to delay line DL501. Within DL501 the pulse is delayed 120 nS between pins 1 and 10 and 160 nS between pins 1 and 6. These two delayed pulses are then compared by NAND gates U501A and U501B. The result of the comparison is a pulse 40 nS wide and 120 nS delayed in reference to the write pulse.

If the write pulse has been adjusted for a 120 nS pulse width, the write pulse at the D flip-flop U502B-11 will go high when the 40 nS delayed pulse is low. This condition causes U502B to latch a low on the Q output, U502B-9. A low at this point turns on the LED, D501.

By adjusting the precompensation controls into this 40 nS "window", it is possible to "tune" write precompensation to be not only between 120 and 160 nS, but also much closer to 120 nS than 160 nS.

To gain additional delay for greater write precompensation, DL502 (optional HE 41-10) can be added to the circuit. DL502 provides four additional delay taps with an additional 40 nS of delay per tap.

H-207 FLOPPY DISK CONTROLLER BOARD DEFINITIONS

A0-A7	Address bits.
ALE	Address latch enable. Data and address lines from the CPU have valid information.
BDSEL	Board select. The H-207 board is selected (enabled).
CLK	Clock signal.
CS	Chip select. When asserted, the 1797 chip is enabled.
DØ-D7	Data bits on the H-207 board's internal data bus.
DDEN	Double density enable.
D1Ø-D17	Data-in bits on the S-100 bus ("in" with respect to the CPU, not the Controller).
DIR	Direction of drive head. When high, the drive head is stepping in. When low, the drive head is stepping out.
DOØ-DO7	Data-out bits on the S-100 bus ("out" with respect to the CPU, not the Controller).
DRQ	Data request. The 1797 data register needs data for write operations or the register has data for read operations.
DSA	Drive select A. Used with DSB to address the drives.
DSB	Drive select B. Used with DSA to address the drives.
EARLY	Write data bit early to disk drive (used for precompensation).
HLD	Head load.

HLT	Head load timing. The drive head is engaged when this signal is high.
INDEX	The index hole on the diskette has been detected.
INTRQ	Interrupt request. H-207 board has input for the CPU.
LATE	Write data bit late for drive precompensation.
MR	Master reset pin on the 1797 Controller chip that sets all registers in the chip to a known state.
pSTVAL*	Status valid.
pSYNC	New bus cycle may begin.
PD	Pump down. Decreases the frequency of the raw read data tracking clock.
PRECOMP	Enables precompensation when low.
PU	Pump up. Increases frequency of the raw read data tracking clock.
pWR	Valid data is on data-out bus (write bus).
RAWREAD	Unprocessed data from the drive.
RCLK	Clock that separates data from drive data and clock stream.
RDD	Data and clock stream from the drive.
RDME	Data or status signals input for the bus are enabled.
RDY	Slave aboard is ready. (H-207 board is a slave board.)
RE	Read enable. Enables the 1797 chip for read operations when low.
READY	The 8" disk drive is ready.

RESET	Reset signal.
SIDE1	Otherwise known as side select output. When high side 1 is selected in the drive. When low, side 0 is selected.
sINP	Status signal signifying data input to the bus (read cycle) may occur.
sOUT	Status signal signifying data output from the bus (write cycle) may occur.
STEP	Steps the drive head one step per pulse.
STB	Strobe output from the 1691 (U1) phase lock loop control.
TG43	Track greater than 43. The drive read/write head is over or past track 43 (track of mandatory precompensation in double density 8" drive.
TKØ	Track 0. The drive read/write head is over track 0 on the diskette.
TWOSIDED	The 8" drive is set for two-sided operation with a two-sided diskette.
VFOE/WF	VFO enable/write fault. When WG is asserted, VFOE/WF flags write faults when deasserted, terminating any write commands. When WG is deasserted, VFDE/WF enables the data separator in the 1691.
V1Ø*-V17*	Vector interrupts.
WAIT	RDY line is low (not ready).
WAITEN	Wait enable. Set RDY line low on all accesses of the 1797 data register.
WD	Write data. Contains the data to be written onto the diskettes as well as the clock signals.
WDIN	Write data into the 1691 phase lock loop control.

WDOUT	Write data out of the 1691 phase lock loop and precompensation controller.
WG	Write gate. Output to the disk drive is valid.
WE	Write enable. Enables the 1797 chip for write operations.
WPRT	Write protect. When this signal is received, no write command can take place and write protect bit in the status register is set.
WRDATA	Precompensated write data pulses that have been reshaped by U16.
5DSØ-5DS3	Five-inch drive select signals.
5"FASTEP	Enables fast stepping in the 5.25" drives.
8"/$\overline{5}$"	Selects between the 8" and the 5.25" drives.
8DSØ-8DS3	Eight-inch drive select signals.
CLOCK	Master clock signal.
ø1 - ø4	Precompensation phase signals.

DISASSEMBLY

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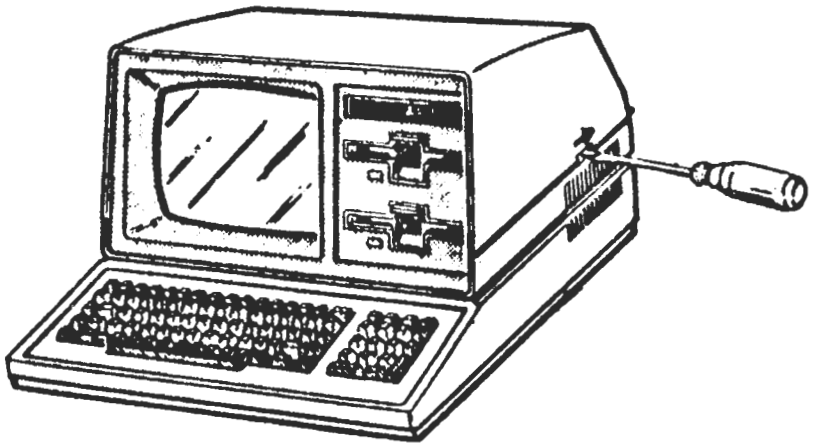
INTRODUCTION

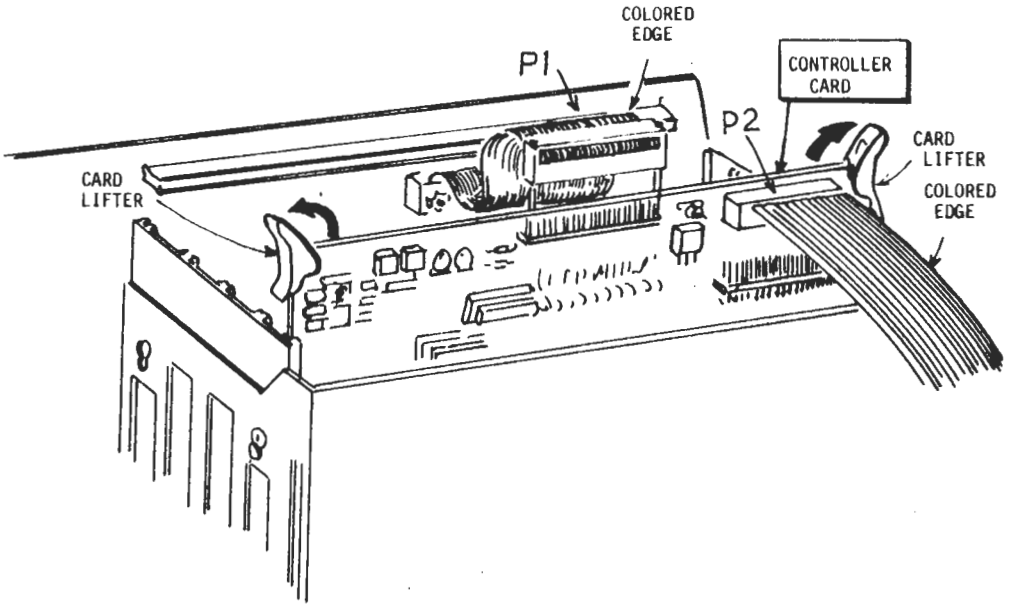
The procedures on the following pages show you how to remove the H-207 Floppy Disk Controller Board from the two different models of the H/Z-100. Find the appropriate procedure and follow the instructions.

ALL-IN-ONE



-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch bracket is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.

-- Remove the cabinet top and set it aside in a safe place.



-- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.

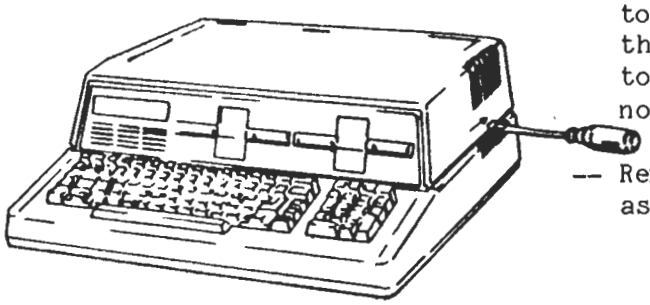
-- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.

-- Now lift the H-207 board from the card cage.

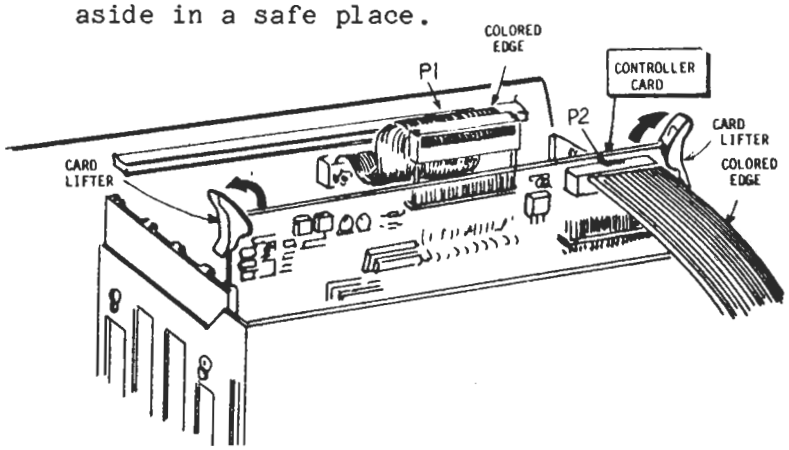
This completes the removal of the H-207 board from the H/Z-100 All-in-One computer. Reverse the procedure to install the board into the computer.

LOW PROFILE

-- With a flat-blade screwdriver, slide the latch bracket to the center of the slot in the cabinet top. The latch is spring loaded, so you will have to work with one side of the cabinet top at a time. While holding the latch in the center position, lift that side of the cabinet top. After one side is freed, perform the procedure on the other side. Be sure to hold the freed side up, so it will not snap back down.



-- Remove the cabinet top and set it aside in a safe place.



-- Disconnect the 50-conductor cable at P1 and the 34-conductor cable at P2 from the H-207 board.

-- Lift up on the H-207 board extractors to pop the board free from the S-100 bus connector.

-- Now lift the H-207 board from the card cage.

This completes the removal of the H-207 board from the H/Z-100 Low-Profile computer. Reverse the procedure to install the board into the computer.

TECHNICIAN NOTES:

VISUAL CHECKS

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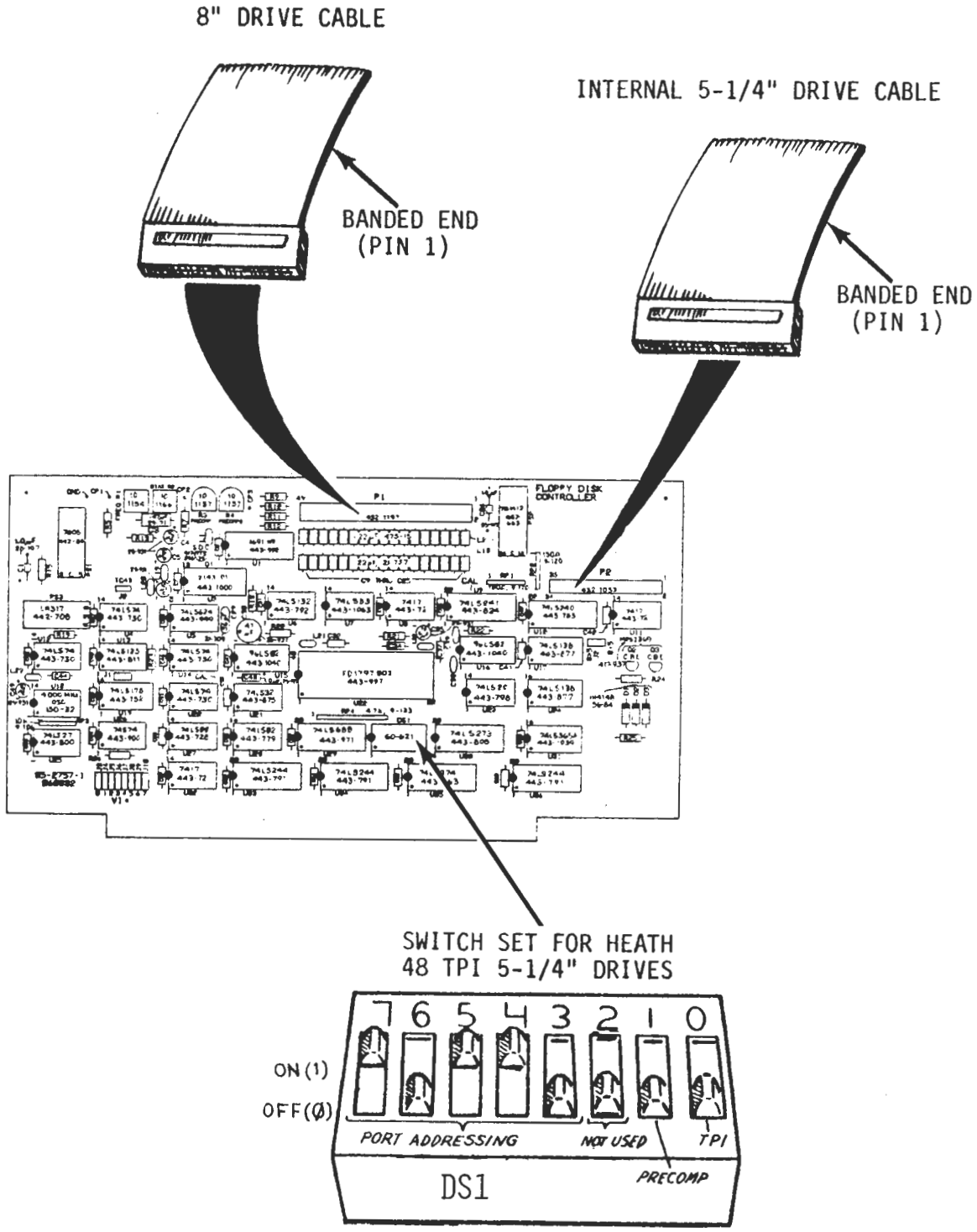
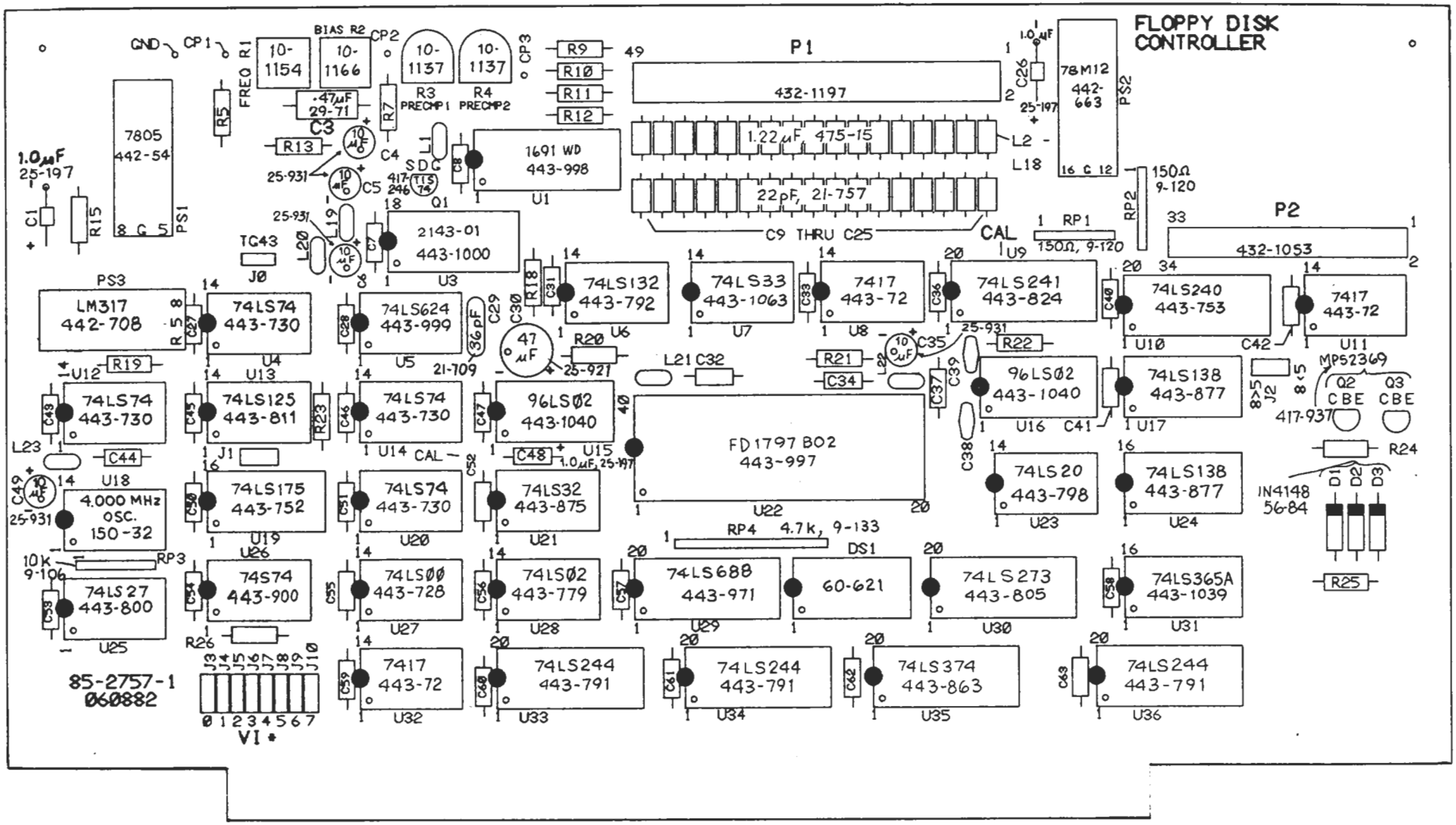
DISK CONTROLLER BOARD CABLE CONNECTIONS AND SWITCH POSITIONS (IN AN H/Z-100 ENVIRONMENT)



CIRCUIT COMPONENT LOCATIONS AND VALUES



H-207 FLOPPY DISK CONTROLLER

ADJUSTMENTS

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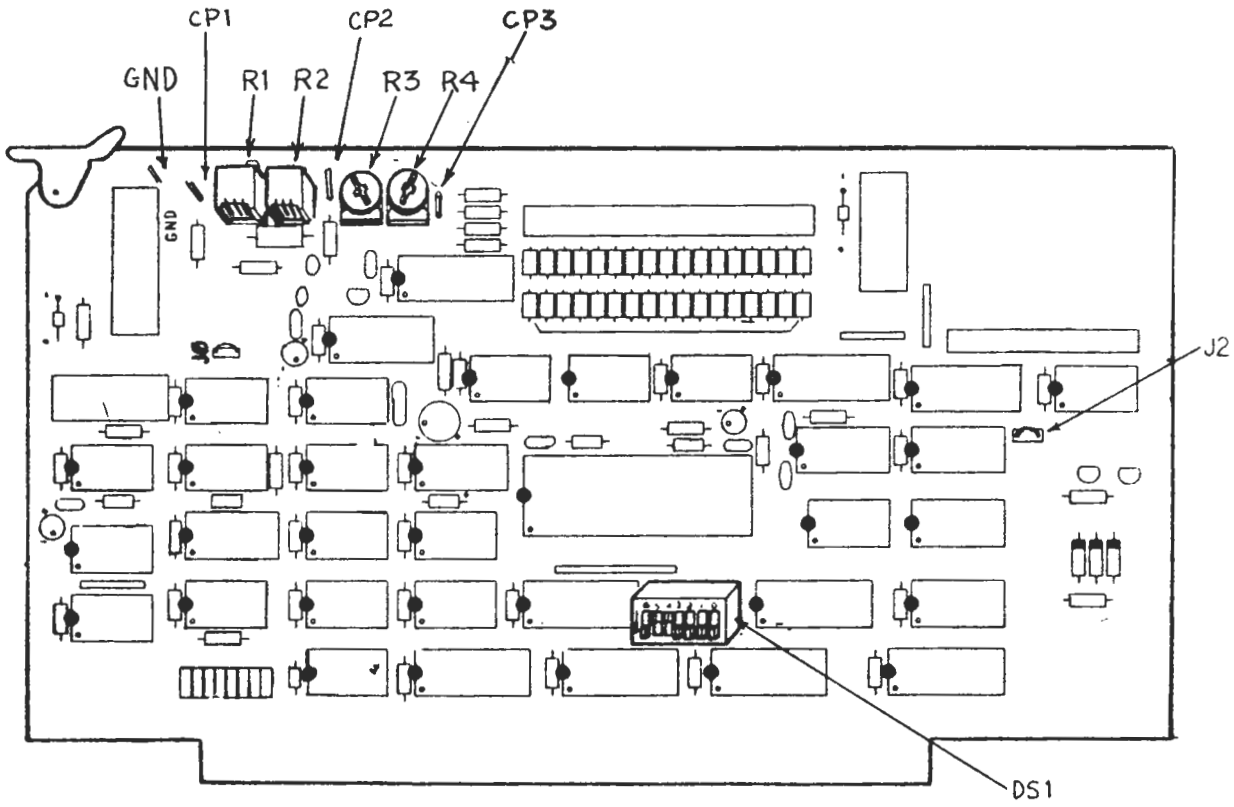


H-207 CONTROLLER BOARD

CONTROLS AND JUMPER LOCATIONS

INTRODUCTION

In this section of the manual, instructions will be given on how to calibrate the H-207 Disk Controller Board. There are two adjustments that the controller board may require. These are Data Separator adjustments and Write Precompensation adjustments. Follow the procedures below to perform these two adjustments.

EQUIPMENT NEEDED

Frequency Counter	IM-2420 or equivalent (optional).
Low Capacitance Probe	PKW-105 or equivalent.
Multimeter	IM-2202 or equivalent.
Oscilloscope	IO-4510 or equivalent.
H-207 Calibration Board	See H-207 assembly manual (HE 595-2909) for parts list and assembly details.

DATA SEPARATOR ADJUSTMENT

Located on the following pages are two methods to adjust the data separator. The first procedure is the preferred method because of its ease and accuracy. The second procedure is the same method given to kitbuilders of the H-207. Locate the procedure you wish to use and follow the steps in that procedure.

FREQUENCY COUNTER METHOD

-- Allow a fifteen minute warm-up of the board with the top cover of the computer in place.

-- Remove the top cover of the computer.

-- Connect the common test lead of the multimeter to the GND test point at the upper left side of the controller board. Refer to the H-207 Controls and Jumper Locations pictorial.

-- Connect the positive test lead to the CP2 test point.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). Switch the multimeter to lower ranges to perform this adjustment accurately.

-- Disconnect the multimeter.

-- Connect the common lead of the frequency counter to the GND test point.

-- Connect the test probe of the frequency counter to the CP1 test point.

-- Adjust the FREQ control (R1) until the frequency counter display shows 4.000 MHz.

-- Disconnect the frequency counter.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

KIT BUILDER METHOD

-- Remove the controller board from the computer.

-- Remove U9, U22, and U30 from their sockets.

-- Tack solder a length of wire between pins 1 and 20 of the socket for U9.

-- Tack solder wires to interconnect pins 30, 33, 37, and 20 of the socket for U22.

-- Set the PRECMP 2 control (R4) to a fully clockwise position.

-- Set the PRECMP 1 control (R3) to a fully counterclockwise position.

-- Connect the common test lead of the multimeter to the GND test point.

-- Reinstall the controller board into the computer.

-- Connect the positive test lead to the CP2 test point and apply power to the computer.

-- Adjust the BIAS control (R2) until the multimeter display shows +1.40 VDC (±.05 volts). You will want to switch the multimeter to lower ranges to perform this adjustment accurately.

-- Allow a period of 15 minutes for drifting; then perform the R2 adjustment again.

-- Power down the computer and remove the controller board.

-- Tack solder a length of wire between the two holes marked CAL.

-- Reinstall the controller board and apply power to the computer.

-- Adjust the FREQ control (R1) for a multimeter display of +1.40 VDC (±0.05 volts) at test point CP2.

-- Power down the computer and remove the controller board.

-- Remove all the temporarily installed jumper wires.

-- Install U9, U22, and U30 in their respective sockets.

-- Reinstall the controller board into the computer.

The adjustments to the Data Separator are now complete. Proceed to WRITE PRECOMPENSATION ADJUSTMENTS.

WRITE PRECOMPENSATION ADJUSTMENTS

Located on the following pages are two methods to adjust write precompensation. The first method uses the calibration circuit board that is included in the H-207 kit. The second method requires the use of an oscilloscope and precompensation data about the drives that are used with the controller board. The first method is the preferred method because of its ease. The second method is required, however, when precompensation values not included on the calibration circuit board are needed for a particular drive. Locate the procedure you wish to use and follow the steps in that procedure.

CALIBRATION CIRCUIT BOARD METHOD

The calibration circuit board method is primarily used to adjust the H-207 for use within a H/Z-100. By using this method, the 5-1/4" drive section of the controller board is set for a write precompensation value of 120 nS. This is the value used for Heath/Zenith 48 TPI, 5-1/4" disk drives that are included in the H/Z-100s. The jumpers at J0 and J2 remain at the stock position. That is, J0 is out and J2 is in the 8 < 5 position (foil bridge).

You may use the calibration circuit board for other values of precompensation. By installing DL502, you may choose from five values of precompensation. These being 120 nS, 160 nS, 200 nS, 240 nS, and 280 nS. However, you may have a customer application that requires a precompensation value not mentioned above. In this case, proceed to Oscilloscope Method of Write Precompensation.

You may also use the calibration circuit board for setting write precompensation for 8" disk drives. Again, if the precompensation value needed is not obtainable with the calibration board, use the Oscilloscope Method. Remember when setting precompensation for 8" drives, you will have to determine if the 8" value is greater than the 5-1/4" value. If it is, you will have to jumper J2 so it is in the 8 > 5 position. Also remember, that R4 is the control that needs to be adjusted instead of R3.

PROCEDURE

-- Obtain a calibration circuit board (see H-207 manual HE 595-2909 for construction).

-- Connect the alligator clip of the calibration board to a source of +5 volts on the H-207 controller board. The positve end of any .1 uF glass capacitor is a good source.

-- Connect the black wire from the calibration board to the GND test point on the H-207 board.

-- Connect the yellow wire from the calibration board to the CP3 test point of the H-207 board.

-- If not already done, set R3 fully counterclockwise and R4 fully clockwise.

-- Set the jumper select wire of the calibration board to 120 nS. If the drive requires more precompensation, set the jumper to the desired position.

-- Turn on the computer.

-- Boot up a system disk. Refer to the appropriate operating system manual and start the disk format program.

-- While the format program is running, adjust R3 on the H-207 board until the LED on the calibration board just turns on.

-- Turn off the computer and disconnect the calibration circuit board.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

OSCILLOSCOPE METHOD

The oscilloscope method of write precompensation adjustment is primarily used to adjust the H-207 for non Heath/Zenith disk drives. To understand the relationship that exists between the PRECOMP switch setting of DS1 and jumper J0, refer to the table below. This table shows how to set the PRECOMP switch of DS1 and J0 for the particular system you are working on. Now perform the following steps to adjust write precompensation. Refer to the illustration at the beginning of this section for the locations of the test points.

	DESIRED RESULTS		
TYPE OF DRIVE	Precomp no tracks	Precomp all tracks	Precomp tracks >43
8" Double-Density	N/A	$\overline{\text{Precomp}}$* = Ø J0 = X	$\overline{\text{Precomp}}$ = 1 J0 - X
5-1/4", 48 TPI, Double-Density	$\overline{\text{Precomp}}$ = 1 J0 = X	$\overline{\text{Precomp}}$ = 0 J0 = X	N/A
5-1/4", 96 TPI, Double-Density	$\overline{\text{Precomp}}$ = 1 J0 = IN	$\overline{\text{Precomp}}$ = 0 J0 = X	$\overline{\text{Precomp}}$ = 1 J0 = OUT

*$\overline{\text{Precomp}}$ is bit 4 in the control latch

X = Don't Care

NOTE: Precomp is automatically disabled in single-density operation.

-- Set the PRECMP 2 control (R4) to a fully clockwise position.

-- Set the PRECMP 1 control (R3) to a fully counterclockwise position.

The position of J2 will determine which of the two following procedures you will use when adjusting write precompensation. Refer to the manufacturer's suggested write precompensation value for the type of drives in the system. If the system has only 8" disk drives, or only 5-1/4" disk drives, or the 8" write precompensation figure is less than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 < 5". If the system has disk drives where the 8" write precompensation figure is greater than the 5-1/4" write precompensation figure, use the procedure under "J2 = 8 > 5".
Typical values of precompensation are:

5-1/4" disk drives	125 to 200 nS	typical 150 nS.
8" disk drives	125 to 175 nS	typical 135 nS

J2 = 8 < 5 PROCEDURE

-- Connect the oscilloscope probe to GND and CP3. Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.

-- Apply power to the computer.

-- If the system has 8" disk drives, start the format routine on an 8" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.

-- If there are 5-1/4" disk drives in addition to 8" disk drives in the system, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation for that type of drive.

-- If the system only has Heath/Zenith 5-1/4" 96 TPI disk drives or non Heath/Zenith disk drives that require write precompensation adjustment, start the format routine on a 5-1/4" diskette. While format is running, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds to the manufacturer's suggested write precompensation value for that drive.

-- Power down the computer.

-- Disconnect the oscilloscope probe.

This completes write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

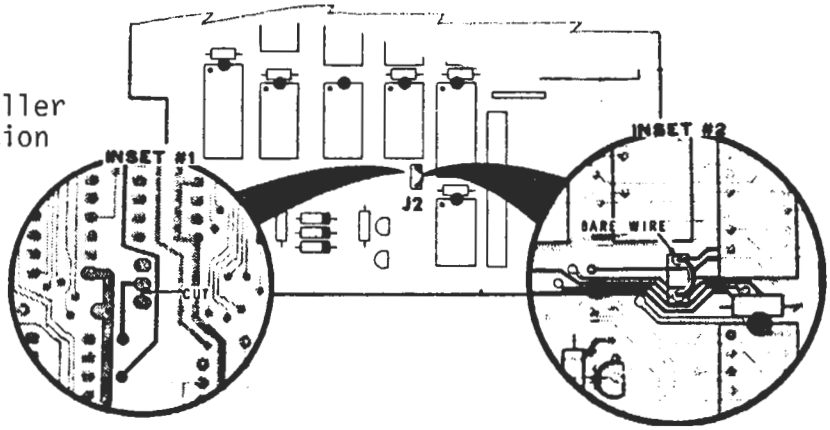
J2 = 8 > 5 PROCEDURE

-- Remove the controller board from the computer.

-- Refer to the H-207 J2 location pictorial and cut the foil that connects the middle of the J2 position to the 8 < 5 position of J2.

-- Install a jumper wire connecting the middle hole of the J2 position to the 8 > 5 hole of the J2 position.

H-207 Controller Board J2 Location



-- Install the floppy board into the computer.

-- Connect the oscilloscope probe to GND and CP3. Set the probe to X10 and set the oscilloscope at 50 nS/division to display a 100 to 300 nS negative going pulse.

-- Apply power to the computer.

-- While formatting a 5-1/4" diskette, adjust the PRECMP 1 control (R3) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.

-- While formatting an 8" diskette, adjust the PRECMP 2 control (R4) until the pulse width displayed on the oscilloscope corresponds with the manufacturer's suggested write precompensation value.

-- Power down the computer.

-- Disconnect the oscilloscope probe.

This completes the write precompensation adjustment.

NOTE: All diskettes should be reformatted before being used.

TROUBLESHOOTING

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INTRODUCTION

To troubleshoot the H-207 Floppy Disk Controller, use this section of the manual in conjunction with the schematic. Located in this section of the manual are service hints that will aid you in servicing the board. The schematic contains voltages and logic levels of a normally functioning board after a hard reset. By using standard troubleshooting techniques, most problems can be quickly located and corrected.

EQUIPMENT NEEDED

Frequency Counter	IM-2420 or equivalent.
Logic Probe	IT-4710 or equivalent.
Low Capacitance Probe	PKW-105 or equivalent.
Multimeter	IM-2260 or equivalent.
Oscilloscope	IO-4510 or equivalent.

H/Z-100 TEST FIXTURE

The H/Z-100 test fixture is set up so that the 5-1/4", 48 TPI disk drives are the primary boot device. Also, auto boot is defeated (See "Configuration").

It is assumed that the H-207 board is configured for operation within the H/Z-100. That is, J1 is jumpered for a 3 MHz or greater clock speed and DS1 is configured for port BO (Hex), 48 TPI, and precompensation disabled.

PREWORK

Once you have received a H-207 Floppy Controller Board in for service, use the checkout procedure below. Included in the procedure are problems that may be identified before power is applied to the circuit board. Many of the checks below may have already been implemented in your preworking.

CHECKOUT PROCEDURE

Check the H-207 Controller Board for:

- Polarized capacitors installed backwards.
- Q1, Q2, or Q3 installed incorrectly.
- D1, D2, or D3 installed backwards.
- ICs installed backwards.
- Dirty S-100 board contacts.
- Solder bridges.
- Cold solder joints.
- Resistor packs installed backwards.
- Correct jumpering.
- Switch settings of DS1.
- Correct voltage regulator for location:

  7805 at PS1.
  78M12 at PS2.
  LM317 at PS3.

After making these checks, install the H-207 into your H/Z-100 test fixture and confirm the customer's complaint. If the board appears to operate properly, align the controller board using the procedure in the Alignment and Adjustments section of this manual.

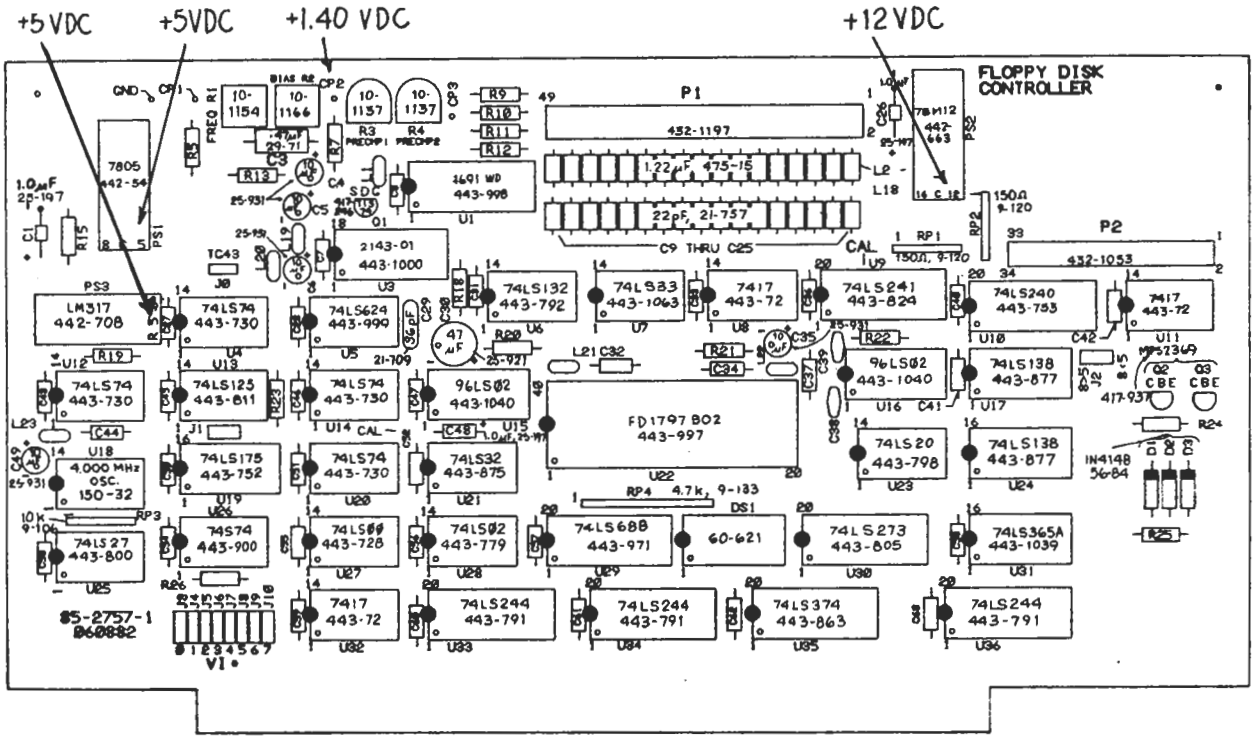
If the problem still exists, proceed to Service Hints.

SERVICE HINTS

VOLTAGE CHECKS

With the H-207 installed in your test fixture, perform the following voltage checks with your multimeter. The GND test point is a good place to connect the common lead of the multimeter. It is assumed that the disk drive cables are disconnected from the controller board.

- The voltage at PS1-5 is +5 VDC.
- The voltage at PS2-12 is +12 VDC.
- The voltage at PS3-5 is +5 VDC.
- The voltage at CP2 is +1.40 VDC.



If the voltages at these test points are within 5% of the values stated, it can be safely assumed U1, U5, and the voltage regulators are operating properly. Assuming the problem still exists, further aid can be found in Logic Level Checks and Waveforms. Otherwise, proceed to the Alignment and Adjustments.

LOGIC LEVEL CHECKS

On the following pages is a logic probe analysis of the H-207 board. When performing the tests, you need only to test the ICs in the left column indicated by an asterisk (*). If you don't get the suggested logic state, then check each IC listed immediately to the right. The logic states for these ICs are listed in the left column below the ICs with the asterisks.

Continue tracing backwards using this procedure until you test an IC that matches the suggested logic state. The previous IC that you tested is likely the bad IC.

Before you replace the suspected IC, check the other lines leading up to it. You must do this because this checkout procedure gives only the most likely causes to the problem. It doesn't cover such things as open ground foils, shorted foil runs, or open resistors.

As you make the following checks, press the (B)oot key and press RETURN. Logic states located inside parenthesis indicates that the probe pulses one or more times while "Read Completed" is printed on the screen. In the case of a (P) indication, the pulse rate (as indicated by the logic probe) will momentarily change during the "Read Completed" interval.

The schematic shows the logic states after a CTRL/RESET has been performed. Refer to these logic states for troubleshooting areas not covered in the following tests.

To setup the H-207 for the following test, connect at least one 48 TPI, 5-1/4" disk drive to P1 and turn on the computer.

H-207 DISK CONTROLLER TEST

CHECK	IF NOT OKAY, CHECK
*Q3 Collector = Z	U21-8
*U1-16 = 2 MHz	U13-6
*U7-4 = L	U7-5 (Also press and release CTR/RESET. U7-4 should remain low for about 18 seconds. If not, then replace U15.)
*U9-19 = L	U30 or the data bus is defective.
*U10-12 = H	U10 or U22 is defective.
*U10-14 = H	U10 or U22 is defective.
*U10-16 = H	U10 or U22 is defective.
*U11-4 = H	U11-3
*U11-6 = H	U11-5
*U11-8 = H	U11-9
*U11-10 = L	U11-11
*U11-12 = H	U11-13
*U22-2 = (H)	U21-11
*U22-3 = (H)	U21-3
*U22-23 = (H)	U15-7
*U22-24 = 1 MHz	U13-8
*U22-27 = P	U16-9
*U22-34 = L	U9 is defective.
*U22-35 = L	U9 is defective.
*U22-36 = H	U9 is defective.
*U31-1 = (H)	U27-8
*U31-15 = (H)	U17-14
*U32-6 = (H)	U32-5
*U35-11 = (P)	U28-4
*U36-1 = (H)	U27-8
*U36-19 = (H)	U27-8

End of test.

U4-3	= 4 MHz	U5-8
U4-5	= 2 MHz	U4-3
U4-9	= L	U4-11, U4-12
U4-11	= P	U4-5
U4-12	= L	U30 or the data bus is defective.
U5-8	= 4 MHz	U5 or U1 defective; R1 or R2 incorrectly adjusted.
U7-5	= H	U23-8
U7-11	= L	U30 or the data bus is defective.
U7-12	= L	U30 or the data bus is defective.
U7-13	= H	U7-11, U7-12
U10-3	= L	U10-17
U10-17	= H	U33-9
U11-3	= H	U16-7
U11-5	= H	U24-14
U11-9	= H	U24-12
U11-11	= L	U24-15
U11-13	= H	U24-13
U12-3	= 4 MHz	U18 is bad.
U12-5	= 2 MHz	U12-3
U12-9	= 1 MHz	U12-11
U12-11	= 2 MHz	U12-5
U13-4	= L	U4-9
U13-5	= 2 MHz	U4-5
U13-6	= 2 MHz	U13-4, U13-5
U13-8	= 1 MHz	U13-9, U13-10
U13-9	= 1 MHz	U12-9
U13-10	= L	U14-8
U14-8	= L	U14-11, U14-12
U14-11	= 1 MHz	U12-9
U14-12	= H	U7-13
U15-4	= H	U22 or the data bus is defective.
U15-7	= (H)	U15-4
U16-4	= L	U1 or U22 is defective.
U16-7	= H	U16-4
U16-9	= P	U16-11
U16-11	= P	U9 is defective.

U17-1 = P	U34-18
U17-2 = P	U34-16
U17-4 = (H)	U20-6
U17-6 = P	U34-14
U17-7 = L	U19-1
U17-14 = (H)	U17-1, U17-2, U17-4, U17-6
U17-15 = (H)	U17-1, U17-2, U17-4, U17-6
U19-1 = (L)	U26-8
U19-14 = L	U19-1
U20-1 = (L)	U28-13
U20-2 = (L)	U28-13
U20-3 = P	U27-6
U20-5 = (L)	U20-1, U20-2, U20-3
U20-6 = (H)	U20-1, U20-2, U20-3
U21-1 = (H)	U27-11
U21-2 = (H)	U27-8
U21-3 = (H)	U21-1, U21-2
U21-4 = (H)	U17-15
U21-5 = (P)	U33-12
U21-6 = (H)	U21-4, U21-5
U21-8 = L	U21-10
U21-10 = L	U22 of data bus is defective.
U21-11 = (H)	U21-12, U21-13
U21-12 = (H)	U27-11
U21-13 = (P)	U33-12
U22-39 = (L)	Check the data bus at pins 7 through 14. These lines pulse from a high impedance state while "Read Completed" is being printed. If not, then check the components along the data bus.
U23-2 = (L)	U30-16
U23-4 = P	U34-18
U23-5 = P	U34-16
U23-6 = (H)	U23-2, U23-4, U23-5
U23-8 = H	U23-13
U23-13 = L	U24-15

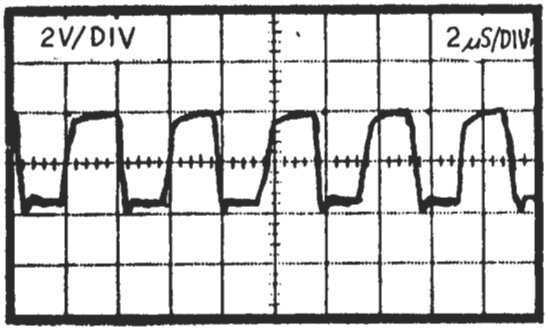
U24-1 = L	U30 or the data bus is defective.
U24-2 = L	U30 or the data bus is defective.
U24-3 = L	U30 or the data bus is defective.
U24-6 = H	U30 or the data bus is defective.
U24-12 = H	U24-1, U24-2, U24-3, U24-6
U24-13 = H	U24-1, U24-2, U24-3, U24-6
U24-14 = H	U24-1, U24-2, U24-3, U24-6
U24-15 = L	U24-1, U24-2, U24-3, U24-6
U25-1 = L	U19-7
U25-2 = L	U10-3
U25-3 = L	U10-3
U25-4 = (L)	U22-39
U25-5 = L	U19-14
U25-6 = (H)	U25-3, U25-4, U25-5
U25-12 = (H)	U25-1, U25-2, U25-13
U25-13 = (L)	U22-39
U26-2 = (H)	U23-6
U26-3 = (L)	U20-5
U26-4 = (H)	U25-12
U26-5 = (H)	U26-2, U26-3, U26-4
U26-8 = (L)	U26-10, U26-11, U26-12
U26-10 = (H)	U25-6
U26-11 = (L)	U20-5
U26-12 = (H)	U23-6
U27-1 = (L)	U22-39
U27-3 = (H)	U27-1
U27-4 = P	U33 defective.
U27-5 = P	U33 defective.
U27-6 = P	U27-5, U27-4
U27-8 = (H)	U27-9, U27-10
U27-9 = P	U33 defective.
U27-10 = (L)	U20-5
U27-11 = (H)	U27-12, U27-13
U27-12 = (L)	U28-10
U27-13 = (H)	U26-5
U28-1 = (H)	U28-2, U28-3
U28-2 = (L)	U33 defective.
U28-3 = (L)	U33 defective.
U28-4 = (P)	U28-6

U28-6 = (P)	U33-12
U28-8 = (H)	U20-6
U28-9 = P	U34-14
U28-10 = (L)	U28-8, U28-9
U28-11 = (P)	U29-19
U28-12 = (H)	U28-1
U28-13 = (L)	U28-11, U28-12
U29-19 = (P)	U29, U34, or DS1 defective.
U30-1 = H	U33-9
U30-11 = (H)	U21-6
U30-16 = (L)	U30-1, U30-11, or data bus problem.
U32-5 = (H)	U27-3
U33-9 = H	U33 defective.
U33-12 = (P)	U33 defective.
U34-14 = P	U34 defective.
U34-16 = P	U34 defective.
U34-18 = P	U34 defective.

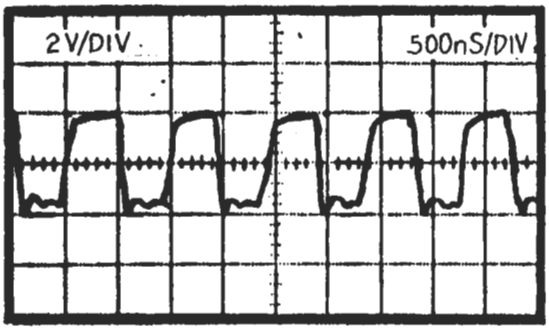
WAVEFORMS

The waveforms shown in this section are generated by a normally functioning controller board in an idle state. Use these waveforms as a reference when checking waveforms on the board you are servicing.

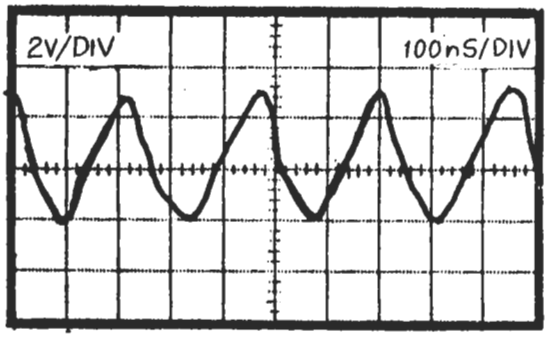
The waveform at the right was taken from U22-26. This is the RCLK signal that originates at U1-12. In an idle state the frequency of RCLK is around 250 kHz.



The waveform at the right was taken from U22-24. This is the CLK signal that originates from the oscillator circuits. The frequency of this signal is 1 MHz when the board is in an idle state.



The waveform at the right was taken from CP1. This is the VCO signal that originates from the VCO, U5-8. The frequency of this signal is 4 MHz when the board is in an idle state.



PARTS LISTS

DISK CONTROLLER CIRCUIT BOARD 5-179
CALIBRATION CIRCUIT BOARD 5-180

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

DISK CONTROLLER CIRCUIT BOARD

CAPACITORS

C1	1.0 uF tantalum	HE 25-197
C2	none	
C3	.47 uF polycarbonate	HE 29-71
C4	10 uF tantalum	HE 25-220
C5	10 uF tantalum	HE 25-220
C6	10 uF tantalum	HE 25-220
C7	.1 uF ceramic	HE 21-762
C8	.1 uF ceramic	HE 21-762
C9	22 pF ceramic	HE 21-757
C10	22 pF ceramic	HE 21-757
C11	22 pF ceramic	HE 21-757
C12	22 pF ceramic	HE 21-757
C13	22 pF ceramic	HE 21-757
C14	22 pF ceramic	HE 21-757
C15	22 pF ceramic	HE 21-757
C16	22 pF ceramic	HE 21-757
C17	22 pF ceramic	HE 21-757
C18	22 pF ceramic	HE 21-757
C19	22 pF ceramic	HE 21-757
C20	22 pF ceramic	HE 21-757
C21	22 pF ceramic	HE 21-757
C22	22 pF ceramic	HE 21-757
C23	22 pF ceramic	HE 21-757
C24	22 pF ceramic	HE 21-757
C25	22 pF ceramic	HE 21-757
C26	1.0 uF tantalum	HE 25-197
C27	.1 uF ceramic	HE 21-762
C28	.1 uF ceramic	HE 21-762
C29	36 pF ceramic	HE 21-709
C30	47 uF electrolytic	HE 25-921
C31	.1 uF ceramic	HE 21-762
C32	.1 uF ceramic	HE 21-762
C32a	10 uF tantalum	HE 25-220
C33	.1 uF ceramic	HE 21-762
C34	.1 uF ceramic	HE 21-762
C35	10 uF tantalum	HE 25-220
C36	.1 uF ceramic	HE 21-762
C37	.1 uF ceramic	HE 21-762
C38	180 pF ceramic	HE 21-746
C39	180 pF ceramic	HE 21-746
C40	.1 uF ceramic	HE 21-762
C41	.1 uF ceramic	HE 21-762
C42	.1 uF ceramic	HE 21-762
C43	.1 uF ceramic	HE 21-762
C44	.1 uF ceramic	HE 21-762
C45	.1 uF ceramic	HE 21-762

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

CAPACITORS (CONTINUED)

C46	.1 uF ceramic	HE 21-762
C47	.1 uF ceramic	HE 21-762
C48	1.0 uF tantalum	HE 25-197
C49	10 uF tantalum	HE 25-220
C50	.1 uF ceramic	HE 21-762
C51	.1 uF ceramic	HE 21-762
C52	.1 uF ceramic	HE 21-762
C53	.1 uF ceramic	HE 21-762
C54	.1 uF ceramic	HE 21-762
C55	.1 uF ceramic	HE 21-762
C56	.1 uF ceramic	HE 21-762
C57	.1 uF ceramic	HE 21-762
C58	.1 uF ceramic	HE 21-762
C59	.1 uF ceramic	HE 21-762
C60	.1 uF ceramic	HE 21-762
C61	.1 uF ceramic	HE 21-762
C62	.1 uF ceramic	HE 21-762
C63	.1 uF ceramic	HE 21-762

INDUCTORS

L1	35 uH	HE 235-229
L2	1.22 uH bead	HE 475-15
L3	1.22 uH bead	HE 475-15
L4	1.22 uH bead	HE 475-15
L5	1.22 uH bead	HE 475-15
L6	1.22 uH bead	HE 475-15
L7	1.22 uH bead	HE 475-15
L8	1.22 uH bead	HE 475-15
L9	1.22 uH bead	HE 475-15
L10	1.22 uH bead	HE 475-15
L11	1.22 uH bead	HE 475-15
L12	1.22 uH bead	HE 475-15
L13	1.22 uH bead	HE 475-15
L14	1.22 uH bead	HE 475-15
L15	1.22 uH bead	HE 475-15
L16	1.22 uH bead	HE 475-15
L17	1.22 uH bead	HE 475-15
L18	1.22 uH bead	HE 475-15
L19	35 uH	HE 235-229
L20	35 uH	HE 235-229
L21	35 uH	HE 235-229
L22	35 uH	HE 235-229
L23	35 uH	HE 235-229

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.

RESISTORS

R1	10 kilohm control		HE 10-1154
R2	100 kilohm control		HE 10-1180
R3	2 kilohm control		HE 10-1137
R4	2 kilohm control		HE 10-1137
R5	47 ohm	1/4 watt, 5%	HE 6-470-12
R6	none		
R7	47 kilohm	1/4 watt, 5%	HE 6-473-12
R8	jumper		
R9	1 megohm	1/4 watt, 5%	HE 6-105-12
R10	1000 ohm	1/4 watt, 5%	HE 6-102-12
R11	3900 ohm	1/4 watt, 5%	HE 6-392-12
R12	1800 ohm	1/4 watt, 5%	HE 6-182-12
R13	47 kilohm	1/4 watt, 5%	HE 6-473-12
R14	jumper		
R15	720 ohm	1/4 watt, 1%	HE 6-7200-12
R16	none		
R17	none		
R18	120 kilohm	1/4 watt, 5%	HE 6-124-12
R19	237 ohm	1/4 watt, 1%	HE 6-2370-12
R20	1 megohm	1/4 watt, 5%	HE 6-105-12
R21	3900 ohm	1/4 watt, 1%	HE 6-3901-12
R22	2200 ohm	1/4 watt, 1%	HE 6-2201-12
R23	1000 ohm	1/4 watt, 5%	HE 6-102-12
R24	120 kilohm	1/4 watt, 5%	HE 6-124-12
R25	1000 ohm	1/4 watt, 5%	HE 6-102-12
R26	1000 ohm	1/4 watt, 5%	HE 6-102-12

RESISTOR PACKS

RP1	150 ohm	HE 9-120
RP2	150 ohm	HE 9-120
RP3	10 kilohm	HE 9-106
RP4	4.7 kilohm	HE 9-133

PARTS LIST

DISK CONTROLLER CIRCUIT BOARD (CONTINUED)

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS		
PS1	7805 5V regulator	HE 442-54
PS2	78M12 +12V regulator	HE 442-663
PS3	LM317 +adj regulator	HE 442-708
U1	WD1691	HE 443-998
U2	none	
U3	2143-01	HE 443-1000
U4	74LS74	HE 443-730
U5	74LS624	HE 443-999
U6	74LS132	HE 443-792
U7	74LS33	HE 443-1063
U8	7417	HE 443-72
U9	74LS241	HE 443-824
U10	74S240	HE 443-753
U11	7417	HE 443-72
U12	74LS74	HE 443-730
U13	74LS125	HE 443-811
U14	74LS74	HE 443-730
U15	96LS02	HE 443-1040
U16	96LS02	HE 443-1040
U17	74LS138	HE 443-877
U18	4.000 MHz oscillator	HE 150-132
U19	74LS175	HE 443-752
U20	74LS74	HE 443-730
U21	74LS32	HE 443-875
U22	FD1797B02	HE 443-997
U23	74LS20	HE 443-798
U24	74LS138	HE 443-877
U25	74LS27	HE 443-800
U26	74S74	HE 443-900
U27	74LS00	HE 443-728
U28	74LS02	HE 443-779
U29	74LS688	HE 443-971
U30	74LS273	HE 443-805
U31	74LS365A	HE 443-1039
U32	7417	HE 443-72
U33	74LS244	HE 443-791
U34	74LS244	HE 443-791
U35	74LS374	HE 443-863
U36	74LS244	HE 443-791
OTHER CIRCUIT COMPONENTS		
D1	1N4148 diode	HE 56-84
D2	1N4148 diode	HE 56-84
D3	1N4148 diode	HE 56-84
DS1	8-section slide switch	HE 60-621
Q1	TIS74 transistor	HE 417-246
Q2	MPS2369 transistor	HE 417-937
Q3	MPS2369 transistor	HE 417-937
CONNECTORS - SOCKETS		
	1-pin connector	HE 423-121
	8-pin inline IC socket	HE 434-230
	14-pin IC socket	HE 434-298
	16-pin IC socket	HE 434-299
	18-pin IC socket	HE 434-310
	20-pin IC socket	HE 434-311
	40-pin IC socket	HE 434-253
P2	34-pin right-angle connector	HE 432-1053
P1	50-pin right-angle connector	HE 432-1197
HARDWARE		
	#4 lockwasher	HE 254-9
	4-40 nut	HE 252-2
	4-40 x 5/16" screw	HE 250-213
MISCELLANEOUS		
	Heat sink	HE 215-669
	H-207 manual	HE 595-2909
	PC board	HE 85-2757-2
	Silicone grease	HE 352-13
	S-100 circuit board extractor	HE 266-1203
	Wire, solid	HE 340-8
	Wire, white solid	HE 344-59

CALIBRATION CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
R501	10 kilohm 1/4 watt, 5%	HE 6-103-12
R502	330 ohm 1/4 watt, 5%	HE 6-331-12
C501	.1 uF ceramic	HE 21-762
DL501	Delay line	HE 41-10
	Alligator clip insulator	HE 73-34
	PC board	HE 85-2800-1
	Alligator clip	HE 260-16
	Wire, black stranded	HE 344-90
	Wire, red stranded	HE 344-92
	Wire, white stranded	HE 344-94
D501	LST5053 LED	HE 412-640
	1-pin socket	HE 432-120
	14-pin IC socket	HE 434-298
U501	74LS00	HE 443-728
U502	74LS74	HE 443-730

CIRCUIT BOARD X-RAY VIEW