# H/Z-37 Controller on Standard Eight Inch Drives 

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Sooner or later the need for more storage overcomes all keyboard pounders. At the present time there are various solutions to this storage problem offered by the many vendors and suppliers of accessories for the Heath/ Zenith line.
This article describes a way to add $8^{\prime \prime}$ drives using the lowest priced double-density controller.
Before I outline the details, however, let me explain how I came to choose this particular solution. You may have come to the same conclusions and it may, therefore, meet your needs as it is certainly meeting mine.

## Background

My first consideration was cost. A quick survey of the available equipment showed the $8^{\prime \prime}$ drives to be the most cost effective as a mass storage device. The $H / Z-47$ seemed to be an excellent unit but it used drives too sophisticated for my needs and was too costly for my budget. I had noticed that standard Shugart compatible drives could be found from four to six hundred dollars; surplus drives from commercial users are showing up at computer flea markets in quantity and at affordable prices.
My first move was to purchase a Shugart 850 double-density doublesided drive. I then began to think about designing a suitable controf-s ler.
A survey of all the available controller boards for the H/Z-89 shows a common factor: the same controller chip, Western Digital's WD1797, was used in all of them. A call to Western Digital brought all of the technical data for their various disk controller chips. After reviewing their material, I realized the project would take considerable time and effort. A more practical approach appeared to be purs chasing, rather than building a controller.
The hardware changes were the simplest part of the task. The technical data on the control chip showed that there are only minor changes in the circuitry for the $5^{\prime \prime}$ drives to that for the $8^{\prime \prime}$ drives. Basically, the changes are as follows:

## CIRCUIT

WD1797 CLOCK
VCO IN-DATA SEPARATOR

## PLL SERIES R/C FILTER

## 5 IN.

1 MRZ

2 MRZ
.68 und
$\& 68$ Ohes
Calls to several manufacturers of controller cards for the $\mathrm{H} / \mathrm{Z}-89$ soliciting their specifications yielded little in technical documentation, I knew that on any controller I bought, the changes would be fairly simple. A visit to my local Heath Electronic Center for a look at the H/Z-37 schematic showed that the circuitry for the WD1797 was exactly as the Western Digital manual recommended and in addition all the interrupt controller circuit for the Z-80 was expanded, the entire circuit had been moved to the $\mathrm{H} / \mathrm{Z}-37$ card. The decision about which controller to buy for modification wasn't hard after this.

The use of a Heath product probably carried the most weight after I considered what had to be done. Rather simple modifications to the hardware would make the card (originally intended for $5^{\prime \prime}$ drives) operate for $8^{\prime \prime}$ drives. The modifications in this article are intended only for use with $8^{\prime \prime}$ drives. Using dual $5^{\prime \prime}$ and $8^{\prime \prime}$ is just not possible with the simple changes listed here.

## Results

tam currently running a pair of Shugart 850 drives. The capacity of a double-sided double-density $8^{\prime \prime}$ drive is 4000 sectors or 1 megabyte; thus, 1 have 2 megabytes on line! A single-sided drive offers 2000 sectors.
Several members of the South Jersey Heath Users' Group (SHUG) have upgraded to 4 MHz and are running various combinations of $8^{\prime \prime}$ drives.
The drives are daisy-chained. Four drives off one connector have worked perfectly. Only three drive-select lines are used (DS0- DS2). If more than 3 drives are desired, a binary select scheme has to be implemented. DS3 is changed to a WG43 signal to lower the drive write current on the inner tracks.
Requirements for Getting Started
The first reguirement is a 4 MHz CPU . There have been a number of articles about how this modification is done on HBBS and in REMark.
The other requirements are made to the $\mathrm{H} / \mathrm{Z}-37$ controller board. These modifications will support only one system: $8^{\prime \prime}$ drives, single and double density. Once the modifications are made, $5^{\prime \prime}$ drives on the $\mathrm{H} / \mathrm{Z}-37$ are no longer possible, though your present $\mathrm{H}-17$ board will still be useable.
An adapter board must be made to change the 34 pin cable from the H/Z- 37 to the 50 pin cable used by $8^{\prime \prime}$ drives.

## Hardware Modifications

Read Data Conditioning


The first modification that needs to be completed involves a change to the raw data conditioning monostable. This is used to set the width of the read data pulses from the drive to the width required by the WD1797 read input. The time needed is 150 s plus or minus 50 ns . To accomplish this, refer to the $H / Z-37$ schematic at U-14A. Capacitor C 27 has to be changed to 15 pfd .
WD1 797 Clock
For 8 " drives the controller chip requires a 2 MHz clock. The clock generator is $U-9$ which is a 16 MHz oscillator module. This drives U-10 which is a Divide By 16 to produce the necessary 1 MHz for the $5^{\prime \prime}$ drives. To obtain 2 MHz required by the $8^{\prime \prime}$ drives, cut the path at $\mathrm{U}-10$, pin 11 and install a jumper from the cut path to $\mathrm{U}-10$, pin 12. At pin 12 is the 2 MHz output of the divider.

## VCO Frequency

The voltage controlled oscillator is $\mathrm{U}-17$. This normally operates at
$\mathbf{2 M H z}$; it must be changed to 4 MHz . The frequency is determined by capacitor C32 which is 82 pfd and must be changed to a value of 39 pfd .

## PLL Filter

The PLL filter is a network used to reduce ripple on the control voltage to the VCO and consists of components C29 (.68mfd) and R68 ( 68 ohms). C29 is changed to 0.33 mfd capacitor and R68 is changed to a 33 ohms resistor.

## TG43

This signal is used on some drives to lower the write current when the density on the media's inner tracks is too high to write reliably with the normal value. This signal is output by the controller chip (WD1797) when track 43 or higher is addressed by the controller. This signal is not available on the $\mathrm{H} / \mathrm{Z}-37$ but is easily added. Another output line is needed from the card so the DS3 line was selected to use existing output buffering.

The modifications for the TG43 are straightforward:

1. The path at U-11 pin 19 is cut to disable use of the DS3.
2. A jumper is added from U-12 pin 29 to $\mathrm{U}-16$ pin 9 . This ties the WG43 pins together.
3. A jumper is added from $\mathrm{U}-12$ pin 29 to $\mathrm{U}-15$ pin 10. This ties the new WG43 signal to the input of an unused drive buffer.
4. A jumper is added from $\mathrm{U}-15$ pin 9 to $\mathrm{U}-22$ pin 1 . This takes the output of the previously unused drive buffer to drive the DS3 line.

Note: The schematic shows U-15's unused drive input on the output side of the chip lines and the unused output on the input side.

## RFI Filters

The RFI filters on the output lines must be removed for the read and write data lines. The constants used attenuate double density signals. The easiest way to do this is to cut capacitors C39 and C44 from the board. They are 470pfd disk. The series inductors L13 and L18 must be removed and replaced with jumpers. The inductors are the ferrite beads with the wire run through twice. This will take care of the top connector P3 If the bottom connector P4 is to be used, then parts C53, C58, L27, and L32 must also be changed as above.

1. L13 and L18 are shorted or removed and jumpered.
2. C39 and C44 are removed.

This prevents the RFI filter from degrading read/write data.
This completes the hardware modifications on the H/Z-37 board. The modified board now needs to be aligned.

## Alignment of Controller

At this point the controller card alignment should be done. Refer to the section in the H/Z-37 operation manual entitled "Recalibration" (p.33).

The following changes need to be made in the section entitled "VCO CENTER FREQUENCY ADJUSTMENT":

1. With a frequency counter the frequency will now be 3950 to 4050 KHz . (See p. 34 in the H/Z-37 Manual.)
2. With an oscilloscope the period will be 247 ns to 253 ns . (See p. 36 in the H/Z-37 Manual.)

## Precompensation

("Precomposition" in the Manual; p.36)

1. Change to comply with drive manufacturer's recommendations.

I found for the drives tested, minimum precompensation worked best.

All other steps in the recalibration section should be followed as written.

If all of these changes have been accomplished, then the project is almost completed. Next is to describe the adapter card for pinout conversion.

## Adapter Card

Next an adapter card is fabricated. A perf board like the Radio Shack (276-162) with 0.100 inch spaced holes can be used. Two headers for the ribbon connectors are also needed. The 34 pin and the 50 pin headers are then mounted on the perf board and all the ground pins are connected together first. Next the signal leads must be cross wired to suit your particular drive. The following list has been prepared for use with Shugart 800-1, 801, 850, and 851 type drives.

Note: Be sure to check orientation of the cable to this adapter card before wiring and verify pin connections at the controller card with an ohmmeter or you may find a reverse wired connector.

| 34 pin co:nector | H-37 Signal | $8^{\circ}$ Drive signal | 50-pin |
| :---: | :---: | :---: | :---: |
| 6 | DS3 (1EW UG43) | WRITE CUPRENT SW | 2 |
| 8 | INDEX | * | 20 |
| 10 | DS0 | DS1 | 26 |
| 12 | DS1 | DS2 | 28 |
| 14 | DS2 | DS3 | 30 |
| 16 | MOTOR | To external Relay (see MOTOR below) | No Connect |
| 18 | DIR | direction seect | 34 |
| 20 | STEP | STEP | 36 |
| 22 | IR DATA | urite data | 38 |
| 24 | UR GATE | IRITE GATE | 40 |
| 26 | TK00 | TRACX 0 | 42 |
| 28 | URPT | URITE PROTECT | 44 |
| 30 | READ DATA | READ DATA | 46 |
| 32 | SIDE SEIECT | SIDE SEECT | 14 |

## Motor

The driver software has a timed motor routine for those who prefer not to run the drive motors continuously. This allows the motor lead +5 V from the controller to operate a solid state relay or equivalent for switching the 115 V to the drive motors. The motor(s) will then switch on as required and then the drive motor after a suitable delay (say, a 30 second period of inactivity) will switch off.

## Software

My primary operating mode is HDOS so this was the first driver to create for the $8^{\prime \prime}$ system. A copy of the H/Z-37 device driver was disassembled. The analysis of the code took about four weeks, rewrite about two more, debugging took another 3 weeks.
The resultant driver has the following characteristics:

1. Set option for number of drives (1-7), allowing minimum use of GRT space taken from HDOS user memory .
-Line select for up to 3 drives.
-Binary select for 4-7 drives on lines DS0-2.
2. Separate set option of step time for each drive.
-Step times are $3,6,10$, and 15 milliseconds.
3. Display of presently set options for all enabled devices.
4. Use of the driver with HDOS Init.
-Will give selection of density and number of sides.
-Sector skew is variable. Track 0 has no skew allowing the block read boot code in MTR-90 to load in less than a second.
-All other tracks have the sector sequence skewed 5 sectors. This skew was optimized by trial, MBASIC loads in less than 3 seconds.
Media8 - A media check program that writes a test pattern over an entire disk and then reads back all sectors verifying the data and reporting bad sector groups.
DUPDK8 - A disk duplicating program to format and copy is currently being tested.

Shugart 800-1 \& 801

| Internal Select Jumper or opti |  | Coment |
| :---: | :---: | :---: |
| $\chi$ | $\chi$ |  |
| DS | $\chi$ |  |
| H. | 0 |  |
| A | $\chi$ |  |
| B | $\chi$ |  |
| 800-801 | $\chi$ | WHICHEVER TYPE OF DRIVE |
| T2 | $\chi$ |  |
| T1 | 0 |  |
| DC | $\chi$ |  |
| D | 0 |  |
| c | 0 |  |
| 1 | 0 |  |
| $R$ | $\chi$ |  |
| S | 0 |  |
| DS1-4 | $\chi$ | WHICHEVER DR. SEAECTED |
| T 3-6 | ALL | TERWINATE LAST IN CHAIN ONEY |
| 2 | x |  |

Automount - A utility intended for use with any DVD that has mountable units. All command line specified devices will have any units with disks in the drives mounted.
CPM
BIOS.SYS modifications are currently being worked out. As CPM is not my favorite system, its lowest on the list of things to do!

## Configuring Drives

The following tables can be used as a guide for configuring a specific drive to the system. The information here should be sufficient to allow an "oddball" drive to be properly configured.
$\mathrm{X}=$ connected or jumper in; $0=$ no connection
Note: Persons interested in making these modifications should contact Ed Blayer, 1008 West Bay Ave., Barnegat, NJ 08005, for software listings, etc. Ed will also make modifications to your H/Z-37 board upon request. Contact Ed concerning price and delivery.

| Shugart 850 \& 851 |  |  |
| :---: | :---: | :---: |
| Internal Selectable Juaper or option |  |  |
| dip shunt |  |  |
| R | $x$ |  |
| 1 | $\chi$ |  |
| S | X |  |
| H. | 0 | HEAD LOAD ON SELECT |
| A | X |  |
| B | x |  |
| $\chi$ | x |  |
| $z$ | $x$ |  |
| MHPERED OPTIOWS |  |  |
| DS1, DS2, DS3, DS4 : ONE ONLY FOR SY0: , 1,2 |  |  |
| RP9 | $\chi$ | LAST DRIVE IN CHAIN ONLY! |
| 850-851 | $\chi$ | 850 POSITION |
| DS | $\chi$ | STEPPER PIR ON SELECT |
| 52 | $\chi$ | STD. SIDE SELECT |
| TS-FS | $\chi$ | JIPER FS POSITION |
| RS-RIM | $\chi$ | M MPER RS POSITION |
| IT | x |  |
| -12,-5 | $\chi$ | POSITION TO SUIT PUR SUPPLY |
| ALL OTHER OPTION PLUG POSITIONS OPEN |  |  |

Note: For more than 3 drives a binary select option must be fitted to the drives.

