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# Technical Manual

## Appendices Z-100 Series Computers

593-0052-02  
CONSISTS OF

MANUAL  
595-2960-02

FLYSHEET  
597-2922-02

TAB SET  
597-2931

TM-100

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## Description

In Appendix A, you are furnished with the IEEE Task 696.1/D2, S-100 Bus Standards.

In Appendices B and C, you are furnished the architecture and instruction sets for the Intel 8085 microprocessor.

The 8085 microprocessor is an 8-bit general purpose microprocessor that is capable of accessing up to 64K bytes of memory and has status lines for controlling large systems.

Contained in the 8085 microprocessor are the functions of clock generation, system bus control, and interrupt priority selection, in addition to execution of the instruction set.

The 8085 microprocessor implements a group of instructions that move data between registers, between a register and memory, and between a register and an I/O port. It also has arithmetic and logic instructions, and machine control instruction. The CPU recognizes these instructions only when they are coded in binary form.

The architecture and instruction set for the 8088 microprocessor are located in the iAPX 88 Book, which is included as part of this Appendix.

The 8088 microprocessor is an 8-bit microprocessor. It combines a 16-bit microprocessor internal architecture with an easy to use 8-bit bus interface. Most of the bus lines are identical in function to the 8085A.

The 8088 is totally software compatible with the 16-bit 8086 CPU. All the power of the 8086 16-bit instruction set is available in the 8-bit 8088.

With the 16-bit internal architecture, the 8088 provides 16-bit wide registers, data paths, a 16-bit ALU, and a set of powerful 16-bit instructions identical to the ones found in the 8086 microprocessor. It also provides a 20-bit memory address range and a 16-bit input/output port address range for I/O cycles. This gives the 8088 a full megabyte of memory addressability and 64K bytes of I/O addressability.

The instruction set for the 8088 includes a full complement of arithmetic operations including addition, subtraction, multiplication, and division, on 8-bit or 16-bit quantities. It also has a complete set of string manipulation operations for performance and flexibility in application where large amounts of data are involved.

Appendix D provides you with the data sheets and programming instruction for the major IC's.

## APPENDIX A

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# **S100 Bus Specifications**

The following pages provide you 1EEE  
Task 696.1/D2, S-100 Bus Standards.



## APPENDIX B

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### **8085 Architecture**

The following pages are reprinted with  
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# 8085A ARCHITECTURE

## 2.1 WHAT THE 8085A IS

The 8085A is an 8-bit general-purpose microprocessor that is very cost-effective in small systems because of its extraordinarily low hardware overhead requirements. At the same time it is capable of accessing up to 64K bytes of memory and has status lines for controlling large systems.

## 2.2 WHAT'S IN THE 8085A

In the 8085A microprocessor are contained the functions of clock generation, system bus control, and interrupt priority selection, in addition to execution of the instruction set. (See Figure 2-1.) The 8085A transfers data on an 8-bit, bi-directional 3-state bus ( $AD_{0,7}$ ) which is time-multiplexed so as to also transmit the eight lower-order address bits. An additional eight lines ( $A_{8-15}$ ) expand the MCS-85 system memory addressing capability to 16 bits, thereby allowing 64K bytes of memory to be accessed directly by the CPU. The 8085A CPU (central processing unit) generates control signals that can be used to select appropriate external devices and

functions to perform READ and WRITE operations and also to select memory or I/O ports. The 8085A can address up to 256 different I/O locations. These addresses have the same numerical values (00 through FFH) as the first 256 memory addresses; they are distinguished by means of the  $IO/\overline{M}$  output from the CPU. You may also choose to address I/O ports as memory locations (i.e., memory-map the I/O, Section 3.2).

### 2.2.1 Registers

The 8085A, like the 8080, is provided with internal 8-bit registers and 16-bit registers. The 8085A has eight addressable 8-bit registers. Six of them can be used either as 8-bit registers or as 16-bit register pairs. Register pairs are treated as though they were single, 16-bit registers; the high-order byte of a pair is located in the first register and the low-order byte is located in the second. In addition to the register pairs, the 8085A contains two more 16-bit registers.

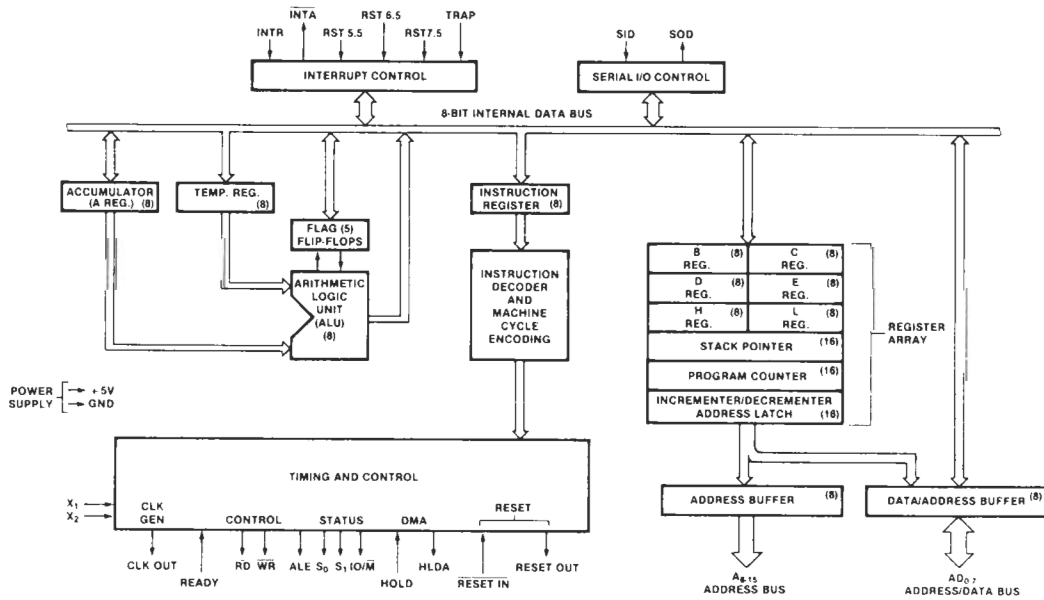


FIGURE 2-1 8085A CPU FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The 8085A's CPU registers are distinguished as follows:

- The **accumulator** (ACC or A Register) is the focus of all of the accumulator instructions (Table 4-1), which include arithmetic, logic, load and store, and I/O instructions. It is an 8-bit register only. (However, see **Flags**, in this list.)
- The **program counter** (PC) always points to the memory location of the next instruction to be executed. It always contains a 16-bit address.
- **General-purpose registers** BC, DE, and HL may be used as six 8-bit registers or as three 16-bit registers, interchangeably, depending on the instruction being performed. HL functions as a **data pointer** to reference memory addresses that are either the sources or the destinations in a number of instructions. A smaller number of instructions can use BC or DE for indirect addressing.
- The **stack pointer** (SP) is a special data pointer that always points to the stack top (next available stack address). It is an indivisible 16-bit register.
- The **flag register** contains five one-bit flags, each of which records processor status information and may also control processor operation. (See following paragraph.)

### 2.2.2 Flags

The five flags in the 8085A CPU are shown below:

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
| S              | Z              |                | AC             |                | P              |                | CY             |

The **carry flag** (CY) is set and reset by arithmetic operations. Its status can be directly tested by a program. For example, the addition of two one-byte numbers can produce an answer that does not fit into one byte:

| HEXIDECIMAL | BINARY            |
|-------------|-------------------|
| AEH         | 1 0 1 0 1 1 1 0   |
| + 74H       | 0 1 1 1 0 1 0 0   |
| 122H        | 1 0 0 1 0 0 0 1 0 |

↑  
Carry bit sets carry flag to 1

An addition operation that results in an overflow out of the high-order bit of the accumulator sets the carry flag. An addition operation that does not result in an overflow clears the carry flag. (See 8080/8085 Assembly Language Programming Manual for further details.) The carry flag also acts as a "borrow" flag for subtract operations.

The **auxiliary carry flag** (AC) indicates overflow out of bit 3 of the accumulator in the same way that the carry flag indicates overflow out of bit 7. This flag is commonly used in BCD (binary coded decimal) arithmetic.

The **sign flag** is set to the condition of the most significant bit of the accumulator following the execution of arithmetic or logic instructions. These instructions use bit 7 of data to represent the sign of the number contained in the accumulator. This permits the manipulation of numbers in the range from -128 to +127.

The **zero flag** is set if the result generated by certain instructions is zero. The zero flag is cleared if the result is not zero. A result that has a carry but has a zero answer byte in the accumulator will set both the carry flag and the zero flag. For example,

| HEXADECIMAL | BINARY            |
|-------------|-------------------|
| A7H         | 1 0 1 0 0 1 1 1   |
| + 59H       | + 0 1 0 1 1 0 0 1 |
| 100H        | 1 0 0 0 0 0 0 0 0 |

↑  
Carry bit

↑  
Eight zero bits set zero flag to 1

Incrementing or decrementing certain CPU registers with a zero result will also set the zero flag.

The **parity flag** (P) is set to 1 if the parity (number of 1-bits) of the accumulator is even. If odd, it is cleared.

### 2.2.3 Stack

The stack pointer maintains the address of the last byte entered into the stack. The stack pointer can be initialized to use any portion of read-write memory as a stack. The stack pointer is decremented each time data is pushed onto the stack and is incremented each time data is popped off the stack (i.e., the stack grows downward in terms of memory address, and the stack "top" is the lowest numerical address represented in the stack currently in use). Note that the stack pointer is always incremented or decremented by two bytes since all stack operations apply to register pairs.

**FUNCTIONAL DESCRIPTION**

**2.2.4 Arithmetic-Logic Unit (ALU)**

The ALU contains the accumulator and the flag register (described in Sections 2.2.1 and 2.2.2) and some temporary registers that are inaccessible to the programmer.

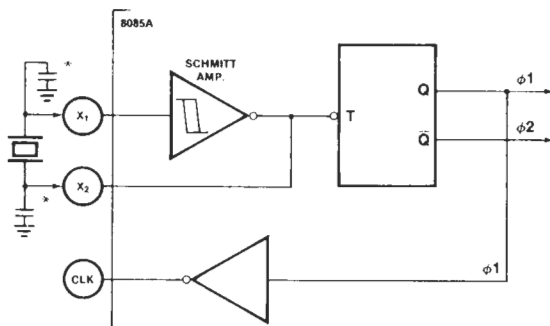
Arithmetic, logic, and rotate operations are performed by the ALU. The results of these operations can be deposited in the accumulator, or they can be transferred to the internal data bus for use elsewhere.

**2.2.5 Instruction Register and Decoder**

During an instruction fetch, the first byte of an instruction (containing the opcode) is transferred from the internal bus to the 8-bit instruction register. (See Figure 2-1.) The contents of the instruction register are, in turn, available to the instruction decoder. The output of the decoder, gated by timing signals, controls the registers, ALU, and data and address buffers. The outputs of the instruction decoder and internal clock generator generate the state and machine cycle timing signals.

**2.2.6 Internal Clock Generator**

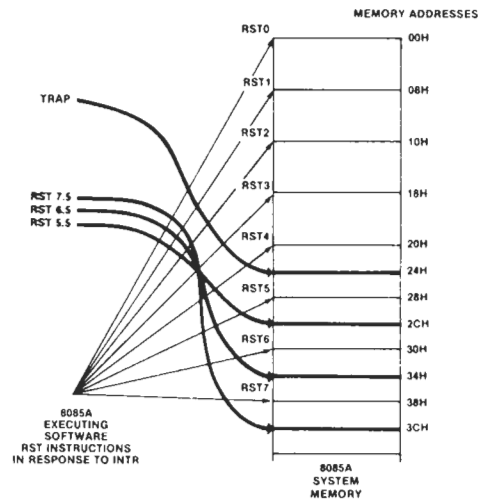
The 8085A CPU incorporates a complete clock generator on its chip, so it requires only the addition of a quartz crystal to establish timing for its operation. (It will accept an external clock input at its X<sub>1</sub> input instead, however.) A suitable crystal for the standard 8085A must be parallel-resonant at a fundamental of 6.25 MHz or less, twice the desired internal clock frequency. The 8085A-2 will operate with crystal of up to 10 MHz. The functions of the 8085A internal clock generator are shown in Figure 2-2. A Schmitt trigger is used interchangeably as oscillator or



\* EXTERNAL CAPACITORS REQUIRED ONLY FOR CRYSTAL FREQUENCIES : 4MHz.

**FIGURE 2-2 8085A CLOCK LOGIC**

as input conditioner, depending upon whether a crystal or an external source is used. The clock circuitry generates two nonoverlapping internal clock signals,  $\phi_1$  and  $\phi_2$  (see Figure 2-2).  $\phi_1$  and  $\phi_2$  control the internal timing of the 8085A and are not directly available on the outside of the chip. The external pin CLK is a buffered, inverted version of  $\phi_1$ . CLK is half the frequency of the crystal input signal and may be used for clocking other devices in the system.



**FIGURE 2-3 8085A HARDWARE AND SOFTWARE RST BRANCH LOCATIONS**

**2.2.7 Interrupts**

The five hardware interrupt inputs provided in the 8085A are of three types. INTR is identical with the 8080A INT line in function; i.e., it is maskable (can be enabled or disabled by EI or DI software instructions), and causes the CPU to fetch in an RST instruction, externally placed on the data bus, which vectors a branch to any one of eight fixed memory locations (Restart addresses). (See Figure 2-3.) INTR can also be controlled by the 8259 programmable interrupt controller, which generates CALL instructions instead of RSTs, and can thus vector operation of the CPU to a preprogrammed subroutine located anywhere in your system's memory map. The RST 5.5, RST 6.5, and RST 7.5 hardware interrupts are different in function in that they are maskable through the use of the SIM

### FUNCTIONAL DESCRIPTION

instruction, which enables or disables these interrupts by clearing or setting corresponding mask flags based on data in the accumulator. (See Figure 2-4.) You may read the status of the interrupt mask previously set by performing a RIM instruction. Its execution loads into the accumulator the following information. (See Figure 2-5.)

- Current interrupt mask status for the RST 5.5, 6.5, and 7.5 hardware status.
- Current interrupt enable flag status (except that immediately following TRAP, the IE flag status **preceding** that interrupt is loaded).
- RST 5.5, 6.5, and 7.5 interrupts pending.

RST 5.5, 6.5, and 7.5 are also subject to being enabled or disabled by the EI and DI instructions, respectively. INTR, RST 5.5, and RST 6.5 are level-sensitive, meaning that these inputs may be acknowledged by the processor when they are held at a high level. RST 7.5 is edge-sensitive, meaning that an internal flip-flop in the 8085A registers the occurrence of an interrupt the instant a rising edge appears on the RST 7.5 input line. This input need not be held high; the flip-flop will remain set until it is cleared by one of three possible actions:

- The 8085A responds to the interrupt, and sends an internal reset signal to the RST 7.5 flip-flop. (See Figure 2-6A.)

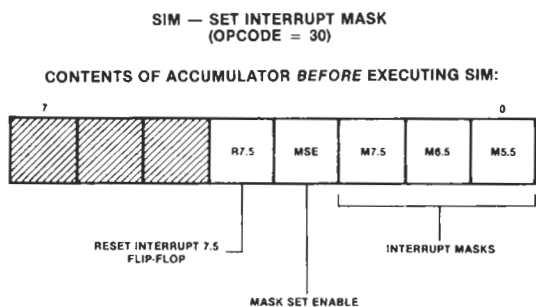


FIGURE 2-4 INTERRUPT MASKS SET USING SIM INSTRUCTION

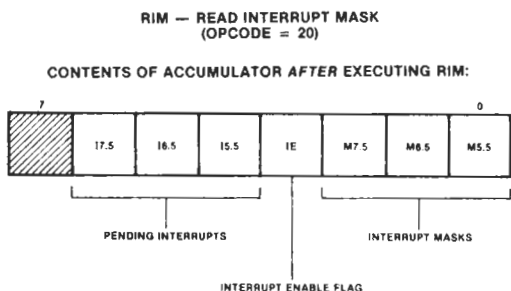


FIGURE 2-5 RIM — READ INTERRUPT MASK

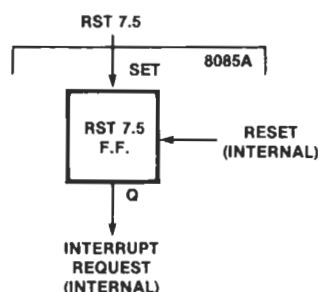


FIGURE 2-6A RST 7.5 FLIP FLOP

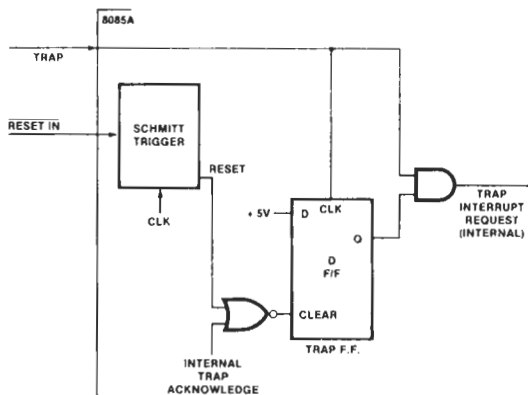


FIGURE 2-6B TRAP INTERRUPT INPUTS

FIGURE 2-6 RST 7.5 AND TRAP INTERRUPT INPUTS

FUNCTIONAL DESCRIPTION

- The 8085A, before responding to the RST 7.5 interrupt, receives a RESET IN signal from an external source; this also activates the internal reset.
- The 8085A executes a SIM instruction, with accumulator bit 4 previously set to 1. (See Figure 2-4.)

The third type of hardware interrupt is TRAP. This input is not subject to any mask or interrupt enable/disable instruction. The receipt of a positive-going edge on the TRAP input triggers the processor's hardware interrupt sequence, but the pulse must be held high until acknowledged internally (see Figure 2-6B).

The sampling of all interrupts occurs on the descending edge of CLK, one cycle before the end of the instruction in which the interrupt input is activated. To be recognized, a valid interrupt must occur at least 160 ns before sampling time in the 8085A, or 150 ns in the 8085A-2. This means that to guarantee being recognized, RST 5.5 and 6.5 and TRAP need to be held on for at least 17 clock states plus 160 ns (150 for 8085A-2), assuming that the interrupt might arrive just barely too late to be acknowledged during a particular instruction, and that the following instruction might be an 18-state CALL. This timing assumes no WAIT or HOLD cycles are used.

The way interrupt masks are set and read is described in Chapter 4 under the RIM (read in-

terrupt mask) and SIM (set interrupt mask) instruction listings. Interrupt functions and their priorities are shown in the table that follows.

| Name    | Priority | Address (1)<br>Branched to<br>when inter-<br>rupt occurs | Type<br>Trigger                                   |
|---------|----------|--|---|
| TRAP    | 1        | 24H  | Rising edge<br>AND high<br>level until<br>sampled |
| RST 7.5 | 2        | 3CH  | Rising edge<br>(latched)                          |
| RST 6.5 | 3        | 34H  | High level<br>until sam-<br>pled                  |
| RST 5.5 | 4        | 2CH  | High level<br>until sam-<br>pled                  |
| INTR    | 5        | (2)  | High level<br>until sam-<br>pled                  |

NOTES:

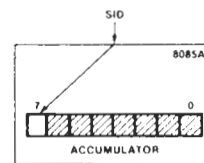
- (1) In the case of TRAP and RST 5.5-7.5, the contents of the Program Counter are pushed onto the stack before the branch occurs.
- (2) Depends on the instruction that is provided to the 8085A by the 8259 or other circuitry when the interrupt is acknowledged.

2.2.8 Serial Input and Output

The SID and SOD pins help to minimize chip count in small systems by providing for easy interface to a serial port using software for timing and for coding and decoding of the data. Each time a RIM instruction is executed, the status of the SID pin is read into bit 7 of the accumulator. RIM is thus a dual-purpose instruction. (See Chapter 4.) In similar fashion, SIM is used to latch bit 7 of the accumulator out to the SOD output via an internal flip-flop, providing that bit 6 of the accumulator is set to 1. (See Figure 2-7.) Section 2.3.8 describes SID and SOD timing.

SID can also be used as a general purpose TEST input and SOD can serve as a one-bit control output.

EFFECT OF RIM INSTRUCTION



EFFECT OF SIM INSTRUCTION

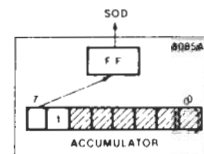


FIGURE 2-7 EFFECT OF RIM AND SIM INSTRUCTIONS ON SERIAL DATA LINES

## FUNCTIONAL DESCRIPTION

### 2.3 HOW THE MCS-85 SYSTEM WORKS

The 8085A CPU generates signals that tell peripheral devices what type of information is on the multiplexed Address/Data bus and from that point on the operation is almost identical to the MCS-80™ CPU Group. A multiplexed bus structure was chosen because it freed device pins so that more functions could be integrated on the 8085A and other components of the family. The multiplexed bus is designed to allow complete compatibility to existing peripheral

components with improved timing margins and access requirements. (See Figure 2-8.)

To enhance the system integration of MCS-85, several special components with combined memory and I/O were designed. These new devices directly interface to the multiplexed bus of the 8085A. The pin locations of the 8085A and the special peripheral components are assigned to minimize PC board area and to allow for efficient layout. The details on peripheral components are contained in subsequent paragraphs of this chapter and in Chapters 5 and 6.

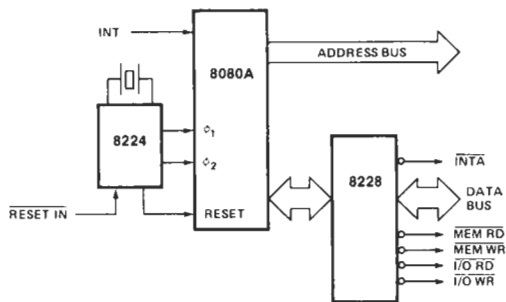


FIGURE 2-8A MCS-80™ CPU GROUP

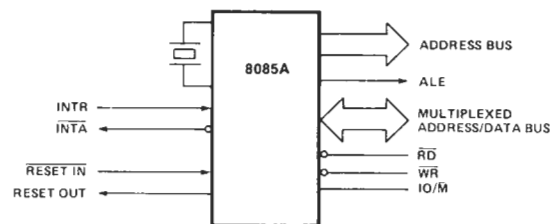


FIGURE 2-8B MCS-85™ CPU/8085A (MCS-80 COMPATIBLE FUNCTIONS)

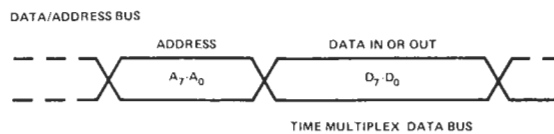


FIGURE 2-8C MULTIPLEXED BUS TIMING

FIGURE 2-8 BASIC CPU FUNCTIONS

FUNCTIONAL DESCRIPTION

2.3.1 Multiplexed Bus Cycle Timing

The execution of any 8085A program consists of a sequence of READ and WRITE operations, of which each transfers a byte of data between the 8085A and a particular memory or I/O address. These READ and WRITE operations are the only communication between the processor and the other components, and are all that is necessary to execute any instruction or program.

Each READ or WRITE operation of the 8085A is referred to as a machine cycle. The execution of each instruction by the 8085A consists of a sequence of from one to five machine cycles, and each machine cycle consists of a minimum of from three to six clock cycles (also referred to as T states). Consider the case of the Store Accumulator Direct (STA) instruction, shown in Figure 2-9. The STA instruction causes the contents of the accumulator to be stored at the direct address specified in the second and third bytes of the instruction. During the first machine cycle ( $M_1$ ), the CPU puts the contents of the program counter (PC) on the address bus and performs a MEMORY READ cycle to read from memory the opcode of the next instruction (STA). The  $M_1$  machine cycle is also referred to as the OPCODE FETCH cycle, since it fetches the operation code of the next instruction. In the fourth clock cycle ( $T_4$ ) of  $M_1$ , the CPU interprets the data read in and recognizes it as the opcode of the STA instruction. At this point the

CPU knows that it must do three more machine cycles (two MEMORY READs and one MEMORY WRITE) to complete the instruction.

The 8085A then increments the program counter so that it points to the next byte of the instruction and performs a MEMORY READ machine cycle ( $M_2$ ) at address (PC + 1). The accessed memory places the addressed data on the data bus for the CPU. The 8085A temporarily stores this data (which is the low-order byte of the direct address) internally in the CPU. The 8085A again increments the program counter to location (PC + 2) and reads from memory ( $M_3$ ) the next byte of data, which is the high-order byte of the direct address.

At this point, the 8085A has accessed all three bytes of the STA instruction, which it must now execute. The execution consists of placing the data accessed in  $M_2$  and  $M_3$  on the address bus, then placing the contents of the accumulator on the data bus, and then performing a MEMORY WRITE machine cycle ( $M_4$ ). When  $M_4$  is finished, the CPU will fetch ( $M_1$ ) the first byte of the next instruction and continue from there.

State Transition Sequence

As the preceding example shows, the execution of an instruction consists of a series of machine cycles whose nature and sequence is determined by the opcode accessed in the  $M_1$

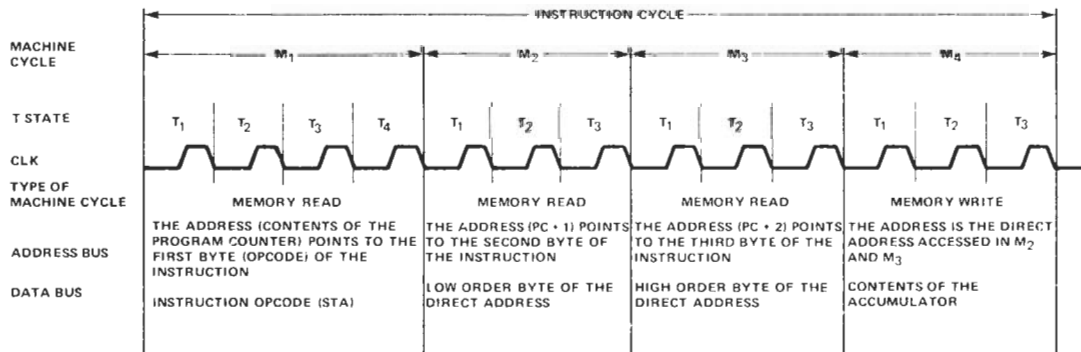


FIGURE 2-9 CPU TIMING FOR STORE ACCUMULATOR DIRECT (STA) INSTRUCTION

FUNCTIONAL DESCRIPTION

| MACHINE CYCLE          | STATUS |    |    | CONTROL |    |      |
|------------------------|--------|----|----|---------|----|------|
|                        | IO/M   | S1 | S0 | RD      | WR | INTA |
| OPCODE FETCH (OF)      | 0      | 1  | 1  | 0       | 1  | 1    |
| MEMORY READ (MR)       | 0      | 1  | 0  | 0       | 1  | 1    |
| MEMORY WRITE (MW)      | 0      | 0  | 1  | 1       | 0  | 1    |
| I/O READ (IOR)         | 1      | 1  | 0  | 0       | 1  | 1    |
| I/O WRITE (IOW)        | 1      | 0  | 1  | 1       | 0  | 1    |
| INTR ACKNOWLEDGE (INA) | 1      | 1  | 1  | 1       | 1  | 0    |
| BUS IDLE (BI): DAD     | 0      | 1  | 0  | 1       | 1  | 1    |
| INA(RST/TRAP)          | 1      | 1  | 1  | 1       | 1  | 1    |
| HALT                   | TS     | 0  | 0  | TS      | TS | 1    |

0 = Logic "0" 1 = Logic "1" TS = High Impedance X = Unspecified

FIGURE 2-10 8085A MACHINE CYCLE CHART

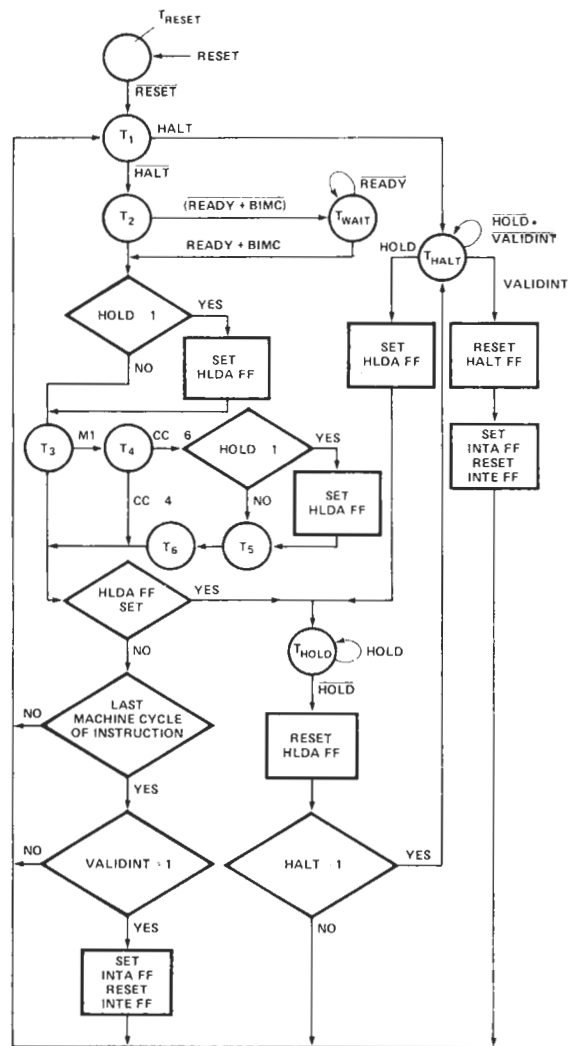
machine cycle. While no one instruction cycle will consist of more than five machine cycles, every machine cycle will be one of the seven types listed in Figure 2-10. These seven types of machine cycles can be differentiated by the state of the three status lines (IO/M, S<sub>0</sub>, and S<sub>1</sub>) and the three control signals (RD, WR, and INTA).

Most machine cycles consist of three T states, (cycles of the CLK output) with the exception of OPCODE FETCH, which normally has either four or six T states. The actual number of states required to perform any instruction depends on the instruction being executed, the particular machine cycle within the instruction cycle, and the number of WAIT and HOLD states inserted into each machine cycle through the use of the READY and HOLD inputs of the 8085A. The state transition diagram in Figure 2-11 illustrates how the 8085A proceeds in the course of a machine cycle. The state of various status and control signals, as well as the system buses, is shown in Figure 2-12 for each of the ten possible T states that the processor can be in.

Figure 2-11 also shows when the READY, HOLD, and interrupt signals are sampled, and how they modify the basic instruction sequence (T<sub>1</sub>-T<sub>6</sub> and T<sub>WAIT</sub>). As we shall see, the timings for each of the seven types of machine cycles are almost identical.

**OPCODE FETCH (OF):**

The OPCODE FETCH (OF) machine cycle is unique in that it has more than three clock cycles. This is because the CPU must interpret the opcode accessed in T<sub>1</sub>, T<sub>2</sub>, and T<sub>3</sub> before it can decide what to do next.



- NOTE: SYMBOL DEFINITION
- CPU STATE T<sub>n</sub>. ALL CPU STATE TRANSITIONS OCCUR ON THE FALLING EDGE OF CLK.
  - A DECISION (X) THAT DETERMINES WHICH OF SEVERAL ALTERNATIVE PATHS TO FOLLOW.
  - PERFORM THE ACTION X.
  - FLOWLINE THAT INDICATES THE SEQUENCE OF EVENTS.
  - FLOWLINE THAT INDICATES THE SEQUENCE OF EVENTS IF CONDITION X IS TRUE.
  - CC - NUMBER OF CLOCK CYCLES IN THE CURRENT MACHINE CYCLE.
  - BIMC - "BUS IDLE MACHINE CYCLE" - MACHINE CYCLE WHICH DOESN'T USE THE SYSTEM BUS.
  - VALIDINT - "VALID INTERRUPT" - AN INTERRUPT IS PENDING THAT IS BOTH ENABLED AND UNMASKED (MASKING ONLY APPLIES FOR RST 5.5, 6.5, AND 7.5 INPUTS).
  - HLDA FF - INTERNAL HOLD ACKNOWLEDGE FLIP FLOP. NOTE THAT THE 8085A SYSTEM BUSES ARE 3-STATE ONE CLOCK CYCLE AFTER THE HLDA FLIP FLOP IS SET.

FIGURE 2-11 8085A CPU STATE TRANSITION

## FUNCTIONAL DESCRIPTION

| Machine State      | Status & Buses |                    |                                 |                                  | Control                           |                   |                |
|--------------------|----------------|--------------------|---------------------------------|----------------------------------|-----------------------------------|-------------------|----------------|
|                    | S1,S0          | IO/ $\overline{M}$ | A <sub>8</sub> -A <sub>15</sub> | AD <sub>0</sub> -AD <sub>7</sub> | $\overline{RD}$ , $\overline{WR}$ | $\overline{INTA}$ | ALE            |
| T <sub>1</sub>     | X              | X                  | X                               | X                                | 1                                 | 1                 | 1 <sup>†</sup> |
| T <sub>2</sub>     | X              | X                  | X                               | X                                | X                                 | X                 | 0              |
| T <sub>WAIT</sub>  | X              | X                  | X                               | X                                | X                                 | X                 | 0              |
| T <sub>3</sub>     | X              | X                  | X                               | X                                | X                                 | X                 | 0              |
| T <sub>4</sub>     | 1              | 0*                 | X                               | TS                               | 1                                 | 1                 | 0              |
| T <sub>5</sub>     | 1              | 0*                 | X                               | TS                               | 1                                 | 1                 | 0              |
| T <sub>6</sub>     | 1              | 0*                 | X                               | TS                               | 1                                 | 1                 | 0              |
| T <sub>RESET</sub> | X              | TS                 | TS                              | TS                               | TS                                | 1                 | 0              |
| T <sub>HALT</sub>  | 0              | TS                 | TS                              | TS                               | TS                                | 1                 | 0              |
| T <sub>HOLD</sub>  | X              | TS                 | TS                              | TS                               | TS                                | 1                 | 0              |

0 = Logic "0" 1 = Logic "1" TS = High Impedance X = Unspecified

<sup>†</sup>ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

\*IO/ $\overline{M}$  = 1 during T<sub>4</sub>-T<sub>6</sub> states of RST and INA cycles.

FIGURE 2-12 8085A MACHINE STATE CHART

Figure 2-13 shows the timing relationships for an OF machine cycle. The particular instruction illustrated is DCX, whose timing for OF differs from other instructions in that it has six T states, while some instructions require only four T states for OF. In this discussion, as well as the following discussions, only the relative timing of the signals will be discussed; for the actual timings, refer to the data sheets of the individual parts in Chapters 5 and 6.

The first thing that the 8085A does at the beginning of every machine cycle is to send out three status signals (IO/ $\overline{M}$ , S1, S0) that define what type of machine cycle is about to take place. The IO/ $\overline{M}$  signal identifies the machine cycle as being either a memory reference or input/output operation. The S1 status signal identifies whether the cycle is a READ or WRITE operation. The S0 and S1 status signals can be used together (see Figure 2-10) to identify READ, WRITE, or OPCODE FETCH machine cycles as well as the HALT state. Referring to Figure 2-13, the 8085A will send out IO/ $\overline{M}$  = 0, S1 = 1, S0 = 1 at the beginning of the machine cycle to identify it as a READ from a memory location to obtain an opcode; in other words, it identifies the machine cycle as an OPCODE FETCH cycle.

The 8085A also sends out a 16-bit address at the beginning of every machine cycle to identify the particular memory location or I/O port that the machine cycle applies to. In the case of an OF cycle, the contents of the program counter is placed on the address bus. The high order byte (PCH) is placed on the A<sub>8</sub>-A<sub>15</sub> lines, where it will stay until at least T<sub>4</sub>. The low order byte (PCL) is placed on the AD<sub>0</sub>-AD<sub>7</sub> lines, whose three-state drivers are enabled if not found already on. Unlike the upper address lines, however, the information on the lower address lines will remain there for only one clock cycle, after which the drivers will go to their high impedance state, indicated by a dashed line in Figure 2-13. This is necessary because the AD<sub>0</sub>-AD<sub>7</sub> lines are time multiplexed between the address and data buses. During T<sub>1</sub> of every machine cycle, AD<sub>0</sub>-AD<sub>7</sub> output the lower 8-bits of address after which AD<sub>0</sub>-AD<sub>7</sub> will either output the desired data for a WRITE operation or the drivers will float (as is the case for the OF cycle), allowing the external device to drive the lines for a READ operation.

Since the address information on AD<sub>0</sub>-AD<sub>7</sub> is of a transitory nature, it must be latched either internally in special multiplexed-bus components like the 8155 or externally in parts like the 8212 8-bit latch. (See Chapter 3.) The 8085A provides a special timing signal, ADDRESS LATCH ENABLE (ALE), to facilitate the latching of A<sub>0</sub>-A<sub>7</sub>; ALE is present during T<sub>1</sub> of every machine cycle.

After the status signals and address have been sent out and the AD<sub>0</sub>-AD<sub>7</sub> drivers have been disabled, the 8085A provides a low level on  $\overline{RD}$  to enable the addressed memory device. The device will then start driving the AD<sub>0</sub>-AD<sub>7</sub> lines; this is indicated by the dashed line turning into a solid line in Figure 2-13. After a period of time (which is the access time of the memory) valid data will be present on AD<sub>0</sub>-AD<sub>7</sub>. The 8085A during T<sub>3</sub> will load the memory data on AD<sub>0</sub>-AD<sub>7</sub> into its instruction register and then raise  $\overline{RD}$  to the high level, disabling the addressed memory device. At this point, the 8085A will have finished accessing the opcode of the instruction. Since this is the first machine cycle (M<sub>1</sub>) of the instruction, the CPU will automatically step to T<sub>4</sub>, as shown in Figure 2-11.

During T<sub>4</sub>, the CPU will decode the opcode in the instruction register and decide whether to enter T<sub>5</sub> on the next clock or to start a new machine cycle and enter T<sub>1</sub>. In the case of the DCX instruction shown in Figure 2-13, it will enter T<sub>5</sub> and then T<sub>6</sub> before going to T<sub>1</sub>.



## FUNCTIONAL DESCRIPTION

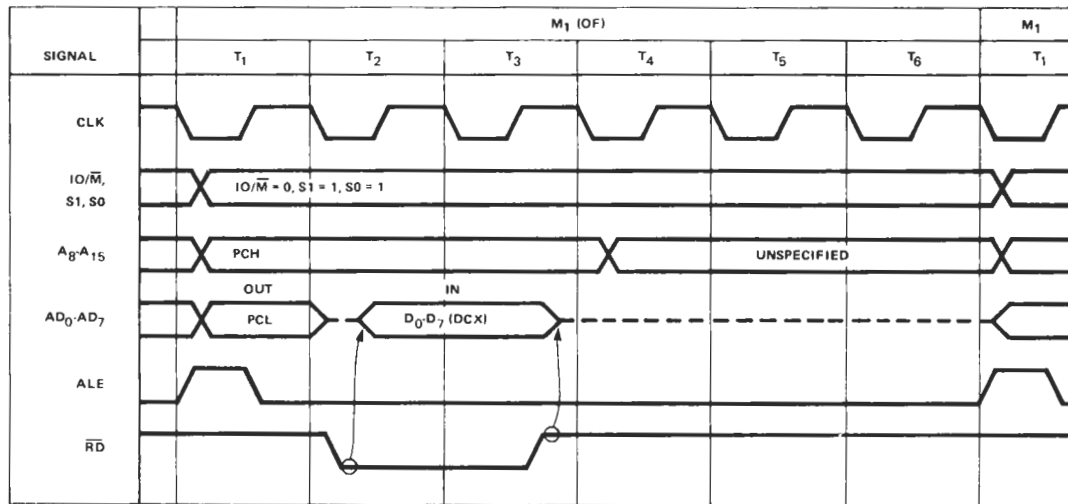


FIGURE 2-13 OPCODE FETCH MACHINE CYCLE (OF DCX INSTRUCTION)

During T<sub>5</sub> and T<sub>6</sub>, of DCX, the CPU will decrement the designated register. Since the A<sub>8</sub>-A<sub>15</sub> lines are driven by the address latch circuits, which are part of the incrementer/decrementer logic, the A<sub>8</sub>-A<sub>15</sub> lines may change during T<sub>5</sub> and T<sub>6</sub>. Because the value of A<sub>8</sub>-A<sub>15</sub> can vary during T<sub>4</sub>-T<sub>6</sub>, it is most important that all memory and I/O devices on the system bus qualify their selection with RD. If they don't use RD, they may be spuriously selected. Moreover, with a linear selection technique (Chapter 3), two or more devices could be simultaneously enabled, which could be potentially damaging. The generation of spurious addresses can also occur momentarily at address bus transitional periods in T<sub>1</sub>. Therefore, the selection of all memory and I/O devices must be qualified with RD or WR. Many new memory devices like the 8155 and 8355 have the RD input that internally is used to enable the data bus outputs, removing the need for externally qualifying the chip enable input with RD.

Figure 2-14 is identical to Figure 2-13 with one exception, which is the use of the READY line. As we can see in Figure 2-11, when the CPU is in T<sub>2</sub>, it examines the state of the READY line. If the READY line is high, the CPU will proceed to T<sub>3</sub> and finish executing the instruction. If the READY line is low, however, the CPU will enter T<sub>WAIT</sub> and stay there indefinitely until READY goes high. When the READY line does go high, the CPU will exit T<sub>WAIT</sub> and enter T<sub>3</sub>, in order to complete the machine cycle. As shown in

Figure 2-14, the external effect of using the READY line is to preserve the exact state of the processor signals at the end of T<sub>2</sub> for an integral number of clock periods, before finishing the machine cycle. This "stretching" of the system timing has the further effect of increasing the allowable access time for memory or I/O devices. By inserting T<sub>WAIT</sub> states, the 8085A can accommodate even the slowest of memories. Another common use of the READY line is to single-step the processor with a manual switch.

### 2.3.2 Read Cycle Timing

#### MEMORY READ (MR):

Figure 2-15 shows the timing of two successive MEMORY READ (MR) machine cycles, the first without a T<sub>WAIT</sub> state and the second with one T<sub>WAIT</sub> state. The timing during T<sub>1</sub>-T<sub>3</sub> is absolutely identical to the OPCODE FETCH machine cycle, with the exception that the status sent out during T<sub>1</sub> is IO/M = 0, S1 = 1, S0 = 0, identifying the cycles as a READ from a memory location. This differs from Figure 2-13 only in that S0 = 1 for an OF cycle, identifying that cycle as an OPCODE FETCH operation. Otherwise, the two cycles are identical during T<sub>1</sub>-T<sub>3</sub>.

A second difference occurs at the end of T<sub>3</sub>. As shown in Figure 2-11, the CPU always goes to T<sub>4</sub> from T<sub>3</sub> during M<sub>1</sub>, which is always an OF cycle. During all other machine cycles, the CPU will always go from T<sub>3</sub> to T<sub>1</sub> of the next machine cycle.

FUNCTIONAL DESCRIPTION

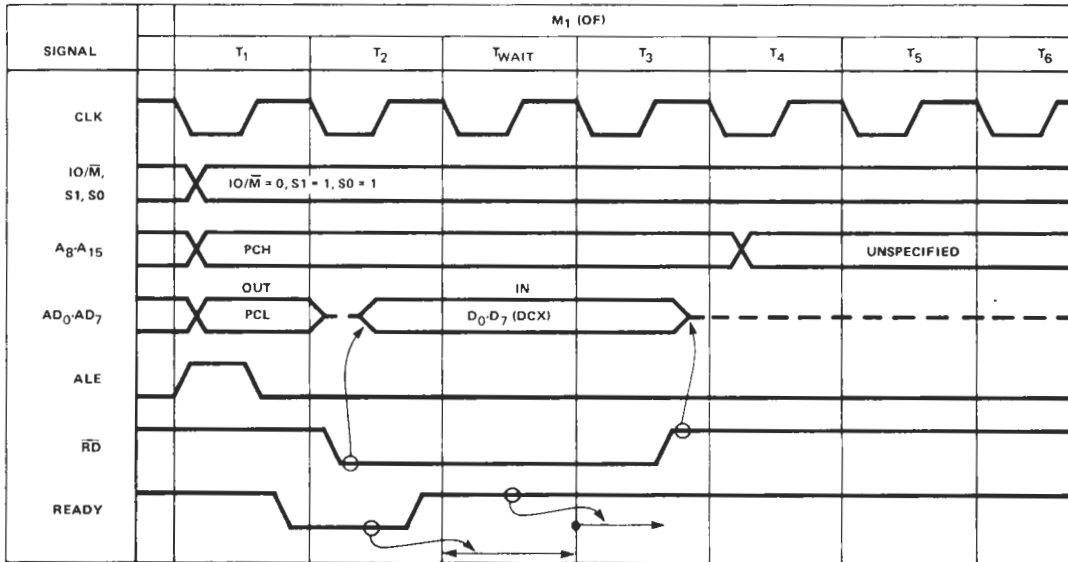


FIGURE 2-14 OPCODE FETCH MACHINE CYCLE WITH ONE WAIT STATE

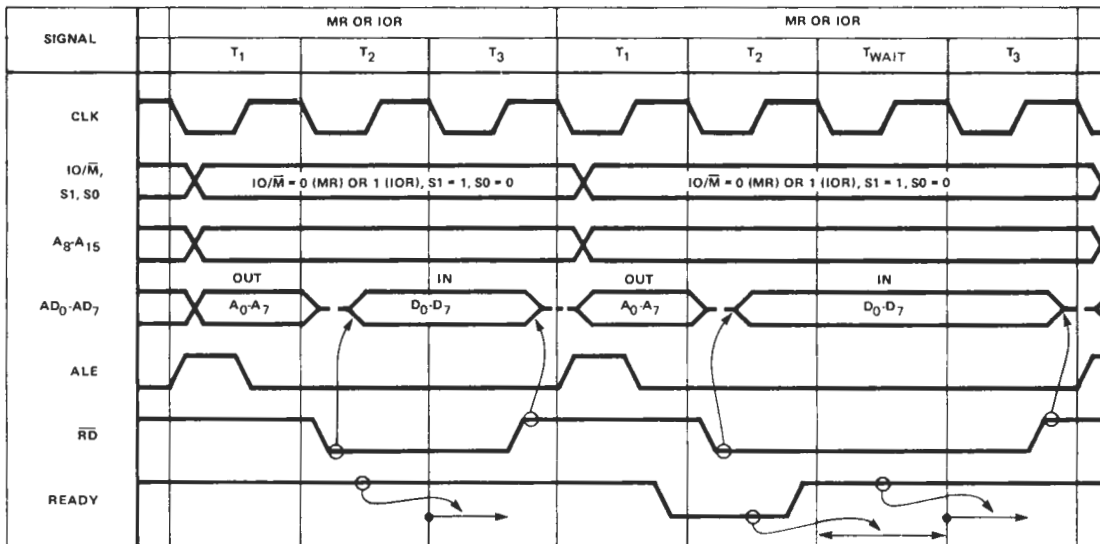


FIGURE 2-15 MEMORY READ (OR I/O READ) MACHINE CYCLES (WITH AND WITHOUT WAIT STATES)

## FUNCTIONAL DESCRIPTION

The memory address used in the OF cycle is always the contents of the program counter, which points to the current instruction, while the address used in the MR cycle can have several possible origins. Also, the data read in during an MR cycle is placed in the appropriate register, not the instruction register.

**I/O READ (IOR):**

Figure 2-15 also shows the timing of two successive I/O READ (IOR) machine cycles, the first without a  $T_{WAIT}$  state. As is readily apparent, the timing of an IOR cycle is identical to the timing of an MR cycle, with the exception of  $IO/\overline{M} = 0$  for MR and  $IO/\overline{M} = 1$  for IOR; recall that  $IO/\overline{M}$  status signal identifies the address of the current machine cycle as selecting either a memory location or an I/O port. The address used in the IOR cycle comes from the second byte (Port No.) of an INPUT instruction. Note that the I/O port address is duplicated onto both  $AD_0-AD_7$  and  $A_8-A_{15}$ . The IOR cycle can occur only as the third machine cycle of an INPUT instruction.

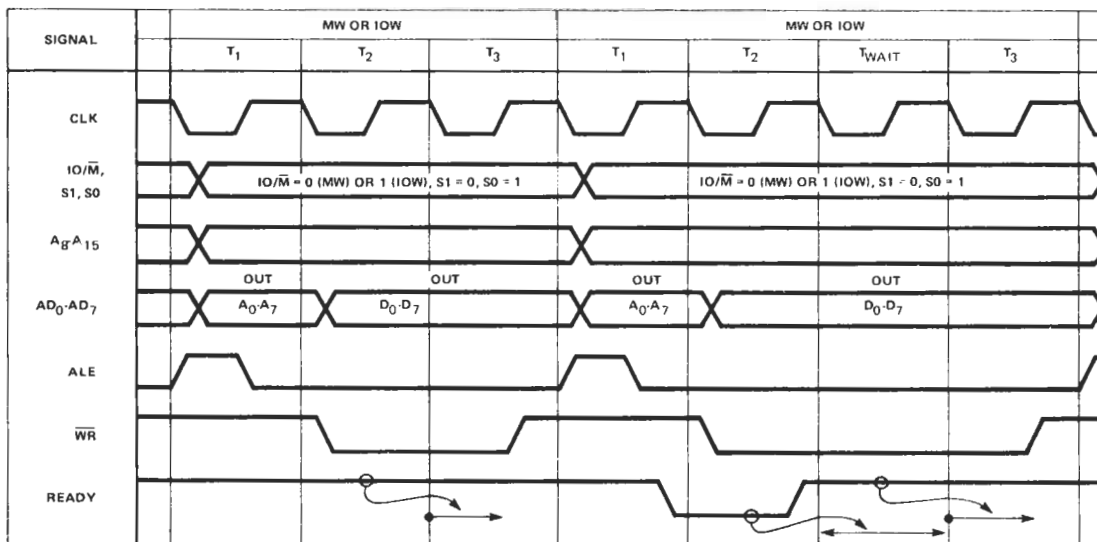
Note that the READY signal can be used to generate  $T_{WAIT}$  states for I/O devices as well as memory devices. By gating the READY signal with the proper status lines, one could generate  $T_{WAIT}$  states for memory devices only or for I/O devices only. By gating in the address lines, one can further qualify  $T_{WAIT}$  state generation by the particular devices being accessed.

**2.3.3 WRITE Cycle Timing****MEMORY WRITE (MW):**

Figure 2-16 shows the timing for two successive MEMORY WRITE (MW) machine cycles, the first without a  $T_{WAIT}$  state, and the second with one  $T_{WAIT}$  state. The 8085A sends out the status during  $T_1$  in a similar fashion to the OF, MR and IOR cycles, except that  $IO/\overline{M} = 0$ ,  $S_1 = 0$ , and  $S_0 = 1$ , identifying the current machine cycle as being a WRITE operation to a memory location.

The address is sent out during  $T_1$  in an identical manner to MR. However, at the end of  $T_1$ , there is a difference. While the  $AD_0-AD_7$  drivers were disabled during  $T_2-T_3$  of MR in expectation of the addressed memory device driving the  $AD_0-AD_7$  lines, the drivers are not disabled for MW. This is because the CPU must provide the data to be written into the addressed memory location. The data is placed on  $AD_0-AD_7$  at the start of  $T_2$ . The  $\overline{WR}$  signal is also lowered at this time to enable the writing of the addressed memory device. During  $T_2$ , the READY line is checked to see if a  $T_{WAIT}$  state is required. If READY is low,  $T_{WAIT}$  states are inserted until READY goes high. During  $T_3$ , the  $\overline{WR}$  line is raised, disabling the addressed memory device and thereby terminating the WRITE operation. The contents of the address and data lines are not changed until the next  $T_1$ , which directly follows.

Note that the data on  $AD_0-AD_7$  is not guaranteed to be stable before the falling edge



**FIGURE 2-16 MEMORY WRITE (OR I/O WRITE) MACHINE CYCLES (WITH AND WITHOUT WAIT STATES)**

FUNCTIONAL DESCRIPTION

of  $\overline{WR}$ . The  $AD_0-AD_7$  lines are guaranteed to be stable both before and after the rising edge of  $\overline{WR}$ .

**I/O WRITE (IOW):**

As Figure 2-16 shows, the timing for an I/O WRITE (IOW) machine cycle is the same as an MW machine cycle except that  $IO/\overline{M} = 0$  during the MW cycle and  $IO/\overline{M} = 1$  during the IOW cycle.

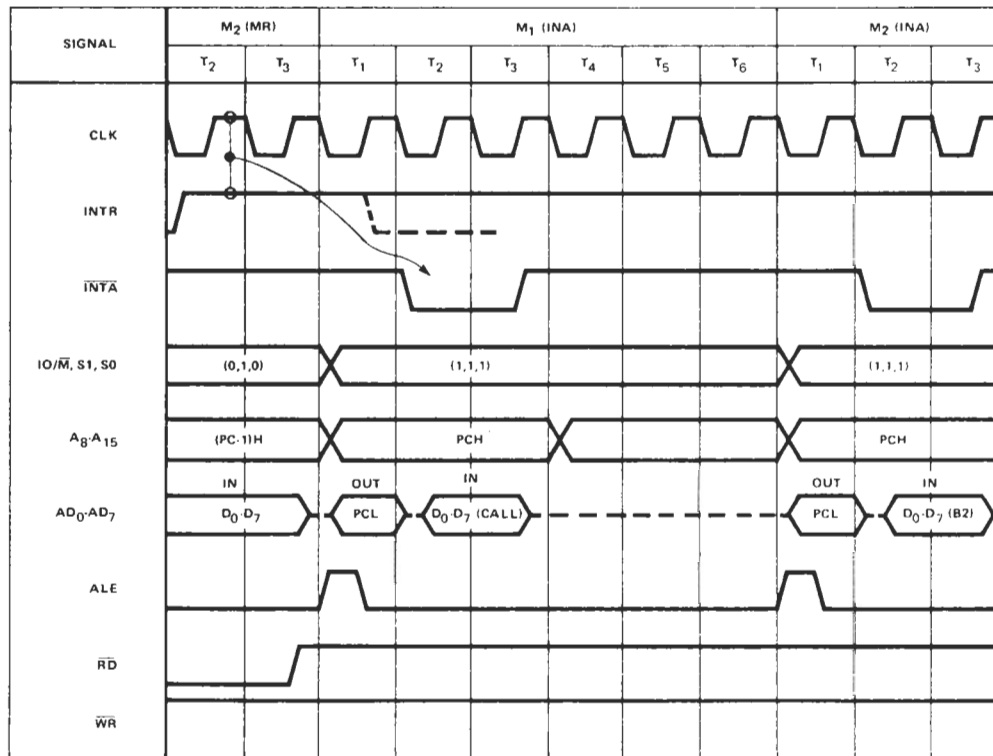
As with the IOR cycle discussed previously, the address used in an IOW cycle is the I/O port number which is duplicated on both the high and low bytes of the address bus. In the case of IOW, the port number comes from the second byte of an OUTPUT instruction as the instruction is executed.

**2.3.4 Interrupt Acknowledge (INA) Timing**

Figures 2-17 and 2-18 (a continuation of 2-17) depict the course of action the CPU takes in response to a high level on the INTR line if the INTE FF (interrupt enable flip-flop) has been set

by the EI instruction. The status of the TRAP and RST pins as well as INTR is sampled during the second clock cycle before  $M_1 \cdot T_1$ . If INTR was the only valid interrupt and if INTE FF is set, then the CPU will reset INTE FF and then enter an INTERRUPT ACKNOWLEDGE (INA) machine cycle. The INA cycle is identical to an OF cycle with two exceptions.  $\overline{INTA}$  is sent out instead of  $\overline{RD}$ . Also,  $IO/\overline{M} = 1$  during INA, whereas  $IO/\overline{M} = 0$  for OF. Although the contents of the program counter are sent out on the address lines, the address lines can be ignored.

When  $\overline{INTA}$  is sent out, the external interrupt logic must provide the opcode of an instruction to execute. The opcode is placed on the data bus and read in by the processor. If the opcode is the first byte of a multiple-byte instruction, additional  $\overline{INTA}$  pulses will be provided by the 8085A to clock in the remaining bytes. RESTART and CALL instructions are the most



**FIGURE 2-17 INTERRUPT ACKNOWLEDGE MACHINE CYCLES (WITH CALL INSTRUCTION IN RESPONSE TO INTR)**

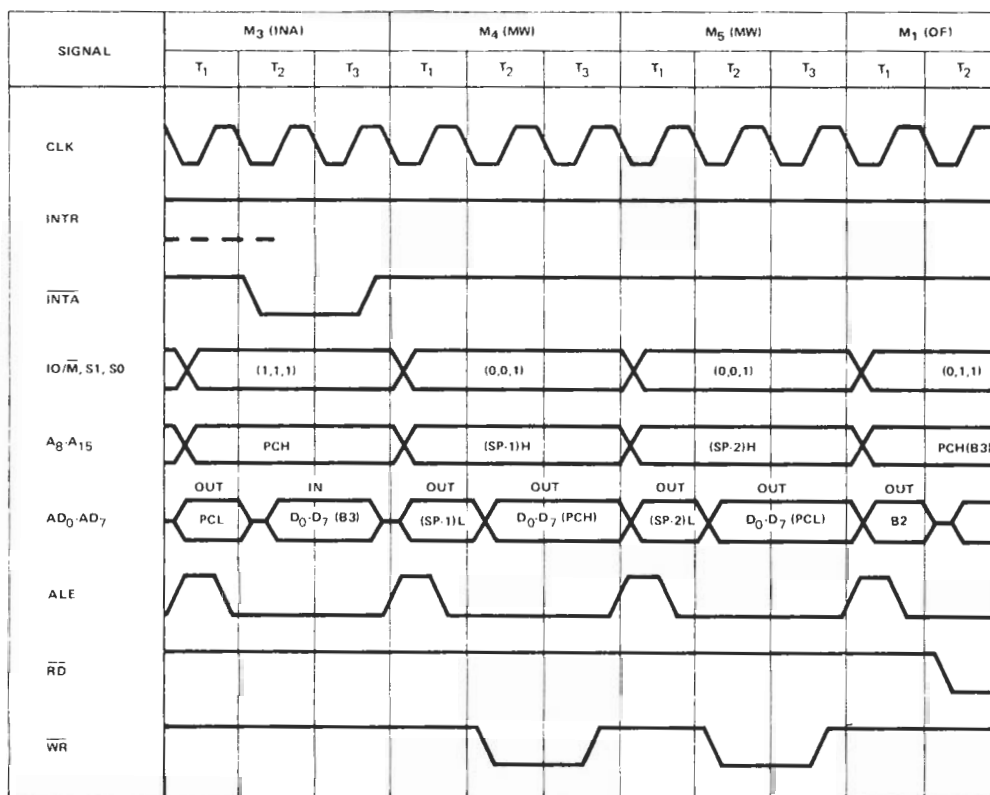
## FUNCTIONAL DESCRIPTION

logical choices, since they both force the processor to push the contents of the program counter onto the stack before jumping to a new location. In Figure 2-17 it is assumed that a CALL opcode is sent to the CPU during  $M_1$ . The CALL opcode could have been placed there by a device like the 8259 programmable interrupt controller.

After receiving the opcode, the processor then decodes it and determines, in this case, that the CALL instruction requires two more bytes. The CPU therefore performs a second INA cycle ( $M_2$ ) to access the second byte of the instruction from the 8259. The timing of this cycle is identical to  $M_1$ , except that it has only three T states.  $M_2$  is followed by another INA cycle ( $M_3$ ) to access the third byte of the CALL instruction from the 8259.

Now that the CPU has accessed the entire instruction used to acknowledge the interrupt, it will execute that instruction. Note that any instruction could be used (except EI or DI, the instructions which enable or disable interrupts), but the RESTART and CALL instructions are the most logical choices. Also notice that the CPU inhibited the incrementing of the program counter (PC) during the three INA cycles, so that the correct PC value can be pushed onto the stack during  $M_4$  and  $M_5$ .

During  $M_4$  and  $M_5$ , the CPU performs MEMORY WRITE machine cycles to write the upper and then lower bytes of the PC onto the top of the stack. The CPU then places the two bytes accessed in  $M_2$  and  $M_3$  into the lower and upper bytes of the PC. This has the effect of jumping the execution of the program to the location specified by the CALL instruction.



**FIGURE 2-18 INTERRUPT ACKNOWLEDGE MACHINE CYCLES (WITH CALL INSTRUCTION IN RESPONSE TO INTR)**

FUNCTIONAL DESCRIPTION

2.3.5 Bus Idle (BI) and HALT State

Most machine cycles of the 8085A are associated with either a READ or WRITE operation. There are two exceptions to this rule. The first exception takes place during M<sub>2</sub> and M<sub>3</sub> of the DAD instruction. The 8085A requires six internal T states to execute a DAD instruction, but it is not desirable to have M<sub>1</sub> be ten (four normal plus six extra) states long. Therefore, the CPU generates two extra machine cycles that do not access either the memory or the I/O. These cycles are referred to as BUS IDLE (BI) machine cycles. In the case of DAD, they are identical to MR cycles except that RD remains high and ALE is not generated. Note that READY is ignored during M<sub>2</sub> and M<sub>3</sub> of DAD.

The other time when the BUS IDLE machine cycle occurs is during the internal opcode generation for the RST or TRAP interrupts. Figure 2-19 illustrates the BI cycle generated in response to RST 7.5. Since this interrupt is rising-edge-triggered, it sets an internal latch; that latch is sampled at the falling edge of the next to the last T-state of the previous instruction. At this point the CPU must generate its own internal RESTART instruction which will (in subsequent machine cycles) cause the processor to push the program counter on the stack and to vector to location 3CH. To do this, it executes an OF machine cycle without issuing RD, generating the RESTART opcode instead. After M<sub>1</sub>, the CPU continues execution normally in all respects except that the state of the READY line is ignored during the BI cycle.

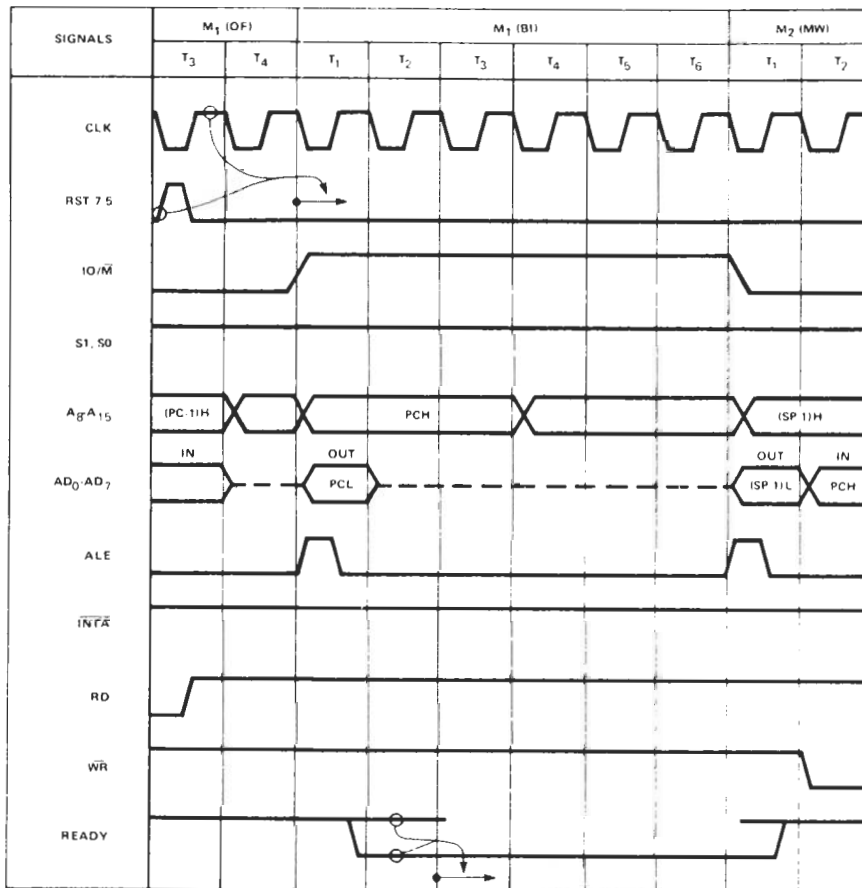


FIGURE 2-19 RST 7.5 BUS IDLE MACHINE CYCLE

## FUNCTIONAL DESCRIPTION

Figure 2-20 illustrates the BI cycle generated in response to RST 7.5 when a HALT instruction has just been executed and the CPU is in the  $T_{\text{HALT}}$  state, with its various signals floating. There are only two ways the processor can completely exit the  $T_{\text{HALT}}$  state, as shown in Figure 2-11. The first way is for RESET to occur, which always forces the 8085A to  $T_{\text{RESET}}$ . The second way to exit  $T_{\text{HALT}}$  permanently is for a valid interrupt to occur, which will cause the CPU to disable further interrupts by resetting INTE FF, and to then proceed to  $M_1 \cdot T_1$  of the next instruction. When the HOLD input is activated, the CPU will exit  $T_{\text{HALT}}$  for the duration of  $T_{\text{HOLD}}$  and then return to  $T_{\text{HALT}}$ .

In Figure 2-20 the RST 7.5 line is pulsed during  $T_{\text{HALT}}$ . Since RST 7.5 is a rising-edge-triggered interrupt, it will set an internal latch which is sampled during  $\text{CLK} = "1"$  of every  $T_{\text{HALT}}$  state (as well as during  $\text{CLK} = "1"$  two T states before any  $M_1 \cdot T_1$ .) The fact that the latched interrupt was high (assuming that  $\text{INTE FF} = 1$  and the RST 7.5 mask = 0) will force the CPU to exit the  $T_{\text{HALT}}$  state at the end of the next CLK period, and to enter  $M_1 \cdot T_1$ .

This completes our analysis of the timing of each of the seven types of machine cycles.

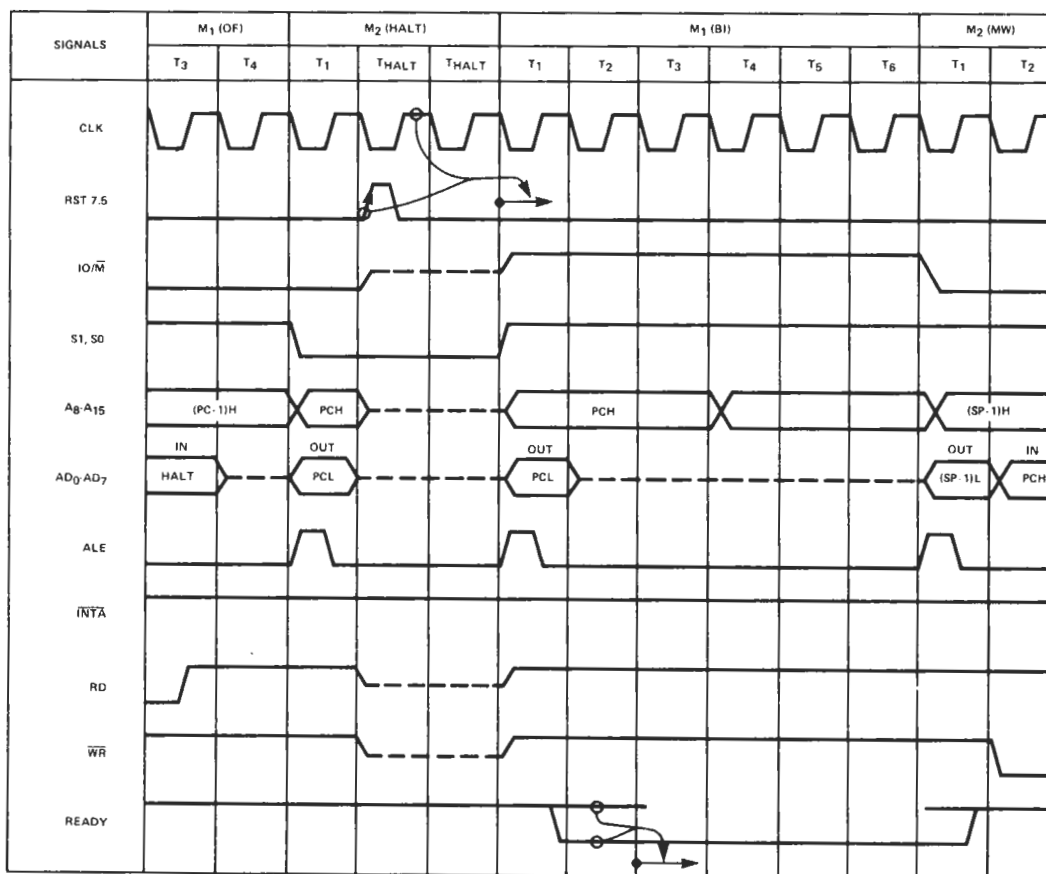


FIGURE 2-20 HALT STATE AND BUS IDLE MACHINE CYCLE  
RST 7.5 TERMINATES  $T_{\text{HALT}}$  STATE

**FUNCTIONAL DESCRIPTION**

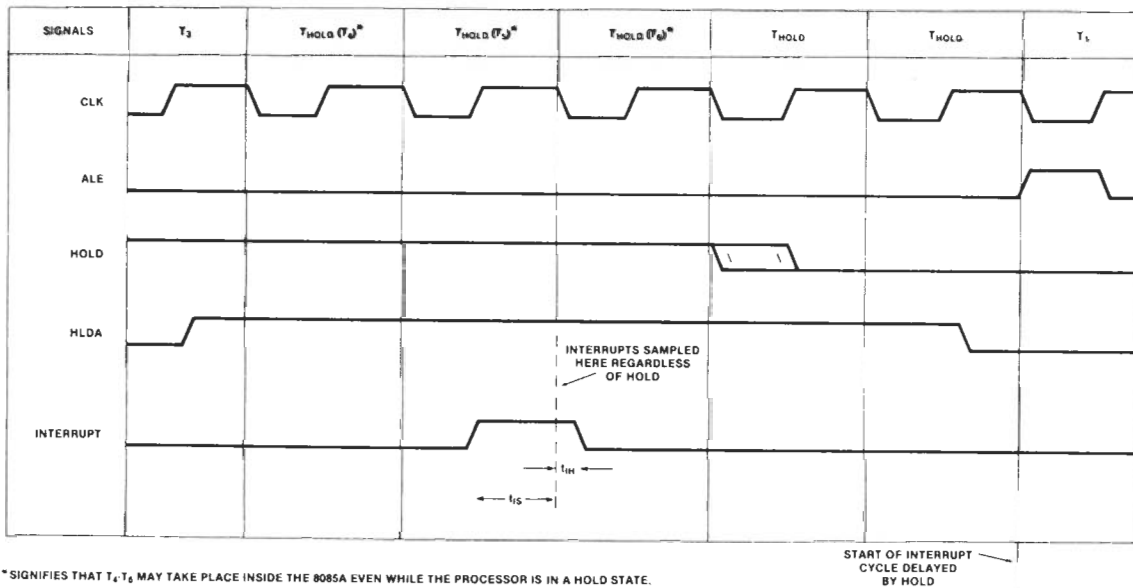
**2.3.6 HOLD and HALT States**

The 8085A uses the  $T_{HOLD}$  state to momentarily cease executing machine cycles, allowing external devices to gain control of the bus and perform DMA cycles. The processor internally latches the state of the HOLD line and the unmasked interrupts during  $CLK = "1"$  of every  $T_{HALT}$  state. If the internal latched HOLD signal is high during  $CLK = "1"$  of any  $T_{HALT}$  state, the CPU will exit  $T_{HALT}$  and enter  $T_{HOLD}$  on the following  $CLK = "1"$ . As shown in Figure 2-21 this will occur even if a valid interrupt occurs simultaneously with the HOLD signal.

The state of the HOLD and the unmasked interrupt lines is latched internally during  $CLK = 1$  of each  $T_{HOLD}$  state as well as during  $T_{HALT}$  states. If the internal latched HOLD signal is low during  $CLK = 1$ , the CPU will exit  $T_{HOLD}$  and enter  $T_{HALT}$  on the following  $CLK = 1$ .

The 8085A accepts the first unmasked, enabled interrupt sampled; thereafter, all interrupt sampling is inhibited. The interrupt thus accepted will inevitably be executed when the CPU exits the HOLD state, even at the expense of holding off higher-priority interrupts (including TRAP). (See Figure 2-22.)

When the CPU is not in  $T_{HALT}$  or  $T_{HOLD}$ , it internally latches the HOLD line only during  $CLK = 1$  of the last state before  $T_3$  ( $T_2$  or  $T_{WAIT}$ ) and during  $CLK = 1$  of the last state before  $T_5$  ( $T_4$  of a six T-state  $M_1$ ). If the internal latched HOLD signal is high during the next  $CLK = 1$ , the CPU will enter  $T_{HOLD}$  after the following clock. When the CPU is not in  $T_{HALT}$  or  $T_{HOLD}$ , it will internally latch the state of the unmasked interrupts only during  $CLK$  of the next to the last state before each  $M_1 \cdot T_1$ .



**FIGURE 2-21 HOLD VS INTERRUPT — NON HALT**



## FUNCTIONAL DESCRIPTION

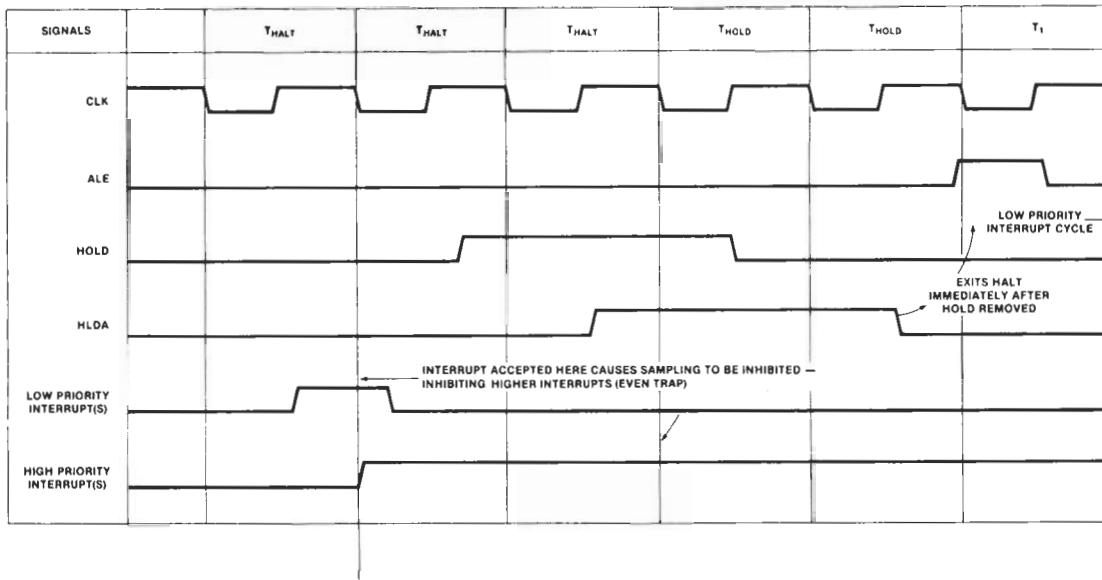


FIGURE 2-22 8085A HOLD VS INTERRUPTS — HALT MODE

2.3.7 Power On and  $\overline{\text{RESET IN}}$ 

The 8085A employs a special internal circuit to increase its speed. This circuit, which is called a substrate bias generator, creates a negative voltage which is used to negatively bias the substrate. The circuit employs an oscillator and a charge pump which require a certain amount of time after POWER ON to stabilize. (See Figure 2-23.)

Taking this circuit into account, the 8085A is not guaranteed to work until 10 ms after  $V_{CC}$  reaches 4.75V. For this reason, it is suggested that  $\overline{\text{RESET IN}}$  be kept low during this period. Note that the 10 ms period does not include the time it takes for the power supply to reach its 4.75V level — which may be milliseconds in some systems. A simple RC network (Figure 3-6) can satisfy this requirement.

The  $\overline{\text{RESET IN}}$  line is latched every  $\text{CLK} = 1$ . This latched signal is recognized by the CPU during  $\text{CLK} = 1$  of the next T state. (See Figure 2-24.) If it is low, the CPU will issue  $\overline{\text{RESET OUT}}$  and enter  $T_{\text{HALT}}$  for the next T state.  $\overline{\text{RESET IN}}$  should be kept low for a minimum of three clock periods to ensure proper synchronization of the CPU. When the  $\overline{\text{RESET IN}}$  signal goes high, the

CPU will enter  $M_1 \cdot T_1$  for the next T state. Note that the various signals and buses are floated in  $T_{\text{RESET}}$  as well as  $T_{\text{HALT}}$  and  $T_{\text{HOLD}}$ . For this reason, it is desirable to provide pull-up resistors for the main control signals (particularly  $\overline{\text{WR}}$ ).

Specifically, the  $\overline{\text{RESET IN}}$  signal causes the following actions:

**RESETS**

PROGRAM COUNTER  
INSTRUCTION REGISTER  
INTE FF  
RST 7.5 FF  
TRAP FF  
SOD FF  
MACHINE STATE FF's  
MACHINE CYCLE FF's  
INTERNALLY LATCHED  
FF's for HOLD, INTR,  
and READY

**SETS**

RST 5.5 MASK  
RST 6.5 MASK  
RST 7.5 MASK

$\overline{\text{RESET IN}}$  does not explicitly change the contents of the 8085A registers (A, B, C, D, E, H, L) and the condition flags, but due to  $\overline{\text{RESET IN}}$  occurring at a random time during instruction execution, the results are indeterminate.

FUNCTIONAL DESCRIPTION

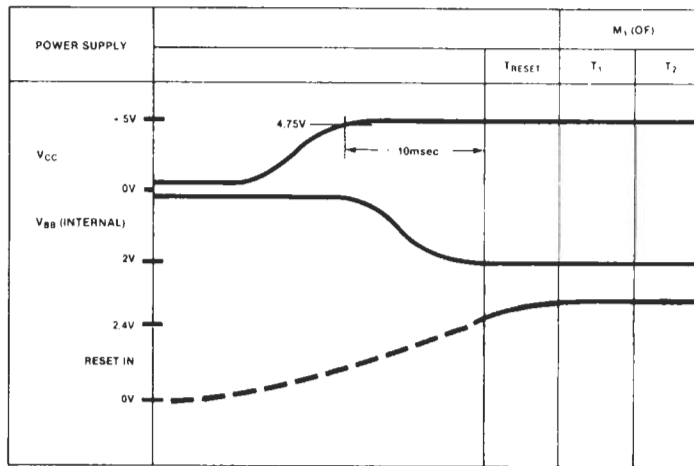


FIGURE 2-23 POWER-ON TIMING

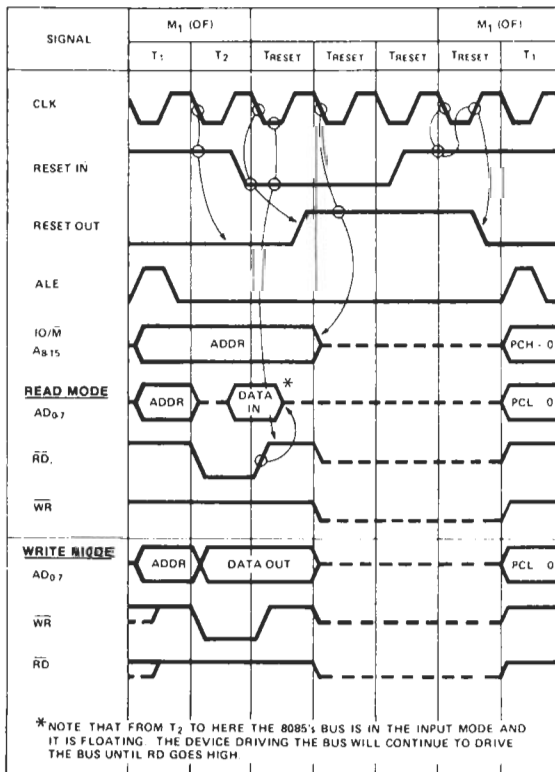


FIGURE 2-24 RESET IN TIMING

Following RESET, the 8085A will start executing instructions at location 0 with the interrupt system disabled, as shown in Figure 2-24.

Figure 2-24 also shows READ and WRITE operations being terminated by a RESET signal. Note that a RESET may prematurely terminate any READ or WRITE operation in process when the RESET occurs.

2.3.8 SID and SOD Signals:

Figure 2-25 shows the timing relationship of the SID and SOD signals to the RIM and SIM instructions. The 8085A has the ability to read the SID line into the accumulator bit 7 using RIM instructions. The state of the SID line is latched internally during T<sub>3</sub> • CLK = 0 of the RIM instruction. Following this, the state of the interrupt pins and masks are also transferred directly to the accumulator.

The 8085A can set the SOD flip-flop from bit 7 of the accumulator using the SIM instruction. (See Figure 2-26.) The data is transferred from the accumulator bit 7 to SOD during M<sub>1</sub> • T<sub>2</sub> • CLK = 0 of the instruction following SIM, assuming that accumulator bit 6 is a 1. Accumulator bit 6 is a "serial output enable" bit.

## FUNCTIONAL DESCRIPTION

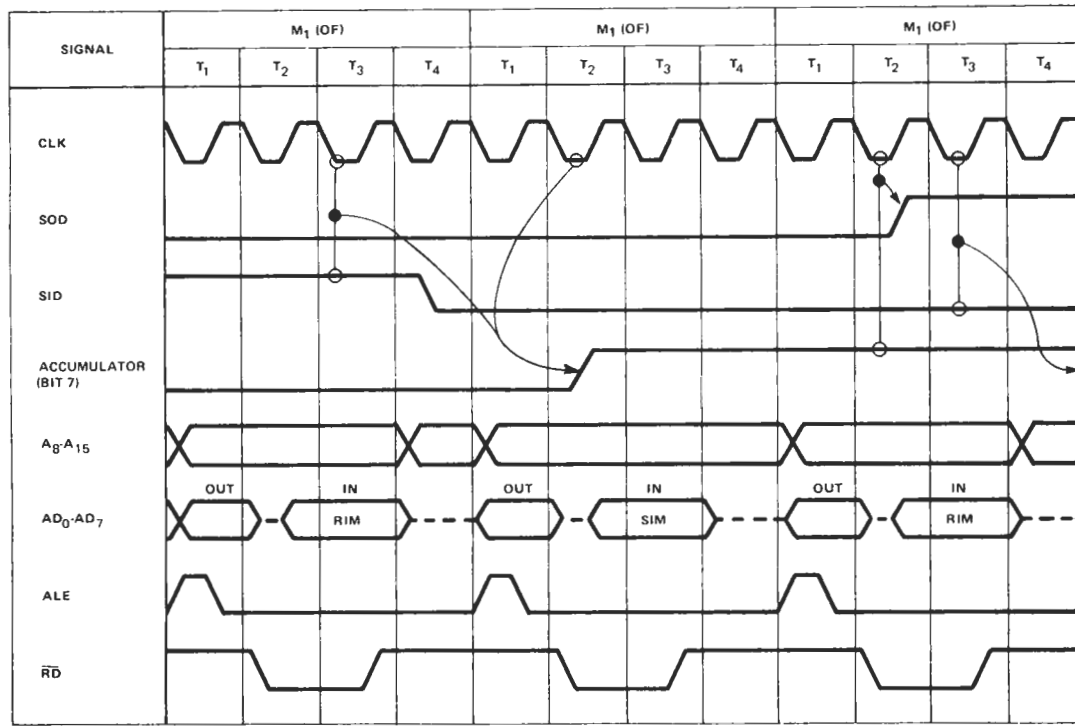
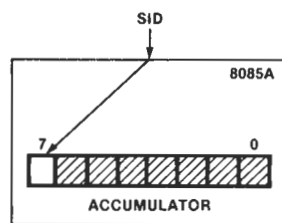


FIGURE 2-25 RELATIONSHIP OF SID AND SOD SIGNALS TO RIM AND SIM INSTRUCTIONS

EFFECT OF RIM INSTRUCTION



EFFECT OF SIM INSTRUCTION

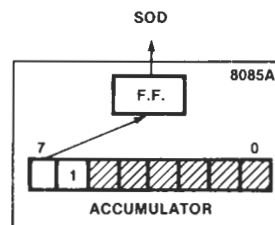


FIGURE 2-26 EFFECT OF RIM AND SIM INSTRUCTIONS

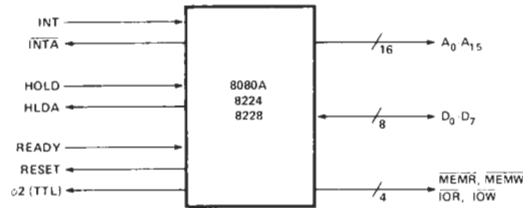
## 2.4 COMPARISON OF MCS-80 AND MCS-85 SYSTEM BUSES

This section compares the MCS-80 bus with the MCS-85 bus. Figure 2-28 details the signals and general timing of the two buses; the timing diagrams are drawn to the same scale (8080A clock cycle = 480 ns and 8085A clock cycle = 320 ns) to facilitate comparison.

**FUNCTIONAL DESCRIPTION**

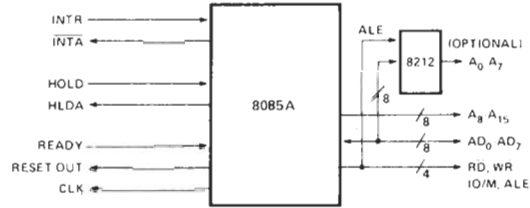
**MCS-80™ System Bus**

The MCS-80 bus is terminated on one end by the CPU-GROUP (consisting of the 8080A, 8224, 8228) and on the other end by the various memory and I/O circuits. The following figure shows the major signals of the MCS-80 bus.



**MCS-85™ System Bus**

The MCS-85 bus is terminated on one end by the 8085A and the other end by various memory and I/O devices. The MCS-85 bus may be optionally de-multiplexed with an 8212 eight bit latch to provide an MCS-80 type bus. The following figure shows the major signals of the MCS-85 bus.



**FIGURE 2-27 COMPARISON OF SYSTEM BUSES**

**MCS-80™ System Bus**

| SIGNAL(S)   | FUNCTION  |
|---|---|
| A <sub>0</sub> -A <sub>15</sub>                                   | The 16 lines of the address bus identify a memory or I/O location for a data transfer operation.  |
| D <sub>0</sub> -D <sub>7</sub>                                    | The 8 lines of the data bus are used for the parallel transfer of data between two devices.   |
| <u>MEMR</u> , <u>MEMW</u> , <u>IOR</u> , <u>IOW</u> , <u>INTA</u> | These five control lines (MEMORY READ, MEMORY WRITE, I/O READ, I/O WRITE, and INTERRUPT ACKNOWLEDGE) identify the type and timing of a data transfer operation. |
| READY, RESET, HOLD, HLDA, φ2 (TTL), INT                           | These signals are used for the synchronization of slow speed memories, system reset, DMA, system timing, and CPU interrupt.                                     |

**MCS-85™ System Bus**

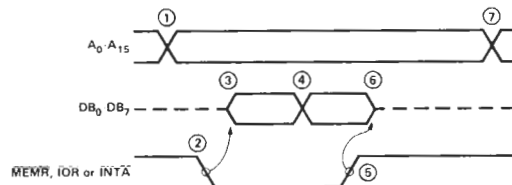
| SIGNAL(S)                               | FUNCTION  |
|---|---|
| A <sub>8</sub> -A <sub>15</sub>         | These are the high order eight bits of the address, and are used to identify a memory or I/O location for a data transfer cycle.  |
| AD <sub>0</sub> -AD <sub>7</sub>        | These eight lines serve a dual function. During the beginning of a data transfer operation, these lines carry the low order eight bits of the address bus. During the remainder of the cycle, these lines are used for the parallel transfer of data between two devices. |
| <u>RD</u> , <u>WR</u> , <u>INTA</u>     | These signals identify the type and timing of a data transfer cycle.  |
| IO/ <u>M</u>                            | The I/O/ <u>MEMORY</u> line identifies a data transfer as being in the I/O address space or the memory address space.   |
| ALE                                     | ADDRESS LATCH ENABLE enables the latching of the A <sub>0</sub> -A <sub>7</sub> signals.  |
| READY, RESET OUT, HOLD, HLDA, CLK, INTR | These signals are used for the synchronization of slow speed memories, system reset, DMA, system timing and CPU interrupt.  |

**FIGURE 2-28 COMPARISON OF SYSTEM BUSES**

## FUNCTIONAL DESCRIPTION

### MCS-80™ System Bus for READ CYCLE

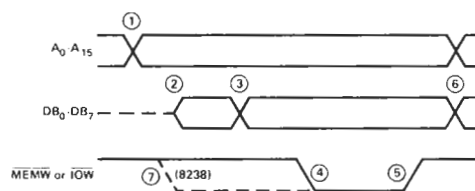
The basic timing of the MCS-80 BUS for a READ CYCLE is as follows:



The MCS-80 first presents the address ① and shortly thereafter the control signal ②. The data bus, which was in the high impedance state, is driven by the selected device ③. The selected device eventually presents the valid data to the processor ④. The processor raises the control signal ⑤, which causes the selected device to put the data bus in the high impedance state ⑥. The processor then changes the address ⑦ for the start of the next data transfer.

### MCS-80™ System Bus for WRITE CYCLE

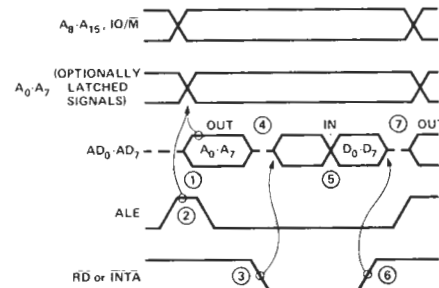
The basic timing of the MCS-80 BUS for a WRITE CYCLE is as follows:



The MCS-80 first presents the address ①, then enables the data bus driver ②, and later presents the data ③. Shortly thereafter, the MCS-80 drops the control signal ④ for an interval of time and then raises the signal ⑤. The MCS-80 then changes the address ⑥ in preparation for the next data transfer. The advance write signal of the 8238 is also shown ⑦.

### MCS-85™ System Bus for READ CYCLE

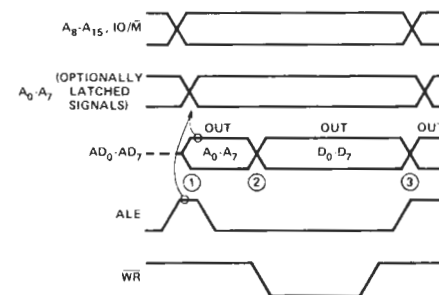
The basic timing of the MCS-85 BUS for a READ CYCLE is as follows:



At the beginning of the READ cycle, the 8085A sends out all 16 bits of address ①. This is followed by ALE ② which causes the lower eight bits of address to be latched in either the 8155/56, 8355, 8755A, or in an external 8212.  $\overline{RD}$  is then dropped ③ by the 8085A. The data bus is then tri-stated by the 8085A in preparation for the selected device driving the bus ④; the selected device will continue to drive the bus with valid data ⑤, until  $\overline{RD}$  is raised ⑥ by the 8085A. At the end of the READ CYCLE ⑦, the address and data lines are changed in preparation for the next cycle.

### MCS-85™ System Bus for WRITE CYCLE

The basic timing of the MCS-85 BUS for a WRITE CYCLE is as follows:



The timing of the WRITE CYCLE is identical to the MCS-85 READ CYCLE with the exception of the  $AD_0-AD_7$  lines. At the beginning of the cycle ①, the low order eight bits of address are on  $AD_0-AD_7$ . After ALE drops, the eight bits of data ② are put on  $AD_0-AD_7$ . They are removed ③ at the end of the WRITE CYCLE, in anticipation of the next data transfer.

**FIGURE 2-28 (Continued) COMPARISON OF SYSTEM BUSES**

## FUNCTIONAL DESCRIPTION

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The following observations of the two buses can be made:

1. The access times from address leaving the processor to returning data are almost identical, even though the 8085A is operating 50% faster than the 8080.
2. With the addition of an 8212 latch to the 8085A, the basic timings of the two systems are very similar.
3. The 8085A has more time for address setup to  $\overline{RD}$  than the 8080.
4. The MCS-80 has a wider  $\overline{RD}$  signal, but a narrower  $\overline{WR}$  signal than the 8085A.
5. The MCS-80 provides stable data setup to the leading and trailing edges of  $\overline{WR}$ , while the 8085 provides stable data setup to only the trailing edge of  $\overline{WR}$ .
6. The MCS-80 control signals have different widths and occur at different points in the machine cycle, while the 8085A control signals have identical timing.
7. While not shown on the chart, the MCS-80 data and address hold times are adversely affected by the processor preparing to enter the HOLD state. The 8085A has identical timing regardless of entering HOLD.
8. Also not shown on the chart is the fact that all output signals of the 8085A have  $-400\mu\text{a}$  of source current and 2.0 ma of sink current. The 8085A also has input voltage levels of  $V_{IL} = 0.8\text{V}$  and  $V_{IH} = 2.0\text{V}$ .

### CONCLUSION:

The preceding discussion has clearly shown that the MCS-85 bus satisfies the two restrictions of COMPATIBILITY and SPEED. It is compatible because it requires only an 8212 latch to generate an MCS-80 type bus. If the four control signals  $\overline{MEMR}$ ,  $\overline{MEMW}$ ,  $\overline{IOR}$  and  $\overline{IOW}$  are desired, they can be generated from  $\overline{RD}$ ,  $\overline{WR}$ ,

and  $\overline{IO/\overline{M}}$  with a decoder or a few gates. The MCS-85 bus is also fast. While running at 3MHz, the 8085A generates better timing signals than the MCS-80 does at 2MHz. Furthermore, the multiplexed bus structure doesn't slow the 8085A down, because it is using the internal states to overlap the fetch and execution portions of different machine cycles. Finally, the MCS-85 can be slowed down or sped up considerably, while still providing reasonable timing.

TO USE. The  $\overline{RD}$ ,  $\overline{WR}$ , and  $\overline{INTA}$  control signals all have identical timing, which isn't affected by the CPU preparing to enter the HOLD state. Furthermore, the address and data bus have good setup and hold times relative to the control signals. The voltage and current levels for the interface signals will all drive buses of up to 40 MOS devices, or 1 schottky TTL device.

The MCS-85 system bus is also EFFICIENT. Efficiency is the reason that the lower eight address lines are multiplexed with the data bus. Every chip that needs to use both  $A_0-A_7$  and  $D_0-D_7$  saves 7 pins (the eighth pin is used for ALE) on the interface to the processor. That means that 7 more pins per part are available to either add features to the part or to use a smaller package in some cases. In the three chip system shown in Figure 3-6, the use of the MCS-85 bus saves  $3 \times 7 = 21$  pins, which are used for extra I/O and interrupt lines. A further advantage of the MCS-85 bus is apparent in Figure 3-7, which shows a printed circuit layout of the circuit in Figure 3-6. The reduced number of pins and the fact that compatible pinouts were used, provides for an extremely compact, simple, and efficient printed circuit. Notice that great care was taken when the pinouts were assigned to ensure that the signals would flow easily from chip to chip to chip.

## APPENDIX C

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### **8085 Instruction Set**

The following pages are reprinted with  
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## 8085A INSTRUCTION SET

### 5.1 WHAT THE INSTRUCTION SET IS

A computer, no matter how sophisticated, can do only what it is instructed to do. A program is a sequence of instructions, each of which is recognized by the computer and causes it to perform an operation. Once a program is placed in memory space that is accessible to your CPU, you may run that same sequence of instructions as often as you wish to solve the same problem or to do the same function. The set of instructions to which the 8085A CPU will respond is permanently fixed in the design of the chip.

Each computer instruction allows you to initiate the performance of a specific operation. The 8085A implements a group of instructions that move data between registers, between a register and memory, and between a register and an I/O port. It also has arithmetic and logic instructions, conditional and unconditional branch instructions, and machine control instructions. The CPU recognizes these instructions only when they are coded in binary form.

### 5.2 SYMBOLS AND ABBREVIATIONS:

The following symbols and abbreviations are used in the subsequent description of the 8085A instructions:

| SYMBOLS     | MEANING                             |
|-------------|-------------------------------------|
| accumulator | Register A                          |
| addr        | 16-bit address quantity             |
| data        | 8-bit quantity                      |
| data 16     | 16-bit data quantity                |
| byte 2      | The second byte of the instruction  |
| byte 3      | The third byte of the instruction   |
| port        | 8-bit address of an I/O device      |
| r,r1,r2     | One of the registers A,B,C, D,E,H,L |

DDD,SSS

The bit pattern designating one of the registers A,B,C,D, E,H,L (DDD= destination, SSS= source):

| DDD or SSS | REGISTER NAME |
|------------|---------------|
| 111        | A             |
| 000        | B             |
| 001        | C             |
| 010        | D             |
| 011        | E             |
| 100        | H             |
| 101        | L             |

rp

One of the register pairs:

B represents the B,C pair with B as the high-order register and C as the low-order register;

D represents the D,E pair with D as the high-order register and E as the low-order register;

H represents the H,L pair with H as the high-order register and L as the low-order register;

SP represents the 16-bit stack pointer register.

RP

The bit pattern designating one of the register pairs B,D,H,SP:

| RP | REGISTER PAIR |
|----|---------------|
| 00 | B-C           |
| 01 | D-E           |
| 10 | H-L           |
| 11 | SP            |

rh

The first (high-order) register of a designated register pair.

rl

The second (low-order) register of a designated register pair.



## THE INSTRUCTION SET

|                |  |
|----------------|--|
| PC             | 16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively). |
| SP             | 16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively).   |
| r <sub>m</sub> | Bit m of the register r (bits are number 7 through 0 from left to right).  |
| LABEL          | 16-bit address of subroutine.  |
|                | The condition flags:   |
| Z              | Zero   |
| S              | Sign   |
| P              | Parity   |
| CY             | Carry  |
| AC             | Auxiliary Carry  |
| ( )            | The contents of the memory location or registers enclosed in the parentheses.  |
| —              | "Is transferred to"  |
| ∧              | Logical AND  |
| ⊕              | Exclusive OR   |
| ∨              | Inclusive OR   |
| +              | Addition   |
| −              | Two's complement subtraction   |
| *              | Multiplication   |
| —              | "Is exchanged with"  |
| —              | The one's complement (e.g., $\overline{(A)}$ )   |
| n              | The restart number 0 through 7   |
| NNN            | The binary representation 000 through 111 for restart number 0 through 7 respectively.                               |

The instruction set encyclopedia is a detailed description of the 8085A instruction set. Each instruction is described in the following manner:

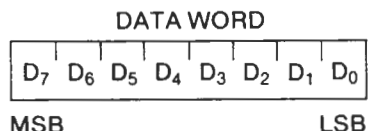
1. The MCS-85 macro assembler format, consisting of the instruction mnemonic and operand fields, is printed in **BOLDFACE** on the first line.
2. The name of the instruction is enclosed in parentheses following the mnemonic.
3. The next lines contain a symbolic description of what the instruction does.
4. This is followed by a narrative description of the operation of the instruction.

5. The boxes describe the binary codes that comprise the machine instruction.
6. The last four lines contain information about the execution of the instruction. The number of machine cycles and states required to execute the instruction are listed first. If the instruction has two possible execution times, as in a conditional jump, both times are listed, separated by a slash. Next, data addressing modes are listed if applicable. The last line lists any of the five flags that are affected by the execution of the instruction.

## 5.3 INSTRUCTION AND DATA FORMATS

Memory used in the MCS-85 system is organized in 8-bit bytes. Each byte has a unique location in physical memory. That location is described by one of a sequence of 16-bit binary addresses. The 8085A can address up to 64K ( $K = 1024$ , or  $2^{10}$ ; hence, 64K represents the decimal number 65,536) bytes of memory, which may consist of both random-access, read-write memory (RAM) and read-only memory (ROM), which is also random-access.

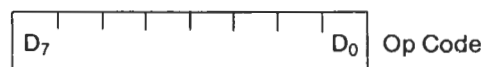
Data in the 8085A is stored in the form of 8-bit binary integers:



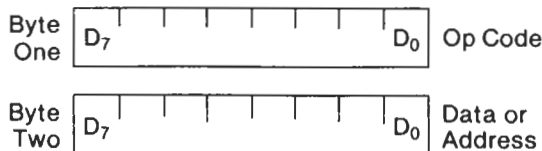
When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the Intel 8085A, BIT 0 is referred to as the **Least Significant Bit (LSB)**, and BIT 7 (of an 8-bit number) is referred to as the **Most Significant Bit (MSB)**.

An 8085A program instruction may be one, two or three bytes in length. Multiple-byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instruction. The exact instruction format will depend on the particular operation to be executed.

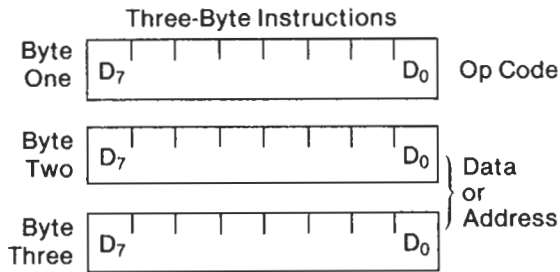
## Single Byte Instructions



## Two-Byte Instructions



## THE INSTRUCTION SET



### 5.4 ADDRESSING MODES:

Often the data that is to be operated on is stored in memory. When multi-byte numeric data is used, the data, like instructions, is stored in successive memory locations, with the least significant byte first, followed by increasingly significant bytes. The 8085A has four different modes for addressing data stored in memory or in registers:

- **Direct** — Bytes 2 and 3 of the instruction contain the exact memory address of the data item (the low-order bits of the address are in byte 2, the high-order bits in byte 3).
- **Register** — The instruction specifies the register or register pair in which the data is located.
- **Register Indirect** — The instruction specifies a register pair which contains the memory address where the data is located (the high-order bits of the address are in the first register of the pair the low-order bits in the second).
- **Immediate** — The instruction contains the data itself. This is either an 8-bit quantity or a 16-bit quantity (least significant byte first, most significant byte second).

Unless directed by an interrupt or branch institution, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the address of the next instruction to be executed in one of two ways:

- **Direct** — The branch instruction contains the address of the next instruction to be executed. (Except for the 'RST' instruction, byte 2 contains the low-order address and byte 3 the high-order address.)

- **Register Indirect** — The branch instruction indicates a register-pair which contains the address of the next instruction to be executed. (The high-order bits of the address are in the first register of the pair, the low-order bits in the second.)

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences). RST includes a three-bit field; program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

### 5.5 CONDITION FLAGS:

There are five condition flags associated with the execution of instructions on the 8085A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry. Each is represented by a 1-bit register (or flip-flop) in the CPU. A flag is set by forcing the bit to 1; it is reset by forcing the bit to 0.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

- Zero:** If the result of an instruction has the value 0, this flag is set; otherwise it is reset.
- Sign:** If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise it is reset.
- Parity:** If the modulo 2 sum of the bits of the result of the operation is 0, (i.e., if the result has even parity), this flag is set; otherwise it is reset (i.e., if the result has odd parity).
- Carry:** If the instruction resulted in a carry (from addition), or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise it is reset.

**Auxiliary Carry:** If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

## THE INSTRUCTION SET

## 5.6 INSTRUCTION SET ENCYCLOPEDIA

In the ensuing dozen pages, the complete 8085A instruction set is described, grouped in order under five different functional headings, as follows:

1. **Data Transfer Group** — Moves data between registers or between memory locations and registers. Includes moves, loads, stores, and exchanges. (See below.)
2. **Arithmetic Group** — Adds, subtracts, increments, or decrements data in registers or memory. (See page 5-13.)
3. **Logic Group** — ANDs, ORs, XORs, compares, rotates, or complements data in registers or between memory and a register. (See page 5-16.)
4. **Branch Group** — Initiates conditional or unconditional jumps, calls, returns, and restarts. (See page 5-20.)
5. **Stack, I/O, and Machine Control Group** — Includes instructions for maintaining the stack, reading from input ports, writing to output ports, setting and reading interrupt masks, and setting and clearing flags. (See page 5-22.)

The formats described in the encyclopedia reflect the assembly language processed by Intel-supplied assembler, used with the Intellec® development systems.

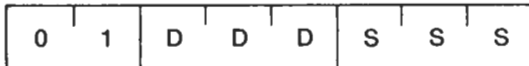
## 5.6.1 Data Transfer Group

This group of instructions transfers data to and from registers and memory. **Condition flags are not affected by any instruction in this group.**

**MOV r1, r2** (Move Register)

(r1) — (r2)

The content of register r2 is moved to register r1.

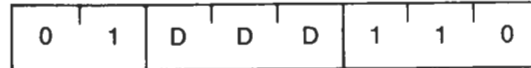


Cycles: 1  
 States: 4 (8085), 5 (8080)  
 Addressing: register  
 Flags: none

**MOV r, M** (Move from memory)

(r) — ((H) (L))

The content of the memory location, whose address is in registers H and L, is moved to register r.

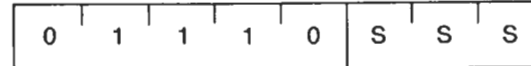


Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: none

**MOV M, r** (Move to memory)

((H) (L)) — (r)

The content of register r is moved to the memory location whose address is in registers H and L.

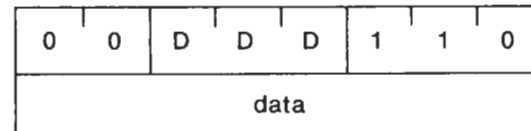


Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: none

**MVI r, data** (Move Immediate)

(r) — (byte 2)

The content of byte 2 of the instruction is moved to register r.

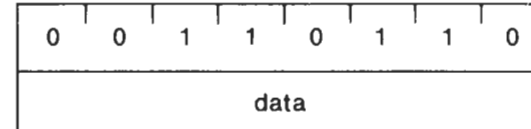


Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: none

**MVI M, data** (Move to memory immediate)

((H) (L)) — (byte 2)

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.



Cycles: 3  
 States: 10  
 Addressing: immed./reg. indirect  
 Flags: none

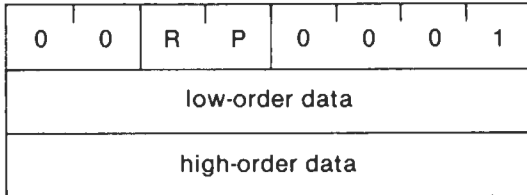
## THE INSTRUCTION SET

**LXI rp, data 16** (Load register pair immediate)

(rh) ← (byte 3),

(rl) ← (byte 2)

Byte 3 of the instruction is moved into the high-order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (rl) of the register pair rp.

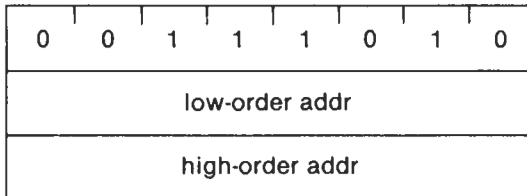


Cycles: 3  
 States: 10  
 Addressing: immediate  
 Flags: none

**LDA addr** (Load Accumulator direct)

(A) ← ((byte 3)(byte 2))

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.

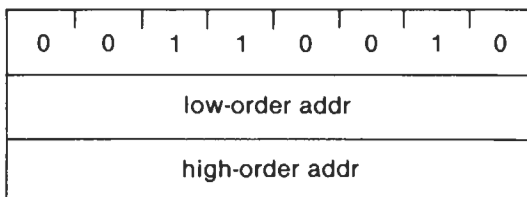


Cycles: 4  
 States: 13  
 Addressing: direct  
 Flags: none

**STA addr** (Store Accumulator direct)

((byte 3)(byte 2)) ← (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.



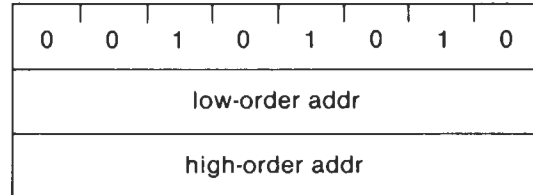
Cycles: 4  
 States: 13  
 Addressing: direct  
 Flags: none

**LHLD addr** (Load H and L direct)

(L) ← ((byte 3)(byte 2))

(H) ← ((byte 3)(byte 2) + 1)

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.



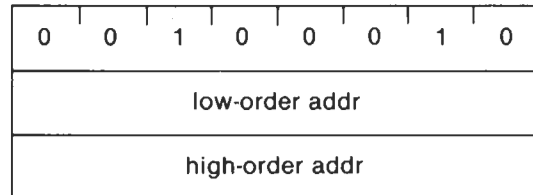
Cycles: 5  
 States: 16  
 Addressing: direct  
 Flags: none

**SHLD addr** (Store H and L direct)

((byte 3)(byte 2)) ← (L)

((byte 3)(byte 2) + 1) ← (H)

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

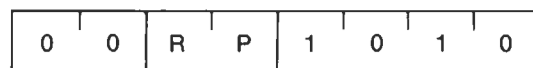


Cycles: 5  
 States: 16  
 Addressing: direct  
 Flags: none

**LDAX rp** (Load accumulator indirect)

(A) ← ((rp))

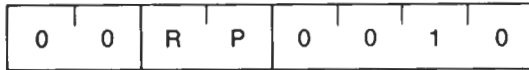
The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: only register pairs rp=B (registers B and C) or rp=D (registers D and E) may be specified.



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: none

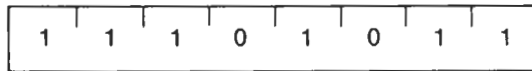
## THE INSTRUCTION SET

**STAX rp** (Store accumulator indirect)  
 $((rp)) - (A)$   
 The content of register A is moved to the memory location whose address is in the register pair rp. Note: only register pairs  $rp=B$  (registers B and C) or  $rp=D$  (registers D and E) may be specified.



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: none

**XCHG** (Exchange H and L with D and E)  
 $(H) \leftrightarrow (D)$   
 $(L) \leftrightarrow (E)$   
 The contents of registers H and L are exchanged with the contents of registers D and E.



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: none

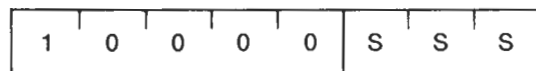
## 5.6.2 Arithmetic Group

This group of instructions performs arithmetic operations on data in registers and memory.

**Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.**

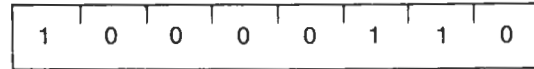
All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

**ADD r** (Add Register)  
 $(A) - (A) + (r)$   
 The content of register r is added to the content of the accumulator. The result is placed in the accumulator.



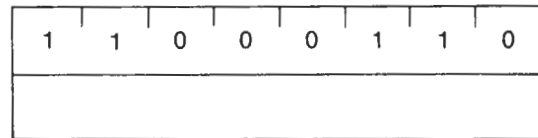
Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

**ADD M** (Add memory)  
 $(A) - (A) + ((H) (L))$   
 The content of the memory location whose address is contained in the H and L registers is added to the content of the accumulator. The result is placed in the accumulator.



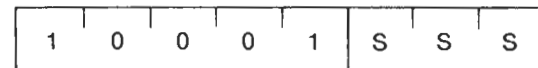
Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**ADI data** (Add immediate)  
 $(A) - (A) + (\text{byte } 2)$   
 The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

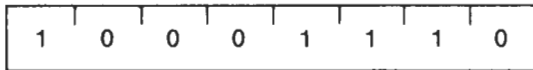
**ADC r** (Add Register with carry)  
 $(A) - (A) + (r) + (CY)$   
 The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

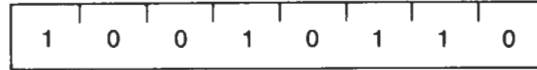
THE INSTRUCTION SET

**ADC M** (Add memory with carry)  
 $(A) \leftarrow (A) + ((H) (L)) + (CY)$   
 The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**SUB M** (Subtract memory)  
 $(A) \leftarrow (A) - ((H) (L))$   
 The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**ACI data** (Add immediate with carry)  
 $(A) \leftarrow (A) + (\text{byte 2}) + (CY)$   
 The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.



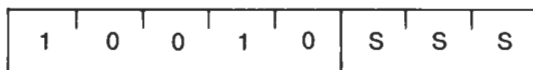
Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**SUI data** (Subtract immediate)  
 $(A) \leftarrow (A) - (\text{byte 2})$   
 The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.



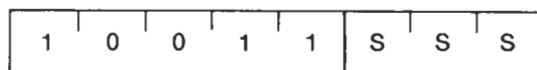
Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**SUB r** (Subtract Register)  
 $(A) \leftarrow (A) - (r)$   
 The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

**SBB r** (Subtract Register with borrow)  
 $(A) \leftarrow (A) - (r) - (CY)$   
 The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



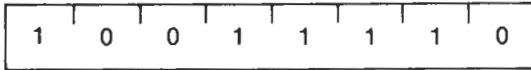
Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

## THE INSTRUCTION SET

**SBB M** (Subtract memory with borrow)

$$(A) - (A) - ((H) (L)) - (CY)$$

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

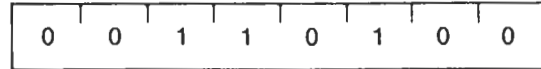


Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**INR M** (Increment memory)

$$((H) (L)) - ((H) (L)) + 1$$

The content of the memory location whose address is contained in the H and L registers is incremented by one. Note: All condition flags **except CY** are affected.



Cycles: 3  
 States: 10  
 Addressing: reg. indirect  
 Flags: Z,S,P,AC

**SBI data** (Subtract immediate with borrow)

$$(A) - (A) - (\text{byte 2}) - (CY)$$

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

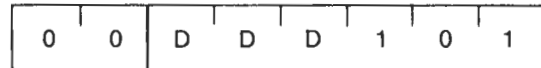


Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**DCR r** (Decrement Register)

$$(r) - (r) - 1$$

The content of register *r* is decremented by one. Note: All condition flags **except CY** are affected.

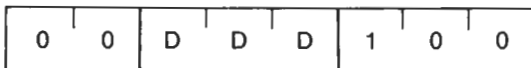


Cycles: 1  
 States: 4 (8085), 5 (8080)  
 Addressing: register  
 Flags: Z,S,P,AC

**INR r** (Increment Register)

$$(r) - (r) + 1$$

The content of register *r* is incremented by one. Note: All condition flags **except CY** are affected.

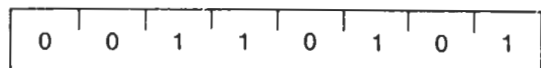


Cycles: 1  
 States: 4 (8085), 5 (8080)  
 Addressing: register  
 Flags: Z,S,P,AC

**DCR M** (Decrement memory)

$$((H) (L)) - ((H) (L)) - 1$$

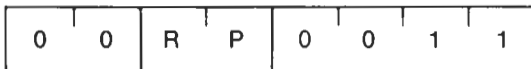
The content of the memory location whose address is contained in the H and L registers is decremented by one. Note: All condition flags **except CY** are affected.



Cycles: 3  
 States: 10  
 Addressing: reg. indirect  
 Flags: Z,S,P,AC

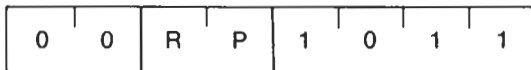
## THE INSTRUCTION SET

**INX rp** (Increment register pair)  
 $(rh)(rl) \rightarrow (rh)(rl) + 1$   
 The content of the register pair *rp* is incremented by one. Note: **No condition flags are affected.**



Cycles: 1  
 States: 6 (8085), 5 (8080)  
 Addressing: register  
 Flags: none

**DCX rp** (Decrement register pair)  
 $(rh)(rl) \rightarrow (rh)(rl) - 1$   
 The content of the register pair *rp* is decremented by one. Note: **No condition flags are affected.**



Cycles: 1  
 States: 6 (8085), 5 (8080)  
 Addressing: register  
 Flags: none

**DAD rp** (Add register pair to H and L)  
 $(H)(L) \rightarrow (H)(L) + (rh)(rl)$   
 The content of the register pair *rp* is added to the content of the register pair H and L. The result is placed in the register pair H and L. Note: **Only the CY flag is affected.** It is set if there is a carry out of the double precision add; otherwise it is reset.

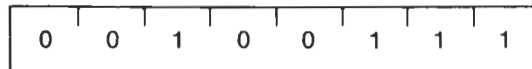


Cycles: 3  
 States: 10  
 Addressing: register  
 Flags: CY

**DAA** (Decimal Adjust Accumulator)  
 The eight-bit number in the accumulator is adjusted to form two four-bit Binary-Coded-Decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.
2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

NOTE: All flags are affected.



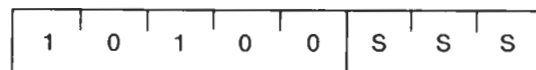
Cycles: 1  
 States: 4  
 Flags: Z,S,P,CY,AC

## 5.6.3 Logical Group

This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

**ANA r** (AND Register)  
 $(A) \rightarrow (A) \wedge (r)$   
 The content of register *r* is logically ANDed with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared and AC is set (8085). The CY flag is cleared and AC is set to the OR'ing of bits 3 of the operands (8080).**



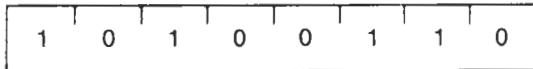
Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC



## THE INSTRUCTION SET

**ANA M** (AND memory) $(A) \leftarrow (A) \wedge ((H) (L))$ 

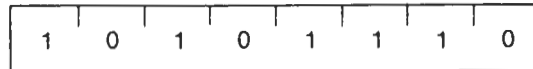
The contents of the memory location whose address is contained in the H and L registers is logically ANDed with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared and AC is set (8085). The CY flag is cleared and AC is set to the OR'ing of bits 3 of the operands (8080).**



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**XRA M** (Exclusive OR Memory) $(A) \leftarrow (A) \vee ((H) (L))$ 

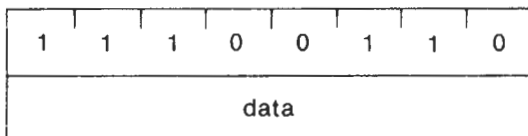
The content of the memory location whose address is contained in the H and L registers is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**ANI data** (AND immediate) $(A) \leftarrow (A) \wedge (\text{byte 2})$ 

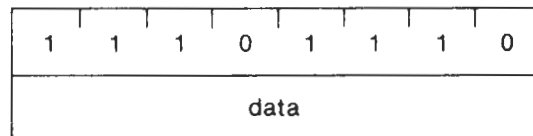
The content of the second byte of the instruction is logically ANDed with the contents of the accumulator. The result is placed in the accumulator. **The CY flag is cleared and AC is set (8085). The CY flag is cleared and AC is set to the OR'ing of bits 3 of the operands (8080).**



Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**XRI data** (Exclusive OR immediate) $(A) \leftarrow (A) \vee (\text{byte 2})$ 

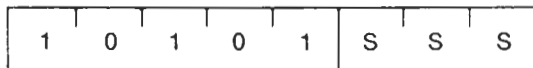
The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**XRA r** (Exclusive OR Register) $(A) \leftarrow (A) \vee (r)$ 

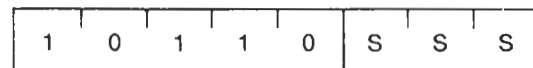
The content of register r is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

**ORA r** (OR Register) $(A) \leftarrow (A) \vee (r)$ 

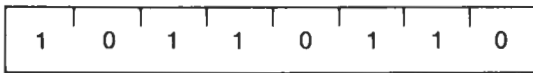
The content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

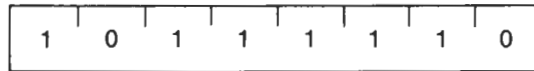
THE INSTRUCTION SET

**ORA M** (OR memory)  
 (A) ← (A) V ((H) (L))  
 The content of the memory location whose address is contained in the H and L registers is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



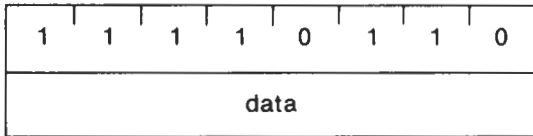
Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**CMP M** (Compare memory)  
 (A) ← ((H) (L))  
 The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. **The Z flag is set to 1 if (A) = ((H) (L)). The CY flag is set to 1 if (A) < ((H) (L)).**



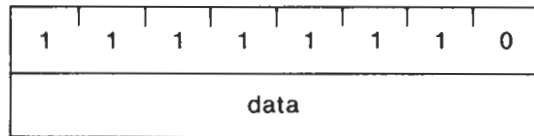
Cycles: 2  
 States: 7  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**ORI data** (OR Immediate)  
 (A) ← (A) V (byte 2)  
 The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



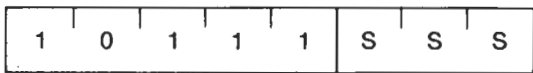
Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**CPI data** (Compare immediate)  
 (A) ← (byte 2)  
 The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. **The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) < (byte 2).**



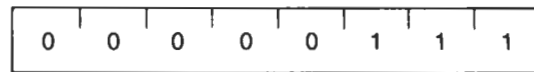
Cycles: 2  
 States: 7  
 Addressing: immediate  
 Flags: Z,S,P,CY,AC

**CMP r** (Compare Register)  
 (A) ← (r)  
 The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. **The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).**



Cycles: 1  
 States: 4  
 Addressing: register  
 Flags: Z,S,P,CY,AC

**RLC** (Rotate left)  
 (A<sub>n+1</sub>) ← (A<sub>n</sub>) ; (A<sub>0</sub>) ← (A<sub>7</sub>)  
 (CY) ← (A<sub>7</sub>)  
 The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. **Only the CY flag is affected.**

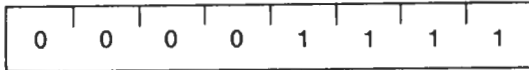


Cycles: 1  
 States: 4  
 Flags: CY

## THE INSTRUCTION SET

**RRC** (Rotate right)
 $(A_n) - (A_{n+1}); (A_7) - (A_0)$   
 $(CY) - (A_0)$ 

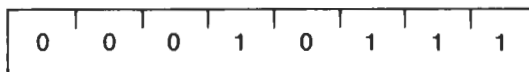
The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. **Only the CY flag is affected.**



Cycles: 1  
 States: 4  
 Flags: CY

**RAL** (Rotate left through carry)
 $(A_{n+1}) - (A_n); (CY) - (A_7)$   
 $(A_0) - (CY)$ 

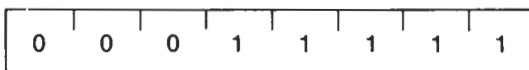
The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. **Only the CY flag is affected.**



Cycles: 1  
 States: 4  
 Flags: CY

**RAR** (Rotate right through carry)
 $(A_n) - (A_{n+1}); (CY) - (A_0)$   
 $(A_7) - (CY)$ 

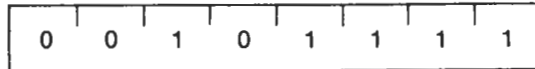
The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. **Only the CY flag is affected.**



Cycles: 1  
 States: 4  
 Flags: CY

**CMA** (Complement accumulator)
 $(A) - (\bar{A})$ 

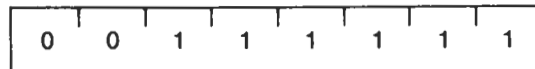
The contents of the accumulator are complemented (zero bits become 1, one bits become 0). **No flags are affected.**



Cycles: 1  
 States: 4  
 Flags: none

**CMC** (Complement carry)
 $(CY) - (\bar{CY})$ 

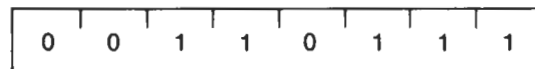
The CY flag is complemented. **No other flags are affected.**



Cycles: 1  
 States: 4  
 Flags: CY

**STC** (Set carry)
 $(CY) - 1$ 

The CY flag is set to 1. **No other flags are affected.**



Cycles: 1  
 States: 4  
 Flags: CY

THE INSTRUCTION SET

5.6.4 Branch Group

This group of instructions alter normal sequential program flow.

**Condition flags are not affected** by any instruction in this group.

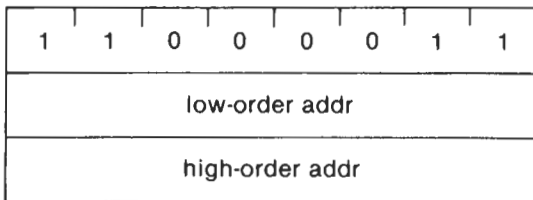
The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows:

| CONDITION                | CCC |
|--------------------------|-----|
| NZ — not zero (Z = 0)    | 000 |
| Z — zero (Z = 1)         | 001 |
| NC — no carry (CY = 0)   | 010 |
| C — carry (CY = 1)       | 011 |
| PO — parity odd (P = 0)  | 100 |
| PE — parity even (P = 1) | 101 |
| P — plus (S = 0)         | 110 |
| M — minus (S = 1)        | 111 |

**JMP addr** (Jump)

(PC) — (byte 3) (byte 2)

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



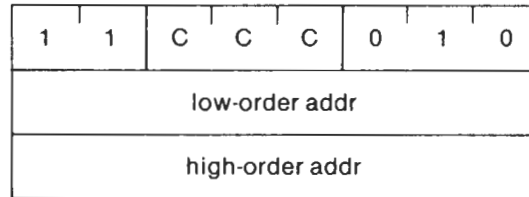
Cycles: 3  
 States: 10  
 Addressing: immediate  
 Flags: none

**Jcondition addr** (Conditional jump)

If (CCC),

(PC) — (byte 3) (byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise, control continues sequentially.



Cycles: 2/3 (8085), 3 (8080)  
 States: 7/10 (8085), 10 (8080)  
 Addressing: immediate  
 Flags: none

**CALL addr** (Call)

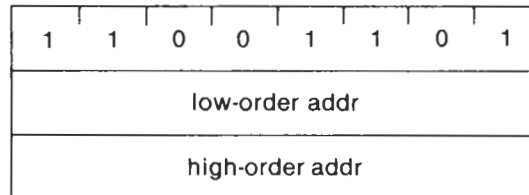
((SP) - 1) - (PCH)

((SP) - 2) - (PCL)

(SP) — (SP) - 2

(PC) — (byte 3) (byte 2)

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

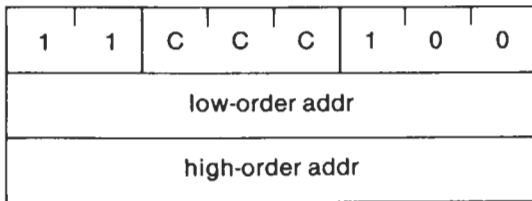


Cycles: 5  
 States: 18 (8085), 17 (8080)  
 Addressing: immediate/  
 reg. indirect  
 Flags: none

## THE INSTRUCTION SET

**Ccondition addr** (Condition call)**If** (CCC), $((SP) - 1) - (PCH)$  $((SP) - 2) - (PCL)$  $(SP) - (SP) - 2$  $(PC) - (\text{byte } 3) (\text{byte } 2)$ 

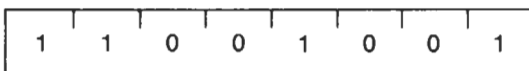
If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.



Cycles: 2/5 (8085), 3/5 (8080)  
 States: 9/18 (8085), 11/17 (8080)  
 Addressing: immediate/  
 reg. indirect  
 Flags: none

**RET** (Return) $(PCL) - ((SP));$  $(PCH) - ((SP) + 1);$  $(SP) - (SP) + 2;$ 

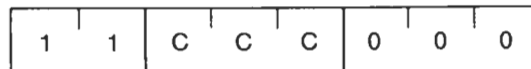
The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.



Cycles: 3  
 States: 10  
 Addressing: reg. indirect  
 Flags: none

**Rcondition** (Conditional return)**If** (CCC), $(PCL) - ((SP))$  $(PCH) - ((SP) + 1)$  $(SP) - (SP) + 2$ 

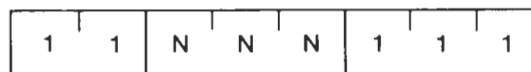
If the specified condition is true, the actions specified in the RET instruction (see above) are performed; otherwise, control continues sequentially.



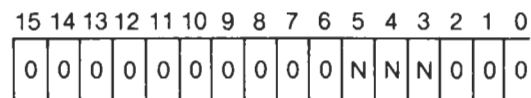
Cycles: 1/3  
 States: 6/12 (8085), 5/11 (8080)  
 Addressing: reg. indirect  
 Flags: none

**RST n** (Restart) $((SP) - 1) - (PCH)$  $((SP) - 2) - (PCL)$  $(SP) - (SP) - 2$  $(PC) - 8 * (NNN)$ 

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.



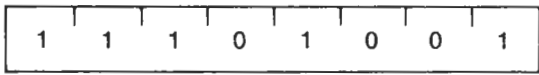
Cycles: 3  
 States: 12 (8085), 11 (8080)  
 Addressing: reg. indirect  
 Flags: none



Program Counter After Restart

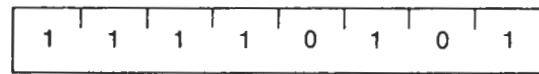
THE INSTRUCTION SET

**PCHL** (Jump H and L indirect — move H and L to PC)  
 (PCH) — (H)  
 (PCL) — (L)  
 The content of register H is moved to the high-order eight bits of register PC. The content of register L is moved to the low-order eight bits of register PC.



Cycles: 1  
 States: 6 (8085), 5 (8080)  
 Addressing: register  
 Flags: none

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.



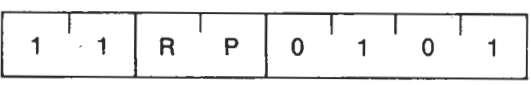
Cycles: 3  
 States: 12 (8085), 11 (8080)  
 Addressing: reg. indirect  
 Flags: none

**5.6.5 Stack, I/O, and Machine Control Group**  
 This group of instructions performs I/O, manipulates the Stack, and alters internal control flags.

Unless otherwise specified, **condition flags are not affected by any instructions in this group.**

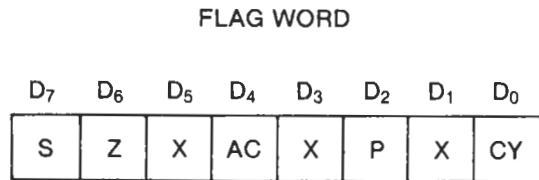
**PUSH rp** (Push)  
 ((SP) — 1) — (rh)  
 ((SP) — 2) — (rl)  
 ((SP) — (SP) — 2

The content of the high-order register of register pair *rp* is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair *rp* is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. **Note: Register pair *rp* = SP may not be specified.**



Cycles: 3  
 States: 12 (8085), 11 (8080)  
 Addressing: reg. indirect  
 Flags: none

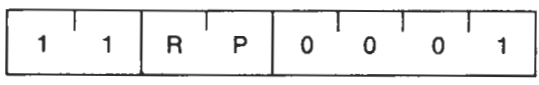
**PUSH PSW** (Push processor status word)  
 ((SP) — 1) — (A)  
 ((SP) — 2)<sub>0</sub> — (CY), ((SP) — 2)<sub>1</sub> — X  
 ((SP) — 2)<sub>2</sub> — (P), ((SP) — 2)<sub>3</sub> — X  
 ((SP) — 2)<sub>4</sub> — (AC), ((SP) — 2)<sub>5</sub> — X  
 ((SP) — 2)<sub>6</sub> — (Z), ((SP) — 2)<sub>7</sub> — (S)  
 (SP) — (SP) — 2 X: Undefined.



X: undefined

**POP rp** (Pop)  
 (rl) — ((SP))  
 (rh) — ((SP) + 1)  
 (SP) — (SP) + 2

The content of the memory location, whose address is specified by the content of register SP, is moved to the low-order register of register pair *rp*. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register *rp*. The content of register SP is incremented by 2. **Note: Register pair *rp* = SP may not be specified.**



Cycles: 3  
 States: 10  
 Addressing: reg.indirect  
 Flags: none

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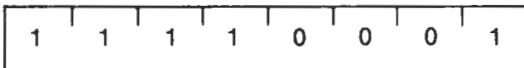
**THE INSTRUCTION SET**


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**POP PSW** (Pop processor status word)

$(CY) \leftarrow ((SP))_0$   
 $(P) \leftarrow ((SP))_2$   
 $(AC) \leftarrow ((SP))_4$   
 $(Z) \leftarrow ((SP))_6$   
 $(S) \leftarrow ((SP))_7$   
 $(A) \leftarrow ((SP) + 1)$   
 $(SP) \leftarrow (SP) + 2$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

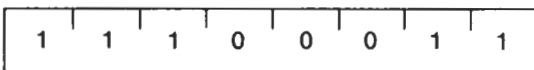


Cycles: 3  
 States: 10  
 Addressing: reg. indirect  
 Flags: Z,S,P,CY,AC

**XTHL** (Exchange stack top with H and L)

$(L) \leftrightarrow ((SP))$   
 $(H) \leftrightarrow ((SP) + 1)$

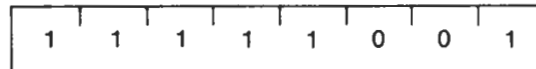
The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.



Cycles: 5  
 States: 16 (8085), 18 (8080)  
 Addressing: reg. indirect  
 Flags: none

**SPHL** (Move HL to SP)

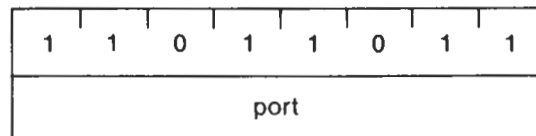
$(SP) \leftarrow (H) (L)$   
 The contents of registers H and L (16 bits) are moved to register SP.



Cycles: 1  
 States: 6 (8085), 5 (8080)  
 Addressing: register  
 Flags: none

**IN port** (Input)

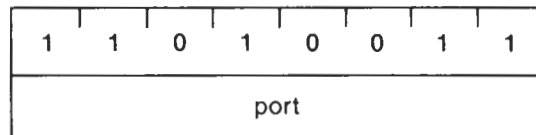
$(A) \leftarrow (\text{data})$   
 The data placed on the eight bit bi-directional data bus by the specified port is moved to register A.



Cycles: 3  
 States: 10  
 Addressing: direct  
 Flags: none

**OUT port** (Output)

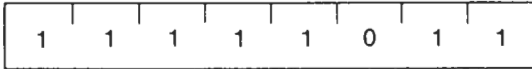
$(\text{data}) \leftarrow (A)$   
 The content of register A is placed on the eight bit bi-directional data bus for transmission to the specified port.



Cycles: 3  
 States: 10  
 Addressing: direct  
 Flags: none

THE INSTRUCTION SET

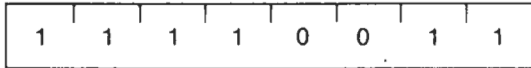
**EI** (Enable interrupts)  
 The interrupt system is enabled **following the execution of the next instruction. Interrupts are not recognized during the EI instruction.**



Cycles: 1  
 States: 4  
 Flags: none

NOTE: Placing an EI instruction on the bus in response to INTA during an INA cycle is prohibited. (8085)

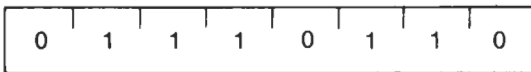
**DI** (Disable interrupts)  
 The interrupt system is disabled **immediately following the execution of the DI instruction. Interrupts are not recognized during the DI instruction.**



Cycles: 1  
 States: 4  
 Flags: none

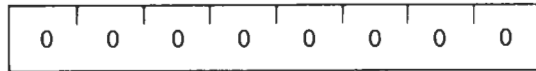
NOTE: Placing a DI instruction on the bus in response to INTA during an INA cycle is prohibited. (8085)

**HLT** (Halt)  
 The processor is stopped. The registers and flags are unaffected. (8080) A second ALE is generated during the execution of HLT to strobe out the Halt cycle status information. (8085)



Cycles: 1+ (8085), 1 (8080)  
 States: 5 (8085), 7 (8080)  
 Flags: none

**NOP** (No op)  
 No operation is performed. The registers and flags are unaffected.

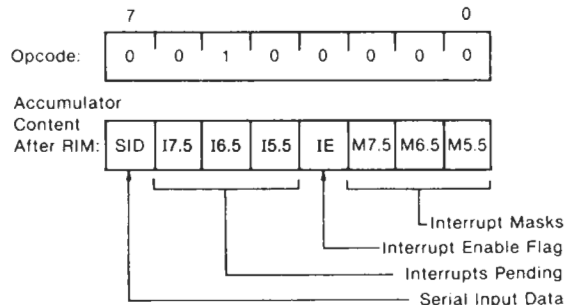


Cycles: 1  
 States: 4  
 Flags: none

**RIM** (Read Interrupt Masks) (8085 only)  
 The RIM instruction loads data into the accumulator relating to interrupts and the serial input. This data contains the following information:

- Current interrupt mask status for the RST 5.5, 6.5, and 7.5 hardware interrupts (1 = mask disabled)
- Current interrupt enable flag status (1 = interrupts enabled) except immediately following a TRAP interrupt. (See below.)
- Hardware interrupts pending (i.e., signal received but not yet serviced), on the RST 5.5, 6.5, and 7.5 lines.
- Serial input data.

Immediately following a TRAP interrupt, the RIM instruction must be executed as a part of the service routine if you need to retrieve current interrupt status later. Bit 3 of the accumulator is (in this special case only) loaded with the interrupt enable (IE) flag status that existed prior to the TRAP interrupt. Following an RST 5.5, 6.5, 7.5, or INTR interrupt, the interrupt flag flip-flop reflects the current interrupt enable status. Bit 6 of the accumulator (I7.5) is loaded with the status of the RST 7.5 flip-flop, which is always set (edge-triggered) by an input on the RST 7.5 input line, even when that interrupt has been previously masked. (See SIM Instruction.)



Cycles: 1  
 States: 4  
 Flags: none



## THE INSTRUCTION SET

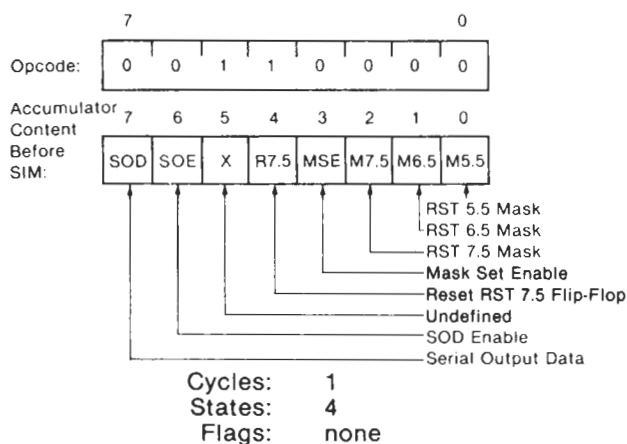
### SIM (Set Interrupt Masks) (8085 only)

The execution of the SIM instruction uses the contents of the accumulator (which must be previously loaded) to perform the following functions:

- Program the interrupt mask for the RST 5.5, 6.5, and 7.5 hardware interrupts.
- Reset the edge-triggered RST 7.5 input latch.
- Load the SOD output latch.

To program the interrupt masks, first set accumulator bit 3 to 1 and set to 1 any bits 0, 1, and 2, which disable interrupts RST 5.5, 6.5, and 7.5, respectively. Then do a SIM instruction. If accumulator bit 3 is 0 when the SIM instruction is executed, the interrupt mask register will not change. If accumulator bit 4 is 1 when the SIM instruction is executed, the RST 7.5 latch is then reset. RST 7.5 is distinguished by the fact that its latch is always set by a rising edge on the RST 7.5 input pin, even if the jump to service routine is inhibited by masking. This latch remains high until cleared by a  $\overline{\text{RESET IN}}$ , by a SIM Instruction with accumulator bit 4 high, or by an internal processor acknowledge to an RST 7.5 interrupt subsequent to the removal of the mask (by a SIM instruction). The  $\overline{\text{RESET IN}}$  signal always sets all three RST mask bits.

If accumulator bit 6 is at the 1 level when the SIM instruction is executed, the state of accumulator bit 7 is loaded into the SOD latch and thus becomes available for interface to an external device. The SOD latch is unaffected by the SIM instruction if bit 6 is 0. SOD is always reset by the  $\overline{\text{RESET IN}}$  signal.



8085A

8080A/8085A INSTRUCTION SET INDEX  
Table 5-1

| Instruction | Code      | Bytes | T States |       | Machine Cycles  |
|-------------|-----------|-------|----------|-------|-----------------|
|             |           |       | 8085A    | 8080A |                 |
| ACI DATA    | CE data   | 2     | 7        | 7     | F R             |
| ADC REG     | 1000 1SSS | 1     | 4        | 4     | F               |
| ADC M       | 8E        | 1     | 7        | 7     | F R             |
| ADD REG     | 1000 0SSS | 1     | 4        | 4     | F               |
| ADD M       | 86        | 1     | 7        | 7     | F R             |
| ADI DATA    | C6 data   | 2     | 7        | 7     | F R             |
| ANA REG     | 1010 0SSS | 1     | 4        | 4     | F               |
| ANA M       | A6        | 1     | 7        | 7     | F R             |
| ANI DATA    | E6 data   | 2     | 7        | 7     | F R             |
| CALL LABEL  | CD addr   | 3     | 18       | 17    | S R R W W*      |
| CC LABEL    | DC addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CM LABEL    | FC addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CMA         | 2F        | 1     | 4        | 4     | F               |
| CMC         | 3F        | 1     | 4        | 4     | F               |
| CMP REG     | 1011 1SSS | 1     | 4        | 4     | F               |
| CMP M       | BE        | 1     | 7        | 7     | F R             |
| CNC LABEL   | D4 addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CNZ LABEL   | C4 addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CP LABEL    | F4 addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CPE LABEL   | EC addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CPI DATA    | FE data   | 2     | 7        | 7     | F R             |
| CPO LABEL   | E4 addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| CZ LABEL    | CC addr   | 3     | 9/18     | 11/17 | S R*/S R R W W* |
| DAA         | 27        | 1     | 4        | 4     | F               |
| DAD RP      | 00RP 1001 | 1     | 10       | 10    | F B B           |
| DCR REG     | 00SS S101 | 1     | 4        | 5     | F*              |
| DCR M       | 35        | 1     | 10       | 10    | F R W           |
| DCX RP      | 00RP 1011 | 1     | 6        | 5     | S*              |
| DI          | F3        | 1     | 4        | 4     | F               |
| EI          | FB        | 1     | 4        | 4     | F               |
| HLT         | 76        | 1     | 5        | 7     | F B             |
| IN PORT     | DB data   | 2     | 10       | 10    | F R I           |
| INR REG     | 00SS S100 | 1     | 4        | 5     | F*              |
| INR M       | 34        | 1     | 10       | 10    | F R W           |
| INX RP      | 00RP 0011 | 1     | 6        | 5     | S*              |
| JC LABEL    | DA addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JM LABEL    | FA addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JMP LABEL   | C3 addr   | 3     | 10       | 10    | F R R           |
| JNC LABEL   | D2 addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JNZ LABEL   | C2 addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JP LABEL    | F2 addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JPE LABEL   | EA addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JPO LABEL   | E2 addr   | 3     | 7/10     | 10    | F R/F R R†      |
| JZ LABEL    | CA addr   | 3     | 7/10     | 10    | F R/F R R†      |
| LDA ADDR    | 3A addr   | 3     | 13       | 13    | F R R R         |
| LDAX RP     | 000X 1010 | 1     | 7        | 7     | F R             |
| LHLD ADDR   | 2A addr   | 3     | 16       | 16    | F R R R R       |

| Instruction      | Code             | Bytes | T States |       | Machine Cycles |
|------------------|------------------|-------|----------|-------|----------------|
|                  |                  |       | 8085A    | 8080A |                |
| LXI RP,DATA16    | 00RP 0001 data16 | 3     | 10       | 10    | F R R          |
| MOV REG,REG      | 01DD 0SSS        | 1     | 4        | 5     | F*             |
| MOV M,REG        | 0111 0SSS        | 1     | 7        | 7     | F W            |
| MOV REG,M        | 01DD D110        | 1     | 7        | 7     | F R            |
| MVI REG,DATA     | 00DD D110 data   | 2     | 7        | 7     | F R            |
| MVI M,DATA       | 36 data          | 2     | 10       | 10    | F R W          |
| NOP              | 00               | 1     | 4        | 4     | F              |
| ORA REG          | 1011 0SSS        | 1     | 4        | 4     | F              |
| ORA M            | B6               | 1     | 7        | 7     | F R            |
| ORI DATA         | F6 data          | 2     | 7        | 7     | F R            |
| OUT PORT         | D3 data          | 2     | 10       | 10    | F R O          |
| PCHL             | E9               | 1     | 6        | 5     | S*             |
| POP RP           | 11RP 0001        | 1     | 10       | 10    | F R R          |
| PUSH RP          | 11RP 0101        | 1     | 12       | 11    | SWW*           |
| RAL              | 17               | 1     | 4        | 4     | F              |
| RAR              | 1F               | 1     | 4        | 4     | F              |
| RC               | D8               | 1     | 6/12     | 5/11  | S/S R R*       |
| RET              | C9               | 1     | 10       | 10    | F R R          |
| RIM (8085A only) | 20               | 1     | 4        | -     | F              |
| RLC              | 07               | 1     | 4        | 4     | F              |
| RM               | F8               | 1     | 6/12     | 5/11  | S/S R R*       |
| RNC              | D0               | 1     | 6/12     | 5/11  | S/S R R*       |
| RNZ              | C0               | 1     | 6/12     | 5/11  | S/S R R*       |
| RP               | F0               | 1     | 6/12     | 5/11  | S/S R R*       |
| RPE              | E8               | 1     | 6/12     | 5/11  | S/S R R*       |
| RPO              | E0               | 1     | 6/12     | 5/11  | S/S R R*       |
| RRC              | 0F               | 1     | 4        | 4     | F              |
| RST N            | 11XX X111        | 1     | 12       | 11    | SWW*           |
| RZ               | C8               | 1     | 6/12     | 5/11  | S/S R R*       |
| SBB REG          | 1001 1SSS        | 1     | 4        | 4     | F              |
| SBB M            | 9E               | 1     | 7        | 7     | F R            |
| SBI DATA         | DE data          | 2     | 7        | 7     | F R            |
| SHLD ADDR        | 22 addr          | 3     | 16       | 16    | F R R W W      |
| SIM (8085A only) | 30               | 1     | 4        | -     | F              |
| SPHL             | F9               | 1     | 6        | 5     | S*             |
| STA ADDR         | 32 addr          | 3     | 13       | 13    | F R R W        |
| STAX RP          | 000X 0010        | 1     | 7        | 7     | F W            |
| STC              | 37               | 1     | 4        | 4     | F              |
| SUB REG          | 1001 0SSS        | 1     | 4        | 4     | F              |
| SUB M            | 96               | 1     | 7        | 7     | F R            |
| SUI DATA         | D6 data          | 2     | 7        | 7     | F R            |
| XCHG             | EB               | 1     | 4        | 4     | F              |
| XRA REG          | 1010 1SSS        | 1     | 4        | 4     | F              |
| XRA M            | AE               | 1     | 7        | 7     | F R            |
| XRI DATA         | EE data          | 2     | 7        | 7     | F R            |
| XTHL             | E3               | 1     | 16       | 18    | F R R W W      |

Machine cycle types:

- F Four clock period instr fetch
- S Six clock period instr fetch
- R Memory read
- I I/O read
- W Memory write
- O I/O write
- B Bus idle
- X Variable or optional binary digit
- DDD Binary digits identifying a destination register B - 000, C - 001, D - 010 Memory - 110
- SSS Binary digits identifying a source register E - 011, H - 100, L - 101 A - 111
- RP Register Pair BC - 00, HL - 10 DE - 01, SP - 11

\*Five clock period instruction fetch with 8080A.

†The longer machine cycle sequence applies regardless of condition evaluation with 8080A.

•An extra READ cycle (R) will occur for this condition with 8080A.

## 8085A

**8085A CPU INSTRUCTIONS IN OPERATION CODE SEQUENCE**  
**Table 5-2**

| OP CODE | MNEMONIC  | OP CODE | MNEMONIC   | OP CODE | MNEMONIC | OP CODE | MNEMONIC | OP CODE | MNEMONIC | OP CODE | MNEMONIC |
|---------|-----------|---------|------------|---------|----------|---------|----------|---------|----------|---------|----------|
| 00      | NOP       | 2B      | DCX H      | 56      | MOV D,M  | 81      | ADD C    | AC      | XRA H    | D7      | RST 2    |
| 01      | LXI B,D16 | 2C      | INR L      | 57      | MOV D,A  | 82      | ADD D    | AD      | XRA L    | D8      | RC       |
| 02      | STAX B    | 2D      | DCR L      | 58      | MOV E,B  | 83      | ADD E    | AE      | XRA M    | D9      | -        |
| 03      | INX B     | 2E      | MVI L,D8   | 59      | MOV E,C  | 84      | ADD H    | AF      | XRA A    | DA      | JC Adr   |
| 04      | INR B     | 2F      | CMA        | 5A      | MOV E,D  | 85      | ADD L    | B0      | ORA B    | DB      | IN D8    |
| 05      | DCR B     | 30      | SIM        | 5B      | MOV E,E  | 86      | ADD M    | B1      | ORA C    | DC      | CC Adr   |
| 06      | MVI B,D8  | 31      | LXI SP,D16 | 5C      | MOV E,H  | 87      | ADD A    | B2      | ORA D    | DD      | -        |
| 07      | RLC       | 32      | STA Adr    | 5D      | MOV E,L  | 88      | ADC B    | B3      | ORA E    | DE      | SBI D8   |
| 08      | -         | 33      | INX SP     | 5E      | MOV E,M  | 89      | ADC C    | B4      | ORA H    | DF      | RST 3    |
| 09      | DAD B     | 34      | INR M      | 5F      | MOV E,A  | 8A      | ADC D    | B5      | ORA L    | E0      | RPO      |
| 0A      | LDAX B    | 35      | DCR M      | 60      | MOV H,B  | 8B      | ADC E    | B6      | ORA M    | E1      | POP H    |
| 0B      | DCX B     | 36      | MVI M,D8   | 61      | MOV H,C  | 8C      | ADC H    | B7      | ORA A    | E2      | JPO Adr  |
| 0C      | INR C     | 37      | STC        | 62      | MOV H,D  | 8D      | ADC L    | B8      | CMP B    | E3      | XTHL     |
| 0D      | DCR C     | 38      | -          | 63      | MOV H,E  | 8E      | ADC M    | B9      | CMP C    | E4      | CPO Adr  |
| 0E      | MVI C,D8  | 39      | DAD SP     | 64      | MOV H,H  | 8F      | ADC A    | BA      | CMP D    | E5      | PUSH H   |
| 0F      | RRC       | 3A      | LDA Adr    | 65      | MOV H,L  | 90      | SUB B    | BB      | CMP E    | E6      | ANI D8   |
| 10      | -         | 3B      | DCX SP     | 66      | MOV H,M  | 91      | SUB C    | BC      | CMP H    | E7      | RST 4    |
| 11      | LXI D,D16 | 3C      | INR A      | 67      | MOV H,A  | 92      | SUB D    | BD      | CMP L    | E8      | RPE      |
| 12      | STAX D    | 3D      | DCR A      | 68      | MOV L,B  | 93      | SUB E    | BE      | CMP M    | E9      | PCHL     |
| 13      | INX D     | 3E      | MVI A,D8   | 69      | MOV L,C  | 94      | SUB H    | BF      | CMP A    | EA      | JPE Adr  |
| 14      | INR D     | 3F      | CMC        | 6A      | MOV L,D  | 95      | SUB L    | C0      | RNZ      | EB      | XCHG     |
| 15      | DCR D     | 40      | MOV B,B    | 6B      | MOV L,E  | 96      | SUB M    | C1      | POP B    | EC      | CPE Adr  |
| 16      | MVI D,D8  | 41      | MOV B,C    | 6C      | MOV L,H  | 97      | SUB A    | C2      | JNZ Adr  | ED      | -        |
| 17      | RAL       | 42      | MOV B,D    | 6D      | MOV L,L  | 98      | SBB B    | C3      | JMP Adr  | EE      | XRI D8   |
| 18      | -         | 43      | MOV B,E    | 6E      | MOV L,M  | 99      | SBB C    | C4      | CNZ Adr  | EF      | RST 5    |
| 19      | DAD D     | 44      | MOV B,H    | 6F      | MOV L,A  | 9A      | SBB D    | C5      | PUSH B   | F0      | RP       |
| 1A      | LDAX D    | 45      | MOV B,L    | 70      | MOV M,B  | 9B      | SBB E    | C6      | ADI D8   | F1      | POP PSW  |
| 1B      | DCX D     | 46      | MOV B,M    | 71      | MOV M,C  | 9C      | SBB H    | C7      | RST 0    | F2      | JP Adr   |
| 1C      | INR E     | 47      | MOV B,A    | 72      | MOV M,D  | 9D      | SBB L    | C8      | RZ       | F3      | DI       |
| 1D      | DCR E     | 48      | MOV C,B    | 73      | MOV M,E  | 9E      | SBB M    | C9      | RET Adr  | F4      | CP Adr   |
| 1E      | MVI E,D8  | 49      | MOV C,C    | 74      | MOV M,H  | 9F      | SBB A    | CA      | JZ       | F5      | PUSH PSW |
| 1F      | RAR       | 4A      | MOV C,D    | 75      | MOV M,L  | A0      | ANA B    | CB      | -        | F6      | ORI D8   |
| 20      | RIM       | 4B      | MOV C,E    | 76      | HLT      | A1      | ANA C    | CC      | CZ Adr   | F7      | RST 6    |
| 21      | LXI H,D16 | 4C      | MOV C,H    | 77      | MOV M,A  | A2      | ANA D    | CD      | CALL Adr | F8      | RM       |
| 22      | SHLD Adr  | 4D      | MOV C,L    | 78      | MOV M,B  | A3      | ANA E    | CE      | ACI D8   | F9      | SPHL     |
| 23      | INX H     | 4E      | MOV C,M    | 79      | MOV M,C  | A4      | ANA H    | CF      | RST 1    | FA      | JM Adr   |
| 24      | INR H     | 4F      | MOV C,A    | 7A      | MOV M,D  | A5      | ANA L    | D0      | RNC      | FB      | EI       |
| 25      | DCR H     | 50      | MOV D,B    | 7B      | MOV M,E  | A6      | ANA M    | D1      | POP D    | FC      | CM Adr   |
| 26      | MVI H,D8  | 51      | MOV D,C    | 7C      | MOV M,H  | A7      | ANA A    | D2      | JNC Adr  | FD      | -        |
| 27      | DAA       | 52      | MOV D,D    | 7D      | MOV M,L  | A8      | XRA B    | D3      | OUT D8   | FE      | CPI D8   |
| 28      | -         | 53      | MOV D,E    | 7E      | MOV M,M  | A9      | XRA C    | D4      | CNC Adr  | FF      | RST 7    |
| 29      | DAD H     | 54      | MOV D,H    | 7F      | MOV M,A  | AA      | XRA D    | D5      | PUSH D   |         |          |
| 2A      | LHLD Adr  | 55      | MOV D,L    | 80      | ADD B    | AB      | XRA E    | D6      | SUI D8   |         |          |

D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity.

Adr = 16-bit address.

D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity.

## 8085A

**8085A INSTRUCTION SET SUMMARY BY FUNCTIONAL GROUPING**  
Table 5-3

| Mnemonic                     | Description                           | Instruction Code (1) |    |    |    |    |    |    |    | Page | Mnemonic                       | Description                      | Instruction Code (1) |    |    |    |    |    |    |    | Page |
|------------------------------|---------------------------------------|----------------------|----|----|----|----|----|----|----|------|--------------------------------|----------------------------------|----------------------|----|----|----|----|----|----|----|------|
|                              |                                       | D7                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |      |                                |                                  | D7                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |      |
| <b>MOVE, LOAD, AND STORE</b> |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| MOV r1 r2                    | Move register to register             | 0                    | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 5-4  | CZ                             | Call on zero                     | 1                    | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 5-14 |
| MOV M,r                      | Move register to memory               | 0                    | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 5-4  | GNZ                            | Call on no zero                  | 1                    | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 5-14 |
| MOV r,M                      | Move memory to register               | 0                    | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 5-4  | CP                             | Call on positive                 | 1                    | 1  | 1  | 1  | 0  | 1  | 0  | 0  | 5-14 |
| MVI r                        | Move immediate register               | 0                    | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 5-4  | CM                             | Call on minus                    | 1                    | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 5-14 |
| MVI M                        | Move immediate memory                 | 0                    | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 5-4  | CPE                            | Call on parity even              | 1                    | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 5-14 |
| LXI B                        | Load immediate register<br>Pair B & C | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 5-5  | CPO                            | Call on parity odd               | 1                    | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 5-14 |
| LXI D                        | Load immediate register<br>Pair D & E | 0                    | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 5-5  | <b>RETURN</b>                  |                                  |                      |    |    |    |    |    |    |    |      |
| LXI H                        | Load immediate register<br>Pair H & L | 0                    | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 5-5  | RET                            | Return                           | 1                    | 1  | 0  | 0  | 1  | 0  | 0  | 1  | 5-14 |
| STAX B                       | Store A indirect                      | 0                    | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 5-6  | RC                             | Return on carry                  | 1                    | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 5-14 |
| STAX D                       | Store A indirect                      | 0                    | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 5-6  | RNC                            | Return on no carry               | 1                    | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 5-14 |
| LDAX B                       | Load A indirect                       | 0                    | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 5-5  | RZ                             | Return on zero                   | 1                    | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 5-14 |
| LDAX D                       | Load A indirect                       | 0                    | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 5-5  | RNZ                            | Return on no zero                | 1                    | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 5-14 |
| STA                          | Store A direct                        | 0                    | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 5-5  | RP                             | Return on positive               | 1                    | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 5-14 |
| LDA                          | Load A direct                         | 0                    | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 5-5  | RM                             | Return on minus                  | 1                    | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 5-14 |
| SHLD                         | Store H & L direct                    | 0                    | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 5-5  | RPE                            | Return on parity even            | 1                    | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 5-14 |
| LHLD                         | Load H & L direct                     | 0                    | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 5-5  | RPO                            | Return on parity odd             | 1                    | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 5-14 |
| XCHG                         | Exchange D & E, H & L<br>Registers    | 1                    | 1  | 1  | 0  | 1  | 0  | 1  | 1  | 5-6  | <b>RESTART</b>                 |                                  |                      |    |    |    |    |    |    |    |      |
| <b>STACK OPS</b>             |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| PUSH B                       | Push register Pair B &<br>C on stack  | 1                    | 1  | 0  | 0  | 0  | 1  | 0  | 1  | 5-15 | RST                            | Restart                          | 1                    | 1  | A  | A  | A  | 1  | 1  | 1  | 5-14 |
| PUSH D                       | Push register Pair D &<br>E on stack  | 1                    | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 5-15 | <b>INPUT/OUTPUT</b>            |                                  |                      |    |    |    |    |    |    |    |      |
| PUSH H                       | Push register Pair H &<br>L on stack  | 1                    | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 5-15 | IN                             | Input                            | 1                    | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 5-16 |
| PUSH PSW                     | Push A and Flags<br>on stack          | 1                    | 1  | 1  | 1  | 0  | 1  | 0  | 1  | 5-15 | OUT                            | Output                           | 1                    | 1  | 0  | 1  | 0  | 0  | 1  | 1  | 5-16 |
| POP B                        | Pop register Pair B &<br>C off stack  | 1                    | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 5-15 | <b>INCREMENT AND DECREMENT</b> |                                  |                      |    |    |    |    |    |    |    |      |
| POP D                        | Pop register Pair D &<br>E off stack  | 1                    | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 5-15 | INR r                          | Increment register               | 0                    | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 5-8  |
| POP H                        | Pop register Pair H &<br>L off stack  | 1                    | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 5-15 | OCR r                          | Decrement register               | 0                    | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 5-8  |
| POP PSW                      | Pop A and Flags<br>off stack          | 1                    | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 5-15 | INR M                          | Increment memory                 | 0                    | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 5-8  |
| XTHL                         | Exchange top of<br>stack, H & L       | 1                    | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 5-16 | OCR M                          | Decrement memory                 | 0                    | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 5-8  |
| SPhL                         | H & L to stack pointer                | 1                    | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 5-16 | INX B                          | Increment B & C<br>registers     | 0                    | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 5-9  |
| LXI SP                       | Load immediate stack<br>pointer       | 0                    | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 5-5  | INX D                          | Increment D & E<br>registers     | 0                    | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 5-9  |
| INX SP                       | Increment stack pointer               | 0                    | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 5-9  | INX H                          | Increment H & L<br>registers     | 0                    | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 5-9  |
| DCX SP                       | Decrement stack<br>pointer            | 0                    | 0  | 1  | 1  | 1  | 0  | 1  | 1  | 5-9  | DCX B                          | Decrement B & C                  | 0                    | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 5-9  |
| <b>JUMP</b>                  |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| JMP                          | Jump unconditional                    | 1                    | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 5-13 | DCX D                          | Decrement D & E                  | 0                    | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 5-9  |
| JC                           | Jump on carry                         | 1                    | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 5-13 | DCX H                          | Decrement H & L                  | 0                    | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 5-9  |
| JNC                          | Jump on no carry                      | 1                    | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 5-13 | DCX SP                         | Decrement H & L                  | 0                    | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 5-9  |
| JZ                           | Jump on zero                          | 1                    | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 5-13 | <b>ADD</b>                     |                                  |                      |    |    |    |    |    |    |    |      |
| JNZ                          | Jump on no zero                       | 1                    | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 5-13 | ADD r                          | Add register to A                | 1                    | 0  | 0  | 0  | 0  | S  | S  | S  | 5-6  |
| JP                           | Jump on positive                      | 1                    | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 5-13 | ADC r                          | Add register to A<br>with carry  | 1                    | 0  | 0  | 0  | 1  | S  | S  | S  | 5-6  |
| JM                           | Jump on minus                         | 1                    | 1  | 1  | 1  | 1  | 0  | 1  | 0  | 5-13 | ADD M                          | Add memory to A                  | 1                    | 0  | C  | 0  | 0  | 1  | 1  | 0  | 5-6  |
| JPE                          | Jump on parity even                   | 1                    | 1  | 1  | 0  | 1  | 0  | 1  | 0  | 5-13 | ADC M                          | Add memory to A<br>with carry    | 1                    | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 5-7  |
| JPO                          | Jump on parity odd                    | 1                    | 1  | 1  | 0  | 0  | 0  | 1  | 0  | 5-13 | ADI                            | Add immediate to A               | 1                    | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 5-6  |
| PCHL                         | H & L to program<br>counter           | 1                    | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 5-15 | ACI                            | Add immediate to A<br>with carry | 1                    | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 5-7  |
| <b>CALL</b>                  |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| CALL                         | Call unconditional                    | 1                    | 1  | 0  | 0  | 1  | 1  | 0  | 1  | 5-13 | DAD B                          | Add B & C to H & L               | 0                    | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 5-9  |
| CC                           | Call on carry                         | 1                    | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 5-14 | DAD D                          | Add D & E to H & L               | 0                    | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 5-9  |
| CNC                          | Call on no carry                      | 1                    | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 5-14 | DAD H                          | Add H & L to H & L               | 0                    | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 5-9  |
| <b>SUBTRACT</b>              |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| <b>CALL</b>                  |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| <b>SUBTRACT</b>              |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |
| <b>CALL</b>                  |                                       |                      |    |    |    |    |    |    |    |      |                                |                                  |                      |    |    |    |    |    |    |    |      |

## 8085A

**8085A INSTRUCTION SET SUMMARY (Cont'd)**  
**Table 5-3**

| Mnemonic       | Description                           | Instruction Code (1) |    |    |    |    |    |    |    | Page | Mnemonic                      | Description                  | Instruction Code (1) |    |    |    |    |    |    |    | Page |                 |                             |   |   |   |   |   |   |   |   |      |
|----------------|---------------------------------------|----------------------|----|----|----|----|----|----|----|------|-------------------------------|------------------------------|----------------------|----|----|----|----|----|----|----|------|-----------------|-----------------------------|---|---|---|---|---|---|---|---|------|
|                |                                       | D7                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |      |                               |                              | D7                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |      |                 |                             |   |   |   |   |   |   |   |   |      |
| SBI            | Subtract immediate from A with borrow | 1                    | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 5-8  | RRC                           | Rotate A right               | 0                    | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 5-12 | RAL             | Rotate A left through carry | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 5-12 |
| <b>LOGICAL</b> |                                       |                      |    |    |    |    |    |    |    |      |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| ANA r          | And register with A                   | 1                    | 0  | 1  | 0  | 0  | S  | S  | S  | 5-9  | RAR                           | Rotate A right through carry | 0                    | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 5-12 | <b>SPECIALS</b> |                             |   |   |   |   |   |   |   |   |      |
| XRA r          | Exclusive OR register with A          | 1                    | 0  | 1  | 0  | 1  | S  | S  | S  | 5-10 | CMA                           | Complement A                 | 0                    | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 5-12 | STC             | Set carry                   | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 5-12 |
| ORA r          | OR register with A                    | 1                    | 0  | 1  | 1  | 0  | S  | S  | S  | 5-10 | CMC                           | Complement carry             | 0                    | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 5-12 | DAA             | Decimal adjust A            | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 5-9  |
| CMP r          | Compare register with A               | 1                    | 0  | 1  | 1  | 1  | S  | S  | S  | 5-11 | <b>CONTROL</b>                |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| ANA M          | And memory with A                     | 1                    | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 5-10 | EI                            | Enable interrupts            | 1                    | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 5-17 | DI              | Disable interrupt           | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 5-17 |
| XRA M          | Exclusive OR memory with A            | 1                    | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 5-10 | NOP                           | No-operation                 | 0                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 5-17 | HLT             | Halt                        | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 5-17 |
| ORA M          | OR memory with A                      | 1                    | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 5-11 | <b>NEW 8085A INSTRUCTIONS</b> |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| CMP M          | Compare memory with A                 | 1                    | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 5-11 | RIM                           | Read Interrupt Mask          | 0                    | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 5-17 | SIM             | Set Interrupt Mask          | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 5-18 |
| ANI            | And immediate with A                  | 1                    | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 5-10 |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| XRI            | Exclusive OR immediate with A         | 1                    | 1  | 1  | 0  | 1  | 1  | 1  | 0  | 5-10 |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| ORI            | OR immediate with A                   | 1                    | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 5-11 |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| CPI            | Compare immediate with A              | 1                    | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 5-11 |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| <b>ROTATE</b>  |                                       |                      |    |    |    |    |    |    |    |      |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |
| RLC            | Rotate A left                         | 0                    | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 5-11 |                               |                              |                      |    |    |    |    |    |    |    |      |                 |                             |   |   |   |   |   |   |   |   |      |

NOTES: 1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.

2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.



## APPENDIX D

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### **Data Sheets**

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## Data Sheet Index

### MAIN BOARD

| PART NUMBER | MODEL NUMBER | DESCRIPTION  | PAGE NUMBER |
|-------------|--------------|--|-------------|
| 443-970     | 6665         | Dynamic RAM  | D.4         |
| 443-1010    | 8085A-2      | Single Chip 8 BIT N-Channel Microprocessor             | D.21        |
| 443-1012    | 8259A        | Programmable Interrupt Controller                      | D.37        |
| 443-1014    | 68A21        | Peripheral Interface Adapter                           | D.56        |
| 443-1040    | 9602         | Dual Retriggerable Resettable Monostable Multivibrator | D.67        |
| 443-1061    | 2661         | Enhanced Programmable Communications Interface         | D.74        |
| 443-1066    | 8253         | Programmable Interval Timer                            | D.94        |
| 444-126     | PAL16L8      | Memory Timing Control                                  | D.105       |
| 444-128     | PAL12H6      | Processor Swap   | D.105       |
| 444-129     | PAL16L2      | PROM Address Decode                                    | D.105       |
| 444-130     | PAL14L4      | Memory HIADS Decode                                    | D.105       |
| 444-9018    | 27S21        | 1024 Bit Generic Series Bipolar PROM                   | D.116       |
| 444-9019    | 27S19        | Bipolar PROM   | D.122       |
| 444-9027    | 2764         | UV Erasable PROM                                       | D.128       |
| 444-9031    | 8741A        | Universal Peripheral Interface                         | D.134       |

### VIDEO LOGIC BOARD

| PART NUMBER | MODEL NUMBER | DESCRIPTION     | PAGE NUMBER |
|-------------|--------------|-----------------|-------------|
| 443-1013    | 68A45        | CRT Controller  | D.146       |
| 444-9011    | TBP18522     | PROM            | D.176       |
| 443-970     | 6665         | 64K Dynamic RAM | D.4         |
| 443-1106    | 6633         | 32K Dynamic RAM | D.219       |

### FLOPPY DISK CONTROLLER BOARD (Z-207)

| PART NUMBER | MODEL NUMBER | DESCRIPTION                | PAGE NUMBER |
|-------------|--------------|----------------------------|-------------|
| 443-997     | 1790         | Floppy Disk Formatter      | D.184       |
| 443-998     | 1691         | Floppy Support Logic       | D.207       |
| 443-1000    | 2143         | Four Phase Clock Generator | D.215       |



# Main Board



**MOTOROLA**

# SEMICONDUCTORS

3501 ED BLUESTEIN BLVD. AUSTIN, TEXAS 78721

## 64K BIT DYNAMIC RAM

The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

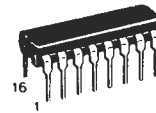
- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation ( $\pm 10\%$ )
- Full Power Supply Range Capabilities
- Maximum Access Time
  - MCM6665A-12 = 120 ns
  - MCM6665A-15 = 150 ns
  - MCM6665A-20 = 200 ns
- Low Power Dissipation
  - 302.5 mW Maximum (Active) (MCM6665A-15)
  - 22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate  $< 0.1\%$  per 1000 Hours (See Soft Error Testing)

## MCM6665A

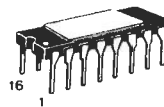
### MOS

(N-CHANNEL, SILICON-GATE)

### 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

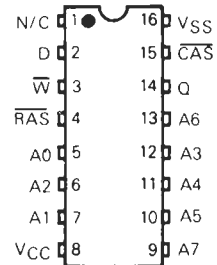


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 690

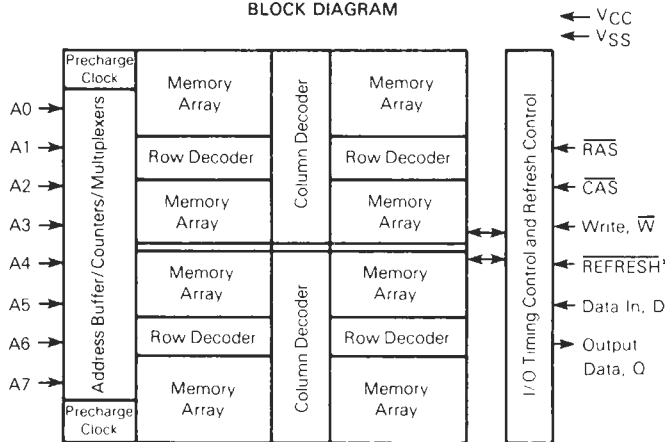
### PIN ASSIGNMENT



### PIN NAMES

|                         |                       |
|-------------------------|-----------------------|
| A0-A7                   | Address Input         |
| D                       | Data In               |
| Q                       | Data Out              |
| $\overline{\text{W}}$   | Read/Write Input      |
| $\overline{\text{RAS}}$ | Row Address Strobe    |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| V <sub>CC</sub>         | Power (+5 V)          |
| V <sub>SS</sub>         | Ground                |

### BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

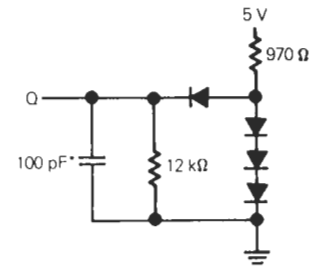
MCM6665A

## ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating   | Symbol                             | Value       | Unit |
|--|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V <sub>SS</sub> (except V <sub>CC</sub> ) | V <sub>in</sub> , V <sub>out</sub> | -2 to +7    | V    |
| Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>            | V <sub>CC</sub>                    | -1 to +7    | V    |
| Operating Temperature Range  | T <sub>A</sub>                     | 0 to +70    | °C   |
| Storage Temperature Range  | T <sub>stg</sub>                   | -65 to +150 | °C   |
| Power Dissipation  | P <sub>D</sub>                     | 1.0         | W    |
| Data Out Current   | I <sub>out</sub>                   | 50          | mA   |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



\*Includes Jig Capacitance

## DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

## RECOMMENDED OPERATING CONDITIONS

| Parameter                   | Symbol                | Min             | Typ | Max                | Unit | Notes |   |
|-----------------------------|-----------------------|-----------------|-----|--------------------|------|-------|---|
| Supply Voltage              | MCM6665A-12, -15, -20 | V <sub>CC</sub> | 4.5 | 5.0                | 5.5  | V     | 1 |
|                             | V <sub>SS</sub>       | 0               | 0   | 0                  | V    | 1     |   |
| Logic 1 Voltage, All Inputs | V <sub>IH</sub>       | 2.4             | —   | V <sub>CC</sub> +1 | V    | 1     |   |
| Logic 0 Voltage, All Inputs | V <sub>IL</sub>       | -1.0*           | —   | 0.8                | V    | 1     |   |

\*The device will withstand undershoots to the -2 volt level with a maximum pulse width of 20 ns at the -1.5 volt level. This is periodically sampled rather than 100% tested.

## DC CHARACTERISTICS

| Characteristic  | Symbol            | Min | Max            | Units   | Notes |
|---|-------------------|-----|----------------|---------|-------|
| V <sub>CC</sub> Power Supply Current (Standby)  | I <sub>CC2</sub>  | —   | 4.0            | mA      | 5     |
| V <sub>CC</sub> Power Supply Current<br>6665A-12, t <sub>RC</sub> = 250 ns<br>6665A-15, t <sub>RC</sub> = 270 ns<br>6665A-20, t <sub>RC</sub> = 330 ns  | I <sub>CC1</sub>  | —   | 60<br>55<br>50 | mA      | 4     |
| V <sub>CC</sub> Power Supply Current During $\overline{\text{RAS}}$ only Refresh Cycles<br>6665A-12, t <sub>RC</sub> = 250 ns<br>6665A-15, t <sub>RC</sub> = 270 ns<br>6665A-20, t <sub>RC</sub> = 330 ns   | I <sub>CC3</sub>  | —   | 50<br>45<br>40 | mA      | 4     |
| V <sub>CC</sub> Power Supply Current During Page Mode Cycle for t <sub>RAS</sub> = 10 $\mu$ sec<br>6665A-12, t <sub>PC</sub> = t <sub>RP</sub> = 120 ns<br>6665A-15, t <sub>PC</sub> = t <sub>RP</sub> = 145 ns<br>6665A-20, t <sub>PC</sub> = t <sub>RP</sub> = 200 ns | I <sub>CC4</sub>  | —   | 45<br>40<br>35 | mA      | 4     |
| Input Leakage Current (V <sub>SS</sub> $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> )  | I <sub>I(L)</sub> | —   | 10             | $\mu$ A | —     |
| Output Leakage Current ( $\overline{\text{CAS}}$ at logic 1, V <sub>SS</sub> $\leq$ V <sub>out</sub> $\leq$ V <sub>CC</sub> )   | I <sub>O(L)</sub> | —   | 10             | $\mu$ A | —     |
| Output Logic 1 Voltage @ I <sub>out</sub> = -4 mA   | V <sub>OH</sub>   | 2.4 | —              | V       | —     |
| Output Logic 0 Voltage @ I <sub>out</sub> = 4 mA  | V <sub>OL</sub>   | —   | 0.4            | V       | —     |

CAPACITANCE (f = 1.0 MHz, T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V Periodically Sampled Rather Than 100% Tested)

| Parameter  | Symbol          | Typ | Max | Unit | Notes |
|--|-----------------|-----|-----|------|-------|
| Input Capacitance (A0-A7), D   | C <sub>I1</sub> | 3   | 5   | pF   | 7     |
| Input Capacitance $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , WRITE            | C <sub>I2</sub> | 6   | 8   | pF   | 7     |
| Output Capacitance (Q), ( $\overline{\text{CAS}}$ = V <sub>IH</sub> to disable output) | C <sub>O</sub>  | 5   | 7   | pF   | 7     |

- NOTES:
- All voltages referenced to V<sub>SS</sub>.
  - V<sub>IH</sub> min and V<sub>IL</sub> max are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
  - An initial pause of 100  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is guaranteed.
  - Current is a function of cycle rate and output loading, maximum current is measured at the fastest cycle rate with the output open.
  - $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are both at a logic 1.
  - The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
  - Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = \frac{I\Delta t}{\Delta V}$



MOTOROLA Semiconductor Products Inc.

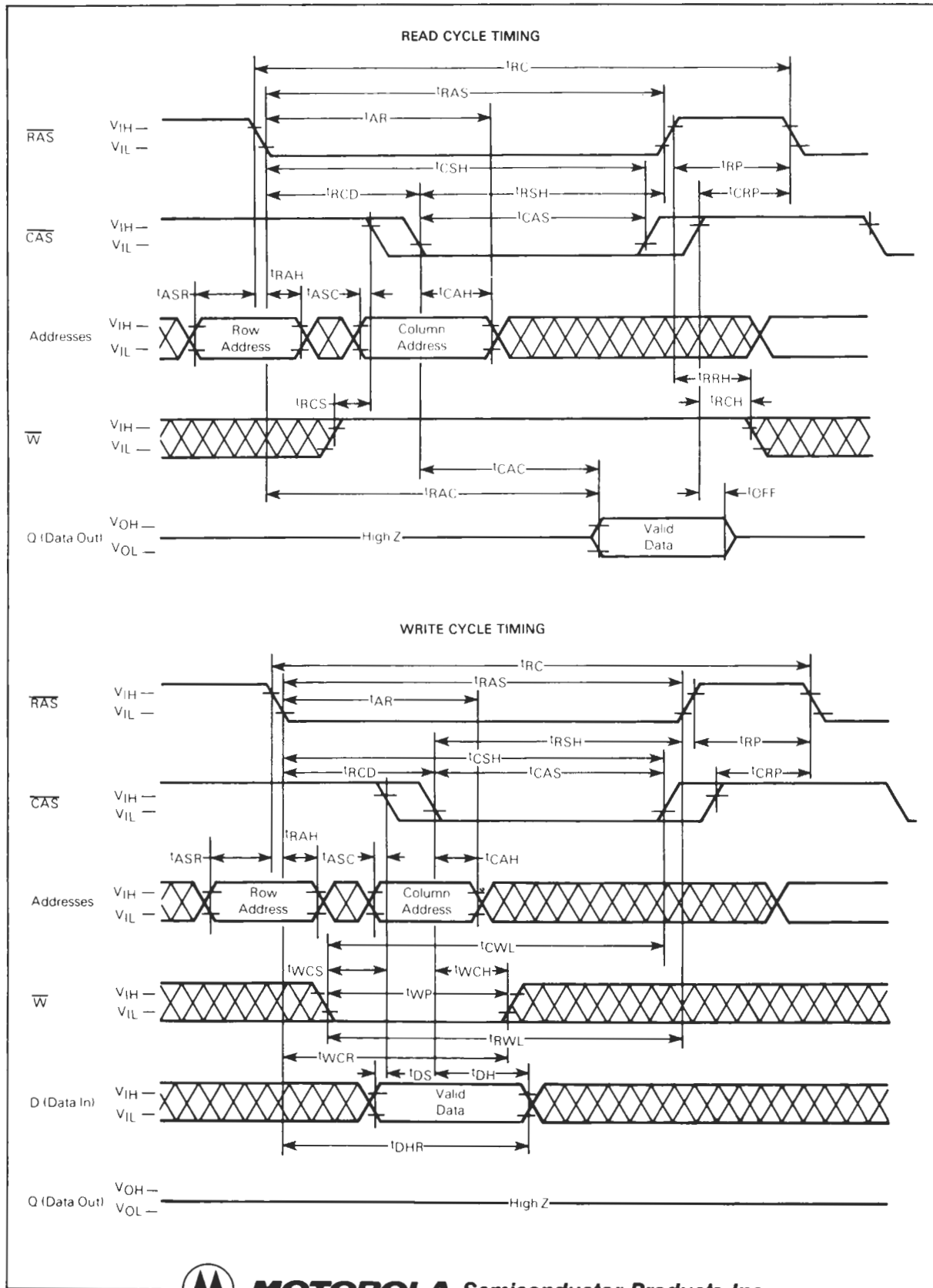
## MCM6665A

**AC OPERATING CONDITIONS AND CHARACTERISTICS** (Read, Write, and Read Modify Write Cycles)  
(Full Operating Voltage and Temperature Range Unless Otherwise Noted. See Notes 2, 3, 6, and Figure 1)

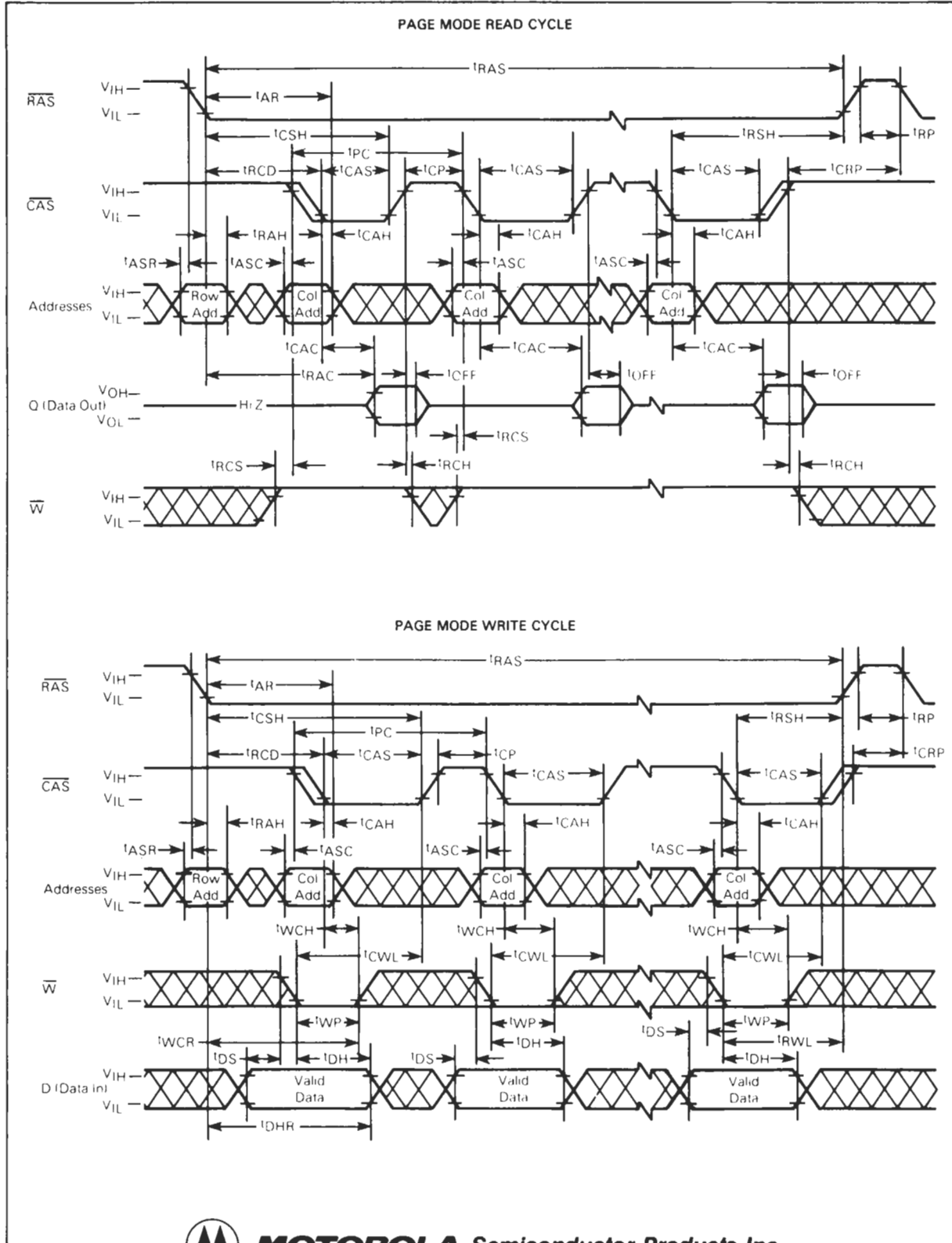
| Parameter                                  | Symbol             | 6665A-12 |       | 6665A-15 |       | 6665A-20 |       | Units | Notes  |
|--|--------------------|----------|-------|----------|-------|----------|-------|-------|--------|
|  |                    | Min      | Max   | Min      | Max   | Min      | Max   |       |        |
| Random Read or Write Cycle Time            | t <sub>RC</sub>    | 250      |       | 270      |       | 330      |       | ns    | 8, 9   |
| Read Write Cycle Time                      | t <sub>RWC</sub>   | 255      |       | 280      |       | 345      |       | ns    | 8, 9   |
| Access Time from Row Address Strobe        | t <sub>RAC</sub>   |          | 120   |          | 150   |          | 200   | ns    | 10, 12 |
| Access Time from Column Address Strobe     | t <sub>CAC</sub>   |          | 60    |          | 75    |          | 100   | ns    | 11, 12 |
| Output Buffer and Turn-Off Delay           | t <sub>OFF</sub>   | 0        | 30    | 0        | 30    | 0        | 40    | ns    | 18     |
| Row Address Strobe Precharge Time          | t <sub>RP</sub>    | 100      |       | 100      |       | 120      |       | ns    | -      |
| Row Address Strobe Pulse Width             | t <sub>RAS</sub>   | 120      | 10000 | 150      | 10000 | 200      | 10000 | ns    | -      |
| Column Address Strobe Pulse Width          | t <sub>CAS</sub>   | 60       | 10000 | 75       | 10000 | 100      | 10000 | ns    | -      |
| Row to Column Strobe Lead Time             | t <sub>RCD</sub>   | 25       | 60    | 30       | 75    | 35       | 100   | ns    | 13     |
| Row Address Setup Time                     | t <sub>ASR</sub>   | 0        |       | 0        |       | 0        |       | ns    | -      |
| Row Address Hold Time                      | t <sub>RAH</sub>   | 15       |       | 20       |       | 25       |       | ns    | -      |
| Column Address Setup Time                  | t <sub>ASC</sub>   | 0        |       | 0        |       | 0        |       | ns    | -      |
| Column Address Hold Time                   | t <sub>CAH</sub>   | 25       |       | 35       |       | 45       |       | ns    | -      |
| Column Address Hold Time Referenced to RAS | t <sub>AR</sub>    | 85       |       | 95       |       | 120      |       | ns    | 17     |
| Transition Time (Rise and Fall)            | t <sub>T</sub>     | 3        | 50    | 3        | 50    | 3        | 50    | ns    | 6      |
| Read Command Setup Time                    | t <sub>RCS</sub>   | 0        |       | 0        |       | 0        |       | ns    | -      |
| Read Command Hold Time                     | t <sub>RCH</sub>   | 0        |       | 0        |       | 0        |       | ns    | 14     |
| Read Command Hold Time Referenced to RAS   | t <sub>RRH</sub>   | 0        |       | 0        |       | 0        |       | ns    | 14     |
| Write Command Hold Time                    | t <sub>WCH</sub>   | 25       |       | 35       |       | 45       |       | ns    | -      |
| Write Command Hold Time Referenced to RAS  | t <sub>WCR</sub>   | 85       |       | 95       |       | 120      |       | ns    | 17     |
| Write Command Pulse Width                  | t <sub>WP</sub>    | 25       |       | 35       |       | 45       |       | ns    | -      |
| Write Command to Row Strobe Lead Time      | t <sub>RWL</sub>   | 40       |       | 45       |       | 55       |       | ns    | -      |
| Write Command to Column Strobe Lead Time   | t <sub>CWL</sub>   | 40       |       | 45       |       | 55       |       | ns    | -      |
| Data in Setup Time                         | t <sub>DS</sub>    | 0        |       | 0        |       | 0        |       | ns    | 15     |
| Data in Hold Time                          | t <sub>DH</sub>    | 25       |       | 35       |       | 45       |       | ns    | 15     |
| Data in Hold Time Referenced to RAS        | t <sub>DHR</sub>   | 85       |       | 95       |       | 120      |       | ns    | 17     |
| Column to Row Strobe Precharge Time        | t <sub>CRP</sub>   | -10      |       | -10      |       | -10      |       | ns    | -      |
| RAS Hold Time                              | t <sub>RSH</sub>   | 60       |       | 75       |       | 100      |       | ns    | -      |
| Refresh Period                             | t <sub>REFSH</sub> |          | 2.0   |          | 2.0   |          | 2.0   | ms    | -      |
| WRITE Command Setup Time                   | t <sub>WCS</sub>   | -10      |       | -10      |       | -10      |       | ns    | 16     |
| CAS to WRITE Delay                         | t <sub>CWD</sub>   | 40       |       | 45       |       | 55       |       | ns    | 16     |
| RAS to WRITE Delay                         | t <sub>RWD</sub>   | 100      |       | 120      |       | 155      |       | ns    | 16     |
| CAS Hold Time                              | t <sub>CSH</sub>   | 120      |       | 150      |       | 200      |       | ns    | -      |
| CAS Precharge Time (Page Mode Cycle Only)  | t <sub>CP</sub>    | 50       |       | 60       |       | 80       |       | ns    | -      |
| Page Mode Cycle Time                       | t <sub>PC</sub>    | 120      |       | 145      |       | 200      |       | ns    | -      |

8. The specifications for t<sub>RC</sub> (min), and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T<sub>A</sub> ≤ 70°C) is assured.
9. AC measurements t<sub>T</sub> = 5.0 ns.
10. Assumes that t<sub>RCD</sub> ≤ t<sub>RCD</sub> (max)
11. Assumes that t<sub>RCD</sub> ≥ t<sub>RCD</sub> (max)
12. Measured with a current load equivalent to 2 TTL (-200 μA, +4 mA) loads and 100 pF with the data output trip points set at V<sub>OH</sub> = 2.0 V and V<sub>OL</sub> = 0.8 V.
13. Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
14. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in random write cycles and to  $\overline{\text{WRITE}}$  leading edge in delayed write or read-modify-write cycles.
16. t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t<sub>WCS</sub> ≥ t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle, if t<sub>CWD</sub> ≥ t<sub>CWD</sub> (min) and t<sub>RWD</sub> ≥ t<sub>RWD</sub> (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t<sub>AR</sub> min ≤ t<sub>AR</sub> = t<sub>RCD</sub> + t<sub>CAH</sub>  
t<sub>DHR</sub> min ≤ t<sub>DHR</sub> = t<sub>RCD</sub> + t<sub>DH</sub>  
t<sub>WCR</sub> min ≤ t<sub>WCR</sub> = t<sub>RCD</sub> + t<sub>WCH</sub>
18. t<sub>off</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels

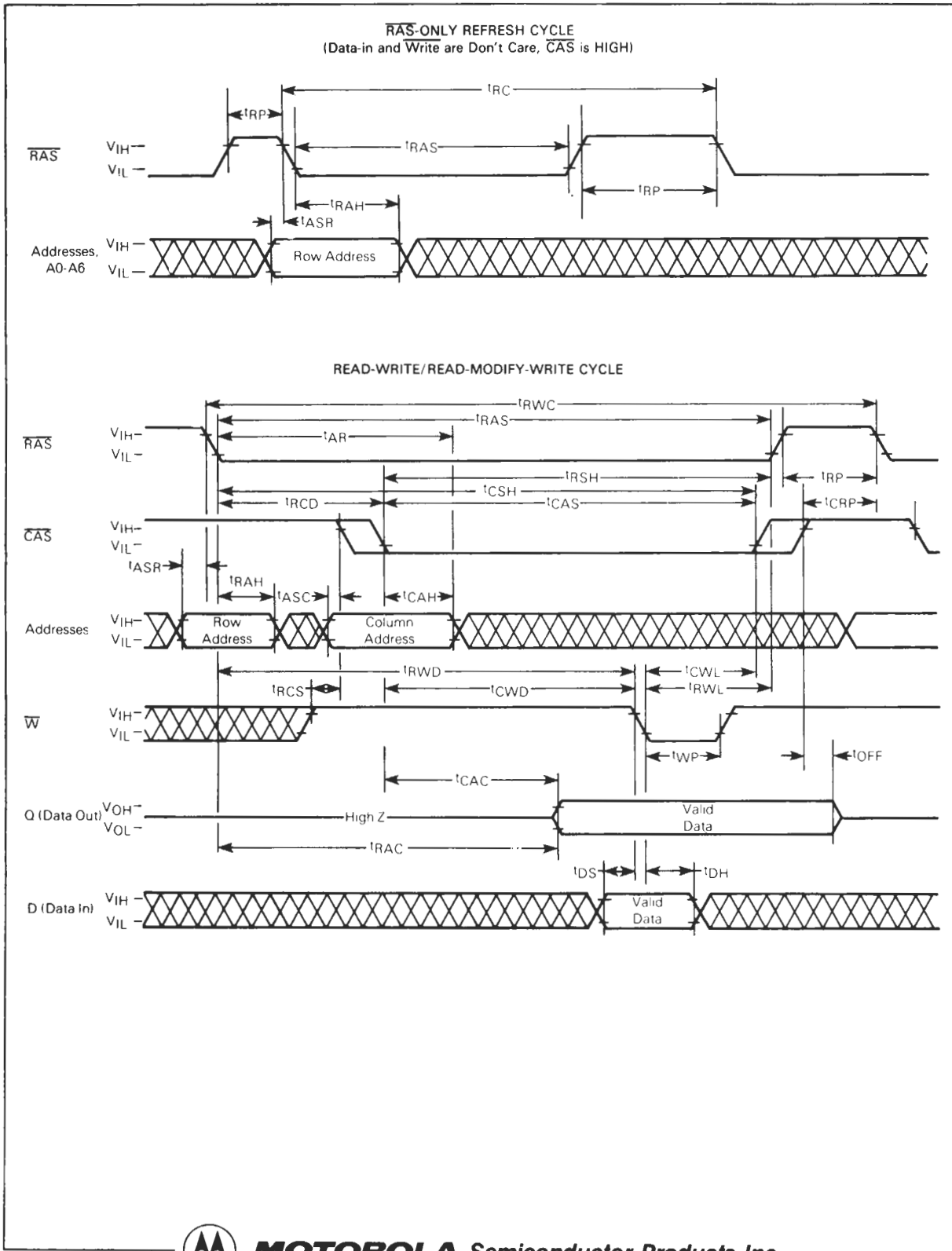




MCM6665A



MCM6665A



MCM6665A

TYPICAL CHARACTERISTICS

FIGURE 2 —  $\overline{RAS}$  ACCESS TIME versus SUPPLY VOLTAGE

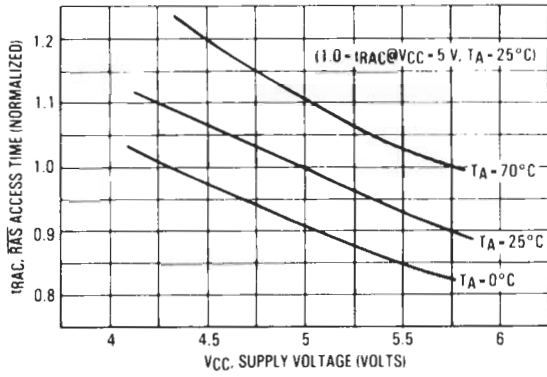


FIGURE 3 —  $\overline{CAS}$  ACCESS TIME versus SUPPLY VOLTAGE

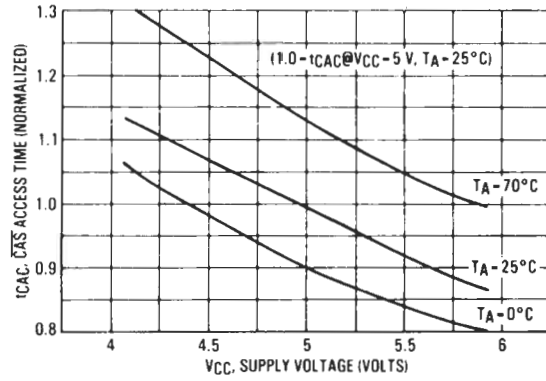


FIGURE 4 —  $\overline{RAS}$  ACCESS TIME versus AMBIENT TEMPERATURE

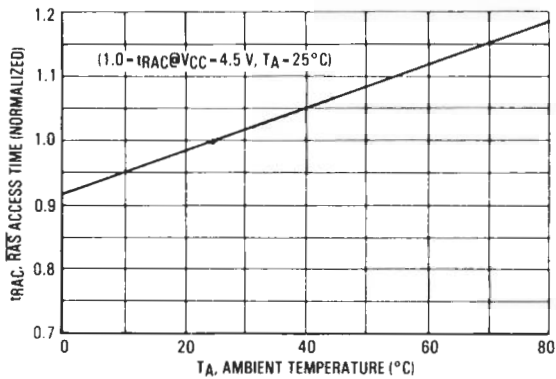


FIGURE 5 —  $\overline{CAS}$  ACCESS TIME versus AMBIENT TEMPERATURE

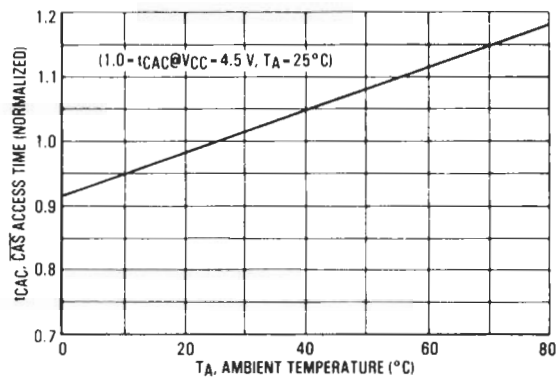


FIGURE 6 —  $\overline{RAS}$ ,  $\overline{W}$  INPUT LEVEL versus SUPPLY VOLTAGE

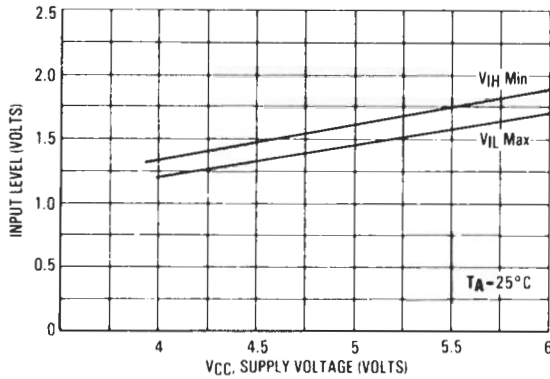
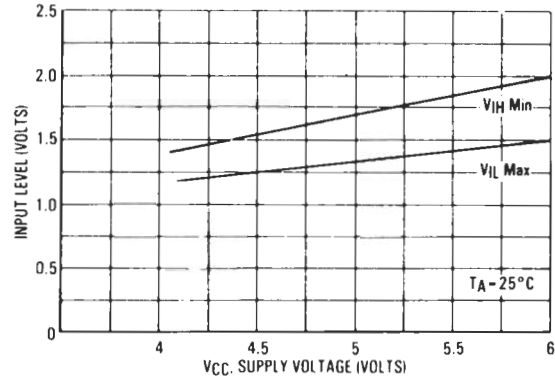


FIGURE 7 —  $\overline{CAS}$ ,  $\overline{W}$  INPUT LEVEL versus SUPPLY VOLTAGE





MCM6665A

TYPICAL CHARACTERISTICS (continued)

FIGURE 8 —  $I_{CC1}$  SUPPLY CURRENT versus CYCLE RATE

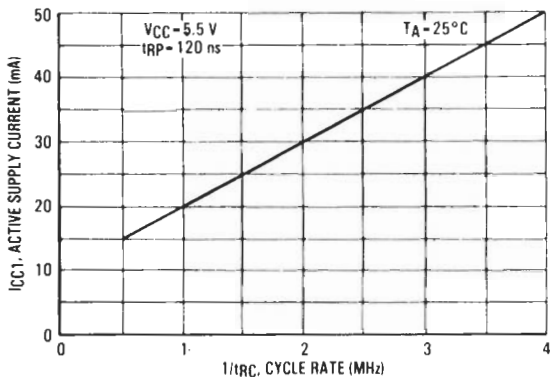


FIGURE 9 —  $I_{CC1}$  SUPPLY CURRENT versus SUPPLY VOLTAGE

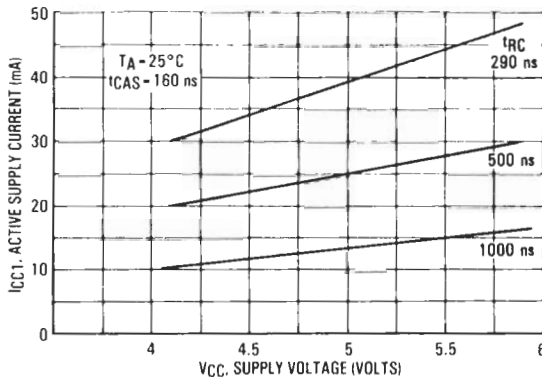


FIGURE 10 —  $I_{CC1}$  SUPPLY CURRENT versus SUPPLY VOLTAGE

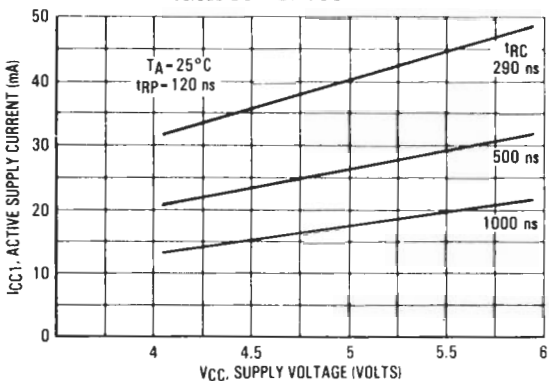


FIGURE 11 —  $I_{CC1}$  SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t<sub>RP</sub>)

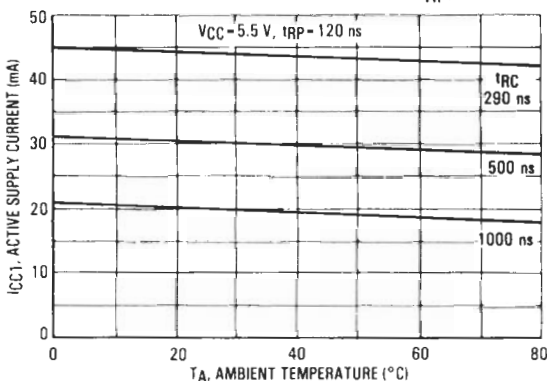


FIGURE 12 —  $I_{CC1}$  SUPPLY CURRENT versus AMBIENT TEMPERATURE (min RAS)

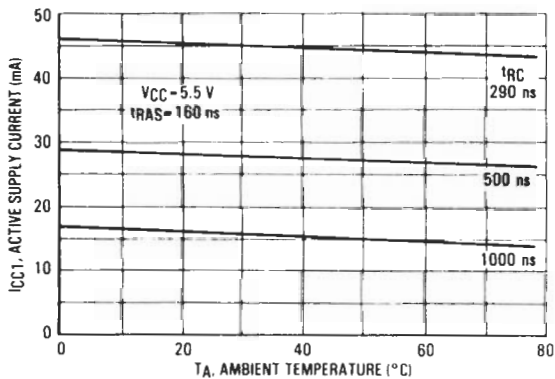
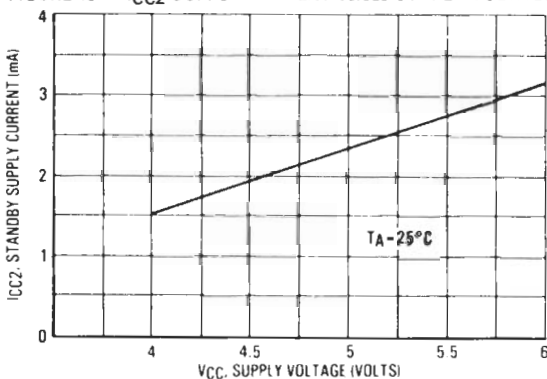


FIGURE 13 —  $I_{CC2}$  SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 —  $I_{CC2}$  STANDBY CURRENT versus AMBIENT TEMPERATURE

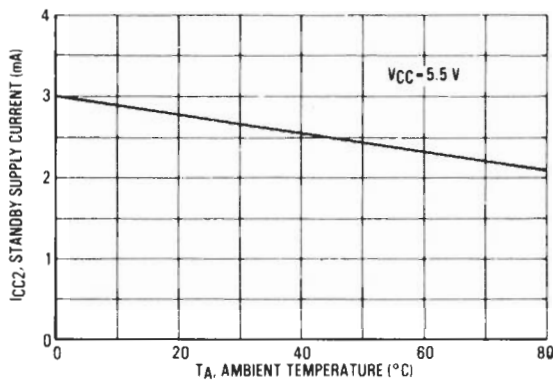


FIGURE 15 —  $I_{CC3}$  SUPPLY CURRENT versus CYCLE RATE

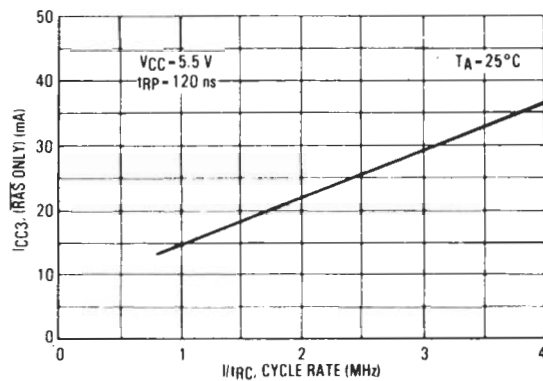


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

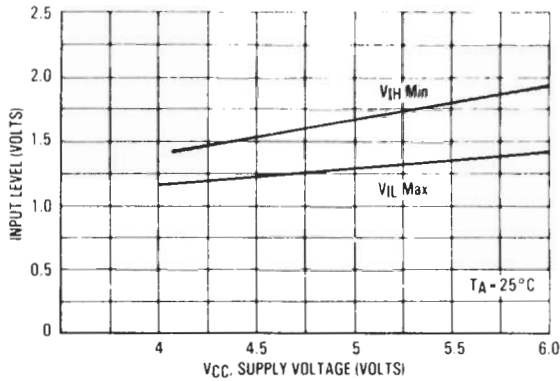
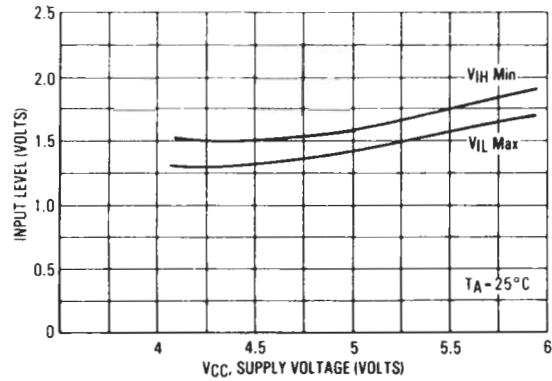


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm<sup>2</sup>/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1 × 10<sup>5</sup> to 6 × 10<sup>5</sup> (alpha/cm<sup>2</sup>hr) placed over un-

coated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

- 1) Cycle time: 1 microsecond for read, write and refresh cycles
- 2) Refresh Rate: 1 millisecond
- 3) Voltage: 5.0 V
- 4) Temperature: 30° C ± 2° C (ambient temperature inside enclosure)
- 5) Elevation: Approximately 620 feet above mean sea level
- 6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.



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FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

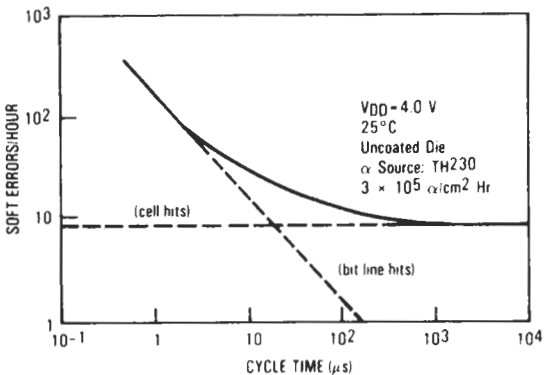
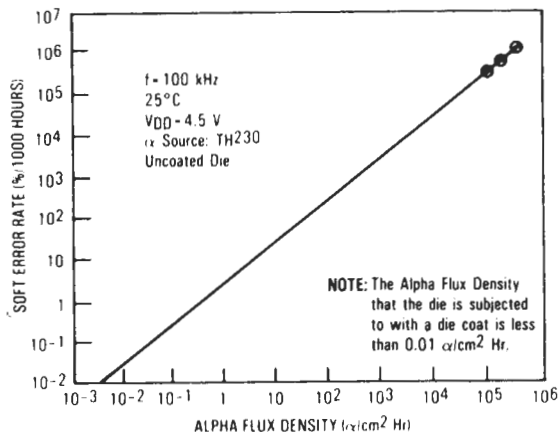


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 —  $\overline{\text{RAS}}/\overline{\text{CAS}}$  CYCLE

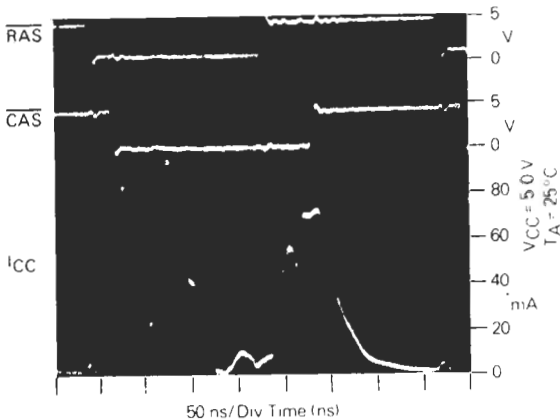


FIGURE 21 — LONG  $\overline{\text{RAS}}/\overline{\text{CAS}}$  CYCLE

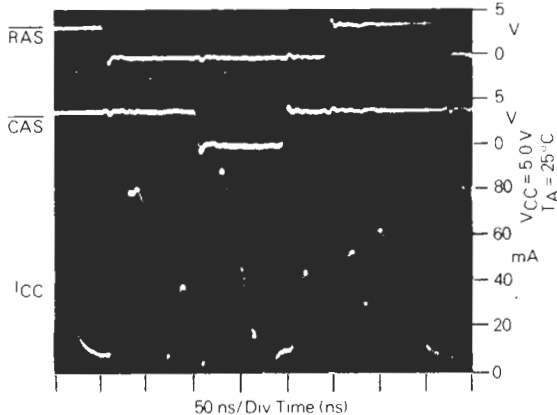


FIGURE 22 —  $\overline{\text{RAS}}$  ONLY CYCLE

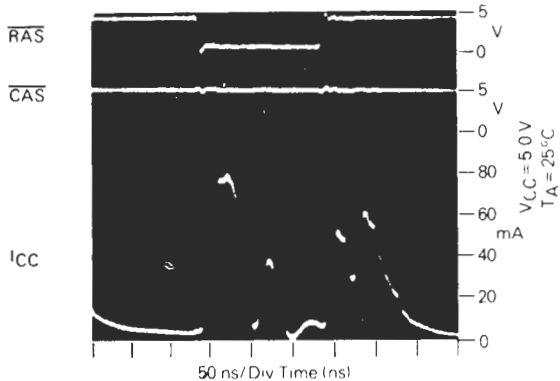
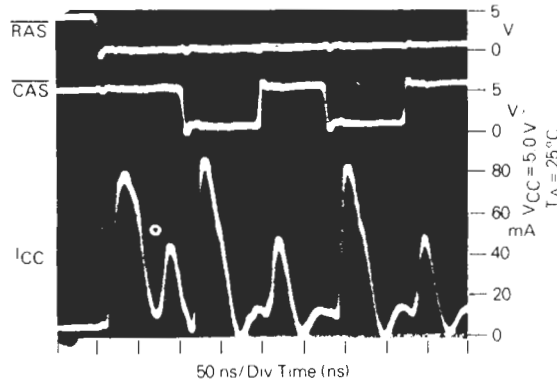
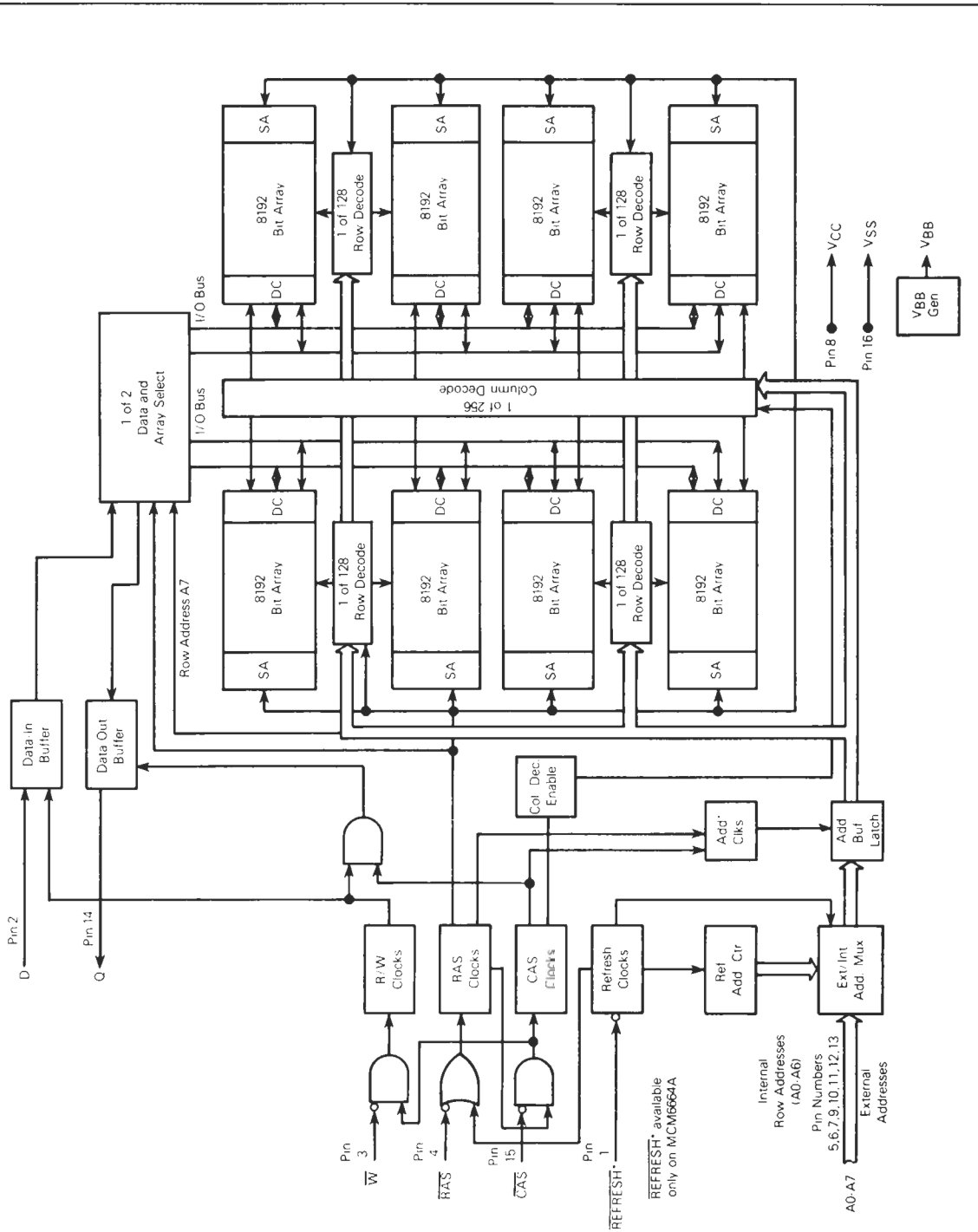


FIGURE 23 — PAGE MODE CYCLE



MCM6665A

FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM



## MCM6665A

## DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25, 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

## ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column

address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t<sub>RCD</sub>," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the  $\overline{\text{CAS}}$  clock, and the other is the  $\overline{\text{RAS}}$  only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the  $\overline{\text{RAS}}$  clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

## NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate it from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the  $\overline{\text{RAS}}$  clock transitioning from  $V_{IH}$  to the  $V_{IL}$  level. The  $\overline{\text{CAS}}$  clock must also make a transition from  $V_{IH}$  to the  $V_{IL}$  level at the specified t<sub>RCD</sub> timing limits when the column addresses are latched. Both the  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the  $\overline{\text{CAS}}$  clock must be active before or at

## CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP,  $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{CC}$

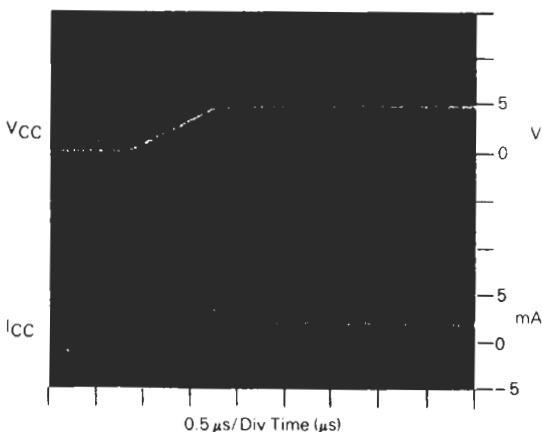
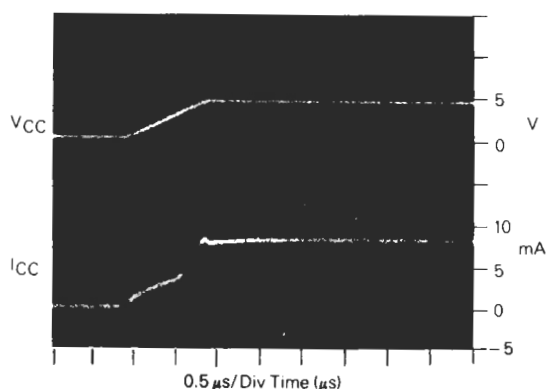


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP,  $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{SS}$



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the  $t_{RCD}$  maximum specification for an access (data valid) from the  $\overline{RAS}$  clock edge to be guaranteed ( $t_{RAC}$ ). If the  $t_{RCD}$  maximum condition is not met, the access ( $t_{CAC}$ ) from the  $\overline{CAS}$  clock active transition will determine read access time. The external  $\overline{CAS}$  signal is ignored until an internal  $\overline{RAS}$  signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the  $\overline{CAS}$  clock will allow the external  $\overline{CAS}$  signal to become active as soon as the row address hold time ( $t_{RAH}$ ) specification has been met and defines the  $t_{RCD}$  minimum specification. The time difference between  $t_{RCD}$  minimum and  $t_{RCD}$  maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the  $\overline{CAS}$  clock.

Once the clocks have become active, they must stay active for the minimum ( $t_{RAS}$ ) period for the  $\overline{RAS}$  clock and the minimum ( $t_{CAS}$ ) period for the  $\overline{CAS}$  clock. The  $\overline{RAS}$  clock must stay inactive for the minimum ( $t_{RP}$ ) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the  $\overline{CAS}$  clock is active; the output will switch to the three-state mode when the  $\overline{CAS}$  clock goes inactive. The  $\overline{CAS}$  clock can remain active for a maximum of 10 ns ( $t_{CRP}$ ) into the next cycle. To perform a read cycle, the write ( $\overline{W}$ ) input must be held at the  $V_{IH}$  level from the time the  $\overline{CAS}$  clock makes its active transition ( $t_{RCS}$ ) to the time when it transitions into the inactive ( $t_{RCH}$ ) mode.

#### WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ( $\overline{W}$ ) clock must go active ( $V_{IL}$  level) at or before the  $\overline{CAS}$  clock goes active at a minimum  $t_{WCS}$  time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the  $\overline{CAS}$  clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time ( $t_{CWL}$ ) and the row strobe to write lead time ( $t_{RWL}$ ). These define the minimum time that  $\overline{RAS}$  and  $\overline{CAS}$  clocks need to be active after the write operation has started ( $\overline{W}$  clock at  $V_{IL}$  level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the  $\overline{CAS}$  goes low which is beyond  $t_{WCS}$  minimum time. Thus the parameters  $t_{CWL}$  and  $t_{RWL}$  must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ( $\overline{W}$ ) clock can occur much later in time with respect to the active transition of the  $\overline{CAS}$  clock. This time could be as long as 10 microseconds — [ $t_{RWL} + t_{RP} + 2t_t$ ].

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ( $\overline{W}$ ) clock prevents the  $\overline{CAS}$  clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

#### READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ( $\overline{W}$ ) clock at the  $V_{IH}$  level until the read data occurs at the device access time ( $t_{RAC}$ ). At this time the write ( $\overline{W}$ ) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters ( $t_{RWD}$ ,  $t_{CWD}$ ) play an important role. A read-while-write cycle starts as a normal read cycle with the write ( $\overline{W}$ ) clock being asserted at minimum  $t_{RWD}$  or minimum  $t_{CWD}$  time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on  $t_{RWD}$  and  $t_{CWD}$  assures that data out does occur. In this case, the data in is set up with respect to write ( $\overline{W}$ ) clock active edge.

#### PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access ( $t_{CAC}$ ) is typically half the regular  $\overline{RAS}$  clock access ( $t_{RAC}$ ) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the  $\overline{RAS}$  clock active while cycling the  $\overline{CAS}$  clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one  $\overline{RAS}$  clock active operation. These are the refresh interval of the device ( $2 \text{ ms}/128 = 15.6 \text{ microseconds}$ ) and the maximum active time specification for the  $\overline{RAS}$  clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the  $\overline{RAS}$  clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the  $\overline{RAS}$  clock is reset.

The page cycle is always initiated with a row address being provided and latched by the  $\overline{RAS}$  clock, followed by the column address and  $\overline{CAS}$  clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter  $\overline{CAS}$  cycles ( $t_{PC}$ ). The  $\overline{CAS}$  cycle time ( $t_{PC}$ ) consists of the  $\overline{CAS}$  clock active time ( $t_{CAS}$ ), and  $\overline{CAS}$  clock precharge time ( $t_{CP}$ ) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

#### REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

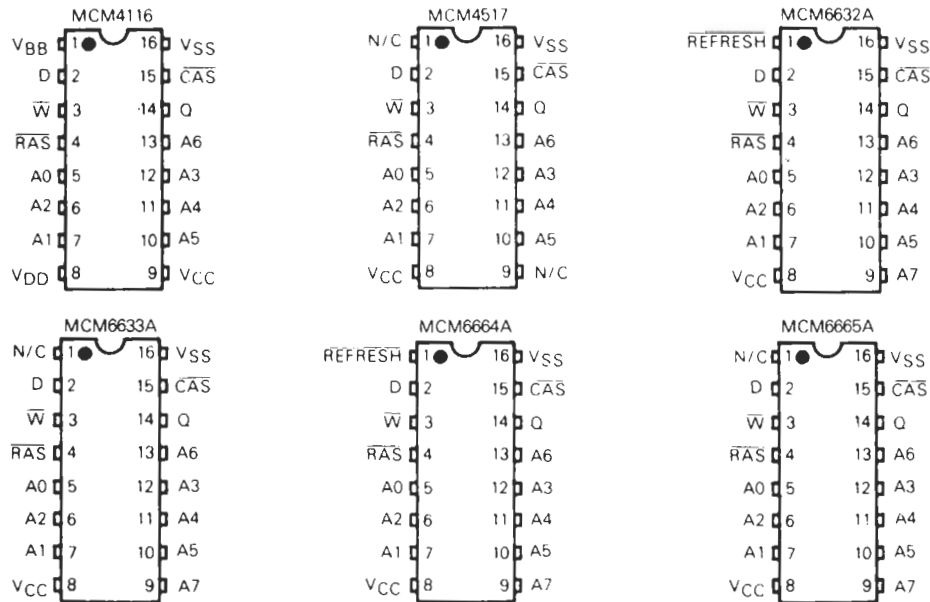


## MCM6665A

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

**RAS Only Refresh** — When the memory component is in standby the RAS only refresh scheme is employed. This refresh method performs a RAS only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the RAS clock, and the associated internal row locations are refreshed. As the heading implies, the CAS clock is not required and should be inactive or at a  $V_{IH}$  level to conserve power.

## PIN ASSIGNMENT COMPARISON



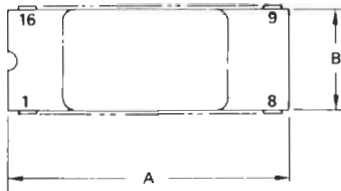
## PIN VARIATIONS

| PIN NUMBER | MCM4116         | MCM4517  | MCM6632A | MCM6663A | MCM6664A | MCM6665A |
|------------|-----------------|----------|----------|----------|----------|----------|
| 1          | $V_{BB}(-5 V)$  | N/C      | REFRESH  | N/C      | REFRESH  | N/C      |
| 8          | $V_{DD}(+12 V)$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| 9          | $V_{CC}(+5 V)$  | N/C      | A7       | A7       | A7       | A7       |



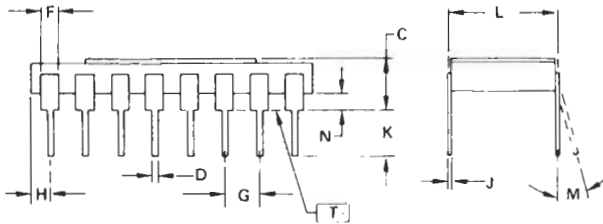
MCM6665A

PACKAGE DIMENSIONS



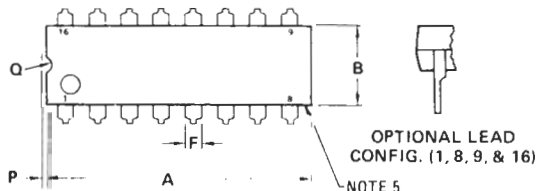
L SUFFIX  
CERAMIC PACKAGE  
CASE 690-13

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 20.07       | 20.57 | 0.790     | 0.810 |
| B   | 7.11        | 7.62  | 0.280     | 0.300 |
| C   | 2.67        | 4.19  | 0.105     | 0.165 |
| D   | 0.38        | 0.53  | 0.015     | 0.021 |
| F   | 0.76        | 1.52  | 0.030     | 0.060 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.76        | 1.78  | 0.030     | 0.070 |
| J   | 0.20        | 0.30  | 0.008     | 0.012 |
| K   | 3.18        | 5.08  | 0.125     | 0.200 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | -           | 10°   | -         | 10°   |
| N   | 0.38        | 1.52  | 0.015     | 0.060 |



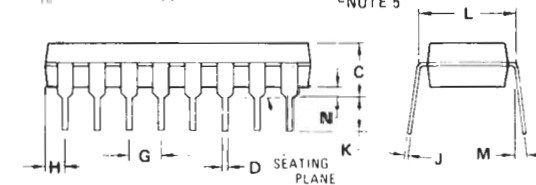
NOTES

1. A AND B ARE DATUMS.
2. T IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).  
 $\text{⌀ } \phi 0.25 (0.010) \text{ (M)} | T | A \text{ (M)} | B \text{ (M)}$
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



P SUFFIX  
PLASTIC PACKAGE  
CASE 648-05

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 18.80       | 21.34 | 0.740     | 0.840 |
| B   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 4.06        | 5.08  | 0.160     | 0.200 |
| D   | 0.38        | 0.53  | 0.015     | 0.021 |
| F   | 1.02        | 1.78  | 0.040     | 0.070 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.38        | 2.41  | 0.015     | 0.095 |
| J   | 0.20        | 0.38  | 0.008     | 0.015 |
| K   | 2.92        | 3.43  | 0.115     | 0.135 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | 0°          | 10°   | 0°        | 10°   |
| N   | 0.51        | 1.02  | 0.020     | 0.040 |



NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.



MOTOROLA Semiconductor Products Inc.









## 8085A/8085A-2

### SINGLE CHIP 8-BIT N-CANNEL MICROPROCESSORS

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3  $\mu$ s Instruction Cycle (8085A);  
0.8  $\mu$ s (8085A-2)**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)) while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

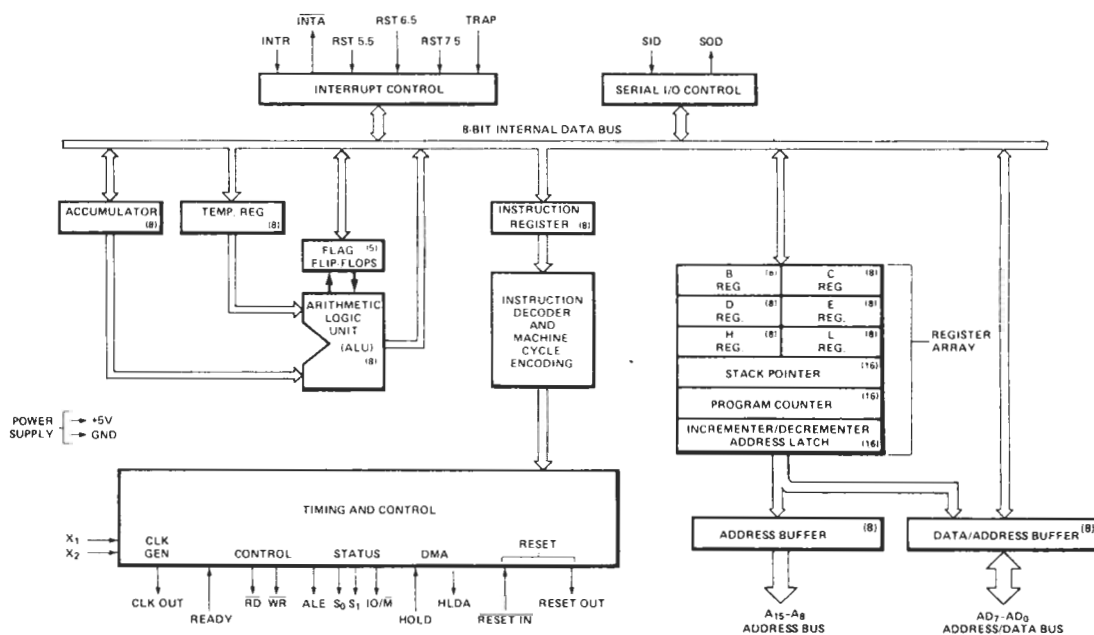


Figure 1. 8085A CPU Functional Block Diagram

8085A/8085A-2

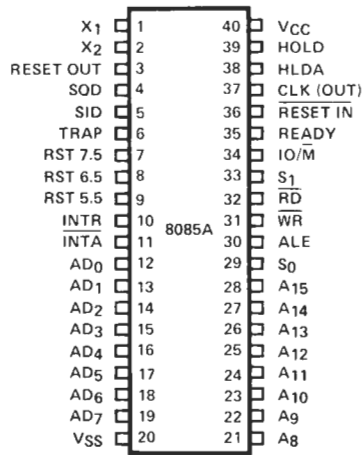


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

| Symbol  | Function  |                |                       |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
|---|---|----------------|-----------------------|----------------|--------|---|---|---|--------------|---|---|---|-------------|---|---|---|-----------|---|---|---|----------|---|---|---|--------------|---|---|---|-----------------------|---|---|---|------|---|---|---|------|---|---|---|-------|
| <b>A<sub>8</sub>-A<sub>15</sub></b><br>(Output, 3-state)  | Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.  |                |                       |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| <b>AD<sub>0-7</sub></b><br>(Input/Output, 3-state)        | Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.   |                |                       |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| <b>ALE</b><br>(Output)                                    | Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.   |                |                       |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| <b>S<sub>0</sub>, S<sub>1</sub>, and IO/M</b><br>(Output) | Machine cycle status:<br><table border="1"> <thead> <tr> <th>IO/M</th> <th>S<sub>1</sub></th> <th>S<sub>0</sub></th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Memory write</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Memory read</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>I/O write</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>I/O read</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Opcode fetch</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>*</td> <td>0</td> <td>0</td> <td>Halt</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Reset</td> </tr> </tbody> </table> <p>* = 3-state (high impedance)<br/>X = unspecified</p> | IO/M           | S <sub>1</sub>        | S <sub>0</sub> | Status | 0 | 0 | 1 | Memory write | 0 | 1 | 0 | Memory read | 1 | 0 | 1 | I/O write | 1 | 1 | 0 | I/O read | 0 | 1 | 1 | Opcode fetch | 1 | 1 | 1 | Interrupt Acknowledge | * | 0 | 0 | Halt | * | X | X | Hold | * | X | X | Reset |
| IO/M  | S <sub>1</sub>  | S <sub>0</sub> | Status                |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 0   | 0   | 1              | Memory write          |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 0   | 1   | 0              | Memory read           |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 1   | 0   | 1              | I/O write             |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 1   | 1   | 0              | I/O read              |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 0   | 1   | 1              | Opcode fetch          |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| 1   | 1   | 1              | Interrupt Acknowledge |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| *   | 0   | 0              | Halt                  |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| *   | X   | X              | Hold                  |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |
| *   | X   | X              | Reset                 |                |        |   |   |   |              |   |   |   |             |   |   |   |           |   |   |   |          |   |   |   |              |   |   |   |                       |   |   |   |      |   |   |   |      |   |   |   |       |

| Symbol                         | Function   |
|--------------------------------|--|
| <b>S<sub>1</sub></b>           | S <sub>1</sub> can be used as an advanced R/W status. IO/M, S <sub>0</sub> and S <sub>1</sub> become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.  |
| <b>RD</b><br>(Output, 3-state) | READ control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.  |
| <b>WR</b><br>(Output, 3-state) | WRITE control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.  |
| <b>READY</b><br>(Input)        | If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.  |
| <b>HOLD</b><br>(Input)         | HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated.  |
| <b>HLDA</b><br>(Output)        | HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.   |
| <b>INTR</b><br>(Input)         | INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted. |

## 8085A/8085A-2

## 8085A FUNCTIONAL PIN DESCRIPTION (Continued)

| <u>Symbol</u>  | <u>Function</u>  | <u>Symbol</u>                                  | <u>Function</u>  |
|--|--|--|--|
| <b>INTA</b><br>(Output)  | INTERRUPT ACKNOWLEDGE: Is used instead of $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.   |  | Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{RESET IN}$ is applied.   |
| <b>RST 5.5</b><br><b>RST 6.5</b><br><b>RST 7.5</b><br>(Inputs) | RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.<br><br>The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction. | <b>RESET OUT</b><br>(Output)                   | Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.  |
| <b>TRAP</b><br>(Input)   | Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)  | <b>X<sub>1</sub>, X<sub>2</sub></b><br>(Input) | X <sub>1</sub> and X <sub>2</sub> are connected to a crystal, LC, or RC network to drive the internal clock generator. X <sub>1</sub> can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency. |
| <b>RESET IN</b><br>(Input)                                     | Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET IN}$ is a  | <b>CLK</b><br>(Output)                         | Clock Output for use as a system clock. The period of CLK is twice the X <sub>1</sub> , X <sub>2</sub> input period.   |
|  |  | <b>SID</b><br>(Input)                          | Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.   |
|  |  | <b>SOD</b><br>(Output)                         | Serial output data line. The output SOD is set or reset as specified by the SIM instruction.   |
|  |  | <b>V<sub>CC</sub></b>                          | +5 volt supply.  |
|  |  | <b>V<sub>SS</sub></b>                          | Ground Reference.  |

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

| Name    | Priority | Address Branched To (1)<br>When Interrupt Occurs | Type Trigger                              |
|---------|----------|--|---|
| TRAP    | 1        | 24H  | Rising edge AND high level until sampled. |
| RST 7.5 | 2        | 3CH  | Rising edge (latched).                    |
| RST 6.5 | 3        | 34H  | High level until sampled.                 |
| RST 5.5 | 4        | 2CH  | High level until sampled.                 |
| INTR    | 5        | See Note (2).                                    | High level until sampled.                 |

## NOTES:

- (1) The processor pushes the PC on the stack before branching to the indicated address.  
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



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**DRIVING THE X<sub>1</sub> AND X<sub>2</sub> INPUTS**

You may drive the clock inputs of the 8085A or 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock). If a crystal is used, it must have the following characteristics:

- Parallel resonance at twice the clock frequency desired
- C<sub>L</sub> (load capacitance) ≤ 30 pF
- C<sub>S</sub> (shunt capacitance) ≤ 7 pF
- R<sub>S</sub> (equivalent shunt resistance) ≤ 75 Ohms
- Drive level: 10 mW
- Frequency tolerance: ±.005% (suggested)

Note the use of the 20pF capacitor between X<sub>2</sub> and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085A, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

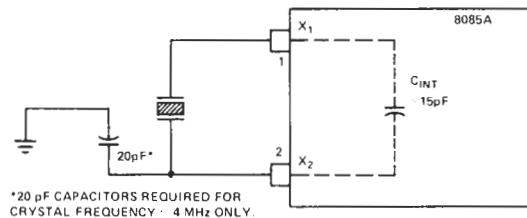
$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C<sub>ext</sub> that is at least twice that of C<sub>int</sub>, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

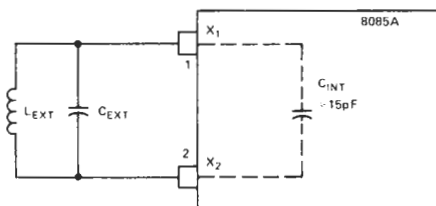
Figure 4 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4 V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X<sub>1</sub> and leave X<sub>2</sub> open-circuited (Figure 4D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X<sub>1</sub> and X<sub>2</sub> with a push-pull source (Figure 4E). To prevent self-oscillation of the 8085A, be sure that X<sub>2</sub> is not coupled back to X<sub>1</sub> through the driving circuit.

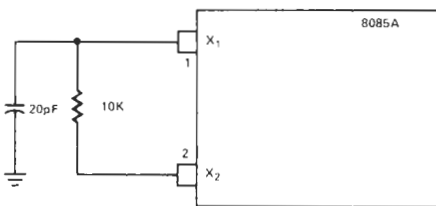


\*20 pF CAPACITORS REQUIRED FOR CRYSTAL FREQUENCY: 4 MHz ONLY.

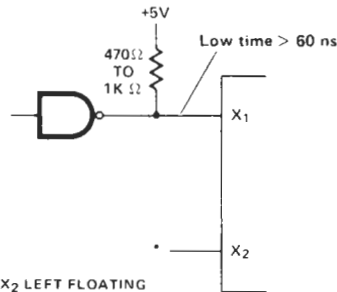
**A. Quartz Crystal Clock Driver**



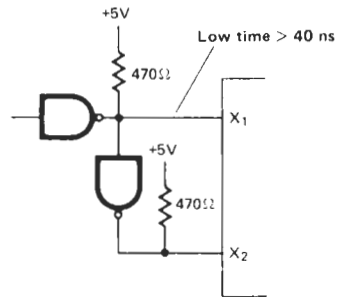
**B. LC Tuned Circuit Clock Driver**



**C. RC Circuit Clock Driver**



**D. 1-6 MHz Input Frequency External Clock Driver Circuit**



**E. 1-10 MHz Input Frequency External Clock Driver Circuit**

**Figure 4. Clock Driver Circuits**







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**BASIC SYSTEM TIMING**

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/M, S<sub>1</sub>, S<sub>0</sub>) and the three control signals (RD, WR, and INTA). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T<sub>1</sub> state, at the outset of each machine cycle. Control lines RD and WR become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OP CODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

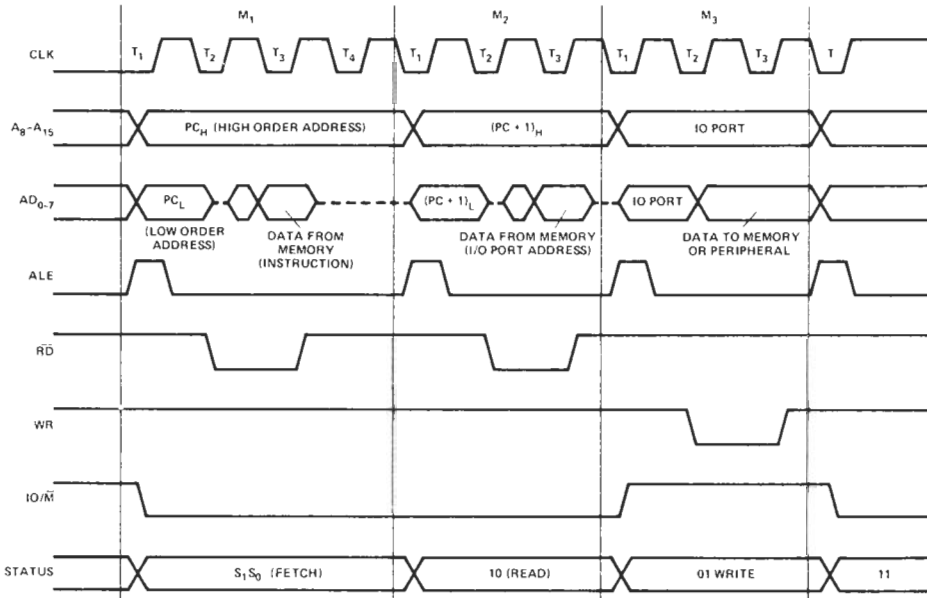
**TABLE 2. 8085A MACHINE CYCLE CHART**

| MACHINE CYCLE                               | STATUS |                |                | CONTROL |    |      |
|---|--------|----------------|----------------|---------|----|------|
|   | IO/M   | S <sub>1</sub> | S <sub>0</sub> | RD      | WR | INTA |
| OPCODE FETCH (OF)                           | 0      | 1              | 1              | 0       | 1  | 1    |
| MEMORY READ (MR)                            | 0      | 1              | 0              | 0       | 1  | 1    |
| MEMORY WRITE (MW)                           | 0      | 0              | 1              | 1       | 0  | 1    |
| I/O READ (IOR)                              | 1      | 1              | 0              | 0       | 1  | 1    |
| I/O WRITE (IOW)                             | 1      | 0              | 1              | 1       | 0  | 1    |
| ACKNOWLEDGE OF INTR (INA)                   | 1      | 1              | 1              | 1       | 1  | 0    |
| BUS IDLE (BI): DAD, ACK. OF RST, TRAP, HALT | 0      | 1              | 0              | 1       | 1  | 1    |
|   | 1      | 1              | 1              | 1       | 1  | 1    |
|   | TS     | 0              | 0              | TS      | TS | 1    |

**TABLE 3. 8085A MACHINE STATE CHART**

| Machine State      | Status & Buses                |      |                                 |                                  | Control |      |     |
|--------------------|-------------------------------|------|---------------------------------|----------------------------------|---------|------|-----|
|                    | S <sub>1</sub> S <sub>0</sub> | IO/M | A <sub>8</sub> -A <sub>15</sub> | AD <sub>0</sub> -AD <sub>7</sub> | RD,WR   | INTA | ALE |
| T <sub>1</sub>     | X                             | X    | X                               | X                                | 1       | 1    | 1*  |
| T <sub>2</sub>     | X                             | X    | X                               | X                                | X       | X    | 0   |
| T <sub>WAIT</sub>  | X                             | X    | X                               | X                                | X       | X    | 0   |
| T <sub>3</sub>     | X                             | X    | X                               | X                                | X       | X    | 0   |
| T <sub>4</sub>     | 1                             | 0'   | X                               | TS                               | 1       | 1    | 0   |
| T <sub>5</sub>     | 1                             | 0'   | X                               | TS                               | 1       | 1    | 0   |
| T <sub>6</sub>     | 1                             | 0'   | X                               | TS                               | 1       | 1    | 0   |
| T <sub>RESET</sub> | X                             | TS   | TS                              | TS                               | TS      | 1    | 0   |
| T <sub>HALT</sub>  | 0                             | TS   | TS                              | TS                               | TS      | 1    | 0   |
| T <sub>HOLD</sub>  | X                             | TS   | TS                              | TS                               | TS      | 1    | 0   |

0 - Logic "0"  
 1 - Logic "1"  
 TS - High Impedance  
 X - Unspecified  
 \* ALE not generated during 2nd and 3rd machine cycles of DAD instruction  
 † IO/M = 1 during T<sub>4</sub>-T<sub>6</sub> of INA machine cycle



**Figure 9. 8085A Basic System Timing**

## 8085A/8085A-2

TABLE 4. ABSOLUTE MAXIMUM RATINGS\*

|  |                 |
|--|-----------------|
| Ambient Temperature Under Bias . . . . .               | 0°C to 70°C     |
| Storage Temperature . . . . .                          | -65°C to +150°C |
| Voltage on Any Pin<br>With Respect to Ground . . . . . | -0.5V to +7V    |
| Power Dissipation . . . . .                            | 1.5 Watt        |

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 5. D.C. CHARACTERISTICS

( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$ ;  $V_{SS} = 0\text{V}$ ; unless otherwise specified)

| Symbol    | Parameter               | Min. | Max.           | Units         | Test Conditions                         |
|-----------|-------------------------|------|----------------|---------------|---|
| $V_{IL}$  | Input Low Voltage       | -0.5 | +0.8           | V             |   |
| $V_{IH}$  | Input High Voltage      | 2.0  | $V_{CC} + 0.5$ | V             |   |
| $V_{OL}$  | Output Low Voltage      |      | 0.45           | V             | $I_{OL} = 2\text{mA}$                   |
| $V_{OH}$  | Output High Voltage     | 2.4  |                | V             | $I_{OH} = -400\mu\text{A}$              |
| $I_{CC}$  | Power Supply Current    |      | 170            | mA            |   |
| $I_{IL}$  | Input Leakage           |      | $\pm 10$       | $\mu\text{A}$ | $V_{in} = V_{CC}$                       |
| $I_{LO}$  | Output Leakage          |      | $\pm 10$       | $\mu\text{A}$ | $0.45\text{V} \leq V_{out} \leq V_{CC}$ |
| $V_{ILR}$ | Input Low Level, RESET  | -0.5 | +0.8           | V             |   |
| $V_{IHR}$ | Input High Level, RESET | 2.4  | $V_{CC} + 0.5$ | V             |   |
| $V_{HY}$  | Hysteresis, RESET       | 0.25 |                | V             |   |

**TABLE 6. A.C. CHARACTERISTICS**  
 $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$ ;  $V_{SS} = 0\text{V}$

| Symbol     | Parameter   | 8085A <sup>[2]</sup> |      | 8085A-2 <sup>[2]</sup><br>(Preliminary) |      | Units |
|------------|---|----------------------|------|---|------|-------|
|            |   | Min.                 | Max. | Min.                                    | Max. |       |
| $t_{CYC}$  | CLK Cycle Period  | 320                  | 2000 | 200                                     | 2000 | ns    |
| $t_1$      | CLK Low Time (Standard CLK Loading)   | 80                   |      | 40                                      |      | ns    |
| $t_2$      | CLK High Time (Standard CLK Loading)  | 120                  |      | 70                                      |      | ns    |
| $t_r, t_f$ | CLK Rise and Fall Time  |                      | 30   |   | 30   | ns    |
| $t_{XKR}$  | $X_1$ Rising to CLK Rising  | 30                   | 120  | 30                                      | 100  | ns    |
| $t_{XKF}$  | $X_1$ Rising to CLK Falling   | 30                   | 150  | 30                                      | 110  | ns    |
| $t_{AC}$   | $A_{8-15}$ Valid to Leading Edge of Control <sup>[1]</sup>  | 270                  |      | 115                                     |      | ns    |
| $t_{ACL}$  | $A_{0-7}$ Valid to Leading Edge of Control  | 240                  |      | 115                                     |      | ns    |
| $t_{AD}$   | $A_{0-15}$ Valid to Valid Data In   |                      | 575  |   | 350  | ns    |
| $t_{AFR}$  | Address Float After Leading Edge of $\overline{\text{READ}}$ ( $\overline{\text{INTA}}$ )           |                      | 0    |   | 0    | ns    |
| $t_{AL}$   | $A_{8-15}$ Valid Before Trailing Edge of ALE <sup>[1]</sup>   | 115                  |      | 50                                      |      | ns    |
| $t_{ALL}$  | $A_{0-7}$ Valid Before Trailing Edge of ALE   | 90                   |      | 50                                      |      | ns    |
| $t_{ARY}$  | READY Valid from Address Valid  |                      | 220  |   | 100  | ns    |
| $t_{CA}$   | Address ( $A_{8-15}$ ) Valid After Control  | 120                  |      | 60                                      |      | ns    |
| $t_{CC}$   | Width of Control Low ( $\overline{\text{RD}}$ , $\overline{\text{WR}}$ , $\overline{\text{INTA}}$ ) |                      |      |   |      |       |
| $t_{CL}$   | Trailing Edge of Control to Leading Edge of ALE   | 400                  |      | 230                                     |      | ns    |
| $t_{CL}$   | Trailing Edge of Control to Leading Edge of ALE   | 50                   |      | 25                                      |      | ns    |
| $t_{DW}$   | Data Valid to Trailing Edge of $\overline{\text{WRITE}}$  | 420                  |      | 230                                     |      | ns    |
| $t_{HABE}$ | HLDA to Bus Enable  |                      | 210  |   | 150  | ns    |
| $t_{HABF}$ | Bus Float After HLDA  |                      | 210  |   | 150  | ns    |
| $t_{HACK}$ | HLDA Valid to Trailing Edge of CLK  | 110                  |      | 40                                      |      | ns    |
| $t_{HDH}$  | HOLD Hold Time  | 0                    |      | 0                                       |      | ns    |
| $t_{HDS}$  | HOLD Setup Time to Trailing Edge of CLK   | 170                  |      | 120                                     |      | ns    |
| $t_{INH}$  | INTR Hold Time  | 0                    |      | 0                                       |      | ns    |
| $t_{INS}$  | INTR, RST, and TRAP Setup Time to Falling Edge of CLK   | 160                  |      | 150                                     |      | ns    |
| $t_{LA}$   | Address Hold Time After ALE   | 100                  |      | 50                                      |      | ns    |
| $t_{LC}$   | Trailing Edge of ALE to Leading Edge of Control   | 130                  |      | 60                                      |      | ns    |
| $t_{LCK}$  | ALE Low During CLK High   | 100                  |      | 50                                      |      | ns    |
| $t_{LDR}$  | ALE to Valid Data During Read   |                      | 460  |   | 270  | ns    |
| $t_{LDW}$  | ALE to Valid Data During Write  |                      | 200  |   | 120  | ns    |
| $t_{LL}$   | ALE Width   | 140                  |      | 80                                      |      | ns    |
| $t_{LRY}$  | ALE to READY Stable   |                      | 110  |   | 30   | ns    |

**8085A/8085A-2**

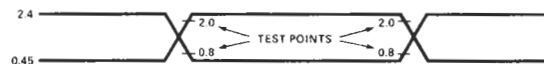
Table 6. A.C. Characteristics (Cont.)

| Symbol           | Parameter   | 8085A <sup>[2]</sup> |      | 8085A-2 <sup>[2]</sup><br>(Preliminary) |      | Units |
|------------------|---|----------------------|------|---|------|-------|
|                  |   | Min.                 | Max. | Min.                                    | Max. |       |
| t <sub>RAE</sub> | Trailing Edge of $\overline{\text{READ}}$ to Re-Enabling of Address                   | 150                  |      | 90                                      |      | ns    |
| t <sub>RD</sub>  | $\overline{\text{READ}}$ (or $\overline{\text{INTA}}$ ) to Valid Data                 |                      | 300  |   | 150  | ns    |
| t <sub>RV</sub>  | Control Trailing Edge to Leading Edge of Next Control                                 | 400                  |      | 220                                     |      | ns    |
| t <sub>RDH</sub> | Data Hold Time After $\overline{\text{READ}}$ $\overline{\text{INTA}}$ <sup>[7]</sup> | 0                    |      | 0                                       |      | ns    |
| t <sub>RYH</sub> | READY Hold Time   | 0                    |      | 0                                       |      | ns    |
| t <sub>RYS</sub> | READY Setup Time to Leading Edge of CLK   | 110                  |      | 100                                     |      | ns    |
| t <sub>WD</sub>  | Data Valid After Trailing Edge of $\overline{\text{WRITE}}$                           | 100                  |      | 60                                      |      | ns    |
| t <sub>WDL</sub> | LEADING Edge of WRITE to Data Valid   |                      | 40   |   | 20   | ns    |

## Notes:

1. A<sub>8</sub>-A<sub>15</sub> address Specs apply to IO/ $\overline{\text{M}}$ . S<sub>0</sub> and S<sub>1</sub> except A<sub>8</sub>-A<sub>15</sub> are undefined during T<sub>4</sub>-T<sub>6</sub> of OF cycle whereas IO/ $\overline{\text{M}}$ , S<sub>0</sub>, and S<sub>1</sub> are stable.
2. Test conditions: t<sub>CYC</sub> = 320 ns (8085A)/200 ns (8085A-2); C<sub>L</sub> = 150 pF.
3. For all output timing where C<sub>L</sub> = 150 pF use the following correction factors:  
25 pF < C<sub>L</sub> < 150 pF: -0.10 ns/pF  
150 pF < C<sub>L</sub> < 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage V<sub>L</sub> = 0.8V, V<sub>H</sub> = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t<sub>CYC</sub> use Table 7
7. Data hold time is guaranteed under all loading conditions.

## Input Waveform for A.C. Tests:



8085A/8085A-2

TABLE 7. BUS TIMING SPECIFICATION AS A  $T_{CYC}$  DEPENDENT

| 8085A      |   |                     |     | 8085A-2 (Preliminary) |   |                     |     |
|------------|---|---------------------|-----|-----------------------|---|---------------------|-----|
| $t_{AL}$   | — | $(1/2) T - 45$      | MIN | $t_{AL}$              | — | $(1/2) T - 50$      | MIN |
| $t_{LA}$   | — | $(1/2) T - 60$      | MIN | $t_{LA}$              | — | $(1/2) T - 50$      | MIN |
| $t_{LL}$   | — | $(1/2) T - 20$      | MIN | $t_{LL}$              | — | $(1/2) T - 20$      | MIN |
| $t_{LCK}$  | — | $(1/2) T - 60$      | MIN | $t_{LCK}$             | — | $(1/2) T - 50$      | MIN |
| $t_{LC}$   | — | $(1/2) T - 30$      | MIN | $t_{LC}$              | — | $(1/2) T - 40$      | MIN |
| $t_{AD}$   | — | $(5/2 + N) T - 225$ | MAX | $t_{AD}$              | — | $(5/2 + N) T - 150$ | MAX |
| $t_{RD}$   | — | $(3/2 + N) T - 180$ | MAX | $t_{RD}$              | — | $(3/2 + N) T - 150$ | MAX |
| $t_{RAE}$  | — | $(1/2) T - 10$      | MIN | $t_{RAE}$             | — | $(1/2) T - 10$      | MIN |
| $t_{CA}$   | — | $(1/2) T - 40$      | MIN | $t_{CA}$              | — | $(1/2) T - 40$      | MIN |
| $t_{DW}$   | — | $(3/2 + N) T - 60$  | MIN | $t_{DW}$              | — | $(3/2 + N) T - 70$  | MIN |
| $t_{WD}$   | — | $(1/2) T - 60$      | MIN | $t_{WD}$              | — | $(1/2) T - 40$      | MIN |
| $t_{CC}$   | — | $(3/2 + N) T - 80$  | MIN | $t_{CC}$              | — | $(3/2 + N) T - 70$  | MIN |
| $t_{CL}$   | — | $(1/2) T - 110$     | MIN | $t_{CL}$              | — | $(1/2) T - 75$      | MIN |
| $t_{ARY}$  | — | $(3/2) T - 260$     | MAX | $t_{ARY}$             | — | $(3/2) T - 200$     | MAX |
| $t_{HACK}$ | — | $(1/2) T - 50$      | MIN | $t_{HACK}$            | — | $(1/2) T - 60$      | MIN |
| $t_{HABF}$ | — | $(1/2) T + 50$      | MAX | $t_{HABF}$            | — | $(1/2) T + 50$      | MAX |
| $t_{HABE}$ | — | $(1/2) T + 50$      | MAX | $t_{HABE}$            | — | $(1/2) T + 50$      | MAX |
| $t_{AC}$   | — | $(2/2) T - 50$      | MIN | $t_{AC}$              | — | $(2/2) T - 85$      | MIN |
| $t_1$      | — | $(1/2) T - 80$      | MIN | $t_1$                 | — | $(1/2) T - 60$      | MIN |
| $t_2$      | — | $(1/2) T - 40$      | MIN | $t_2$                 | — | $(1/2) T - 30$      | MIN |
| $t_{RV}$   | — | $(3/2) T - 80$      | MIN | $t_{RV}$              | — | $(3/2) T - 80$      | MIN |
| $t_{LDR}$  | — | $(4/2) T - 180$     | MAX | $t_{LDR}$             | — | $(4/2) T - 130$     | MAX |

NOTE: N is equal to the total WAIT states.  
 $T = t_{CYC}$ .

NOTE: N is equal to the total WAIT states.  
 $T = t_{CYC}$ .

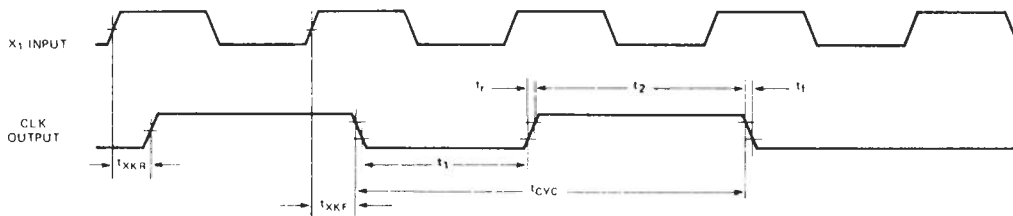
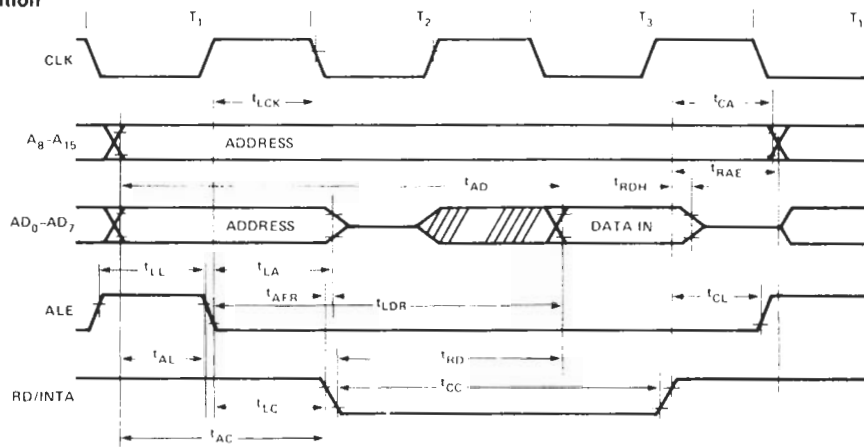


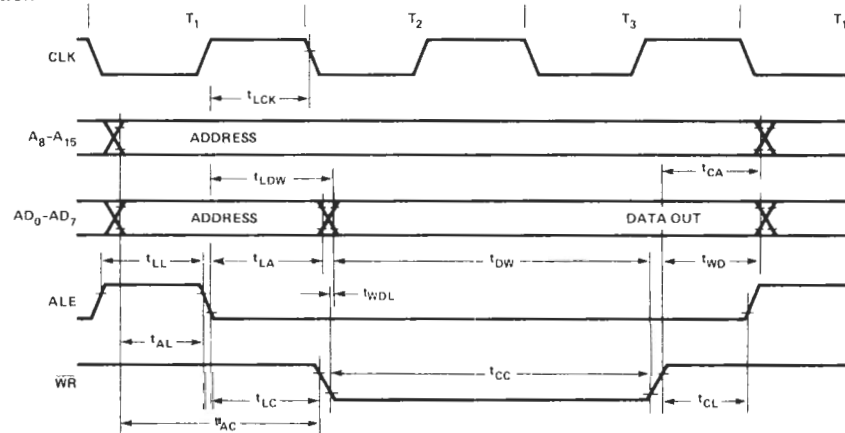
Figure 10. Clock Timing Waveform

8085A/8085A-2

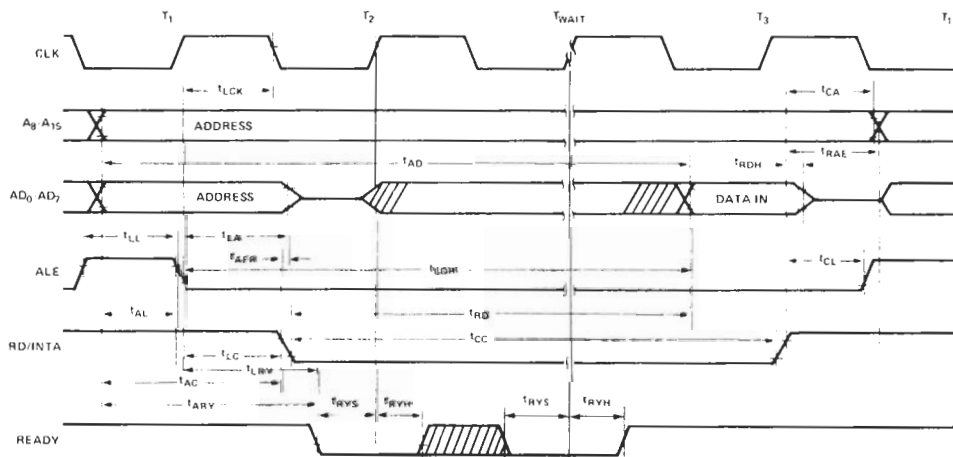
Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.



NOTE 1. READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

Figure 11. 8085A Bus Timing, With and Without Wait

8085A/8085A-2

Hold Operation

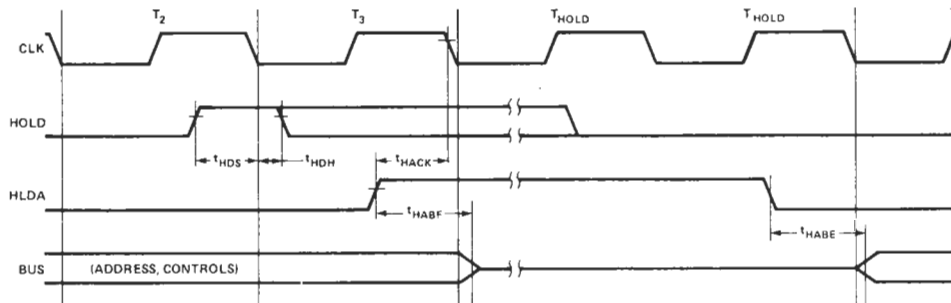


Figure 12. 8085A Hold Timing.

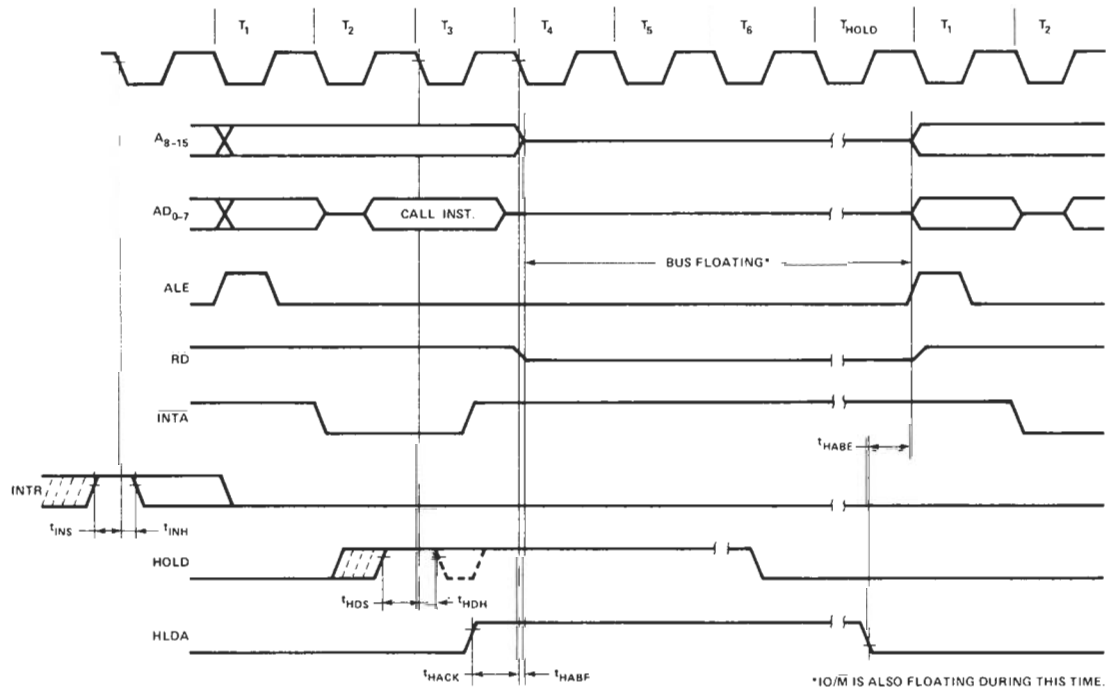


Figure 13. 8085A Interrupt and Hold Timing



## 8085A/8085A-2

## 8085A INSTRUCTION SET SUMMARY BY FUNCTIONAL GROUPING

Table 6-1

| Mnemonic                     | Description                           | Instruction Code (1) |                |                |                |                |                |                |                | Page | Mnemonic                       | Description                             | Instruction Code (1) |                |                |                |                |                |                |                | Page |
|------------------------------|---------------------------------------|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------|--------------------------------|---|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------|
|                              |                                       | D <sub>7</sub>       | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |      |                                |   | D <sub>7</sub>       | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |      |
| <b>MOVE, LOAD, AND STORE</b> |                                       |                      |                |                |                |                |                |                |                |      |                                |   |                      |                |                |                |                |                |                |                |      |
| MOV r1 r2                    | Move register to register             | 0                    | 1              | 0              | 0              | 0              | S              | S              | S              | 5.4  | CZ                             | Call on zero                            | 1                    | 1              | 0              | 0              | 1              | 1              | 0              | 0              | 5.14 |
| MOV M,r                      | Move register to memory               | 0                    | 1              | 1              | 1              | 0              | S              | S              | S              | 5.4  | CNZ                            | Call on no zero                         | 1                    | 1              | 0              | 0              | 0              | 1              | 0              | 0              | 5.14 |
| MOV r,M                      | Move memory to register               | 0                    | 1              | 0              | 0              | 0              | 1              | 1              | 0              | 5.4  | CP                             | Call on positive                        | 1                    | 1              | 1              | 1              | 0              | 1              | 0              | 0              | 5.14 |
| MVI r                        | Move immediate register               | 0                    | 0              | 0              | 0              | 0              | 1              | 1              | 0              | 5.4  | CM                             | Call on minus                           | 1                    | 1              | 1              | 1              | 1              | 1              | 0              | 0              | 5.14 |
| MVI M                        | Move immediate memory                 | 0                    | 0              | 1              | 1              | 0              | 1              | 1              | 0              | 5.4  | CPE                            | Call on parity even                     | 1                    | 1              | 1              | 0              | 1              | 1              | 0              | 0              | 5.14 |
| LXI B                        | Load immediate register<br>Pair B & C | 0                    | 0              | 0              | 0              | 0              | 0              | 0              | 1              | 5.5  | CPO                            | Call on parity odd                      | 1                    | 1              | 1              | 0              | 0              | 1              | 0              | 0              | 5.14 |
| LXI D                        | Load immediate register<br>Pair D & E | 0                    | 0              | 0              | 1              | 0              | 0              | 0              | 1              | 5.5  | <b>RETURN</b>                  |   |                      |                |                |                |                |                |                |                |      |
| LXI H                        | Load immediate register<br>Pair H & L | 0                    | 0              | 1              | 0              | 0              | 0              | 0              | 1              | 5.5  | RET                            | Return                                  | 1                    | 1              | 0              | 0              | 1              | 0              | 0              | 1              | 5.14 |
| STAX B                       | Store A indirect                      | 0                    | 0              | 0              | 0              | 0              | 0              | 1              | 0              | 5.6  | RC                             | Return on carry                         | 1                    | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 5.14 |
| STAX D                       | Store A indirect                      | 0                    | 0              | 0              | 1              | 0              | 0              | 1              | 0              | 5.6  | RNC                            | Return on no carry                      | 1                    | 1              | 0              | 1              | 0              | 0              | 0              | 0              | 5.14 |
| LDAX B                       | Load A indirect                       | 0                    | 0              | 0              | 0              | 1              | 0              | 1              | 0              | 5.5  | RZ                             | Return on zero                          | 1                    | 1              | 0              | 0              | 1              | 0              | 0              | 0              | 5.14 |
| LDAX D                       | Load A indirect                       | 0                    | 0              | 0              | 1              | 1              | 0              | 1              | 0              | 5.5  | RNZ                            | Return on no zero                       | 1                    | 1              | 0              | 0              | 0              | 0              | 0              | 0              | 5.14 |
| STA                          | Store A direct                        | 0                    | 0              | 1              | 1              | 0              | 0              | 1              | 0              | 5.5  | RP                             | Return on positive                      | 1                    | 1              | 1              | 1              | 0              | 0              | 0              | 0              | 5.14 |
| LDA                          | Load A direct                         | 0                    | 0              | 1              | 1              | 1              | 0              | 1              | 0              | 5.5  | RM                             | Return on minus                         | 1                    | 1              | 1              | 1              | 1              | 0              | 0              | 0              | 5.14 |
| SHLD                         | Store H & L direct                    | 0                    | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 5.5  | RPE                            | Return on parity even                   | 1                    | 1              | 1              | 0              | 1              | 0              | 0              | 0              | 5.14 |
| LHLD                         | Load H & L direct                     | 0                    | 0              | 1              | 0              | 1              | 0              | 1              | 0              | 5.5  | RPO                            | Return on parity odd                    | 1                    | 1              | 1              | 0              | 0              | 0              | 0              | 0              | 5.14 |
| XCHG                         | Exchange D & E, H & L<br>Registers    | 1                    | 1              | 1              | 0              | 1              | 0              | 1              | 1              | 5.6  | <b>RESTART</b>                 |   |                      |                |                |                |                |                |                |                |      |
| <b>STACK OPS</b>             |                                       |                      |                |                |                |                |                |                |                |      |                                |   |                      |                |                |                |                |                |                |                |      |
| PUSH B                       | Push register Pair B &<br>C on stack  | 1                    | 1              | 0              | 0              | 0              | 1              | 0              | 1              | 5.15 | RST                            | Restart                                 | 1                    | 1              | A              | A              | A              | 1              | 1              | 1              | 5.14 |
| PUSH D                       | Push register Pair D &<br>E on stack  | 1                    | 1              | 0              | 1              | 0              | 1              | 0              | 1              | 5.15 | <b>INPUT/OUTPUT</b>            |   |                      |                |                |                |                |                |                |                |      |
| PUSH H                       | Push register Pair H &<br>L on stack  | 1                    | 1              | 1              | 0              | 0              | 1              | 0              | 1              | 5.15 | IN                             | Input                                   | 1                    | 1              | 0              | 1              | 1              | 0              | 1              | 1              | 5.16 |
| PUSH PSW                     | Push A and Flags<br>on stack          | 1                    | 1              | 1              | 1              | 0              | 1              | 0              | 1              | 5.15 | OUT                            | Output                                  | 1                    | 1              | 0              | 1              | 0              | 0              | 1              | 1              | 5.16 |
| POP B                        | Pop register Pair B &<br>C off stack  | 1                    | 1              | 0              | 0              | 0              | 0              | 0              | 1              | 5.15 | <b>INCREMENT AND DECREMENT</b> |   |                      |                |                |                |                |                |                |                |      |
| POP D                        | Pop register Pair D &<br>E off stack  | 1                    | 1              | 0              | 1              | 0              | 0              | 0              | 1              | 5.15 | INR r                          | Increment register                      | 0                    | 0              | 0              | 0              | 0              | 1              | 0              | 0              | 5.8  |
| POP H                        | Pop register Pair H &<br>L off stack  | 1                    | 1              | 1              | 0              | 0              | 0              | 0              | 1              | 5.15 | DCR r                          | Decrement register                      | 0                    | 0              | 0              | 0              | 0              | 1              | 0              | 1              | 5.8  |
| POP PSW                      | Pop A and Flags<br>off stack          | 1                    | 1              | 1              | 1              | 0              | 0              | 0              | 1              | 5.15 | INR M                          | Increment memory                        | 0                    | 0              | 1              | 1              | 0              | 1              | 0              | 0              | 5.8  |
| XTHL                         | Exchange top of<br>stack, H & L       | 1                    | 1              | 1              | 0              | 0              | 0              | 1              | 1              | 5.16 | DCR M                          | Decrement memory                        | 0                    | 0              | 1              | 1              | 0              | 1              | 0              | 1              | 5.8  |
| SPHL                         | H & L to stack pointer                | 1                    | 1              | 1              | 1              | 1              | 0              | 0              | 1              | 5.16 | INX B                          | Increment B & C<br>registers            | 0                    | 0              | 0              | 0              | 0              | 0              | 1              | 1              | 5.9  |
| LXI SP                       | Load immediate stack<br>pointer       | 0                    | 0              | 1              | 1              | 0              | 0              | 0              | 1              | 5.5  | INX D                          | Increment D & E<br>registers            | 0                    | 0              | 0              | 1              | 0              | 0              | 1              | 1              | 5.9  |
| INX SP                       | Increment stack pointer               | 0                    | 0              | 1              | 1              | 0              | 0              | 1              | 1              | 5.9  | INX H                          | Increment H & L<br>registers            | 0                    | 0              | 1              | 0              | 0              | 0              | 1              | 1              | 5.9  |
| DCX SP                       | Decrement stack<br>pointer            | 0                    | 0              | 1              | 1              | 1              | 0              | 1              | 1              | 5.9  | DCX B                          | Decrement B & C                         | 0                    | 0              | 0              | 0              | 1              | 0              | 1              | 1              | 5.9  |
| <b>JUMP</b>                  |                                       |                      |                |                |                |                |                |                |                |      |                                |   |                      |                |                |                |                |                |                |                |      |
| JMP                          | Jump unconditional                    | 1                    | 1              | 0              | 0              | 0              | 0              | 1              | 1              | 5.13 | DCX D                          | Decrement D & E                         | 0                    | 0              | 0              | 1              | 1              | 0              | 1              | 1              | 5.9  |
| JC                           | Jump on carry                         | 1                    | 1              | 0              | 1              | 1              | 0              | 1              | 0              | 5.13 | DCX H                          | Decrement H & L                         | 0                    | 0              | 1              | 0              | 1              | 0              | 1              | 1              | 5.9  |
| JNC                          | Jump on no carry                      | 1                    | 1              | 0              | 1              | 0              | 0              | 1              | 0              | 5.13 | DAD B                          | Add B & C to H & L                      | 0                    | 0              | 0              | 0              | 1              | 0              | 0              | 1              | 5.9  |
| JZ                           | Jump on zero                          | 1                    | 1              | 0              | 0              | 1              | 0              | 1              | 0              | 5.13 | DAD D                          | Add D & E to H & L                      | 0                    | 0              | 0              | 1              | 1              | 0              | 0              | 1              | 5.9  |
| JNZ                          | Jump on no zero                       | 1                    | 1              | 0              | 0              | 0              | 0              | 1              | 0              | 5.13 | DAD H                          | Add H & L to H & L                      | 0                    | 0              | 1              | 0              | 1              | 0              | 0              | 1              | 5.9  |
| JP                           | Jump on positive                      | 1                    | 1              | 1              | 1              | 0              | 0              | 1              | 0              | 5.13 | DAD SP                         | Add stack pointer to<br>H & L           | 0                    | 0              | 1              | 1              | 1              | 0              | 0              | 1              | 5.9  |
| JM                           | Jump on minus                         | 1                    | 1              | 1              | 1              | 1              | 0              | 1              | 0              | 5.13 | <b>SUBTRACT</b>                |   |                      |                |                |                |                |                |                |                |      |
| JPE                          | Jump on parity even                   | 1                    | 1              | 1              | 0              | 1              | 0              | 1              | 0              | 5.13 | SUB r                          | Subtract register<br>from A             | 1                    | 0              | 0              | 1              | 0              | S              | S              | S              | 5.7  |
| JPO                          | Jump on parity odd                    | 1                    | 1              | 1              | 0              | 0              | 0              | 1              | 0              | 5.13 | SBB r                          | Subtract register from<br>A with borrow | 1                    | 0              | 0              | 1              | 1              | S              | S              | S              | 5.7  |
| PCHL                         | H & L to program<br>counter           | 1                    | 1              | 1              | 0              | 1              | 0              | 0              | 1              | 5.15 | SUB M                          | Subtract memory<br>from A               | 1                    | 0              | 0              | 1              | 0              | 1              | 1              | 0              | 5.7  |
| <b>CALL</b>                  |                                       |                      |                |                |                |                |                |                |                |      |                                |   |                      |                |                |                |                |                |                |                |      |
| CALL                         | Call unconditional                    | 1                    | 1              | 0              | 0              | 1              | 1              | 0              | 1              | 5.13 | SBB M                          | Subtract memory from<br>A with borrow   | 1                    | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 5.8  |
| CC                           | Call on carry                         | 1                    | 1              | 0              | 1              | 1              | 1              | 0              | 0              | 5.14 | SUI                            | Subtract immediate<br>from A            | 1                    | 1              | 0              | 1              | 0              | 1              | 1              | 0              | 5.7  |
| CNC                          | Call on no carry                      | 1                    | 1              | 0              | 1              | 0              | 1              | 0              | 0              | 5.14 |                                |   |                      |                |                |                |                |                |                |                |      |

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## 8085A/8085A-2

**8085A INSTRUCTION SET SUMMARY (Cont'd)**  
**Table 6-1**

| Mnemonic       | Description                           | Instruction Code (1) |                |                |                |                |                |                |                | Page | Mnemonic                      | Description                  | Instruction Code (1) |                |                |                |                |                |                |                | Page |
|----------------|---------------------------------------|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------|-------------------------------|------------------------------|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------|
|                |                                       | D <sub>7</sub>       | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |      |                               |                              | D <sub>7</sub>       | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |      |
| SBI            | Subtract immediate from A with borrow | 1                    | 1              | 0              | 1              | 1              | 1              | 1              | 0              | 5-8  | RRC                           | Rotate A right               | 0                    | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 5-12 |
| <b>LOGICAL</b> |                                       |                      |                |                |                |                |                |                |                | RAL  | Rotate A left through carry   | 0                            | 0                    | 0              | 1              | 0              | 1              | 1              | 1              | 5-12           |      |
| ANA r          | And register with A                   | 1                    | 0              | 1              | 0              | 0              | S              | S              | S              | 5-9  | RAR                           | Rotate A right through carry | 0                    | 0              | 0              | 1              | 1              | 1              | 1              | 1              | 5-12 |
| XRA r          | Exclusive OR register with A          | 1                    | 0              | 1              | 0              | 1              | S              | S              | S              | 5-10 | <b>SPECIALS</b>               |                              |                      |                |                |                |                |                |                |                |      |
| ORA r          | OR register with A                    | 1                    | 0              | 1              | 1              | 0              | S              | S              | S              | 5-10 | CMA                           | Complement A                 | 0                    | 0              | 1              | 0              | 1              | 1              | 1              | 1              | 5-12 |
| CMP r          | Compare register with A               | 1                    | 0              | 1              | 1              | 1              | S              | S              | S              | 5-11 | STC                           | Set carry                    | 0                    | 0              | 1              | 1              | 0              | 1              | 1              | 1              | 5-12 |
| ANA M          | And memory with A                     | 1                    | 0              | 1              | 0              | 0              | 1              | 1              | 0              | 5-10 | CMC                           | Complement carry             | 0                    | 0              | 1              | 1              | 1              | 1              | 1              | 1              | 5-12 |
| XRAM           | Exclusive OR memory with A            | 1                    | 0              | 1              | 0              | 1              | 1              | 1              | 0              | 5-10 | DAA                           | Decimal adjust A             | 0                    | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 5-9  |
| ORAM           | OR memory with A                      | 1                    | 0              | 1              | 1              | 0              | 1              | 1              | 0              | 5-11 | <b>CONTROL</b>                |                              |                      |                |                |                |                |                |                |                |      |
| CMP M          | Compare memory with A                 | 1                    | 0              | 1              | 1              | 1              | 1              | 1              | 0              | 5-11 | EI                            | Enable Interrupts            | 1                    | 1              | 1              | 1              | 1              | 0              | 1              | 1              | 5-17 |
| ANI            | And immediate with A                  | 1                    | 1              | 1              | 0              | 0              | 1              | 1              | 0              | 5-10 | DI                            | Disable Interrupt            | 1                    | 1              | 1              | 1              | 0              | 0              | 1              | 1              | 5-17 |
| XRI            | Exclusive OR immediate with A         | 1                    | 1              | 1              | 0              | 1              | 1              | 1              | 0              | 5-10 | NOP                           | No-operation                 | 0                    | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 5-17 |
| ORI            | OR immediate with A                   | 1                    | 1              | 1              | 1              | 0              | 1              | 1              | 0              | 5-11 | HLT                           | Halt                         | 0                    | 1              | 1              | 1              | 0              | 1              | 1              | 0              | 5-17 |
| CPi            | Compare immediate with A              | 1                    | 1              | 1              | 1              | 1              | 1              | 1              | 0              | 5-11 | <b>NEW 8085A INSTRUCTIONS</b> |                              |                      |                |                |                |                |                |                |                |      |
| <b>ROTATE</b>  |                                       |                      |                |                |                |                |                |                |                | RIM  | Read Interrupt Mask           | 0                            | 0                    | 1              | 0              | 0              | 0              | 0              | 0              | 5-17           |      |
| RLC            | Rotate A left                         | 0                    | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 5-11 | SIM                           | Set Interrupt Mask           | 0                    | 0              | 1              | 1              | 0              | 0              | 0              | 0              | 5-18 |

NOTES: 1. DDS or SSS: 8 000, C 001, D 010, E011, H 100, L 101, Memory 110, A 111.

2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

\*All mnemonics copyrighted © Intel Corporation 1976.



## 8259A PROGRAMMABLE INTERRUPT CONTROLLER

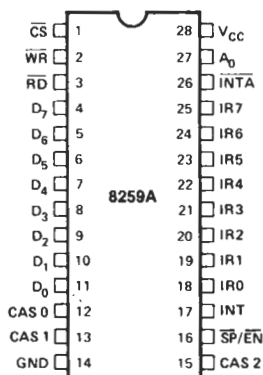
- MCS-86™ Compatible
- MCS-80/85™ Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28-Pin Dual-In-Line Package

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

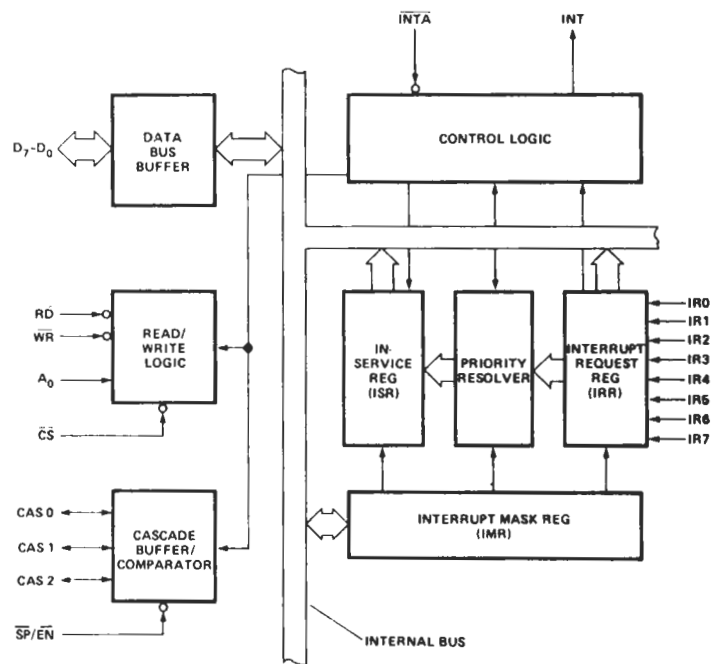
### PIN CONFIGURATION



### PIN NAMES

|                                |                             |
|--------------------------------|-----------------------------|
| D <sub>7</sub> -D <sub>0</sub> | DATA BUS (BI-DIRECTIONAL)   |
| RD                             | READ INPUT                  |
| WR                             | WRITE INPUT                 |
| A <sub>0</sub>                 | COMMAND SELECT ADDRESS      |
| CS                             | CHIP SELECT                 |
| CAS2-CAS0                      | CASCADE LINES               |
| SP/EN                          | SLAVE PROGRAM INPUT/ENABLE  |
| INT                            | INTERRUPT OUTPUT            |
| INTA                           | INTERRUPT ACKNOWLEDGE INPUT |
| IR0-IR7                        | INTERRUPT REQUEST INPUTS    |

### BLOCK DIAGRAM



## 8259A

## INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

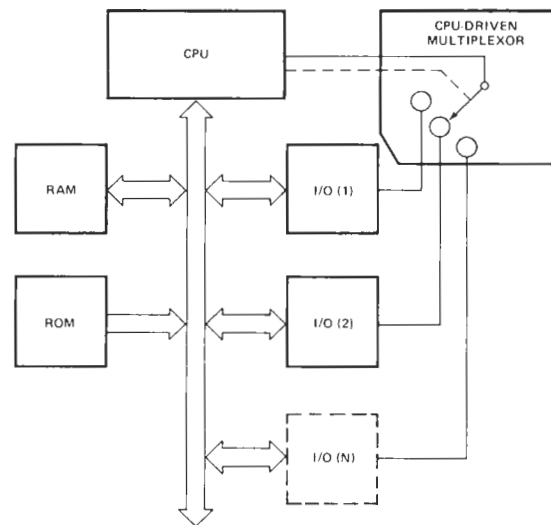
Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

## 8259A BASIC FUNCTIONAL DESCRIPTION

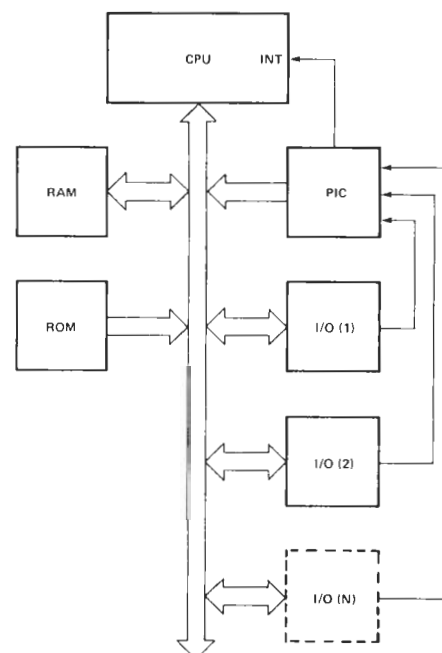
### GENERAL

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to

match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.



Polled Method



Interrupt Method

## 8259A

**INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)**

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

**PRIORITY RESOLVER**

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during  $\overline{INTA}$  pulse.

**INTERRUPT MASK REGISTER (IMR)**

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

**INT (INTERRUPT)**

This output goes directly to the CPU interrupt input. The  $V_{OH}$  level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

 **$\overline{INTA}$  (INTERRUPT ACKNOWLEDGE)**

$\overline{INTA}$  pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode ( $\mu$ PM) of the 8259A.

**DATA BUS BUFFER**

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

**READ/WRITE CONTROL LOGIC**

The function of this block is to accept OUTPUT commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

 **$\overline{CS}$  (CHIP SELECT)**

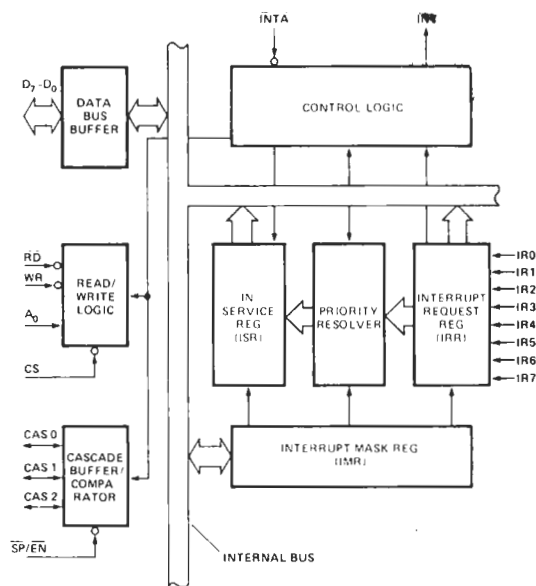
A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

 **$\overline{WR}$  (WRITE)**

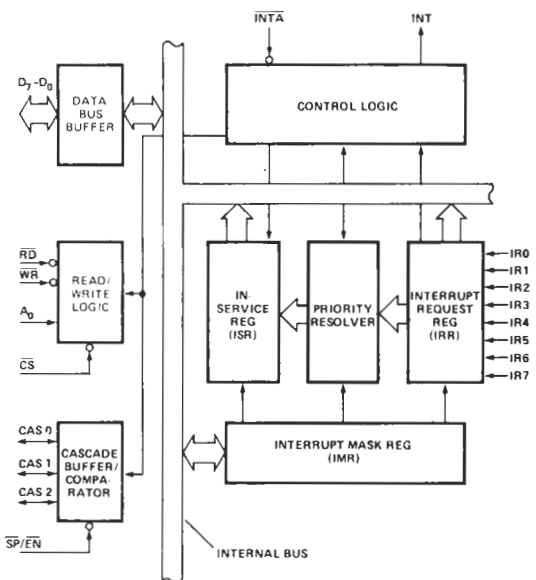
A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

 **$\overline{RD}$  (READ)**

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.



8259A Block Diagram



8259A Block Diagram

**A<sub>0</sub>**

This input signal is used in conjunction with  $\overline{WR}$  and  $\overline{RD}$  signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

8259A

**THE CASCADE BUFFER/COMPARATOR**

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive  $\overline{INTA}$  pulses. (See section "Cascading the 8259A".)

**INTERRUPT SEQUENCE**

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

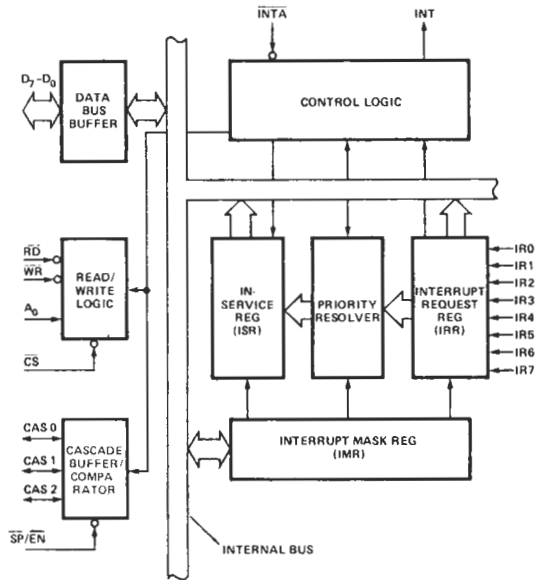
The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an  $\overline{INTA}$  pulse.
4. Upon receiving an  $\overline{INTA}$  from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more  $\overline{INTA}$  pulses to be sent to the 8259A from the CPU group.
6. These two  $\overline{INTA}$  pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first  $\overline{INTA}$  pulse and the higher 8-bit address is released at the second  $\overline{INTA}$  pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third  $\overline{INTA}$  pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

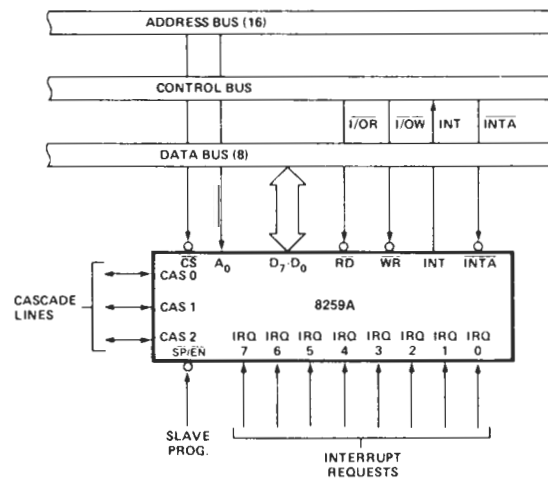
The events occurring in an MCS-86 system are the same until step 4.

4. Upon receiving an  $\overline{INTA}$  from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The MCS-86 CPU will initiate a second  $\overline{INTA}$  pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second  $\overline{INTA}$  pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.



8259A Block Diagram



8259A Interface to Standard System Bus

**8259A****INTERRUPT SEQUENCE OUTPUTS****MCS-80/85 SYSTEM**

This sequence is timed by three  $\overline{\text{INTA}}$  pulses. During the first  $\overline{\text{INTA}}$  pulse the CALL opcode is enabled onto the data bus.

**Content of First Interrupt Vector Byte**

|           | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|----|----|----|----|----|----|----|----|
| CALL CODE | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 1  |

During the second  $\overline{\text{INTA}}$  pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A<sub>5</sub>-A<sub>7</sub> are programmed, while A<sub>0</sub>-A<sub>4</sub> are automatically inserted by the 8259A. When Interval = 8 only A<sub>6</sub> and A<sub>7</sub> are programmed, while A<sub>0</sub>-A<sub>5</sub> are automatically inserted.

**Content of Second Interrupt Vector Byte**

| IR | Interval = 4 |    |    |    |    |    |    |    |
|----|--------------|----|----|----|----|----|----|----|
|    | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 7  | A7           | A6 | A5 | 1  | 1  | 1  | 0  | 0  |
| 6  | A7           | A6 | A5 | 1  | 1  | 0  | 0  | 0  |
| 5  | A7           | A6 | A5 | 1  | 0  | 1  | 0  | 0  |
| 4  | A7           | A6 | A5 | 1  | 0  | 0  | 0  | 0  |
| 3  | A7           | A6 | A5 | 0  | 1  | 1  | 0  | 0  |
| 2  | A7           | A6 | A5 | 0  | 1  | 0  | 0  | 0  |
| 1  | A7           | A6 | A5 | 0  | 0  | 1  | 0  | 0  |
| 0  | A7           | A6 | A5 | 0  | 0  | 0  | 0  | 0  |

| IR | Interval = 8 |    |    |    |    |    |    |    |
|----|--------------|----|----|----|----|----|----|----|
|    | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 7  | A7           | A6 | 1  | 1  | 1  | 0  | 0  | 0  |
| 6  | A7           | A6 | 1  | 1  | 0  | 0  | 0  | 0  |
| 5  | A7           | A6 | 1  | 0  | 1  | 0  | 0  | 0  |
| 4  | A7           | A6 | 1  | 0  | 0  | 0  | 0  | 0  |
| 3  | A7           | A6 | 0  | 1  | 1  | 0  | 0  | 0  |
| 2  | A7           | A6 | 0  | 1  | 0  | 0  | 0  | 0  |
| 1  | A7           | A6 | 0  | 0  | 1  | 0  | 0  | 0  |
| 0  | A7           | A6 | 0  | 0  | 0  | 0  | 0  | 0  |

During the third  $\overline{\text{INTA}}$  pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A<sub>8</sub>-A<sub>15</sub>), is enabled onto the bus.

**Content of Third Interrupt Vector Byte**

| D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |

**MCS-86 SYSTEM**

MCS-86 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80/85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the  $\overline{\text{INTA}}$  pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in MCS-86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A<sub>5</sub>-A<sub>11</sub> are unused in MCS-86 mode):

**Content of Interrupt Vector Byte for MCS-86 System Mode**

|     | D7  | D6  | D5  | D4  | D3  | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|
| IR7 | A15 | A14 | A13 | A12 | A11 | 1  | 1  | 1  |
| IR6 | A15 | A14 | A13 | A12 | A11 | 1  | 1  | 0  |
| IR5 | A15 | A14 | A13 | A12 | A11 | 1  | 0  | 1  |
| IR4 | A15 | A14 | A13 | A12 | A11 | 1  | 0  | 0  |
| IR3 | A15 | A14 | A13 | A12 | A11 | 0  | 1  | 1  |
| IR2 | A15 | A14 | A13 | A12 | A11 | 0  | 1  | 0  |
| IR1 | A15 | A14 | A13 | A12 | A11 | 0  | 0  | 1  |
| IR0 | A15 | A14 | A13 | A12 | A11 | 0  | 0  | 0  |

## 8259A

**PROGRAMMING THE 8259A**

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs)*: Before normal operation can begin, each 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by  $\overline{WR}$  pulses. This sequence is described in Figure 1.
2. *Operation Command Words (OCWs)*: These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
  - a. Fully nested mode
  - b. Rotating priority mode
  - c. Special mask mode
  - d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

**INITIALIZATION****GENERAL**

Whenever a command is issued with  $A_0 = 0$  and  $D_4 = 1$ , this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

- a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
- b. The Interrupt Mask Register is cleared.
- c. IR 7 input is assigned priority 7.
- d. The slave mode address is set to 7.
- e. Special Mask Mode is cleared and Status Read is set to IRR.
- f. If  $IC_4 = 0$ , then all functions selected in ICW4 are set to zero. (Non-Buffered mode\*, no Auto-EOI, MCS-80/85 system).

\*Note: Master/Slave in ICW4 is only used in the buffered mode.

| $A_0$ | $D_4$ | $D_3$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | INPUT OPERATION (READ)                             |
|-------|-------|-------|-----------------|-----------------|-----------------|--|
| 0     |       |       | 0               | 1               | 0               | IRR, ISR or Interrupting Level → DATA BUS (Note 1) |
| 1     |       |       | 0               | 1               | 0               | IMR → DATA BUS                                     |
|       |       |       |                 |                 |                 | OUTPUT OPERATION (WRITE)                           |
| 0     | 0     | 0     | 1               | 0               | 0               | DATA BUS → OCW2                                    |
| 0     | 0     | 1     | 1               | 0               | 0               | DATA BUS → OCW3                                    |
| 0     | 1     | X     | 1               | 0               | 0               | DATA BUS → ICW1                                    |
| 1     | X     | X     | 1               | 0               | 0               | DATA BUS → OCW1, ICW2, ICW3, ICW4 (Note 2)         |
|       |       |       |                 |                 |                 | DISABLE FUNCTION                                   |
| X     | X     | X     | 1               | 1               | 0               | DATA BUS → 3-STATE                                 |
| X     | X     | X     | X               | X               | 1               | DATA BUS → 3-STATE                                 |

**Notes:** 1. Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.  
2. On-chip sequencer logic queues these commands into proper sequence.

**8259A Basic Operation**



## 8259A

**INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)**

**A<sub>5</sub>-A<sub>15</sub>:** Page starting address of service routines. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A<sub>0</sub>-A<sub>15</sub>). When the routine interval is 4, A<sub>0</sub>-A<sub>4</sub> are automatically inserted by the 8259A, while A<sub>5</sub>-A<sub>15</sub> are programmed externally. When the routine interval is 8, A<sub>0</sub>-A<sub>5</sub> are automatically inserted by the 8259A, while A<sub>6</sub>-A<sub>15</sub> are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system A<sub>15</sub>-A<sub>11</sub> are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A<sub>10</sub>-A<sub>5</sub> are ignored and ADI (Address interval) has no effect.

**LTIM:** If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

**ADI:** CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

**SNGL:** Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

**IC4:** If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

**INITIALIZATION COMMAND WORD 3 (ICW3)**

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

- In the master mode (either when  $\overline{SP} = 1$ , or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for MCS-86 only byte 2) through the cascade lines.
- In the slave mode (either when  $\overline{SP} = 0$ , or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for MCS-86) are released by it on the Data Bus.

**INITIALIZATION COMMAND WORD 4 (ICW4)**

**FNM:** If FNM = 1 the fully nested mode is programmed.

**BUF:** If BUF = 1 the buffered mode is programmed. In buffered mode  $\overline{SP}/\overline{EN}$  becomes an enable output and the master/slave determination is by M/S.

**M/S:** If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

**AEOI:** If AEOI = 1 the automatic end of interrupt mode is programmed.

**$\mu$ PM:** Microprocessor mode:  $\mu$ PM = 0 sets the 8259A for MCS-80/85 system operation,  $\mu$ PM = 1 sets the 8259A for MCS-86 system operation.

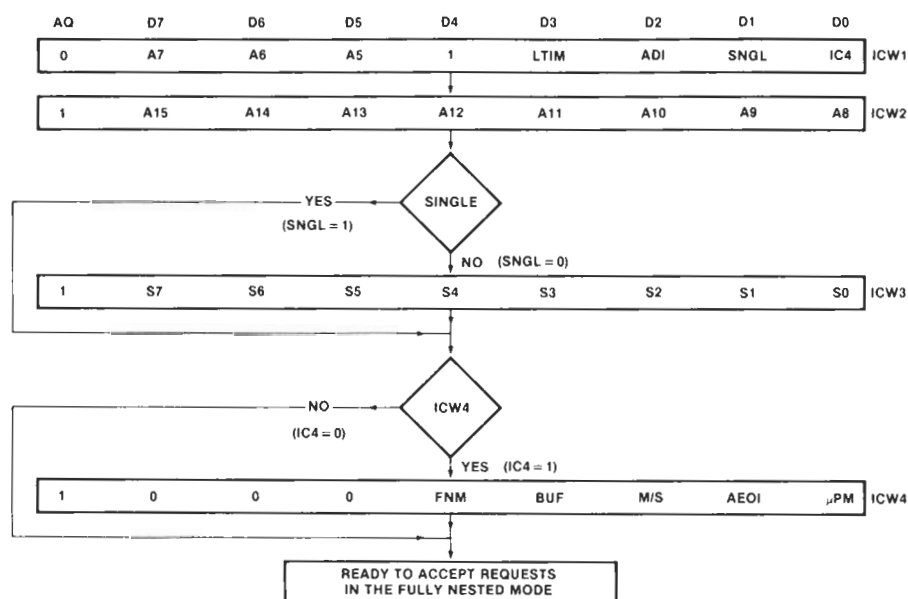
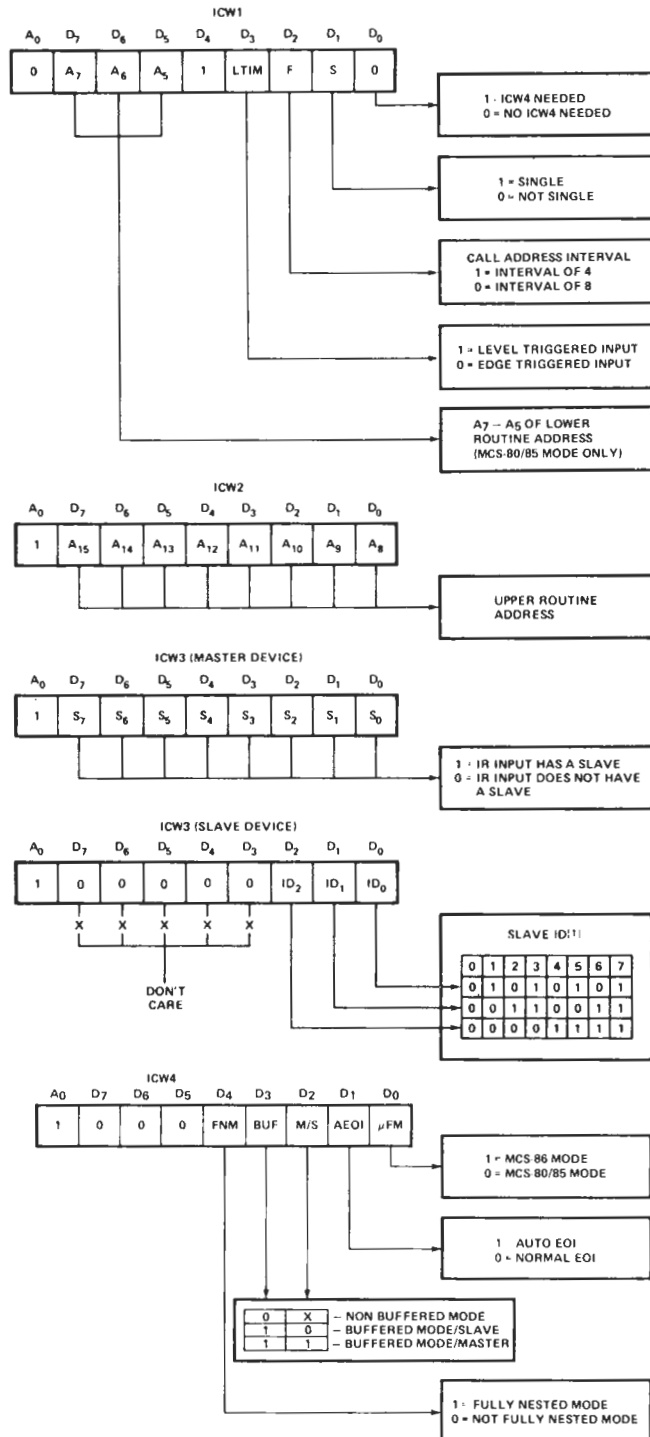


Figure 1. Initialization Sequence

8259A

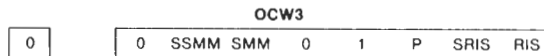
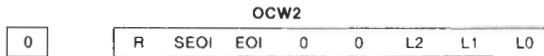
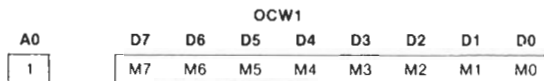


NOTE 1: SLAVED ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.  
NOTE 2: X INDICATED "DON'T CARE".

Initialization Command Word Format

**8259A****OPERATION COMMAND WORDS (OCWs)**

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

**OPERATION CONTROL WORDS (OCWs)****OPERATION CONTROL WORD 1 (OCW1)**

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR).  $M_7$ – $M_0$  represent the eight mask bits.  $M = 1$  indicates the channel is masked (inhibited).  $M = 0$  indicates the channel is enabled.

**OPERATION CONTROL WORD 2 (OCW2)**

R, SEOI, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

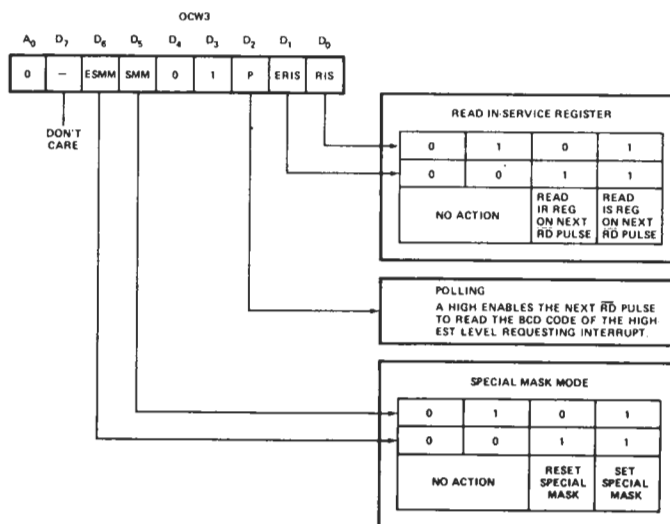
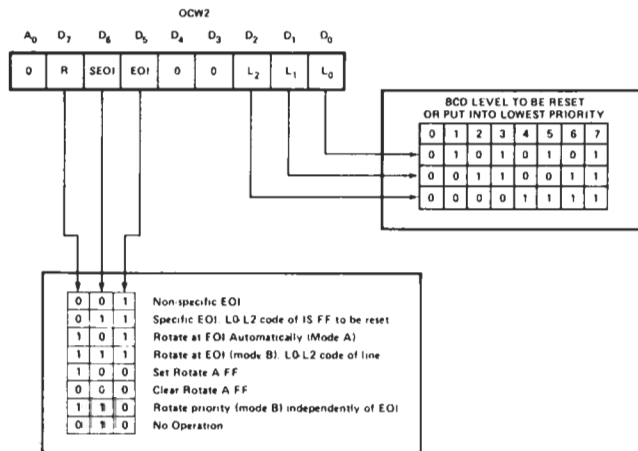
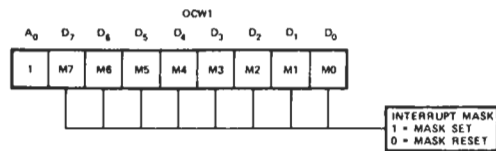
$L_2$ ,  $L_1$ ,  $L_0$  — These bits determine the interrupt level acted upon when the SEOI bit is active.

**OPERATION CONTROL WORD 3 (OCW3)**

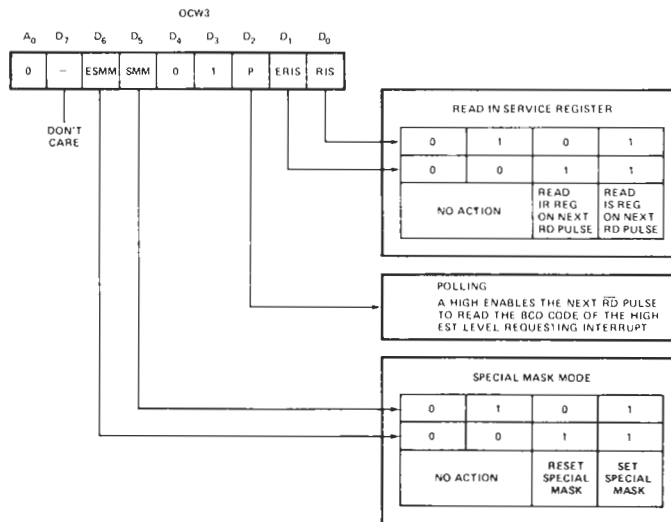
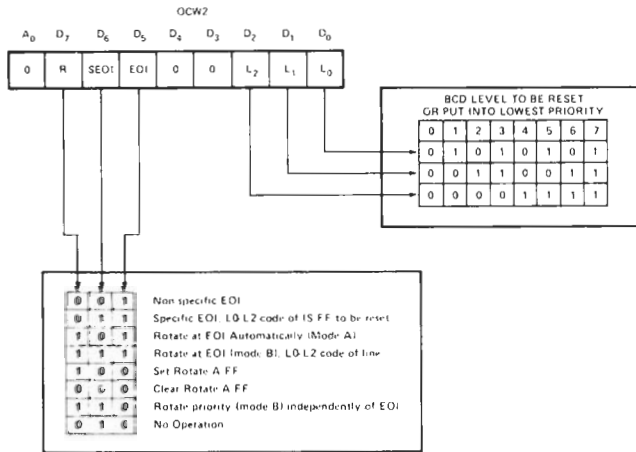
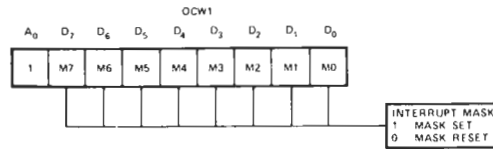
ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When  $ESMM = 0$  the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If  $ESMM = 1$  and  $SMM = 1$  the 8259A will enter Special Mask Mode. If  $ESMM = 1$  and  $SMM = 0$  the 8259A will revert to normal mask mode. When  $ESMM = 0$ , SMM has no effect.

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**8259A****INTERRUPT MASKS**

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

**SPECIAL MASK MODE**

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

**BUFFERED MODE**

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on  $\overline{SP/EN}$  to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the  $\overline{SP/EN}$  output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

**NESTED MODE**

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an

End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

**THE SPECIAL FULLY NESTED MODE**

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

- a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)
- b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

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**POLL**

In this mode the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by programmer initiative using a Poll command.

The Poll command is issued by setting  $P = "1"$  in OCW3. The 8259A treats the next  $\overline{RD}$  pulse to the 8259A (i.e.,  $\overline{RD} = 0$ ,  $\overline{CS} = 0$ ) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from  $\overline{WR}$  to  $\overline{RD}$ .

The word enabled onto the data bus during  $\overline{RD}$  is:

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| I  | —  | —  | —  | —  | W2 | W1 | W0 |

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the  $\overline{INTA}$  sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

**END OF INTERRUPT (EOI)**

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence  $\overline{INTA}$  pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice, once for the master and once for the corresponding slave if slaves are in use.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the nested mode the highest IS level was necessarily the last level acknowledged and serviced.

However, when a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt (SEOI) must be issued which includes as part of the command the IS level to be reset. EOI is issued whenever  $E = 1$ , in OCW2, where L0-L2 is the binary level of the IS bit to be reset. Note that although the Rotate command can be issued together with an EOI where  $E = 1$ , it is not necessarily tied to it.

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

**AUTOMATIC END OF INTERRUPT (AEOI) MODE**

If  $AEOI = 1$  in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85,

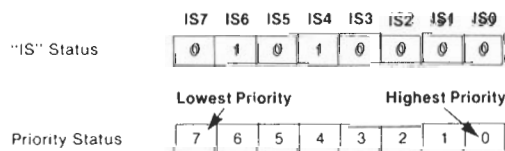
second in MCS-86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

To achieve automatic rotation (Rotate Mode A) within AEOI, there is a special rotate flip-flop. It is set by OCW2 with  $R = 1$ ,  $SEOI = 0$ ,  $E = 0$ , and cleared with  $R = 0$ ,  $SEOI = 0$ ,  $E = 0$ .

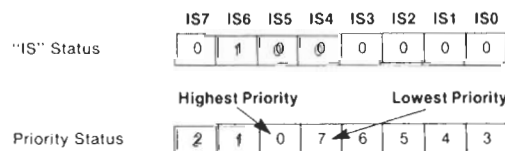
**ROTATING PRIORITY MODE A (AUTOMATIC ROTATION) FOR EQUAL PRIORITY DEVICES**

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

**Before Rotate** (IR4 the highest priority requiring service)



**After Rotate** (IR4 was serviced, all other priorities rotated correspondingly)



The Rotate command mode A is issued in OCW2 where:  $R = 1$ ,  $E = 1$ ,  $SEOI = 0$ . Internal status is updated by an End of Interrupt (EOI or AEOI) command. If  $R = 1$ ,  $E = 0$ ,  $SEOI = 0$ , a "Rotate-A" flip-flop is set. This is useful in AEOI, and described under Automatic End of Interrupt.

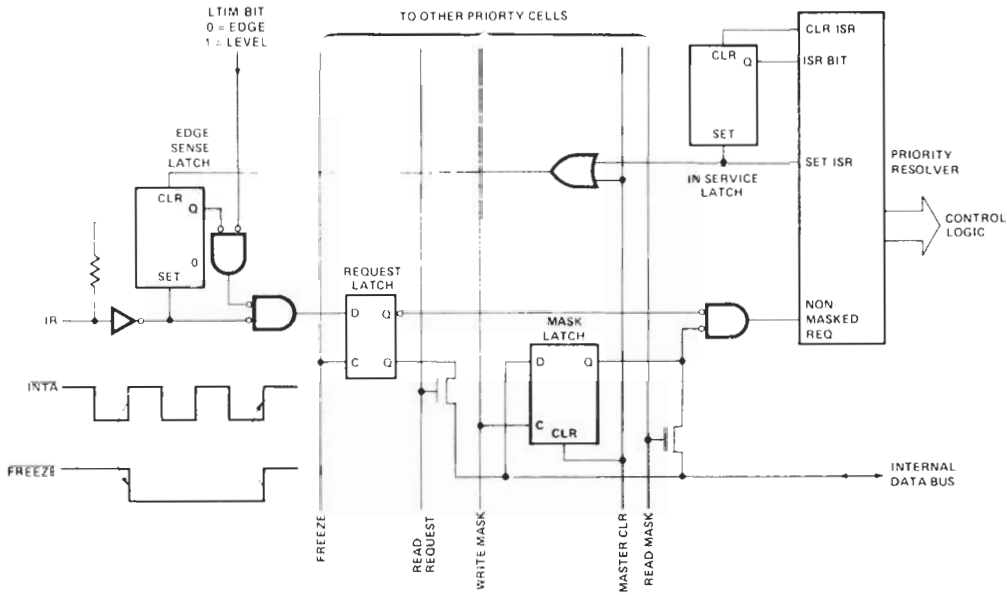
**ROTATING PRIORITY MODE B (ROTATION BY SOFTWARE)**

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Rotate command is issued in OCW2 where:  $R = 1$ ,  $SEOI = 1$ ; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command or independently.

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NOTES

1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE/IS ACTIVE DURING INTA/ AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D LATCH

| C | D              | Q                | OPERATION |
|---|----------------|------------------|-----------|
| 1 | D <sub>i</sub> | D <sub>i</sub>   | FOLLOW    |
| 0 | X              | Q <sub>n-1</sub> | HOLD      |

Priority Cell

LEVEL TRIGGERED MODE

This mode is programmed using bit 3 in ICW1.

If LTM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The above figure shows a conceptual circuit to give the reader an understanding of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW3 and reading with RD.

**Interrupt Mask Register:** 8-bit register whose content specifies the interrupt request lines being masked. acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

**In-Service Register (ISR):** 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

**Interrupt Mask Register:** 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a WR pulse is issued with OCW3 (ERIS = 1, RIS = 0.)

The ISR can be read in a similar mode when ERIS = 1, RIS = 1 in the OCW3.

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever RD is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.



## 8259A

## SUMMARY OF 8259A INSTRUCTION SET

| Inst. # | Mnemonic | A0 | D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 | Operation Description   |
|---------|----------|----|-----|-----|-----|-----|-----|-----|----|----|---|
| 1       | ICW1 A   | 0  | A7  | A6  | A5  | 1   | 0   | 1   | 1  | 0  | } Format = 4, single, edge triggered<br>Format = 4, single, level triggered<br>Byte 1 Initialization Format = 4, not single, edge triggered<br>Format = 4, not single, level triggered<br>No ICW4 Required Format = 8, single, edge triggered<br>Format = 8, single, level triggered<br>Format = 8, not single, edge triggered<br>Format = 8, not single, level triggered |
| 2       | ICW1 B   | 0  | A7  | A6  | A5  | 1   | 1   | 1   | 1  | 0  |   |
| 3       | ICW1 C   | 0  | A7  | A6  | A5  | 1   | 0   | 1   | 0  | 0  |   |
| 4       | ICW1 D   | 0  | A7  | A6  | A5  | 1   | 1   | 1   | 0  | 0  |   |
| 5       | ICW1 E   | 0  | A7  | A6  | 0   | 1   | 0   | 0   | 1  | 0  |   |
| 6       | ICW1 F   | 0  | A7  | A6  | 0   | 1   | 1   | 0   | 1  | 0  |   |
| 7       | ICW1 G   | 0  | A7  | A6  | 0   | 1   | 0   | 0   | 0  | 0  |   |
| 8       | ICW1 H   | 0  | A7  | A6  | 0   | 1   | 1   | 0   | 0  | 0  |   |
| 9       | ICW1 I   | 0  | A7  | A6  | A5  | 1   | 0   | 1   | 1  | 1  | } Format = 4, single, edge triggered<br>Format = 4, single, level triggered<br>Byte 1 Initialization Format = 4, not single, edge triggered<br>Format = 4, not single, level triggered<br>ICW4 Required Format = 8, single, edge triggered<br>Format = 8, single, level triggered<br>Format = 8, not single, edge triggered<br>Format = 8, not single, level triggered    |
| 10      | ICW1 J   | 0  | A7  | A6  | A5  | 1   | 1   | 1   | 1  | 1  |   |
| 11      | ICW1 K   | 0  | A7  | A6  | A5  | 1   | 0   | 1   | 0  | 1  |   |
| 12      | ICW1 L   | 0  | A7  | A6  | A5  | 1   | 1   | 1   | 0  | 1  |   |
| 13      | ICW1 M   | 0  | A7  | A6  | 0   | 1   | 0   | 0   | 1  | 1  |   |
| 14      | ICW1 N   | 0  | A7  | A6  | 0   | 1   | 1   | 0   | 1  | 1  |   |
| 15      | ICW1 O   | 0  | A7  | A6  | 0   | 1   | 0   | 0   | 0  | 1  |   |
| 16      | ICW1 P   | 0  | A7  | A6  | 0   | 1   | 1   | 0   | 0  | 1  |   |
| 17      | ICW2     | 1  | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | Byte 2 initialization   |
| 18      | ICW3 M   | 1  | S7  | S6  | S5  | S4  | S3  | S2  | S1 | S0 | Byte 3 initialization — master  |
| 19      | ICW3 S   | 1  | 0   | 0   | 0   | 0   | 0   | S2  | S1 | S0 | Byte 3 initialization — slave   |
| 20      | ICW4 A   | 1  | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | No action, redundant  |
| 21      | ICW4 B   | 1  | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 1  | Non-buffered mode, no AEOI, MCS-86  |
| 22      | ICW4 C   | 1  | 0   | 0   | 0   | 0   | 0   | 0   | 1  | 0  | Non-buffered mode, AEOI, MCS-80/85  |
| 23      | ICW4 D   | 1  | 0   | 0   | 0   | 0   | 0   | 0   | 1  | 1  | Non-buffered mode, AEOI, MCS-86   |
| 24      | ICW4 E   | 1  | 0   | 0   | 0   | 0   | 0   | 1   | 0  | 0  | No action, redundant  |
| 25      | ICW4 F   | 1  | 0   | 0   | 0   | 0   | 0   | 1   | 0  | 1  | Non-buffered mode, no AEOI, MCS-86  |
| 26      | ICW4 G   | 1  | 0   | 0   | 0   | 0   | 0   | 1   | 1  | 0  | Non-buffered mode, AEOI, MCS-80/85  |
| 27      | ICW4 H   | 1  | 0   | 0   | 0   | 0   | 0   | 1   | 1  | 1  | Non-buffered mode, AEOI, MCS-86   |
| 28      | ICW4 I   | 1  | 0   | 0   | 0   | 0   | 1   | 0   | 0  | 0  | Buffered mode, slave, no AEOI, MCS-80/85  |
| 29      | ICW4 J   | 1  | 0   | 0   | 0   | 0   | 1   | 0   | 0  | 1  | Buffered mode, slave, no AEOI, MCS-86   |
| 30      | ICW4 K   | 1  | 0   | 0   | 0   | 0   | 1   | 0   | 1  | 0  | Buffered mode, slave, AEOI, MCS-80/85   |
| 31      | ICW4 L   | 1  | 0   | 0   | 0   | 0   | 1   | 0   | 1  | 1  | Buffered mode, slave, AEOI, MCS-86  |
| 32      | ICW4 M   | 1  | 0   | 0   | 0   | 0   | 1   | 1   | 0  | 0  | Buffered mode, master, no AEOI, MCS-80/85   |
| 33      | ICW4 N   | 1  | 0   | 0   | 0   | 0   | 1   | 1   | 0  | 1  | Buffered mode, master, no AEOI, MCS-86  |
| 34      | ICW4 O   | 1  | 0   | 0   | 0   | 0   | 1   | 1   | 1  | 0  | Buffered mode, master, AEOI, MCS-80/85  |
| 35      | ICW4 P   | 1  | 0   | 0   | 0   | 0   | 1   | 1   | 1  | 1  | Buffered mode, master, AEOI, MCS-86   |
| 36      | ICW4 NA  | 1  | 0   | 0   | 0   | 1   | 0   | 0   | 0  | 0  | Fully nested mode, MCS-80, non-buffered, no AEOI  |
| 37      | ICW4 NB  | 1  | 0   | 0   | 0   | 1   | 0   | 0   | 0  | 1  | } ICW4 NB through ICW4 ND are identical to<br>ICW4 B through ICW4 D with the addition of<br>Fully Nested Mode   |
| 38      | ICW4 NC  | 1  | 0   | 0   | 0   | 1   | 0   | 0   | 1  | 0  |   |
| 39      | ICW4 ND  | 1  | 0   | 0   | 0   | 1   | 0   | 0   | 1  | 1  |   |
| 40      | ICW4 NE  | 1  | 0   | 0   | 0   | 1   | 0   | 1   | 0  | 0  |   |
| 41      | ICW4 NF  | 1  | 0   | 0   | 0   | 1   | 0   | 1   | 0  | 1  | } ICW4 NF through ICW4 NP are identical to<br>ICW4 F through ICW4 P with the addition of<br>Fully Nested Mode   |
| 42      | ICW4 NG  | 1  | 0   | 0   | 0   | 1   | 0   | 1   | 1  | 0  |   |
| 43      | ICW4 NH  | 1  | 0   | 0   | 0   | 1   | 0   | 1   | 1  | 1  |   |
| 44      | ICW4 NI  | 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0  | 0  |   |
| 45      | ICW4 NJ  | 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0  | 1  |   |
| 46      | ICW4 NK  | 1  | 0   | 0   | 0   | 1   | 1   | 0   | 1  | 0  |   |
| 47      | ICW4 NL  | 1  | 0   | 0   | 0   | 1   | 1   | 0   | 1  | 1  |   |
| 48      | ICW4 NM  | 1  | 0   | 0   | 0   | 1   | 1   | 1   | 0  | 0  |   |
| 49      | ICW4 NN  | 1  | 0   | 0   | 0   | 1   | 1   | 1   | 0  | 1  |   |
| 50      | ICW4 NO  | 1  | 0   | 0   | 0   | 1   | 1   | 1   | 1  | 0  |   |
| 51      | ICW4 NP  | 1  | 0   | 0   | 0   | 1   | 1   | 1   | 1  | 1  |   |
| 36      | OCW1     | 1  | M7  | M6  | M5  | M4  | M3  | M2  | M1 | M0 | Load mask register, read mask register  |
| 37      | OCW2 E   | 0  | 0   | 0   | 1   | 0   | 0   | 0   | 0  | 0  | Non-specific EOI  |
| 38      | OCW2 SE  | 0  | 0   | 1   | 1   | 0   | 0   | L2  | L1 | L0 | Specific EOI, L0-L2 code of IS FF to be reset   |
| 39      | OCW2 RE  | 0  | 1   | 0   | 1   | 0   | 0   | 0   | 0  | 0  | Rotate at EOI Automatically (Mode A)  |
| 40      | OCW2 RSE | 0  | 1   | 1   | 1   | 0   | 0   | L2  | L1 | L0 | Rotate at EOI (mode B), L0-L2 code of line  |
| 41      | OCW2 R   | 0  | 1   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | Set Rotate A FF   |
| 42      | OCW2 CR  | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | Clear Rotate A FF   |
| 43      | OCW2 RS  | 0  | 1   | 1   | 0   | 0   | 0   | L2  | L1 | L0 | Rotate priority (mode B) independently of EOI   |
| 44      | OCW3 P   | 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0  | 0  | Poll mode   |
| 45      | OCW3 RIS | 0  | 0   | 0   | 0   | 0   | 1   | 0   | 1  | 1  | Read IS register  |

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### SUMMARY OF 8259A INSTRUCTION SET (Cont.)

| Inst. # | Mnemonic | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operation Description |                         |
|---------|----------|----|----|----|----|----|----|----|----|----|-----------------------|-------------------------|
| 46      | OCW3 RR  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0                     | Read request register   |
| 47      | OCW3 SM  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 0                     | Set special mask mode   |
| 48      | OCW3 RSM | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0                     | Reset special mask mode |

**Note:** 1. In the master mode SP pin = 1, in slave mode SP = 0

### Cascading

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

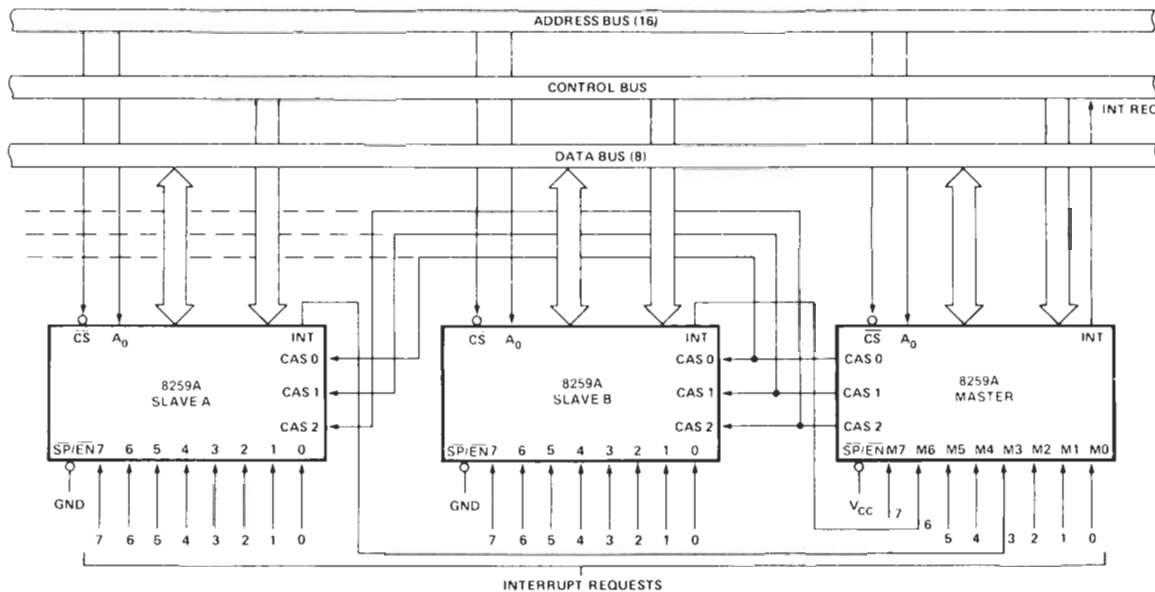
A typical MCS-80/85 system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave

to release the device routine address during bytes 2 and 3 of  $\overline{INTA}$ . (Byte 2 only for MCS-86).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first  $\overline{INTA}$  pulse to the trailing edge of the third pulse. It is obvious that each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ( $\overline{CS}$ ) input of each 8259A.

The cascade lines of the Master 8259A are activated for any interrupt input, even if no slave is connected to that input.



**Figure 2. Cascading the 8259A**

**8259A****PIN FUNCTIONS**

| Name              | I/O | Pin # | Function  |                               |     |                |   |
|-------------------|-----|-------|---|-------------------------------|-----|----------------|---|
| V <sub>CC</sub>   |     | 28    | + 5V supply.  |                               |     |                |   |
| GND               |     | 14    | Ground.   |                               |     |                |   |
| D <sub>0-7</sub>  | I/O | 11-14 | Bidirectional data bus, used for:<br>a) programming the mode of the 8259A (programming is done by software); b) the microprocessor can read the status of the 8259A; c) the 8259A will send vectoring data to the microprocessor when an interrupt is acknowledged.   | A0                            | I   | 27             | Usually the least significant bit of the microprocessor address output. When A0 = 1 the Interrupt Mask Register can be loaded or read. When A0 = 0 the 8259A mode can be programmed or its status can be read. $\overline{CS}$ is active LOW.   |
| IR <sub>0-7</sub> | I   | 18-25 | Interrupt Requests: These are asynchronous inputs. A positive-going edge will generate an interrupt request. Thus a request can be generated by raising the line and holding it high until acknowledged, or by a negative pulse. In level triggered mode, no edge is required. These lines are active HIGH. | INT                           | O   | 17             | Goes directly to the microprocessor interrupt input. This output will have high V <sub>OH</sub> to match the 8080 3.3V V <sub>IH</sub> . INT is active HIGH.  |
| $\overline{RD}$   | I   | 3     | Read (generally from 8228 in MCS-80 system or from 8086 in MCS-86 system).  | C0-C2                         | I/O | 12<br>13<br>15 | Three cascade lines, outputs in master mode and inputs in slave mode. The master issues the binary code of the acknowledged interrupt level on these lines. Each slave compares this code with its own.   |
| $\overline{WR}$   | I   | 2     | Write (generally from 8228 in MCS-80 system or from 8086 in MCS-86 system).   |                               |     |                |   |
| $\overline{INTA}$ | I   | 26    | Interrupt Acknowledge (generally from 8228 in MCS-80 system, 8086 in MCS-86 system). The 8288 generates three distinct $\overline{INTA}$ pulses when a CALL is inserted, the 8086 produces two distinct $\overline{INTA}$ pulses during an interrupt cycle.   | $\overline{SP}/\overline{EN}$ | I/O | 16             | $\overline{SP}/\overline{EN}$ is a dual function pin. In the buffered mode $\overline{SP}/\overline{EN}$ is used to enable bus transceivers ( $\overline{EN}$ ). In the non-buffered mode $\overline{SP}/\overline{EN}$ determines if this 8259A is a master or a slave. If $\overline{SP} = 1$ the 8259A is master; $\overline{SP} = 0$ indicates a slave. |

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias . . . . . - 40°C to 85°C  
Storage Temperature . . . . . - 65°C to + 150°C  
Voltage On Any Pin

With Respect to Ground . . . . . - 0.5V to + 7V  
Power Dissipation . . . . . 1 Watt

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**D.C. CHARACTERISTICS**

T<sub>A</sub> = 0°C to 70°C V<sub>CC</sub> = 5V ± 5% (8259A-8) V<sub>CC</sub> = 5V ± 10% (8259A)

| Symbol               | Parameter                      | Min.       | Max.                  | Units  | Test Conditions  |
|----------------------|--------------------------------|------------|-----------------------|--------|--|
| V <sub>IL</sub>      | Input Low Voltage              | -.5        | .8                    | V      |  |
| V <sub>IH</sub>      | Input High Voltage             | 2.0        | V <sub>CC</sub> + .5V | V      |  |
| V <sub>OL</sub>      | Output Low Voltage             |            | .45                   | V      | I <sub>OL</sub> = 2.2 mA                                 |
| V <sub>OH</sub>      | Output High Voltage            | 2.4        |                       | V      | I <sub>OH</sub> = - 400 μA                               |
| V <sub>OH(INT)</sub> | Interrupt Output High Voltage  | 3.5<br>2.4 |                       | V<br>V | I <sub>OH</sub> = - 100 μA<br>I <sub>OH</sub> = - 400 μA |
| I <sub>LI</sub>      | Input Load Current             |            | 10                    | μA     | V <sub>IN</sub> = V <sub>CC</sub> to 0V                  |
| I <sub>LOL</sub>     | Output Leakage Current         |            | - 10                  | μA     | V <sub>OUT</sub> = 0.45V                                 |
| I <sub>LOH</sub>     | Output Leakage Current         |            | 10                    | μA     | V <sub>OUT</sub> = V <sub>CC</sub>                       |
| I <sub>CC</sub>      | V <sub>CC</sub> Supply Current |            | 85                    | mA     |  |

**8259A**

**8259A A.C. CHARACTERISTICS**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$   $V_{CC} = 5V \pm 5\%$  (8259A-8)  $V_{CC} = 5V \pm 10\%$  (8259A)

**TIMING REQUIREMENTS**

**8259A-8**

**8259A**

| Symbol | Parameter   | Min. | Max. | Min. | Max. | Units | Test Conditions |
|--------|---|------|------|------|------|-------|-----------------|
| TAHRL  | A0/CS Setup to RD/INTA↓                             | 50   |      | 0    |      | ns    |                 |
| TRHAX  | A0/CS Hold after RD/INTA↑                           | 5    |      | 0    |      | ns    |                 |
| TRLRH  | RD Pulse Width                                      | 420  |      | 235  |      | ns    |                 |
| TAHWL  | A0/CS Setup to WR↓                                  | 50   |      | 0    |      | ns    |                 |
| TWHAX  | A0/CS Hold after WR↑                                | 20   |      | 0    |      | ns    |                 |
| TWLWH  | WR Pulse Width                                      | 400  |      | 290  |      | ns    |                 |
| TDVWH  | Data Setup to WR↑                                   | 300  |      | 240  |      | ns    |                 |
| TWHDX  | Data Hold after WR↑                                 | 40   |      | 0    |      | ns    |                 |
| TJLJH  | Interrupt Request Width (Low)                       | 100  |      | 100  |      | ns    | See Note 1      |
| TCVIAH | Cascade Setup to Second or Third INTA↓ (Slave Only) | 55   |      | 55   |      | ns    |                 |
| TRHRL  | End of RD to Next Command                           | 160  |      | 160  |      | ns    |                 |
| TWHRL  | End of WR to Next Command                           | 190  |      | 190  |      | ns    |                 |

**Note:** 1. This is the low time required to clear the input latch in the edge triggered mode.

**TIMING RESPONSES**

**8259A-8**

**8259A**

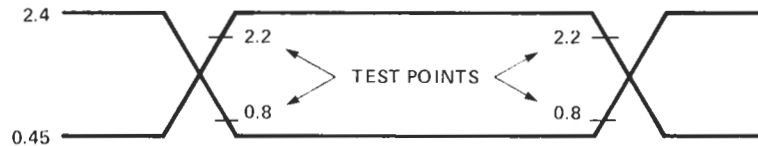
| Symbol | Parameter                                    | Min. | Max. | Min. | Max. | Units | Test Conditions                             |
|--------|--|------|------|------|------|-------|---|
| TRLDV  | Data Valid from RD/INTA↓                     |      | 300  |      | 200  | ns    | C of Data Bus = 100 pF                      |
| TRHDZ  | Data Float after RD/INTA↑                    | 20   | 200  |      | 100  | ns    | C of Data Bus                               |
| TJHIH  | Interrupt Output Delay                       |      | 400  |      | 350  | ns    | Max. test C = 100 pF<br>Min. test C = 15 pF |
| TIAHCV | Cascade Valid from First INTA↓ (Master Only) |      | 565  |      | 565  | ns    | C <sub>INT</sub> = 100 pF                   |
| TRLEL  | Enable Active from RD↓ or INTA↓              |      | 160  |      | 125  | ns    | C <sub>CASCADE</sub> = 100 pF               |
| TRHEH  | Enable Inactive from RD↑ or INTA↑            |      | 325  |      | 150  | ns    |   |
| TAHDV  | Data Valid from Stable Address               |      | 350  |      | 200  | ns    |   |
| TCVDV  | Cascade Valid to Valid Data                  |      | 300  |      | 300  | ns    |   |

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0V$

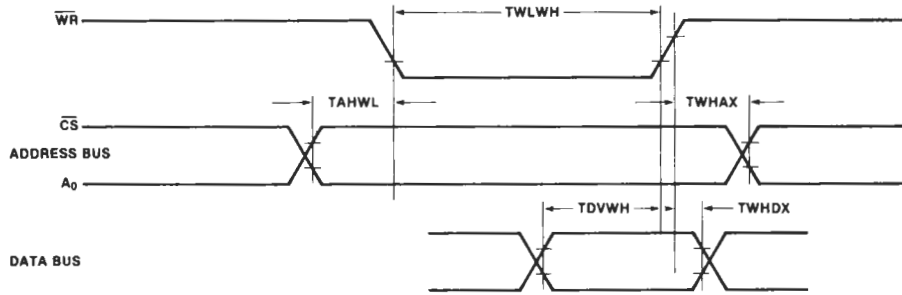
| Symbol           | Parameter         | Min. | Typ. | Max. | Unit | Test Conditions                             |
|------------------|-------------------|------|------|------|------|---|
| C <sub>IN</sub>  | Input Capacitance |      |      | 10   | pF   | f <sub>c</sub> = 1 MHz                      |
| C <sub>I/O</sub> | I/O Capacitance   |      |      | 20   | pF   | Unmeasured pins returned to V <sub>SS</sub> |

**Input Waveforms for A.C. Tests**

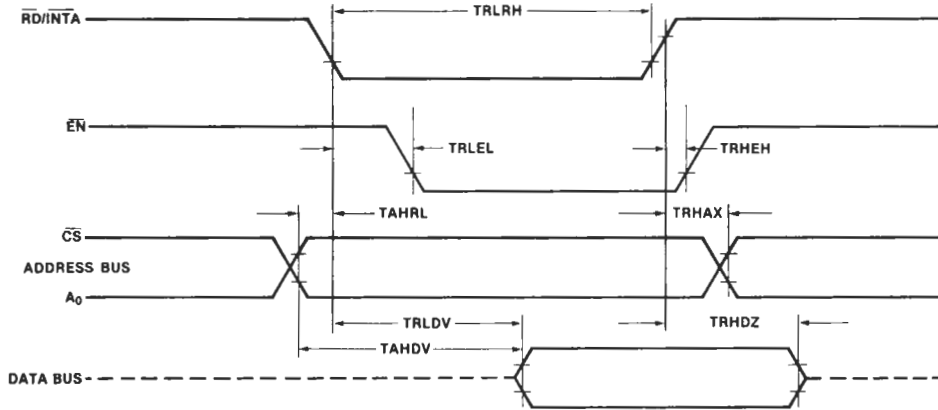


8259A

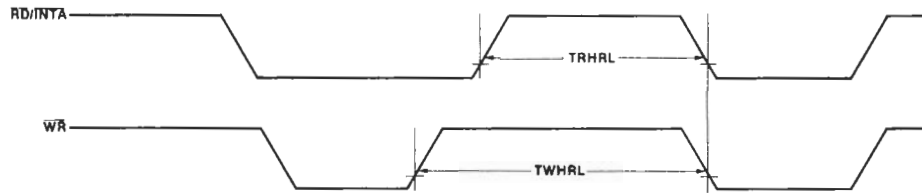
WRITE MODE



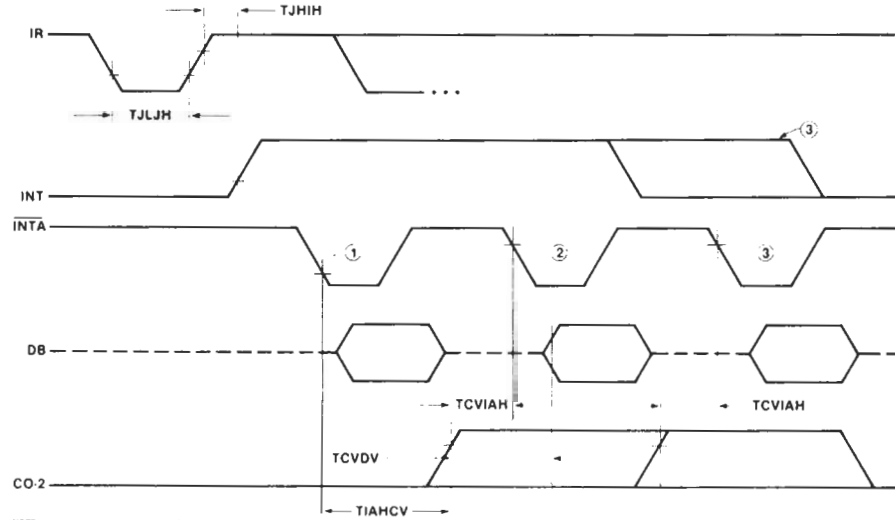
READ/INTA MODE



OTHER TIMING



INTA SEQUENCE



NOTE: Interrupt output must remain HIGH (at least) until leading edge of first INTA.  
 ① MCS 8085 Systems only.  
 ② Cycle 1 in MCS 86 Systems the Data Bus is not active.



### PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Micro-processing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

### ORDERING INFORMATION

| Speed                        | Device        | Temperature Range |
|------------------------------|---------------|-------------------|
| 1.0 MHz                      | MC6821P, L    | 0 to +70°C        |
|                              | MC6821CP, CL  | -40 to +85°C      |
| MIL-STD-883B<br>MIL-STD-883C | MC6821BQCS    | -55 to +125°C     |
|                              | MC6821CQCS    |                   |
| 1.5 MHz                      | MC68A21P, L   | 0 to +70°C        |
|                              | MC68A21CP, CL | -40 to +85°C      |
| 2.0 MHz                      | MC68B21P, L   | 0 to +70°C        |

**MC6821**

(1.0 MHz)

**MC68A21**

(1.5 MHz)

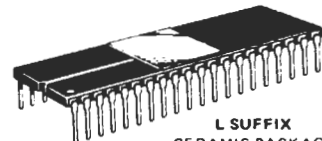
**MC68B21**

(2.0 MHz)

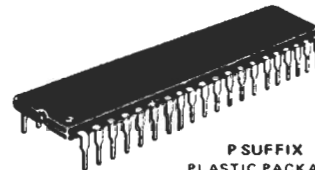
**MOS**

(N-CHANNEL, SILICON-GATE,  
DEPLETION LOAD)

**PERIPHERAL INTERFACE  
ADAPTER**



L SUFFIX  
CERAMIC PACKAGE  
CASE 715



P SUFFIX  
PLASTIC PACKAGE  
CASE 711

### PIN ASSIGNMENT

|    |     |       |    |
|----|-----|-------|----|
| 1  | O   | CA1   | 40 |
| 2  | VSS | CA2   | 39 |
| 3  | PA0 | IRQA  | 38 |
| 4  | PA1 | IRQB  | 37 |
| 5  | PA2 | RS0   | 36 |
| 6  | PA3 | RS1   | 35 |
| 7  | PA4 | Reset | 34 |
| 8  | PA5 | D0    | 33 |
| 9  | PA6 | D1    | 32 |
| 10 | PA7 | D2    | 31 |
| 11 | PB0 | D3    | 30 |
| 12 | PB1 | D4    | 29 |
| 13 | PB2 | D5    | 28 |
| 14 | PB3 | D6    | 27 |
| 15 | PB4 | D7    | 26 |
| 16 | PB5 | E     | 25 |
| 17 | PB6 | CS1   | 24 |
| 18 | PB7 | CS2   | 23 |
| 19 | CB1 | CS0   | 22 |
| 20 | CB2 | R/W   | 21 |

## MC6821

## MAXIMUM RATINGS

| Rating   | Symbol        | Value  | Unit                                      |
|--|---------------|--|---|
| Supply Voltage   | $V_{CC}$      | -0.3 to +7.0   | Vdc                                       |
| Input Voltage  | $V_{in}$      | -0.3 to +7.0   | Vdc                                       |
| Operating Temperature Range<br>MC6821, MC68A21, MC68B21<br>MC6821C, MC68A21C<br>MC6821CQCS, MC6821BQCS | $T_A$         | $T_L$ to $T_H$<br>0 to 70<br>-40 to 85<br>-55 to 125 | $^{\circ}C$<br>$^{\circ}C$<br>$^{\circ}C$ |
| Storage Temperature Range  | $T_{stg}$     | -55 to +150  | $^{\circ}C$                               |
| Thermal Resistance   | $\theta_{JA}$ | 82.5   | $^{\circ}C/W$                             |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance.

ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = T_L$  to  $T_H$  unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

BUS CONTROL INPUTS ( $R/\bar{W}$ , Enable, Reset, RS0, RS1, CS0, CS1, CS2)

|  |          |                |     |                |               |
|--|----------|----------------|-----|----------------|---------------|
| Input High Voltage   | $V_{IH}$ | $V_{SS} + 2.0$ | -   | $V_{CC}$       | Vdc           |
| Input Low Voltage  | $V_{IL}$ | $V_{SS} - 0.3$ | -   | $V_{SS} + 0.8$ | Vdc           |
| Input Leakage Current<br>( $V_{in} = 0$ to 5.25 Vdc)                         | $I_{in}$ | -              | 1.0 | 2.5            | $\mu\text{A}$ |
| Capacitance<br>( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0\text{ MHz}$ ) | $C_{in}$ | -              | -   | 7.5            | pF            |

INTERRUPT OUTPUTS ( $\bar{IROA}$ ,  $\bar{IROB}$ )

|  |           |   |     |                |               |
|--|-----------|---|-----|----------------|---------------|
| Output Low Voltage<br>( $I_{Load} = 3.2\text{ mA}$ )                         | $V_{OL}$  | - | -   | $V_{SS} + 0.4$ | Vdc           |
| Output Leakage Current (Off State)<br>( $V_{OH} = 2.4\text{ Vdc}$ )          | $I_{LOH}$ | - | 1.0 | 10             | $\mu\text{A}$ |
| Capacitance<br>( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0\text{ MHz}$ ) | $C_{out}$ | - | -   | 5.0            | pF            |

## DATA BUS (D0-D7)

|  |           |                |     |                |               |
|--|-----------|----------------|-----|----------------|---------------|
| Input High Voltage   | $V_{IH}$  | $V_{SS} + 2.0$ | -   | $V_{CC}$       | Vdc           |
| Input Low Voltage  | $V_{IL}$  | $V_{SS} - 0.3$ | -   | $V_{SS} + 0.8$ | Vdc           |
| Three-State (Off State) Input Current<br>( $V_{in} = 0.4$ to 2.4 Vdc)        | $I_{TSI}$ | -              | 2.0 | 10             | $\mu\text{A}$ |
| Output High Voltage<br>( $I_{Load} = -205\text{ }\mu\text{A}$ )              | $V_{OH}$  | $V_{SS} + 2.4$ | -   | -              | Vdc           |
| Output Low Voltage<br>( $I_{Load} = 1.6\text{ mA}$ )                         | $V_{OL}$  | -              | -   | $V_{SS} + 0.4$ | Vdc           |
| Capacitance<br>( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0\text{ MHz}$ ) | $C_{in}$  | -              | -   | 12.5           | pF            |

## PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)

|   |   |                                  |        |                |               |
|---|---|----------------------------------|--------|----------------|---------------|
| Input Leakage Current $R/\bar{W}$ , Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1, Enable<br>( $V_{in} = 0$ to 5.25 Vdc) | $I_{in}$  | -                                | 1.0    | 2.5            | $\mu\text{A}$ |
| Three-State (Off State) Input Current<br>( $V_{in} = 0.4$ to 2.4 Vdc)   | PB0-PB7, CB2<br>$I_{TSI}$                             | -                                | 2.0    | 10             | $\mu\text{A}$ |
| Input High Current<br>( $V_{IH} = 2.4\text{ Vdc}$ )   | PA0-PA7, CA2<br>$I_{IH}$                              | -200                             | -400   | -              | $\mu\text{A}$ |
| Darlington Drive Current<br>$V_O = 1.5\text{ Vdc}$  | PB0-PB7, CB2<br>$I_{OH}$                              | -1.0                             | -      | -10            | $\text{mA}$   |
| Input Low Current<br>( $V_{IL} = 0.4\text{ Vdc}$ )  | PA0-PA7, CA2<br>$I_{IL}$                              | -                                | -1.3   | -2.4           | $\text{mA}$   |
| Output High Voltage<br>( $I_{Load} = -200\text{ }\mu\text{A}$ )<br>( $I_{Load} = -10\text{ }\mu\text{A}$ )          | PA0-P7, PB0-PB7, CA2, CB2<br>PA0-PA7, CA2<br>$V_{OH}$ | $V_{SS} + 2.4$<br>$V_{CC} - 1.0$ | -<br>- | -<br>-         | Vdc           |
| Output Low Voltage<br>( $I_{Load} = 3.2\text{ mA}$ )  | $V_{OL}$  | -                                | -      | $V_{SS} + 0.4$ | Vdc           |
| Capacitance<br>( $V_{in} = 0$ , $T_A = 25^{\circ}C$ , $f = 1.0\text{ MHz}$ )  | $C_{in}$  | -                                | -      | 10             | pF            |

## POWER REQUIREMENTS

|                   |       |   |   |     |    |
|-------------------|-------|---|---|-----|----|
| Power Dissipation | $P_D$ | - | - | 550 | mW |
|-------------------|-------|---|---|-----|----|

MC6821

**BUS TIMING CHARACTERISTICS** ( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $T_A = T_L$  to  $T_H$  unless otherwise specified.)

| Characteristic  | Symbol           | MC6821 |     | MC68A21 |     | MC68B21 |     | Unit | Ref. Fig. No. |
|---|------------------|--------|-----|---------|-----|---------|-----|------|---------------|
|   |                  | Min    | Max | Min     | Max | Min     | Max |      |               |
| Enable Cycle Time   | $t_{cycE}$       | 1000   | —   | 666     | —   | 500     | —   | ns   | 1             |
| Enable Pulse Width, High  | $PW_{EH}$        | 450    | —   | 280     | —   | 220     | —   | ns   | 1             |
| Enable Pulse Width, Low   | $PW_{EL}$        | 430    | —   | 280     | —   | 210     | —   | ns   | 1             |
| Enable Pulse Rise and Fall Times                                | $t_{Er}, t_{Ef}$ | —      | 25  | —       | 25  | —       | 25  | ns   | 1             |
| Setup Time, Address and R/W valid to Enable positive transition | $t_{AS}$         | 160    | —   | 140     | —   | 70      | —   | ns   | 2, 3          |
| Address Hold Time   | $t_{AH}$         | 10     | —   | 10      | —   | 10      | —   | ns   | 2, 3          |
| Data Delay Time, Read   | $t_{DDR}$        | —      | 320 | —       | 220 | —       | 180 | ns   | 2, 4          |
| Data Hold Time, Read  | $t_{DHR}$        | 10     | —   | 10      | —   | 10      | —   | ns   | 2, 4          |
| Data Setup Time, Write  | $t_{DSW}$        | 195    | —   | 80      | —   | 60      | —   | ns   | 3, 4          |
| Data Hold Time, Write   | $t_{DHW}$        | 10     | —   | 10      | —   | 10      | —   | ns   | 3, 4          |

FIGURE 1 — ENABLE SIGNAL CHARACTERISTICS

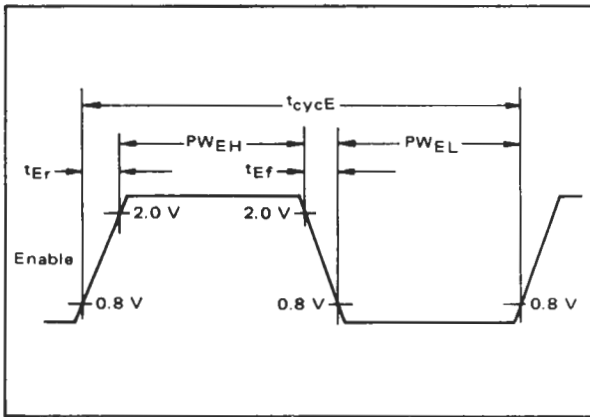


FIGURE 2 — BUS READ TIMING CHARACTERISTICS (Read Information from PIA)

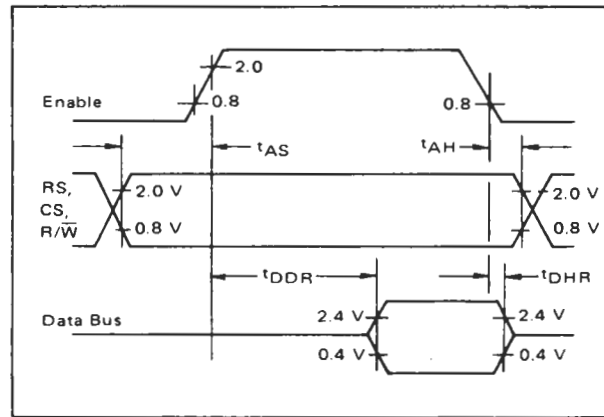


FIGURE 3 — BUS WRITE TIMING CHARACTERISTICS (Write Information into PIA)

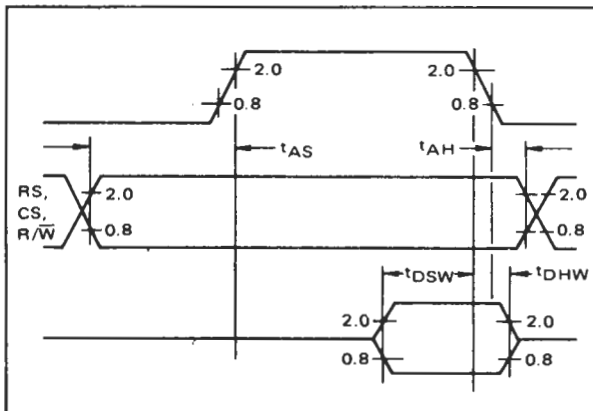
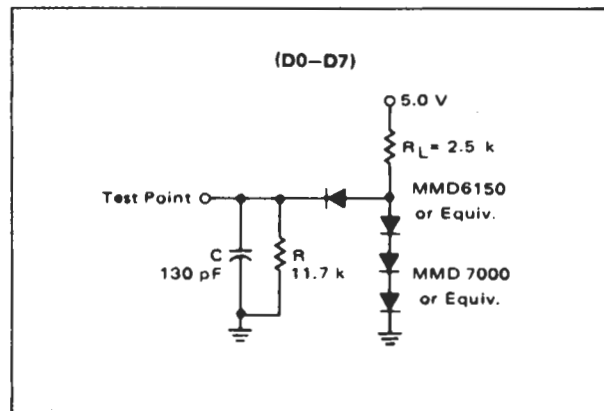


FIGURE 4 — BUS TIMING TEST LOADS





## MC6821

PERIPHERAL TIMING CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_A = T_L$  to  $T_H$  unless otherwise specified.)

| Characteristic  | Symbol     | MC6821 |      | MC68A21 |       | MC68B21 |       | Unit          | Reference Fig. No. |
|---|------------|--------|------|---------|-------|---------|-------|---------------|--------------------|
|   |            | Min    | Max  | Min     | Max   | Min     | Max   |               |                    |
| Peripheral Data Setup Time  | $t_{PDSU}$ | 200    | —    | 135     | —     | 100     | —     | ns            | 8                  |
| Peripheral Data Hold Time   | $t_{PDH}$  | 0      | —    | 0       | —     | 0       | —     | ns            | 8                  |
| Delay Time, Enable negative transition to CA2                                     | $t_{CA2}$  | —      | 1.0  | —       | 0.670 | —       | 0.500 | $\mu\text{s}$ | 5, 9, 10           |
| Delay Time, Enable negative transition to CA2                                     | $t_{RS1}$  | —      | 1.0  | —       | 0.670 | —       | 0.500 | $\mu\text{s}$ | 5, 9               |
| Rise and Fall Times for CA1 and CA2 input signals                                 | $t_r, t_f$ | —      | 1.0  | —       | 1.0   | —       | 1.0   | $\mu\text{s}$ | 5, 10              |
| Delay Time from CA1 active transition to CA2                                      | $t_{RS2}$  | —      | 2.0  | —       | 1.35  | —       | 1.0   | $\mu\text{s}$ | 5, 10              |
| Delay Time, Enable negative transition to Peripheral Data Valid                   | $t_{PDW}$  | —      | 1.0  | —       | 0.670 | —       | 0.5   | $\mu\text{s}$ | 5, 11, 12          |
| Delay Time, Enable negative transition to Peripheral CMOS Data Valid PA0-PA7, CA2 | $t_{CMOS}$ | —      | 2.0  | —       | 1.35  | —       | 1.0   | $\mu\text{s}$ | 6, 11              |
| Delay Time, Enable positive transition to CB2                                     | $t_{CB2}$  | —      | 1.0  | —       | 0.670 | —       | 0.5   | $\mu\text{s}$ | 5, 13, 14          |
| Delay Time, Peripheral Data Valid to CB2  | $t_{DC}$   | 20     | —    | 20      | —     | 20      | —     | ns            | 5, 12              |
| Delay Time, Enable positive transition to CB2                                     | $t_{RS1}$  | —      | 1.0  | —       | 0.670 | —       | 0.5   | $\mu\text{s}$ | 5, 13              |
| Peripheral Control Output Pulse Width, CA2/CB2                                    | $PW_{CT}$  | 550    | —    | 550     | —     | 500     | —     | ns            | 5, 13              |
| Rise and Fall Time for CB1 and CB2 input signals                                  | $t_r, t_f$ | —      | 1.0  | —       | 1.0   | —       | 1.0   | $\mu\text{s}$ | 14                 |
| Delay Time, CB1 active transition to CB2  | $t_{RS2}$  | —      | 2.0  | —       | 1.35  | —       | 1.0   | $\mu\text{s}$ | 5, 14              |
| Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$                   | $t_{IR}$   | —      | 1.60 | —       | 1.10  | —       | 0.85  | $\mu\text{s}$ | 7, 16              |
| Interrupt Response Time   | $t_{RS3}$  | —      | 1.0  | —       | 1.0   | —       | 1.0   | $\mu\text{s}$ | 7, 15              |
| Interrupt Input Pulse Width   | $PW_I$     | 500    | —    | 500     | —     | 500     | —     | ns            | 15                 |
| Reset Low Time*   | $t_{RL}$   | 1.0    | —    | 0.66    | —     | 0.5     | —     | $\mu\text{s}$ | 17                 |

\*The Reset line must be high a minimum of  $1.0 \mu\text{s}$  before addressing the PIA.

FIGURE 5 – TTL EQUIV. TEST LOAD

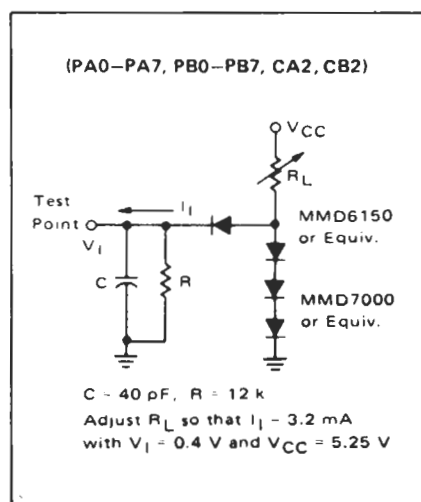


FIGURE 6 – CMOS EQUIV. TEST LOAD

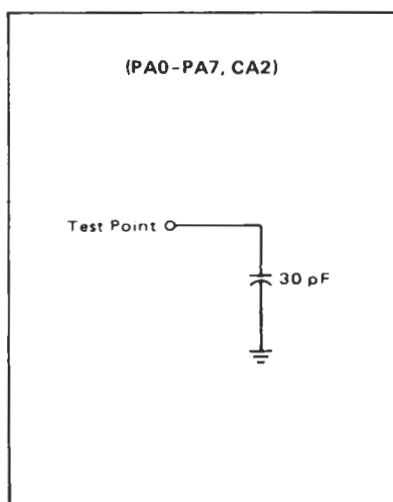
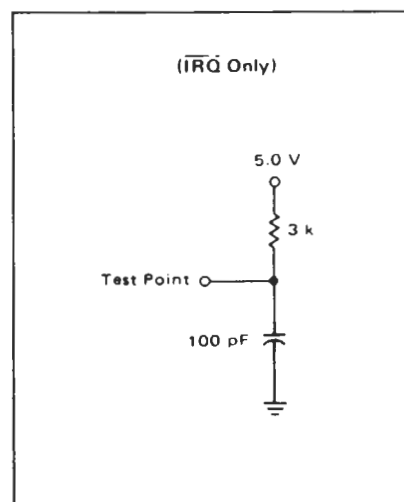


FIGURE 7 – NMOS EQUIV. TEST LOAD



MC6821

FIGURE 8 – PERIPHERAL DATA SETUP AND HOLD TIMES  
(Read Mode)

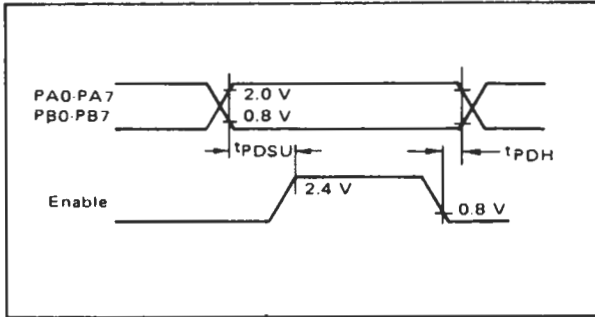


FIGURE 9 – CA2 DELAY TIME  
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

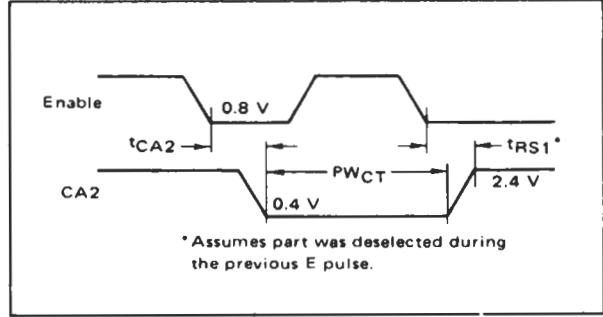


FIGURE 10 – CA2 DELAY TIME  
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

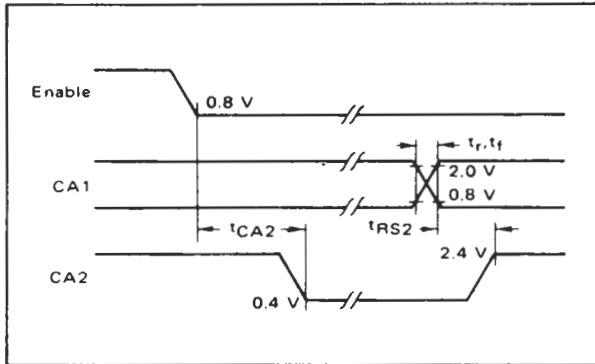


FIGURE 11 – PERIPHERAL CMOS DATA DELAY TIMES  
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

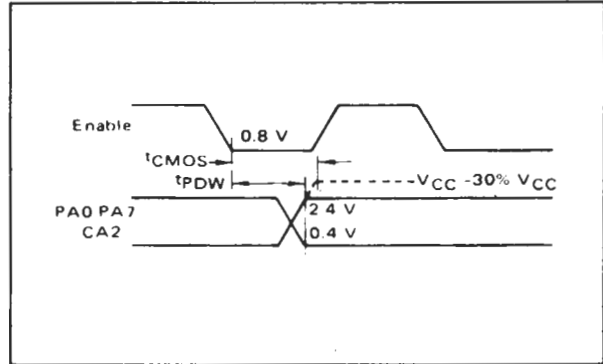


FIGURE 12 – PERIPHERAL DATA AND CB2 DELAY TIMES  
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

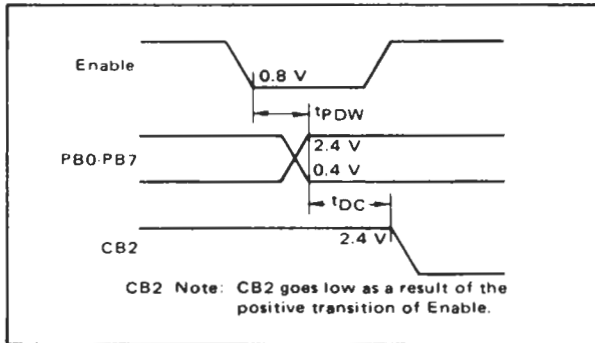


FIGURE 13 – CB2 DELAY TIME  
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

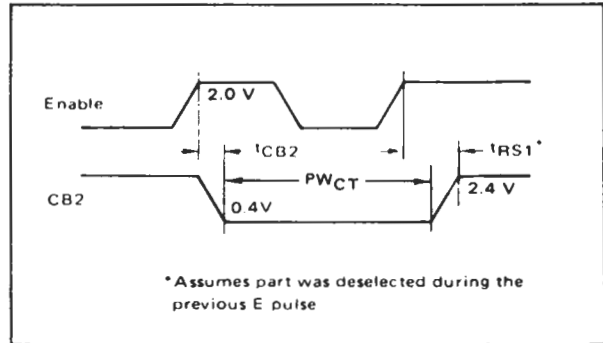


FIGURE 14 – CB2 DELAY TIME  
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)

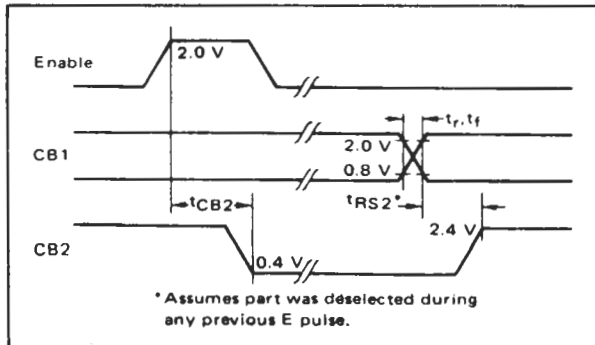
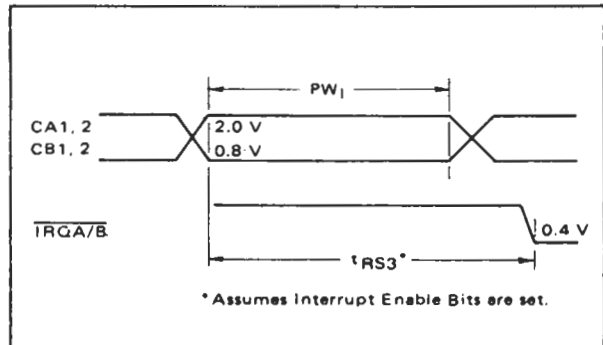


FIGURE 15 – INTERRUPT PULSE WIDTH AND  $\overline{TRQ}$  RESPONSE



MC6821

FIGURE 16 –  $\overline{\text{IRO}}$  RELEASE TIME

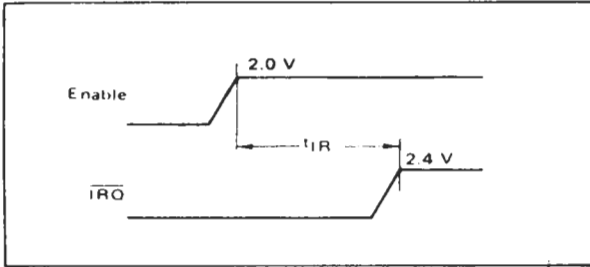
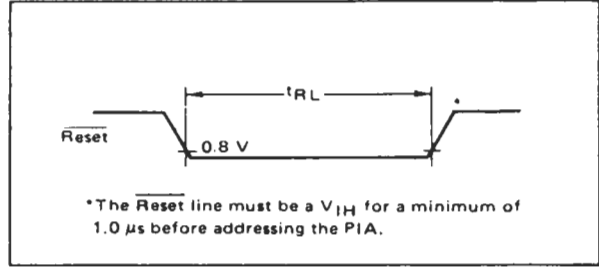
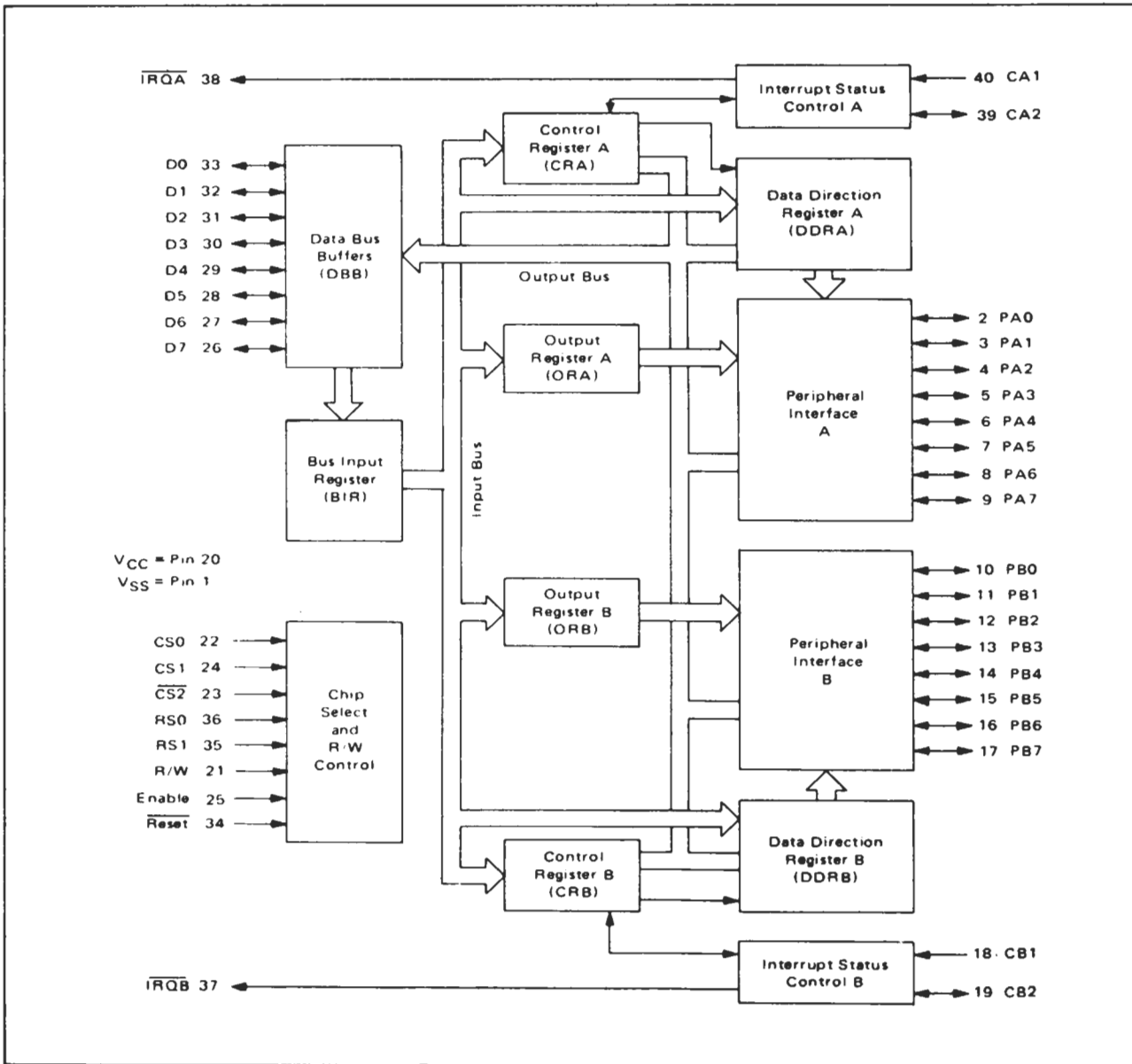


FIGURE 17 –  $\overline{\text{RESET}}$  LOW TIME



EXPANDED BLOCK DIAGRAM



**MC6821****PIA INTERFACE SIGNALS FOR MPU**

The PIA interfaces to the MC6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the PIA. VMA should be utilized in conjunction with an MPU address line into a chip select of the PIA.

**PIA Bi-Directional Data (D0-D7)** – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.

**PIA Enable (E)** – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800  $\phi 2$  Clock

**PIA Read/Write (R/W)** – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

**Reset** – The active low  $\overline{\text{Reset}}$  line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

**PIA Chip Select (CS0, CS1 and  $\overline{\text{CS2}}$ )** – These three input signals are used to select the PIA. CS0 and CS1 must be high and  $\overline{\text{CS2}}$  must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse. The device is

deselected when any of the chip selects are in the inactive state.

**PIA Register Select (RS0 and RS1)** – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

**Interrupt Request ( $\overline{\text{IRQA}}$  and  $\overline{\text{IRQB}}$ )** – The active low Interrupt Request lines ( $\overline{\text{IRQA}}$  and  $\overline{\text{IRQB}}$ ) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

**MC6821****PIA PERIPHERAL INTERFACE LINES**

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

**Section A Peripheral Data (PA0-PA7)** – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a “1” in the corresponding Data Direction Register bit for those lines which are to be outputs. A “0” in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical “1” written into the register will cause a “high” on the corresponding data line while a “0” results in a “low”. Data in Output Register A may be read by an MPU “Read Peripheral Data A” operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic “1” output and less than 0.8 volt for a logic “0” output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

**Section B Peripheral Data (PB0-PB7)** – The peripheral data lines in the B Section of the PIA can be programmed

to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a “high”. As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

**Interrupt Input (CA1 and CB1)** – Peripheral Input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

**Peripheral Control (CA2)** – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

**Peripheral Control (CB2)** – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

## MC6821

## INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

| RS1 | RS0 | Control Register Bit |       | Location Selected         |
|-----|-----|----------------------|-------|---------------------------|
|     |     | CRA-2                | CRB-2 |                           |
| 0   | 0   | 1                    | X     | Peripheral Register A     |
| 0   | 0   | 0                    | X     | Data Direction Register A |
| 0   | 1   | X                    | X     | Control Register A        |
| 1   | 0   | X                    | 1     | Peripheral Register B     |
| 1   | 0   | X                    | 0     | Data Direction Register B |
| 1   | 1   | X                    | X     | Control Register B        |

X = Don't Care

## INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

## DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

## CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

|     | 7     | 6     | 5           | 4 | 3 | 2           | 1           | 0 |
|-----|-------|-------|-------------|---|---|-------------|-------------|---|
| CRA | IRQA1 | IRQA2 | CA2 Control |   |   | DDRA Access | CA1 Control |   |
| CRB | IRQB1 | IRQB2 | CB2 Control |   |   | DDRB Access | CB1 Control |   |

**Data Direction Access Control Bit (CRA-2 and CRB-2)** – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

**Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7)** – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

| CRA-1 (CRB-1) | CRA-0 (CRB-0) | Interrupt Input CA1 (CB1) | Interrupt Flag CRA-7 (CRB-7) | MPU Interrupt Request IRQA (IRQB)                            |
|---------------|---------------|---------------------------|------------------------------|--|
| 0             | 0             | ↓ Active                  | Set high on ↓ of CA1 (CB1)   | Disabled — IRQ remains high                                  |
| 0             | 1             | ↓ Active                  | Set high on ↓ of CA1 (CB1)   | Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high |
| 1             | 0             | ↑ Active                  | Set high on ↑ of CA1 (CB1)   | Disabled — IRQ remains high                                  |
| 1             | 1             | ↑ Active                  | Set high on ↑ of CA1 (CB1)   | Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high |

Notes: 1 ↑ indicates positive transition (low to high)

2 ↓ indicates negative transition (high to low)

3 The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.

4 If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, IRQA (IRQB) occurs after CRA-0 (CRB-0) is written to a "one".

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**Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1)** – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are

used to enable the MPU interrupt signals  $\overline{IRQA}$  and  $\overline{IRQB}$ , respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

**TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS**  
CRA5 (CRB5) is low

| CRA-5 (CRB-5) | CRA-4 (CRB-4) | CRA-3 (CRB-3) | Interrupt Input CA2 (CB2) | interrupt Flag CRA-6 (CRB-6) | MPU Interrupt Request $\overline{IRQA}$ ( $\overline{IRQB}$ ) |
|---------------|---------------|---------------|---------------------------|------------------------------|---|
| 0             | 0             | 0             | ↓ Active                  | Set high on ↓ of CA2 (CB2)   | Disabled — $\overline{IRQ}$ remains high                      |
| 0             | 0             | 1             | ↓ Active                  | Set high on ↓ of CA2 (CB2)   | Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high  |
| 0             | 1             | 0             | * Active                  | Set high on * of CA2 (CB2)   | Disabled — $\overline{IRQ}$ remains high                      |
| 0             | 1             | 1             | ↑ Active                  | Set high on ↑ of CA2 (CB2)   | Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high  |

- Notes. 1 ↑ indicates positive transition (low to high)  
 2 ↓ indicates negative transition (high to low)  
 3 The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register  
 4 If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high,  $\overline{IRQA}$  ( $\overline{IRQB}$ ) occurs after CRA-3 (CRB-3) is written to a "one".

**TABLE 5 – CONTROL OF CB2 AS AN OUTPUT**  
CRB-5 is high

| CRB-5 | CRB-4 | CRB-3 | CB2   |   |
|-------|-------|-------|---|---|
|       |       |       | Cleared   | Set   |
| 1     | 0     | 0     | Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation                          | High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal                               |
| 1     | 0     | 1     | Low on the positive transition of the first E pulse after an MPU Write "B" Data Register operation.                             | High on the positive edge of the first "E" pulse following an "E" pulse which occurred while the part was deselected. |
| 1     | 1     | 0     | Low when CRB-3 goes low as a result of an MPU Write in Control Register B.  | Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register B that changes CRB-3 to one.     |
| 1     | 1     | 1     | Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to zero. | High when CRB-3 goes high as a result of an MPU Write into Control Register "B".                                      |

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**Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5)** – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5)

is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

**TABLE 6 – CONTROL OF CA-2 AS AN OUTPUT**  
CRA-5 is high

| CRA-5 | CRA-4 | CRA-3 | Cleared  | Set   |
|-------|-------|-------|--|---|
| 1     | 0     | 0     | Low on negative transition of E after an MPU Read "A" Data operation.  | High when the interrupt flag bit CRA-7 is set by an active transition of the CA1 signal.                              |
| 1     | 0     | 1     | Low on negative transition of E after an MPU Read "A" Data operation.  | High on the negative edge of the first "E" pulse which occurs during a deselect.                                      |
| 1     | 1     | 0     | Low when CRA-3 goes low as a result of an MPU Write to Control Register "A".   | Always low as long as CRA-3 is low. Will go high on an MPU Write to Control Register "A" that changes CRA-3 to "one". |
| 1     | 1     | 1     | Always high as long as CRA-3 is high. Will be cleared on an MPU Write to Control Register "A" that clears CRA-3 to a "zero". | High when CRA-3 goes high as a result of an MPU Write to Control Register "A".  |

**PACKAGE DIMENSIONS**

**CASE 711-01**  
PLASTIC

| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| A   | 51.82       | 52.32 | 2.040  | 2.060 |
| B   | 13.72       | 14.22 | 0.540  | 0.560 |
| C   | 4.57        | 5.08  | 0.180  | 0.200 |
| D   | 0.36        | 0.51  | 0.014  | 0.020 |
| F   | 1.02        | 1.52  | 0.040  | 0.060 |
| G   | 2.41        | 2.67  | 0.095  | 0.105 |
| H   | 1.65        | 2.16  | 0.065  | 0.085 |
| J   | 0.20        | 0.30  | 0.008  | 0.012 |
| K   | 3.68        | 4.19  | 0.145  | 0.165 |
| L   | 14.99       | 15.49 | 0.590  | 0.610 |
| M   | 0°          | 10°   | 0°     | 10°   |
| N   | 0.51        | 1.02  | 0.020  | 0.040 |

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**CASE 715-02**  
CERAMIC

**NOTE:**  
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 50.29       | 51.31 | 1.980     | 2.020 |
| B   | 14.86       | 15.62 | 0.585     | 0.615 |
| C   | 2.54        | 4.19  | 0.100     | 0.165 |
| D   | 0.38        | 0.53  | 0.015     | 0.021 |
| F   | 0.76        | 1.40  | 0.030     | 0.055 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.76        | 1.78  | 0.030     | 0.070 |
| J   | 0.20        | 0.33  | 0.008     | 0.013 |
| K   | 2.54        | 4.19  | 0.100     | 0.165 |
| L   | 14.60       | 15.37 | 0.575     | 0.605 |
| M   | –           | 10°   | –         | 10°   |
| N   | 0.51        | 1.52  | 0.020     | 0.060 |



## 96S02 • 96LS02

## 96S02 96LS02

### DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

**DESCRIPTION** — The 96S02 and 96LS02 are dual retriggerable and resettable monostable multivibrators. These one-shots provide exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 M $\Omega$  for the 96LS02 and 2.0 M $\Omega$  for the 96S02 reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 and on the positive trigger input of the 96S02 for increased noise immunity.

- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.0 k $\Omega$  to 2.0 M $\Omega$**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 2000:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns 96LS02, 12 ns 96S02**
- **0.3 V HYSTERESIS ON TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO  $\infty$  OUTPUT PULSE WIDTH RANGE**

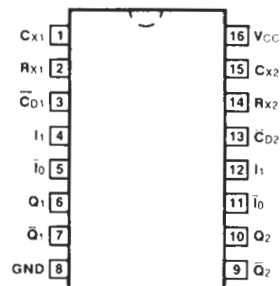
**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE   | MILITARY GRADE   | PKG TYPE |
|-----------------|---------|--|--|----------|
|                 |         | $V_{CC} = +5.0 \text{ V} \pm 5\%$ ,<br>$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | $V_{CC} = +5.0 \text{ V} \pm 10\%$ ,<br>$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ |          |
| Plastic DIP (P) | A       | 96S02PC, 96LS02PC  |  | 9B       |
| Ceramic DIP (D) | A       | 96S02DC, 96LS02DC  | 96S02DM, 96LS02DM  | 6B       |
| Flatpak (F)     | A       | 96S02FC, 96LS02FC  | 96S02FM, 96LS02FM  | 4L       |

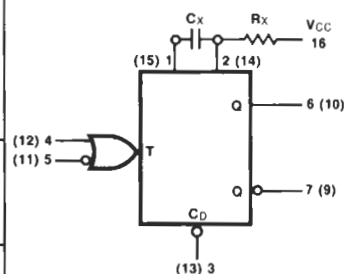
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES   | DESCRIPTION                                 | 96S (U.L.) HIGH/LOW | 96LS (U.L.) HIGH/LOW |
|-------------|---|---------------------|----------------------|
| $\bar{I}_0$ | Trigger Input (Active Falling Edge)         | 0.5/0.625           |                      |
| $\bar{I}_0$ | Schmitt Trigger Input (Active Falling Edge) |                     | 0.5/0.25             |
| $I_1$       | Schmitt Trigger Input (Active Rising Edge)  | 0.5/0.625           | 0.5/0.25             |
| $\bar{C}_D$ | Direct Clear Input (Active LOW)             | 0.5/0.625           | 0.5/0.25             |
| Q           | True Pulse Output                           | 25/12.5             | 10/5.0<br>(2.5)      |
| $\bar{Q}$   | Complementary Pulse Output                  | 25/12.5             | 10/5.0<br>(2.5)      |

#### CONNECTION DIAGRAM PINOUT A

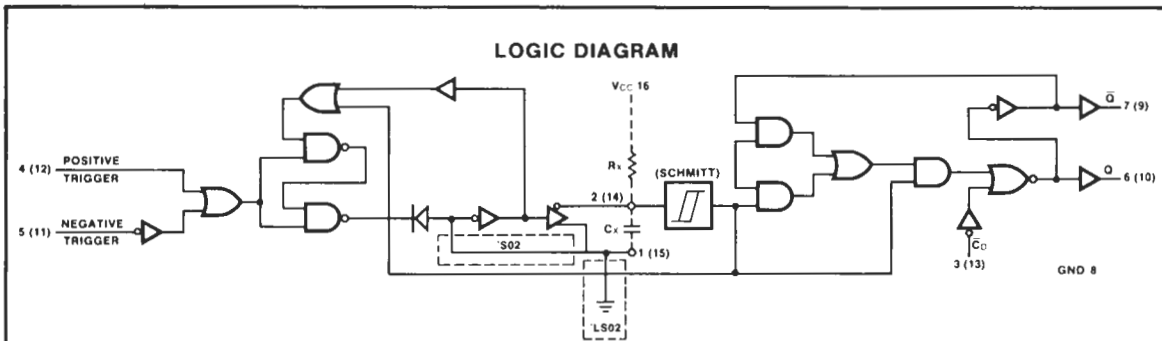


#### LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$   
 $GND = \text{Pin } 8$

## 96S02 • 96LS02



**FUNCTIONAL DESCRIPTION** — The 96S02 and 96LS02 dual retriggerable resettable monostable multivibrators have two dc coupled trigger inputs per function, one active LOW ( $\bar{I}_0$ ) and one active HIGH ( $I_1$ ). The  $I_1$  input of both circuit types and the  $\bar{I}_0$  input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggerring may be inhibited by tying the  $\bar{Q}$  output to  $\bar{I}_0$  or the Q output to  $I_1$ . Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

**Operation Notes****TIMING**

1. An external resistor ( $R_x$ ) and an external capacitor ( $C_x$ ) are required as shown in the Logic Diagram. The value of  $R_x$  may vary from 1.0 k $\Omega$  to 1.0 M $\Omega$  (96LS02) or 2.0 M $\Omega$  (96S02).
2. The value of  $C_x$  may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to  $V_{CC}/R_x$  the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (-) terminal to pin 2 (14) and  $R_x$ . Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle. In the 96S02, however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to pin 2 (14) depending on values of  $R_x$  and  $V_{CC}$ . For values of  $R_x \geq 10$  k $\Omega$  the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the 96S02 when  $R_x \geq 10$  k $\Omega$ .
4. The output pulse width  $t_w$  for  $R_x \geq 10$  k $\Omega$  and  $C_x \geq 1000$  pF is determined as follows:
 

|          |                      |
|----------|----------------------|
| (96S02)  | $t_w = 0.55 R_x C_x$ |
| (96LS02) | $t_w = 0.43 R_x C_x$ |

 Where  $R_x$  is in k $\Omega$ ,  $C_x$  is in pF,  $t$  is in ns or  $R_x$  is in k $\Omega$ ,  $C_x$  is in  $\mu$ F,  $t$  is in ms.
5. The output pulse width for  $R_x < 10$  k $\Omega$  or  $C_x < 1000$  pF should be determined from pulse width versus  $C_x$  or  $R_x$  graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



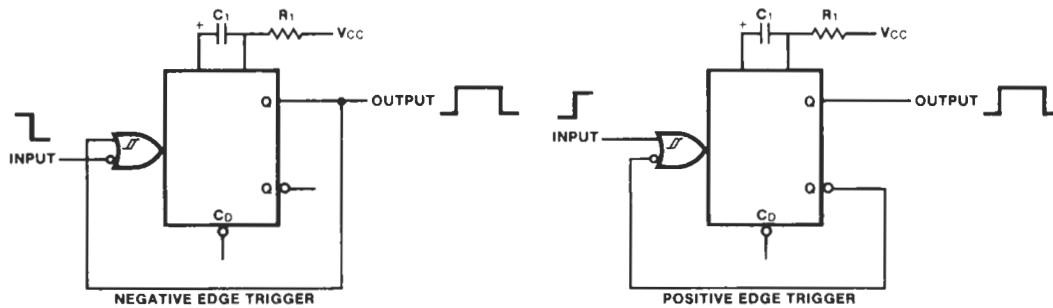
## 96S02 • 96LS02

### Operation Notes (Cont'd)

- Under any operating condition,  $C_X$  and  $R_X$  (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
- $V_{CC}$  and ground wiring should conform to good high frequency standards so that switching transients on  $V_{CC}$  and ground leads do not cause interaction between one shots. Use of a  $0.01 \mu\text{F}$  to  $0.1 \mu\text{F}$  bypass capacitor between  $V_{CC}$  and ground located near the circuit is recommended.

### TRIGGERING

- The minimum negative pulse width into  $\bar{I}_0$  is 8.0 ns; the minimum positive pulse width into  $I_1$  is 12 ns.
- Input signals to the 96S02 exhibiting slow or noisy transitions should use the positive trigger input  $I_1$  which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
- When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



- An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on  $\bar{C}_D$  will not trigger the 96S02 or 96LS02. If the  $\bar{C}_D$  input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

TRIGGERING TRUTH TABLE

| PIN NO'S. |        |        | OPERATION |
|-----------|--------|--------|-----------|
| 5 (11)    | 4 (12) | 3 (13) |           |
| H→L       | L      | H      | Trigger   |
| H         | L→H    | H      | Trigger   |
| X         | X      | L      | Reset     |

H = HIGH Voltage Level  $\geq V_{IH}$

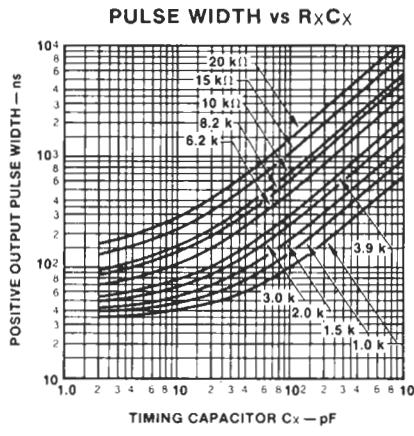
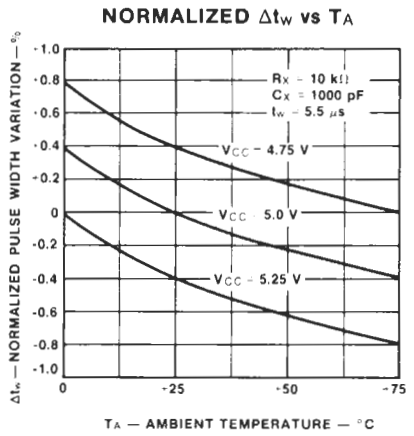
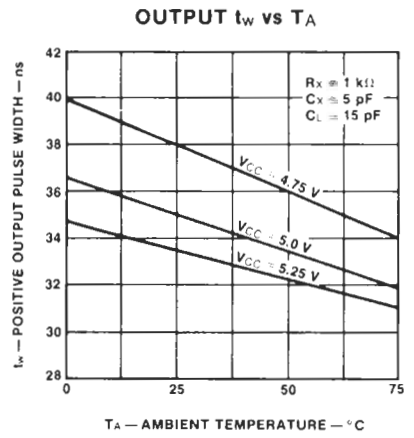
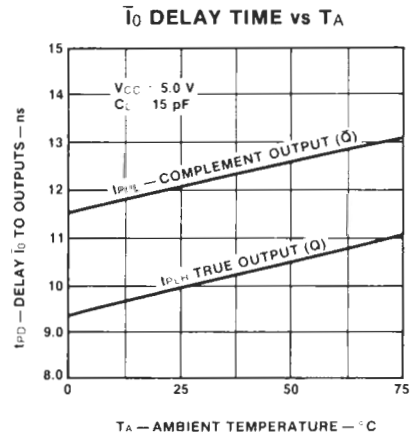
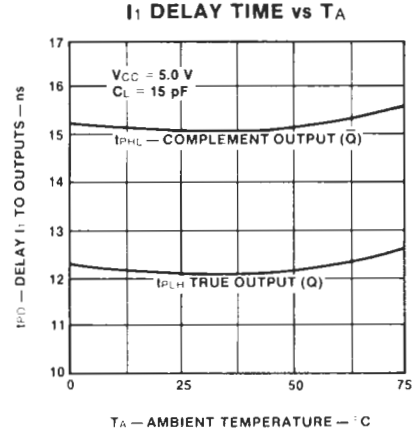
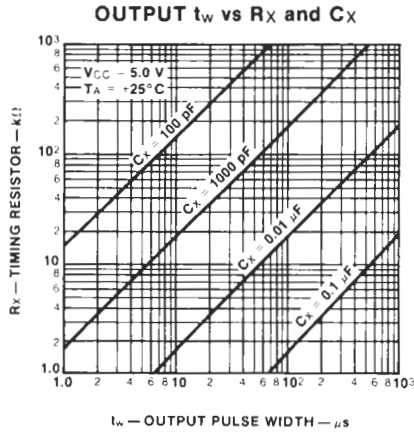
L = LOW Voltage Level  $\leq V_{IL}$

X = Immaterial (either H or L)

H→L = HIGH to LOW Voltage Level transition

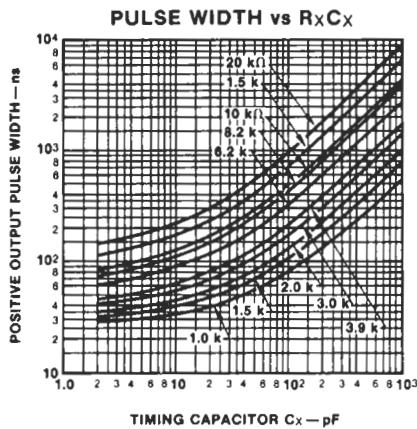
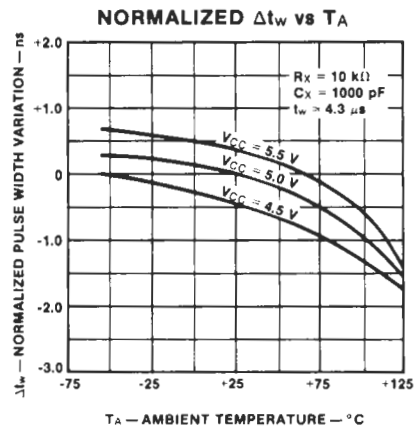
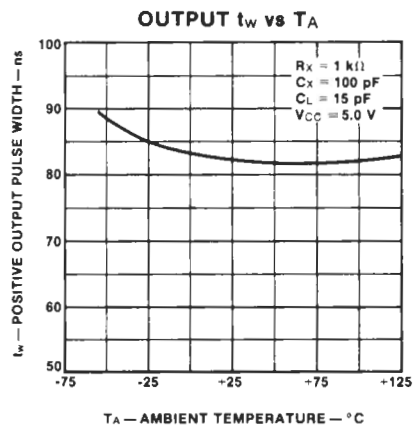
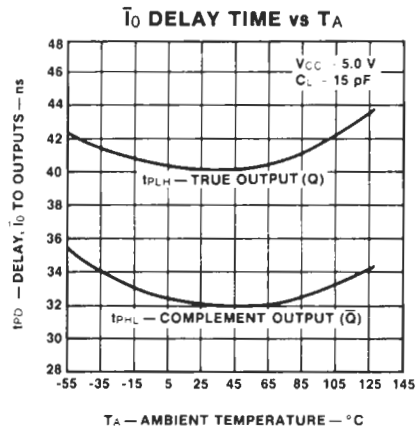
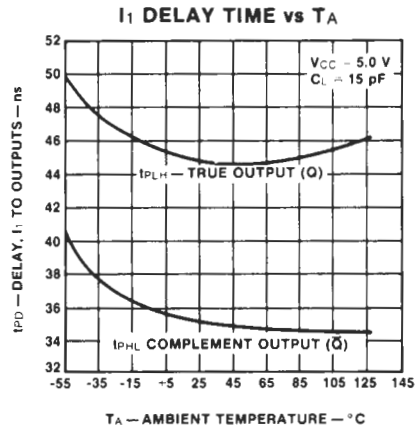
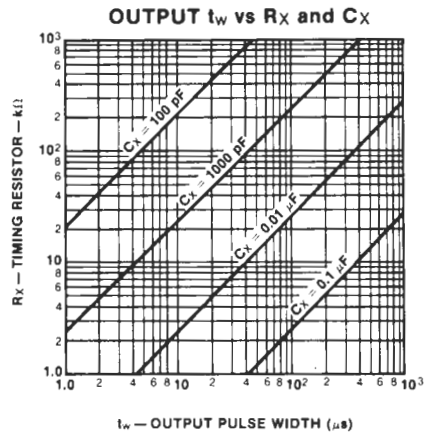
L→H = LOW to HIGH Voltage Level transition

TYPICAL CHARACTERISTICS  
96S02



96S02 • 96LS02

TYPICAL CHARACTERISTICS  
96LS02



96S02 • 96LS02

| DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified) |  |       |      |      |      |   |  |
|--|--|-------|------|------|------|---|--|
| SYMBOL   | PARAMETER  | 96S   |      | 96LS |      | UNITS   | CONDITIONS   |
|  |  | Min   | Max  | Min  | Max  |   |  |
| $V_{T+}$   | Positive-going Threshold Voltage, $\bar{I}_0$ , $I_1$ (96LS02) $I_1$ (96S02) | 2.0   |      | 2.0  |      | V   | $V_{CC} = 5.0$ V   |
| $V_{T-}$   | Negative-going Threshold Voltage $\bar{I}_0$ , $I_1$ (96LS02) $I_1$ (96S02)  | XM    | 0.8  | 0.7  | V    | $V_{CC} = 5.0$ V  |  |
|  |  | XC    | 0.8  | 0.8  |      |   |  |
| $V_{OH}$   | Output HIGH Voltage  | XM    | 2.7  | 2.5  | V    | $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH} = -400 \mu\text{A}$ ('LS02)<br>$I_{OH} = -1.0 \text{ mA}$ ('S02) |  |
|  |  | XC    | 2.7  | 2.7  |      |   |  |
| $V_{OL}$   | Output LOW Voltage   | XM    | 0.5  | 0.5  | V    | $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$   |  |
|  |  | XC    | 0.5  | 0.4  |      |   |  |
| $V_{CX}$   | Capacitor Voltage<br>Pin 1 (15) Referenced to Pin 2 (14)                     | -0.85 | 3.0  | 0    | 3.0  | V   | $R_x = 1.0 \text{ k}\Omega$ $V_{CC} = 4.75$ V<br>$R_x = > 10 \text{ k}\Omega$ to 5.25 V<br>$R_x > 1.0 \text{ M}\Omega$ |
| $I_{IH}$   | Input HIGH Current   | 20    |      | 20   |      | $\mu\text{A}$   | $V_{IN} = 2.7$ V<br>$V_{IN} = 5.5$ V ('S02) $V_{CC} = \text{Max}$<br>$V_{IN} = 10$ V ('LS02)                           |
|  |  | 0.1   |      | 0.1  |      | mA  |  |
| $I_{IL}$   | Input LOW Current  | -1.0  |      | -0.4 |      | mA  | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$  |
| $I_{OS}$   | Output Short Circuit Current   | -40   | -100 | -20  | -100 | mA  | $V_{CC} = \text{Max}$ , $V_{OUT} = 0$ V  |
| $I_{CC}$   | Power Supply Current   | 75    |      | 36   |      | mA  | $V_{IN} = \text{Open}$ , $V_{CC} = \text{Max}$   |

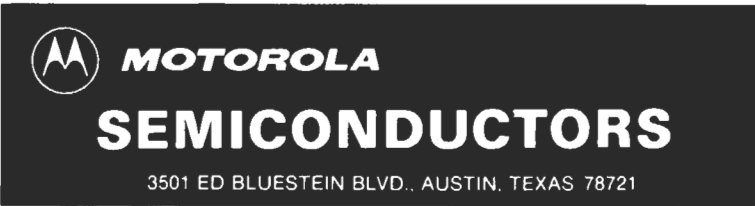
The diagram shows an input pulse  $V_{IN}$  with a width of 100 ns and a peak of 1.5 V. The output signals  $Q$  and  $\bar{Q}$  are shown with propagation delays  $t_{PLH}$  and  $t_{PHL}$  and a pulse width  $t_w$ . The output levels are also marked as 1.5 V.

Fig. a

**96S02 • 96LS02**

| AC CHARACTERISTICS: $V_{CC} = +5.0\text{ V}$ , $T_A = +25^\circ\text{C}$ (See Section 3 for waveforms and load configurations) |  |                      |      |                      |      |                  |  |
|--|--|----------------------|------|----------------------|------|------------------|--|
| SYMBOL   | PARAMETER                                      | 96S                  |      | 96LS                 |      | UNITS            | CONDITIONS   |
|  |  | $C_L = 15\text{ pF}$ |      | $C_L = 15\text{ pF}$ |      |                  |  |
|  |  | Min                  | Max  | Min                  | Max  |                  |  |
| $t_{PLH}$  | Propagation Delay<br>$\bar{I}_0$ to Q          | 15                   |      | 55                   |      | ns               | Fig. a   |
| $t_{PHL}$  | Propagation Delay<br>$\bar{I}_0$ to $\bar{Q}$  | 19                   |      | 50                   |      | ns               |  |
| $t_{PLH}$  | Propagation Delay<br>$I_1$ to Q                | 19                   |      | 60                   |      | ns               |  |
| $t_{PHL}$  | Propagation Delay<br>$I_1$ to $\bar{Q}$        | 20                   |      | 55                   |      | ns               |  |
| $t_{PHL}$  | Propagation Delay<br>$\bar{C}_D$ to Q          | 20                   |      | 30                   |      | ns               |  |
| $t_{PLH}$  | Propagation Delay<br>$\bar{C}_D$ to $\bar{Q}$  | 14                   |      | 35                   |      | ns               |  |
| $t_w$ (L)  | $\bar{I}_0$ Pulse Width LOW                    | 8.0                  |      | 15                   |      | ns               |  |
| $t_w$ (H)  | $I_1$ Pulse Width HIGH                         | 12                   |      | 30                   |      | ns               |  |
| $t_w$ (L)  | $\bar{C}_D$ Pulse Width LOW                    | 7.0                  |      | 22                   |      | ns               |  |
| $t_w$ (H)  | Minimum Q Pulse Width HIGH                     | 30                   | 45   | 25                   | 55   | ns               | $R_X = 1.0\text{ k}\Omega$ , $C_X = 10\text{ pF}$<br>including jig and stray   |
| $t_w$  | Q Pulse Width                                  | 5.2                  | 5.8  | 4.1                  | 4.5  | $\mu\text{s}$    | $R_X = 10\text{ k}\Omega$ , $C_X = 1000\text{ pF}$   |
| $R_X$  | Timing Resistor Range*                         | 1.0                  | 2000 | 1.0                  | 1000 | $\text{k}\Omega$ | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ ,<br>$V_{CC} = 4.5\text{ V}$ to $5.5\text{ V}$   |
| t  | Change in Q Pulse Width<br>over Temperature    | XM                   |      | 3.0                  |      | %                | $R_X = 10\text{ k}\Omega$ , $C_X = 1000\text{ pF}$   |
|  |  | XC                   |      | 1.0                  |      |                  |  |
| t  | Change in Q Pulse Width<br>over $V_{CC}$ Range | 1.0                  |      | 0.8                  |      | %                | $T_A = 25^\circ\text{C}$ , $V_{CC} = 4.75\text{ V}$ to<br>$5.25\text{ V}$ , $R_X = 10\text{ k}\Omega$ ,<br>$C_X = 1000\text{ pF}$<br>$T_A = 25^\circ\text{C}$ , $V_{CC} = 4.5\text{ V}$ to<br>$5.5\text{ V}$ , $R_X = 10\text{ k}\Omega$ ,<br>$C_X = 1000\text{ pF}$ |
|  |  |                      |      | 1.5                  |      |                  |  |

\*Applies only over commercial  $V_{CC}$  and  $T_A$  range for 96S02.



**Advance Information**

**ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI)**

The MC2661/MC68661, Enhanced Programmable Communications Interface (EPCI), is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the Signetics 2651. The EPCI directly interfaces to most 8-bit MPUs and easily to the MC68000 MPU and other 16-bit MPUs. It may be used in either a polled or interrupt driven system. Programmed instructions can be accepted from the host MPU while supporting many synchronous or asynchronous serial-data communication protocols in a full or half-duplex mode. Special support for BISYNC is provided.

The EPCI converts parallel data characters, accepted from the microprocessor data bus, into transmit-serial data. Simultaneously, the EPCI can convert receive-serial data to parallel data characters for input to the microprocessor.

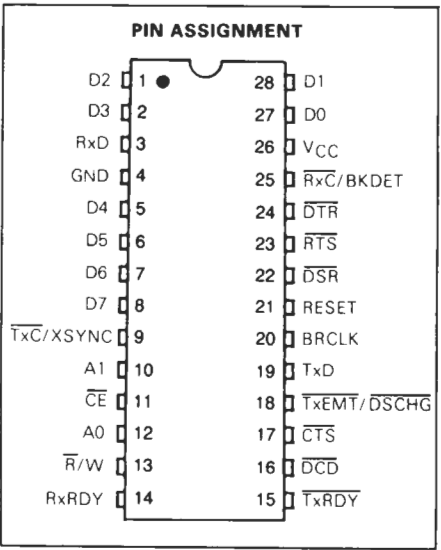
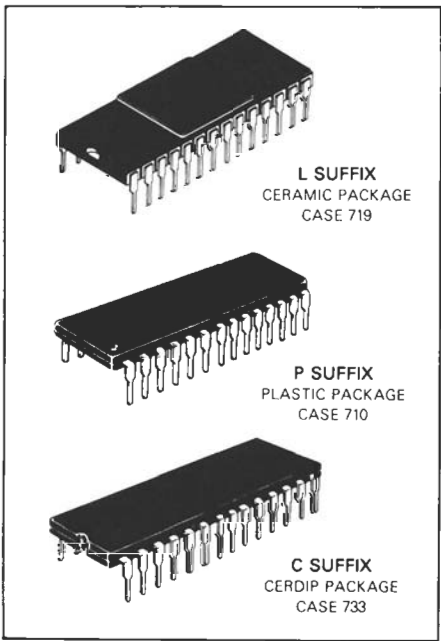
A baud rate generator in the EPCI can be programmed to either accept an external clock, or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

**FEATURES**

- **Synchronous Operation**
  - Single or Double SYN Operation
  - Internal or External Character Synchronization
  - Transparent or Non-transparent Mode
  - Transparent Mode DLE Stuffing (Tx) and Detection (Rx)
  - Automatic SYN or DLE-SYN Insertion
  - SYN, DLE, and DLE-SYN Stripping
  - Baud Rate: dc to 1M bps (1X Clock)
- **Asynchronous Operation**
  - 1, 1½, or 2 Stop Bits Transmitted
  - Parity, Overrun, and Framing Error Detection
  - Line Break Detection and Generation
  - False Start Bit Detection
  - Automatic Serial Echo Mode (Echoplex)
  - Baud Rate: dc 1M bps (1X Clock)
    - dc to 62.5k bps (16X Clock)
    - dc to 15.625k bps (64X Clock)
- **Common Features**
  - Internal or External Baud Rate Clock; No System Clock Required
  - 3 Baud Rate Sets (A, B, C); 16 Internal Rates for Each Set
  - 5- to 8-Bit Characters plus parity, Odd, Even, or No Parity
  - Double Buffered Transmitter and Receiver
  - Dynamic Character Length Switching
  - Full- or Half-Duplex Operation
  - Local or Remote Maintenance Loop-Back Mode
  - TTL-Compatible Inputs and Outputs
  - RxC and TxC Pins and Short Circuit Protected
  - 3 Open-Drain MOS Outputs can be Wire ORed
  - Single 5 V Power Supply
- **Applications**
  - Intelligent Terminals
  - Network Processors
  - Front End Processors
  - Remote Data Concentrators
  - Computer-to-Computer Links
  - Serial Peripherals
  - BISYNC Adaptors

**MC2661A/MC68661A**  
(Baud Rate Set A)  
**MC2661B/MC68661B**  
(Baud Rate Set B)  
**MC2661C/MC68661C**  
(Baud Rate Set C)

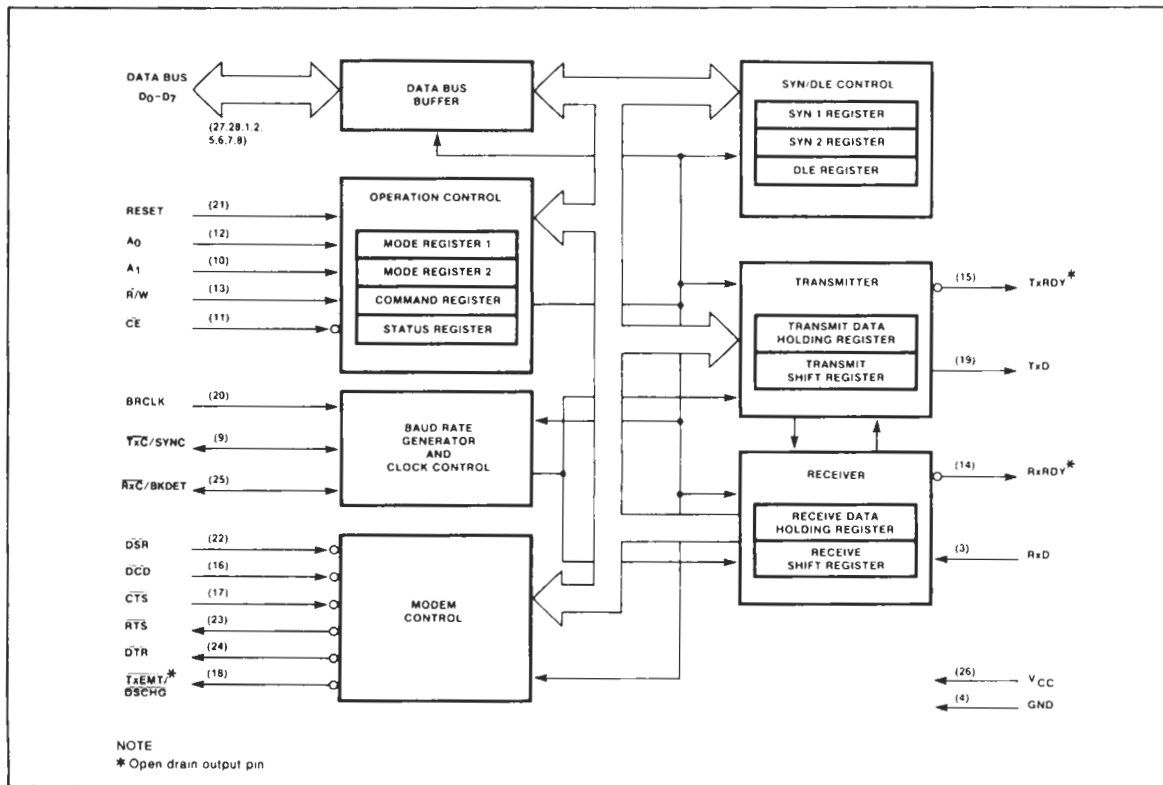
**MOS**  
(N-CHANNEL, SILICON-GATE)  
**ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI)**





## MC2661A,B,C/MC68661A,B,C

## BLOCK DIAGRAM



## BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

## Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

Table 1 BAUD RATE GENERATOR CHARACTERISTICS  
Set A (BRCLK = 4.9152MHz)

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY<br>16X CLOCK | PERCENT ERROR | DIVISOR |
|---------|-----------|-------------------------------|---------------|---------|
| 0000    | 50        | 0.8kHz                        | -             | 6144    |
| 0001    | 75        | 1.2                           | -             | 4096    |
| 0010    | 110       | 1.7598                        | -0.01         | 2793    |
| 0011    | 134.5     | 2.152                         | -             | 2284    |
| 0100    | 150       | 2.4                           | -             | 2048    |
| 0101    | 200       | 3.2                           | -             | 1536    |
| 0110    | 300       | 4.8                           | -             | 1024    |
| 0111    | 600       | 9.6                           | -             | 512     |
| 1000    | 1050      | 16.8329                       | 0.196         | 292     |
| 1001    | 1200      | 19.2                          | -             | 256     |
| 1010    | 1800      | 28.7438                       | -0.19         | 171     |
| 1011    | 2000      | 31.9168                       | -0.26         | 154     |
| 1100    | 2400      | 38.4                          | -             | 128     |
| 1101    | 4800      | 76.8                          | -             | 64      |
| 1110    | 9600      | 153.6                         | -             | 32      |
| 1111    | 19200     | 307.2                         | -             | 16      |



**MC2661A,B,C/MC68661A,B,C**

**Timing**

The EPC1 contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See table 1.

**Receiver**

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

**Transmitter**

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

**Modem Control**

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

**SYN/DLE Control**

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

**Table 1 BAUD RATE GENERATOR CHARACTERISTICS (Cont'd)**  
**Set B (BRCLK = 4.9152MHz)**

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY<br>16X CLOCK | PERCENT ERROR | DIVISOR |
|---------|-----------|-------------------------------|---------------|---------|
| 0000    | 45.5      | 0.7279kHz                     | 0.005         | 6752    |
| 0001    | 50        | 0.8                           | -             | 6144    |
| 0010    | 75        | 1.2                           | -             | 4096    |
| 0011    | 110       | 1.7598                        | -0.01         | 2793    |
| 0100    | 134.5     | 2.152                         | -             | 2284    |
| 0101    | 150       | 2.4                           | -             | 2048    |
| 0110    | 300       | 4.8                           | -             | 1024    |
| 0111    | 600       | 9.6                           | -             | 512     |
| 1000    | 1200      | 19.2                          | -             | 256     |
| 1001    | 1800      | 28.7438                       | -0.19         | 171     |
| 1010    | 2000      | 31.9168                       | -0.26         | 154     |
| 1011    | 2400      | 38.4                          | -             | 128     |
| 1100    | 4800      | 76.8                          | -             | 64      |
| 1101    | 9600      | 153.6                         | -             | 32      |
| 1110    | 19200     | 307.2                         | -             | 16      |
| 1111    | 38400     | 614.4                         | -             | 8       |

**Set C (BRCLK = 5.0688MHz)**

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY<br>16X CLOCK | PERCENT ERROR | DIVISOR |
|---------|-----------|-------------------------------|---------------|---------|
| 0000    | 50        | 0.8kHz                        | -             | 6336    |
| 0001    | 75        | 1.2                           | -             | 4224    |
| 0010    | 110       | 1.76                          | -             | 2880    |
| 0011    | 134.5     | 2.1523                        | 0.016         | 2355    |
| 0100    | 150       | 2.4                           | -             | 2112    |
| 0101    | 300       | 4.8                           | -             | 1056    |
| 0110    | 600       | 9.6                           | -             | 528     |
| 0111    | 1200      | 19.2                          | -             | 264     |
| 1000    | 1800      | 28.8                          | -             | 176     |
| 1001    | 2000      | 32.081                        | 0.253         | 158     |
| 1010    | 2400      | 38.4                          | -             | 132     |
| 1011    | 3600      | 57.6                          | -             | 88      |
| 1100    | 4800      | 76.8                          | -             | 66      |
| 1101    | 7200      | 115.2                         | -             | 44      |
| 1110    | 9600      | 153.6                         | -             | 33      |
| 1111    | 19200     | 316.8                         | 3.125         | 16      |

NOTE  
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

**ORDERING CODE**

| PACKAGES    | COMMERCIAL RANGES<br>V <sub>CC</sub> = 5V ±5%, T <sub>A</sub> = 0°C to 70°C            |
|-------------|--|
| Ceramic DIP | MC2661A/MC68661A<br>MC2661B/MC68661B<br>MC2661C/MC68661C<br>See table 1 for baud rates |
| Plastic DIP | MC2661A/MC68661A<br>MC2661B/MC68661B<br>MC2661C/MC68661C<br>See table 1 for baud rates |



## MC2661A,B,C/MC68661A,B,C

Table 2 CPU-RELATED SIGNALS

| PIN NAME                                  | PIN NO.                     | INPUT/<br>OUTPUT | FUNCTION  |
|---|-----------------------------|------------------|---|
| VCC                                       | 26                          | I                | +5V supply input  |
| GND                                       | 4                           | I                | Ground  |
| RESET                                     | 21                          | I                | A high on this input performs a master reset on the 2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.  |
| A <sub>1</sub> -A <sub>0</sub>            | 10,12                       | I                | Address lines used to select internal EPCI registers.   |
| $\bar{R}/W$                               | 13                          | I                | Read command when low, write command when high.   |
| $\overline{CE}$                           | 11                          | I                | Chip enable command. When low, indicates that control and data lines to the EPCI are valid and that the operation specified by the $\bar{R}/W$ , A <sub>1</sub> and A <sub>0</sub> inputs should be performed. When high, places the D <sub>0</sub> -D <sub>7</sub> lines in the three-state condition.   |
| D <sub>7</sub> -D <sub>0</sub>            | 8, 7, 6, 5,<br>2, 1, 28, 17 | I/O              | 8-bit, three-state data bus used to transfer commands, data and status between EPCI and the CPU. D <sub>0</sub> is the least significant bit; D <sub>7</sub> the most significant bit.  |
| $\overline{TxRDY}$                        | 15                          | O                | This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.  |
| $\overline{RxRDY}$                        | 14                          | O                | This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.  |
| $\overline{TxEMT}/$<br>$\overline{DSCHG}$ | 18                          | O                | This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU. |

## OPERATION

The functional operation of the 2661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

## Receiver

The 2661 is conditioned to receive data when the  $\overline{DCD}$  input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the  $\overline{RxRDY}$  output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of  $\overline{RxC}$  corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.



## MC2661A,B,C/MC68861A,B,C

Table 3 DEVICE-RELATED SIGNALS

| PIN NAME                         | PIN NO. | INPUT/<br>OUTPUT | FUNCTION   |
|----------------------------------|---------|------------------|--|
| BRCLK                            | 20      | I                | Clock input to the internal baud rate generator (see table 1). Not required if external receiver and transmitter clocks are used.  |
| * $\overline{\text{RxC}}$ /BKDET | 25      | I/O              | Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.                                       |
| * $\overline{\text{TxC}}$ /XSYNC | 9       | I/O              | Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input. |
| RxD                              | 3       | I                | Serial data input to the receiver. "Mark" is high, "space" is low.   |
| TxD                              | 19      | O                | Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.  |
| $\overline{\text{DSR}}$          | 22      | I                | General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{\text{TxE}}/\overline{\text{DSCHG}}$ when its state changes if CR2 or CR0 = 1.  |
| $\overline{\text{DCD}}$          | 16      | I                | Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{\text{TxE}}/\overline{\text{DSCHG}}$ when its state changes if CR2 or CR0 = 1. If $\overline{\text{DCD}}$ goes high while receiving, the RxC is internally inhibited.  |
| $\overline{\text{CTS}}$          | 17      | I                | Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.  |
| $\overline{\text{DTR}}$          | 24      | O                | General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.   |
| $\overline{\text{RTS}}$          | 23      | O                | General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. If the transmit shift register is not empty when CR5 is reset (1 to 0), then $\overline{\text{RTS}}$ will go high one TxC time after the last serial bit is transmitted.  |

## NOTE

\* $\overline{\text{RxC}}$  and  $\overline{\text{TxC}}$  outputs have short circuit protection max  $C_L = 100\text{pF}$ . Outputs become open circuited upon detection of a zero pulled high or a one pulled low.

When the EPC1 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN(CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPC1 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPC1 continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the RxRDY output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

**Transmitter**

The EPC1 is conditioned to transmit data when the  $\overline{\text{CTS}}$  input is low and the TxEN command register bit is set. The 2661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the  $\overline{\text{TxDY}}$  output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.





## MC2661A,B,C/MC68661A,B,C

$\bar{R}/W = 1$ . The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 2661 register formats are summarized in tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPC1, while the command register controls the operation within this basic framework. The EPC1 indicates its status in the status register. These registers are cleared when a RESET input is applied.

#### Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted char-

acter and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12-MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN=0 or when TxEN = 1 and the transmitter is marking in half duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12-15 must be changed within n bit times of the active going state of  $\bar{R}xRDY/TxRDY$ . Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = smaller of the new and old character lengths.)

#### Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPC1 version (A, B, C). Versions A and B specify a 4.9152 MHz TTL input at BRCLK (pin 20); version C specifies a 5.0688 MHz input which is identical to the Signetics 2651. MR23-20 are don't cares if external clocks are selected (MR25-MR24 = 0). The individual rates are given in table 1.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 6.

#### Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second  $\bar{R}xC$  rising edge. Disabling the receiver causes  $\bar{R}xRDY$  to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state

Table 5 MODE REGISTER 1 (MR 1)

| MR17  | MR16   | MR15                | MR14                        | MR13   | MR12  | MR11                      | MR10 |
|---|--|---------------------|-----------------------------|--|---|---------------------------|------|
| Sync/Async  |  | Parity Type         | Parity Control              | Character Length   |   | Mode and Baud Rate Factor |      |
| <b>Async: Stop Bit Length</b><br>00 = Invalid<br>01 = 1 stop bit<br>10 = 1½ stop bits<br>11 = 2 stop bits |  | 0 = Odd<br>1 = Even | 0 = Disabled<br>1 = Enabled | 00 = 5 bits<br>01 = 6 bits<br>10 = 7 bits<br>11 = 8 bits | 00 = Synchronous 1X rate<br>01 = Asynchronous 1X rate<br>10 = Asynchronous 16X rate<br>11 = Asynchronous 64X rate |                           |      |
| <b>Sync: Number of SYN char</b><br>0 = Double SYN<br>1 = Single SYN                                       | <b>Sync: Transparency Control</b><br>0 = Normal<br>1 = Transparent |                     |                             |  |   |                           |      |

NOTE

Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.



## MC2661A,B,C/MC68661A,B,C

Table 6 MODE REGISTER 2 (MR2)

| MR27-MR24 |     |       |        |     |      |       |        |                    |                     | MR23-MR20 |
|-----------|-----|-------|--------|-----|------|-------|--------|--------------------|---------------------|-----------|
| TxC       | RxC | Pin 9 | Pin 25 | TxC | RxC  | Pin 9 | Pin 25 | Mode               | Baud Rate Selection |           |
| 0000      | E   | E     | TxC    | RxC | 1000 | E     | E      | XSYNC <sup>1</sup> | RxC/TxC             | sync      |
| 0001      | E   | I     | TxC    | 1X  | 1001 | E     | I      | TxC                | BKDET               | async     |
| 0010      | I   | E     | 1X     | RxC | 1010 | I     | E      | XSYNC <sup>1</sup> | RxC                 | sync      |
| 0011      | I   | I     | 1X     | 1X  | 1011 | I     | I      | 1X                 | BKDET               | async     |
| 0100      | E   | E     | TxC    | RxC | 1100 | E     | E      | XSYNC <sup>1</sup> | RxC/TxC             | sync      |
| 0101      | E   | I     | TxC    | 16X | 1101 | E     | I      | TxC                | BKDET               | async     |
| 0110      | I   | E     | 16X    | RxC | 1110 | I     | E      | XSYNC <sup>1</sup> | RxC                 | sync      |
| 0111      | I   | I     | 16X    | 16X | 1111 | I     | I      | 16X                | BKDET               | async     |

## NOTES

1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E = External clock

I = Internal clock (BRG)

1X and 16X are clock outputs

Table 7 COMMAND REGISTER (CR)

| CR7   | CR6 | CR5   | CR4  | CR3   | CR2                       | CR1   | CR0                       |
|---|-----|---|--|---|---------------------------|---|---------------------------|
| Operating Mode  |     | Request To Send   | Reset Error  | Sync/Async  | Receive Control (RxEN)    | Data Terminal Ready                                   | Transmit Control (TxEN)   |
| 00 = Normal operation<br>01 = Async:<br>Automatic echo mode<br>Sync. SYN and/or DLE stripping mode<br>10 = Local loop back<br>11 = Remote loop back |     | 0 = Force RTS output high one clock time after TxSR serialization<br>1 = Force RTS output low | 0 = Normal<br>1 = Reset error flags in status register (FE, OE, PE/DLE detect) | Async:<br>Force break<br>0 = Normal<br>1 = Force break<br><br>Sync:<br>Send DLE<br>0 = Normal<br>1 = Send DLE | 0 = Disable<br>1 = Enable | 0 = Force DTR output high<br>1 = Force DTR output low | 0 = Disable<br>1 = Enable |

Table 8 STATUS REGISTER (SR)

| SR7   | SR6   | SR5  | SR4                             | SR3   | SR2  | SR1   | SR0   |
|---|---|--|---------------------------------|---|--|---|---|
| Data Set Ready                                | Data Carrier Detect                           | FE/SYN Detect  | Overrun                         | PE/DLE Detect   | TxE <sub>MT</sub> -D <sub>S</sub> CHG  | RxRDY   | TxRDY   |
| 0 = DSR input is high<br>1 = DSR input is low | 0 = DCD input is high<br>1 = DCD input is low | Async:<br>0 = Normal<br>1 = Framing Error<br><br>Sync:<br>0 = Normal<br>1 = SYN detected | 0 = Normal<br>1 = Overrun Error | Async:<br>0 = Normal<br>1 = Parity error<br><br>Sync:<br>0 = Normal<br>1 = Parity error or DLE received | 0 = Normal<br>1 = Change in DSR, or DCD, or transmit shift register is empty | 0 = Receive holding register empty<br>1 = Receive holding register has data | 0 = Transmit holding register busy<br>1 = Transmit holding register empty |

(high) while  $\overline{\text{TxRDY}}$  and  $\overline{\text{TxE<sub>MT}</sub>}$  will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0 to 1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the DTR and RTS outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the Tx<sub>D</sub> output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The Tx<sub>D</sub> line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit

data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.



## MC2661A,B,C/MC68661A,B,C

Table 9 MC2661/MC68661 EPCI vs SIGNETICS 2651 PCI

| FEATURE  | EPCI  | PCI   |
|--|---|---|
| 1. MR2 Bit 6, 7  | Control pin 9, 25   | Not used  |
| 2. DLE detect-SR3                                      | SR3 = 0 for DLE-DLE,<br>DLE-SYNC1                                       | SR3 = 1 for DLE-DLE,<br>DLE-SYNC1   |
| 3. Reset of SR3, DLE detect                            | Second character after DLE, or receiver disable, or CR4 = 1             | Receiver disable, or CR4 = 1  |
| 4. Send DLE-CR3  | One time command  | Reset via CR3 on next $\overline{\text{TxRDY}}$   |
| 5. DLE stuffing in transparent mode                    | Automatic DLE stuffing when DLE is loaded except if CR3 = 1             | None  |
| 6. SYNC1 stripping in double sync non-transparent mode | All SYNC1   | First SYNC1 of pair   |
| 7. Baud rate versions                                  | Three   | One   |
| 8. Terminate ASYNC transmission (drop RTS)             | Reset CR5 in response to $\overline{\text{TxRDY}}$ changing from 0 to 1 | Reset CR0 when $\overline{\text{TxEMT}}$ goes from 1 to 0. Then reset CR5 when $\overline{\text{TxEMT}}$ goes from 0 to 1 |
| 9. Break detect  | Pin 25 <sup>1</sup>   | FE and null character   |
| 10. Stop bit searched                                  | One   | Two   |
| 11. External jam sync                                  | Pin 9 <sup>2</sup>  | No  |
| 12. Data bus timing                                    | Improved over 2651  | —   |
| 13. Data bus drivers                                   | Sink 2.2mA<br>Source 400 $\mu$ A  | Sink 1.6mA<br>Source 100 $\mu$ A  |

## NOTES

1. Internal BRG used for RxC
2. Internal BRG used for TxC

When CR5 (RTS) is set, the  $\overline{\text{RTS}}$  pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause  $\overline{\text{RTS}}$  to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The EPCI can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7-CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3.  $\overline{\text{TxRDY}}$  output = 1.
4. The  $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$  pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16 = 1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However,

only the first DLE of a DLE-DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loop back mode (CR7-CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2.  $\overline{\text{DTR}}$  is connected to  $\overline{\text{DCD}}$  and  $\overline{\text{RTS}}$  is connected to  $\overline{\text{CTS}}$ .
3. The receiver is clocked by the transmit clock.
4. The  $\overline{\text{DTR}}$ ,  $\overline{\text{RTS}}$  and  $\overline{\text{TxD}}$  outputs are held high.
5. The  $\overline{\text{CTS}}$ ,  $\overline{\text{DCD}}$ ,  $\overline{\text{DSR}}$  and RxD inputs are ignored.

Additional requirements to operate in the local loop back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loop back mode (CR7-CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The  $\overline{\text{RxRDY}}$ ,  $\overline{\text{TxRDY}}$ , and  $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$  outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

### Status Register

The data contained in the status register (as shown in table 8) indicate receiver and transmitter conditions and modem/data set status.

SRO is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the  $\overline{\text{TxRDY}}$  output pin is low. In





the automatic echo and remote loop back modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the RxRDY output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the DSR or DCD inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is

cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 = 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the TxEMT/DSCHG output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared

when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the DCD and DSR inputs respectively. A low input sets its corresponding status bit, and a high input clears it.

#### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| PARAMETER  | RATING       | UNIT |
|--|--------------|------|
| Operating ambient temperature <sup>2</sup>       | 0 to +70     | °C   |
| Storage temperature                              | -55 to +150  | °C   |
| All voltages with respect to ground <sup>3</sup> | -0.3 to +7.0 | V    |

#### THERMAL CHARACTERISTICS

| CHARACTERISTIC     | SYMBOL        | VALUE | UNIT |
|--------------------|---------------|-------|------|
| Thermal Resistance |               |       |      |
| Ceramic            |               | 50    |      |
| Plastic            | $\theta_{JA}$ | 100   | °C/W |
| Cerdip             |               | 60    |      |

#### DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = 5.0\text{V} \pm 5\%$ <sup>4,5,6</sup>

| PARAMETER                                       | TEST CONDITIONS   | LIMITS |   |                 | UNIT |
|---|---|--------|---|-----------------|------|
|   |   | Min    | Typ   | Max             |      |
| V <sub>IL</sub><br>V <sub>IH</sub>              | Input voltage<br>Low<br>High                                    | -0.3   |   | 0.8             | V    |
|   |   | 2.0    |   | V <sub>CC</sub> |      |
| V <sub>OL</sub><br>V <sub>OH</sub> <sup>7</sup> | Output voltage<br>Low<br>High                                   |        |   | 0.4             | V    |
|   |   |        | I <sub>OL</sub> = 2.2mA<br>I <sub>OH</sub> = -400μA |                 |      |
| I <sub>IL</sub>                                 | Input leakage current   |        |   | 10              | μA   |
| I <sub>LH</sub><br>I <sub>LL</sub>              | 3-state output leakage current<br>Data bus high<br>Data bus low |        |   | 10              | μA   |
|   |   |        | V <sub>OUT</sub> = 0 to 5.25 V                      | 10              |      |
| I <sub>CC</sub>                                 | Power supply current  |        |   | 150             | mA   |

#### CAPACITANCE $T_A = 25^\circ\text{C}, V_{CC} = 0\text{V}$

| PARAMETER   | TEST CONDITIONS   | LIMITS |     |     | UNIT |
|---|---|--------|-----|-----|------|
|   |   | Min    | Typ | Max |      |
| C <sub>IN</sub><br>C <sub>OUT</sub><br>C <sub>I/O</sub> | Capacitance<br>Input<br>Output<br>Input/Output  |        |     | 20  | pF   |
|   |   |        |     | 20  |      |
|   |   |        |     | 20  |      |
|   | V <sub>IN</sub> = V <sub>OUT</sub> = 0 V<br>f <sub>c</sub> = 1MHz<br>Unmeasured pins tied to ground |        |     |     |      |

Notes on following page



MOTOROLA Semiconductor Products Inc.

**AC ELECTRICAL CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$  <sup>4,5,6</sup>

| PARAMETER  | TEST CONDITIONS        | Min  | Typ    | Max    | UNIT |
|--|------------------------|------|--------|--------|------|
| t <sub>RES</sub><br>Pulse width<br>Reset   |                        | 1000 |        |        | ns   |
| t <sub>CE</sub><br>Chip enable   |                        | 250  |        |        |      |
| t <sub>AS</sub><br>Setup and hold time<br>Address setup                                    |                        | 10   |        |        | ns   |
| t <sub>AH</sub><br>Address hold  |                        | 10   |        |        |      |
| t <sub>CS</sub><br>R/W control setup   |                        | 10   |        |        |      |
| t <sub>CH</sub><br>R/W control hold  |                        | 10   |        |        |      |
| t <sub>DS</sub><br>Data setup for write  |                        | 150  |        |        |      |
| t <sub>DH</sub><br>Data hold for write   |                        | 0    |        |        |      |
| t <sub>RXS</sub><br>Rx data setup  |                        | 300  |        |        |      |
| t <sub>RXH</sub><br>Rx data hold   |                        | 350  |        |        |      |
| t <sub>DD</sub><br>Data delay time for read  | C <sub>L</sub> = 150pF |      |        | 200    | ns   |
| t <sub>DF</sub><br>Data bus floating time for read   | C <sub>L</sub> = 150pF |      |        | 100    |      |
| t <sub>CED</sub><br>CE to CE delay   |                        | 600  |        |        |      |
| f <sub>BRG</sub><br>Input clock frequency<br>Baud rate generator<br>(MC2661A,B/MC68661A,B) |                        | 1.0  | 4.9152 | 4.9202 | MHz  |
| f <sub>BRG</sub><br>Baud rate generator<br>(MC2661C/MC68661C)                              |                        | 1.0  | 5.0688 | 5.0738 |      |
| f <sub>R/T</sub><br>TxC or RxC   |                        | dc   |        | 1.0    |      |
| t <sub>BRH</sub> <sup>9</sup><br>Clock width<br>Baud rate high (MC2661A,B/MC68661A,B)      |                        | 75   |        |        | ns   |
| t <sub>BRH</sub> <sup>9</sup><br>Baud rate high (MC2661C/MC68661C)                         |                        | 70   |        |        |      |
| t <sub>BRL</sub> <sup>9</sup><br>Baud rate low (MC2661A,B/MC68661A,B)                      |                        | 75   |        |        |      |
| t <sub>BRL</sub> <sup>9</sup><br>Baud rate low (MC2661C/MC68661C)                          |                        | 70   |        |        |      |
| t <sub>R/TH</sub><br>TxC or RxC high   |                        | 480  |        |        |      |
| t <sub>R/TL</sub><br>TxC or RxC low  |                        | 480  |        |        |      |
| t <sub>TXD</sub><br>TxD delay from falling edge of TxC                                     | C <sub>L</sub> = 150pF |      |        | 650    | ns   |
| t <sub>TCS</sub><br>Skew between TxD changing and falling edge of TxC output <sup>8</sup>  | C <sub>L</sub> = 150pF | TBD  |        | TBD    |      |

## NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
- For operating at elevated temperatures, the device must be derated based on  $+150^\circ\text{C}$  maximum junction temperature and thermal resistance of  $60^\circ\text{C}/\text{W}$  junction to ambient (IQ ceramic package).
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t<sub>BRH</sub> and t<sub>BRL</sub>) and at 0.8 V and 2.0 V for outputs. Input levels swing between 0.4 V and 2.4 V, with a transition time of 20ns maximum.
- Typical values are at  $+25^\circ\text{C}$ , typical supply voltages and typical processing parameters.
- TxDY, RxRDY and TxEMT/DSCHG outputs are open drain.
- Parameter applies when internal transmitter clock is used.
- Under test conditions of 5.0688 MHz f<sub>BRG</sub> (MC2661C/MC68661C) and 4.9152 MHz f<sub>BRG</sub> (MC2661A,B/MC68661A,B), t<sub>BRH</sub> and t<sub>BRL</sub> measured at V<sub>IH</sub> and V<sub>IL</sub> respectively.

**POWER CONSIDERATIONS**

The average chip-junction temperature, T<sub>J</sub>, in  $^\circ\text{C}$  can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

- T<sub>A</sub> = Ambient Temperature,  $^\circ\text{C}$
- $\theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient,  $^\circ\text{C}/\text{W}$
- P<sub>D</sub> = P<sub>INT</sub> + P<sub>PORT</sub>
- P<sub>INT</sub> = I<sub>CC</sub> × V<sub>CC</sub>, Watts – Chip Internal Power
- P<sub>PORT</sub> = Port Power Dissipation, Watts – User Determined

For most applications P<sub>PORT</sub> ≪ P<sub>INT</sub> and can be neglected. P<sub>PORT</sub> may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P<sub>D</sub> and T<sub>J</sub> (if P<sub>PORT</sub> is neglected) is:

$$P_D = K + (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

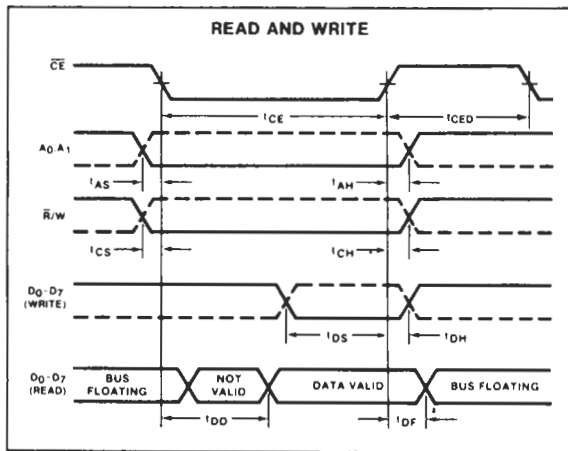
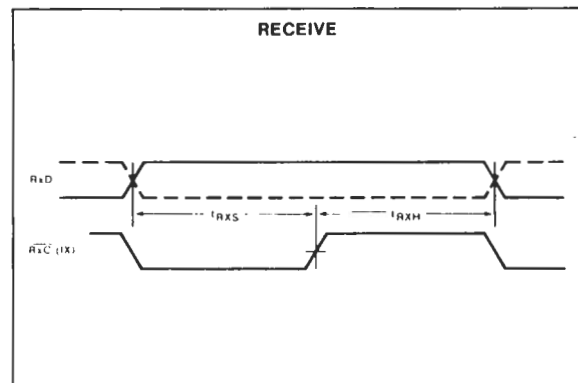
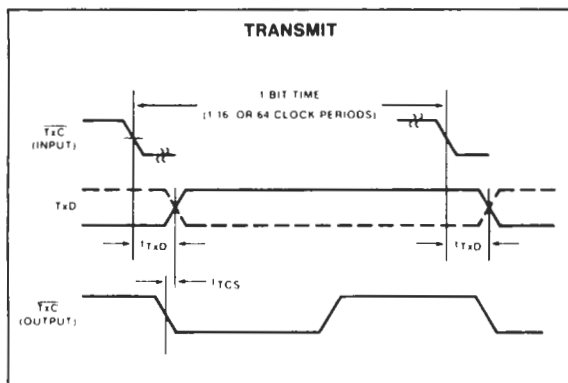
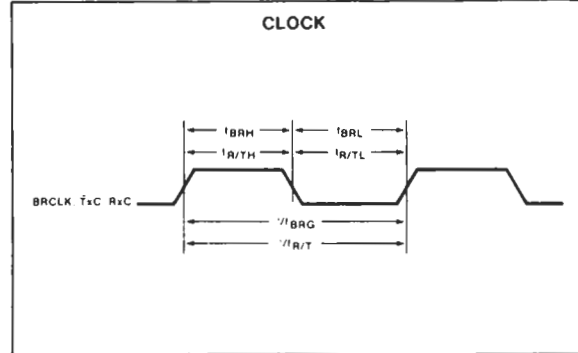
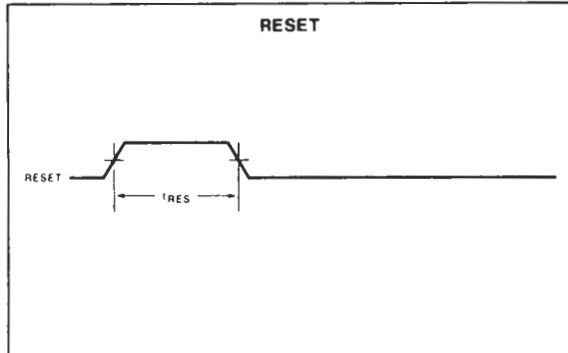
$$K = P_D \cdot (T_A + 273^\circ\text{C}) + \theta_{JA} \cdot P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P<sub>D</sub> (at equilibrium) for a known T<sub>A</sub>. Using this value of K the values of P<sub>D</sub> and T<sub>J</sub> can be obtained by solving equations (1) and (2) iteratively for any value of T<sub>A</sub>.



MC2661A,B,C/MC68661A,B,C

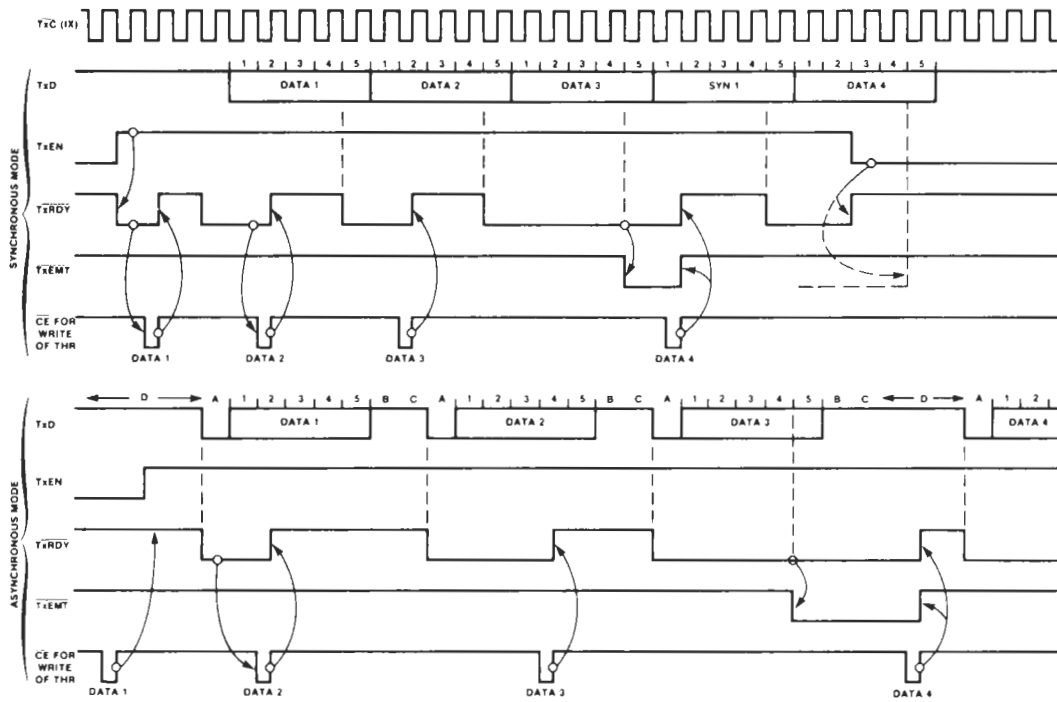
TIMING DIAGRAMS



**MC2661A,B,C/MC68661A,B,C**

**TIMING DIAGRAMS** (Cont'd)

**TxRDY, TxEMT** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



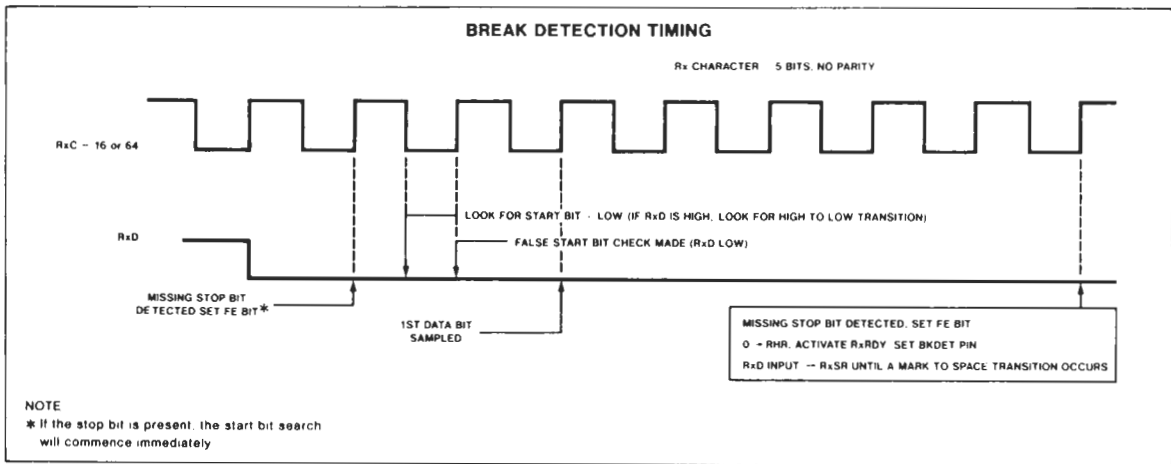
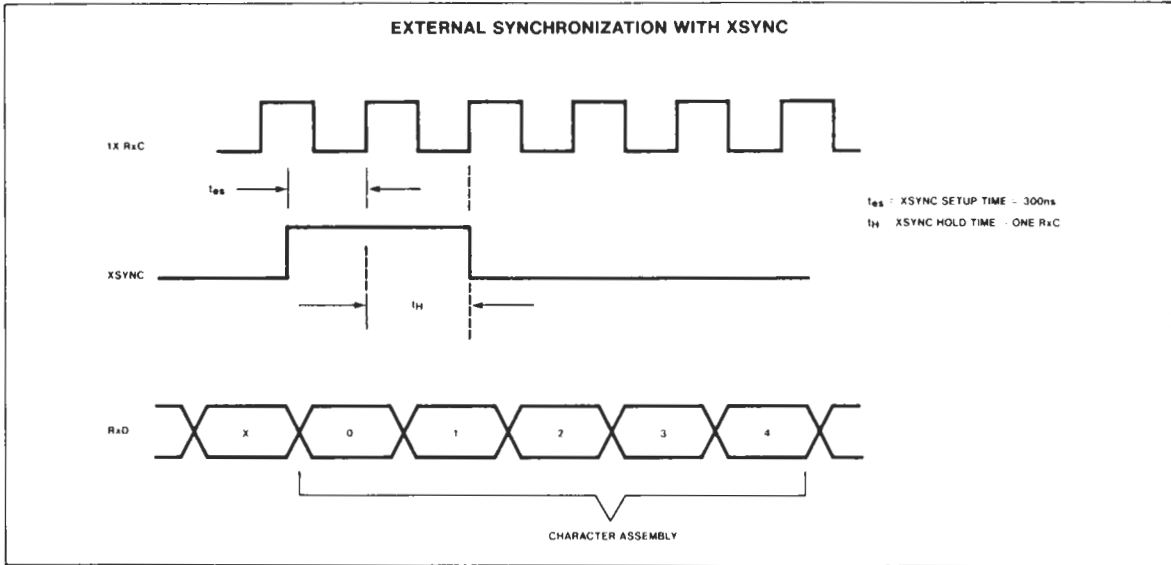
**NOTES**

- A = Start bit
  - B = Stop bit 1
  - C = Stop bit 2
  - D = TxD marking condition
- TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit



**MC2661A,B,C/MC68661A,B,C**

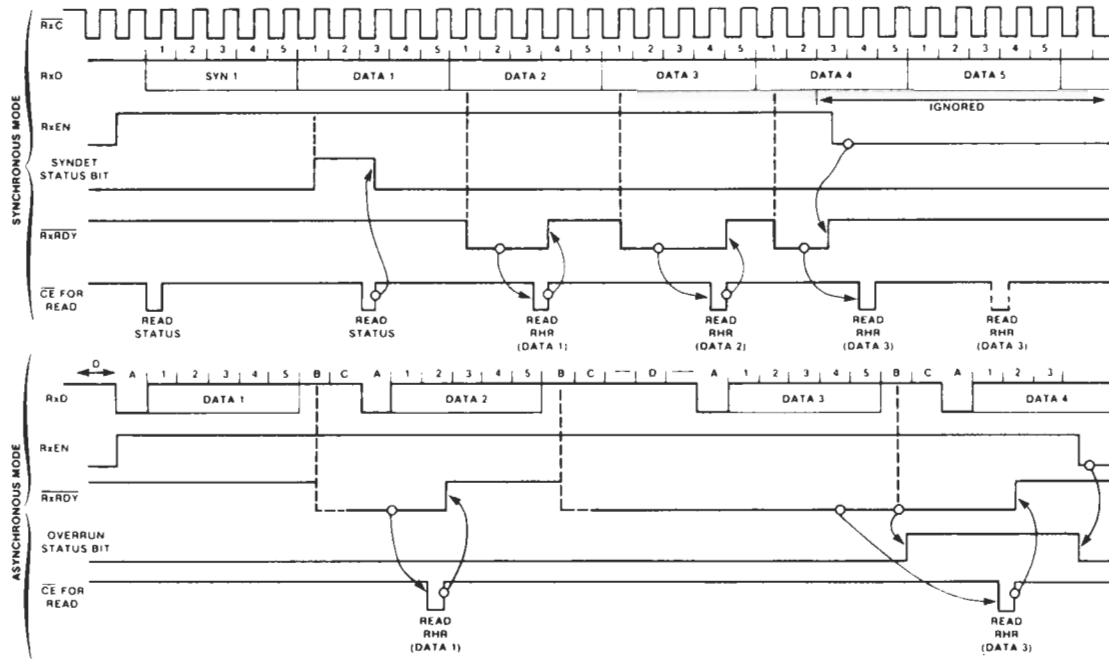
**TIMING DIAGRAMS (Cont'd)**



MC2661A,B,C/MC68661A,B,C

TIMING DIAGRAMS (Cont'd)

RxRDY (Shown for 5-bit characters, no parity, 2 stops bits (in asynchronous mode) )

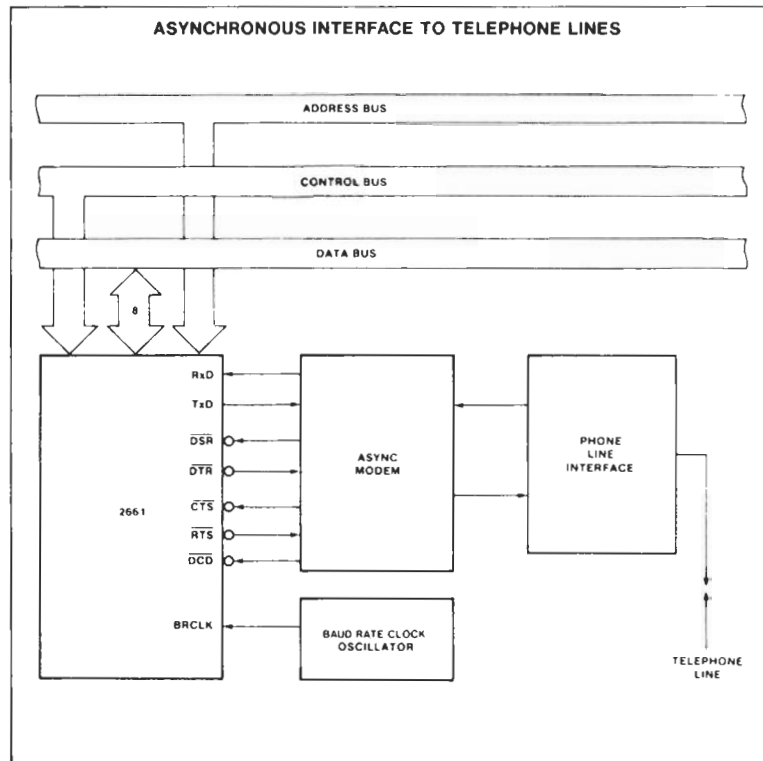
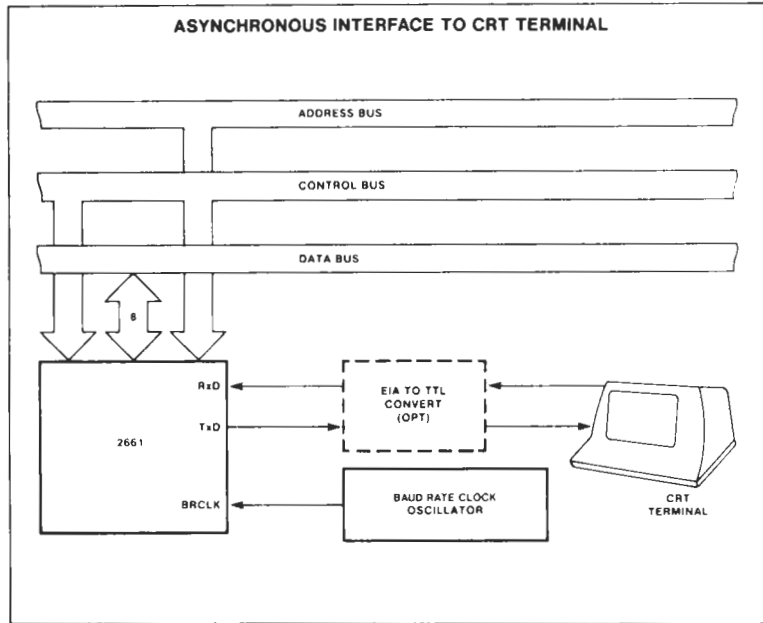


NOTES  
 A = Start bit  
 B = Stop bit 1  
 C = Stop bit 2  
 D = TxD marking condition  
 Only one stop bit is detected



MC2661A,B,C/MC68661A,B,C

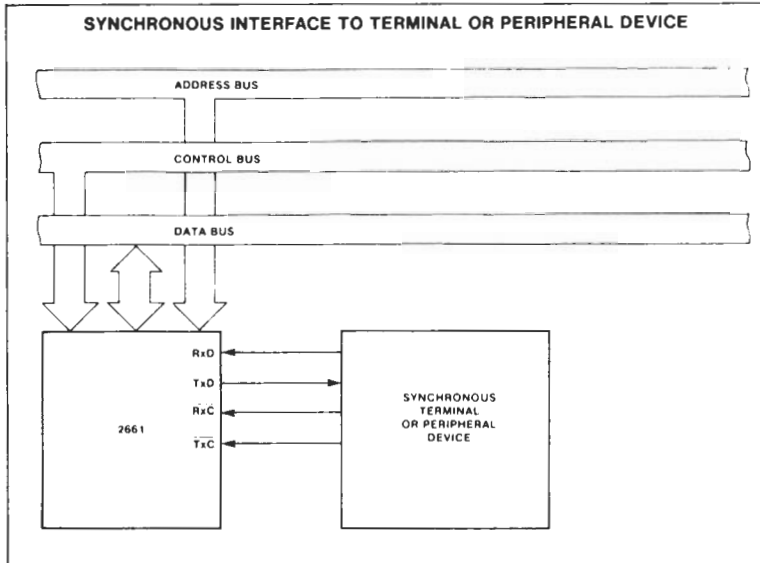
TYPICAL APPLICATIONS



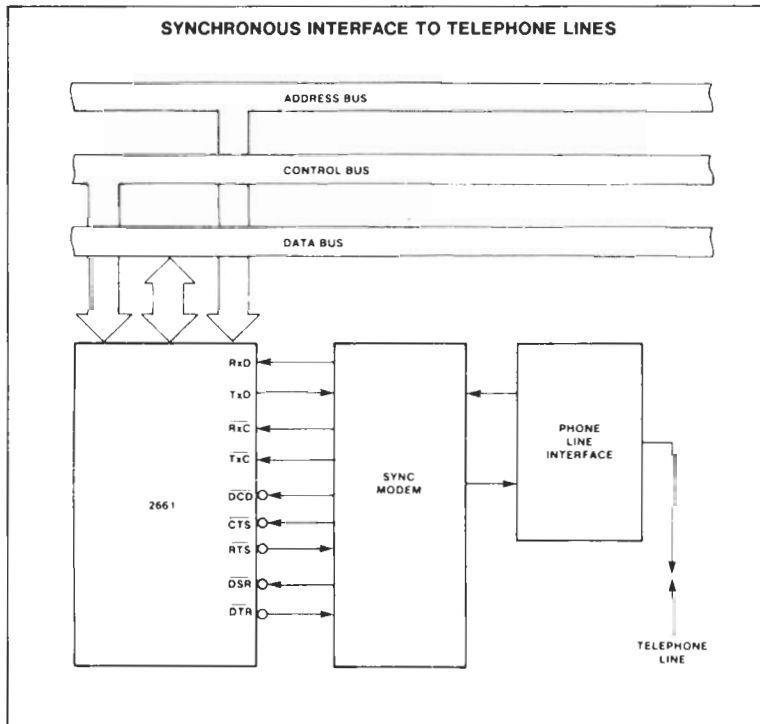
**MC2661A,B,C/MC68661A,B,C**

**TYPICAL APPLICATIONS (Cont'd)**

**SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE**



**SYNCHRONOUS INTERFACE TO TELEPHONE LINES**





## MC2661A,B,C/MC68661A,B,C

**MC68000 MPU-TO-EPCI INTERFACE REQUIREMENTS**

The circuit shown in Figure 2 interfaces the EPCI to the MC68000 MPU. The 8-bit data bus of the EPCI is connected to the low order 8 bits of the MPU data bus (D0-D7). Due to this, the EPCI's registers are addressed on word (even byte) boundaries and so address line A1 of the MPU is connected to the A0 address line of the EPCI. Similarly, A2 of the MPU is connected to A1 of the EPCI.  $\overline{R}/\overline{W}$  on the MC68000 is inverted and connected to  $\overline{R}/\overline{W}$  of the EPCI.

The  $\overline{CE}$  signal must be generated for the EPCI and the  $\overline{DTACK}$  signal must be supplied to the

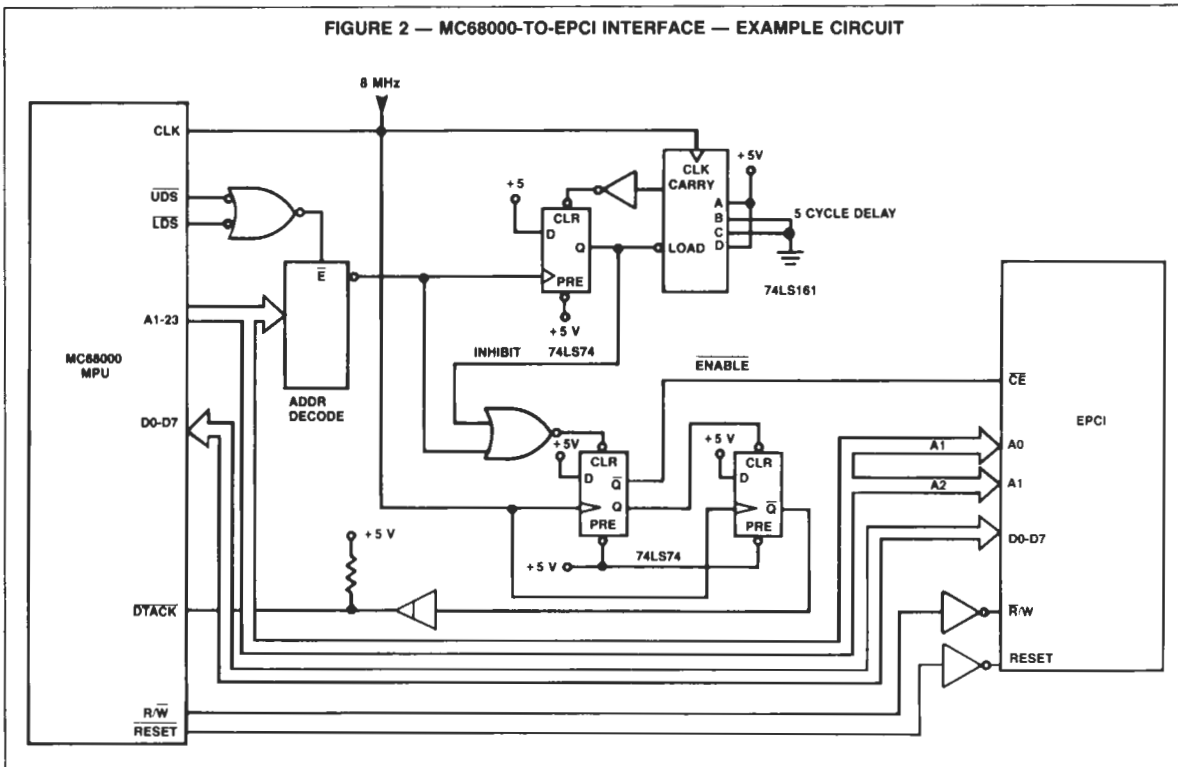
MPU. To allow for the data setup time on a read of the EPCI,  $\overline{CE}$  must be delayed one-half clock cycle and  $\overline{DTACK}$  generated on the next rising edge of the system clock. This causes the processor to insert one wait state in the bus cycle. In addition to this,  $\overline{CE}$  must not be reasserted until the chip enable period  $t_{CE}$  has expired. Since some instructions on the MC68000 can cause access to consecutive addresses on consecutive bus cycles (e.g., MOVEP), an INHIBIT signal must be generated to hold-off an access during this period. A state machine consisting of a 74LS161 binary counter and a 74LS74 D flip-flop is configured as a digital "one shot." The rising edge

of  $\overline{CE}$  starts the counter which times out after given number of clock cycles. Since  $t_{CE}$  is 600 ns, a minimum of 5 clock cycles at 8 MHz (625 ns) is required. The timing for two consecutive read bus cycles is shown in Figure 3. The INHIBIT signal prevents  $\overline{CE}$  from being generated and  $\overline{DTACK}$  from being asserted, causing the processor to generate wait states until INHIBIT is negated.

**M6809 FAMILY MPU-TO-EPCI INTERFACE REQUIREMENTS**

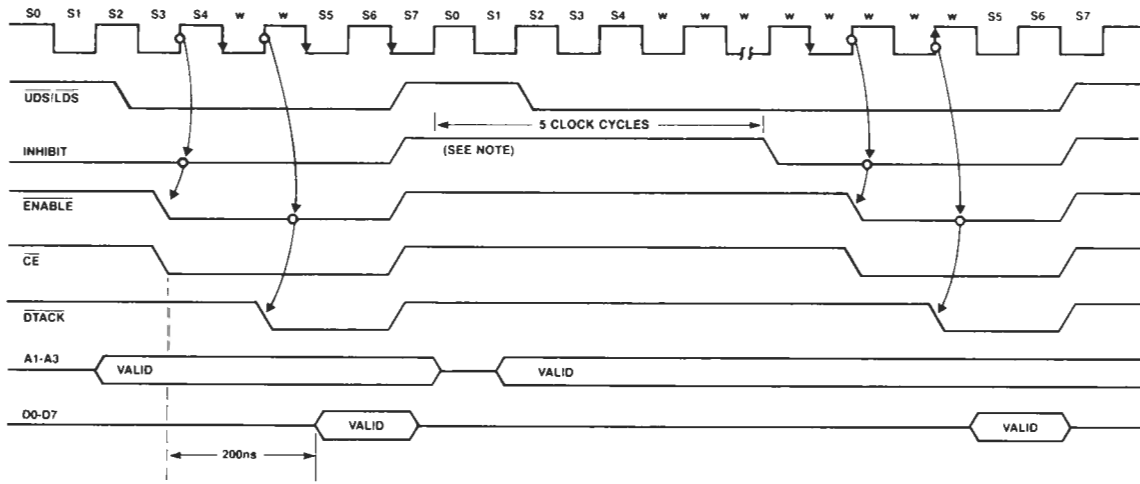
The M6809 family of microprocessors can be easily interfaced to the EPCI as shown in Figure 4.

FIGURE 2 — MC68000-TO-EPCI INTERFACE — EXAMPLE CIRCUIT



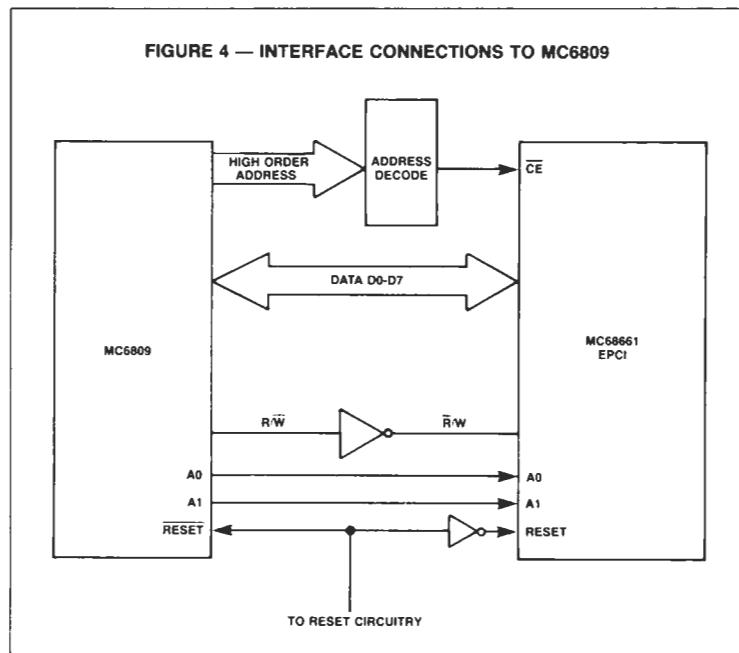
MC2661A,B,C/MC68661A,B,C

FIGURE 3 — MC68000-TO-EPCI READ BUS CYCLE TIMING



NOTE: INSERTION OF INHIBIT PERIOD DELAYS NEXT READ CYCLE FOR 5 CLOCK CYCLES

FIGURE 4 — INTERFACE CONNECTIONS TO MC6809



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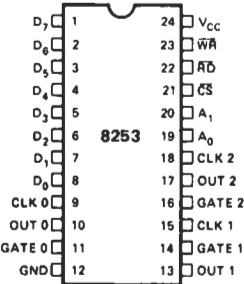
## 8253/8253-5 PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
  - 3 Independent 16-Bit Counters
  - DC to 2 MHz
  - Programmable Counter Modes
- Count Binary or BCD
  - Single +5V Supply
  - 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

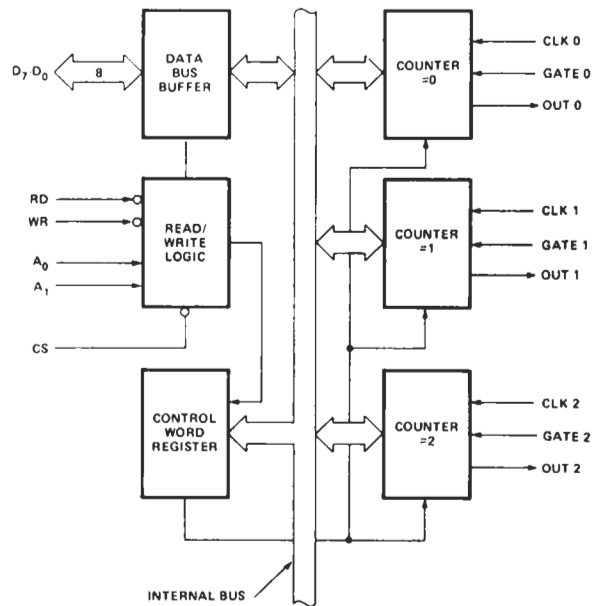
### PIN CONFIGURATION



### PIN NAMES

|                                 |                       |
|---------------------------------|-----------------------|
| D <sub>7</sub> , D <sub>0</sub> | DATA BUS (8 BIT)      |
| CLK N                           | COUNTER CLOCK INPUTS  |
| GATE N                          | COUNTER GATE INPUTS   |
| OUT N                           | COUNTER OUTPUTS       |
| RD                              | READ COUNTER          |
| WR                              | WRITE COMMAND OR DATA |
| CS                              | CHIP SELECT           |
| A <sub>0</sub> , A <sub>1</sub> | COUNTER SELECT        |
| V <sub>CC</sub>                 | +5 VOLTS              |
| GND                             | GROUND                |

### BLOCK DIAGRAM



## 8253/8253-5

## FUNCTIONAL DESCRIPTION

## General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Micro-computer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

## Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

## Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

## RD (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

## WR (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

## A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

## CS (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The CS input has no effect upon the actual operation of the counters.

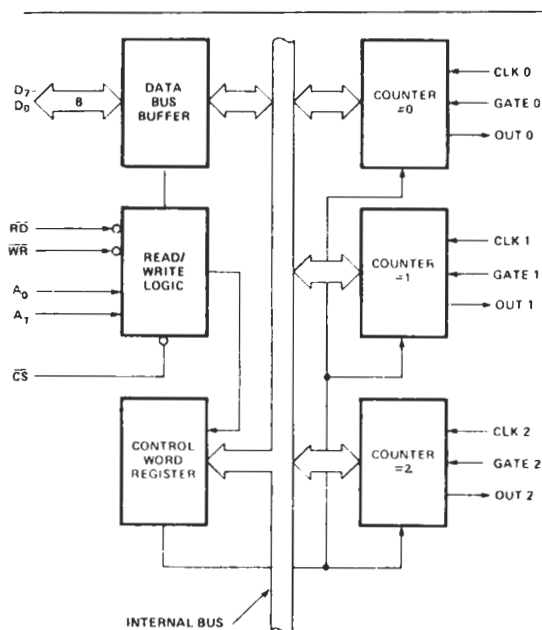


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

| CS | RD | WR | A <sub>1</sub> | A <sub>0</sub> |                      |
|----|----|----|----------------|----------------|----------------------|
| 0  | 1  | 0  | 0              | 0              | Load Counter No. 0   |
| 0  | 1  | 0  | 0              | 1              | Load Counter No. 1   |
| 0  | 1  | 0  | 1              | 0              | Load Counter No. 2   |
| 0  | 1  | 0  | 1              | 1              | Write Mode Word      |
| 0  | 0  | 1  | 0              | 0              | Read Counter No. 0   |
| 0  | 0  | 1  | 0              | 1              | Read Counter No. 1   |
| 0  | 0  | 1  | 1              | 0              | Read Counter No. 2   |
| 0  | 0  | 1  | 1              | 1              | No-Operation 3-State |
| 1  | X  | X  | X              | X              | Disable 3-State      |
| 0  | 1  | 1  | X              | X              | No-Operation 3-State |

8253/8253-5

**Control Word Register**

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

**Counter #0, Counter #1, Counter #2**

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

**8253 SYSTEM INTERFACE**

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The  $\overline{CS}$  can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

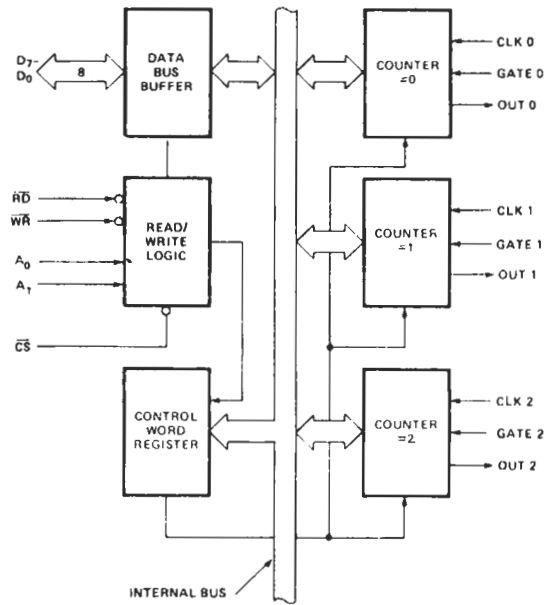


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

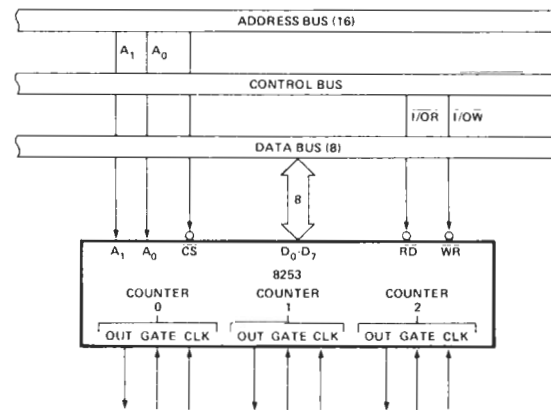


Figure 3. 8253 System Interface

## 8253/8253-5

## OPERATIONAL DESCRIPTION

**General**

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

**Programming the 8253**

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

**Control Word Format**

| D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| SC1            | SC0            | RL1            | RL0            | M2             | M1             | M0             | BCD            |

**Definition of Control****SC — Select Counter:**

| SC1 | SC0 |                  |
|-----|-----|------------------|
| 0   | 0   | Select Counter 0 |
| 0   | 1   | Select Counter 1 |
| 1   | 0   | Select Counter 2 |
| 1   | 1   | Illegal          |

**RL — Read/Load:**

| RL1 | RL0 |   |
|-----|-----|---|
| 0   | 0   | Counter Latching operation (see READ/WRITE Procedure Section)       |
| 1   | 0   | Read/Load most significant byte only.                               |
| 0   | 1   | Read/Load least significant byte only.                              |
| 1   | 1   | Read/Load least significant byte first, then most significant byte. |

**M — MODE:**

| M2 | M1 | M0 |        |
|----|----|----|--------|
| 0  | 0  | 0  | Mode 0 |
| 0  | 0  | 1  | Mode 1 |
| X  | 1  | 0  | Mode 2 |
| X  | 1  | 1  | Mode 3 |
| 1  | 0  | 0  | Mode 4 |
| 1  | 0  | 1  | Mode 5 |

**BCD:**

|   |  |
|---|--|
| 0 | Binary Counter 16-bits                         |
| 1 | Binary Coded Decimal (BCD) Counter (4 Decades) |

**Counter Loading**

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

**MODE Definition**

**MODE 0: Interrupt on Terminal Count.** The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

**MODE 1: Programmable One-Shot.** The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

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**MODE 2: Rate Generator.** Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

**MODE 3: Square Wave Rate Generator.** Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for  $(N + 1)/2$  counts and low for  $(N - 1)/2$  counts.

**MODE 4: Software Triggered Strobe.** After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

**MODE 5: Hardware Triggered Strobe.** The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

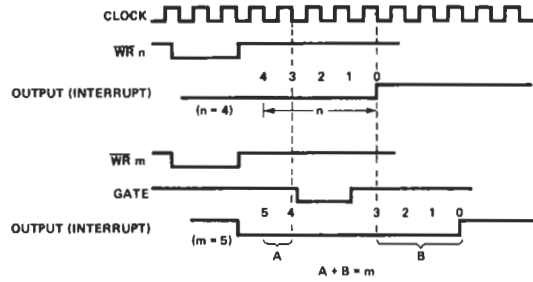
| Modes | Signal Status | Low Or Going Low  | Rising   | High             |
|-------|---------------|---|--|------------------|
| 0     |               | Disables counting                                       | ---  | Enables counting |
| 1     |               | ---   | 1) Initiates counting<br>2) Resets output after next clock | ---              |
| 2     |               | 1) Disables counting<br>2) Sets output immediately high | 1) Reloads counter<br>2) Initiates counting                | Enables counting |
| 3     |               | 1) Disables counting<br>2) Sets output immediately high | Initiates counting   | Enables counting |
| 4     |               | Disables counting                                       | ---  | Enables counting |
| 5     |               | ---   | Initiates counting   | ---              |

Figure 4. Gate Pin Operations Summary

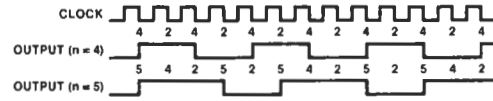


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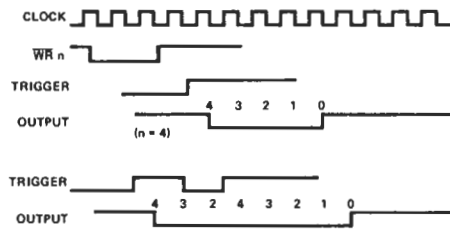
**MODE 0: Interrupt on Terminal Count**



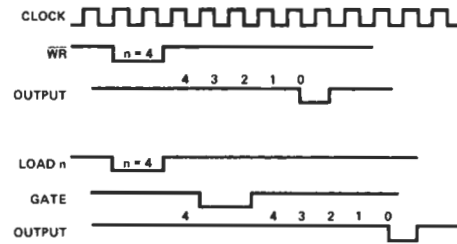
**MODE 3: Square Wave Generator**



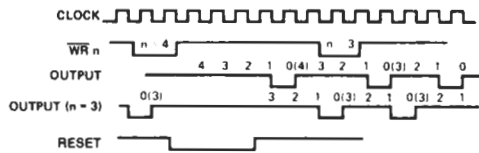
**MODE 1: Programmable One-Shot**



**MODE 4: Software Triggered Strobe**



**MODE 2: Rate Generator**



**MODE 5: Hardware Triggered Strobe**

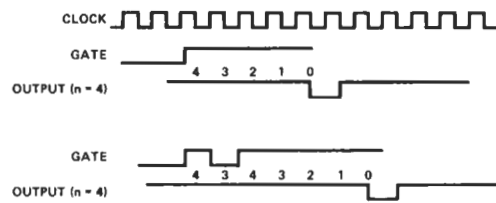


Figure 5. 8253 Timing Diagrams

## 8253/8253-5

## 8253 READ/WRITE PROCEDURE

## Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count ( $2^{16}$  for Binary or  $10^4$  for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

| MODE Control Word<br>Counter n |                                  |
|--------------------------------|----------------------------------|
| LSB                            | Count Register byte<br>Counter n |
| MSB                            | Count Register byte<br>Counter n |

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 6. Programming Format

|       |                                      | A1 | A0 |
|-------|--------------------------------------|----|----|
| No. 1 | MODE Control Word<br>Counter 0       | 1  | 1  |
| No. 2 | MODE Control Word<br>Counter 1       | 1  | 1  |
| No. 3 | MODE Control Word<br>Counter 2       | 1  | 1  |
| No. 4 | LSB Count Register Byte<br>Counter 1 | 0  | 1  |
| No. 5 | MSB Count Register Byte<br>Counter 1 | 0  | 1  |
| No. 6 | LSB Count Register Byte<br>Counter 2 | 1  | 0  |
| No. 7 | MSB Count Register Byte<br>Counter 2 | 1  | 0  |
| No. 8 | LSB Count Register Byte<br>Counter 0 | 0  | 0  |
| No. 9 | MSB Count Register Byte<br>Counter 0 | 0  | 0  |

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats

## 8253/8253-5

**Read Operations**

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

**Read Operation Chart**

| A1 | A0 | RD |                    |
|----|----|----|--------------------|
| 0  | 0  | 0  | Read Counter No. 0 |
| 0  | 1  | 0  | Read Counter No. 1 |
| 1  | 0  | 0  | Read Counter No. 2 |
| 1  | 1  | 0  | Illegal            |

**Reading While Counting**

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

**MODE Register for Latching Count**

A0, A1 = 11

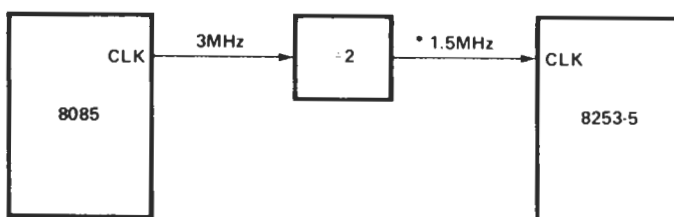
| D7  | D6  | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|----|----|----|----|----|----|
| SC1 | SC0 | 0  | 0  | X  | X  | X  | X  |

SC1, SC0 — specify counter to be latched.

D5, D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



\*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

Figure 8. MCS-85™ Clock Interface\*

**8253/8253-5****ABSOLUTE MAXIMUM RATINGS\***

|                                |                   |
|--------------------------------|-------------------|
| Ambient Temperature Under Bias | 0° C to 70° C     |
| Storage Temperature            | -65° C to +150° C |
| Voltage On Any Pin             |                   |
| With Respect to Ground         | -0.5 V to +7 V    |
| Power Dissipation              | 1 Watt            |

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

| SYMBOL    | PARAMETER               | MIN. | MAX.                 | UNITS         | TEST CONDITIONS          |
|-----------|-------------------------|------|----------------------|---------------|--------------------------|
| $V_{IL}$  | Input Low Voltage       | -0.5 | 0.8                  | V             |                          |
| $V_{IH}$  | Input High Voltage      | 2.2  | $V_{CC} + 5\text{V}$ | V             |                          |
| $V_{OL}$  | Output Low Voltage      |      | 0.45                 | V             | Note 1                   |
| $V_{OH}$  | Output High Voltage     | 2.4  |                      | V             | Note 2                   |
| $I_{IL}$  | Input Load Current      |      | $\pm 10$             | $\mu\text{A}$ | $V_{IN} = V_{CC}$ to 0V  |
| $I_{OFL}$ | Output Float Leakage    |      | $\pm 10$             | $\mu\text{A}$ | $V_{OUT} = V_{CC}$ to 0V |
| $I_{CC}$  | $V_{CC}$ Supply Current |      | 140                  | mA            |                          |

Note 1:  $I_{OL} = 2.2\text{ mA}$ .

Note 2:  $I_{OH} = -400\ \mu\text{A}$ .

**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0\text{V}$ )

| Symbol    | Parameter         | Min. | Typ. | Max. | Unit | Test Conditions                      |
|-----------|-------------------|------|------|------|------|--------------------------------------|
| $C_{IN}$  | Input Capacitance |      |      | 10   | pF   | $f_c = 1\text{ MHz}$                 |
| $C_{I/O}$ | I/O Capacitance   |      |      | 20   | pF   | Unmeasured pins returned to $V_{SS}$ |

## 8253/8253-5

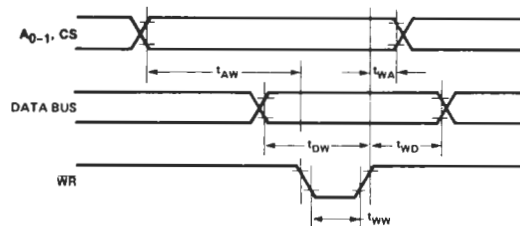
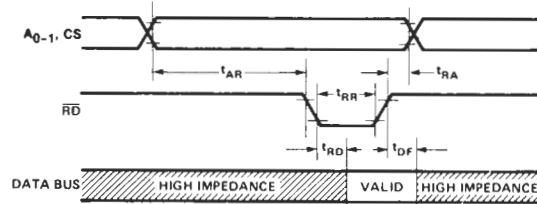
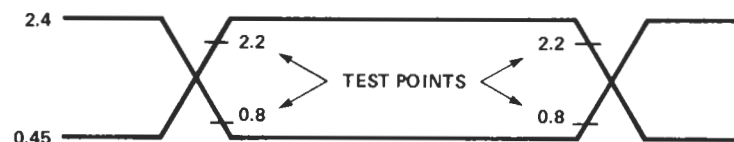
**A.C. CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 5\%$ ;  $\text{GND} = 0\text{V}$ **Bus Parameters (Note 1)****Read Cycle:**

| SYMBOL   | PARAMETER   | 8253 |      | 8253-5 |      | UNIT          |
|----------|---|------|------|--------|------|---------------|
|          |   | MIN. | MAX. | MIN.   | MAX. |               |
| $t_{AR}$ | Address Stable Before $\overline{\text{READ}}$          | 50   |      | 30     |      | ns            |
| $t_{RA}$ | Address Hold Time for $\overline{\text{READ}}$          | 5    |      | 5      |      | ns            |
| $t_{RR}$ | $\overline{\text{READ}}$ Pulse Width                    | 400  |      | 300    |      | ns            |
| $t_{RD}$ | Data Delay From $\overline{\text{READ}}^{\text{1}}$     |      | 300  |        | 200  | ns            |
| $t_{DF}$ | $\overline{\text{READ}}$ to Data Floating               | 25   | 125  | 25     | 100  | ns            |
| $t_{RV}$ | Recovery Time Between READ and Any Other Control Signal | 1    |      | 1      |      | $\mu\text{s}$ |

**Write Cycle:**

| SYMBOL   | PARAMETER  | 8253 |      | 8253-5 |      | UNIT          |
|----------|--|------|------|--------|------|---------------|
|          |  | MIN. | MAX. | MIN.   | MAX. |               |
| $t_{AW}$ | Address Stable Before $\overline{\text{WRITE}}$                              | 50   |      | 30     |      | ns            |
| $t_{WA}$ | Address Hold Time for $\overline{\text{WRITE}}$                              | 30   |      | 30     |      | ns            |
| $t_{WW}$ | $\overline{\text{WRITE}}$ Pulse Width  | 400  |      | 300    |      | ns            |
| $t_{DW}$ | Data Set Up Time for $\overline{\text{WRITE}}$                               | 300  |      | 250    |      | ns            |
| $t_{WD}$ | Data Hold Time for $\overline{\text{WRITE}}$                                 | 40   |      | 30     |      | ns            |
| $t_{RV}$ | Recovery Time Between $\overline{\text{WRITE}}$ and Any Other Control Signal | 1    |      | 1      |      | $\mu\text{s}$ |

Notes: 1. AC timings measured at  $V_{OH} = 2.2$ ,  $V_{OL} = 0.8$   
 2.  $C_L = 150\text{pF}$ .

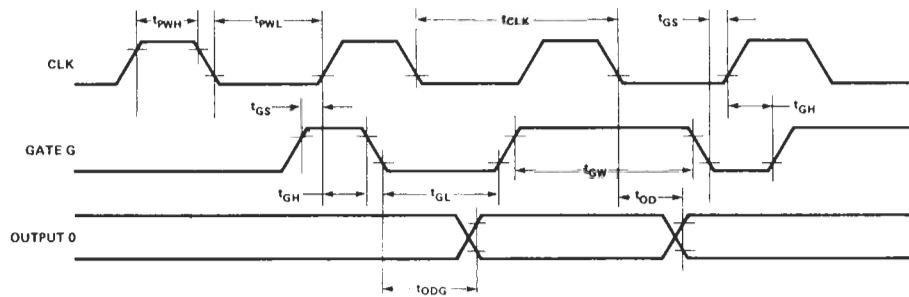
**Write Timing:****Read Timing:****Input Waveforms for A.C. Tests:**

**8253/8253-5**

**Clock and Gate Timing:**

| SYMBOL    | PARAMETER  | 8253 |      | 8253-5 |      | UNIT |
|-----------|--|------|------|--------|------|------|
|           |  | MIN. | MAX. | MIN.   | MAX. |      |
| $t_{CLK}$ | Clock Period                                       | 380  | dc   | 380    | dc   | ns   |
| $t_{PWH}$ | High Pulse Width                                   | 230  |      | 230    |      | ns   |
| $t_{PWL}$ | Low Pulse Width                                    | 150  |      | 150    |      | ns   |
| $t_{GW}$  | Gate Width High                                    | 150  |      | 150    |      | ns   |
| $t_{GL}$  | Gate Width Low                                     | 100  |      | 100    |      | ns   |
| $t_{GS}$  | Gate Set Up Time to CLK $\uparrow$                 | 100  |      | 100    |      | ns   |
| $t_{GH}$  | Gate Hold Time After CLK $\uparrow$                | 50   |      | 50     |      | ns   |
| $t_{OD}$  | Output Delay From CLK $\downarrow$ <sup>[1]</sup>  |      | 400  |        | 400  | ns   |
| $t_{ODG}$ | Output Delay From Gate $\downarrow$ <sup>[1]</sup> |      | 300  |        | 300  | ns   |

Note 1:  $C_L = 150pF$ .



# Programmable Array Logic Family

## PAL<sup>®</sup> Series 20

U.S. Patent 4124899

March 1981

### Features/Benefits

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin SKINNY DIP<sup>®</sup> packages.
- High speed: 25ns typical propagation delay.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature reduces possibility of copying by competitors.

### Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

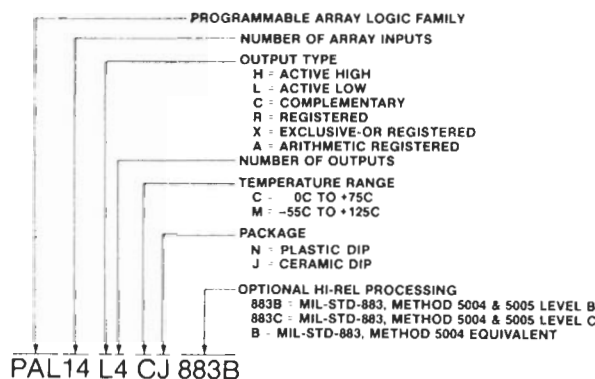
PAL<sup>®</sup> is a registered trademark of Monolithic Memories

| PART NUMBER | DESCRIPTION  |
|-------------|--|
| PAL10H8     | OCTAL 10 INPUT AND-OR GATE ARRAY                     |
| PAL12H6     | HEX 12 INPUT AND-OR GATE ARRAY                       |
| PAL14H4     | QUAD 14 INPUT AND-OR GATE ARRAY                      |
| PAL16H2     | DUAL 16 INPUT AND-OR GATE ARRAY                      |
| PAL16C1     | 16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY             |
| PAL10L8     | OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY              |
| PAL12L6     | HEX 12 INPUT AND-OR-INVERT GATE ARRAY                |
| PAL14L4     | QUAD 14 INPUT AND-OR-INVERT GATE ARRAY               |
| PAL16L2     | DUAL 16 INPUT AND-OR-INVERT GATE ARRAY               |
| PAL16L8     | OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY              |
| PAL16R8     | OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY          |
| PAL16R6     | HEX 16 INPUT REGISTERED AND-OR GATE ARRAY            |
| PAL16R4     | QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY           |
| PAL16X4     | QUAD 16 INPUT REGISTERED AND-OR-XOR GATE ARRAY       |
| PAL16A4     | QUAD 16 INPUT REGISTERED AND-CARRY-OR-XOR GATE ARRAY |

Unused inputs are tied directly to  $V_{CC}$  or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

### Ordering Information

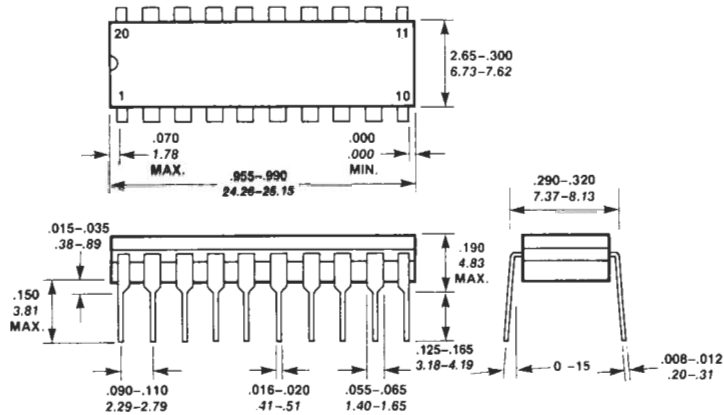


**PAL Series 20**

**J20 Ceramic DIP**

$\theta_{JA} = 75^\circ \text{C/W}$

$\theta_{JC} = 35^\circ \text{C/W}$

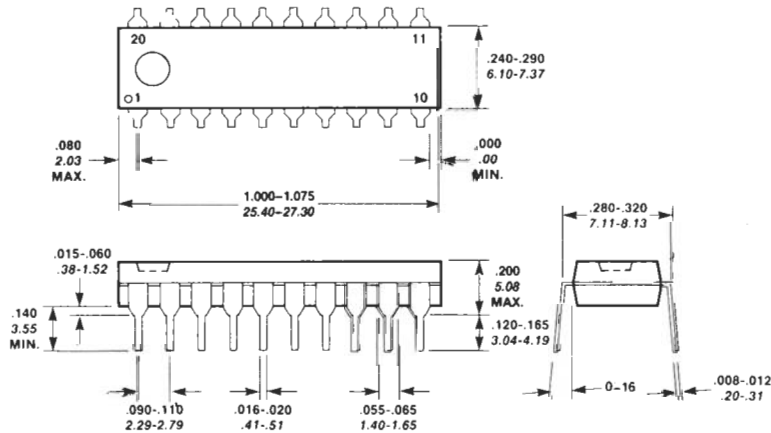


UNLESS OTHERWISE SPECIFIED:  
ALL DIMENSIONS MIN.-MAX. IN INCHES.  
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

**N20 Plastic Kool Dip™**

$\theta_{JA} = 75^\circ \text{C/W}$

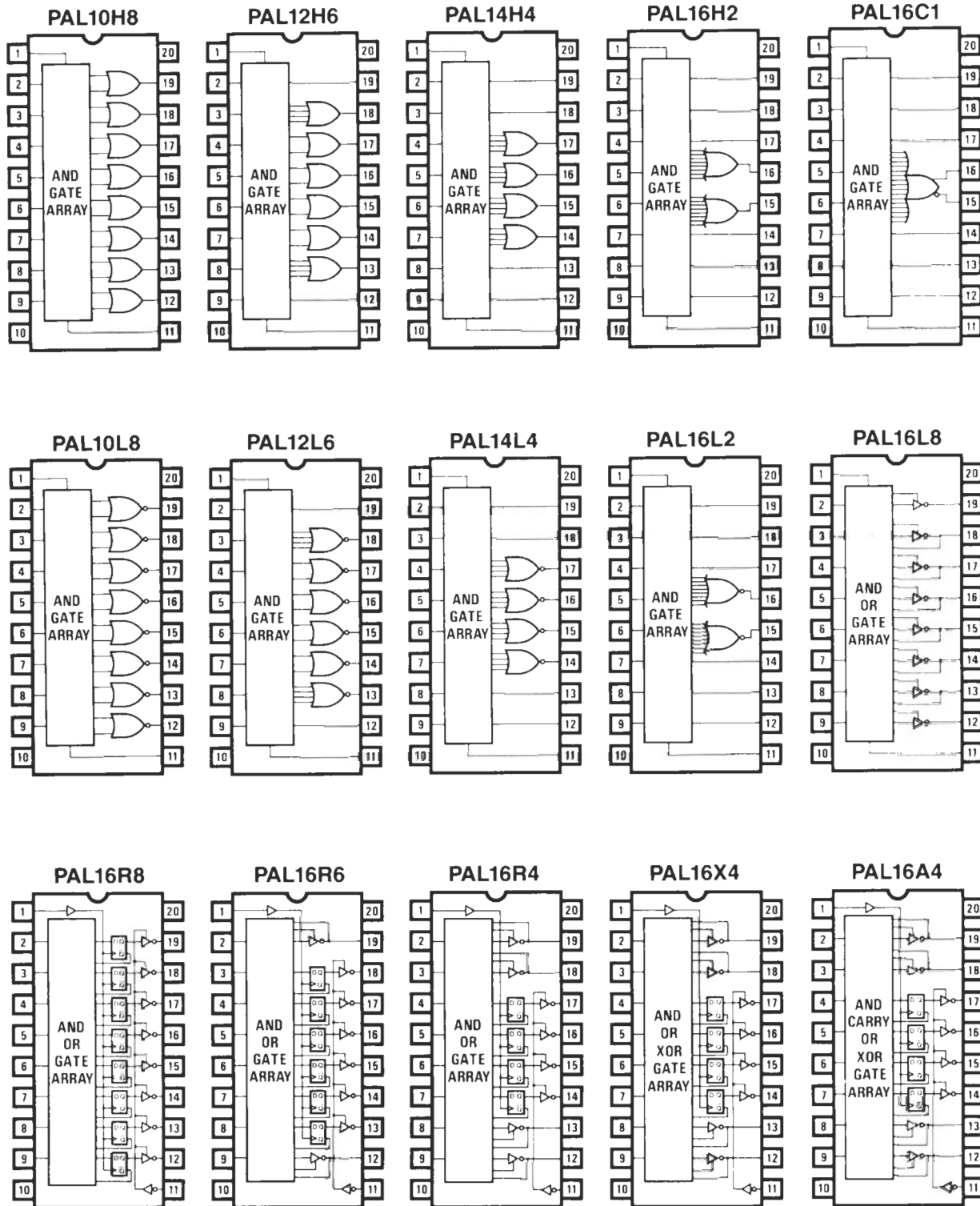
$\theta_{JC} = 35^\circ \text{C/W}$



UNLESS OTHERWISE SPECIFIED:  
ALL DIMENSIONS MIN.-MAX. IN INCHES.  
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.



**PAL Series 20**



**PAL Series 20**

**Absolute Maximum Ratings**

|                          | Operating      | Programming |
|--------------------------|----------------|-------------|
| Supply Voltage, VCC      | 7              | 12V         |
| Input Voltage            | 5.5V           | 12V*        |
| Off-state output Voltage | 5.5V           | 12V         |
| Storage temperature      | -65° to +150°C |             |

**Operating Conditions**

| SYMBOL          | PARAMETER                      | MILITARY |     |     | COMMERCIAL |     |      | UNIT |
|-----------------|--------------------------------|----------|-----|-----|------------|-----|------|------|
|                 |                                | MIN      | NOM | MAX | MIN        | NOM | MAX  |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5      | 5   | 5.5 | 4.75       | 5   | 5.25 | V    |
| T <sub>A</sub>  | Operating free-air temperature |          |     |     | 0          |     | 75   | °C   |
| T <sub>C</sub>  | Operating case temperature     | -55      |     | 125 |            |     |      | °C   |

**Electrical Characteristics Over Operating Conditions**

| SYMBOL           | PARAMETER                      | TEST CONDITIONS   |  | MIN                      | TYP                   | MAX   | UNIT |                        |     |
|------------------|--------------------------------|---|--|--------------------------|-----------------------|-------|------|------------------------|-----|
| V <sub>IL</sub>  | Low-level input voltage        |   |  |                          |                       | 0.8   | V    |                        |     |
| V <sub>IH</sub>  | High-level input voltage       |   |  | 2                        |                       |       | V    |                        |     |
| V <sub>IC</sub>  | Input clamp voltage            | V <sub>CC</sub> = MIN   | I <sub>I</sub> = -18mA                                   |                          |                       | -1.5  | V    |                        |     |
| I <sub>IL</sub>  | Low-level input current †      | V <sub>CC</sub> = MAX   | V <sub>I</sub> = 0.4V                                    |                          |                       | -0.25 | mA   |                        |     |
| I <sub>IH</sub>  | High-level input current †     | V <sub>CC</sub> = MAX   | V <sub>I</sub> = 2.4V                                    |                          |                       | 25    | μA   |                        |     |
| I <sub>I</sub>   | Maximum input current          | V <sub>CC</sub> = MAX   | V <sub>I</sub> = 5.5V                                    |                          |                       | 1     | mA   |                        |     |
| V <sub>OL</sub>  | Low-level output voltage       | V <sub>CC</sub> = MIN<br>V <sub>IL</sub> = 0.8V<br>V <sub>IH</sub> = 2V | 10H8, 12H6, 14H4<br>16H2, 16C1, 10L8<br>12L6, 14L4, 16L2 | MIL                      | I <sub>OL</sub> = 8mA | 0.5   | V    |                        |     |
|                  |                                |   | 16L8 16R8<br>16R6 16R4<br>16X4 16A4                      | COM                      |                       |       |      | I <sub>OL</sub> = 12mA |     |
|                  |                                |   |  | COM                      |                       |       |      | I <sub>OL</sub> = 24mA |     |
| V <sub>OH</sub>  | High-level output voltage      | V <sub>CC</sub> = MIN<br>V <sub>IL</sub> = 0.8V<br>V <sub>IH</sub> = 2V | MIL  | I <sub>OH</sub> = -2mA   | 2.4                   |       | V    |                        |     |
|                  |                                |   | COM  | I <sub>OH</sub> = -3.2mA |                       |       |      |                        |     |
| I <sub>OZL</sub> | Off-state output current †     | V <sub>CC</sub> = MAX<br>V <sub>IL</sub> = 0.8V<br>V <sub>IH</sub> = 2V | 16L8 16R8<br>16R6 16R4<br>16X4 16A4                      | V <sub>O</sub> = 0.4V    |                       | -100  | μA   |                        |     |
| I <sub>OZH</sub> |                                |   |  |                          |                       |       |      | V <sub>O</sub> = 2.4V  | 100 |
| I <sub>OS</sub>  | Output short-circuit current** | V <sub>CC</sub> = 5V  |  | V <sub>O</sub> = 0V      |                       | -30   | -130 | mA                     |     |
| I <sub>CC</sub>  | Supply current                 | V <sub>CC</sub> = MAX   | 10H8, 12H6, 14H4, 16H2, 16C1<br>10L8, 12L6, 14L4, 16L2   |                          |                       | 55    | 90   | mA                     |     |
|                  |                                |   | 16R4, 16R6,<br>16R8, 16L8                                | COM                      |                       |       | 120  |                        | 180 |
|                  |                                |   | 16L8   | MIL                      |                       |       | 140  |                        | 210 |
|                  |                                |   | 16R4, 16R6, 16R8   | MIL                      |                       |       | 150  |                        | 225 |
|                  |                                |   | 16X4   |                          |                       |       | 160  |                        | 225 |
|                  |                                |   | 16A4   |                          |                       |       | 170  |                        | 240 |

† I<sub>O</sub> pin leakage is the worst case of I<sub>OZL</sub> or I<sub>I</sub> e.g. I<sub>IL</sub> and I<sub>OZH</sub>

\* Pins 1 and 11 may be raised to 22V max

\*\* Only one output shorted at a time

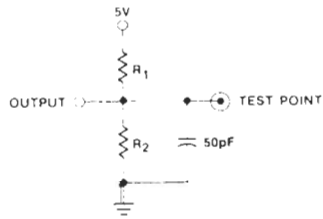
**PAL Series 20**

**Switching Characteristics**

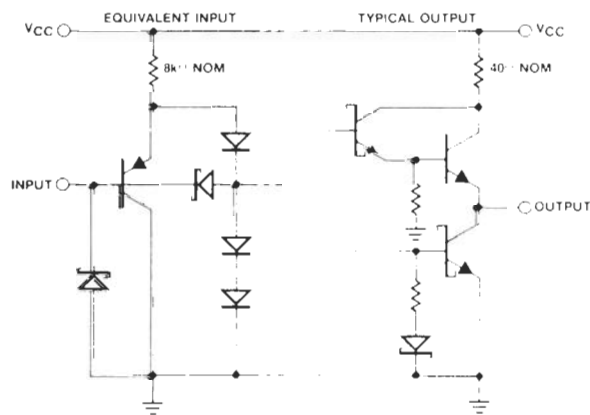
Over Operating Conditions

| SYMBOL    | PARAMETER  | TEST CONDITIONS                         | MILITARY          |     |     | COMMERCIAL |     |     | UNIT |
|-----------|--|---|-------------------|-----|-----|------------|-----|-----|------|
|           |  |   | MIN               | TYP | MAX | MIN        | TYP | MAX |      |
| $t_{PD}$  | Input to output<br>10H8 12H6 14H4<br>16H2 10L8 12L6<br>14L4 16L2<br>16C1 | $R_1 = 560\Omega$<br>$R_2 = 1.1k\Omega$ | 25                | 45  |     | 25         | 35  | ns  |      |
|           |  |   | 25                | 45  |     | 25         | 40  |     |      |
| $t_{PD}$  | Input or feedback to output  | 16R8 16R6 16R4 16L8<br>16X4 16A4        | 25                | 45  |     | 25         | 35  | ns  |      |
| $t_{CLK}$ | Clock to output or feedback  |   | 15                | 25  |     | 15         | 25  | ns  |      |
| $t_{PZX}$ | Pin 11 to output enable  |   | 15                | 25  |     | 15         | 25  | ns  |      |
| $t_{PXZ}$ | Pin 11 to output disable   |   | 15                | 25  |     | 15         | 25  | ns  |      |
| $t_{PZX}$ | Input to output enable   |   | 25                | 45  |     | 25         | 35  | ns  |      |
| $t_{PXZ}$ | Input to output disable  |   | 25                | 45  |     | 25         | 35  | ns  |      |
| $t_W$     | Width of clock<br>Low<br>High  |   | $R_1 = 200\Omega$ | 25  |     |            | 25  |     | ns   |
|           |  | $R_2 = 390\Omega$                       | 25                |     |     | 25         |     |     |      |
| $t_{SU}$  | Setup time from input or feedback<br>16R8 16R6 16R4<br>16X4 16A4         |   | 45                |     |     | 35         |     | ns  |      |
|           |  |   | 55                |     |     | 45         |     |     |      |
| $t_H$     | Hold time  |   | 0                 | -15 |     | 0          | -15 | ns  |      |
| $f_{MAX}$ | Maximum frequency<br>16R8 16R6 16R4<br>16X4 16A4                         |   | 14                |     |     | 16         |     | MHz |      |
|           |  |   | 12                |     |     | 14         |     |     |      |

**Test Load**



**Schematic of Inputs and Outputs**



**Available Programmers**

| MANUFACTURER                        | PERSONALITY CARD SET | SOCKET ADAPTER CONFIGURATION   |
|-------------------------------------|----------------------|--|
| Cybernetic Programming Systems, Inc | CYMPC-1              |  |
| Data I/O Corporation                | 909-1427             | 715 1428-1<br>715 1428-2<br>715 1428-3                                     |
| Pro-Log Corporation                 | PM9068               |  |
| Stag Systems                        | PM202                | AM10H8 AM10L8<br>AM12H6 AM12L6<br>AM14H4 AM14L4<br>AM16H2 AM16L2<br>AM16C1 |
| Structured Design                   | SD20/24              |  |

**PAL Series 20**

**Programming**

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

- Step 1 Raise Output Disable, OD, to  $V_{IHH}$
- Step 2 Select an input line by specifying  $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$  and L/R as shown in Table 1.
- Step 3 Select a product line by specifying  $A_0, A_1$  and  $A_2$  one-of-eight select as shown in Table 2.
- Step 4 Raise  $V_{CC}$  (pin 20) to  $V_{IHH}$

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to  $V_{IHH}$  as shown in Programming Waveform.

Step 6 Lower  $V_{CC}$  (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower  $V_{CC}$  (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to  $V_P$ .  $V_{CC}$  is not required during this operation.

**Voltage Legend**

L = Low-level input voltage,  $V_{IL}$   
 H = High-level input voltage,  $V_{IH}$   
 HH = High-level program voltage,  $V_{IHH}$   
 Z = High impedance (e.g., 10k $\Omega$  to 5.0V)

| INPUT LINE NUMBER | PIN IDENTIFICATION |    |    |    |    |    |    |    | L/R |
|-------------------|--------------------|----|----|----|----|----|----|----|-----|
|                   | I7                 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |     |
| 0                 | HH                 | HH | HH | HH | HH | HH | HH | L  | Z   |
| 1                 | HH                 | HH | HH | HH | HH | HH | HH | H  | Z   |
| 2                 | HH                 | HH | HH | HH | HH | HH | HH | L  | HH  |
| 3                 | HH                 | HH | HH | HH | HH | HH | HH | H  | HH  |
| 4                 | HH                 | HH | HH | HH | HH | HH | L  | HH | Z   |
| 5                 | HH                 | HH | HH | HH | HH | HH | H  | HH | Z   |
| 6                 | HH                 | HH | HH | HH | HH | HH | L  | HH | HH  |
| 7                 | HH                 | HH | HH | HH | HH | HH | H  | HH | HH  |
| 8                 | HH                 | HH | HH | HH | HH | L  | HH | HH | Z   |
| 9                 | HH                 | HH | HH | HH | HH | H  | HH | HH | Z   |
| 10                | HH                 | HH | HH | HH | HH | L  | HH | HH | HH  |
| 11                | HH                 | HH | HH | HH | HH | H  | HH | HH | HH  |
| 12                | HH                 | HH | HH | HH | L  | HH | HH | HH | Z   |
| 13                | HH                 | HH | HH | HH | H  | HH | HH | HH | Z   |
| 14                | HH                 | HH | HH | HH | L  | HH | HH | HH | HH  |
| 15                | HH                 | HH | HH | HH | H  | HH | HH | HH | HH  |
| 16                | HH                 | HH | HH | L  | HH | HH | HH | HH | Z   |
| 17                | HH                 | HH | HH | H  | HH | HH | HH | HH | Z   |
| 18                | HH                 | HH | HH | L  | HH | HH | HH | HH | HH  |
| 19                | HH                 | HH | HH | H  | HH | HH | HH | HH | HH  |
| 20                | HH                 | HH | L  | HH | HH | HH | HH | HH | Z   |
| 21                | HH                 | HH | H  | HH | HH | HH | HH | HH | Z   |
| 22                | HH                 | HH | L  | HH | HH | HH | HH | HH | HH  |
| 23                | HH                 | HH | H  | HH | HH | HH | HH | HH | HH  |
| 24                | HH                 | L  | HH | HH | HH | HH | HH | HH | Z   |
| 25                | HH                 | H  | HH | HH | HH | HH | HH | HH | Z   |
| 26                | HH                 | L  | HH | HH | HH | HH | HH | HH | HH  |
| 27                | HH                 | H  | HH | HH | HH | HH | HH | HH | HH  |
| 28                | L                  | HH | HH | HH | HH | HH | HH | HH | Z   |
| 29                | H                  | HH | HH | HH | HH | HH | HH | HH | Z   |
| 30                | L                  | HH | HH | HH | HH | HH | HH | HH | HH  |
| 31                | H                  | HH | HH | HH | HH | HH | HH | HH | HH  |

Table 1 Input Line Select

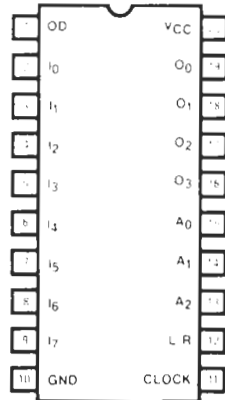
| PRODUCT LINE NUMBER | PIN IDENTIFICATION |    |    |    |    |    |    |
|---------------------|--------------------|----|----|----|----|----|----|
|                     | O3                 | O2 | O1 | O0 | A2 | A1 | A0 |
| 0, 32               | Z                  | Z  | Z  | HH | Z  | Z  | Z  |
| 1, 33               | Z                  | Z  | Z  | HH | Z  | Z  | HH |
| 2, 34               | Z                  | Z  | Z  | HH | Z  | HH | Z  |
| 3, 35               | Z                  | Z  | Z  | HH | Z  | HH | HH |
| 4, 36               | Z                  | Z  | Z  | HH | HH | Z  | Z  |
| 5, 37               | Z                  | Z  | Z  | HH | HH | Z  | HH |
| 6, 38               | Z                  | Z  | Z  | HH | HH | HH | Z  |
| 7, 39               | Z                  | Z  | Z  | HH | HH | HH | HH |
| 8, 40               | Z                  | Z  | HH | Z  | Z  | Z  | Z  |
| 9, 41               | Z                  | Z  | HH | Z  | Z  | Z  | HH |
| 10, 42              | Z                  | Z  | HH | Z  | Z  | HH | Z  |
| 11, 43              | Z                  | Z  | HH | Z  | Z  | HH | HH |
| 12, 44              | Z                  | Z  | HH | Z  | HH | Z  | Z  |
| 13, 45              | Z                  | Z  | HH | Z  | HH | Z  | HH |
| 14, 46              | Z                  | Z  | HH | Z  | HH | HH | Z  |
| 15, 47              | Z                  | Z  | HH | Z  | HH | HH | HH |
| 16, 48              | Z                  | HH | Z  | Z  | Z  | Z  | Z  |
| 17, 49              | Z                  | HH | Z  | Z  | Z  | Z  | HH |
| 18, 50              | Z                  | HH | Z  | Z  | Z  | HH | Z  |
| 19, 51              | Z                  | HH | Z  | Z  | Z  | HH | HH |
| 20, 52              | Z                  | HH | Z  | Z  | HH | Z  | Z  |
| 21, 53              | Z                  | HH | Z  | Z  | HH | Z  | HH |
| 22, 54              | Z                  | HH | Z  | Z  | HH | HH | Z  |
| 23, 55              | Z                  | HH | Z  | Z  | HH | HH | HH |
| 24, 56              | HH                 | Z  | Z  | Z  | Z  | Z  | Z  |
| 25, 57              | HH                 | Z  | Z  | Z  | Z  | Z  | HH |
| 26, 58              | HH                 | Z  | Z  | Z  | Z  | HH | Z  |
| 27, 59              | HH                 | Z  | Z  | Z  | Z  | HH | HH |
| 28, 60              | HH                 | Z  | Z  | Z  | HH | Z  | Z  |
| 29, 61              | HH                 | Z  | Z  | Z  | HH | Z  | HH |
| 30, 62              | HH                 | Z  | Z  | Z  | HH | HH | Z  |
| 31, 63              | HH                 | Z  | Z  | Z  | HH | HH | HH |

Table 2 Product Line Select

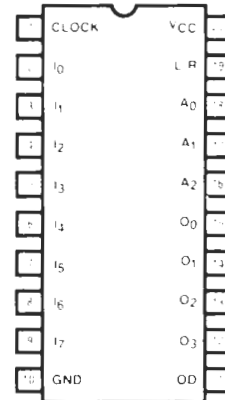
**PAL Series 20**

**Pin Configurations**

PRODUCTS 0 THRU 31



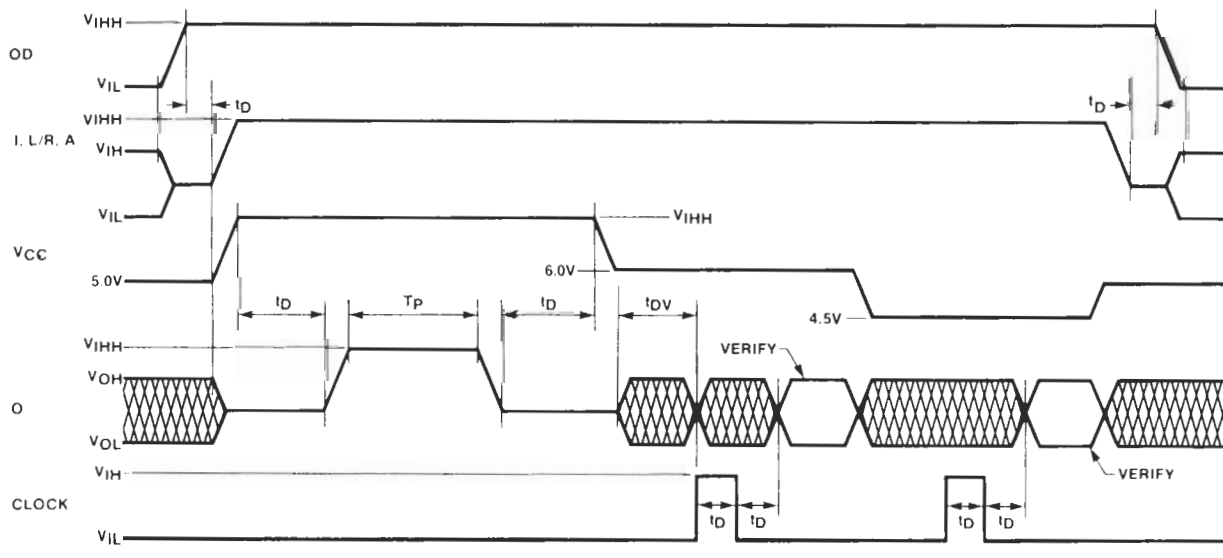
PRODUCTS 32 THRU 63



**Programming Parameters**  $T_A = 25^\circ C$

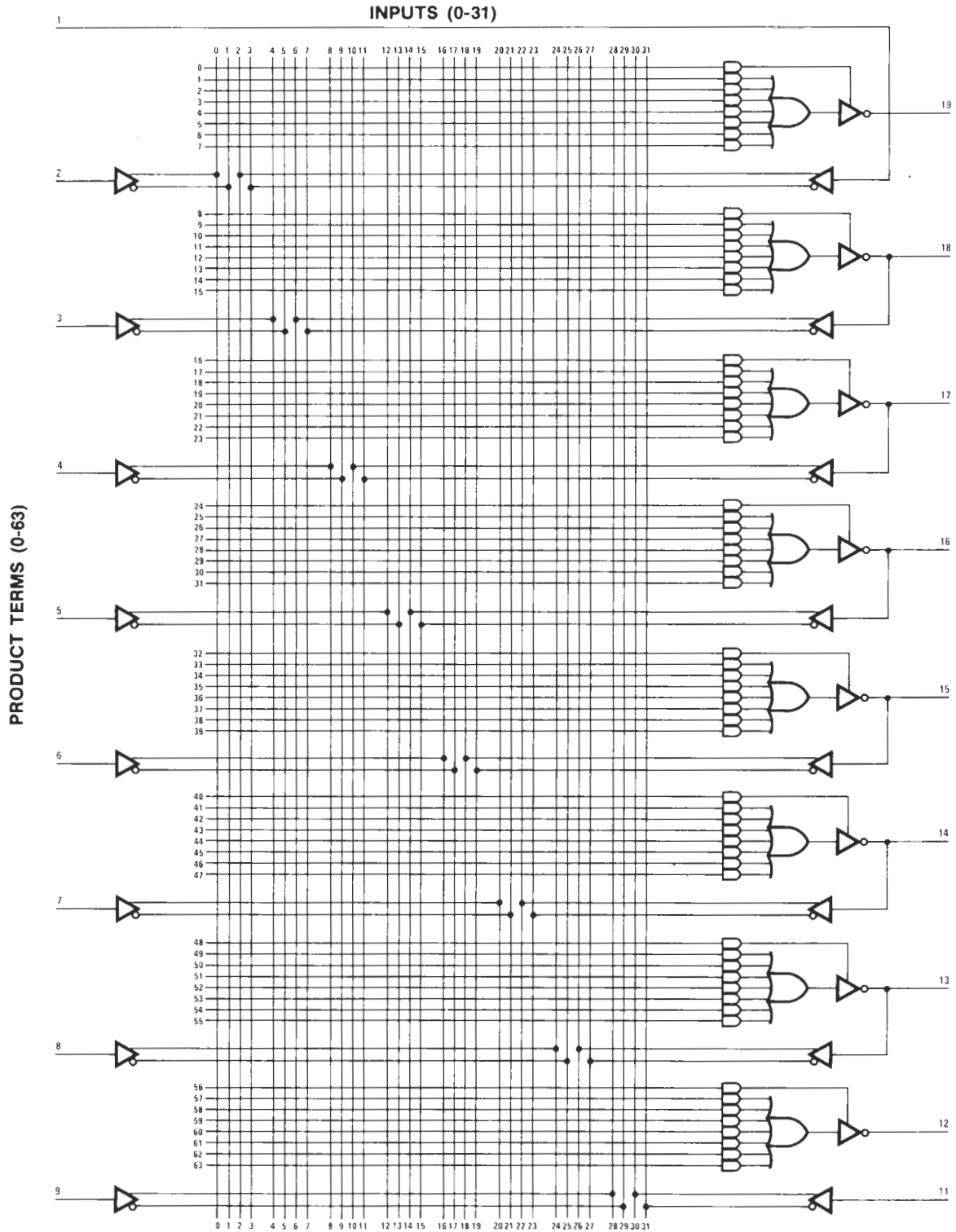
| SYMBOL    | PARAMETER                    | LIMITS               |      |     | UNIT    |
|-----------|------------------------------|----------------------|------|-----|---------|
|           |                              | MIN                  | TYP  | MAX |         |
| $V_{IH}$  | Program-level input voltage  | 11                   | 11.5 | 12  | V       |
| $I_{IH}$  | Program-level input current  |                      |      | 50  | mA      |
|           |                              | Output Program Pulse |      | 25  |         |
|           |                              | OD, L/R              |      | 5   |         |
| $I_{CCH}$ | Program Supply Current       |                      |      | 400 | mA      |
| $T_P$     | Program Pulse Width          | 10                   |      | 50  | $\mu s$ |
| $t_D$     | Delay time                   | 100                  |      |     | ns      |
| $t_{DV}$  | Delay Time to Verify         | 100                  |      |     | $\mu s$ |
|           | Program Pulse duty cycle     |                      |      | 25  | %       |
| $V_P$     | Verify-Protect-input voltage | 20                   | 21   | 22  | V       |
| $I_P$     | Verify-Protect-input current |                      |      | 400 | mA      |
| $T_{PP}$  | Verify-Protect Pulse Width   | 20                   |      | 50  | msec    |

**Programming Waveforms**



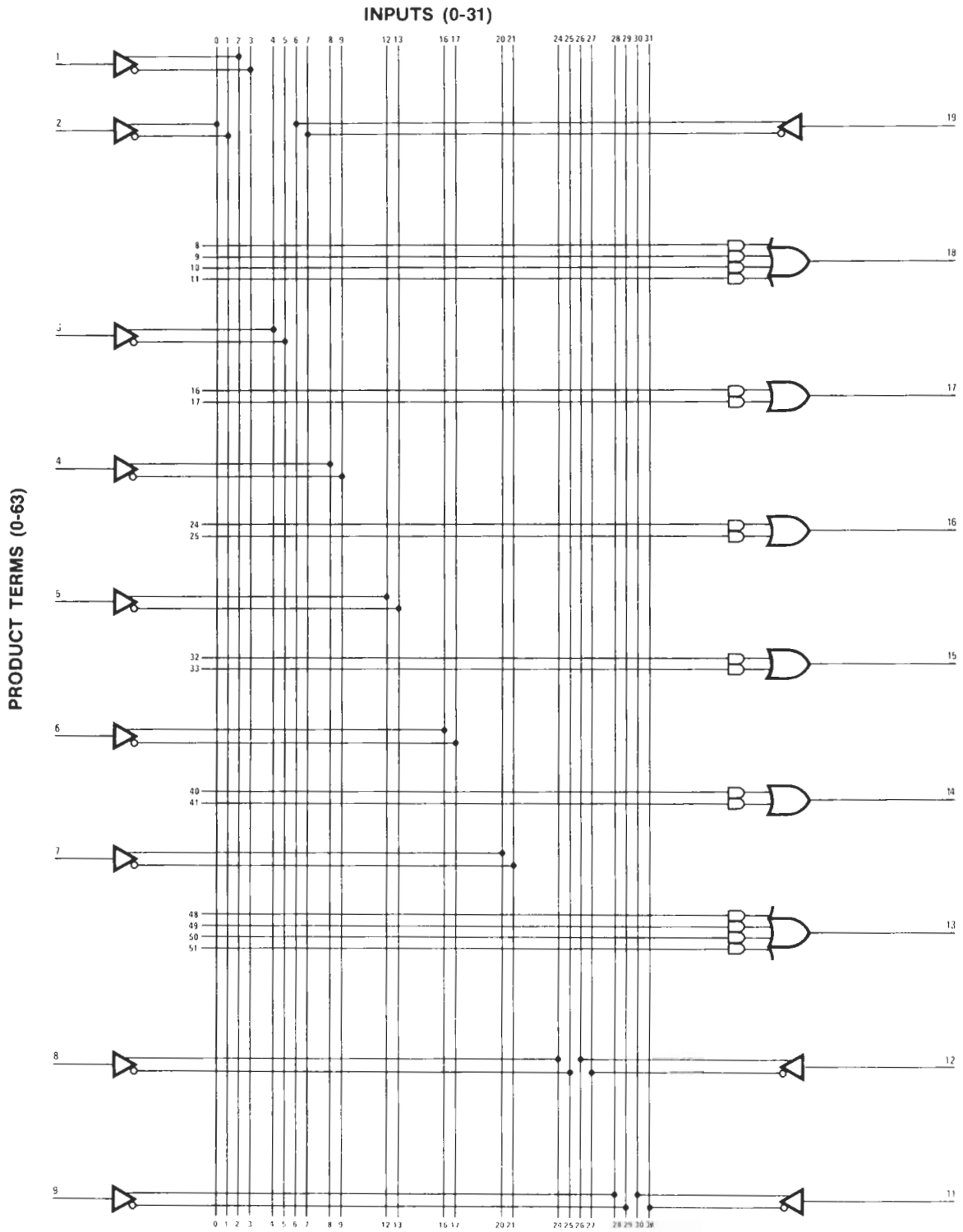
PAL Series 20

Logic Diagram PAL16L8



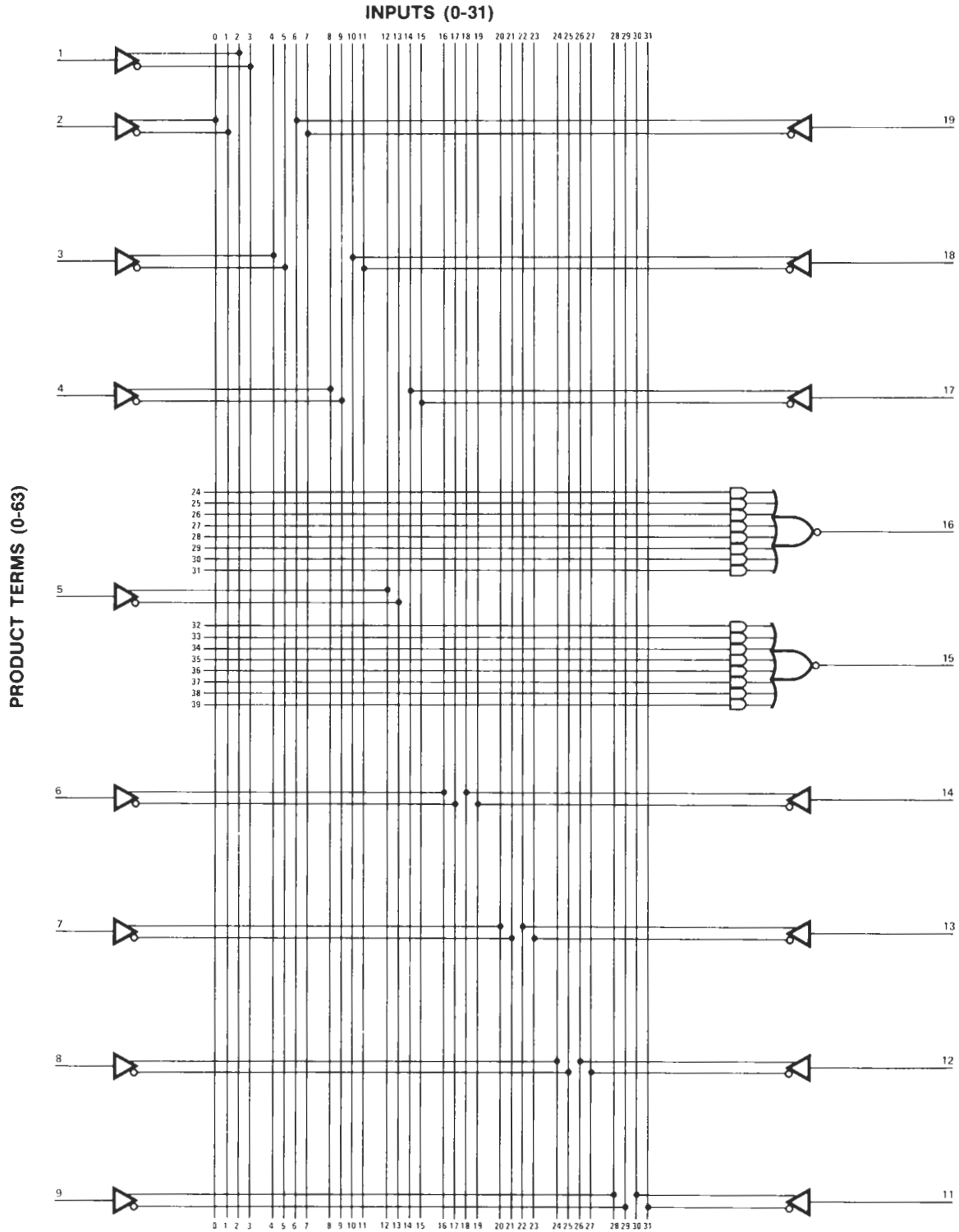
PAL Series 20

Logic Diagram PAL12H6



PAL Series 20

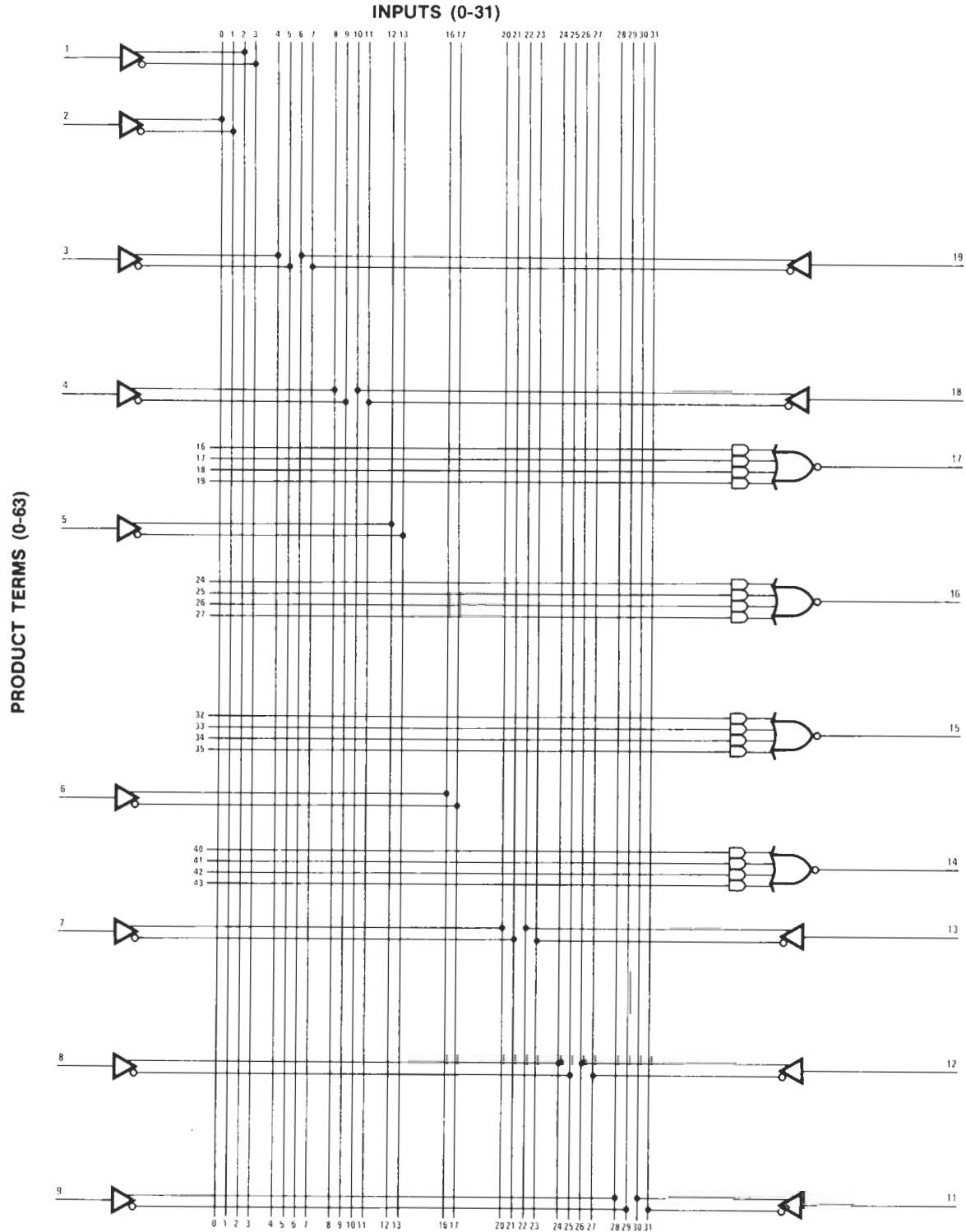
Logic Diagram PAL16L2





PAL Series 20

Logic Diagram PAL14L4



# Am27S20 • Am27S21

## 1024-Bit Generic Series Bipolar PROM

### DISTINCTIVE CHARACTERISTICS

- High Speed – 45ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N<sup>2</sup> patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

### GENERIC SERIES CHARACTERISTICS

The Am27S20 and Am27S21 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

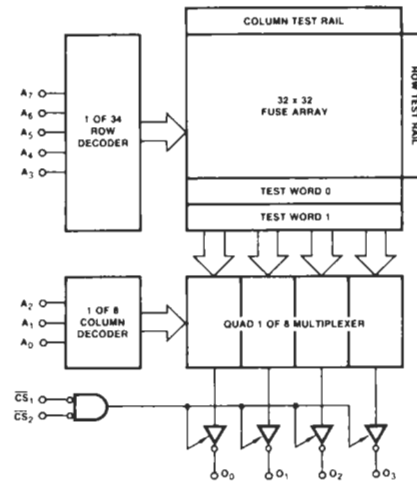
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

### FUNCTIONAL DESCRIPTION

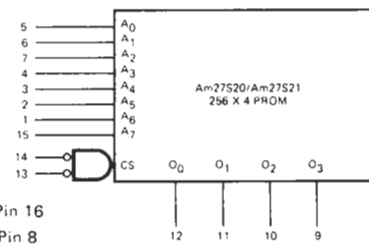
The Am27S20 and Am27S21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am27S20 and three-state Am27S21 output versions. After programming, stored information is read on outputs O<sub>0</sub>–O<sub>3</sub> by applying unique binary addresses to A<sub>0</sub>–A<sub>7</sub> and holding the chip select inputs,  $\overline{CS}_1$  and  $\overline{CS}_2$ , at a logic LOW. If either chip select input goes to a logic HIGH, O<sub>0</sub>–O<sub>3</sub> go to the off or high impedance state.

### BLOCK DIAGRAM



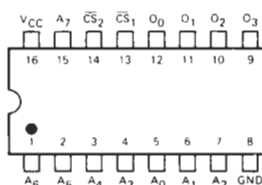
BPM-027

### LOGIC SYMBOL



BPM-028

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

BPM-029

### ORDERING INFORMATION

| Package Type        | Temperature Range | Order Number |
|---------------------|-------------------|--------------|
| Open Collectors     |                   |              |
| Hermetic DIP        | 0°C to +75°C      | AM27S20DC    |
| Hermetic DIP        | -55°C to +125°C   | AM27S20DM    |
| Hermetic Flat Pak   | -55°C to +125°C   | AM27S20FM    |
| Three-State Outputs |                   |              |
| Hermetic DIP        | 0°C to +75°C      | AM27S21DC    |
| Hermetic DIP        | -55°C to +125°C   | AM27S21DM    |
| Hermetic Flat Pak   | -55°C to +125°C   | AM27S21FM    |

**Am27S20 • Am27S21****MAXIMUM RATINGS** (Above which the useful life may be impaired)

|  |                                |
|--|--------------------------------|
| Storage Temperature  | -65°C to +150°C                |
| Temperature (Ambient) Under Bias   | -55°C to +125°C                |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous          | -0.5V to +7.0V                 |
| DC Voltage Applied to Outputs (Except During Programming)                | -0.5V to +V <sub>CC</sub> max. |
| DC Voltage Applied to Outputs During Programming                         | 21V                            |
| Output Current into Outputs During Programming (Max. Duration of 1 sec.) | 200mA                          |
| DC Input Voltage   | -0.5V to +5.5V                 |
| DC Input Current   | -30mA to +5mA                  |

**OPERATING RANGE**

|       |                      |                                  |                             |
|-------|----------------------|----------------------------------|-----------------------------|
| COM'L | Am27S20XC, Am27S21XC | T <sub>A</sub> = 0°C to +75°C    | V <sub>CC</sub> = 5.0V ±5%  |
| MIL   | Am27S20XM, Am27S21XM | T <sub>A</sub> = -55°C to +125°C | V <sub>CC</sub> = 5.0V ±10% |

**ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE** (Unless Otherwise Noted)  
**PRELIMINARY DATA**

| Parameters                        | Description                  | Test Conditions  | Min. | Typ.<br>(Note 1) | Max.                  | Units |    |
|-----------------------------------|------------------------------|--|------|------------------|-----------------------|-------|----|
| V <sub>OH</sub><br>(Am27S21 only) | Output HIGH Voltage          | V <sub>CC</sub> = MIN., I <sub>OH</sub> = -2.0mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4  |                  |                       | Volts |    |
| V <sub>OL</sub>                   | Output LOW Voltage           | V <sub>CC</sub> = MIN., I <sub>OL</sub> = 16mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |      |                  | 0.45                  | Volts |    |
| V <sub>IH</sub>                   | Input HIGH Level             | Guaranteed input logical HIGH voltage for all inputs   | 2.0  |                  |                       | Volts |    |
| V <sub>IL</sub>                   | Input LOW Level              | Guaranteed input logical LOW voltage for all inputs  |      |                  | 0.8                   | Volts |    |
| I <sub>IL</sub>                   | Input LOW Current            | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.45V  |      | -0.010           | -0.250                | mA    |    |
| I <sub>IH</sub>                   | Input HIGH Current           | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.7V   |      |                  | 25                    | μA    |    |
| I <sub>I</sub>                    | Input HIGH Current           | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5V   |      |                  | 1.0                   | mA    |    |
| I <sub>SC</sub><br>(Am27S21 only) | Output Short Circuit Current | V <sub>CC</sub> = MAX., V <sub>OUT</sub> = 0.0V (Note 2)   | -20  | -40              | -90                   | mA    |    |
| I <sub>CC</sub>                   | Power Supply Current         | All inputs - GND<br>V <sub>CC</sub> = MAX.   |      | 95               | 130                   | mA    |    |
| V <sub>I</sub>                    | Input Clamp Voltage          | V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA  |      |                  | -1.2                  | Volts |    |
| I <sub>CEX</sub>                  | Output Leakage Current       | V <sub>CC</sub> = MAX.<br>V <sub>CS1</sub> = 2.4V  |      | Am27S21<br>only  | V <sub>O</sub> = 4.5V | 40    | μA |
|                                   |                              |  |      |                  | V <sub>O</sub> = 2.4V | 40    |    |
|                                   |                              |  |      |                  | V <sub>O</sub> = 0.4V | -40   |    |
| C <sub>IN</sub>                   | Input Capacitance            | V <sub>IN</sub> = 2.0V @ f = 1 MHz (Note 3)  |      | 4                |                       | pF    |    |
| C <sub>OUT</sub>                  | Output Capacitance           | V <sub>OUT</sub> = 2.0V @ f = 1 MHz (Note 3)   |      | 8                |                       |       |    |

Note 1. Typical limits are at V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

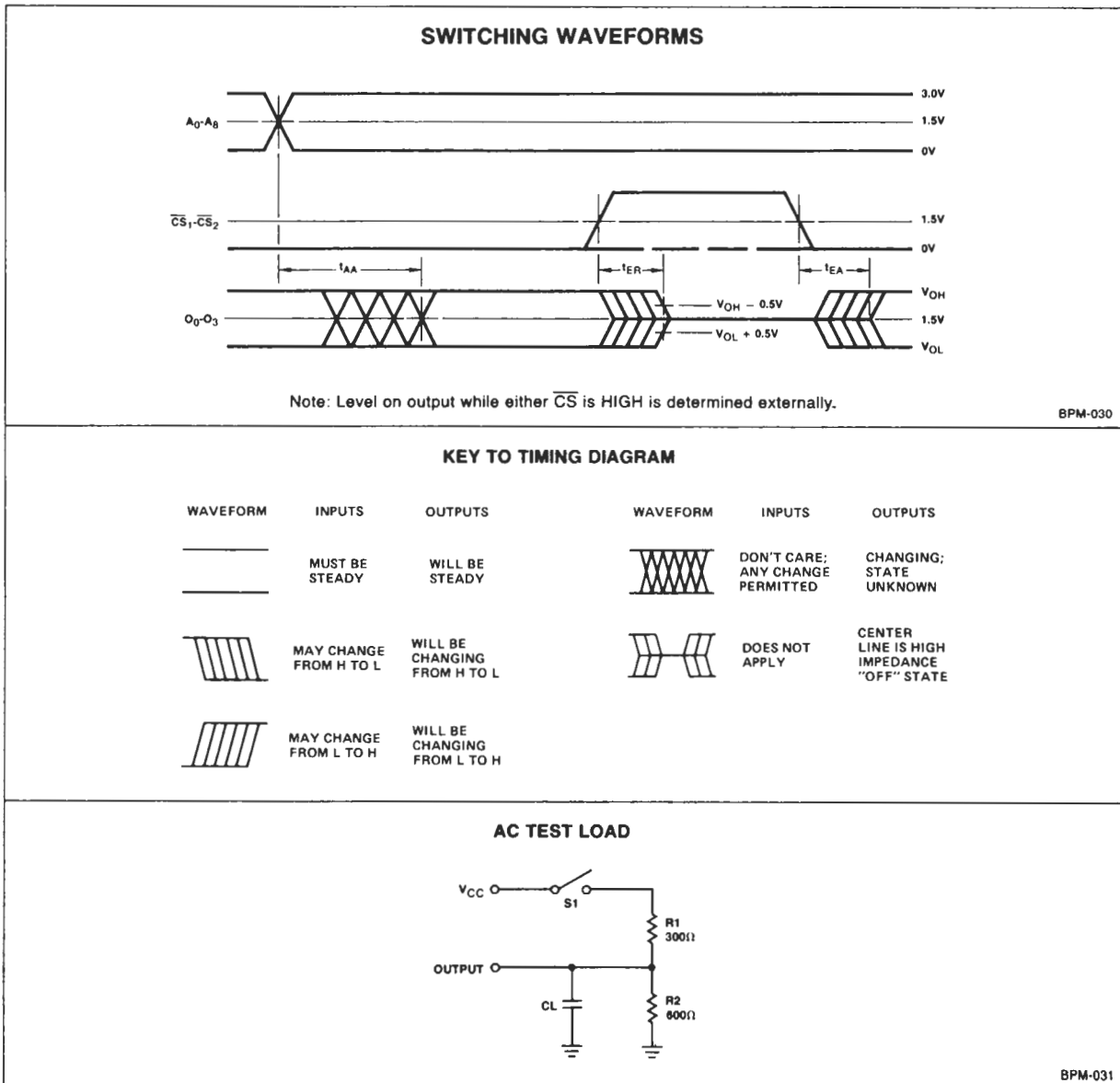
3. These parameters are not 100% tested, but are periodically sampled.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**  
PRELIMINARY DATA

**Am27S20 • Am27S21**

| Parameter | Description          | Test Conditions                 | Typ        | Max   |     | Units |
|-----------|----------------------|---------------------------------|------------|-------|-----|-------|
|           |                      |                                 | 5V<br>25°C | COM'L | MIL |       |
| $t_{AA}$  | Address Access Time  | AC Test Load<br>(See Notes 1-3) | 25         | 45    | 60  | ns    |
| $t_{EA}$  | Enable Access Time   |                                 | 15         | 20    | 30  | ns    |
| $t_{ER}$  | Enable Recovery Time |                                 | 15         | 20    | 30  | ns    |

- Notes: 1.  $t_{AA}$  is tested with switch  $S_1$  closed and  $C_L = 30\text{pF}$ .  
 2. For open collector outputs,  $t_{EA}$  and  $t_{ER}$  are tested with  $S_1$  closed to the 1.5V output level.  $C_L = 30\text{pF}$ .  
 3. For three state outputs,  $t_{EA}$  is tested with  $C_L = 30\text{pF}$  to the 1.5V level;  $S_1$  is open for high impedance to HIGH tests and closed for high impedance to LOW tests.  $t_{ER}$  is tested with  $C_L = 5\text{pF}$ . HIGH to high impedance tests are made with  $S_1$  open to an output voltage of  $V_{OH} - 0.5\text{V}$ ; LOW to high impedance tests are made with  $S_1$  closed to the  $V_{OL} + 0.5\text{V}$  level.



## Am27S20 • Am27S21

## PROGRAMMING

The Am27S20 and Am27S21 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the  $\overline{CS}_1$  input is at a logic HIGH. Current is gated through the addressed fuse by raising the  $\overline{CS}_1$  input from a logic HIGH to 15 volts. After 50  $\mu\text{sec}$ , the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50  $\mu\text{sec}$ . Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which

the current drops to approximately 40mA. Current into the  $\overline{CS}_1$  pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including  $V_{CC}$  should be removed for a period of 5 seconds after which programming may be resumed.

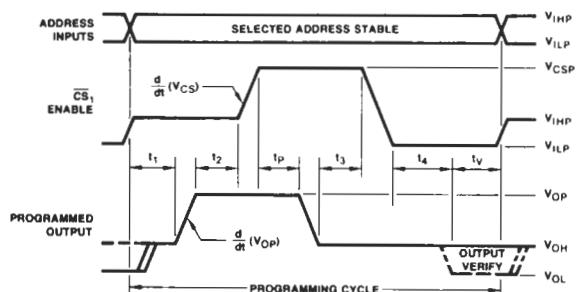
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING PARAMETERS

| Parameter      | Description                                  | Min. | Max.            | Units              |
|----------------|--|------|-----------------|--------------------|
| $V_{CCP}$      | $V_{CC}$ During Programming                  | 5.0  | 5.5             | Volts              |
| $V_{IHP}$      | Input HIGH Level During Programming          | 2.4  | 5.5             | Volts              |
| $V_{ILP}$      | Input LOW Level During Programming           | 0.0  | 0.45            | Volts              |
| $V_{CSP}$      | $\overline{CS}_1$ Voltage During Programming | 14.5 | 15.5            | Volts              |
| $V_{OP}$       | Output Voltage During Programming            | 19.5 | 20.5            | Volts              |
| $V_{ONP}$      | Voltage on Outputs Not to be Programmed      | 0    | $V_{CCP} + 0.3$ | Volts              |
| $I_{ONP}$      | Current into Outputs Not to be Programmed    |      | 20              | mA                 |
| $d(V_{OP})/dt$ | Rate of Output Voltage Change                | 20   | 250             | V/ $\mu\text{sec}$ |
| $d(V_{CS})/dt$ | Rate of $\overline{CS}_1$ , Voltage Change   | 100  | 1000            | V/ $\mu\text{sec}$ |
| $t_p$          | Programming Period – First Attempt           | 50   | 100             | $\mu\text{sec}$    |
|                | Programming Period – Subsequent Attempts     | 5.0  | 15              | msec               |

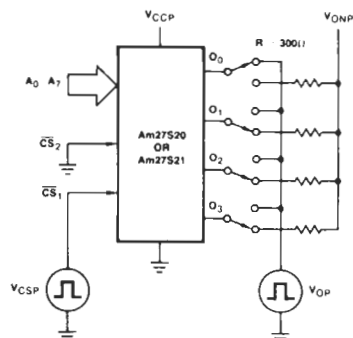
- Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.  
 2. Delays  $t_1$ ,  $t_2$ ,  $t_3$  and  $t_4$  must be greater than 100 ns; maximum delays of 1  $\mu\text{sec}$  are recommended to minimize heating during programming.  
 3. During  $t_v$ , a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.  
 4. Outputs not being programmed are connected to  $V_{ONP}$  through resistor R which provides output current limiting.

## PROGRAMMING WAVEFORMS



BPM-032

## SIMPLIFIED PROGRAMMING DIAGRAM



BPM-033

**PROGRAMMING EQUIPMENT**

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic

programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

|   |   |  |
|---|---|--|
| SOURCE AND LOCATION                         | Data I/O Corp.<br>P.O. Box 308<br>Issaquah, Wash. 98027 | Pro-Log Corp.<br>2411 Garden Road<br>Monterey, Ca. 93940 |
| PROGRAMMER MODEL(S)                         | Model 5, 7 and 9  | M900 and M920  |
| AMD GENERIC BIPOLAR PROM PERSONALITY BOARD  | 909-1286-1  | PM9058   |
| Am27S20 • Am27S21 ADAPTERS AND CONFIGURATOR | 715-1408-1  | PA16-5 and 256 x 4 (L)                                   |

**OBTAINING PROGRAMMED UNITS**

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

**ASCII BPNF**

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 256 words, starting with word 0, in the following format:
  - a. Any characters, including carriage return and line feed, except "B".
  - b. The letter "B", indicating the beginning of the data word.
  - c. A sequence of four Ps or Ns, starting with output O<sub>3</sub>.
  - d. The letter "F", indicating the finish of the data word.
  - e. Any text, including carriage return and line feed, except the letter "B".

3. A trailer of at least 25 rubouts.
- A P is a HIGH logic level = 2.4 volts.  
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

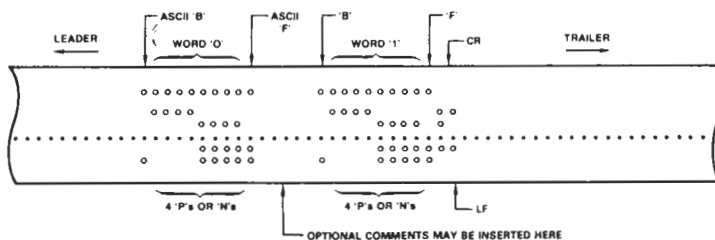
**TYPICAL PAPER TAPE FORMAT**

|     |       |               |     |     |     |
|-----|-------|---------------|-----|-----|-----|
| ∅∅∅ | BNNNF | WORD ZERO     | (R) | (L) | (L) |
|     | BPPNF | COMMENT FIELD | (R) | (L) |     |
| ∅∅2 | BPPNF | ANY           | (R) | (L) |     |
|     | BNNNF | TEXT          | (R) | (L) |     |
| ∅∅4 | BNNNF | CAN           | (R) | (L) |     |
|     | BPPNF | GO            | (R) | (L) |     |
| ∅∅6 | BPPNF | HERE          | (R) | (L) |     |
| .   | ..... | .             |     |     |     |
| 255 | BPPNF | END           | (R) | (L) |     |

**RESULTING DEVICE TRUTH TABLE ( $\overline{CS}_1$  &  $\overline{CS}_2$  = LOW)**

| A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | O <sub>3</sub> | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| L              | L              | L              | L              | L              | L              | L              | L              | L              | L              | L              | H              |
| L              | L              | L              | L              | L              | L              | L              | H              | H              | H              | L              | L              |
| L              | L              | L              | L              | L              | L              | H              | L              | H              | H              | H              | L              |
| L              | L              | L              | L              | L              | H              | H              | L              | L              | L              | L              | L              |
| L              | L              | L              | L              | L              | H              | L              | L              | L              | L              | L              | H              |
| L              | L              | L              | L              | L              | H              | L              | H              | H              | H              | L              | L              |
| L              | L              | L              | L              | L              | H              | H              | L              | H              | H              | L              | L              |
|                |                |                |                |                |                |                |                |                |                |                |                |
| H              | H              | H              | H              | H              | H              | H              | H              | H              | H              | H              | L              |

**ASCII PAPER TAPE**

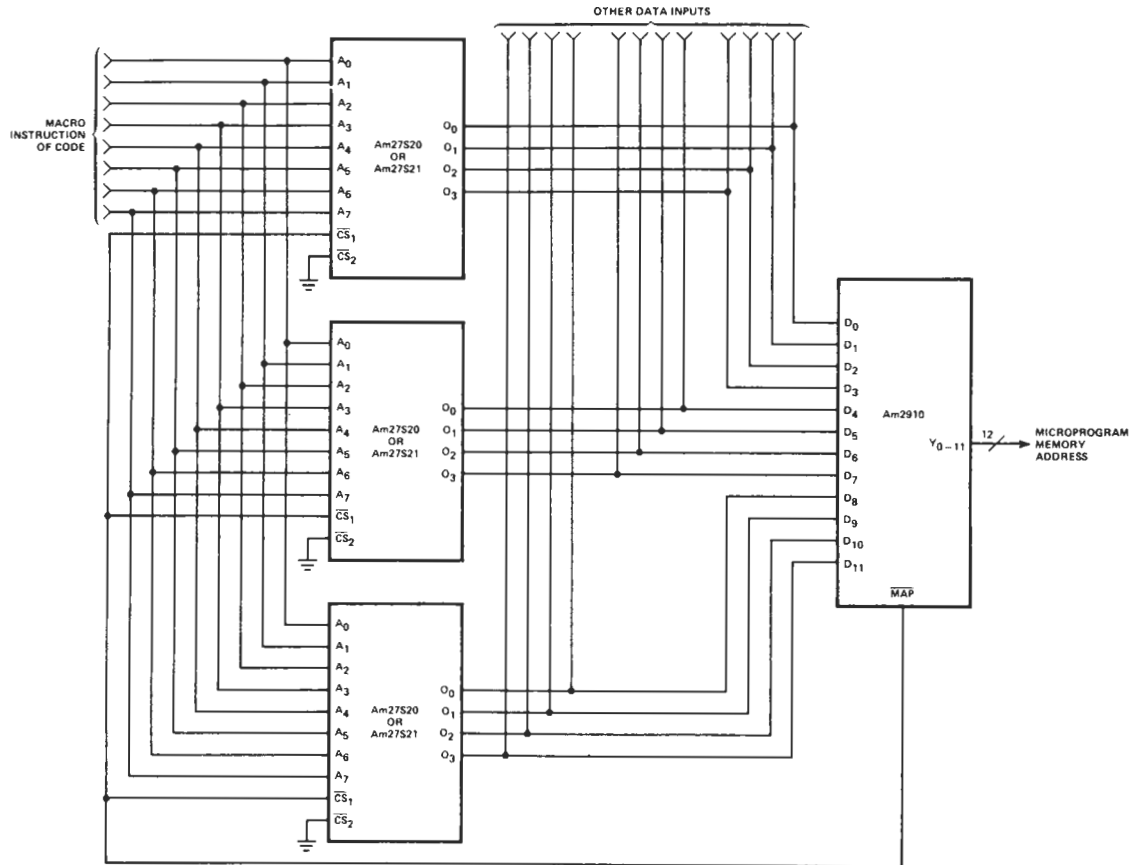


**Am27S20 • Am27S21**

**APPLYING THE Am27S20/21**

Typical application of the Am27S20/21 is shown below. The Am27S20/21's are employed as mapping ROMs in a micro-program computer control unit. The eight-bit macroinstruction from main memory is brought into the A<sub>0-7</sub> inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram

memory. The  $\overline{\text{MAP}}$  output of the Am2910 is connected to the  $\overline{\text{CS}}_1$  input of the Am27S20/21 such that when the  $\overline{\text{CS}}_1$  input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20 or in the three-state mode in the case of the Am27S21. In both cases the  $\overline{\text{CS}}_2$  input is grounded, thus data from other sources are free to drive the D inputs of the Am2910 when  $\overline{\text{MAP}}$  is HIGH.

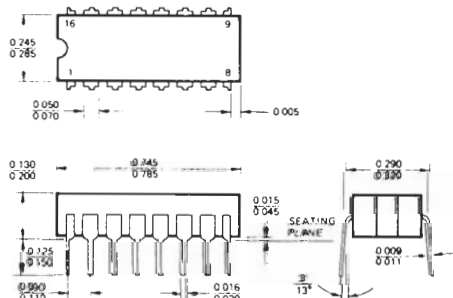


**MICROPROGRAMMING INSTRUCTION MAPPING**

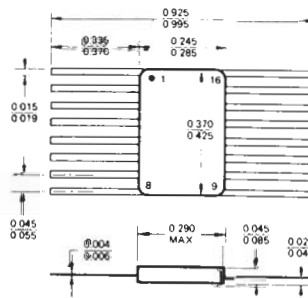
BPM-035

**PHYSICAL DIMENSIONS  
Dual-In-Line**

**16-Pin Ceramic**



**16-Pin Flat Package**



# Am27S18 • Am27S19

## 256-Bit Generic Series Bipolar PROM

### DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with  $N^2$  patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

### FUNCTIONAL DESCRIPTION

The Am27S18 and Am27S19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27S18 and three-state Am27S19 output versions. After programming, stored information is read on outputs  $O_0$ – $O_7$  by applying unique binary addresses to  $A_0$ – $A_4$  and holding the chip select input,  $\overline{CS}$ , at a logic LOW. If the chip select input goes to a logic HIGH,  $O_0$ – $O_7$  go to the off or high impedance state.

### GENERIC SERIES CHARACTERISTICS

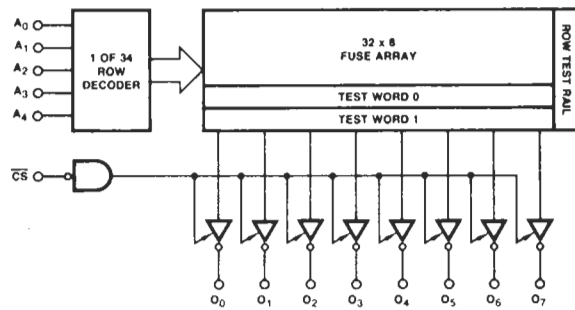
The Am27S18 and Am27S19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

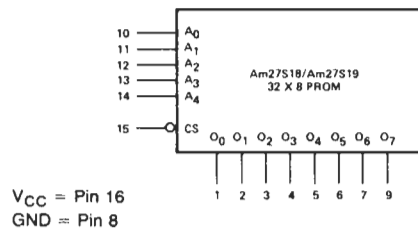
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

### BLOCK DIAGRAM



BPM-018

### LOGIC SYMBOL

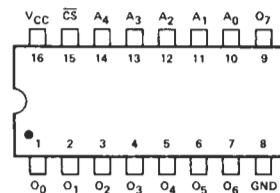


BPM-019

### ORDERING INFORMATION

| Package Type        | Temperature Range | Order Number |
|---------------------|-------------------|--------------|
| Open Collectors     |                   |              |
| Hermetic DIP        | 0°C to +75°C      | AM27S18DC    |
| Hermetic DIP        | -55°C to +125°C   | AM27S18DM    |
| Hermetic Flat Pak   | -55°C to +125°C   | AM27S18FM    |
| Three-State Outputs |                   |              |
| Hermetic DIP        | 0°C to +75°C      | AM27S19DC    |
| Hermetic DIP        | -55°C to +125°C   | AM27S19DM    |
| Hermetic Flat Pak   | -55°C to +125°C   | AM27S19FM    |

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

BPM-020



**Am27S18 • Am27S19****MAXIMUM RATINGS** (Above which the useful life may be impaired)

|  |                                |
|--|--------------------------------|
| Storage Temperature  | -65°C to +150°C                |
| Temperature (Ambient) Under Bias   | -55°C to +125°C                |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous          | -0.5V to +7.0V                 |
| DC Voltage Applied to Outputs (Except During Programming)                | -0.5V to +V <sub>CC</sub> max. |
| DC Voltage Applied to Outputs During Programming                         | 21V                            |
| Output Current into Outputs During Programming (Max. Duration of 1 sec.) | 200mA                          |
| DC Input Voltage   | -0.5V to +5.5V                 |
| DC Input Current   | -30mA to +5mA                  |

**OPERATING RANGE**

|       |                      |                                  |                             |
|-------|----------------------|----------------------------------|-----------------------------|
| COM'L | Am27S18XC, Am27S19XC | T <sub>A</sub> = 0°C to +75°C    | V <sub>CC</sub> = 5.0V ±5%  |
| MIL   | Am27S18XM, Am27S19XM | T <sub>A</sub> = -55°C to +125°C | V <sub>CC</sub> = 5.0V ±10% |

**ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE** (Unless Otherwise Noted)  
**PRELIMINARY DATA**

| Parameters                         | Description                  | Test Conditions  | Min. | Typ.<br>(Note 1) | Max.   | Units |
|------------------------------------|------------------------------|--|------|------------------|--------|-------|
| V <sub>OH</sub><br>(Am27LS19 only) | Output HIGH Voltage          | V <sub>CC</sub> = MIN., I <sub>OH</sub> = -2.0mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4  |                  |        | Volts |
| V <sub>OL</sub>                    | Output LOW Voltage           | V <sub>CC</sub> = MIN., I <sub>OL</sub> = 16mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |      |                  | 0.45   | Volts |
| V <sub>IH</sub>                    | Input HIGH Level             | Guaranteed input logical HIGH<br>voltage for all inputs  | 2.0  |                  |        | Volts |
| V <sub>IL</sub>                    | Input LOW Level              | Guaranteed input logical LOW<br>voltage for all inputs   |      |                  | 0.8    | Volts |
| I <sub>IL</sub>                    | Input LOW Current            | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.45V  |      | -0.010           | -0.250 | mA    |
| I <sub>IH</sub>                    | Input HIGH Current           | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.7V   |      |                  | 25     | μA    |
| I <sub>I</sub>                     | Input HIGH Current           | V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5V   |      |                  | 1.0    | mA    |
| I <sub>SC</sub><br>(Am27LS19 only) | Output Short Circuit Current | V <sub>CC</sub> = MAX., V <sub>OUT</sub> = 0.0V (Note 2)   | -20  | -40              | -90    | mA    |
| I <sub>CC</sub>                    | Power Supply Current         | All inputs = GND<br>V <sub>CC</sub> = MAX.   |      | 90               | 115    | mA    |
| V <sub>I</sub>                     | Input Clamp Voltage          | V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA  |      |                  | -1.2   | Volts |
| I <sub>CEX</sub>                   | Output Leakage Current       | V <sub>CC</sub> = MAX.<br>V <sub>CS</sub> = 2.4V<br>Am27LS19<br>only                                     |      |                  | 40     | μA    |
|                                    |                              |  |      |                  | 40     |       |
|                                    |                              |  |      |                  | -40    |       |
| C <sub>IN</sub>                    | Input Capacitance            | V <sub>IN</sub> = 2.0V @ f = 1 MHz (Note 3)  |      | 4                |        | pF    |
| C <sub>OUT</sub>                   | Output Capacitance           | V <sub>OUT</sub> = 2.0V @ f = 1 MHz (Note 3)   |      | 8                |        |       |

Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.

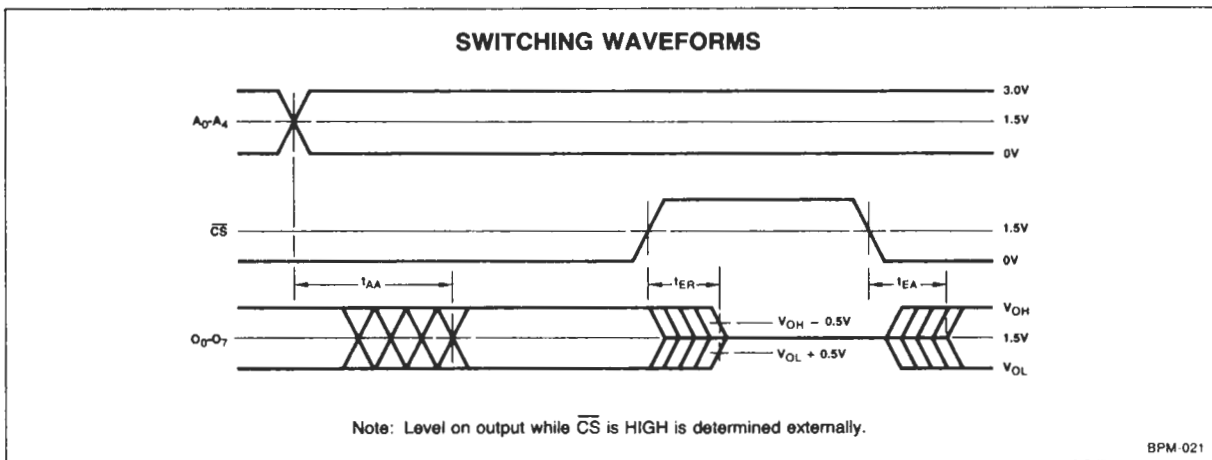
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but periodically sampled.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**  
**PRELIMINARY DATA**

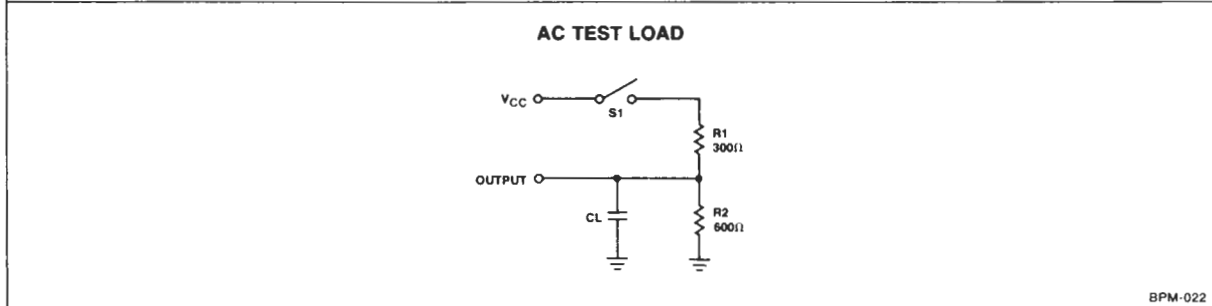
| Parameter | Description          | Test Conditions                 | Typ        | Max   |     | Units |
|-----------|----------------------|---------------------------------|------------|-------|-----|-------|
|           |                      |                                 | 5V<br>25°C | COM'L | MIL |       |
| $t_{AA}$  | Address Access Time  | AC Test Load<br>(See Notes 1-3) | 25         | 40    | 50  | ns    |
| $t_{EA}$  | Enable Access Time   |                                 | 15         | 25    | 30  | ns    |
| $t_{ER}$  | Enable Recovery Time |                                 | 15         | 25    | 30  | ns    |

- Notes: 1.  $t_{AA}$  is tested with switch  $S_1$  closed and  $C_L = 30pF$ .  
 2. For open collector outputs,  $t_{EA}$  and  $t_{ER}$  are tested with  $S_1$  closed to the 1.5V output level.  $C_L = 30pF$ .  
 3. For three state outputs,  $t_{EA}$  is tested with  $C_L = 30pF$  to the 1.5V level;  $S_1$  is open for high impedance to HIGH tests and closed for high impedance to LOW tests.  $t_{ER}$  is tested with  $C_L = 5pF$ . HIGH to high impedance tests are made with  $S_1$  open to an output voltage of  $V_{OH} - 0.5V$ ; LOW to high impedance tests are made with  $S_1$  closed to the  $V_{OL} + 0.5V$  level.



**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS                 | OUTPUTS                      | WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|------------------------|------------------------------|----------|----------------------------------|---|
|          | MUST BE STEADY         | WILL BE STEADY               |          | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN                   |
|          | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |          | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |
|          | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |          |                                  |   |



## Am27S18 • Am27S19

## PROGRAMMING

The Am27S18 and Am27S19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the  $\overline{CS}$  input is at a logic HIGH. Current is gated through the addressed fuse by raising the  $\overline{CS}$  input from a logic HIGH to 15 volts. After 50  $\mu\text{sec}$ , the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50  $\mu\text{sec}$ . Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which

the current drops to approximately 40mA. Current into the  $\overline{CS}$  pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including  $V_{CC}$  should be removed for a period of 5 seconds after which programming may be resumed.

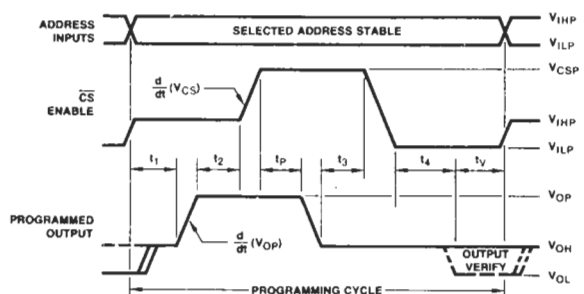
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING PARAMETERS

| Parameter      | Description                                | Min. | Max.            | Units             |
|----------------|--|------|-----------------|-------------------|
| $V_{CCP}$      | $V_{CC}$ During Programming                | 5.0  | 5.5             | Volts             |
| $V_{IHP}$      | Input HIGH Level During Programming        | 2.4  | 5.5             | Volts             |
| $V_{ILP}$      | Input LOW Level During Programming         | 0.0  | 0.45            | Volts             |
| $V_{CSP}$      | $\overline{CS}$ Voltage During Programming | 14.5 | 15.5            | Volts             |
| $V_{OP}$       | Output Voltage During Programming          | 19.5 | 20.5            | Volts             |
| $V_{ONP}$      | Voltage on Outputs Not to be Programmed    | 0    | $V_{CCP} + 0.3$ | Volts             |
| $I_{ONP}$      | Current into Outputs Not to be Programmed  |      | 20              | mA                |
| $d(V_{OP})/dt$ | Rate of Output Voltage Change              | 20   | 250             | $V/\mu\text{sec}$ |
| $d(V_{CS})/dt$ | Rate of $\overline{CS}$ Voltage Change     | 100  | 1000            | $V/\mu\text{sec}$ |
| $t_p$          | Programming Period - First Attempt         | 50   | 100             | $\mu\text{sec}$   |
|                | Programming Period - Subsequent Attempts   | 5.0  | 15              | msec              |

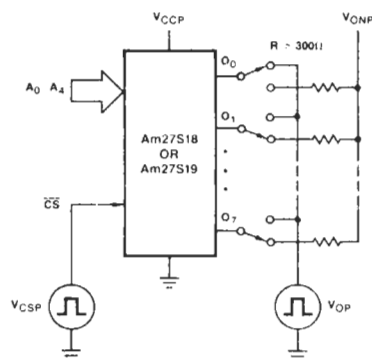
- Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.  
 2. Delays  $t_1$ ,  $t_2$ ,  $t_3$  and  $t_4$  must be greater than 100 ns; maximum delays of 1  $\mu\text{sec}$  are recommended to minimize heating during programming.  
 3. During  $t_v$ , a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.  
 4. Outputs not being programmed are connected to  $V_{ONP}$  through resistor R which provides output current limiting.

## PROGRAMMING WAVEFORMS



BPM-023

## SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

**PROGRAMMING EQUIPMENT**

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic

programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

|   |   |  |
|---|---|--|
| SOURCE AND LOCATION                         | Data I/O Corp.<br>P.O. Box 308<br>Issaquah, Wash. 98027 | Pro-Log Corp.<br>2411 Garden Road<br>Monterey, Ca. 93940 |
| PROGRAMMER MODEL(S)                         | Model 5, 7 and 9  | M900 and M920  |
| AMD GENERIC BIPOLAR PROM PERSONALITY BOARD  | 909-1286-1  | PM9058   |
| Am27S18 • Am27S19 ADAPTERS AND CONFIGURATOR | 715-1407-1  | PA16-6 and 32 x 8 (L)                                    |

**OBTAINING PROGRAMMED UNITS**

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

**ASCII BPNF**

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
  - a. Any characters, including carriage return and line feed, except "B".
  - b. The letter "B", indicating the beginning of the data word.
  - c. A sequence of eight Ps or Ns, starting with output O<sub>7</sub>.
  - d. The letter "F", indicating the finish of the data word.
  - e. Any text, including carriage return and line feed, except the letter "B".

3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.  
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

**TYPICAL PAPER TAPE FORMAT**

```

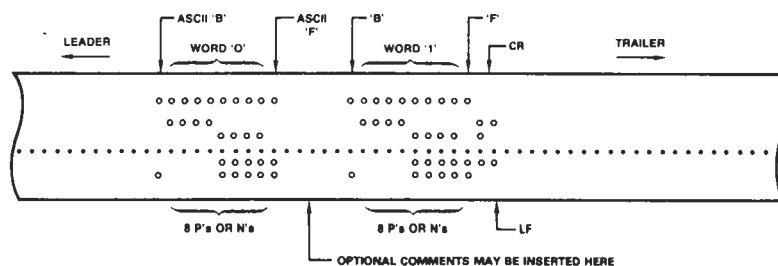
φφφ BPNPPNNPF WORD ZERO (R) (L)
      BPPPPPPNF COMMENT FIELD (R) (L)
φφ2 BNNPPPPNF ANY (R) (L)
      BNNNNNNNF TEXT (R) (L)
φφ4 BPNNNNNPF CAN (R) (L)
      BNPPPPNNF GO (R) (L)
φφ6 BPNPPPPNF HERE (R) (L)
      :
      :
φ31 BNNPPPPNF END (R) (L)
  
```

(R) = CARRIAGE RETURN  
(L) = LINE FEED

**RESULTING DEVICE TRUTH TABLE ( $\overline{CS}$  = LOW)**

| A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | O <sub>7</sub> | O <sub>6</sub> | O <sub>5</sub> | O <sub>4</sub> | O <sub>3</sub> | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| L              | L              | L              | L              | L              | H              | L              | H              | H              | L              | L              | L              | H              |
| L              | L              | L              | L              | H              | H              | H              | H              | H              | H              | H              | L              | L              |
| L              | L              | L              | H              | L              | L              | L              | L              | H              | H              | H              | H              | L              |
| L              | L              | L              | H              | H              | L              | L              | L              | L              | L              | L              | L              | L              |
| L              | L              | H              | L              | L              | H              | L              | L              | L              | L              | L              | L              | H              |
| L              | L              | H              | L              | H              | L              | H              | H              | L              | H              | H              | L              | L              |
| L              | L              | H              | H              | L              | H              | L              | L              | H              | H              | H              | L              | L              |
| :              | :              | :              | :              | :              | :              | :              | :              | :              | :              | :              | :              | :              |
| H              | H              | H              | H              | H              | L              | L              | L              | L              | H              | H              | H              | L              |

**ASCII PAPER TAPE**

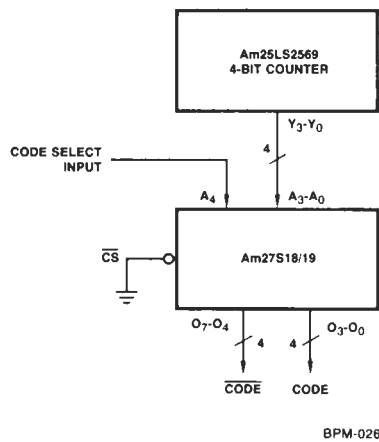


Am27S18 • Am27S19

APPLYING THE Am27S18 AND Am27S19

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking con-

trol or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.

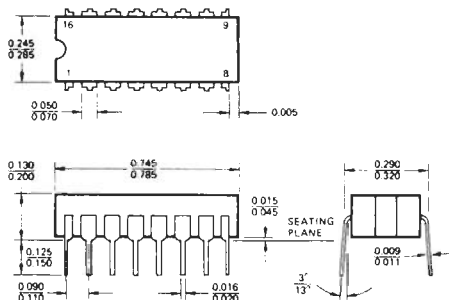


TRUTH TABLE

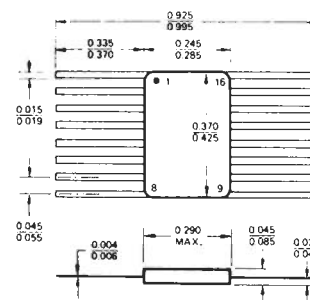
| ADDRESS        |                |                |                |                | COMPLEMENT     |                |                |                | TRUE           |                |                |                |   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | O <sub>7</sub> | O <sub>6</sub> | O <sub>5</sub> | O <sub>4</sub> | O <sub>3</sub> | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 0              | 0              | 0              | 1              | 1              | 0              | 0              | 0              | 0              | 1              | 1              | 1 | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 0              | 0              | 1              | 1              | 0              | 1              | 1              | 0              | 1              | 0              | 1              | 0 |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 0              | 1              | 0              | 1              | 0              | 1              | 0              | 0              | 1              | 0              | 1              | 1 |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 0              | 1              | 1              | 1              | 0              | 0              | 1              | 0              | 1              | 1              | 0              | 0 |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 1              | 0              | 0              | 1              | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 1 |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 1              | 0              | 1              | 0              | 1              | 1              | 1              | 1              | 1              | 0              | 0              | 0 |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 1              | 1              | 0              | 0              | 1              | 1              | 0              | 1              | 0              | 0              | 1              | 0 |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |                   |
| 0              | 0              | 1              | 1              | 1              | 0              | 1              | 0              | 1              | 0              | 1              | 0              | 1              | 0 |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |                   |
| 0              | 1              | 0              | 0              | 0              | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 1              | 1 |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |                   |
| 0              | 1              | 0              | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |                   |
| 0              | 1              | 0              | 1              | 0              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |                   |
| 0              | 1              | 0              | 1              | 1              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |                   |
| 0              | 1              | 1              | 0              | 0              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |                   |
| 0              | 1              | 1              | 0              | 1              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |                   |
| 0              | 1              | 1              | 1              | 0              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | EXCESS THREE CODE |
| 0              | 1              | 1              | 1              | 1              | X              | X              | X              | X              | X              | X              | X              | X              | X |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 1              | 1              | 0              | 0              | 0 | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | 0              | 0              | 0              | 1 |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 0              | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 0              | 1              | 1              | 1 |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 1              | 0              | 1              | 0              | 1              | 0 |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 1              | 0              | 0              | 1              | 0              | 0              | 0              | 1              | 0              | 1              | 1              | 0 |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 1 |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 1              | 1              | 0              | 1              | 0              | 1              | 1              | 0              | 1              | 0              | 0              | 1 |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 0              | 1              | 1              | 1              | 1              | 0              | 1              | 1              | 1              | 0              | 0              | 0              | 1 |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |
| 1              | 1              | 0              | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | 1 |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |                   |
| 1              | 1              | 0              | 0              | 1              | 0              | 0              | 1              | 0              | 1              | 1              | 0              | 1              | 0 |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |                   |
| 1              | 1              | 0              | 1              | 0              | 0              | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |                   |
| 1              | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 1              | 1              | 1              | 1              | 0              | 0 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |                   |
| 1              | 1              | 1              | 0              | 0              | 0              | 1              | 0              | 1              | 0              | 0              | 1              | 0              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |                   |
| 1              | 1              | 1              | 0              | 1              | 0              | 1              | 0              | 0              | 1              | 0              | 1              | 1              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |                   |
| 1              | 1              | 1              | 1              | 0              | 0              | 1              | 1              | 0              | 1              | 0              | 0              | 1              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   | GRAY CODE         |
| 1              | 1              | 1              | 1              | 1              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | 0              | 1 |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |
| 1              | 1              | 1              | 1              | 1              | 0              | 1              | 1              | 1              | 1              | 0              | 0              | 0              | 0 | GRAY CODE         |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |                   |

PHYSICAL DIMENSIONS  
Dual-In-Line

16-Pin Ceramic



16-Pin Flat Package





## 2764 (8K x 8) UV ERASABLE PROM

- 200 ns (2764-2) Maximum Access Time . . . HMOS\*-E Technology
- Compatible to High Speed 8MHz 8086-2 MPU . . . Zero WAIT State
- Two Line Control
- Pin Compatible to 2732A EPROM
- Industry Standard Pinout . . . JEDEC Approved
- Low Active Current...100mA Max.
- ±10% V<sub>CC</sub> Tolerance Available

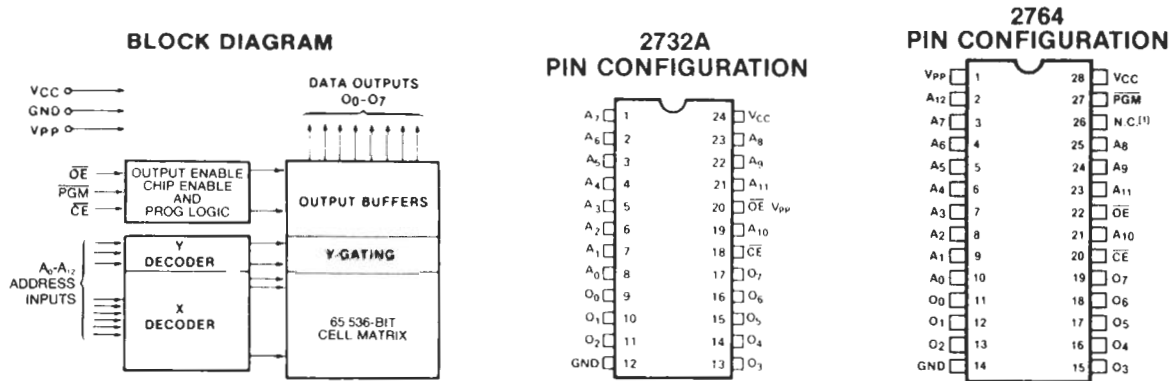
The Intel® 2764 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8MHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ( $\overline{OE}$ ) from the Chip Enable control ( $\overline{CE}$ ). The  $\overline{OE}$  control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the  $\overline{OE}$  and  $\overline{CE}$  controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA, while the standby current is only 40mA. The standby mode is achieved by applying a TTL-high signal to the  $\overline{CE}$  input.

±10% V<sub>CC</sub> tolerance is available as an alternative to the standard ±5% V<sub>CC</sub> tolerance for the 2764. This can allow the system designer more leeway in terms of his power supply requirements and other system parameters.

The 2764 is fabricated with HMOS\*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.



<sup>[1]</sup>For upgradability to JEDEC approved 128K EPROMs, provide an address line to pin 26. For compatibility with the 2732A and 32K ROMs, provide a trace from V<sub>CC</sub> to pin 26

### MODE SELECTION

| MODE            | PINS | $\overline{CE}$ (20) | $\overline{OE}$ (22) | PGM (27)        | V <sub>PP</sub> (1) | V <sub>CC</sub> (28) | Outputs (11-13, 15-19) |
|-----------------|------|----------------------|----------------------|-----------------|---------------------|----------------------|------------------------|
| Read            |      | V <sub>IL</sub>      | V <sub>IL</sub>      | V <sub>IN</sub> | V <sub>CC</sub>     | V <sub>CC</sub>      | D <sub>OUT</sub>       |
| Standby         |      | V <sub>IH</sub>      | x                    | x               | V <sub>CC</sub>     | V <sub>CC</sub>      | High Z                 |
| Program         |      | V <sub>IL</sub>      | x                    | V <sub>IL</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | D <sub>IN</sub>        |
| Program Verify  |      | V <sub>IL</sub>      | V <sub>IL</sub>      | V <sub>IN</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | D <sub>OUT</sub>       |
| Program Inhibit |      | V <sub>IH</sub>      | x                    | x               | V <sub>PP</sub>     | V <sub>CC</sub>      | High Z                 |

x can be either V<sub>IL</sub> or V<sub>IH</sub>

### PIN NAMES

|                                 |               |
|---------------------------------|---------------|
| A <sub>0</sub> -A <sub>12</sub> | ADDRESSES     |
| $\overline{CE}$                 | CHIP ENABLE   |
| $\overline{OE}$                 | OUTPUT ENABLE |
| O <sub>0</sub> -O <sub>7</sub>  | OUTPUTS       |
| PGM                             | PROGRAM       |
| N.C.                            | NO CONNECT    |

\*HMOS is a patented process of Intel Corporation.



2764

**ABSOLUTE MAXIMUM RATINGS\***

|  |                 |
|--|-----------------|
| Temperature Under Bias   | -10°C to +80°C  |
| Storage Temperature  | -65°C to +125°C |
| All Input or Output Voltages with Respect to Ground                      | +6V to -0.6V    |
| V <sub>PP</sub> Supply Voltage with Respect to Ground During Programming | +22V to -0.6V   |

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. AND A.C. OPERATING CONDITIONS DURING READ**

|   | 2764-2                            | 2764                              | 2764-3                            | 2764-4                            |
|---|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Operating Temperature Range                 | 0°C-70°C                          | 0°C-70°C                          | 0°C-70°C                          | 0°C-70°C                          |
| V <sub>CC</sub> Power Supply <sup>1,2</sup> | 5V ± 5%                           | 5V ± 5%                           | 5V ± 5%                           | 5V ± 5%                           |
| V <sub>PP</sub> Voltage <sup>2</sup>        | V <sub>PP</sub> = V <sub>CC</sub> | V <sub>PP</sub> = V <sub>CC</sub> | V <sub>PP</sub> = V <sub>CC</sub> | V <sub>PP</sub> = V <sub>CC</sub> |

|   | 2764-25                           | 2764-30                           | 2764-45                           |
|---|-----------------------------------|-----------------------------------|-----------------------------------|
| Operating Temperature Range                 | 0°C-70°C                          | 0°C-70°C                          | 0°C-70°C                          |
| V <sub>CC</sub> Power Supply <sup>1,2</sup> | 5V ± 10%                          | 5V ± 10%                          | 5V ± 10%                          |
| V <sub>PP</sub> Voltage <sup>2</sup>        | V <sub>PP</sub> = V <sub>CC</sub> | V <sub>PP</sub> = V <sub>CC</sub> | V <sub>PP</sub> = V <sub>CC</sub> |

**READ OPERATION****D.C. AND OPERATING CHARACTERISTICS**

| Symbol                        | Parameter                       | Limits |                  |                     | Unit | Conditions                               |
|-------------------------------|---------------------------------|--------|------------------|---------------------|------|--|
|                               |                                 | Min    | Typ <sup>3</sup> | Max                 |      |  |
| I <sub>LI</sub>               | Input Load Current              |        |                  | 10                  | μA   | V <sub>IN</sub> = 5.5V                   |
| I <sub>LO</sub>               | Output Leakage Current          |        |                  | 10                  | μA   | V <sub>OUT</sub> = 5.5V                  |
| I <sub>PP1</sub> <sup>2</sup> | V <sub>PP</sub> Current Read    |        |                  | 5                   | mA   | V <sub>PP</sub> = 5.5V                   |
| I <sub>CC1</sub> <sup>2</sup> | V <sub>CC</sub> Current Standby |        |                  | 40                  | mA   | $\overline{CE} = V_{IH}$                 |
| I <sub>CC2</sub> <sup>2</sup> | V <sub>CC</sub> Current Active  |        | 70               | 100                 | mA   | $\overline{CE} = \overline{OE} = V_{IL}$ |
| V <sub>IL</sub>               | Input Low Voltage               | -0.1   |                  | +0.8                | V    |  |
| V <sub>IH</sub>               | Input High Voltage              | 2.0    |                  | V <sub>CC</sub> + 1 | V    |  |
| V <sub>OL</sub>               | Output Low Voltage              |        |                  | .45                 | V    | I <sub>OL</sub> = 2.1 mA                 |
| V <sub>OH</sub>               | Output High Voltage             | 2.4    |                  |                     | V    | I <sub>OH</sub> = -400 μA                |

**A.C. CHARACTERISTICS**

| Symbol                       | Parameter   | 2764-2 Limits |     | 2764-25 & 2764 Limits |     | 2764-30 & 2764-3 Limits |     | 2764-45 & 2764-4 Limits |     | Unit | Test Conditions                          |
|------------------------------|---|---------------|-----|-----------------------|-----|-------------------------|-----|-------------------------|-----|------|--|
|                              |   | Min           | Max | Min                   | Max | Min                     | Max | Min                     | Max |      |  |
| t <sub>ACC</sub>             | Address to Output Delay   |               | 200 |                       | 250 |                         | 300 |                         | 450 | ns   | $\overline{CE} = \overline{OE} = V_{IL}$ |
| t <sub>CE</sub>              | $\overline{CE}$ to Output Delay   |               | 200 |                       | 250 |                         | 300 |                         | 450 | ns   | $\overline{OE} = V_{IL}$                 |
| t <sub>OE</sub>              | $\overline{OE}$ to Output Delay   |               | 75  |                       | 100 |                         | 120 |                         | 150 | ns   | $\overline{CE} = V_{IL}$                 |
| t <sub>DF</sub> <sup>4</sup> | $\overline{OE}$ High to Output Float  | 0             | 60  | 0                     | 85  | 0                       | 105 | 0                       | 130 | ns   | $\overline{CE} = V_{IL}$                 |
| t <sub>OH</sub>              | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First | 0             |     | 0                     |     | 0                       |     | 0                       |     | ns   | $\overline{CE} = \overline{OE} = V_{IL}$ |

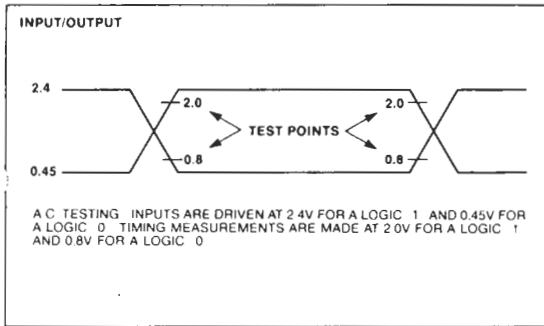
- NOTES:**
- V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.
  - V<sub>PP</sub> may be connected directly to V<sub>CC</sub> except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP1</sub>.
  - Typical values are for t<sub>a</sub> = 25°C and nominal supply voltages.
  - This parameter is only sampled and not 100% tested.



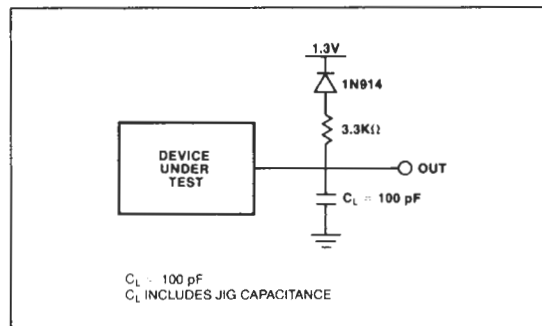
**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$

| Symbol     | Parameter          | Typ. <sup>1</sup> | Max. | Unit | Conditions            |
|------------|--------------------|-------------------|------|------|-----------------------|
| $C_{IN}^2$ | Input Capacitance  | 4                 | 6    | pF   | $V_{IN} = 0\text{V}$  |
| $C_{OUT}$  | Output Capacitance | 8                 | 12   | pF   | $V_{OUT} = 0\text{V}$ |

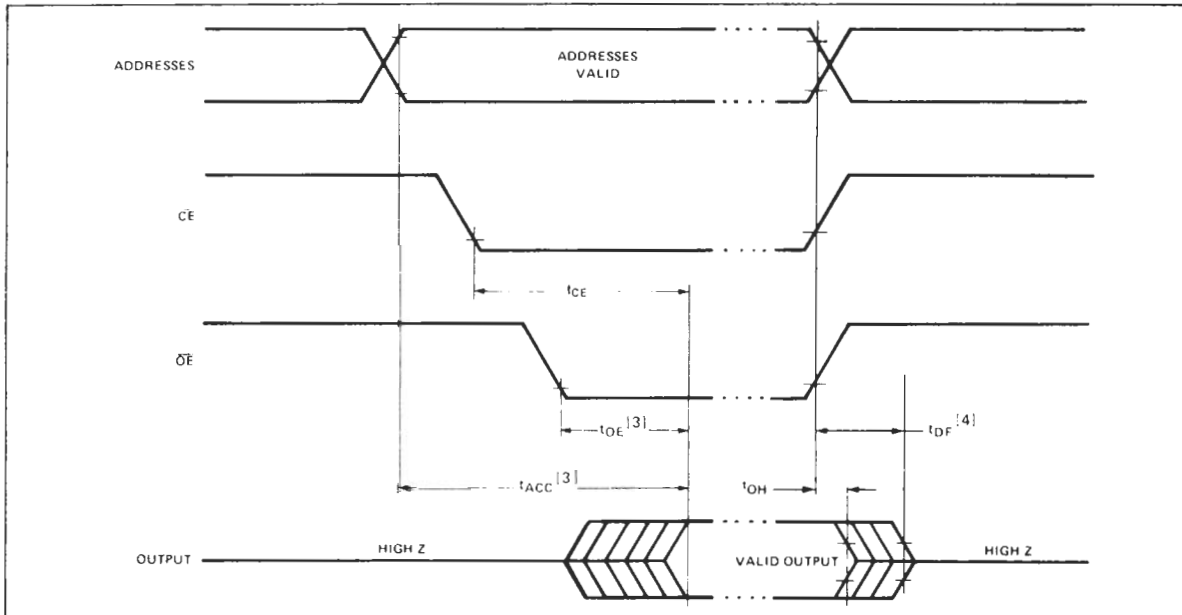
**A.C. TESTING INPUT, OUTPUT WAVEFORM**



**A.C. TESTING LOAD CIRCUIT**



**A.C. WAVEFORMS**



- NOTES:**
1. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages.
  2. This parameter is only sampled and is not 100% tested.
  3. OE may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .
  4.  $t_{DF}$  is specified from OE or CE, whichever occurs first.





2764

**PROGRAMMING****D.C. PROGRAMMING CHARACTERISTICS:**  $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = 21V \pm 0.5V$  (see Note 1)

| Symbol    | Parameter                         | Limits |      |              |               | Test Conditions                                  |
|-----------|-----------------------------------|--------|------|--------------|---------------|--|
|           |                                   | Min.   | Typ. | Max.         | Unit          |  |
| $I_{LI}$  | Input Current (All Inputs)        |        |      | 10           | $\mu\text{A}$ | $V_{IN} = V_{IL}$ or $V_{IH}$                    |
| $V_{OL}$  | Output Low Voltage During Verify  |        |      | 0.45         | V             | $I_{OL} = 2.1 \text{ mA}$                        |
| $V_{OH}$  | Output High Voltage During Verify | 2.4    |      |              | V             | $I_{OH} = -400 \mu\text{A}$                      |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Active)  |        |      | 100          | mA            |  |
| $V_{IL}$  | Input Low Level (All Inputs)      | -0.1   |      | 0.8          | V             |  |
| $V_{IH}$  | Input High Level                  | 2.0    |      | $V_{CC} + 1$ | V             |  |
| $I_{PP}$  | $V_{PP}$ Supply Current           |        |      | 30           | mA            | $\overline{CE} = V_{IL} = \overline{\text{PGM}}$ |

**A.C. PROGRAMMING CHARACTERISTICS:**  $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = 21V \pm 0.5V$  (see Note 1)

| Symbol    | Parameter                              | Limits |      |      |               | Test Conditions* |
|-----------|--|--------|------|------|---------------|------------------|
|           |  | Min.   | Typ. | Max. | Unit          |                  |
| $t_{AS}$  | Address Setup Time                     | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{OES}$ | $\overline{\text{OE}}$ Setup Time      | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{DS}$  | Data Setup Time                        | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{AH}$  | Address Hold Time                      | 0      |      |      | $\mu\text{S}$ |                  |
| $t_{DH}$  | Data Hold Time                         | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{DF}$  | Chip Enable to Output Float Delay      | 0      |      | 130  | ns            |                  |
| $t_{VS}$  | $V_{PP}$ Setup Time                    | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{PW}$  | PGM Pulse Width During Programming     | 45     | 50   | 55   | ms            |                  |
| $t_{CES}$ | $\overline{\text{CE}}$ Setup Time      | 2      |      |      | $\mu\text{S}$ |                  |
| $t_{OE}$  | Data Valid from $\overline{\text{OE}}$ |        |      | 150  | ns            |                  |

**\*A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20ns  
 Input Pulse Levels . . . . . 0.45V to 2.4V  
 Input Timing Reference Level . . . . . 1V and 2V  
 Output Timing Reference Level . . . . . 0.8V and 2.0V

**NOTE:**

1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .





## READ MODE

The 2764 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ( $t_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $t_{CE}$ ). Data is available at the outputs after a delay of  $t_{OE}$  from the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least  $t_{ACC}-t_{OE}$ .

## Standby Mode

The 2764 has a standby mode which reduces the active power current from 100mA to 40mA. The 2764 is placed in the standby mode by applying a TTL high signal to the  $\overline{CE}$  input. When in standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

## Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To use these two control lines most efficiently,  $\overline{CE}$  (pin 20) should be decoded and used as the primary device selecting function, while  $\overline{OE}$  (pin 22) should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

## System Consideration

The power switching characteristics of HMOS-E EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer — the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, as detailed in Intel's Application Note, AP-72, and/or by properly selected decoupling capacitors. It is recommended that a 0.1  $\mu$ F ceramic capacitor be used on every device between  $V_{CC}$  and GND. This should be a high

frequency capacitor of low inherent inductance. In addition, a 4.7  $\mu$ F bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board-traces.

## Programming

**Caution: Exceeding 22V on pin 1 ( $V_{PP}$ ) will damage the 2764.**

Initially, and after each erasure, all bits of the 2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2764 is in the programming mode when  $V_{PP}$  input is at 21V and  $\overline{CE}$  and  $\overline{PGM}$  are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming,  $\overline{CE}$  should be kept TTL low at all times while  $V_{PP}$  is kept at 21V. When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to  $\overline{PGM}$  input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

Programming of multiple 2764s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2764s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the  $\overline{PGM}$  input programs the paralleled 2764s.

## Program Inhibit

Programming of multiple 2764s in parallel with different data is also easily accomplished. A high level  $\overline{CE}$  or  $\overline{PGM}$  input inhibits the other 2764s from being programmed. Except for  $\overline{CE}$  (or  $\overline{PGM}$ ), all like inputs (including  $\overline{OE}$ ) of the parallel 2764s may be common. A TTL low level pulse applied to a 2764  $\overline{CE}$  and  $\overline{PGM}$  input with  $V_{PP}$  at 21V will program that 2764.

## Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\overline{CE}$  and  $\overline{OE}$  at  $V_{L}$ . However,  $\overline{PGM}$  is at  $V_{IH}$ .



## 8041A/8641A/8741A UNIVERSAL PERIPHERAL INTERFACE 8-BIT MICROCOMPUTER

- 8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package
- One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- DMA, Interrupt, or Polled Operation Supported
- 1024 x 8 ROM/EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins
- Fully Compatible with MCS-48™, MCS-80™, MCS-85™, and MCS-86™ Microprocessor Families
- Interchangeable ROM and EPROM Versions
- 3.6 MHz 8741A-8 Available
- Expandable I/O
- RAM Power-Down Capability
- Over 90 Instructions: 70% Single Byte
- Single 5V Supply

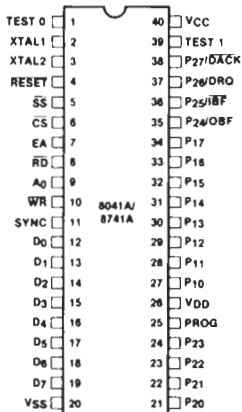
The Intel® 8041A/8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-48™, MCS-80™, MCS-85™, MCS-86™, and other 8-bit systems.

The UPI-41A™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041A version or as UV-erasable EPROM in the 8741A version. The 8741A and the 8041A are fully pin compatible for easy transition from prototype to production level designs. The 8641A is a one-time programmable (at the factory) 8741A which can be ordered as the first 25 pieces of a new 8041A order. The substitution of 8641A's for 8041A's allows for very fast turnaround for initial code verification and evaluation results.

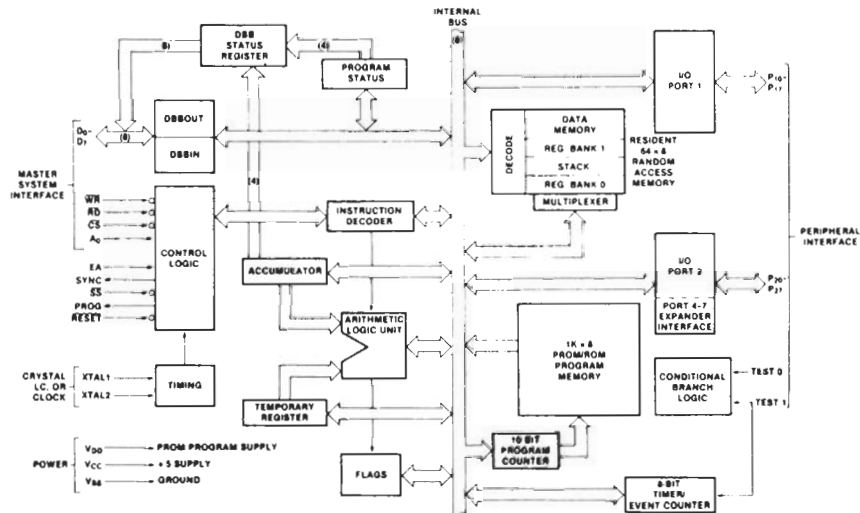
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041A), single-step mode for debug (in the 8741A), and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

### PIN CONFIGURATION



### BLOCK DIAGRAM





## 8041A/8641A/8741A

## PIN DESCRIPTION

| Signal                                  | Description  |
|---|--|
| D <sub>0</sub> –D <sub>7</sub><br>(BUS) | Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-41A to an 8-bit master system data bus.   |
| P <sub>10</sub> –P <sub>17</sub>        | 8-bit, PORT 1 quasi-bidirectional I/O lines.   |
| P <sub>20</sub> –P <sub>27</sub>        | 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P <sub>20</sub> –P <sub>23</sub> ) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P <sub>24</sub> –P <sub>27</sub> ) can be programmed to provide Interrupt Request and DMA Handshake capability. Software control can configure P <sub>24</sub> as OBF (Output Buffer Full), P <sub>25</sub> as IBF (Input Buffer Full), P <sub>26</sub> as DRQ (DMA Request), and P <sub>27</sub> as DACK (DMA Acknowledge). |
| $\overline{WR}$                         | I/O write input which enables the master CPU to write data and command words to the UPI-41A INPUT DATA BUS BUFFER.   |
| $\overline{RD}$                         | I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.  |
| $\overline{CS}$                         | Chip select input used to select one UPI-41A out of several connected to a common data bus.  |
| A <sub>0</sub>                          | Address input used by the master processor to indicate whether byte transfer is data or command.   |
| TEST 0,<br>TEST 1                       | Input pins which can be directly tested using conditional branch instructions.<br><br>T <sub>1</sub> also functions as the event timer input (under software control). T <sub>0</sub> is used during PROM programming and verification in the 8741A.   |
| XTAL1,<br>XTAL2                         | Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.  |
| SYNC                                    | Output signal which occurs once per UPI-41A instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.  |
| EA                                      | External access input which allows emulation, testing and PROM/ROM verification.   |
| PROG                                    | Multifunction pin used as the program pulse input during PROM programming.<br><br>During I/O expander access the PROG pin acts as an address/data strobe to the 8243.  |
| $\overline{RESET}$                      | Input used to reset status flip-flops and to set the program counter to zero.<br><br>$\overline{RESET}$ is also used during PROM programming and verification.   |
| $\overline{SS}$                         | Single step input used in the 8741A in conjunction with the SYNC output to step the program through each instruction.  |
| V <sub>CC</sub>                         | +5V main power supply pin.   |
| V <sub>DD</sub>                         | +5V during normal operation. +25V during programming operation. Low power standby pin in ROM version.  |
| V <sub>SS</sub>                         | Circuit ground potential.  |

## UPI™ INSTRUCTION SET

| Mnemonic             | Description  | Bytes | Cycles |
|----------------------|--|-------|--------|
| <b>ACCUMULATOR</b>   |  |       |        |
| ADD A,Rr             | Add register to A                                    | 1     | 1      |
| ADD A,@Rr            | Add data memory to A                                 | 1     | 1      |
| ADD A,#data          | Add immediate to A                                   | 2     | 2      |
| ADDC A,Rr            | Add register to A with carry                         | 1     | 1      |
| ADDC A,@Rr           | Add data memory to A with carry                      | 1     | 1      |
| ADDC A,#data         | Add immed. to A with carry                           | 2     | 2      |
| ANL A,Rr             | AND register to A                                    | 1     | 1      |
| ANL A,@Rr            | AND data memory to A                                 | 1     | 1      |
| ANL A,#data          | AND immediate to A                                   | 2     | 2      |
| ORL A,Rr             | OR register to A                                     | 1     | 1      |
| ORL A,@Rr            | OR data memory to A                                  | 1     | 1      |
| ORL A,#data          | OR immediate to A                                    | 2     | 2      |
| XRL A,Rr             | Exclusive OR register to A                           | 1     | 1      |
| XRL A,@Rr            | Exclusive OR data memory to A                        | 1     | 1      |
| XRL A,#data          | Exclusive OR immediate to A                          | 2     | 2      |
| INC A                | Increment A  | 1     | 1      |
| DEC A                | Decrement A  | 1     | 1      |
| CLR A                | Clear A  | 1     | 1      |
| CPL A                | Complement A   | 1     | 1      |
| DA A                 | Decimal Adjust A                                     | 1     | 1      |
| SWAP A               | Swap nibbles of A                                    | 1     | 1      |
| RL A                 | Rotate A left  | 1     | 1      |
| RLC A                | Rotate A left through carry                          | 1     | 1      |
| RR A                 | Rotate A right                                       | 1     | 1      |
| RRC A                | Rotate A right through carry                         | 1     | 1      |
| <b>INPUT/OUTPUT</b>  |  |       |        |
| IN A,Pp              | Input port to A                                      | 1     | 2      |
| OUTL Pp,A            | Output A to port                                     | 1     | 2      |
| ANL Pp,#data         | AND immediate to port                                | 2     | 2      |
| ORL Pp,#data         | OR immediate to port                                 | 2     | 2      |
| IN A,DBB             | Input DBB to A, clear IBF                            | 1     | 1      |
| OUT DBB,A            | Output A to DBB, set OBF                             | 1     | 1      |
| MOV STS,A            | A <sub>4</sub> –A <sub>7</sub> to Bits 4–7 of Status | 1     | 1      |
| MOVD A,Pp            | Input Expander port to A                             | 1     | 2      |
| MOVD Pp,A            | Output A to Expander port                            | 1     | 2      |
| ANLD Pp,A            | AND A to Expander port                               | 1     | 2      |
| ORLD Pp,A            | OR A to Expander port                                | 1     | 2      |
| <b>DATA MOVES</b>    |  |       |        |
| MOV A,Rr             | Move register to A                                   | 1     | 1      |
| MOV A,@Rr            | Move data memory to A                                | 1     | 1      |
| MOV A,#data          | Move immediate to A                                  | 2     | 2      |
| MOV Rr,A             | Move A to register                                   | 1     | 1      |
| MOV @Rr,A            | Move A to data memory                                | 1     | 1      |
| MOV Rr,#data         | Move immediate to register                           | 2     | 2      |
| MOV @Rr,#data        | Move immediate to data memory                        | 2     | 2      |
| MOV A,PSW            | Move PSW to A  | 1     | 1      |
| MOV PSW,A            | Move A to PSW  | 1     | 1      |
| XCH A,Rr             | Exchange A and register                              | 1     | 1      |
| XCH A,@Rr            | Exchange A and data memory                           | 1     | 1      |
| XCHD A,@Rr           | Exchange digit of A and register                     | 1     | 1      |
| MOVP A,@A            | Move to A from current page                          | 1     | 2      |
| MOVP3 A,@A           | Move to A from page 3                                | 1     | 2      |
| <b>TIMER/COUNTER</b> |  |       |        |
| MOV A,T              | Read Timer/Counter                                   | 1     | 1      |
| MOV T,A              | Load Timer/Counter                                   | 1     | 1      |
| STRT T               | Start Timer  | 1     | 1      |
| STRT CNT             | Start Counter  | 1     | 1      |
| STOP TCNT            | Stop Timer/Counter                                   | 1     | 1      |
| EN TCNTI             | Enable Timer/Counter Interrupt                       | 1     | 1      |
| DIS TCNTI            | Disable Timer/Counter Interrupt                      | 1     | 1      |

### 8041A/8641A/8741A

| Mnemonic          | Description                | Bytes | Cycles | Mnemonic      | Description                        | Bytes | Cycles |
|-------------------|----------------------------|-------|--------|---------------|------------------------------------|-------|--------|
| <b>CONTROL</b>    |                            |       |        | <b>BRANCH</b> |                                    |       |        |
| EN DMA            | Enable DMA Handshake Lines | 1     | 1      | CPL F0        | Complement Flag 0                  | 1     | 1      |
| EN I              | Enable IBF Interrupt       | 1     | 1      | CLR F1        | Clear F1 Flag                      | 1     | 1      |
| DIS I             | Disable IBF Interrupt      | 1     | 1      | CPL F1        | Complement F1 Flag                 | 1     | 1      |
| EN FLAGS          | Enable Master Interrupts   | 1     | 1      | <b>BRANCH</b> |                                    |       |        |
| SEL RB0           | Select register bank 0     | 1     | 1      | JMP addr      | Jump unconditional                 | 2     | 2      |
| SEL RB1           | Select register bank 1     | 1     | 1      | JMPP @A       | Jump indirect                      | 1     | 2      |
| NOP               | No Operation               | 1     | 1      | DJNZ Rr, addr | Decrement register and jump        | 2     | 2      |
| <b>REGISTERS</b>  |                            |       |        | JC addr       | Jump on Carry = 1                  | 2     | 2      |
| INC Rr            | Increment register         | 1     | 1      | JNC addr      | Jump on Carry = 0                  | 2     | 2      |
| INC @Rr           | Increment data memory      | 1     | 1      | JZ addr       | Jump on A Zero                     | 2     | 2      |
| DEC Rr            | Decrement register         | 1     | 1      | JNZ addr      | Jump on A not Zero                 | 2     | 2      |
| <b>SUBROUTINE</b> |                            |       |        | JT0 addr      | Jump on T0 = 1                     | 2     | 2      |
| CALL addr         | Jump to subroutine         | 2     | 2      | JNT0 addr     | Jump on T0 = 0                     | 2     | 2      |
| RET               | Return                     | 1     | 2      | JT1 addr      | Jump on T1 = 1                     | 2     | 2      |
| RETR              | Return and restore status  | 1     | 2      | JNT1 addr     | Jump on T1 = 0                     | 2     | 2      |
| <b>FLAGS</b>      |                            |       |        | JF0 addr      | Jump on F0 Flag = 1                | 2     | 2      |
| CLR C             | Clear Carry                | 1     | 1      | JF1 addr      | Jump on F1 Flag = 1                | 2     | 2      |
| CPL C             | Complement Carry           | 1     | 1      | JTF addr      | Jump on Timer Flag = 1, Clear Flag | 2     | 2      |
| CLR F0            | Clear Flag 0               | 1     | 1      | JNIBF addr    | Jump on IBF Flag = 0               | 2     | 2      |
|                   |                            |       |        | JOBf addr     | Jump on OBF Flag = 1               | 2     | 2      |
|                   |                            |       |        | JBb addr      | Jump on Accumulator Bit            | 2     | 2      |

### APPLICATIONS

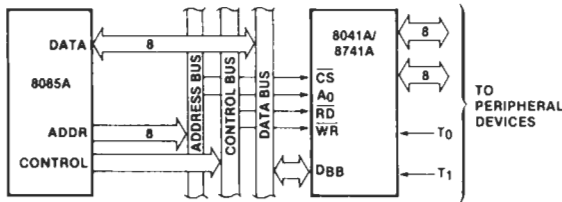


Figure 1. 8085A-8041A Interface

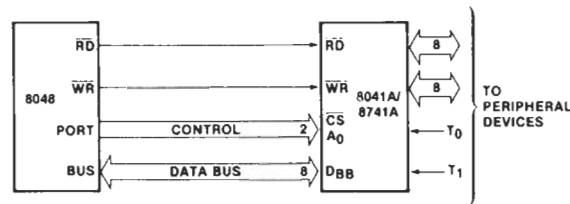


Figure 2. 8048-8041A Interface

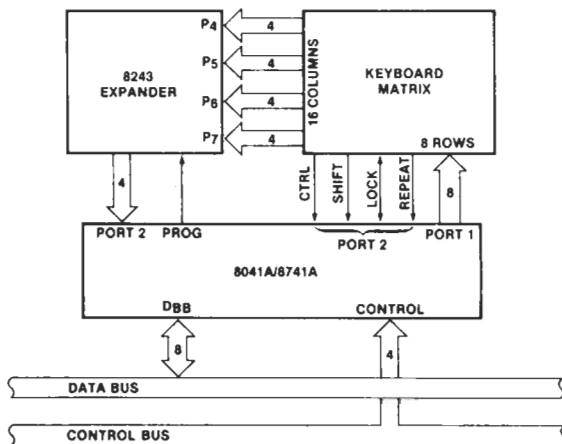


Figure 3. 8041A-8243 Keyboard Scanner

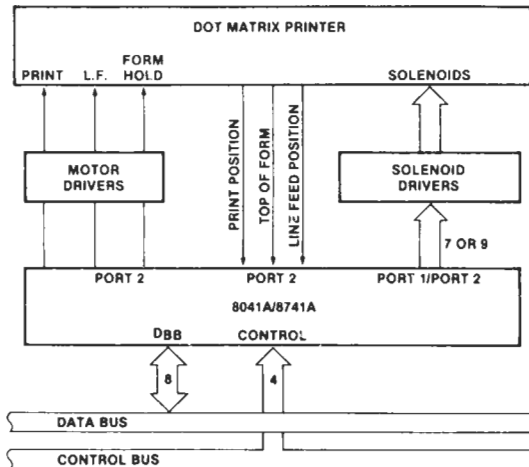


Figure 4. 8041A Matrix Printer Interface

**8041A/8641A/8741A**

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias . . . . . 0°C to 70°C  
 Storage Temperature . . . . . - 65°C to + 150°C  
 Voltage on Any Pin With Respect  
     to Ground . . . . . 0.5V to + 7V  
 Power Dissipation . . . . . 1.5 Watt

\**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. AND OPERATING CHARACTERISTICS**

T<sub>A</sub> = 0°C to 70°C, V<sub>SS</sub> = 0V, 8041A: V<sub>CC</sub> = V<sub>DD</sub> = +5V ± 10%, 8741A: V<sub>CC</sub> = V<sub>DD</sub> = +5V ± 5%

| Symbol                            | Parameter   | Min.  | Max.            | Unit | Test Conditions  |
|-----------------------------------|---|-------|-----------------|------|--|
| V <sub>IL</sub>                   | Input Low Voltage (Except XTAL1, XTAL2, RESET)  | - 0.5 | 0.8             | V    |  |
| V <sub>IL1</sub>                  | Input Low Voltage (XTAL1, XTAL2, RESET)   | - 0.5 | 0.6             | V    |  |
| V <sub>IH</sub>                   | Input High Voltage (Except XTAL1, XTAL2, RESET)   | 2.2   | V <sub>CC</sub> |      |  |
| V <sub>IH1</sub>                  | Input High Voltage (XTAL1, XTAL2, RESET)  | 3.8   | V <sub>CC</sub> | V    |  |
| V <sub>OL</sub>                   | Output Low Voltage (D <sub>0</sub> -D <sub>7</sub> )  |       | 0.45            | V    | I <sub>OL</sub> = 2.0 mA                                   |
| V <sub>OL1</sub>                  | Output Low Voltage (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> , Sync) |       | 0.45            | V    | I <sub>OL</sub> = 1.6 mA                                   |
| V <sub>OL2</sub>                  | Output Low Voltage (Prog)   |       | 0.45            | V    | I <sub>OL</sub> = 1.0 mA                                   |
| V <sub>OH</sub>                   | Output High Voltage (D <sub>0</sub> -D <sub>7</sub> )   | 2.4   |                 | V    | I <sub>OH</sub> = - 400 μA                                 |
| V <sub>OH1</sub>                  | Output High Voltage (All Other Outputs)   | 2.4   |                 | V    | I <sub>OH</sub> = - 50 μA                                  |
| I <sub>IL</sub>                   | Input Leakage Current (T <sub>0</sub> , T <sub>1</sub> , RD, WR, CS, A <sub>0</sub> , EA)     |       | ± 10            | μA   | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>        |
| I <sub>OZ</sub>                   | Output Leakage Current (D <sub>0</sub> -D <sub>7</sub> , High Z State)                        |       | ± 10            | μA   | V <sub>SS</sub> + 0.45 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> |
| I <sub>LI</sub>                   | Low Input Load Current (P <sub>10</sub> P <sub>17</sub> , P <sub>20</sub> P <sub>27</sub> )   |       | 0.5             | mA   | V <sub>IL</sub> = 0.8V                                     |
| I <sub>LI1</sub>                  | Low Input Load Current (RESET, SS)  |       | 0.2             | mA   | V <sub>IL</sub> = 0.8V                                     |
| I <sub>DD</sub>                   | V <sub>DD</sub> Supply Current  |       | 15              | mA   | Typical = 5 mA   |
| I <sub>CC</sub> + I <sub>DD</sub> | Total Supply Current  |       | 125             | mA   | Typical = 60 mA  |

**A.C. CHARACTERISTICS**

T<sub>A</sub> = 0°C to 70°C, V<sub>SS</sub> = 0V, 8041A: V<sub>CC</sub> = V<sub>DD</sub> = + 5V ± 10%, 8741A: V<sub>CC</sub> = V<sub>DD</sub> = + 5V ± 5%

**DBB READ**

| Symbol          | Parameter                            | Min. | Max. | Unit | Test Conditions         |
|-----------------|--------------------------------------|------|------|------|-------------------------|
| t <sub>AR</sub> | CS, A <sub>0</sub> Setup to RD!      | 0    |      | ns   |                         |
| t <sub>RA</sub> | CS, A <sub>0</sub> Hold After RD!    | 0    |      | ns   |                         |
| t <sub>RR</sub> | RD Pulse Width                       | 250  |      | ns   |                         |
| t <sub>AD</sub> | CS, A <sub>0</sub> to Data Out Delay |      | 225  | ns   | C <sub>L</sub> = 150 pF |
| t <sub>RD</sub> | RD! to Data Out Delay                |      | 225  | ns   | C <sub>L</sub> = 150 pF |
| t <sub>DF</sub> | RD! to Data Float Delay              |      | 100  | ns   |                         |
| t <sub>CY</sub> | Cycle Time (Except 8741A-8)          | 2.5  | 15   | μs   | 6.0 MHz XTAL            |
| t <sub>CY</sub> | Cycle Time (8741A-8)                 | 4.17 | 15   | μs   | 3.6 MHz XTAL            |

**DBB WRITE**

| Symbol          | Parameter                         | Min. | Max. | Unit | Test Conditions |
|-----------------|-----------------------------------|------|------|------|-----------------|
| t <sub>AW</sub> | CS, A <sub>0</sub> Setup to WR!   | 0    |      | ns   |                 |
| t <sub>WA</sub> | CS, A <sub>0</sub> Hold After WR! | 0    |      | ns   |                 |
| t <sub>WW</sub> | WR Pulse Width                    | 250  |      | ns   |                 |
| t <sub>DW</sub> | Data Setup to WR!                 | 150  |      | ns   |                 |
| t <sub>WD</sub> | Data Hold After WR!               | 0    |      | ns   |                 |



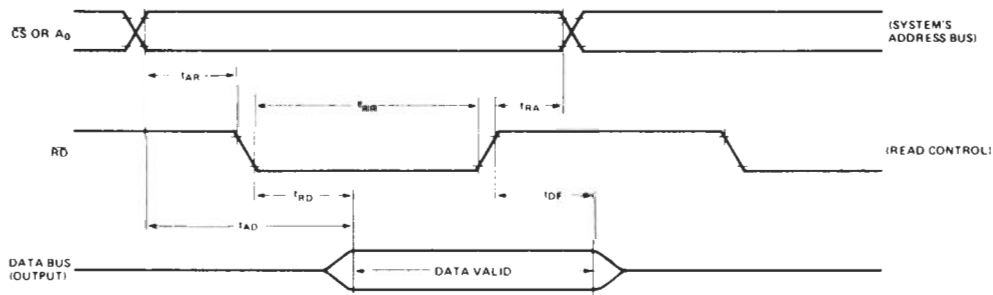
8041A/8641A/8741A

INPUT AND OUTPUT WAVEFORMS FOR A.C. TESTS

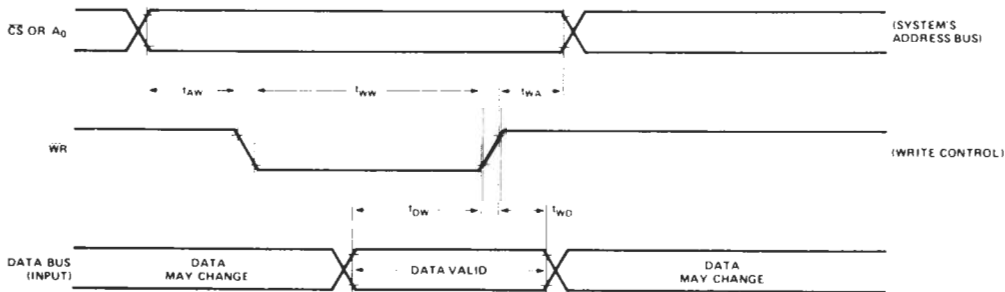


WAVEFORMS

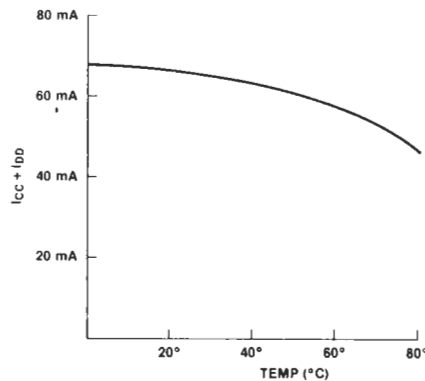
1. READ OPERATION—DATA BUS BUFFER REGISTER.



2. WRITE OPERATION—DATA BUS BUFFER REGISTER.



TYPICAL 8041/8741A CURRENT



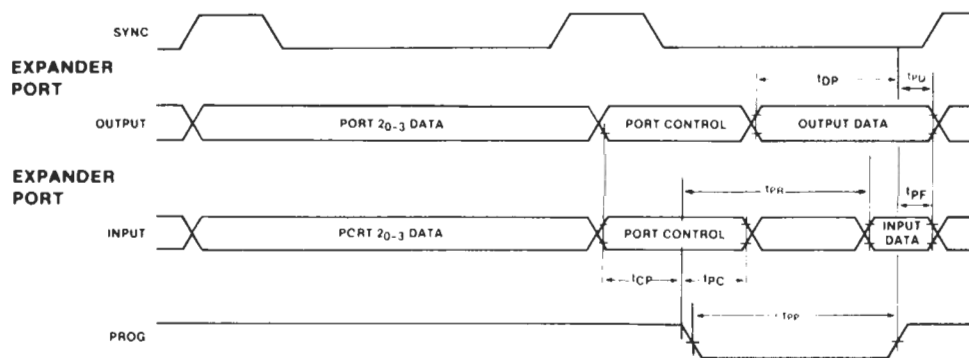
8041A/8641A/8741A

A.C. CHARACTERISTICS—PORT 2

T<sub>A</sub> = 0°C to 70°C, 8041A: V<sub>CC</sub> = +5V ± 10%, 8741A: V<sub>CC</sub> = +5V ± 5%

| Symbol          | Parameter                                      | Min. | Max. | Unit | Test Conditions |
|-----------------|--|------|------|------|-----------------|
| t <sub>CP</sub> | Port Control Setup Before Falling Edge of PROG | 110  |      | ns   |                 |
| t <sub>PC</sub> | Port Control Hold After Falling Edge of PROG   | 100  |      | ns   |                 |
| t <sub>PR</sub> | PROG to Time P2 Input Must Be Valid            |      | 810  | ns   |                 |
| t <sub>PF</sub> | Input Data Hold Time                           | 0    | 150  | ns   |                 |
| t <sub>DP</sub> | Output Data Setup Time                         | 250  |      | ns   |                 |
| t <sub>PD</sub> | Output Data Hold Time                          | 65   |      | ns   |                 |
| t <sub>PP</sub> | PROG Pulse Width                               | 1200 |      | ns   |                 |

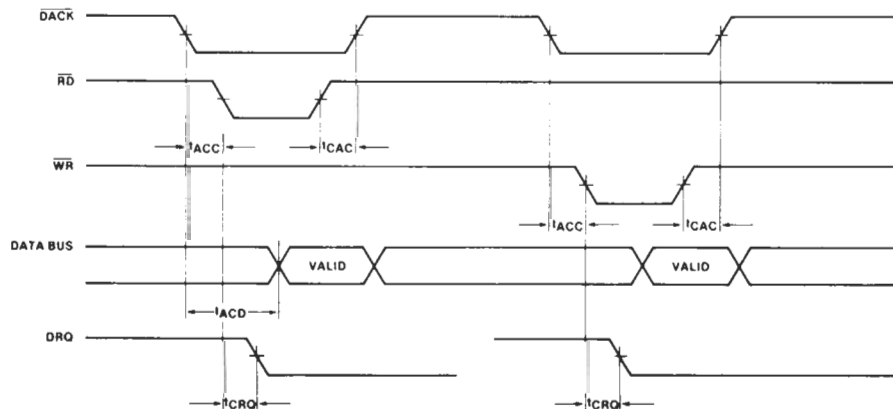
PORT 2 TIMING



A.C. CHARACTERISTICS—DMA

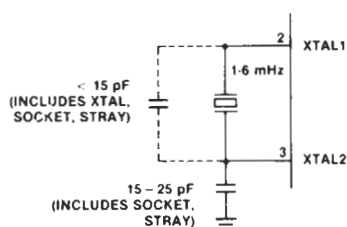
| Symbol           | Parameter   | Min. | Max. | Unit | Test Conditions         |
|------------------|---|------|------|------|-------------------------|
| t <sub>ACC</sub> | DACK to $\overline{WR}$ or $\overline{RD}$              | 0    |      | ns   |                         |
| t <sub>CAC</sub> | $\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$ | 0    |      | ns   |                         |
| t <sub>ACD</sub> | $\overline{DACK}$ to Data Valid                         |      | 225  | ns   | C <sub>L</sub> = 150 pF |
| t <sub>CRQ</sub> | $\overline{RD}$ or $\overline{WR}$ to DRQ Cleared       |      | 200  | ns   |                         |

WAVEFORMS—DMA



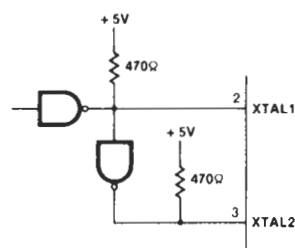
## 8041A/8641A/8741A

## CRYSTAL OSCILLATOR MODE



CRYSTAL SERIES RESISTANCE SHOULD BE  $< 75 \Omega$  AT 6 MHz;  $< 180 \Omega$  AT 3.6 MHz.

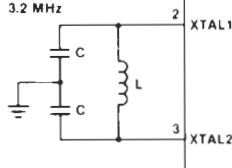
## DRIVING FROM EXTERNAL SOURCE



BOTH XTAL1 AND XTAL2 SHOULD BE DRIVEN. RESISTORS TO  $V_{CC}$  ARE NEEDED TO ENSURE  $V_{IH} = 3.8V$  IF TTL CIRCUITRY IS USED.

## LC OSCILLATOR MODE

| L                 | C     | NOMINAL f |
|-------------------|-------|-----------|
| 45 $\mu\text{H}$  | 20 pF | 5.2 MHz   |
| 120 $\mu\text{H}$ | 20 pF | 3.2 MHz   |



$$f = \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = C + 3C_{pp}$$

$C_{pp} = 5 - 10 \text{ pF}$  PIN-TO-PIN CAPACITANCE

EACH C SHOULD BE APPROXIMATELY 20 pF, INCLUDING STRAY CAPACITANCE.

## PROGRAMMING, VERIFYING, AND ERASING THE 8741A EPROM

## Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

| Pin                       | Function  |
|---------------------------|---|
| XTAL 1                    | Clock Input (1 to 6MHz)                             |
| $\overline{\text{Reset}}$ | Initialization and Address Latching                 |
| Test 0                    | Selection of Program or Verify Mode                 |
| EA                        | Activation of Program/Verify Modes                  |
| BUS                       | Address and Data Input<br>Data Output During Verify |
| P20-1                     | Address Input                                       |
| $V_{DD}$                  | Programming Power Supply                            |
| PROG                      | Program Pulse Input                                 |

## WARNING:

An attempt to program a missocketed 8741A will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1.  $A_0 = 0V$ ,  $\overline{\text{CS}} = 5V$ ,  $EA = 5V$ ,  $\overline{\text{RESET}} = 0V$ ,  $\text{TEST0} = 5V$ ,  $V_{DD} = 5V$ , clock applied or internal oscillator operating, BUS and PROG floating.
2. Insert 8741A in programming socket
3.  $\text{TEST0} = 0V$  (select program mode)
4.  $EA = 23V$  (activate program mode)
5. Address applied to BUS and P20-1
6.  $\overline{\text{RESET}} = 5V$  (latch address)
7. Data applied to BUS
8.  $V_{DD} = 25V$  (programming power)
9.  $\text{PROG} = 0V$  followed by one 50ms pulse to 23V
10.  $V_{DD} = 5V$
11.  $\text{TEST0} = 5V$  (verify mode)
12. Read and verify data on BUS
13.  $\text{TEST0} = 0V$
14.  $\overline{\text{RESET}} = 0V$  and repeat from step 5
15. Programmer should be at conditions of step 1 when 8741A is removed from socket.

## 8041A/8641A/8741A

**8741A Erasure Characteristics**

The erasure characteristics of the 8741A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8741A in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which

should be placed over the 8741A window to prevent unintentional erasure.

The recommended erasure procedure for the 8741A is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 w-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm<sup>2</sup> power rating. The 8741A should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

**A.C. TIMING SPECIFICATION FOR PROGRAMMING**

$$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}, V_{CC} = 5\text{V} \pm 5\%, V_{DD} = 25\text{V} \pm 1\text{V}$$

| Symbol             | Parameter  | Min. | Max. | Unit | Test Conditions |
|--------------------|--|------|------|------|-----------------|
| t <sub>AW</sub>    | Address Setup Time to $\overline{\text{RESET}}$ ↑      | 4tcy |      |      |                 |
| t <sub>WA</sub>    | Address Hold Time After $\overline{\text{RESET}}$ ↓    | 4tcy |      |      |                 |
| t <sub>DW</sub>    | Data in Setup Time to PROG ↑                           | 4tcy |      |      |                 |
| t <sub>WD</sub>    | Data in Hold Time After PROG ↓                         | 4tcy |      |      |                 |
| t <sub>PH</sub>    | $\overline{\text{RESET}}$ Hold Time to Verify          | 4tcy |      |      |                 |
| t <sub>VDDW</sub>  | V <sub>DD</sub> Setup Time to PROG ↑                   | 4tcy |      |      |                 |
| t <sub>VDDH</sub>  | V <sub>DD</sub> Hold Time After PROG ↓                 | 0    |      |      |                 |
| t <sub>PW</sub>    | Program Pulse Width                                    | 50   | 60   | mS   |                 |
| t <sub>rw</sub>    | Test 0 Setup Time for Program Mode                     | 4tcy |      |      |                 |
| t <sub>WT</sub>    | Test 0 Hold Time After Program Mode                    | 4tcy |      |      |                 |
| t <sub>DO</sub>    | Test 0 to Data Out Delay                               |      | 4tcy |      |                 |
| t <sub>ww</sub>    | $\overline{\text{RESET}}$ Pulse Width to Latch Address | 4tcy |      |      |                 |
| t <sub>r, tf</sub> | V <sub>DD</sub> and PROG Rise and Fall Times           | 0.5  | 2.0  | μS   |                 |
| t <sub>CY</sub>    | CPU Operation Cycle Time                               | 5.0  |      | μS   |                 |
| t <sub>RE</sub>    | $\overline{\text{RESET}}$ Setup Time Before EA ↑.      | 4tcy |      |      |                 |

Note: If TEST 0 is high, t<sub>DO</sub> can be triggered by  $\overline{\text{RESET}}$  ↓.

**D.C. SPECIFICATION FOR PROGRAMMING**

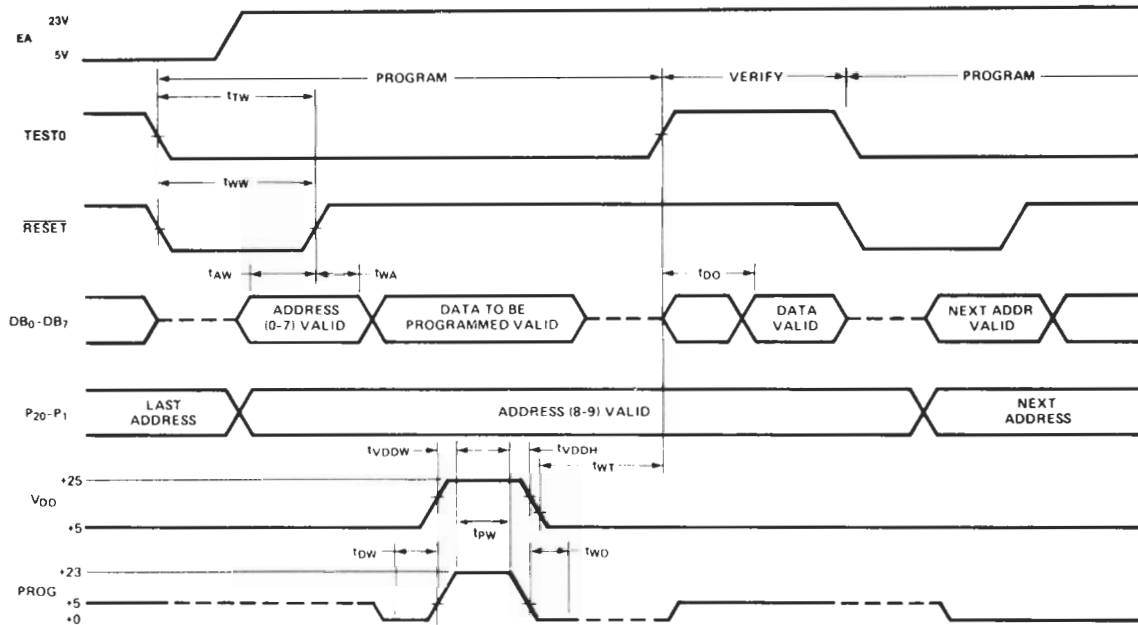
$$T_A = 25^\circ\text{C} \pm 5^\circ\text{C}, V_{CC} = 5\text{V} \pm 5\%, V_{DD} = 25\text{V} \pm 1\text{V}$$

| Symbol            | Parameter                                   | Min. | Max. | Unit | Test Conditions |
|-------------------|---|------|------|------|-----------------|
| V <sub>DOH</sub>  | V <sub>DD</sub> Program Voltage High Level  | 24.0 | 26.0 | V    |                 |
| V <sub>DDL</sub>  | V <sub>DD</sub> Voltage Low Level           | 4.75 | 5.25 | V    |                 |
| V <sub>PH</sub>   | PROG Program Voltage High Level             | 21.5 | 24.5 | V    |                 |
| V <sub>PL</sub>   | PROG Voltage Low Level                      |      | 0.2  | V    |                 |
| V <sub>EAH</sub>  | EA Program or Verify Voltage High Level     | 21.5 | 24.5 | V    |                 |
| V <sub>EAL</sub>  | EA Voltage Low Level                        |      | 5.25 | V    |                 |
| I <sub>DD</sub>   | V <sub>DD</sub> High Voltage Supply Current |      | 30.0 | mA   |                 |
| I <sub>PROG</sub> | PROG High Voltage Supply Current            |      | 16.0 | mA   |                 |
| I <sub>EA</sub>   | EA High Voltage Supply Current              |      | 1.0  | mA   |                 |

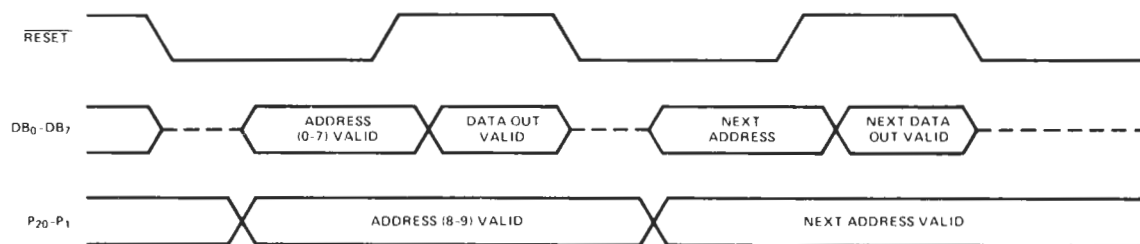
## 8041A/8641A/8741A

## WAVEFORMS FOR PROGRAMMING

## COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



## VERIFY MODE (ROM/EPROM)



## NOTES:

1. PROG MUST FLOAT IF EA IS LOW (i.e.,  $\neq 23V$ ), OR IF  $T_0 = 5V$  FOR THE 8741A. FOR THE 8041A PROG MUST ALWAYS FLOAT.
2. XTAL1 AND XTAL2 DRIVEN BY 3.8 MHz CLOCK WILL GIVE 4.17  $\mu\text{sec}$   $t_{CY}$ . THIS IS ACCEPTABLE FOR 8741A-8 PARTS AS WELL AS STANDARD PARTS.
3. AO MUST BE HELD LOW (i.e.,  $= 0V$ ) DURING PROGRAM/VERIFY MODES.

The 8741A EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.



## **Video Logic Board**

# HD6845S, HD68A45S, HD68B45S

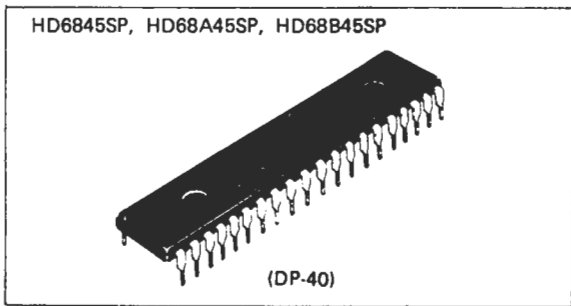
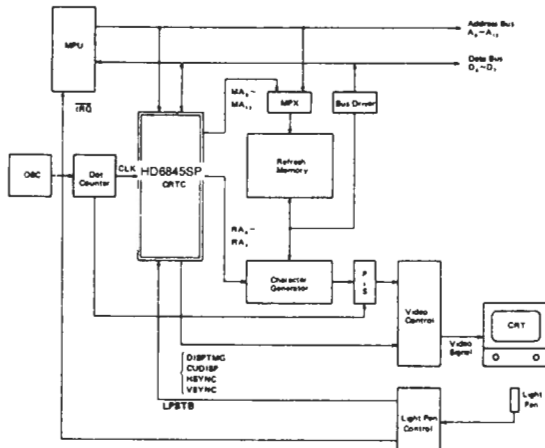
## CRTC (CRT Controller)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

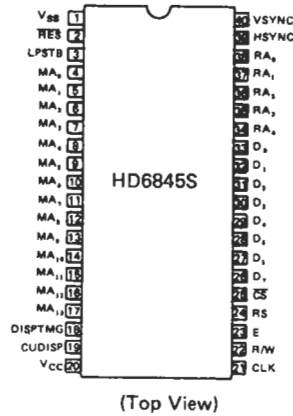
### FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interlace/Non-interlace Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply
- Upward compatible with MC6845

### SYSTEM BLOCK DIAGRAM



### PIN ARRANGEMENT



### ORDERING INFORMATION

| CRTC      | Bus Timing | CRT Display Timing |
|-----------|------------|--------------------|
| HD6845SP  | 1.0 MHz    | 3.7 MHz max.       |
| HD68A45SP | 1.5 MHz    |                    |
| HD68B45SP | 2.0 MHz    |                    |



## HD6845S, HD68A45S, HD68B45S

## ■ ABSOLUTE MAXIMUM RATINGS

| Item                  | Symbol     | Value       | Unit |
|-----------------------|------------|-------------|------|
| Supply Voltage        | $V_{CC}^*$ | -0.3 ~ +7.0 | V    |
| Input Voltage         | $V_{in}^*$ | -0.3 ~ +7.0 | V    |
| Operating Temperature | $T_{opr}$  | -20 ~ +75   | °C   |
| Storage Temperature   | $T_{stg}$  | -55 ~ +150  | °C   |

\* With respect to  $V_{SS}$  (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

## ■ RECOMMENDED OPERATING CONDITIONS

| Item                  | Symbol     | min  | typ | max      | Unit |
|-----------------------|------------|------|-----|----------|------|
| Supply Voltage        | $V_{CC}^*$ | 4.75 | 5   | 5.25     | V    |
| Input Voltage         | $V_{IL}^*$ | -0.3 | -   | 0.8      | V    |
|                       | $V_{IH}^*$ | 2.0  | -   | $V_{CC}$ | V    |
| Operating Temperature | $T_{opr}$  | -20  | 25  | 75       | °C   |

\* With respect to  $V_{SS}$  (SYSTEM GND)

## ■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = -20 \sim +75^\circ C$ , unless otherwise noted.)

| Item                                  | Symbol    | Test Condition  | min            | typ | max      | Unit    |    |
|---------------------------------------|-----------|---|----------------|-----|----------|---------|----|
| Input "High" Voltage                  | $V_{IH}$  |   | 2.0            | -   | $V_{CC}$ | V       |    |
| Input "Low" Voltage                   | $V_{IL}$  |   | -0.3           | -   | 0.8      | V       |    |
| Input Leakage Current                 | $I_{in}$  | $V_{in} = 0 \sim 5.25V$ (Except $D_0 \sim D_7$ )                | -2.5           | -   | 2.5      | $\mu A$ |    |
| Three-State Input Current (off-state) | $I_{TSI}$ | $V_{in} = 0.4 \sim 2.4V$<br>$V_{CC} = 5.25V$ ( $D_0 \sim D_7$ ) | -10            | -   | 10       | $\mu A$ |    |
| Output "High" Voltage                 | $V_{OH}$  | $I_{LOAD} = -205 \mu A$ ( $D_0 \sim D_7$ )                      | 2.4            | -   | -        | V       |    |
|                                       |           | $I_{LOAD} = -100 \mu A$ (Other Outputs)                         |                |     |          |         |    |
| Output "Low" Voltage                  | $V_{OL}$  | $I_{LOAD} = 1.6 mA$   | -              | -   | 0.4      | V       |    |
| Input Capacitance                     | $C_{in}$  | $V_{in} = 0$<br>$T_a = 25^\circ C$<br>$f = 1.0 MHz$             | $D_0 \sim D_7$ | -   | -        | 12.5    | pF |
|                                       |           |   | Other Inputs   | -   | -        | 10.0    | pF |
| Output Capacitance                    | $C_{out}$ | $V_{in} = 0V$ , $T_a = 25^\circ C$ , $f = 1.0 MHz$              | -              | -   | 10.0     | pF      |    |
| Power Dissipation                     | $P_D$     |   | -              | 600 | 1000     | mW      |    |

## HD6845S, HD68A45S, HD68B45S

• AC CHARACTERISTICS ( $V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = -20 \sim +75^\circ C$ , unless otherwise noted.)

## 1. TIMING OF CRTIC SIGNAL

| Item                               | Symbol           | Test Condition | min | typ | max | Unit |
|------------------------------------|------------------|----------------|-----|-----|-----|------|
| Clock Cycle Time                   | $t_{cyc}$        | Fig. 1         | 270 | —   | —   | ns   |
| Clock "High" Pulse Width           | $PW_{CH}$        |                | 130 | —   | —   | ns   |
| Clock "Low" Pulse Width            | $PW_{CL}$        |                | 130 | —   | —   | ns   |
| Rise and Fall Time for Clock Input | $t_{Cr}, t_{Cf}$ |                | —   | —   | 20  | ns   |
| Memory Address Delay Time          | $t_{MAD}$        |                | —   | —   | 160 | ns   |
| Raster Address Delay Time          | $t_{RAD}$        |                | —   | —   | 160 | ns   |
| DISPTMG Delay Time                 | $t_{DTP}$        |                | —   | —   | 250 | ns   |
| CUDISP Delay Time                  | $t_{CDD}$        |                | —   | —   | 250 | ns   |
| Horizontal Sync Delay Time         | $t_{HSD}$        |                | —   | —   | 200 | ns   |
| Vertical Sync Delay Time           | $t_{VSD}$        |                | —   | —   | 250 | ns   |
| Light Pen Strobe Pulse Width       | $PW_{LPH}$       | Fig. 2         | 60  | —   | —   | ns   |
| Light Pen Strobe                   | $t_{LPD1}$       |                | —   | —   | 70  | ns   |
| Uncertain Time of Acceptance       | $t_{LPD2}$       |                | —   | —   | 0   | ns   |

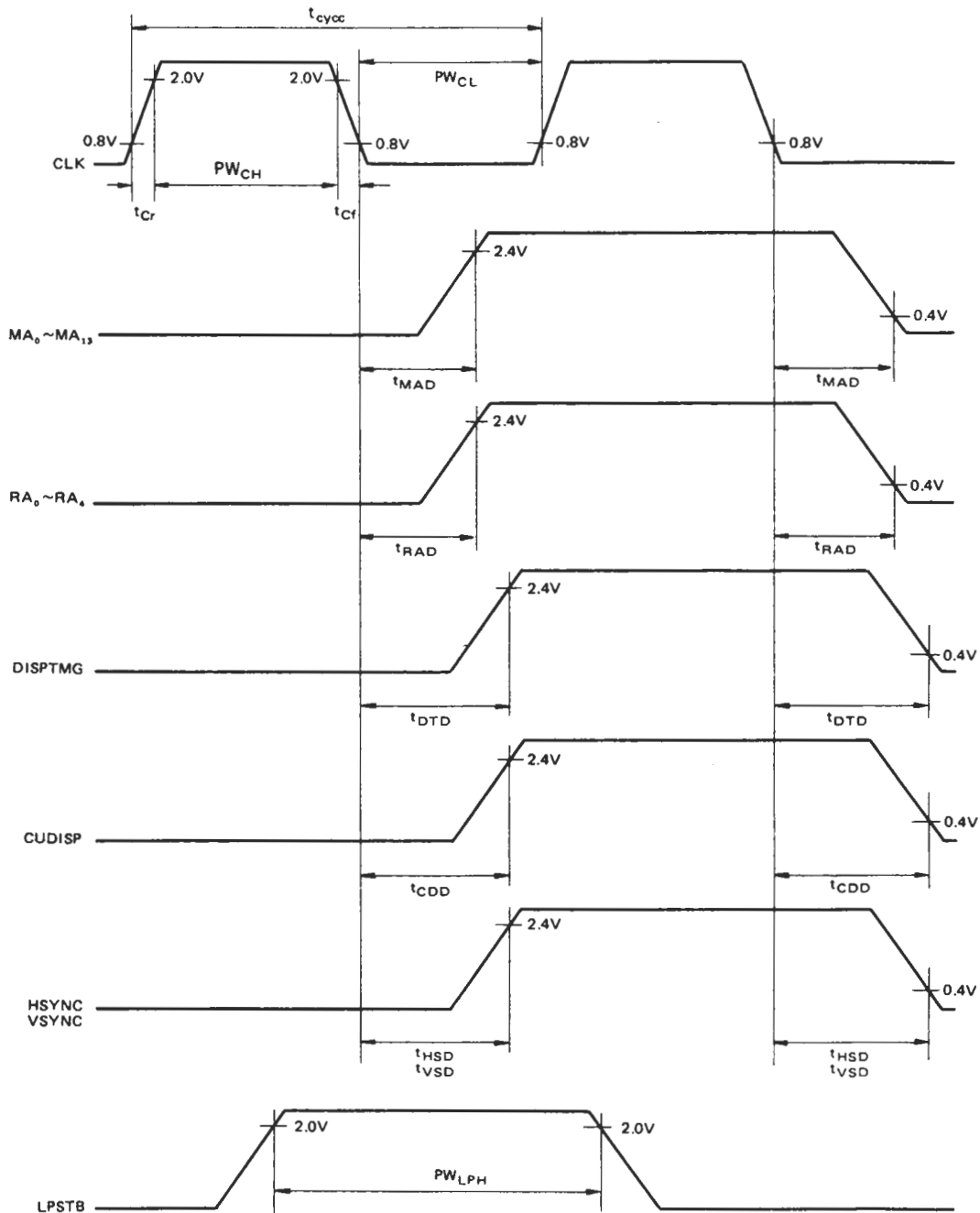
## 2. MPU READ TIMING

| Item                      | Symbol           | Test Condition | HD6845SP |     |     | HD68A45SP |     |     | HD68B45SP |     |     | Unit    |
|---------------------------|------------------|----------------|----------|-----|-----|-----------|-----|-----|-----------|-----|-----|---------|
|                           |                  |                | min      | typ | max | min       | typ | max | min       | typ | max |         |
| Enable Cycle Time         | $t_{tvcE}$       | Fig. 3         | 1.0      | —   | —   | 0.666     | —   | —   | 0.5       | —   | —   | $\mu s$ |
| Enable "High" Pulse Width | $PW_{EH}$        |                | 0.45     | —   | —   | 0.280     | —   | —   | 0.22      | —   | —   | $\mu s$ |
| Enable "Low" Pulse Width  | $PW_{EL}$        |                | 0.40     | —   | —   | 0.280     | —   | —   | 0.21      | —   | —   | $\mu s$ |
| Enable Rise and Fall Time | $t_{Er}, t_{Ef}$ |                | —        | —   | 25  | —         | —   | 25  | —         | —   | 25  | ns      |
| Address Set Up Time       | $t_{AS}$         |                | 140      | —   | —   | 140       | —   | —   | 70        | —   | —   | ns      |
| Data Delay Time           | $t_{DDR}$        |                | —        | —   | 320 | —         | —   | 220 | —         | —   | 180 | ns      |
| Data Hold Time            | $t_H$            |                | 10       | —   | —   | 10        | —   | —   | 10        | —   | —   | ns      |
| Address Hold Time         | $t_{AH}$         |                | 10       | —   | —   | 10        | —   | —   | 10        | —   | —   | ns      |
| Data Access Time          | $t_{ACC}$        |                | —        | —   | 460 | —         | —   | 360 | —         | —   | 250 | ns      |

## 3. MPU WRITE TIMING

| Item                      | Symbol           | Test Condition | HD6845SP |     |     | HD68A45SP |     |     | HD68B45SP |     |     | Unit    |
|---------------------------|------------------|----------------|----------|-----|-----|-----------|-----|-----|-----------|-----|-----|---------|
|                           |                  |                | min      | typ | max | min       | typ | max | min       | typ | max |         |
| Enable Cycle Time         | $t_{cycE}$       | Fig. 4         | 1.0      | —   | —   | 0.666     | —   | —   | 0.5       | —   | —   | $\mu s$ |
| Enable "High" Pulse Width | $PW_{EH}$        |                | 0.45     | —   | —   | 0.280     | —   | —   | 0.22      | —   | —   | $\mu s$ |
| Enable "Low" Pulse Width  | $PW_{EL}$        |                | 0.40     | —   | —   | 0.280     | —   | —   | 0.21      | —   | —   | $\mu s$ |
| Enable Rise and Fall Time | $t_{Er}, t_{Ef}$ |                | —        | —   | 25  | —         | —   | 25  | —         | —   | 25  | ns      |
| Address Set Up Time       | $t_{AS}$         |                | 140      | —   | —   | 140       | —   | —   | 70        | —   | —   | ns      |
| Data Set Up Time          | $t_{DSW}$        |                | 195      | —   | —   | 80        | —   | —   | 60        | —   | —   | ns      |
| Data Hold Time            | $t_H$            |                | 10       | —   | —   | 10        | —   | —   | 10        | —   | —   | ns      |
| Address Hold Time         | $t_{AH}$         |                | 10       | —   | —   | 10        | —   | —   | 10        | —   | —   | ns      |

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This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 9 ~ 15.

Figure 1 Time Chart of the CRTC

HD6845S, HD68A45S, HD68B45S

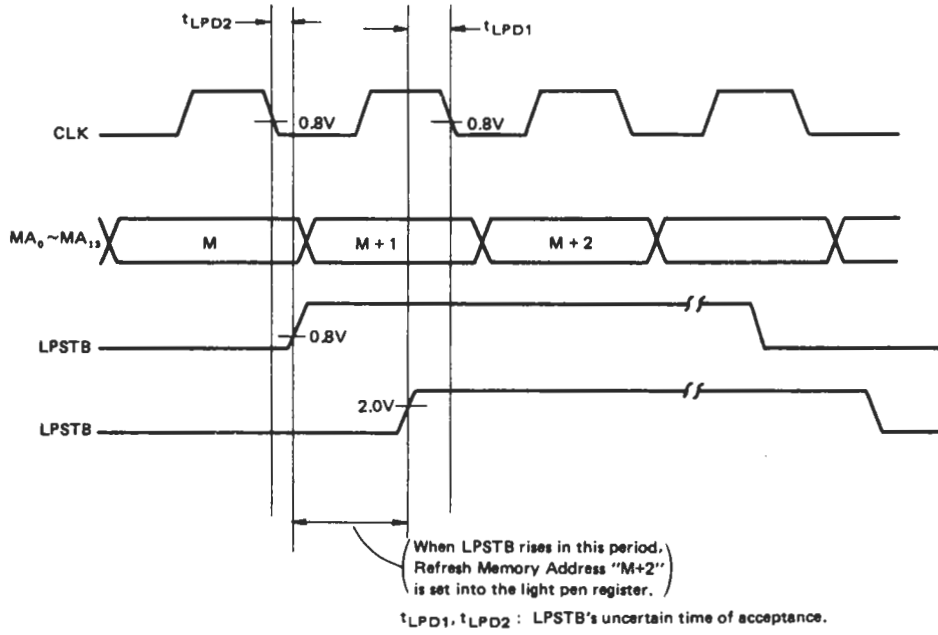


Figure 2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

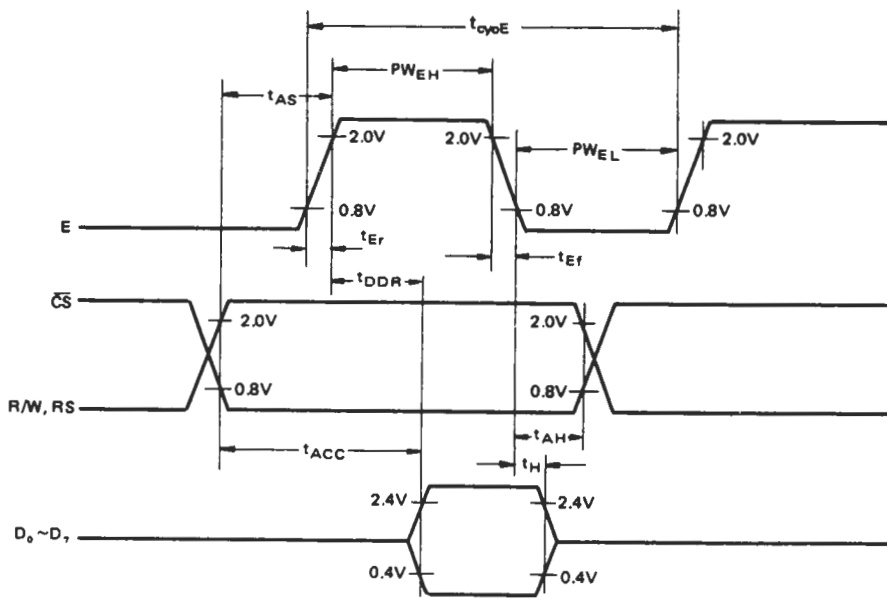


Figure 3 Read Sequence

## HD6845S, HD68A45S, HD68B45S

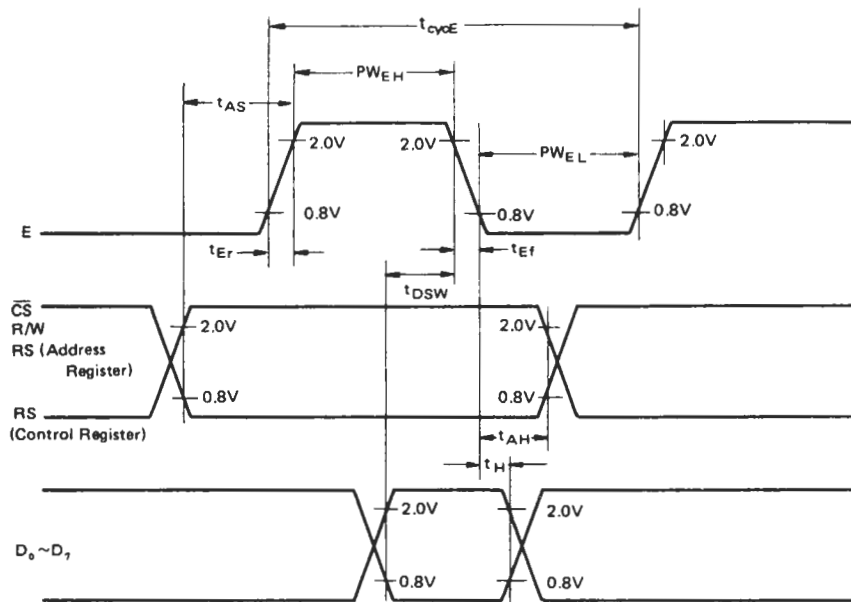


Figure 4 Write Sequence

#### ■ SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate  $RA_0 \sim RA_4$ , DISPTMG, HSYNC, and VSYNC.  $RA_0 \sim RA_4$  are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit.

Linear address generator generates refresh memory address  $MA_0 \sim MA_{13}$  to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16k words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.



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 HD6845S, HD68A45S, HD68B45S
 

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**■ FUNCTION OF SIGNAL LINE**

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

**● Interface Signals to MPU**
**Bi-directional Data Bus (D<sub>0</sub>~D<sub>7</sub>)**

Bi-directional data bus(D<sub>0</sub>~D<sub>7</sub>) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

**Read/Write (R/W)**

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transferred to MPU. When R/W is at "Low" level, data of MPU is transferred to CRTC.

**Chip Select ( $\overline{CS}$ )**

Chip Select signal ( $\overline{CS}$ ) is used to address the CRTC. When  $\overline{CS}$  is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

**Register Select (RS)**

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A<sub>0</sub>) of MPU address bus.

**Enable(E)**

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System  $\phi_2$  clock.

**Reset ( $\overline{RES}$ )**

Reset signal ( $\overline{RES}$ ) is an input signal used to reset the CRTC. When  $\overline{RES}$  is at "Low" level, it forces the CRTC into the following status.

- 1) All the counters in the CRTC are cleared and the device stops the display operation.
- 2) All the outputs go down to "Low" level.
- 3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

- 1)  $\overline{RES}$  signal has capability of reset function only when LPSTB is at "Low" level.
- 2) The CRTC starts the display operation immediately after  $\overline{RES}$  signal goes "High".

**● Interface Signals to CRT Display Device**
**Character Clock (CLK)**

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

**Horizontal Sync (HSYNC)**

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

**Vertical Sync (VSYNC)**

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

**Display Timing (DISPTMG)**

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

**Refresh Memory Address (MA<sub>0</sub>~MA<sub>13</sub>)**

MA<sub>0</sub>~MA<sub>13</sub> are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

**Raster Address (RA<sub>0</sub>~RA<sub>4</sub>)**

RA<sub>0</sub>~RA<sub>4</sub> are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

**Cursor Display (CUDISP)**

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

**Light Pen Strobe (LPSTB)**

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address (MA<sub>0</sub>~MA<sub>13</sub>) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.





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- **Address Register (AR)**

This is a 5-bit register used to select 18 internal control registers (R0~R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0~R17 requires, first of all, to write the address of corresponding control register into this register. When RS and CS are at "Low" level, this register is selected.

- **Horizontal Total Register (R0)**

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even.

- **Horizontal Displayed Register (R1)**

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

- **Horizontal Sync Position Register (R2)**

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

- **Sync Width Register (R3)**

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" cannot be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

- **Vertical Total Register (R4)**

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRT. When N is total number of lines, (N-1) shall be programmed to this register.

- **Vertical Total Adjust Register (R5)**

This is a register used to program the optimum number to adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

- **Vertical Displayed Register (R6)**

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

| VSW            |                |                |                | Pulse Width |
|----------------|----------------|----------------|----------------|-------------|
| 2 <sup>7</sup> | 2 <sup>6</sup> | 2 <sup>5</sup> | 2 <sup>4</sup> |             |
| 0              | 0              | 0              | 0              | 16H         |
| 0              | 0              | 0              | 1              | 1           |
| 0              | 0              | 1              | 0              | 2           |
| 0              | 0              | 1              | 1              | 3           |
| 0              | 1              | 0              | 0              | 4           |
| 0              | 1              | 0              | 1              | 5           |
| 0              | 1              | 1              | 0              | 6           |
| 0              | 1              | 1              | 1              | 7           |
| 1              | 0              | 0              | 0              | 8           |
| 1              | 0              | 0              | 1              | 9           |
| 1              | 0              | 1              | 0              | 10          |
| 1              | 0              | 1              | 1              | 11          |
| 1              | 1              | 0              | 0              | 12          |
| 1              | 1              | 0              | 1              | 13          |
| 1              | 1              | 1              | 0              | 14          |
| 1              | 1              | 1              | 1              | 15          |

H: Raster period

Table 3 Pulse Width of Horizontal Sync Signal

| HSW            |                |                |                | Pulse Width |
|----------------|----------------|----------------|----------------|-------------|
| 2 <sup>3</sup> | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> |             |
| 0              | 0              | 0              | 0              | — (Note)    |
| 0              | 0              | 0              | 1              | 1 CH        |
| 0              | 0              | 1              | 0              | 2           |
| 0              | 0              | 1              | 1              | 3           |
| 0              | 1              | 0              | 0              | 4           |
| 0              | 1              | 0              | 1              | 5           |
| 0              | 1              | 1              | 0              | 6           |
| 0              | 1              | 1              | 1              | 7           |
| 1              | 0              | 0              | 0              | 8           |
| 1              | 0              | 0              | 1              | 9           |
| 1              | 0              | 1              | 0              | 10          |
| 1              | 0              | 1              | 1              | 11          |
| 1              | 1              | 0              | 0              | 12          |
| 1              | 1              | 0              | 1              | 13          |
| 1              | 1              | 1              | 0              | 14          |
| 1              | 1              | 1              | 1              | 15          |

CH: Character clock period  
(Note) HSW = "0" cannot be used.

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● **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

● **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP signal and DISPTMG signal.

**Interlace Mode Program Bit (V, S)**

Raster scan mode is programmed in the V, S bit.

Table 4 Interlace Mode ( $2^1, 2^0$ )

| V | S | Raster Scan Mode            |
|---|---|-----------------------------|
| 0 | 0 | Non-interlace Mode          |
| 1 | 0 |                             |
| 0 | 1 | Interlace Sync Mode         |
| 1 | 1 | Interlace Sync & Video Mode |

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

● **Skew Program Bit (C1, C0, D1, D0)**

These are used to program the skew (delay) of CUDISP signal and DISPTMG signal.

Skew of these two kinds of signals are programmed separately.

Table 5 DISPTMG Skew Bit ( $2^7, 2^6$ )

| D1 | D0 | DISPTMG Signal     |
|----|----|--------------------|
| 0  | 0  | Non-skew           |
| 0  | 1  | One-character skew |
| 1  | 0  | Two-character skew |
| 1  | 1  | Non-output         |

Table 6 Cursor Skew Bit ( $2^5, 2^4$ )

| C1 | C0 | Non-skew           |
|----|----|--------------------|
| 0  | 0  | Non-skew           |
| 0  | 1  | One-character skew |
| 1  | 0  | Two-character skew |
| 1  | 1  | Non-output         |

Skew function is used to delay the output timing of CUDISP and DISPTMG signals in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

● **Maximum Raster Address Register (R9)**

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including space. This register is programmed as follows.

**Non-interlace Mode, Interlace Sync Mode**

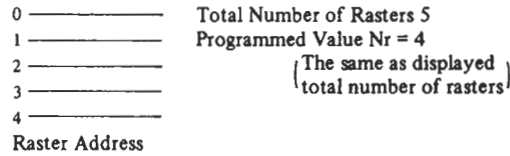
When total number of rasters is RN, (RN-1) shall be programmed.

**Interlace Sync & Video Mode**

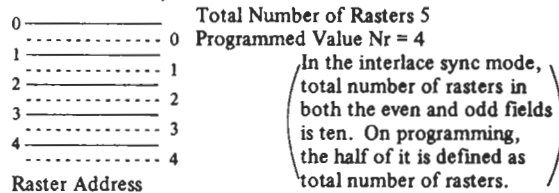
When total number of rasters is RN, (RN-2) shall be programmed.

This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

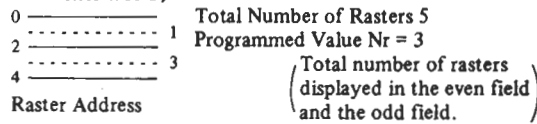
**Non-interlace Mode**



**Interlace Sync Mode**



**Interlace Sync & Video Mode**

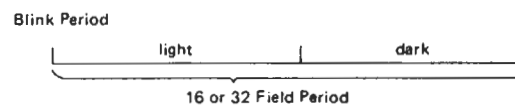


● **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit ( $2^0 \sim 2^4$ ) and the cursor display mode by higher 2-bit ( $2^5, 2^6$ ).

Table 7 Cursor Display Mode ( $2^6, 2^5$ )

| B | P | Cursor Display Mode    |
|---|---|------------------------|
| 0 | 0 | Non-blink              |
| 0 | 1 | Cursor Non-display     |
| 1 | 0 | Blink, 16 Field Period |
| 1 | 1 | Blink, 32 Field Period |



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- **Cursor End Raster Register (R11)**  
This is register used to program the cursor end raster address.
- **Start Address Register (R12, R13)**  
These are used to program the first address of refresh memory to read out.  
Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit ( $2^6, 2^7$ ) of R12 are always "0".
- **Cursor Register (R14, R15)**  
These two read/write registers stores the cursor location. The higher 2-bit ( $2^6, 2^7$ ) of R14 are always "0".
- **Light Pen Register (R16, R17)**  
These read only registers are used to catch the detection address of the light pen. The higher 2-bit ( $2^6, 2^7$ ) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

**Restriction on Programming Internal Register**

- 1)  $0 < Nhd < Nht + 1 \leq 256$
- 2)  $0 < Nvd < Nvt + 1 \leq 128$
- 3)  $0 \leq Nhs \leq Nht$
- 4)  $0 \leq Nvsp \leq Nvt^*$
- 5)  $0 \leq NCSTART \leq NCEND \leq Nr$  (Non-interlace, Interlace sync mode)  
 $0 \leq NCSTART \leq NCEND \leq Nr + 1$  (Interlace sync & video mode)

- 6)  $2 \leq Nr \leq 30$
  - 7)  $3 \leq Nht$  (Except non-interlace mode)  
 $5 \leq Nht$  (Non-interlace mode only)
- In the interlace mode, pulse width is changed  $\pm \frac{1}{2}$  raster time when vertical sync signal extends over two fields.

**Notes for Use**

The method of directly using the value programmed in the internal register of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asynchronously with the display operation.

**Cursor Register**

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

**Start Address Register**

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

■ **OPERATION OF THE CRTC**

● **Time Chart of CRT Interface Signals**

The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 6 shows the CRT screen format. Fig. 9 shows the time chart of signals output from the CRTC.

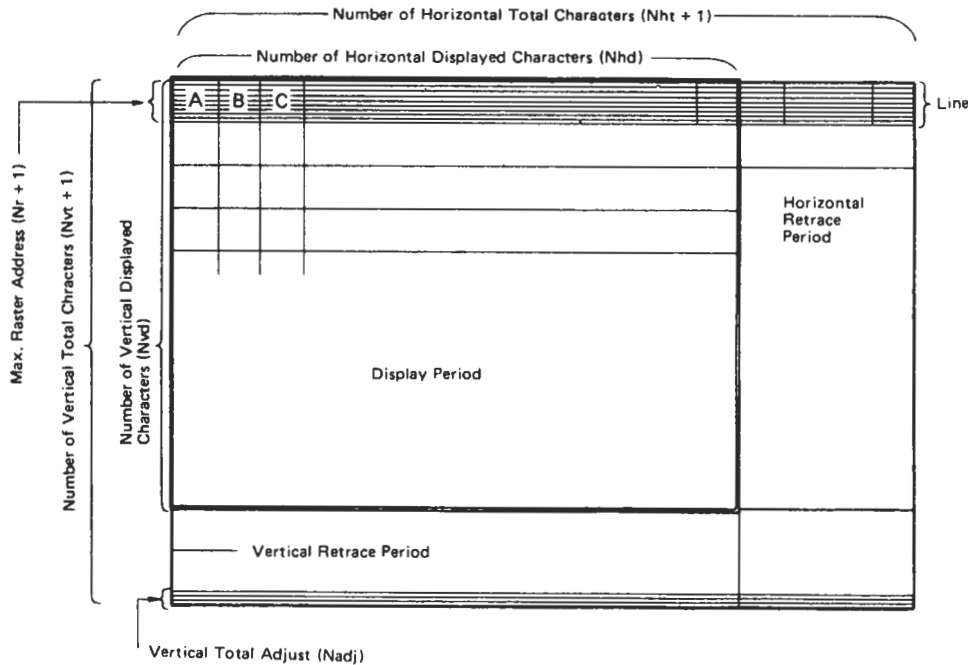


Figure 6 CRT screen Format

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Table 8 Programmed Values into the Registers

| Register | Register Name            | Value      | Register | Register Name       | Value |
|----------|--------------------------|------------|----------|---------------------|-------|
| R0       | Horizontal Total         | Nht        | R9       | Max. Raster Address | Nr    |
| R1       | Horizontal Displayed     | Nhd        | R10      | Cursor Start Raster |       |
| R2       | Horizontal Sync Position | Nhsp       | R11      | Cursor End Raster   |       |
| R3       | Sync Width               | Nvsw, Nhsw | R12      | Start Address (H)   | 0     |
| R4       | Vertical Total           | Nvt        | R13      | Start Address (L)   | 0     |
| R5       | Vertical Total Adjust    | Nadj       | R14      | Cursor (H)          |       |
| R6       | Vertical Displayed       | Nvd        | R15      | Cursor (L)          |       |
| R7       | Vertical Sync Position   | Nvsp       | R16      | Light Pen (H)       |       |
| R8       | Interlace & Skew         |            | R17      | Light Pen (L)       |       |

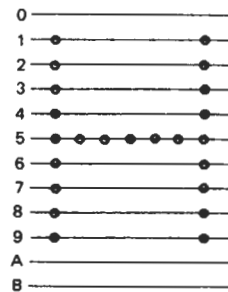
[NOTE] Nhd<Nht, Nvd<Nvt

The relation between values of Refresh Memory Address ( $MA_0 \sim MA_{13}$ ) and Raster Address ( $RA_0 \sim RA_4$ ) and the display position on the screen is shown in Fig. 15. Fig. 15 shows the case where the value of Start Address is 0.

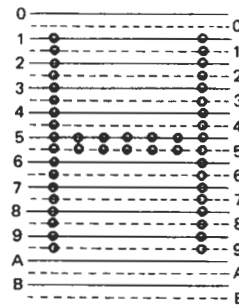
● Interlace Control

Fig. 7 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

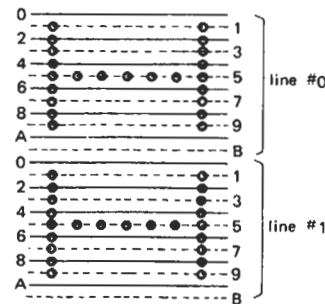
Non-interlace Mode Display



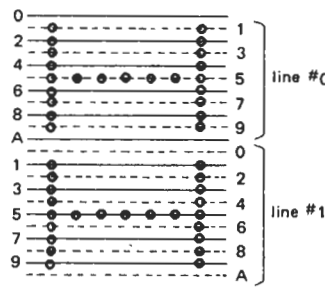
Non-interlace Mode



Interlace Sync Mode



Interlace Sync & Video Mode  
(Total number of rasters in a line is even.)



Interlace Sync & Video Mode  
(Total number of rasters in a line is odd.)

Figure 7 Example of Raster Scan Display

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**Interlace Sync & Video Mode Display**

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9 The Output of Raster Address in Interlace Sync & Video Mode

| Total Number of Rasters in a Line | Field      | Even Field   | Odd Field    |
|-----------------------------------|------------|--------------|--------------|
|                                   | Even       | Even Address | Odd Address  |
| Odd                               | Even Line* | Even Address | Odd Address  |
|                                   | Odd Line*  | Odd Address  | Even Address |

\* Internal line address begins from 0.

1) Total number of rasters in a line is even;

When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;

When total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller the case of 1). Then interlace can be displayed more stably.

[NOTE] The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields may be shifted. Characters appears distorting on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 12 shows fine chart in each mode when interlace is performed.

● **Cursor Control**

Fig. 8 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register  $\leq$  Cursor End Raster Register  $\leq$  Maximum Raster Address Register.

Time chart of CUDISP output signal is shown in Fig. 13 and Fig. 14.

■ **INTERFACE TO DISPLAY CONTROL UNIT**

Fig. 16 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

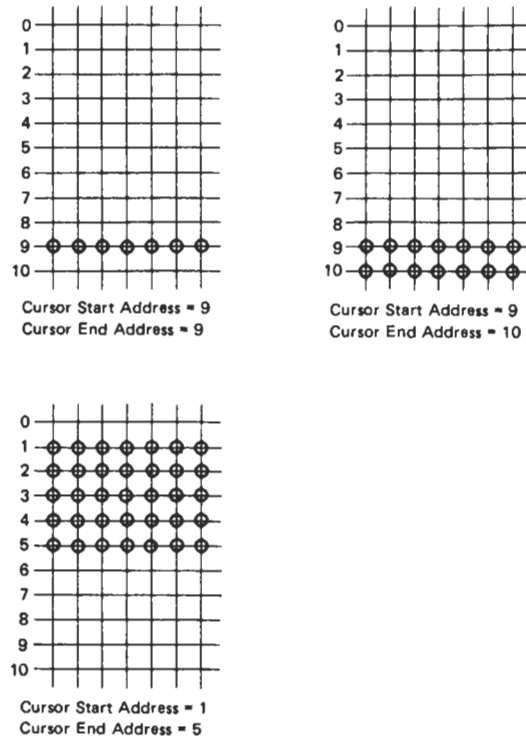


Figure 8 Cursor Control

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 17 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG signal is AND-ed with character video signal, and CUDISP signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 17 shows the example in the case that both refresh memory and CG can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 20. This method is used when a few character needed to be displayed in horizontal direction on the screen.

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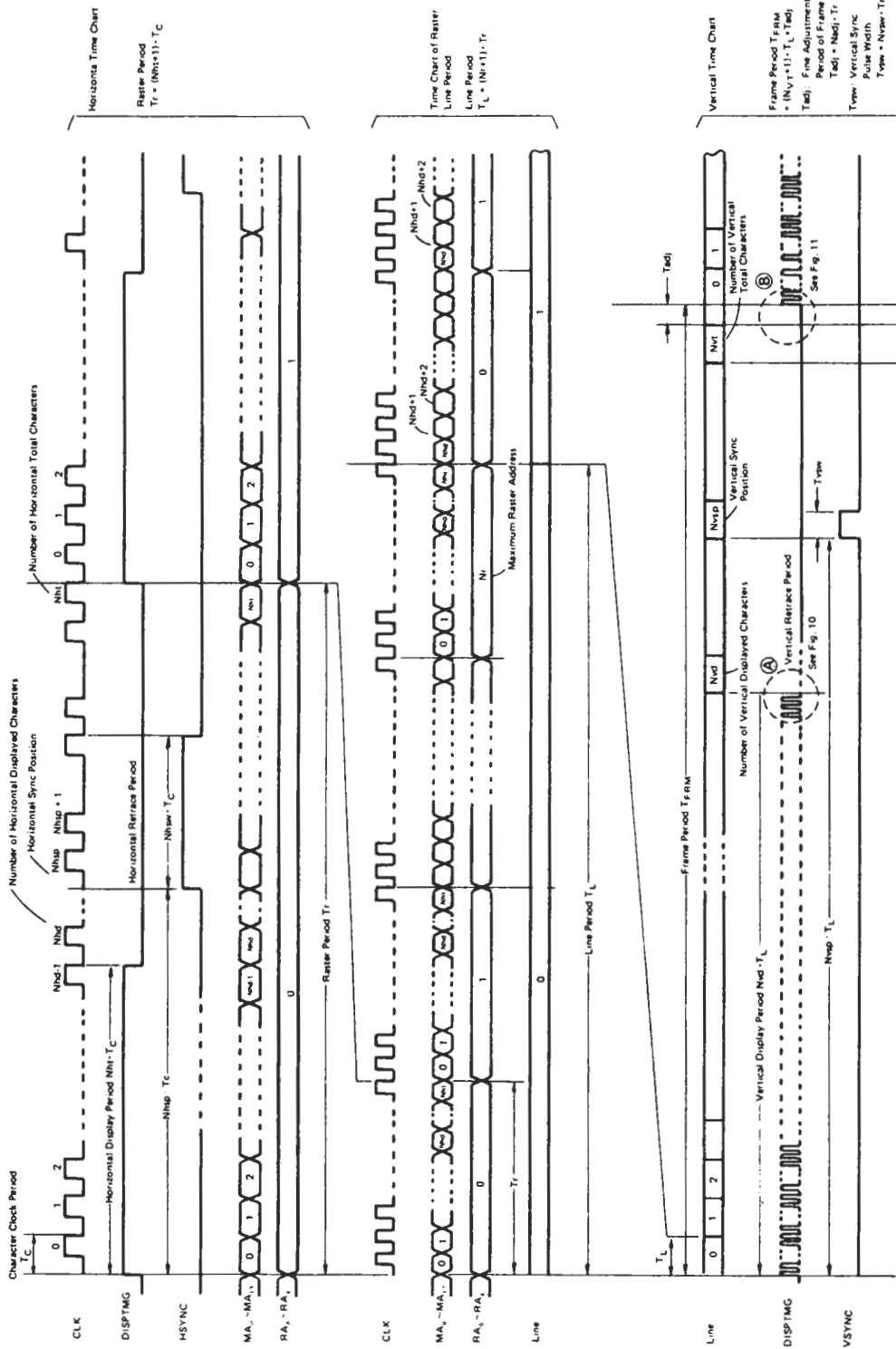


Figure 9 CRTC Time Chart

(Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.)

HD6845S, HD68A45S, HD68B45S

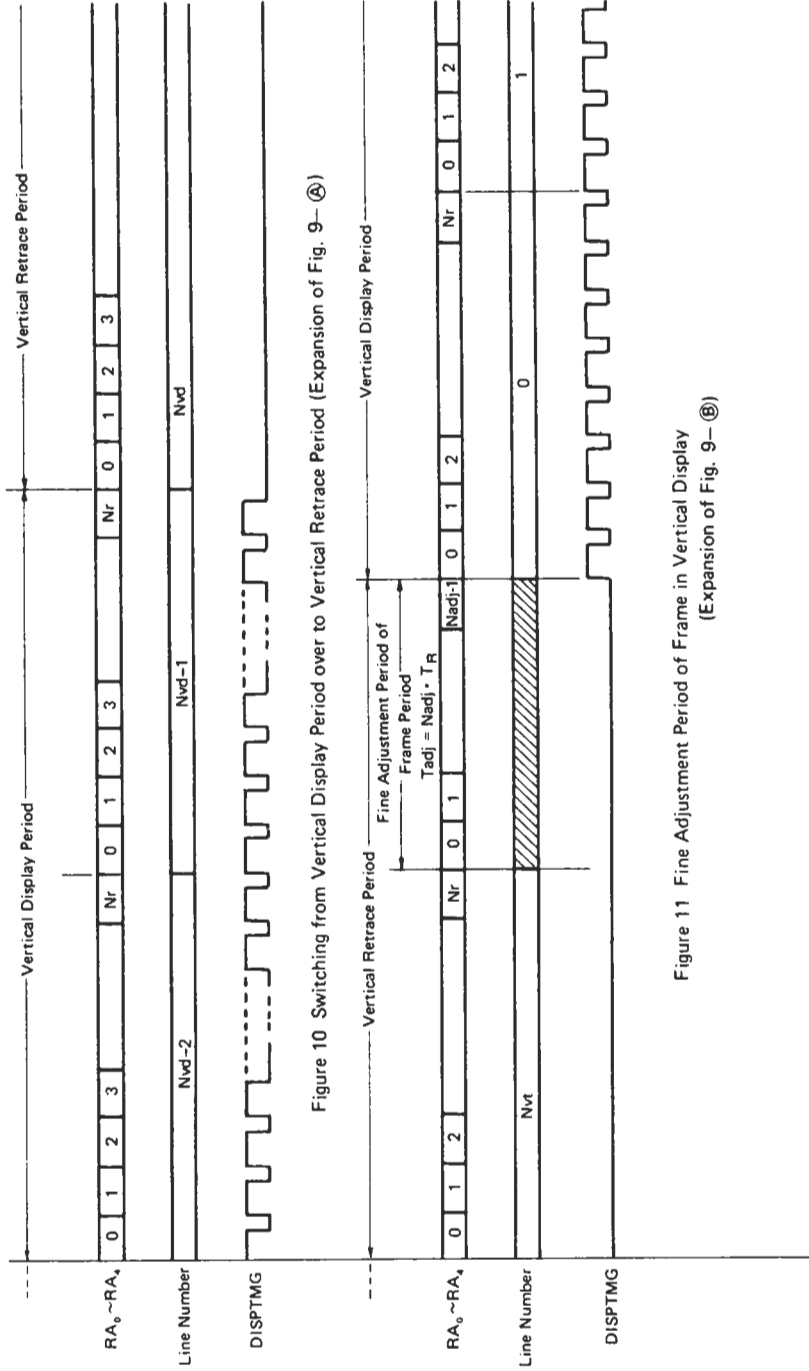
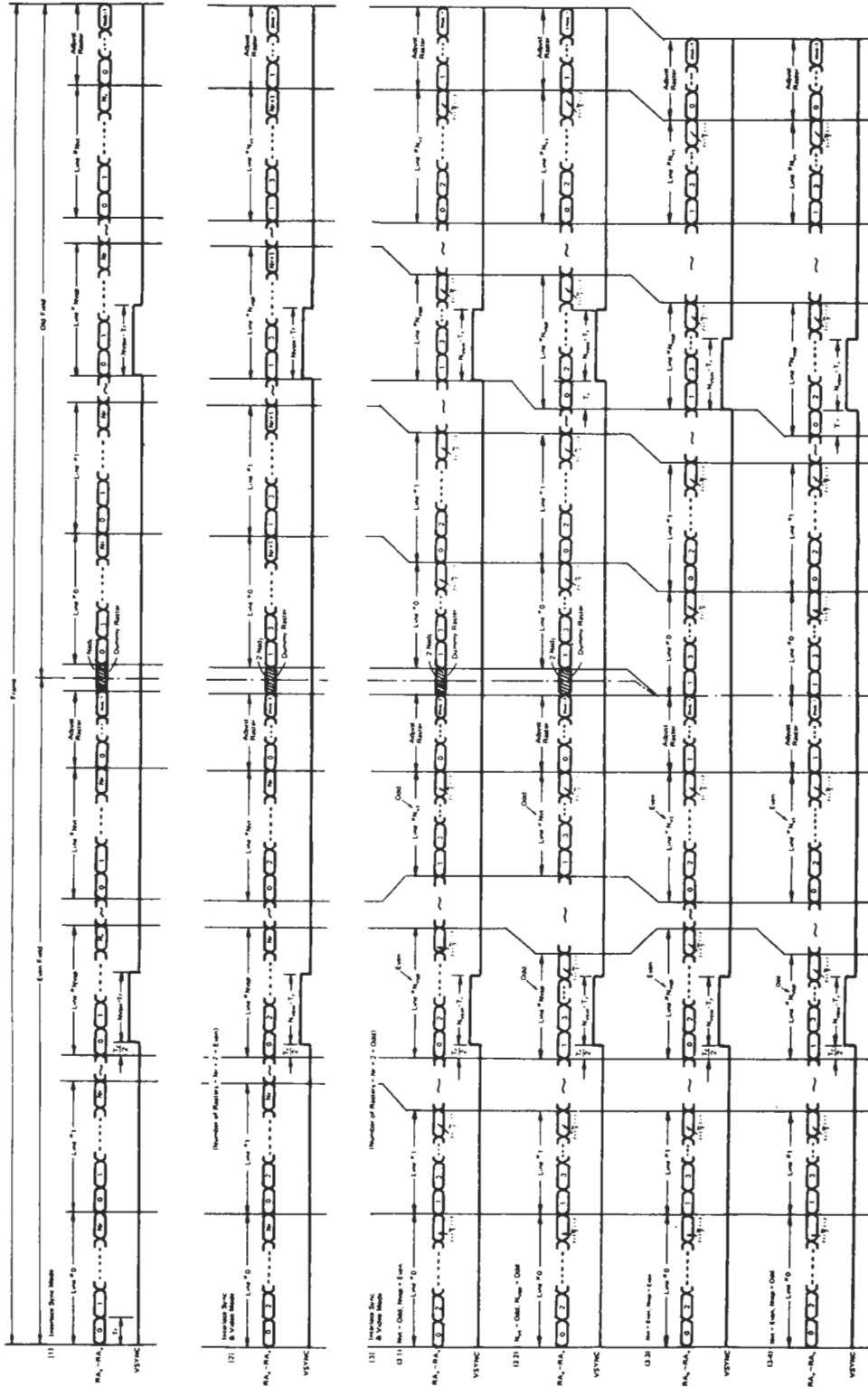


Figure 11 Fine Adjustment Period of Frame in Vertical Display (Expansion of Fig. 9-Ⓑ)

HD6845S, HD68A45S, HD68B45S





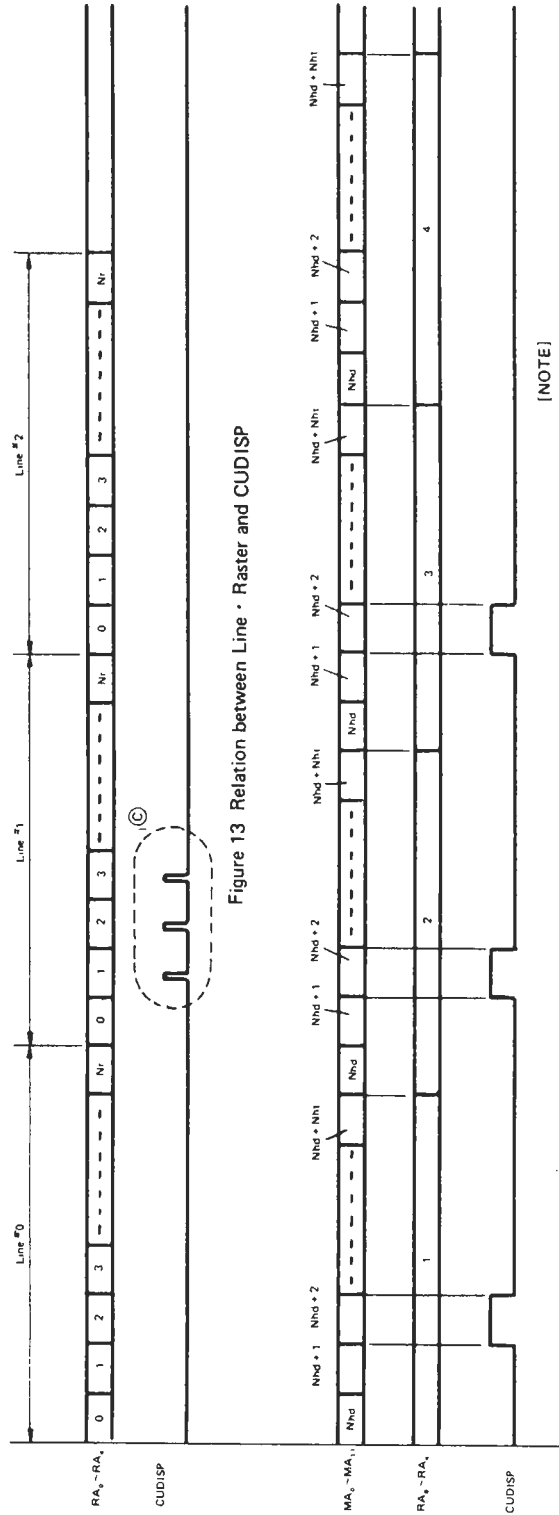


Figure 13 Relation between Line · Raster and CUDISP

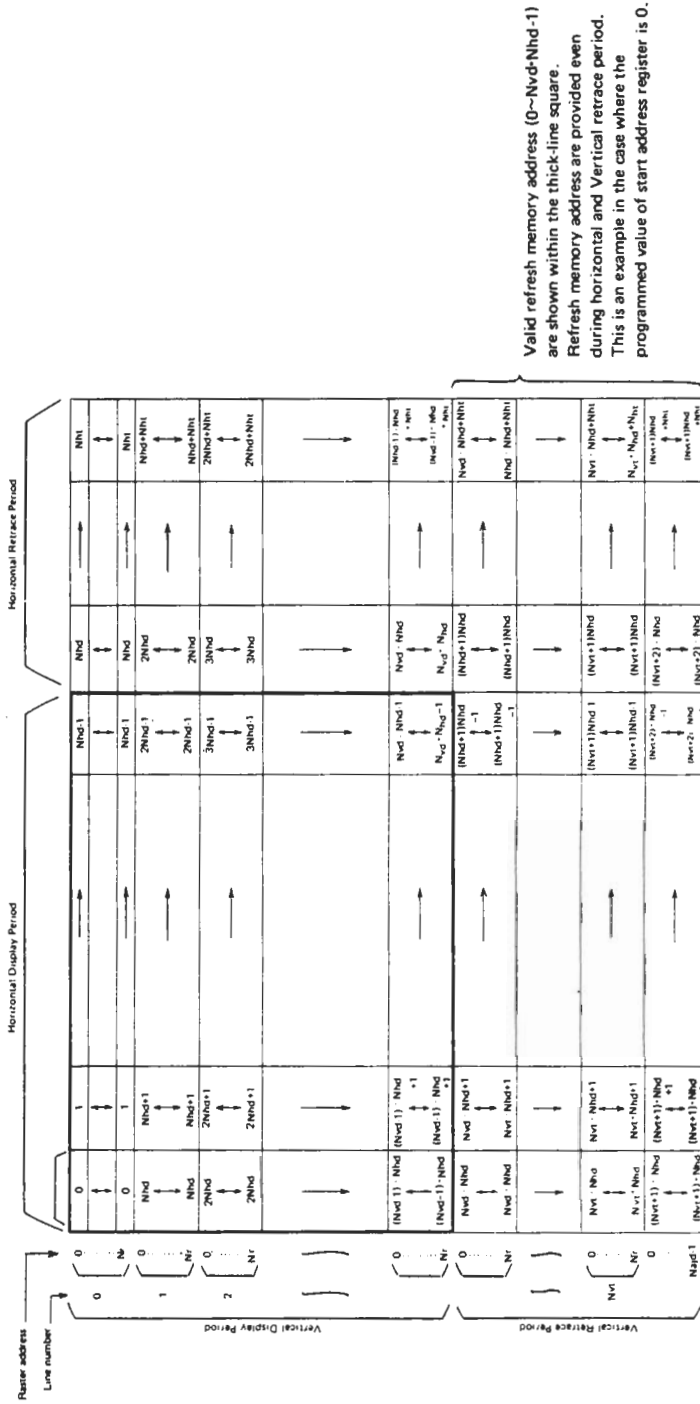
(NOTE)

- Cursor register =  $Nhd+2$
  - Cursor Start
  - Raster Register = 1
  - Cursor End
  - Raster Register = 3
- are Programmed in cursor display mode.

In blink mode, it is changed into display or non-display mode when field period is 16 or 32-time period.

Figure 14 CUDISP Output Timing (Expansion of Fig. 13-©)

HD6845S, HD68A45S, HD68B45S



Valid refresh memory address (0~Nrd-Nhd-1) are shown within the thick-line square. Refresh memory address are provided even during horizontal and vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

Figure 15 Refresh Memory Address (MA<sub>0</sub>~MA<sub>13</sub>)

HD6845S, HD68A45S, HD68B45S

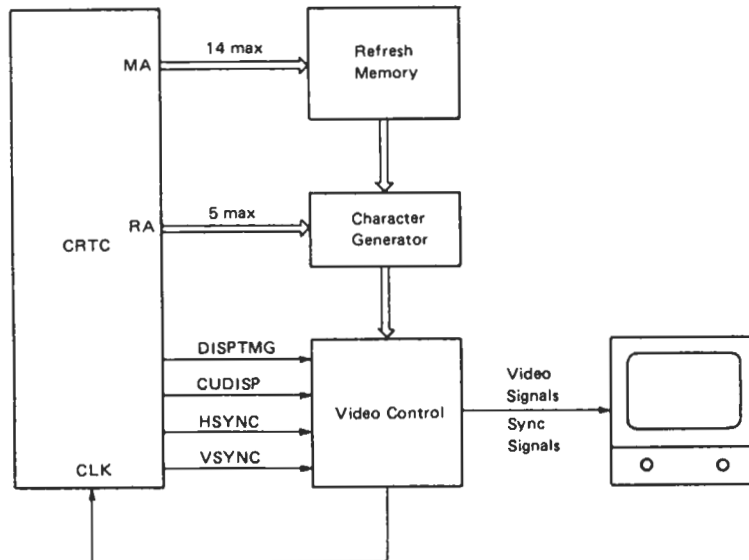


Figure 16 Interface to Display Control Unit

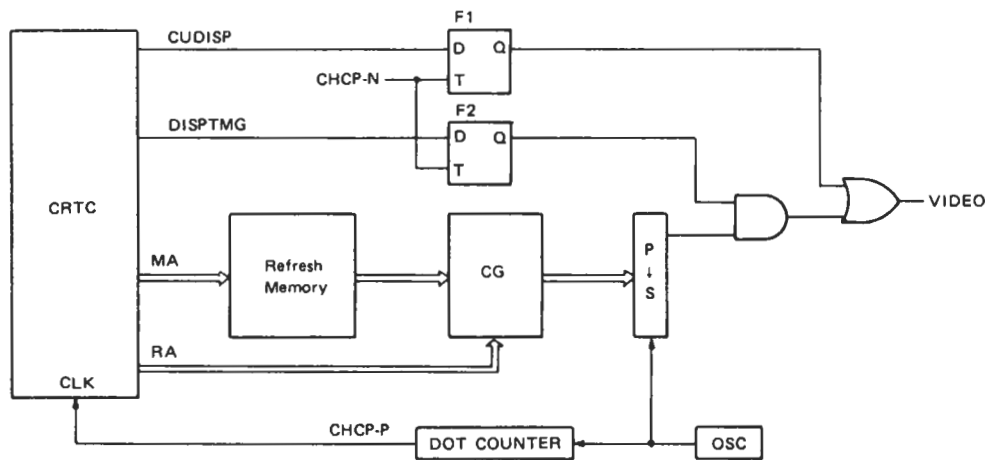


Figure 17 Display Control Unit (1)

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When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and CG cannot be accessed, the circuitry shown in Fig. 18 should be used. In this case refresh memory output shall be latched and CG shall be accessed at the next cycle. The time chart in this case is shown in Fig. 21. CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some

troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig.19 is adopted. The time chart in this case is shown in Fig.22. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG signals by delaying for two-character time.

Table 10 Circuitry Standard of Display Control Unit

| Case | Relation among $t_{CH}$ , RM and CG   | Block Diagram | Interlace & Skew Register Bit Programming |    |    |    |
|------|---|---------------|---|----|----|----|
|      |   |               | C1  | C0 | D1 | D0 |
| 1    | $t_{CH} > RM \text{ Access} + CG \text{ Access} + t_{MAD}$                                  | Fig. 17       | 0   | 0  | 0  | 0  |
| 2    | $RM \text{ Access} + CG \text{ Access} + t_{MAD} \geq t_{CH} > RM \text{ Access} + t_{MAD}$ | Fig. 18       | 0   | 1  | 0  | 1  |
| 3    | $RM \text{ Access} + t_{MAD} \geq t_{CH} > RM \text{ Access}$                               | Fig. 19       | 1   | 0  | 1  | 0  |

$t_{CH}$  : CHCP Period;  $t_{MAD}$  : MA Delay

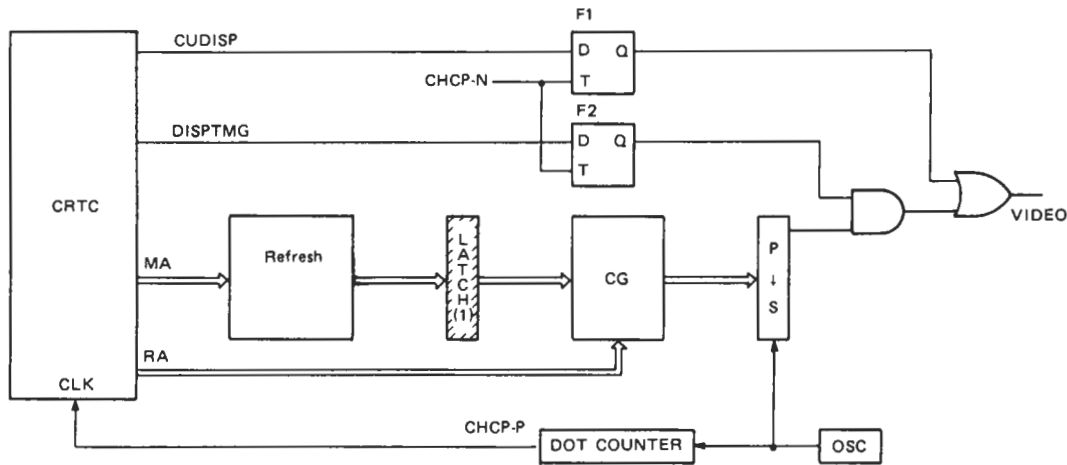


Figure 18 Display Control Unit (2)

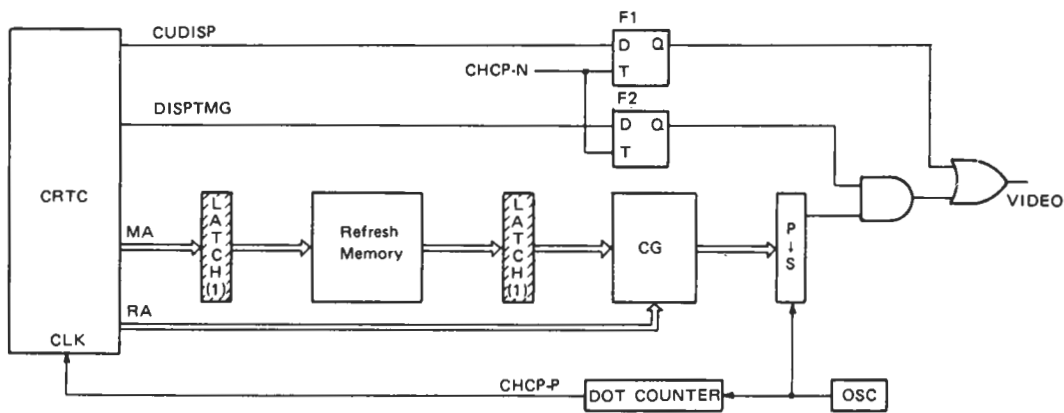


Figure 19 Display Control Unit (For high-speed display operation) (3)

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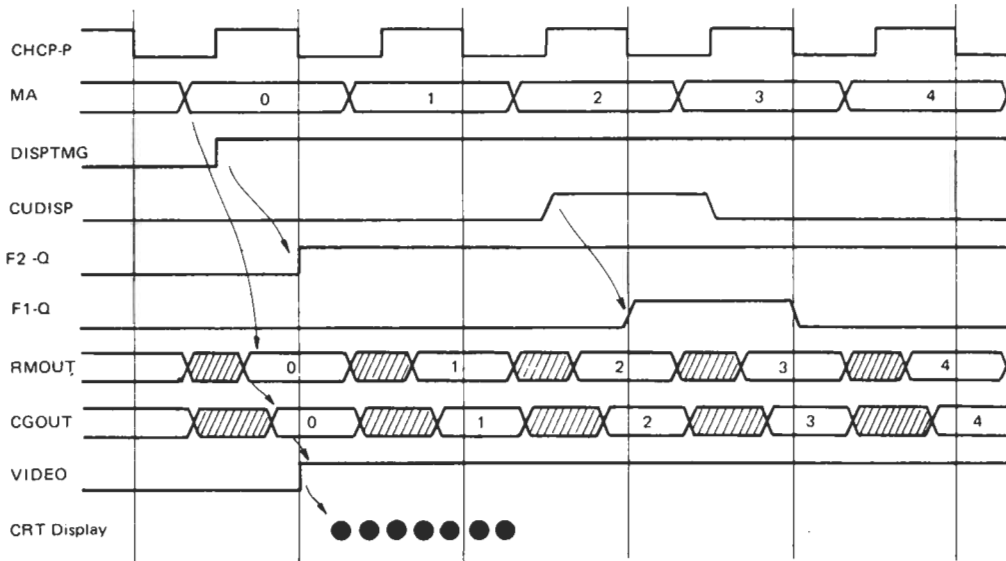


Figure 20 Time Chart of Display Control Unit (1)

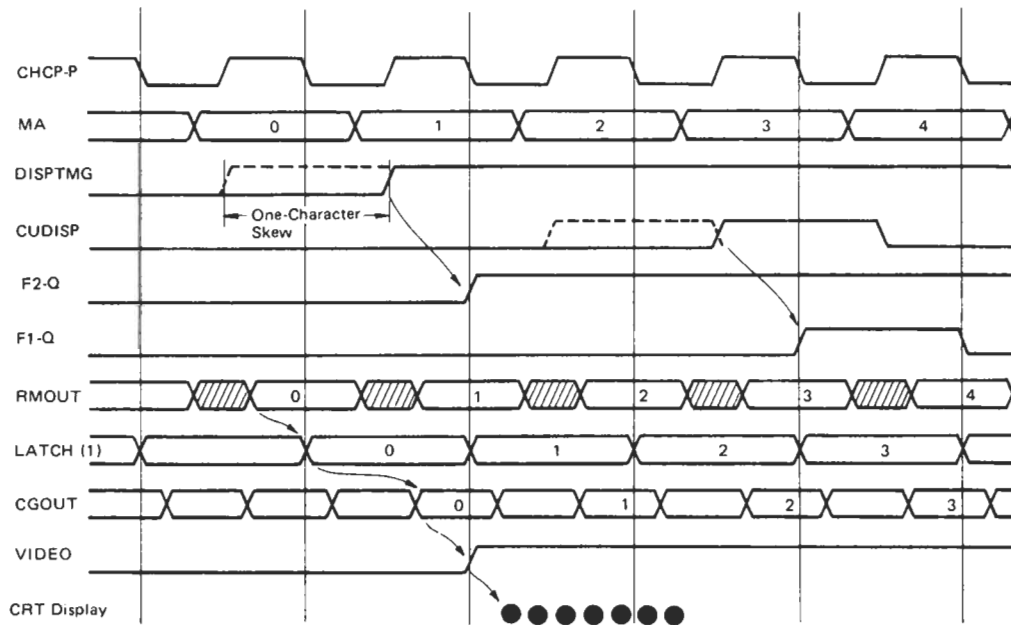


Figure 21 Time Chart of Display Control Unit (2)

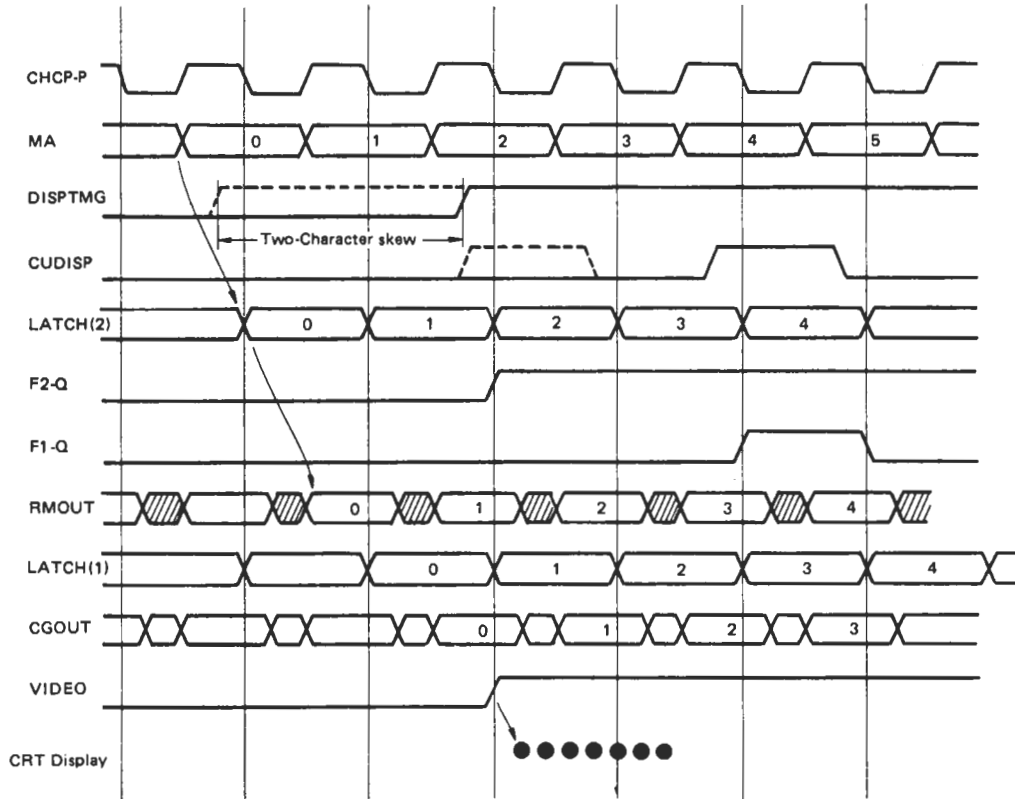


Figure 23 Time Chart of Display Unit (3)

■ **HOW TO DECIDE PARAMETERS SET ON THE CRTC**

● **How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)**

**Number of Horizontal Total Characters**

Horizontal deflection frequency  $f_h$  is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$f_h = \frac{1}{t_C (N_{ht} + 1)}$$

where,

- $t_C$  : Cycle Time of CLK (Character Clock)
- $N_{ht}$  : Programmed Value of Horizontal Total Register (R0)

**Number of Vertical Total Characters**

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

- 1) Non-interlace Mode  
 $R_t = (N_{vt} + 1)(N_r + 1) + N_{adj}$
- 2) Interlace Sync Mode  
 $R_t = (N_{vt} + 1)(N_r + 1) + N_{adj} + 0.5$
- 3) Interlace Sync & Video Mode

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj}}{2} \dots \dots \dots (a)$$

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj} + 1}{2} \dots \dots \dots (b)$$

(a) is applied when both total numbers of vertical characters ( $N_{vt} + 1$ ) and that of rasters in a line ( $N_r + 2$ ) are odd.

(b) is applied when total number of rasters ( $N_r + 2$ ) is even, or when ( $N_r + 2$ ) is odd and total number of vertical characters ( $N_{vt} + 1$ ) is even.

where,

- $R_t$  : Number of Total Rasters per frame (Including retrace period)
- $N_{vt}$  : Programmed Value of Vertical Total Register (R4)
- $N_r$  : Programmed Value of Maximum Raster Address Register (R9)
- $N_{adj}$  : Programmed Value of Vertical Total Adjust Register (R5)

**Horizontal Sync Pulse Width**

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to 15.

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**Horizontal Sync Position**

As shown in Fig. 24, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

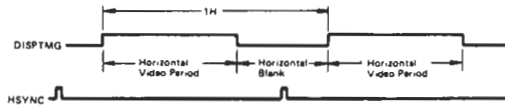


Figure 24 Time Chart of HSYNC

**Vertical Sync Pulse Width**

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of raster period. Programmed value can be selected within from 1 to 16.

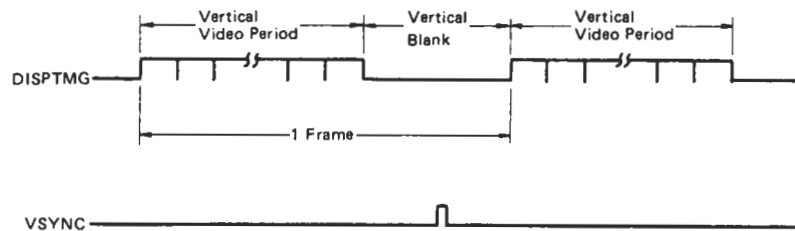


Figure 25 Time Chart of VSYNC

**Vertical Sync Position**

As shown in Fig. 25, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

• **How to Decide Parameters Based on Screen Format**

**Dot Number of Characters (Horizontal)**

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 26. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 27.

**Dot Number of Characters (Vertical)**

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 26. Dot number of characters (vertical) is programmed to maximum raster address (register R9) of CRT. When  $N_r$  is programmed

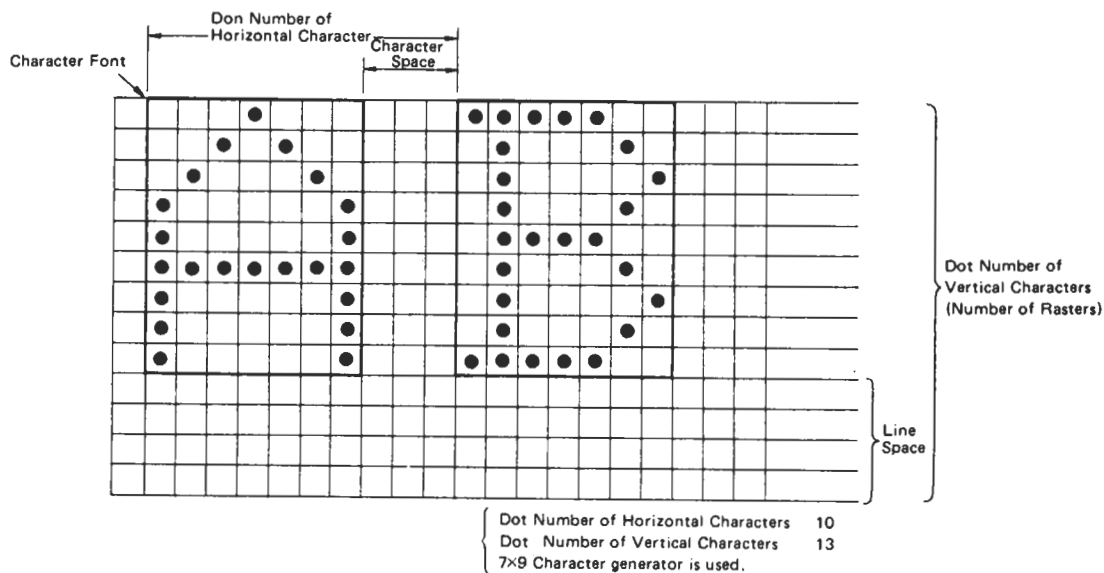


Figure 26 Dot Number of Horizontal and Vertical Characters

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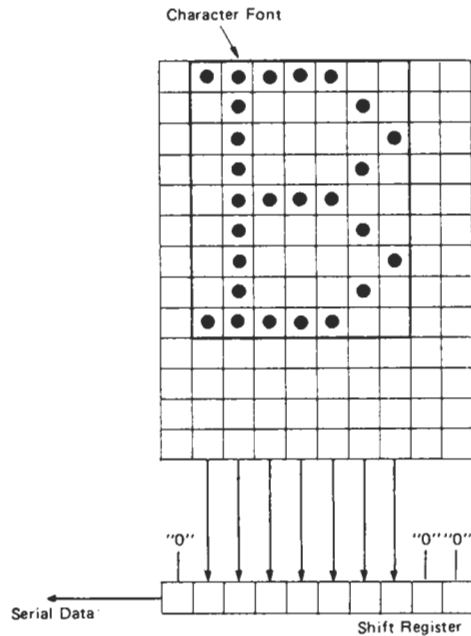


Figure 27 How to Make Character Space

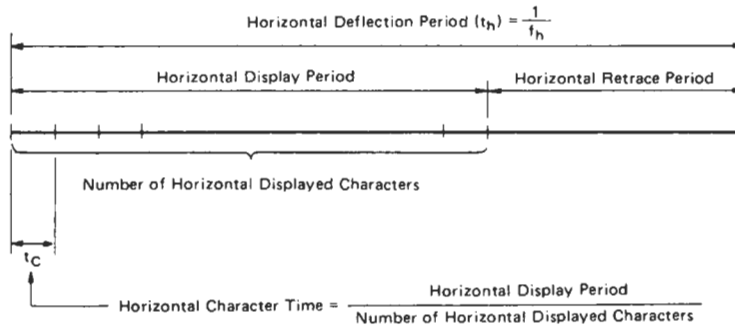


Figure 28 Number of Horizontal Displayed Characters

value of R9, dot number of characters (vertical) is  $(N_r+1)$ .

**Number of Horizontal Displayed Characters**

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

**Number of Vertical Displayed Characters**

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters ( $R_t$ ) including verti-

cal retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster ( $N_{adj}$ ) within specification of vertical deflection frequency.

**Scan Mode**

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 7.



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Table 11 Program of Scan Mode

| 2 <sup>1</sup> | 2 <sup>0</sup> | Scan Mode              | Main Usage   |
|----------------|----------------|------------------------|--|
| 0              | 0              | Non-interlace          | Normal Display of Characters & Figures                                 |
| 1              | 0              |                        |  |
| 0              | 1              | Interlace Sync         | Fine Display of Characters & Figures                                   |
| 1              | 1              | Interlace Sync & Video | Display of Many Characters & Figures Without Using High-resolution CRT |

[NOTE] In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

**Cursor Display Method**

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 8. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

**Start Address**

Start address registers (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

**Cursor Register**

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

■ **EXAMPLES OF APPLIED CIRCUIT OF THE CRTC**

Fig. 30 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table 12. Moreover, specification of CRT display unit is shown in Table 13 and initializing values for the CRTC are shown in Table 14.

Table 12 Specification of Applied Circuit

| Item                            | Specification   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------------------------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Character Format                | 5 × 7 Dot   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Character Space                 | Horizontal : 3 Dot Vertical : 5 Dot   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| One Character Time              | 1 μs  |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Number of Displayed Characters  | 40 characters × 16 lines = 640 characters   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Access Method to Refresh Memory | Synchronous Method (DISPTMG Read)   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Refresh Memory                  | 1 kB  |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Address Map                     | <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th>2<sup>15</sup></th> <th>2<sup>14</sup></th> <th>2<sup>13</sup></th> <th>2<sup>12</sup></th> <th>2<sup>11</sup></th> <th>2<sup>10</sup></th> <th>2<sup>9</sup></th> <th>2<sup>8</sup></th> <th>2<sup>7</sup></th> <th>2<sup>6</sup></th> <th>2<sup>5</sup></th> <th>2<sup>4</sup></th> <th>2<sup>3</sup></th> <th>2<sup>2</sup></th> <th>2<sup>1</sup></th> <th>2<sup>0</sup></th> </tr> </thead> <tbody> <tr> <td>Refresh Memory</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td><td>*</td> </tr> <tr> <td>CRTC Address Register</td> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td> </tr> <tr> <td>CRTC Control Register</td> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td> </tr> </tbody> </table> |                 | 2 <sup>15</sup> | 2 <sup>14</sup> | 2 <sup>13</sup> | 2 <sup>12</sup> | 2 <sup>11</sup> | 2 <sup>10</sup> | 2 <sup>9</sup> | 2 <sup>8</sup> | 2 <sup>7</sup> | 2 <sup>6</sup> | 2 <sup>5</sup> | 2 <sup>4</sup> | 2 <sup>3</sup> | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> | Refresh Memory | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | * | * | * | CRTC Address Register | 0 | 0 | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | 0 | CRTC Control Register | 0 | 0 | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | 1 |
|                                 |   | 2 <sup>15</sup> | 2 <sup>14</sup> | 2 <sup>13</sup> | 2 <sup>12</sup> | 2 <sup>11</sup> | 2 <sup>10</sup> | 2 <sup>9</sup>  | 2 <sup>8</sup> | 2 <sup>7</sup> | 2 <sup>6</sup> | 2 <sup>5</sup> | 2 <sup>4</sup> | 2 <sup>3</sup> | 2 <sup>2</sup> | 2 <sup>1</sup> | 2 <sup>0</sup> |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                                 | Refresh Memory  | 0               | 0               | 0               | 0               | 0               | 0               | *               | *              | *              | *              | *              | *              | *              | *              | *              | *              |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                                 | CRTC Address Register   | 0               | 0               | 0               | 1               | 0               | 0               | x               | x              | x              | x              | x              | x              | x              | x              | x              | 0              |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| CRTC Control Register           | 0   | 0               | 0               | 1               | 0               | 0               | x               | x               | x              | x              | x              | x              | x              | x              | x              | 1              |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|                                 | x . . . don't care, * . . . 0 or 1  |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| Synchronization Method          | HVSYNC Method   |                 |                 |                 |                 |                 |                 |                 |                |                |                |                |                |                |                |                |                |                |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Table 13 Specification of Character Display

| Item  | Specification                        |
|---|--------------------------------------|
| Scan Mode                                   | Non-interlace                        |
| Horizontal Deflection Frequency             | 15.625 kHz                           |
| Vertical Deflection Frequency               | 60.1 Hz                              |
| Dot Frequency                               | 8 MHz                                |
| Character Dot (Horizontal × Vertical)       | 8 × 12 (Character Font 5 × 9)        |
| Number of Displayed Characters (Row × Line) | 40 × 16                              |
| HSYNC Width                                 | 4 μs                                 |
| VSYSNC Width                                | 3 H                                  |
| Cursor Display                              | Raster 9 ~ 10, Blink 16 Field Period |
| Paging, Scrolling                           | Not used                             |

HD6845S, HD68A45S, HD68B45S

Table 14 Initializing Values for Character Display

| Register | Name                     | Symbol        | Initializing Value<br>Hex (Decimal) |
|----------|--------------------------|---------------|-------------------------------------|
| R0       | Horizontal Total         | Nht           | 3F (63)                             |
| R1       | Horizontal Displayed     | Nhd           | 28 (40)                             |
| R2       | Horizontal Sync Position | Nhsp          | 34 (52)                             |
| R3       | Sync Width               | Nvsw, Nhsw    | 34                                  |
| R4       | Vertical Total           | Nvt           | 14 (20)                             |
| R5       | Vertical Total Adjust    | Nadj          | 08 ( 8)                             |
| R6       | Vertical Displayed       | Nvd           | 10 (16)                             |
| R7       | Vertical Sync Position   | Nvsp          | 13 (19)                             |
| R8       | Interlace & Skew         |               | 00                                  |
| R9       | Maximum Raster Address   | Nr            | 0B (11)                             |
| R10      | Cursor Start Raster      | B, P, NCSTART | 49                                  |
| R11      | Cursor End Raster        | NCEND         | 0A (10)                             |
| R12      | Start Address (H)        |               | 00 ( 0)                             |
| R13      | Start Address (L)        |               | 00 ( 0)                             |
| R14      | Cursor (H)               |               | 00 ( 0)                             |
| R15      | Cursor (L)               |               | 00 ( 0)                             |

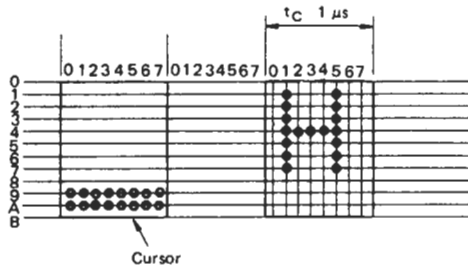


Figure 29 Non-interlace Display (Example)

HD6845S, HD68A45S, HD68B45S

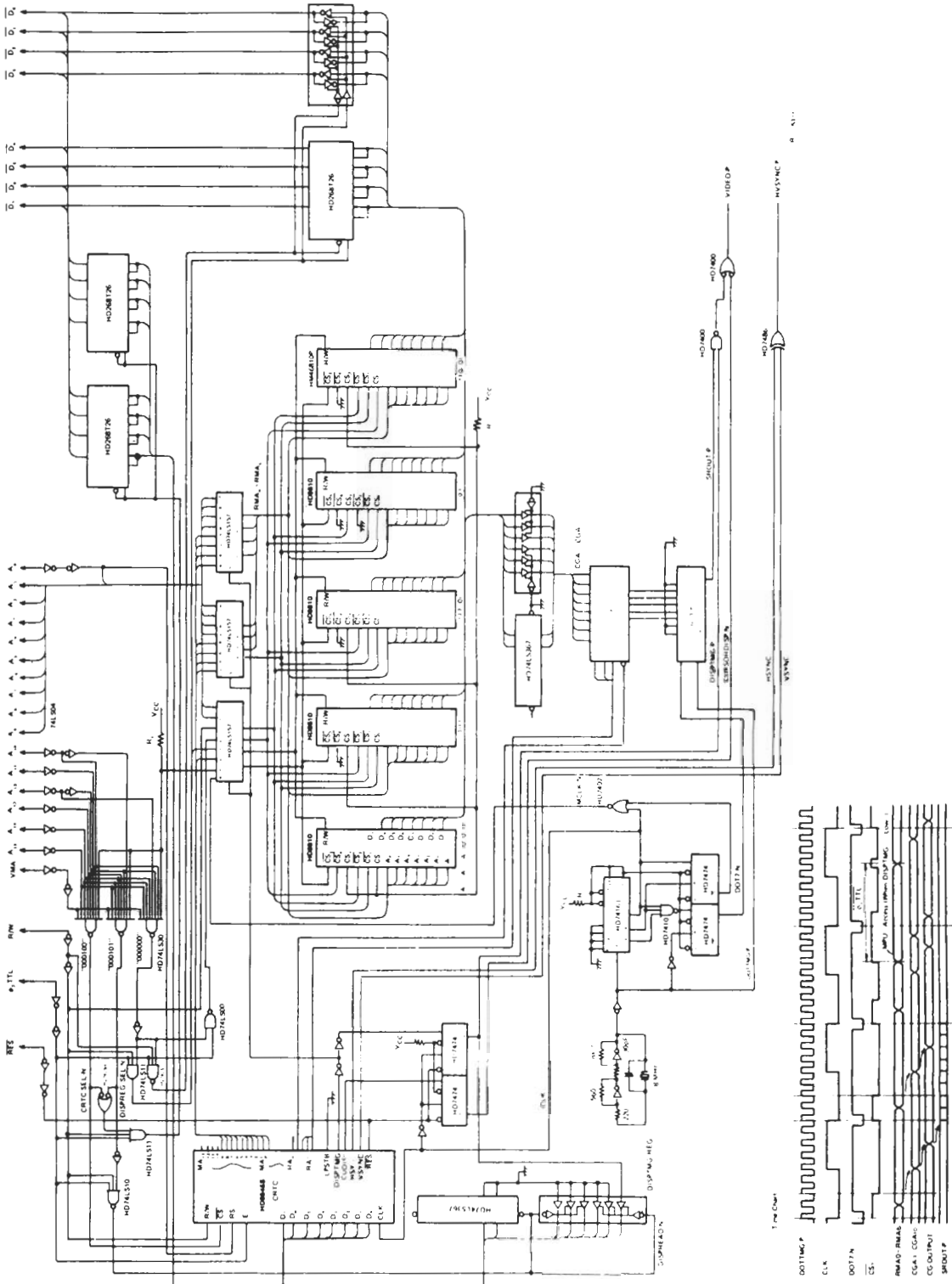
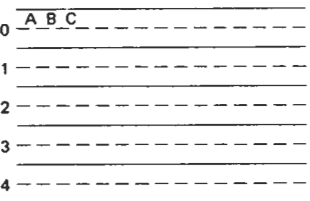
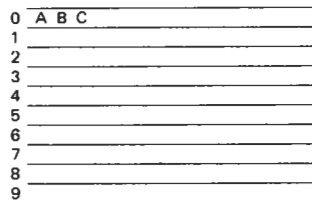
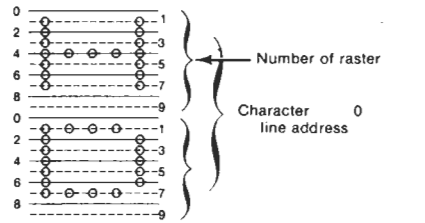
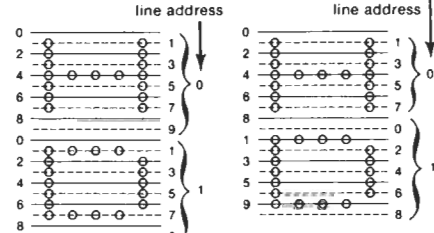
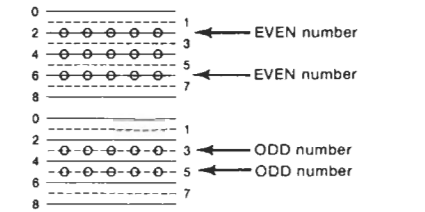
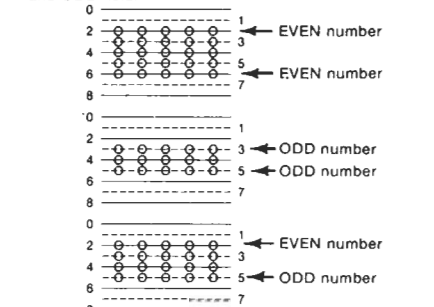


Figure 30 Example of Applied Circuit of the CRTIC (Monochrome Character Display)

HD6845S, HD68A45S, HD68B45S

Differences between the HD6845R (Motorola MC6845 Compatible) and the HD6845S (Enhanced)

| No. | Functional Difference               | HD6845R   | HD6845S  |
|-----|-------------------------------------|---|--|
| 1   | Interface Sync & Video Mode Display | <p>Character line address</p>  <p>Programming unit for number of vertical characters</p> <p>In HD6845R, number of characters is vertically programmed in units of two lines, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position)</p> <p>Example of above figure . . .</p> <p>Programmed number into Vertical Displayed Register = 5</p> | <p>Character line address</p>  <p>Programming unit for number of vertical characters</p> <p>In HD6845S, number of characters is vertically programmed in unit of one line, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position)</p> <p>Example of above figure . . .</p> <p>Programmed number into Vertical Displayed Register = 10</p>  |
|     | Number of raster per character line | <p>Only even number can be specified.</p>  <p>Number of raster</p> <p>Character line address</p> <p>Number of raster = 10 scanline (specified)</p> <p>However, number which is programmed into register is calculated as follows.</p> <p>Programmed number (Nr)</p> $= (\text{Number specified}) - 1$   | <p>Both even number and odd number can be specified.</p>  <p>Character line address</p> <p>Character line address</p> <p>When number of raster per character line is EVEN</p> <p>When number of raster per character line is ODD.</p> <p>Number of raster = 10 scan line (specified)</p> <p>Number of raster = 9 scan line (specified)</p> <p>However, number which is programmed into register is calculated as follows.</p> <p>Programmed number (NR)</p> $= (\text{Number specified}) - 2$ |
|     | Cursor Display                      | <p>Cursor is displayed in either EVEN field or ODD field.</p>  <p>← EVEN number</p> <p>← EVEN number</p> <p>← ODD number</p> <p>← ODD number</p>   | <p>Cursor is displayed in both EVEN field and ODD field.</p>  <p>← EVEN number</p> <p>← EVEN number</p> <p>← ODD number</p> <p>← ODD number</p> <p>← EVEN number</p> <p>← ODD number</p>   |

HD6845S, HD68A45S, HD68B45S

| No. | Functional Difference                    | HD6845R  | HD6845S   |
|-----|--|--|---|
| 2   | Vertical Sync Pulse Width (VSYNC output) | <p>Fixed at 16 raster scan cycle (16H)</p>   | <p>Programmable (1 - 16 raster scan cycle)</p>  |
| 3   | SKEW Function                            | <p>Not included</p>  | <p>SKEW capability is included in DISPTMG, CUDISP signals.</p> <p>Attached byte</p> <p>Example of DISPTMG output</p>  |
| 4   | Start Address Register                   | Write Only   | Read or Write   |
| 5   | RESET Signal (RES)                       | <p>MA<sub>0</sub> ~ MA<sub>13</sub> Output } ----- Synchronous reset<br/> RA<sub>0</sub> ~ RA<sub>4</sub> Output }<br/> Other Outputs ----- Asynchronous reset</p> <p>Output signals of MA<sub>0</sub> ~ MA<sub>13</sub>, RA<sub>0</sub> ~ RA<sub>4</sub>, synchronized with CLK "LOW" level, go to "LOW" level, after RES has gone to "LOW". Other outputs go to "LOW" immediately after RES has gone to "LOW" level.</p> | <p>MA<sub>0</sub> ~ MA<sub>13</sub> Output } ----- Asynchronous reset<br/> RA<sub>0</sub> ~ RA<sub>4</sub> Output }<br/> Other Outputs }<br/> Output signals of MA<sub>0</sub> ~ MA<sub>13</sub>, RA<sub>0</sub> ~ RA<sub>4</sub> and others go to "LOW" level immediately after RES has gone to "LOW" level.</p> |

AC Characteristic Differences between HD6845R (Motorola MC6845 Compatible) and HD6845S (Enhanced)

| No. | Characteristic Difference                      | Symbol                                | HD46505R |      |      | HD46505S |      |      | Unit |
|-----|--|---------------------------------------|----------|------|------|----------|------|------|------|
|     |  |                                       | min.     | typ. | max. | min.     | typ. | max. |      |
| 1   | Clock Cycle Time                               | <i>t<sub>cycc</sub></i>               | 330      | —    | —    | 270      | —    | —    | ns   |
| 2   | Clock Pulse Width "High"                       | <i>PW<sub>CH</sub></i>                | 150      | —    | —    | 130      | —    | —    | ns   |
| 3   | Clock Pulse Width "Low"                        | <i>PW<sub>CL</sub></i>                | 150      | —    | —    | 130      | —    | —    | ns   |
| 4   | Rise and Fall Time for Clock Input             | <i>T<sub>CR</sub>, T<sub>CF</sub></i> | —        | —    | 15   | —        | —    | 20   | ns   |
| 5   | Horizontal Sync Delay Time                     | <i>T<sub>HSD</sub></i>                | —        | —    | 250  | —        | —    | 200  | ns   |
| 6   | Light Pan Strobe Pulse Width                   | <i>PW<sub>LPH</sub></i>               | 80       | —    | —    | 60       | —    | —    | ns   |
| 7   | Light Pan Strobe, Uncertain Time of Acceptance | <i>T<sub>LPD1</sub></i>               | —        | —    | 80   | —        | —    | 70   | ns   |
|     |  | <i>T<sub>LPD2</sub></i>               | —        | —    | 10   | —        | —    | 0    | ns   |

**SCHOTTKY<sup>†</sup>  
PROMS**

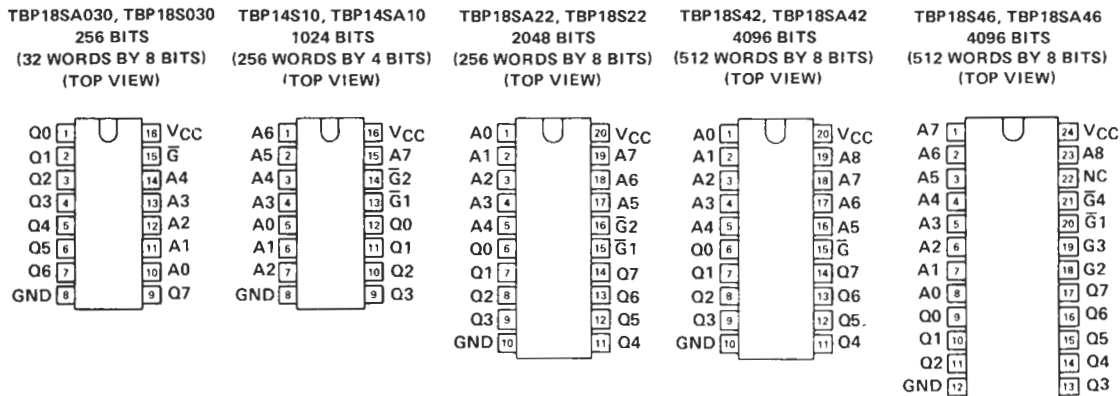
**SERIES 14 AND 18  
PROGRAMMABLE READ-ONLY MEMORIES**

JUNE 1981

- Titanium-Tungsten (Ti-W) Fuse Link For Reliable Low-Voltage Full Family Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs For Reduced Loading On System Buffers/Drivers
- Applications Include:  
Microprogramming/Firmware Loaders  
Code Converters/Character Generators  
Translators/Emulators  
Address Mapping/Look-Up Tables

| NEW TYPE NUMBER                | OLD TYPE NUMBER | BIT SIZE<br>(ORGANIZATION) | OUTPUT<br>CONFIGURATION <sup>†</sup> | TYPICAL PERFORMANCE    |                      |
|--------------------------------|-----------------|----------------------------|--------------------------------------|------------------------|----------------------|
|                                |                 |                            |                                      | ADDRESS<br>ACCESS TIME | POWER<br>DISSIPATION |
| 0°C to 70°C                    | 0°C to 70°C     |                            |                                      |                        |                      |
| TBP18SA030 (J, N) <sup>▲</sup> | SN74S188 (J, N) | 256 Bits<br>(32W X 8B)     | ◇                                    | 25 ns                  | 400 mW               |
| TBP18S030 (J, N) <sup>▲</sup>  | SN74S288 (J, N) |                            | ▽                                    |                        |                      |
| TBP14S10 (J, N) <sup>▲</sup>   | SN74S287 (J, N) | 1024 Bits<br>(256W X 4B)   | ▽                                    | 42 ns                  | 500 mW               |
| TBP14SA10 (J, N) <sup>▲</sup>  | SN74S387 (J, N) |                            | ◇                                    |                        |                      |
| TBP18SA22 (J, N) <sup>▲</sup>  | SN74S470 (J, N) | 2048 Bits<br>(256W X 8B)   | ◇                                    | 50 ns                  | 550 mW               |
| TBP18S22 (J, N) <sup>▲</sup>   | SN74S471 (J, N) |                            | ▽                                    |                        |                      |
| TBP18S42 (J, N) <sup>▲</sup>   | SN74S472 (J, N) | 4096 Bits<br>(512W X 8B)   | ▽                                    | 55 ns                  | 600 mW               |
| TBP18SA42 (J, N) <sup>▲</sup>  | SN74S473 (J, N) |                            | ◇                                    |                        |                      |
| TBP18S46 (J, N) <sup>▲</sup>   | SN74S474 (J, N) | 4096 Bits<br>(512W X 8B)   | ▽                                    | 55 ns                  | 600 mW               |
| TBP18SA46 (J, N) <sup>▲</sup>  | SN74S475 (J, N) |                            | ◇                                    |                        |                      |

<sup>▲</sup> For full temperature parts (-55°C to +125°C) use suffix MJ. For devices with MIL-STD 883B processing (-55°C to +125°C) see page 2-3.  
<sup>†</sup> ◇ = open collector, ▽ = three state.



Pin assignments for all of these memories are the same for the J and N packages. See Product Guide, Section 7, for chip carrier pin assignments.

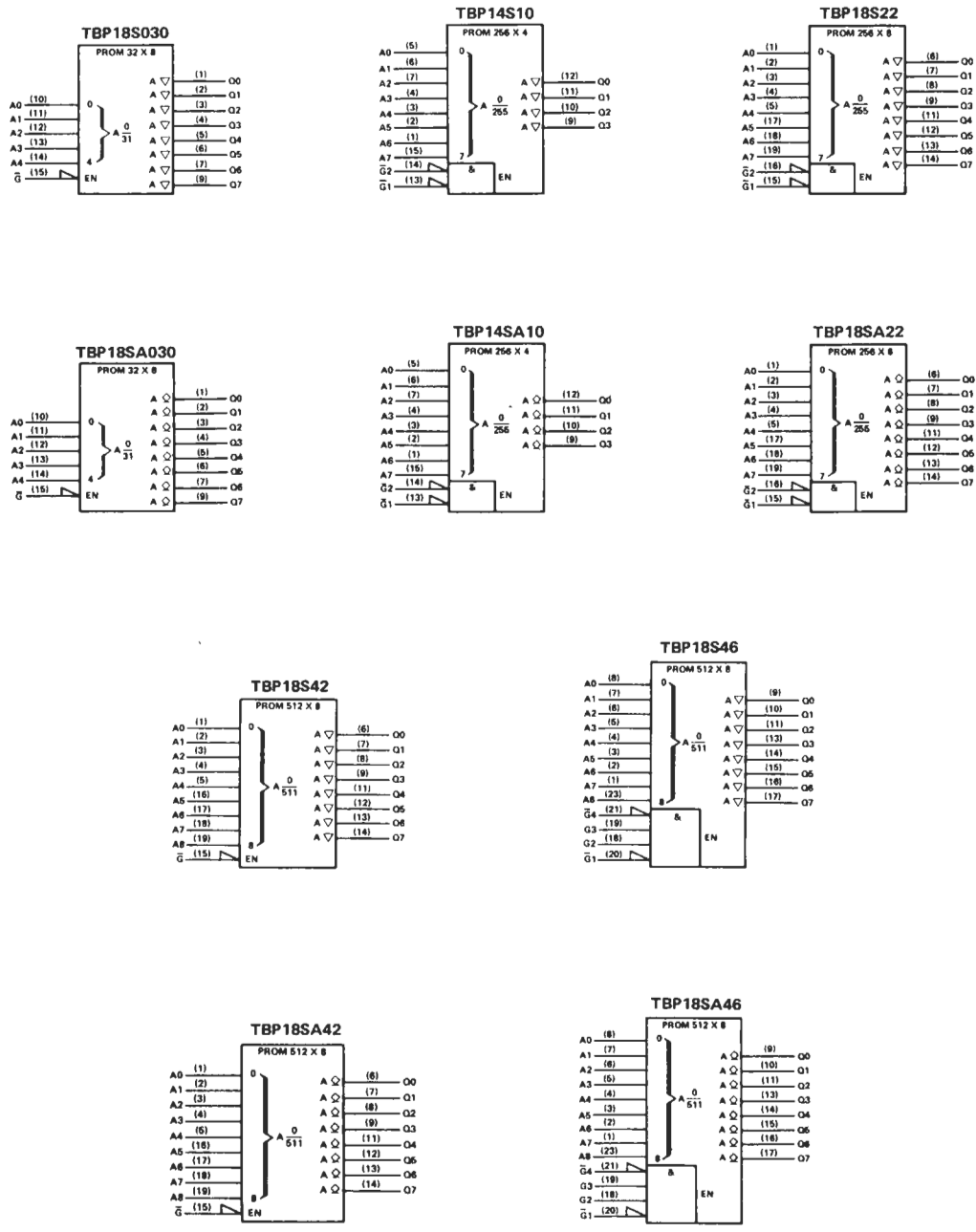
**description**

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 100 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROMs can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch (7,62 mm).

# SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES

logic symbols



## SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES

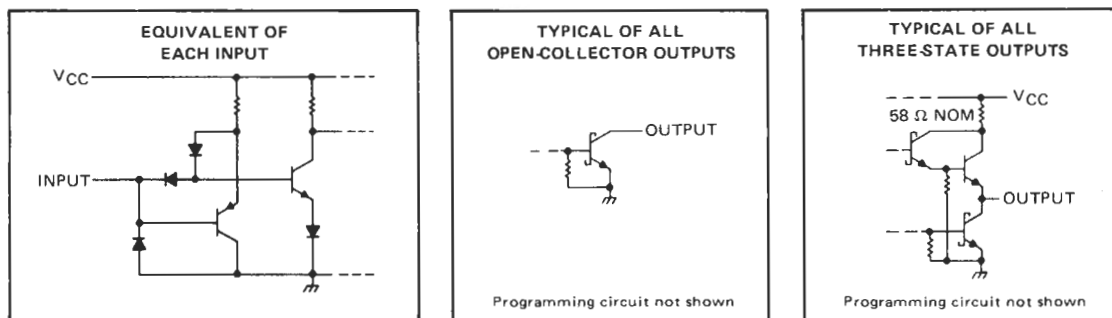
### description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs, except the TBP14S10 and TBP14SA10 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                       |                |
|---------------------------------------|----------------|
| Supply voltage (see Note 1)           | 7V             |
| Input voltage                         | 5.5V           |
| Off-state output voltage              | 5.5V           |
| Operating free-air temperature range: |                |
| Full-temperature-range circuits       | -55°C to 125°C |
| Commercial-temperature-range circuits | 0°C to 70°C    |
| Storage temperature range             | -65°C to 150°C |

### recommended conditions for programming the TBP18S', TBP18SA', TBP14S', and TBP14SA' PROMs

|  |                      | MIN                         | NOM  | MAX  | UNIT    |
|--|----------------------|-----------------------------|------|------|---------|
| Supply voltage, $V_{CC}$ (see Note 1)                                | Steady state         | 4.75                        | 5    | 5.25 | V       |
|  | Program pulse        | 9                           | 9.25 | 9.5  |         |
| Input voltage  | High level, $V_{IH}$ | 2.4                         |      | 5    | V       |
|  | Low level, $V_{IL}$  | 0                           |      | 0.5  |         |
| Termination of all outputs except the one to be programmed           |                      | See load circuit (Figure 1) |      |      |         |
| Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2) |                      | 0                           | 0.25 | 0.3  | V       |
| Duration of $V_{CC}$ programming pulse X (see Figure 2 and Note 3)   |                      | 15                          | 25   | 100  | $\mu$ s |
| Programming duty cycle for Y pulse                                   |                      |                             | 25   | 35   | %       |
| Free-air temperature   |                      | 20                          | 25   | 30   | °C      |

† Absolute maximum ratings.

- NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.  
 2. The TBP18S030, TBP18SA030, TBP18SA22, TBP18S22, TBP18S42, TBP18SA42, TBP18S46 and TBP18SA46 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The TBP14S10, TBP14SA10 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.  
 3. Programming is guaranteed if the pulse applied as 98  $\mu$ s in duration.





## SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES WITH 3-STATE OUTPUTS

### recommended operating conditions

| PARAMETER                             |      | TBP14S10, TBP18S22 |     |      | TBP18S030 |     |      | TBP18S42, TBP18S46 |     |      | UNIT |
|---------------------------------------|------|--------------------|-----|------|-----------|-----|------|--------------------|-----|------|------|
|                                       |      | MIN                | NOM | MAX  | MIN       | NOM | MAX  | MIN                | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | MJ   | 4.5                | 5   | 5.5  | 4.5       | 5   | 5.5  | 4.5                | 5   | 5.5  | V    |
|                                       | J, N | 4.75               | 5   | 5.25 | 4.75      | 5   | 5.25 | 4.75               | 5   | 5.25 |      |
| High-level output current, $I_{OH}$   | MJ   |                    |     | -2   |           |     | -2   |                    |     | -2   | mA   |
|                                       | J, N |                    |     | -6.5 |           |     | -6.5 |                    |     | -6.5 |      |
| Low-level output current, $I_{OL}$    |      |                    |     | 16   |           |     | 20   |                    |     | 12   | mA   |
| Operating free-air temperature, $T_A$ | MJ   | -55                |     | 125  | -55       |     | 125  | -55                |     | 125  | °C   |
|                                       | J, N | 0                  |     | 70   | 0         |     | 70   | 0                  |     | 70   |      |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS†   | FULL TEMP<br>(MJ)  |      |     | COMM. TEMP<br>(J, N) |      |      | UNIT               |    |
|--|--|--------------------|------|-----|----------------------|------|------|--------------------|----|
|  |  | MIN                | TYP‡ | MAX | MIN                  | TYP‡ | MAX  |                    |    |
| $V_{IH}$ High-level input voltage                              |  |                    | 2    |     |                      | 2    |      | V                  |    |
| $V_{IL}$ Low-level input voltage                               |  |                    |      |     |                      | 0.8  |      | 0.8 V              |    |
| $V_{IK}$ Input clamp voltage                                   | $V_{CC} = \text{MIN}$ ,<br>$I_I = -18 \text{ mA}$                                |                    |      |     |                      | -1.2 |      | -1.2 V             |    |
| $V_{OH}$ High-level output voltage                             | $V_{CC} = \text{MIN}$ ,<br>$V_{IL} = 0.8 \text{ V}$ ,<br>$I_{OH} = \text{MAX}$   |                    | 2.4  | 3.4 |                      | 2.4  | 3.2  | V                  |    |
| $V_{OL}$ Low-level output voltage                              | $V_{CC} = \text{MIN}$ ,<br>$V_{IL} = 0.8 \text{ V}$ ,<br>$I_{OL} = \text{MAX}$   |                    |      |     |                      | 0.5  |      | 0.5 V              |    |
| $I_{OZH}$ Off-state output current, high-level voltage applied | $V_{CC} = \text{MAX}$ ,<br>$V_{IH} = 2 \text{ V}$ ,<br>$V_O = 2.4 \text{ V}$     |                    |      |     |                      | 50   |      | 50 $\mu\text{A}$   |    |
| $I_{OZL}$ Off-state output current, low-level voltage applied  | $V_{CC} = \text{MAX}$ ,<br>$V_{IH} = 2 \text{ V}$ ,<br>$V_O = 0.5 \text{ V}$     |                    |      |     |                      | -50  |      | -50 $\mu\text{A}$  |    |
| $I_I$ Input current at maximum input voltage                   | $V_{CC} = \text{MAX}$ ,<br>$V_I = 5.5 \text{ V}$                                 |                    |      |     |                      | 1    |      | 1 mA               |    |
| $I_{IH}$ High-level input current                              | $V_{CC} = \text{MAX}$ ,<br>$V_I = 2.7 \text{ V}$                                 |                    |      |     |                      | 25   |      | 25 $\mu\text{A}$   |    |
| $I_{IL}$ Low-level input current                               | $V_{CC} = \text{MAX}$ ,<br>$V_I = 0.5 \text{ V}$                                 |                    |      |     |                      | -250 |      | -250 $\mu\text{A}$ |    |
| $I_{OS}$ Short-circuit output current§                         | $V_{CC} = \text{MAX}$  |                    |      |     |                      | -30  | -100 | -30 -100 mA        |    |
| $I_{CC}$ Supply current  | $V_{CC} = \text{MAX}$ ,<br>Chip select(s) at 0 V,<br>Outputs open,<br>See Note 4 | TBP14S10           |      | 100 | 135                  |      | 100  | 135                | mA |
|  |  | TBP18S030          |      | 80  | 110                  |      | 80   | 110                |    |
|  |  | TBP18S22           |      | 110 | 155                  |      | 110  | 155                |    |
|  |  | TBP18S42, TBP18S46 |      | 120 | 155                  |      | 120  | 155                |    |

### switching characteristics over recommended ranges of $T_A$ and $V_{CC}$ (unless otherwise noted)

| TYPE                   | TEST CONDITIONS   | $t_a(A)$ (ns)<br>Access time from address |      |     | $t_a(S)$ (ns)<br>Access time from chip select (enable time) |      |     | $t_{pXZ}$ (ns)<br>Disable time from high or low level |      |     | UNIT |
|------------------------|---|---|------|-----|---|------|-----|---|------|-----|------|
|                        |   | MIN                                       | TYP‡ | MAX | MIN   | TYP‡ | MAX | MIN   | TYP‡ | MAX |      |
| TBP14S10MJ             | $C_L = 30 \text{ pF}$ for<br>$t_a(A)$ and $t_a(S)$ ,<br>5 pF for $t_{pXZ}$ ,<br>See Page 1-12 |   | 42   | 75  |   | 15   | 40  |   | 12   | 40  | ns   |
| TBP14S10               |   |   | 42   | 65  |   | 15   | 35  |   | 12   | 35  | ns   |
| TBP18S030MJ            |   |   | 25   | 50  |   | 12   | 30  |   | 8    | 30  | ns   |
| TBP18S030              |   |   | 25   | 40  |   | 12   | 25  |   | 8    | 20  | ns   |
| TBP18S22MJ             |   |   | 50   | 80  |   | 20   | 40  |   | 15   | 35  | ns   |
| TBP18S22               |   |   | 50   | 70  |   | 20   | 35  |   | 15   | 30  | ns   |
| TBP18S42MJ, TBP18S46MJ |   |   | 55   | 85  |   | 20   | 45  |   | 15   | 40  | ns   |
| TBP18S42, TBP18S46     |   |   | 55   | 75  |   | 20   | 40  |   | 15   | 35  | ns   |

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 4: The typical values of  $I_{CC}$  are with all outputs low.

## SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

### recommended operating conditions

| PARAMETER                             |      | TBP14SA10, TBP18SA22 |     |      | TBP18SA030 |     |      | TBP18SA42, TBP18SA46 |     |      | UNIT |
|---------------------------------------|------|----------------------|-----|------|------------|-----|------|----------------------|-----|------|------|
|                                       |      | MIN                  | NOM | MAX  | MIN        | NOM | MAX  | MIN                  | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | MJ   | 4.5                  | 5   | 5.5  | 4.5        | 5   | 5.5  | 4.5                  | 5   | 5.5  | V    |
|                                       | J, N | 4.75                 | 5   | 5.25 | 4.75       | 5   | 5.25 | 4.75                 | 5   | 5.25 |      |
| High-level output voltage, $V_{OH}$   |      |                      |     | 5.5  |            |     | 5.5  |                      |     | 5.5  | V    |
| Low-level output current, $I_{OL}$    |      |                      |     | 16   |            |     | 20   |                      |     | 16   | mA   |
| Operating free-air temperature, $T_A$ | MJ   | -55                  |     | 125  | -55        |     | 125  | -55                  |     | 125  | °C   |
|                                       | J, N | 0                    |     | 70   | 0          |     | 70   | 0                    |     | 70   |      |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS†   | MIN                      | TYP† | MAX | UNIT |     |     |    |
|--|--|--------------------------|------|-----|------|-----|-----|----|
| $V_{IH}$ High-level input voltage            |  | 2                        |      |     | V    |     |     |    |
| $V_{IL}$ Low-level input voltage             |  | 0.8                      |      |     | V    |     |     |    |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}$ ,<br>$I_I = -18 \text{ mA}$                                | -1.2                     |      |     | V    |     |     |    |
| $I_{OH}$ High-level output current           | $V_{CC} = \text{MIN}$ ,<br>$V_{IH} = 2 \text{ V}$ ,<br>$V_{IL} = 0.8 \text{ V}$  | $V_{OH} = 2.4 \text{ V}$ |      |     | 50   |     |     |    |
|  |  | $V_{OH} = 5.5 \text{ V}$ |      |     | 100  |     |     |    |
| $V_{OL}$ Low-level output voltage            | $V_{CC} = \text{MIN}$ ,<br>$V_{IL} = 0.8 \text{ V}$ ,<br>$I_{OL} = \text{MAX}$   | 0.5                      |      |     | V    |     |     |    |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}$ ,<br>$V_I = 5.5 \text{ V}$                                 | 1                        |      |     | mA   |     |     |    |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}$ ,<br>$V_I = 2.7 \text{ V}$                                 | 25                       |      |     | μA   |     |     |    |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}$ ,<br>$V_I = 0.5 \text{ V}$                                 | -250                     |      |     | μA   |     |     |    |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX}$ ,<br>Chip select(s) at 0 V,<br>Outputs open,<br>See Note 4 | TBP18SA030               |      |     | 80   |     |     |    |
|  |  | TBP14SA10                |      |     | 100  |     |     |    |
|  |  | TBP18SA22                |      |     | 110  |     |     |    |
|  |  | TBP18SA42, TBP18SA46     |      |     | 120  |     |     |    |
|  |  |                          |      | 110 | 155  | 120 | 155 | mA |

### switching characteristics over recommended ranges of $T_A$ and $V_{CC}$ (unless otherwise noted)

| TYPE                     | TEST CONDITIONS  | $t_a(\text{A})$<br>Access time from address |      |     | $t_a(\text{S})$<br>Access time from chip select (enable time) |      |     | $t_{PLH}$<br>Propagation delay time, low-to-high-level output from chip select (disable time) |      |     | UNIT |
|--------------------------|--|---|------|-----|---|------|-----|---|------|-----|------|
|                          |  | MIN   | TYP† | MAX | MIN   | TYP† | MAX | MIN   | TYP† | MAX |      |
| TBP18SA030MJ             | $C_L = 30 \text{ pF}$ ,<br>$R_{L1} = 300 \Omega$ ,<br>$R_{L2} = 600 \Omega$ ,<br>See Page 1-12 | 25  | 50   |     | 12  | 30   |     | 12  | 30   | ns  |      |
| TBP18SA030               |  | 25  | 40   |     | 12  | 25   |     | 12  | 25   | ns  |      |
| TBP14SA10MJ              |  | 42  | 75   |     | 15  | 40   |     | 15  | 40   | ns  |      |
| TBP14SA10                |  | 42  | 65   |     | 15  | 35   |     | 15  | 35   | ns  |      |
| TBP18SA22MJ              |  | 50  | 80   |     | 20  | 40   |     | 15  | 35   | ns  |      |
| TBP18SA22                |  | 50  | 70   |     | 20  | 35   |     | 15  | 30   | ns  |      |
| TBP18SA42MJ, TBP18SA46MJ |  | 55  | 85   |     | 20  | 45   |     | 15  | 40   | ns  |      |
| TBP18SA42, TBP18SA46     |  | 55  | 75   |     | 20  | 40   |     | 15  | 35   | ns  |      |

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

NOTE 4: The typical values of  $I_{CC}$  are with all output low.

**SCHOTTKY<sup>†</sup>**  
**PROMS**
**SERIES 24 AND 28**  
**STANDARD, LOW-POWER, POWER-DOWN, REGISTERED**  
**PROGRAMMABLE READ-ONLY MEMORIES**

JUNE 1981

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  - Microprogramming/Firm Ware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

## STANDARD PROMS

| TYPE NUMBER                    |                  | OUTPUT CONFIGURATION <sup>‡</sup> | BIT SIZE (ORGANIZATION)     | TYPICAL PERFORMANCE |        |                   |
|--------------------------------|------------------|-----------------------------------|-----------------------------|---------------------|--------|-------------------|
| NEW TYPE NUMBER                | OLD TYPE NUMBER  |                                   |                             | ACCESS TIMES        |        | POWER DISSIPATION |
|                                |                  |                                   |                             | ADDRESS             | SELECT |                   |
| TBP24S10 (J, N) <sup>▲</sup>   |                  | ▽                                 | 1024 Bits<br>(256W X 4B)    | 35 ns               | 20 ns  | 375 mW            |
| TBP24SA10 (J, N) <sup>▲</sup>  |                  | ◇                                 |                             |                     |        |                   |
| TBP28S42 (J, N) <sup>▲</sup>   |                  | ▽                                 | 4096 Bits<br>(512W X 8B)    | 35 ns               | 20 ns  | 500 mW            |
| TBP28SA42                      |                  | ◇                                 |                             |                     |        |                   |
| TBP28S45 (J, N) † <sup>▲</sup> |                  | ▽                                 |                             |                     |        |                   |
| TBP28S46                       |                  | ▽                                 |                             |                     |        |                   |
| TBP28SA46                      |                  | ◇                                 |                             |                     |        |                   |
| TBP24S41 (J, N) <sup>▲</sup>   | SN74S476 (J, N)  | ▽                                 |                             |                     |        |                   |
| TBP24SA41 (J, N) <sup>▲</sup>  | SN74S477 (J, N)  | ◇                                 | 4096 Bits<br>(1024W X 4B)   | 40 ns               | 20 ns  | 475 mW            |
| TBP24S81 (J, N) <sup>▲</sup>   | SN74S454 (J, N)  | ▽                                 | 8192 Bits<br>(2048W X 4B)   | 45 ns               | 20 ns  | 625 mW            |
| TBP24SA81 (J, N) <sup>▲</sup>  | SN74S455 (J, N)  | ◇                                 |                             |                     |        |                   |
| TBP28S86 (J, N) <sup>▲</sup>   | SN74S478 (J, N)  | ▽                                 | 8192 Bits<br>(1024W X 8B)   | 45 ns               | 20 ns  | 625 mW            |
| TBP28SA86 (J, N) <sup>▲</sup>  | SN74S479 (J, N)  | ◇                                 |                             |                     |        |                   |
| TBP28S2708 (J, N)              | SN74S2708 (J, N) | ▽                                 |                             |                     |        |                   |
| TBP28S85 (J, N) † <sup>▲</sup> |                  | ▽                                 |                             |                     |        |                   |
| TBP28S166 (J, N) <sup>▲</sup>  |                  | ▽                                 | 16,384 Bits<br>(2048W X 8B) | 35 ns               | 15 ns  | 650 mW            |
| TBP28SA166                     |                  | ◇                                 |                             |                     |        |                   |

## LOW POWER PROMS

| TYPE NUMBER                     |                  | OUTPUT CONFIGURATION <sup>‡</sup> | BIT SIZE (ORGANIZATION)     | TYPICAL PERFORMANCE |        |                   |
|---------------------------------|------------------|-----------------------------------|-----------------------------|---------------------|--------|-------------------|
| NEW TYPE NUMBER                 | OLD TYPE NUMBER  |                                   |                             | ACCESS TIMES        |        | POWER DISSIPATION |
|                                 |                  |                                   |                             | ADDRESS             | SELECT |                   |
| TBP28L22 (J, N) <sup>▲</sup>    |                  | ▽                                 | 2048 Bits<br>(256W X 8B)    | 45 ns               | 20 ns  | 375 mW            |
| TBP28LA22                       |                  | ◇                                 |                             |                     |        |                   |
| TBP28L42 (J, N) <sup>▲</sup>    |                  | ▽                                 | 4096 Bits<br>(512W X 8B)    | 60 ns               | 30 ns  | 250 mW            |
| TBP28L45 (J, N) † <sup>▲</sup>  |                  | ▽                                 |                             |                     |        |                   |
| TBP28L46 (J, N) <sup>▲</sup>    |                  | ▽                                 |                             |                     |        |                   |
| TBP28L86 (J, N) <sup>▲</sup>    | SN74LS478 (J, N) | ▽                                 | 8192 Bits<br>(1024W X 8B)   | 80 ns               | 35 ns  | 350 mW            |
| TBP28L85 (J, N) † <sup>▲</sup>  |                  | ▽                                 |                             | 65 ns               | 30 ns  | 275 mW            |
| TBP28L166 (J, N) † <sup>▲</sup> |                  | ▽                                 | 16,384 Bits<br>(2048W X 8B) | 65 ns               | 30 ns  | 350 mW            |

All PROMs are also available in chip carriers.

† NOTE — Electrical parameters for these devices are design goals only.

▲ NOTE — These devices available as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ).

‡ ◇ = open collector, ▽ - three state.

## **Floppy Disk Controller Board (Z-207)**

# WESTERN DIGITAL

C O R P O R A T I O N

## FD179X-02 FLOPPY DISK FORMATTER/CONTROLLER FAMILY

### FEATURES

- TWO VFO CONTROL SIGNALS — RG & VFOE
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
  - Non IBM Format for Increased Capacity
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128, 256, 512 or 1024 Byte Sector Lengths
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information

- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

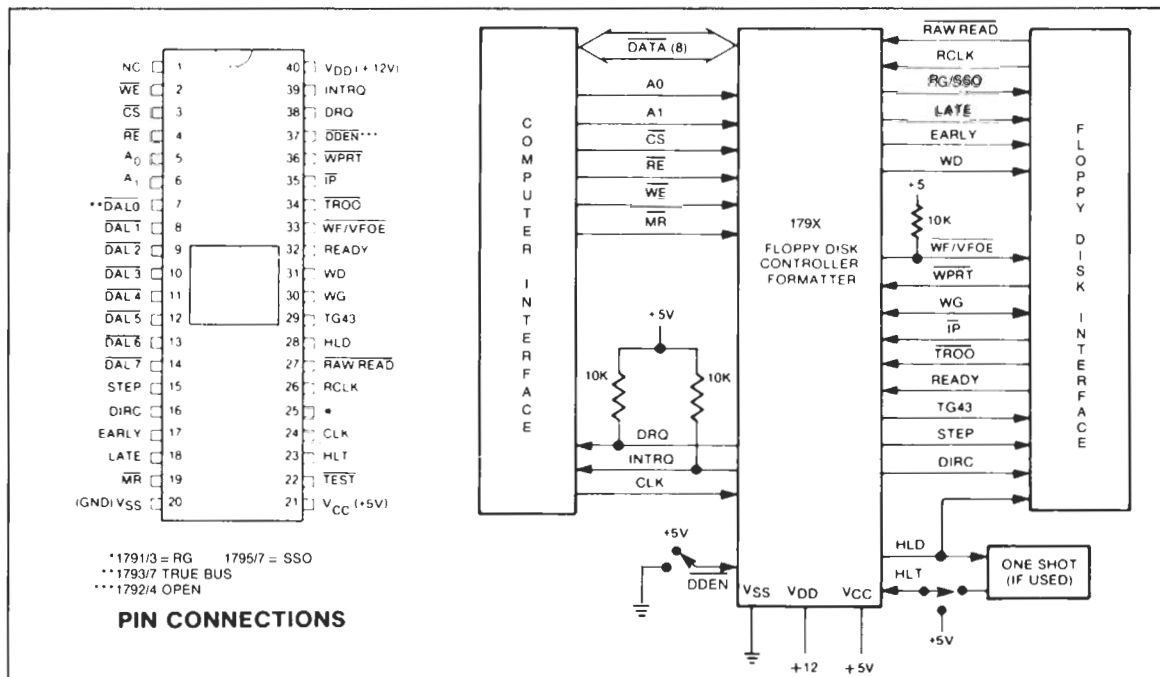
AUGUST, 1981

### 179X-02 FAMILY CHARACTERISTICS

| FEATURES              | 1791 | 1792 | 1793 | 1794 | 1795 | 1797 |
|-----------------------|------|------|------|------|------|------|
| Single Density (FM)   | X    | X    | X    | X    | X    | X    |
| Double Density (MFM)  | X    |      | X    |      | X    | X    |
| True Data Bus         |      |      | X    | X    |      | X    |
| Inverted Data Bus     | X    | X    |      |      | X    |      |
| Write Precomp         | X    | X    | X    | X    | X    | X    |
| Side Selection Output |      |      |      |      | X    | X    |

### APPLICATIONS

8" FLOPPY AND 5 1/4" MINI FLOPPY CONTROLLER  
SINGLE OR DOUBLE DENSITY  
CONTROLLER/FORMATTER



FD179X SYSTEM BLOCK DIAGRAM

## PIN OUTS

| PIN NUMBER                    | PIN NAME              | SYMBOL          | FUNCTION  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
|-------------------------------|-----------------------|-----------------|---|-----------------|----|----|-----------------|-----------------|---|---|---|------------|-------------|---|---|---|-----------|-----------|---|---|---|------------|------------|---|---|---|----------|----------|
| 1                             | NO CONNECTION         | NC              | Pin 1 is internally connected to a back bias generator and must be left open by the user.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 19                            | MASTER RESET          | $\overline{MR}$ | A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 20                            | POWER SUPPLIES        | V <sub>ss</sub> | Ground  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 21                            |                       | V <sub>cc</sub> | +5V $\pm$ 5%  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 40                            |                       | V <sub>DD</sub> | +12V $\pm$ 5%   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| <b>COMPUTER INTERFACE:</b>    |                       |                 |   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 2                             | WRITE ENABLE          | $\overline{WE}$ | A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 3                             | CHIP SELECT           | $\overline{CS}$ | A logic low on this input selects the chip and enables computer communication with the device.  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 4                             | READ ENABLE           | $\overline{RE}$ | A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 5,6                           | REGISTER SELECT LINES | A0, A1          | These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:<br><table border="1" style="margin-left: 20px;"> <thead> <tr> <th><math>\overline{CS}</math></th> <th>A1</th> <th>A0</th> <th><math>\overline{RE}</math></th> <th><math>\overline{WE}</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Status Reg</td> <td>Command Reg</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Track Reg</td> <td>Track Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Sector Reg</td> <td>Sector Reg</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Data Reg</td> <td>Data Reg</td> </tr> </tbody> </table> | $\overline{CS}$ | A1 | A0 | $\overline{RE}$ | $\overline{WE}$ | 0 | 0 | 0 | Status Reg | Command Reg | 0 | 0 | 1 | Track Reg | Track Reg | 0 | 1 | 0 | Sector Reg | Sector Reg | 0 | 1 | 1 | Data Reg | Data Reg |
| $\overline{CS}$               | A1                    | A0              | $\overline{RE}$   | $\overline{WE}$ |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 0                             | 0                     | 0               | Status Reg  | Command Reg     |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 0                             | 0                     | 1               | Track Reg   | Track Reg       |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 0                             | 1                     | 0               | Sector Reg  | Sector Reg      |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 0                             | 1                     | 1               | Data Reg  | Data Reg        |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 7-14                          | DATA ACCESS LINES     | DAL0-DAL7       | Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$ . Each line will drive 1 standard TTL load.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 24                            | CLOCK                 | CLK             | This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz $\pm$ 1% for 8" drives, 1 MHz $\pm$ 1% for mini-floppies.  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 38                            | DATA REQUEST          | DRQ             | This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.  |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 39                            | INTERRUPT REQUEST     | INTRQ           | This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| <b>FLOPPY DISK INTERFACE:</b> |                       |                 |   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 15                            | STEP                  | STEP            | The step output contains a pulse for each step.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 16                            | DIRECTION             | DIRC            | Direction Output is active high when stepping in, active low when stepping out.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 17                            | EARLY                 | EARLY           | Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |
| 18                            | LATE                  | LATE            | Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.   |                 |    |    |                 |                 |   |   |   |            |             |   |   |   |           |           |   |   |   |            |            |   |   |   |          |          |

| PIN NUMBER | PIN NAME                              | SYMBOL   | FUNCTION  |
|------------|---------------------------------------|----------|---|
| 22         | TEST                                  | TEST     | This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated steppers.   |
| 23         | HEAD LOAD TIMING                      | HLT      | When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.  |
| 25         | READ GATE<br>(1791, 1792, 1793, 1794) | RG       | This output is used for synchronization of external data separators. The output goes high after two Bytes of zeros in single density, or 4 Bytes of either zeros or ones in double density operation.   |
| 25         | SIDE SELECT OUTPUT<br>(1795, 1797)    | SSO      | The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.  |
| 26         | READ CLOCK                            | RCLK     | A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.   |
| 27         | RAW READ                              | RAW READ | The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.  |
| 28         | HEAD LOAD                             | HLD      | The HLD output controls the loading of the Read-Write head against the media.   |
| 29         | TRACK GREATER THAN 43                 | TG43     | This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.  |
| 30         | WRITE GATE                            | WG       | This output is made valid before writing is to be performed on the diskette.  |
| 31         | WRITE DATA                            | WD       | A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.  |
| 32         | READY                                 | READY    | This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.   |
| 33         | WRITE FAULT<br>VFO ENABLE             | WF/VFOE  | This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100K Ohm pull-up resistor. |
| 34         | TRACK 00                              | TR00     | This input informs the FD179X that the Read/Write head is positioned over Track 00.   |



| PIN NUMBER | PIN NAME       | SYMBOL            | FUNCTION   |
|------------|----------------|-------------------|--|
| 35         | INDEX PULSE    | $\overline{IP}$   | This input informs the FD179X when the index hole is encountered on the diskette.  |
| 36         | WRITE PROTECT  | $\overline{WPRT}$ | This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.  |
| 37         | DOUBLE DENSITY | $\overline{DDEN}$ | This input pin selects either single or double density operation. When $\overline{DDEN} = 0$ , double density is selected. When $\overline{DDEN} = 1$ , single density is selected. This line must be left open on the 1792/4. |

### GENERAL DESCRIPTION

The FD179X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is TTL compatible on all inputs and outputs. The outputs will drive ONE TTL load or three LS loads. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793 respectively. On these devices, DDEN must be left open.

### ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include, the parallel processor interface and the Floppy Disk interface.

**Data Shift Register** — This 8-bit register assembles serial data from the Read Data input ( $\overline{RAW READ}$ ) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register** — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Track Register** — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

**Sector Register (SR)** — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)** — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)** — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

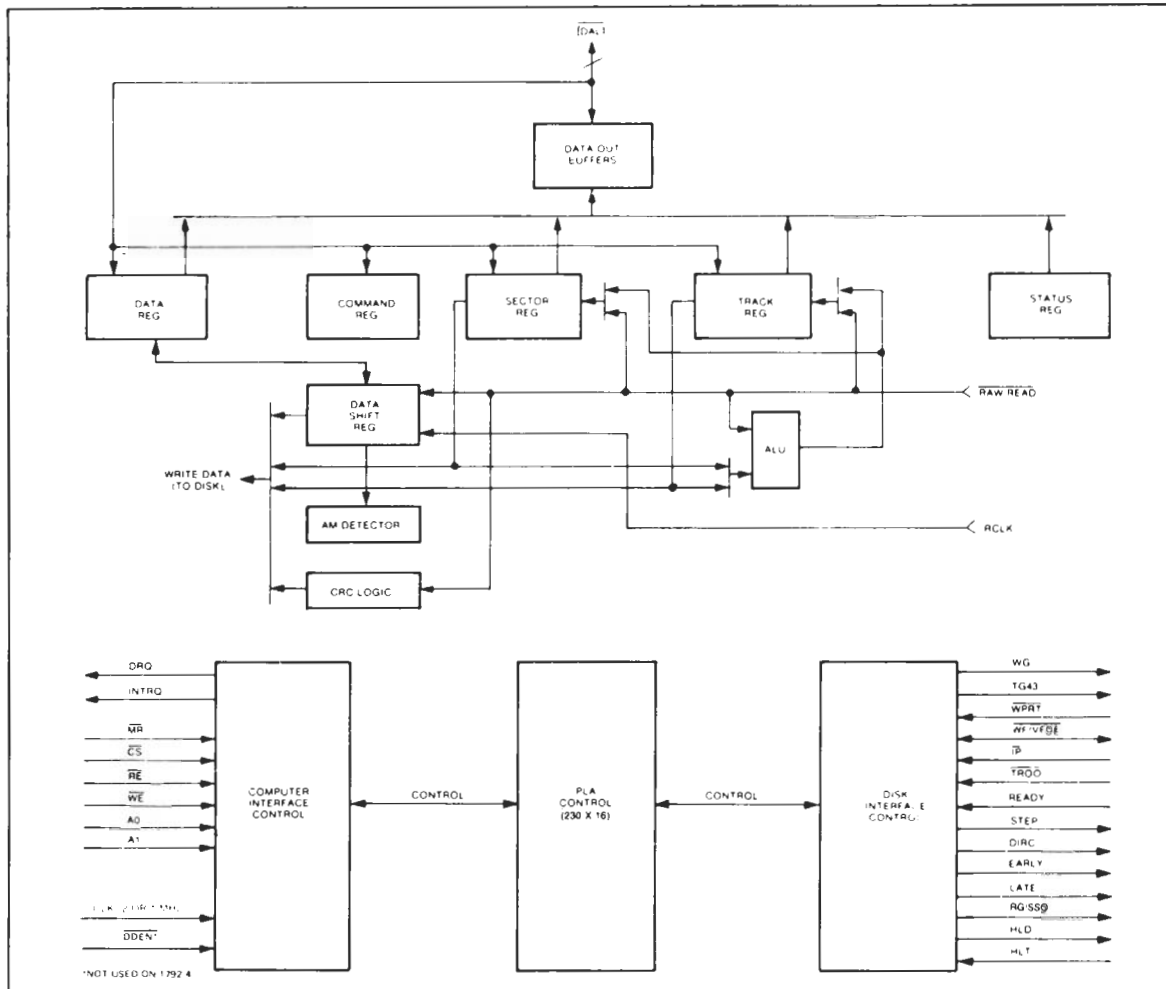
**CRC Logic** — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:  $G(x) = x^{16} + x^{12} + x^5 + 1$ .

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** — The ALU is a serial comparator, incrementer, and decremter and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD179X has two different modes of operation according to the state of DDEN. When  $\overline{DDEN} = 0$  double density (MFM) is assumed. When  $\overline{DDEN} = 1$ , single



FD179X BLOCK DIAGRAM

density (FM) is assumed. 1792 & 1794 are single density only.

**AM Detector** — The address mark detector detects ID, data and index address marks during read and write operations.

**PROCESSOR INTERFACE**

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD179X. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

| A1 - A0 | READ (RE)       | WRITE (WE)       |
|---------|-----------------|------------------|
| 0 0     | Status Register | Command Register |
| 0 1     | Track Register  | Track Register   |
| 1 0     | Sector Register | Sector Register  |
| 1 1     | Data Register   | Data Register    |

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data

Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 179X has two modes of operation according to the state of DDEN (Pin 37). When DDEN = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density.

#### GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical "1." For MFM formats, DDEN should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
|---------------------------|-------------------------------------|
| 00                        | 128                                 |
| 01                        | 256                                 |
| 02                        | 512                                 |
| 03                        | 1024                                |

\*1795/97 may vary — see command summary.

The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table)

For read operations in 8" double density the FD179X requires RAW READ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1791/92/93/94 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the VFOE (Pin 33) is provided for phase lock loop synchronization. VFOE will go active low when:

- Both HLT and HLD are True
- Settling Time, if programmed, has expired
- The 179X is inspecting data off the disk

If WF/VFOE is not used, leave open or tie to a 10K resistor to +5.

#### GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM (DDEN = 1) and 200 ns pulses in MFM (DDEN = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

#### READY

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

#### COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**TABLE 1. COMMAND SUMMARY**

| A. Commands for Models: 1791, 1792, 1793, 1794 |                 |   |   |   |      |    |    |    | B. Commands for Models: 1795, 1797 |   |   |      |   |    |    |    |    |
|--|-----------------|---|---|---|------|----|----|----|------------------------------------|---|---|------|---|----|----|----|----|
| Type   | Command         | 7 | 6 | 5 | Bits |    |    |    | 7                                  | 6 | 5 | Bits |   |    |    |    |    |
|  |                 |   |   |   | 4    | 3  | 2  | 1  | 0                                  |   |   |      | 4 | 3  | 2  | 1  | 0  |
| I  | Restore         | 0 | 0 | 0 | 0    | h  | V  | r1 | r0                                 | 0 | 0 | 0    | 0 | h  | V  | r1 | r0 |
| I  | Seek            | 0 | 0 | 0 | 1    | h  | V  | r1 | r0                                 | 0 | 0 | 0    | 1 | h  | V  | r1 | r0 |
| I  | Step            | 0 | 0 | 1 | T    | h  | V  | r1 | r0                                 | 0 | 0 | 1    | T | h  | V  | r1 | r0 |
| I  | Step-in         | 0 | 1 | 0 | T    | h  | V  | r1 | r0                                 | 0 | 1 | 0    | T | h  | V  | r1 | r0 |
| I  | Step-out        | 0 | 1 | 1 | T    | h  | V  | r1 | r0                                 | 0 | 1 | 1    | T | h  | V  | r1 | r0 |
| II   | Read Sector     | 1 | 0 | 0 | m    | S  | E  | C  | 0                                  | 1 | 0 | 0    | m | L  | E  | U  | 0  |
| II   | Write Sector    | 1 | 0 | 1 | m    | S  | E  | C  | a0                                 | 1 | 0 | 1    | m | L  | E  | U  | a0 |
| III  | Read Address    | 1 | 1 | 0 | 0    | 0  | E  | 0  | 0                                  | 1 | 1 | 0    | 0 | 0  | E  | U  | 0  |
| III  | Read Track      | 1 | 1 | 1 | 0    | 0  | E  | 0  | 0                                  | 1 | 1 | 1    | 0 | 0  | E  | U  | 0  |
| III  | Write Track     | 1 | 1 | 1 | 1    | 0  | E  | 0  | 0                                  | 1 | 1 | 1    | 1 | 0  | E  | U  | 0  |
| IV   | Force Interrupt | 1 | 1 | 0 | l1   | l3 | l2 | l1 | l0                                 | 1 | 1 | 0    | 1 | l3 | l2 | l1 | l0 |

**TABLE 2. FLAG SUMMARY**

**FLAG SUMMARY**

| Command Type                    | Bit No(s) | Description  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
|---------------------------------|-----------|--|---------------------------------|------|--|--|--|--|----|----|----|----|-------|-----|-----|------|-----|-------|-----|-----|-----|------|
| I                               | 0, 1      | r1 r0 = Stepping Motor Rate<br>See Table 3 for Rate Summary  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| I                               | 2         | V = Track Number Verify Flag<br>V = 0, No verify<br>V = 1, Verify on destination track   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| I                               | 3         | h = Head Load Flag<br>h = 0, Load head at beginning<br>h = 1, Unload head at beginning   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| I                               | 4         | T = Track Update Flag<br>T = 0, No update<br>T = 1, Update track register  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II & III                        | 0         | a0 = Data Address Mark<br>a0 = 0, FB (DAM)<br>a0 = 1, F8 (deleted DAM)   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II                              | 1         | C = Side Compare Flag<br>C = 0, Disable side compare<br>C = 1, Enable side compare   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II & III                        | 1         | U = Update SSO<br>U = 0, Update SSO to 0<br>U = 1, Update SSO to 1   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II & III                        | 2         | E = 15 MS Delay<br>E = 0, No 15 MS delay<br>E = 1, 15 MS delay   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II                              | 3         | S = Side Compare Flag<br>S = 0, Compare for side 0<br>S = 1, Compare for side 1  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II                              | 3         | L = Sector Length Flag   |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
|                                 |           | <table border="1"> <thead> <tr> <th colspan="5">LSB's Sector Length in ID Field</th> </tr> <tr> <th></th> <th>00</th> <th>01</th> <th>10</th> <th>11</th> </tr> </thead> <tbody> <tr> <td>L = 0</td> <td>256</td> <td>512</td> <td>1024</td> <td>128</td> </tr> <tr> <td>L = 1</td> <td>128</td> <td>256</td> <td>512</td> <td>1024</td> </tr> </tbody> </table> | LSB's Sector Length in ID Field |      |  |  |  |  | 00 | 01 | 10 | 11 | L = 0 | 256 | 512 | 1024 | 128 | L = 1 | 128 | 256 | 512 | 1024 |
| LSB's Sector Length in ID Field |           |  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
|                                 | 00        | 01   | 10                              | 11   |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| L = 0                           | 256       | 512  | 1024                            | 128  |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| L = 1                           | 128       | 256  | 512                             | 1024 |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| II                              | 4         | m = Multiple Record Flag<br>m = 0, Single record<br>m = 1, Multiple records  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |
| IV                              | 0-3       | lx = Interrupt Condition Flags<br>l0 = 1 Not Ready To Ready Transition<br>l1 = 1 Ready To Not Ready Transition<br>l2 = 1 Index Pulse<br>l3 = 1 Immediate Interrupt, Requires A Reset<br>l3-l1 = 0 Terminate With No Interrupt (INTRQ)  |                                 |      |  |  |  |  |    |    |    |    |       |     |     |      |     |       |     |     |     |      |

\*NOTE: See Type IV Command Description for further information.

## TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field ( $\overline{r0}$   $r1$ ), which determines the stepping motor rate as defined in Table 3.

A 2  $\mu$ s (MFM) or 4  $\mu$ s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12  $\mu$ s before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

| CLK               | 2 MHz               | 2 MHz               | 1 MHz               | 1 MHz               | 2 MHz               | 1 MHz               |
|-------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| $\overline{DDEN}$ | 0                   | 1                   | 0                   | 1                   | x                   | x                   |
| R1 R0             | $\overline{TEST}=1$ | $\overline{TEST}=1$ | $\overline{TEST}=1$ | $\overline{TEST}=1$ | $\overline{TEST}=0$ | $\overline{TEST}=0$ |
| 0 0               | 3 ms                | 3 ms                | 6 ms                | 6 ms                | 184 $\mu$ s         | 368 $\mu$ s         |
| 0 1               | 6 ms                | 6 ms                | 12 ms               | 12 ms               | 190 $\mu$ s         | 380 $\mu$ s         |
| 1 0               | 10 ms               | 10 ms               | 20 ms               | 20 ms               | 198 $\mu$ s         | 396 $\mu$ s         |
| 1 1               | 15 ms               | 15 ms               | 30 ms               | 30 ms               | 208 $\mu$ s         | 416 $\mu$ s         |

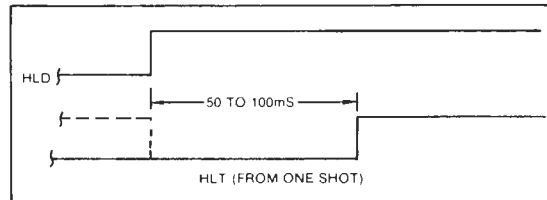
After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If  $\overline{TEST} = 0$ , there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by settling bit 2 ( $V = 1$ ) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If  $V = 0$ , no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set ( $h = 1$ ), at the end of the Type I command if the verify flag ( $V = 1$ ), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with ( $h = 0$  and  $V = 0$ ); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the FD179X which is used for the head engage time. When  $HLT = 1$ , the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if  $h = 0$  and  $V = 0$ , HLD is reset. If  $h = 1$  and  $V = 0$ , HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If  $h = 0$  and  $V = 1$ , HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If  $h = 1$  and  $V = 1$ , HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

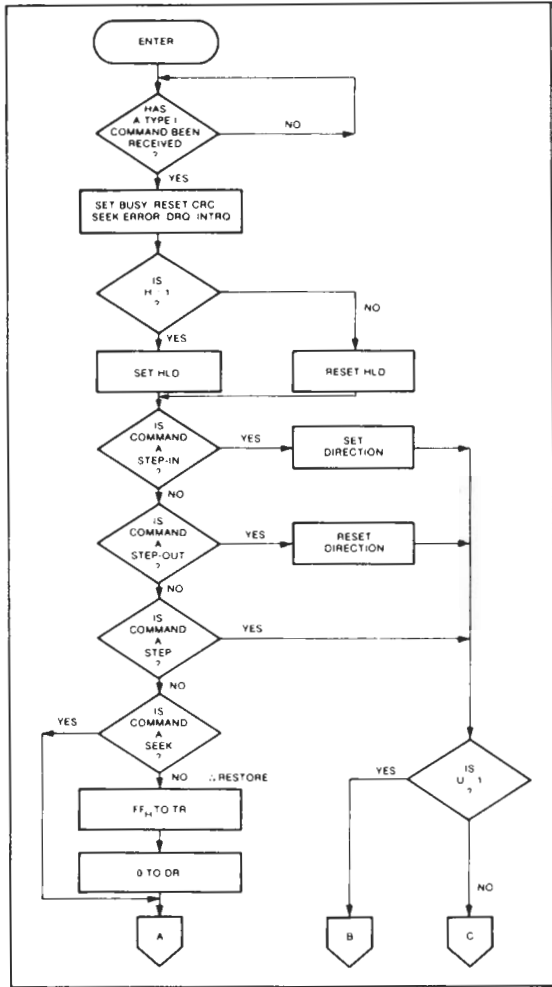
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

## RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ( $\overline{TR00}$ ) input is sampled. If  $\overline{TR00}$  is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If  $\overline{TR00}$  is not active low, stepping pulses (pins 15 to 16) at a rate specified by the  $r1$   $r0$  field are issued until the  $\overline{TR00}$  input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the  $\overline{TR00}$  input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when  $\overline{MR}$  goes from an active to an inactive state and that the DRQ pin stays low.

## SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of



TYPE I COMMAND FLOW

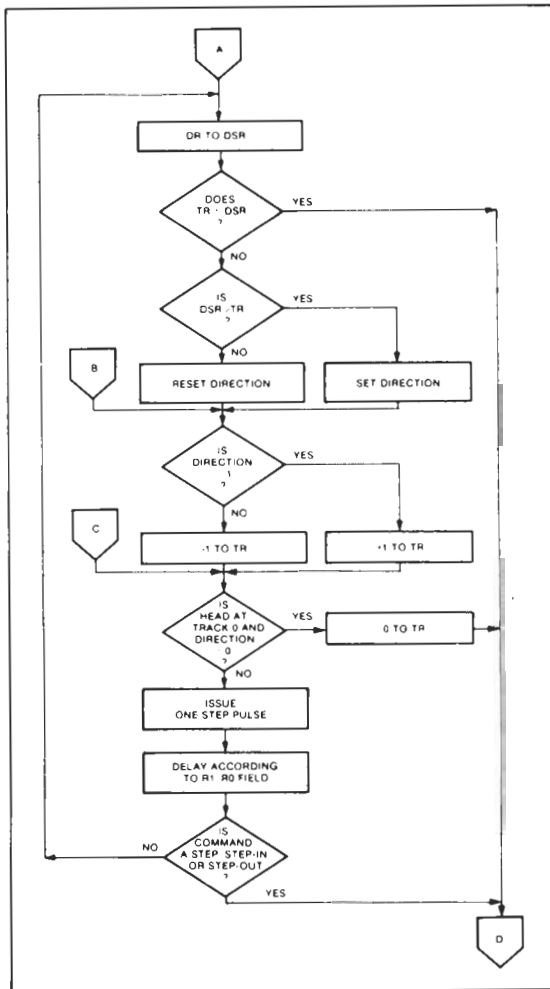
the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

**STEP**

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**STEP-IN**

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the U



TYPE I COMMAND FLOW

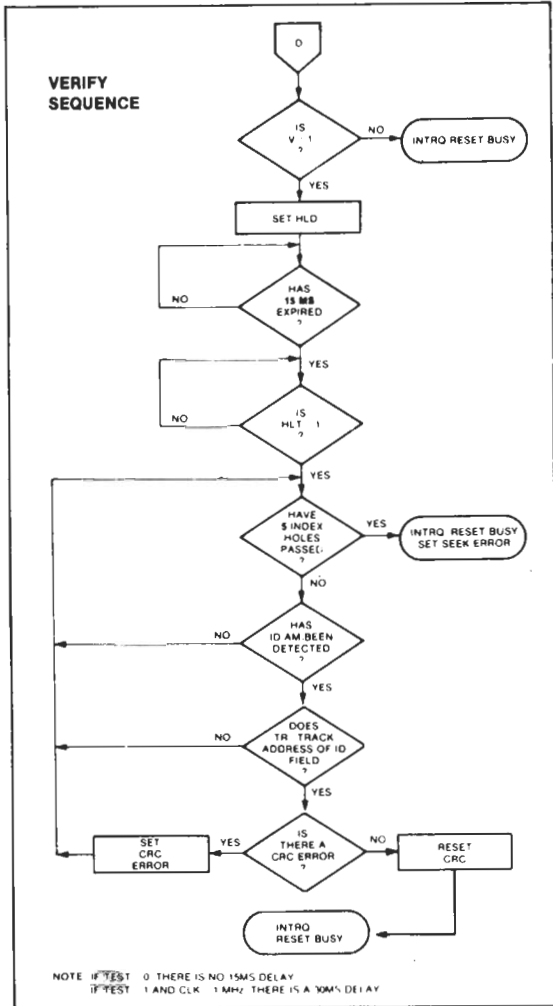
flag is on, the Track Register is incremented by one. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**STEP-OUT**

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1f0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**EXCEPTIONS**

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



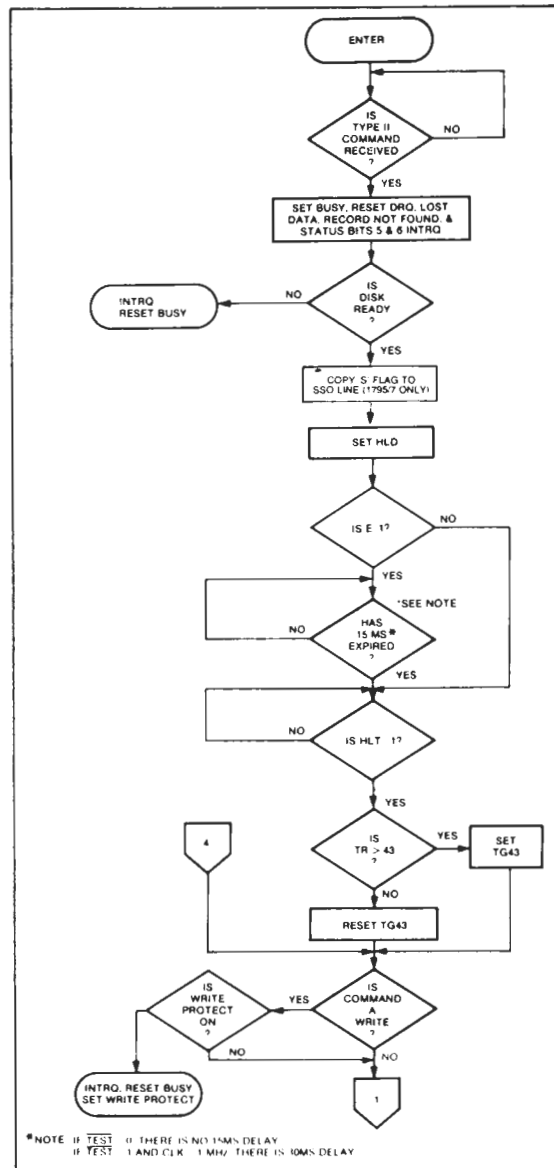
TYPE I COMMAND FLOW

**TYPE II COMMANDS**

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons

again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the

completion of the command. If  $m = 1$ , multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the FD179X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The FD179X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for 1791-94 also contain side select compare flags. When  $C = 0$  (Bit 1) no side comparison is made. When  $C = 1$ , the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the FD179X continues with the ID search. If a comparison is not made within 5 index

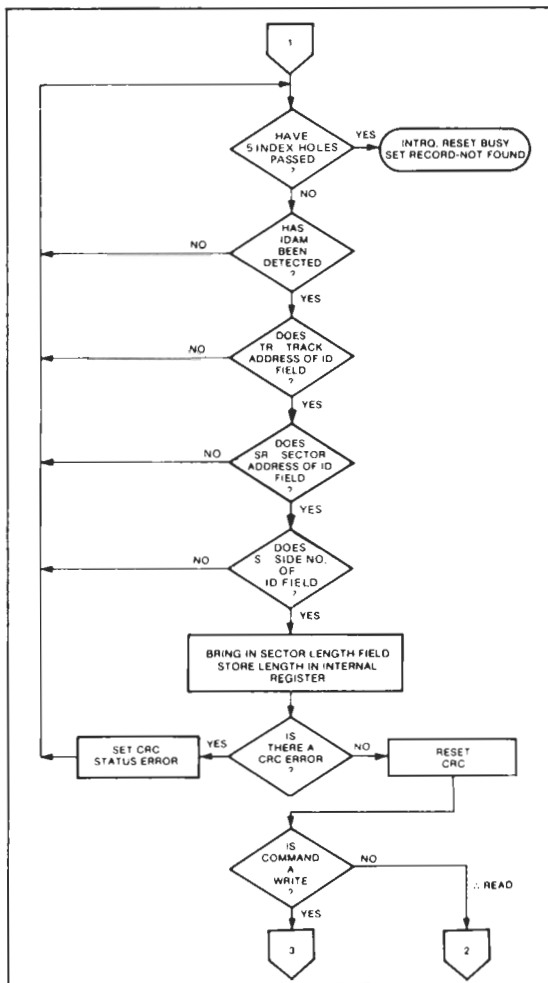
pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 1795-97 contain a side select flag (Bit 1). When  $U = 0$ , SSO is updated to 0. Similarly,  $U = 1$  updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

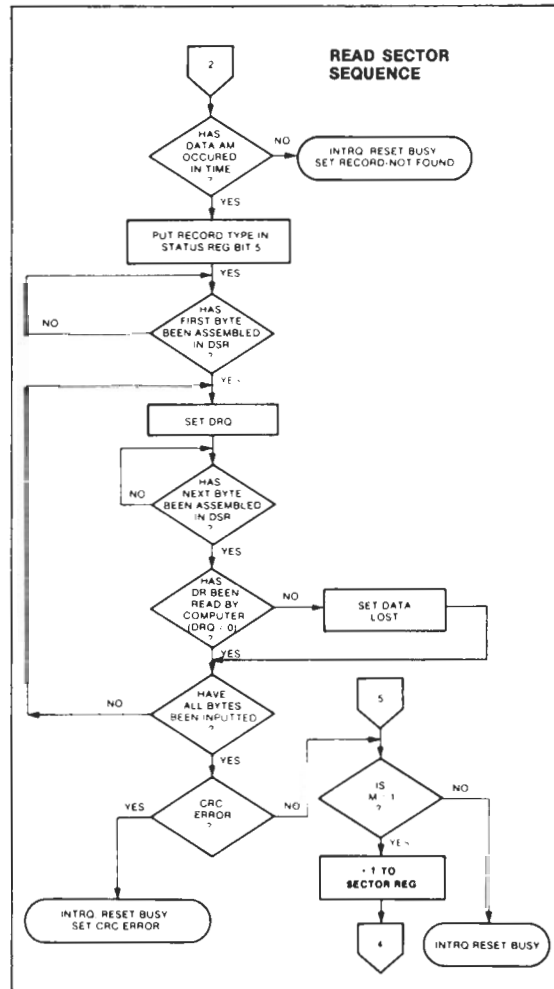
The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

**READ SECTOR**

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address

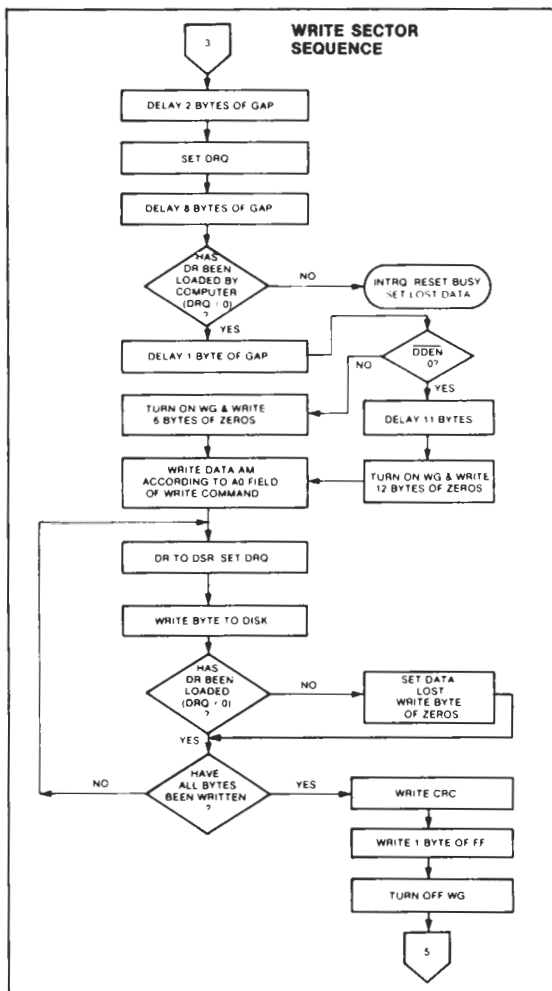


TYPE II COMMAND



TYPE II COMMAND





TYPE II COMMAND

Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown :

STATUS BIT 5

|   |                   |
|---|-------------------|
| 1 | Deleted Data Mark |
| 0 | Data Mark         |

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

a0 Data Address Mark (Bit 0)

|   |                   |
|---|-------------------|
| 1 | Deleted Data Mark |
| 0 | Data Mark         |

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDRESS | SECTOR LENGTH | CRC 1 | CRC 2 |
|------------|-------------|----------------|---------------|-------|-------|
| 1          | 2           | 3              | 4             | 5     | 6     |

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

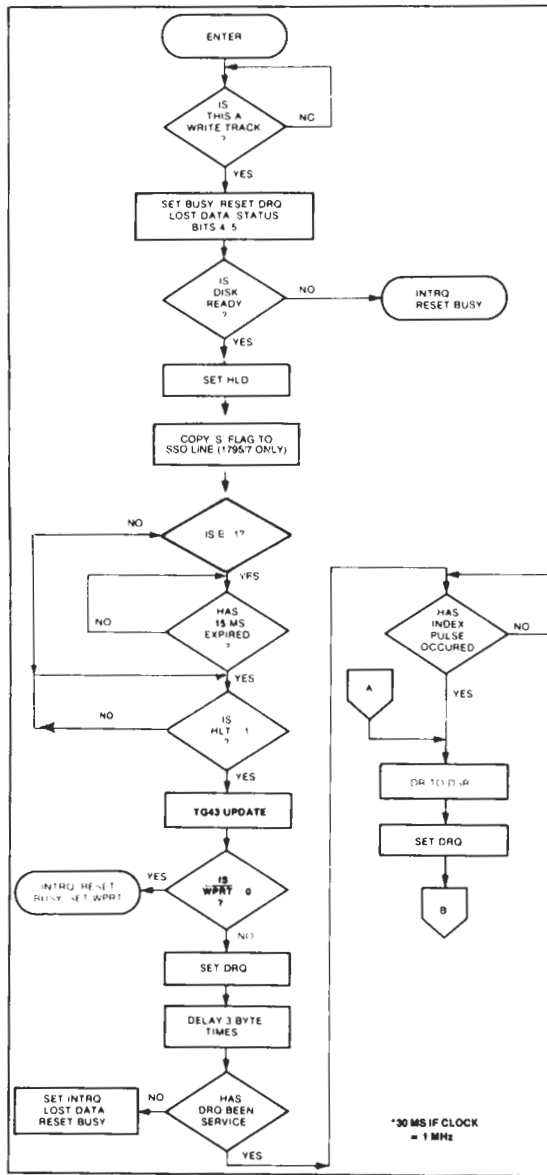
**READ TRACK**

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

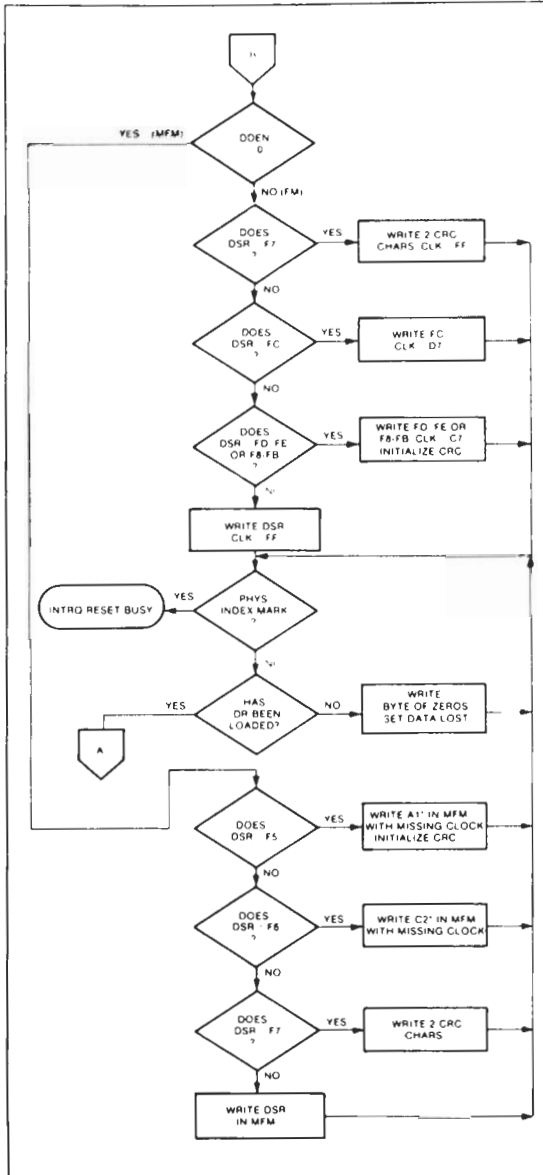
This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate

is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set.

The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.



**TYPE III COMMAND WRITE TRACK**



**TYPE III COMMAND WRITE TRACK**

## CONTROL BYTES FOR INITIALIZATION

| DATA PATTERN<br>IN DR (HEX) | FD179X INTERPRETATION<br>IN FM (DDEN = 1) | FD1791/3 INTERPRETATION<br>IN MFM (DDEN = 0) |
|-----------------------------|---|--|
| 00 thru F4                  | Write 00 thru F4 with CLK = FF            | Write 00 thru F4, in MFM                     |
| F5                          | Not Allowed                               | Write A1* in MFM, Preset CRC                 |
| F6                          | Not Allowed                               | Write C2** in MFM                            |
| F7                          | Generate 2 CRC bytes                      | Generate 2 CRC bytes                         |
| F8 thru FB                  | Write F8 thru FB, Clk = C7, Preset CRC    | Write F8 thru FB, in MFM                     |
| FC                          | Write FC with Clk = D7                    | Write FC in MFM                              |
| FD                          | Write FD with Clk = FF                    | Write FD in MFM                              |
| FE                          | Write FE, Clk = C7, Preset CRC            | Write FE in MFM                              |
| FF                          | Write FF with Clk = FF                    | Write FF in MFM                              |

\*Missing clock transition between bits 4 and 5

\*\*Missing clock transition between bits 3 &amp; 4

## WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the RW head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

## TYPE IV COMMANDS

The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to in-

sure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

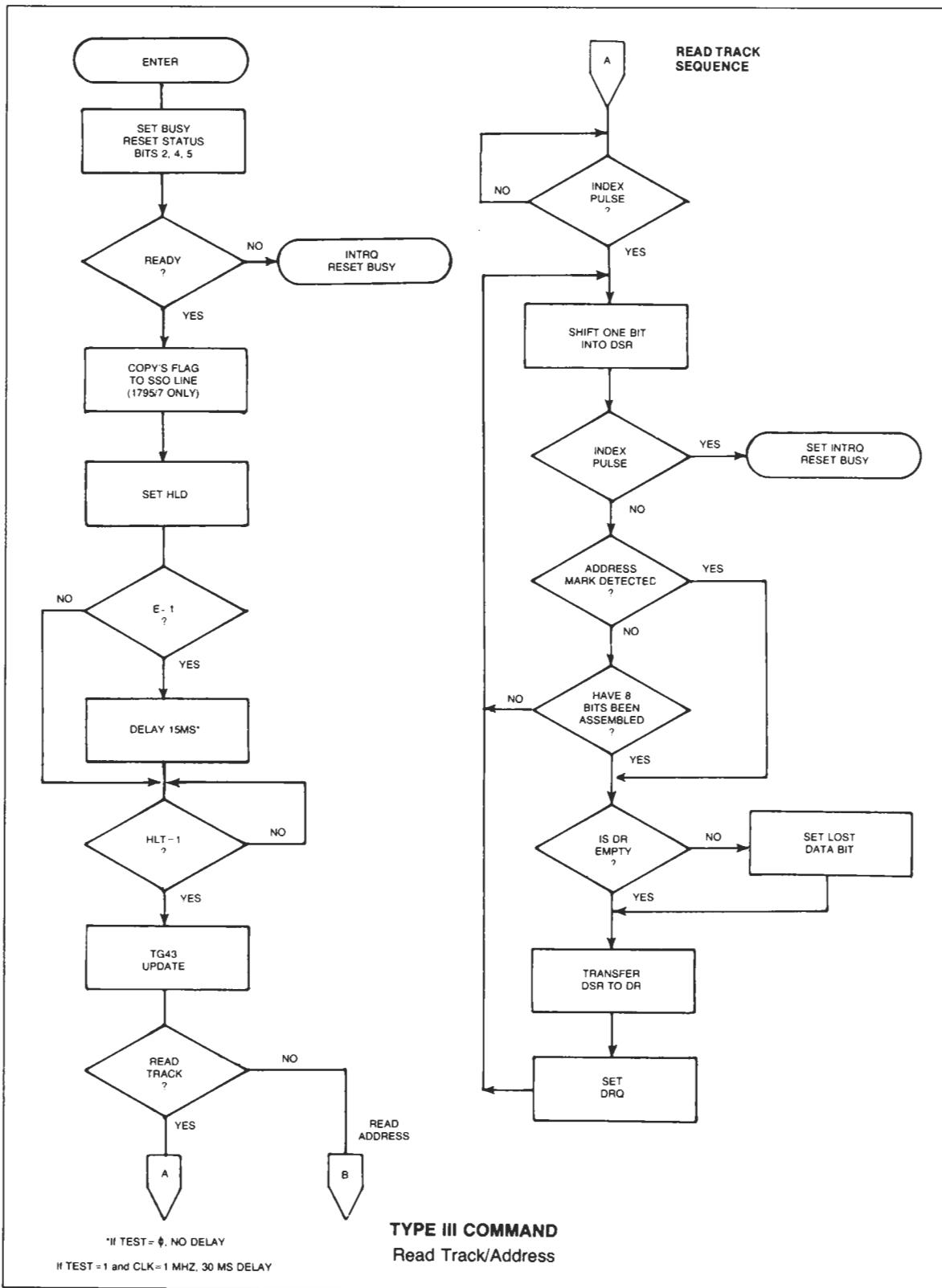
- I0 = Not-Ready to Ready Transition
- I1 = Ready to Not-Ready Transition
- I2 = Every Index Pulse
- I3 = Immediate Interrupt

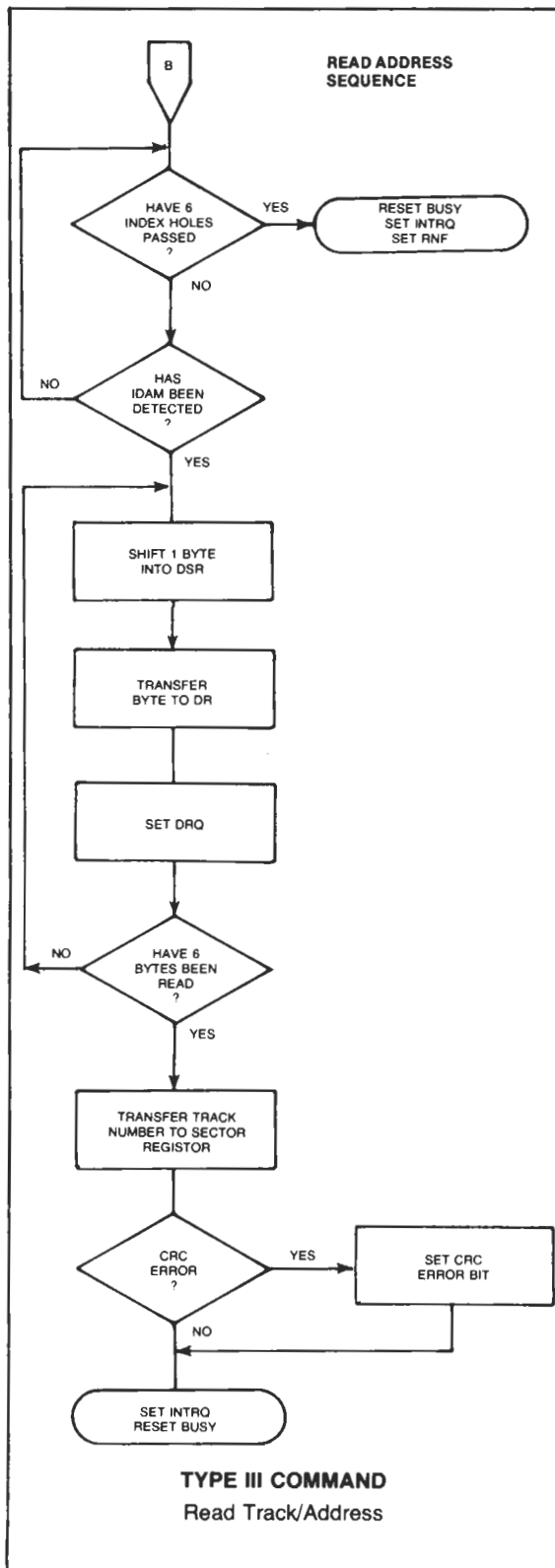
The conditional interrupt is enabled when the corresponding bit positions of the command (I3 - I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I3 - I0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1) an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.





**STATUS REGISTER**

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

| (BITS) |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| S7     | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

| Operation             | Next Operation               | Delay Req'd. |       |
|-----------------------|------------------------------|--------------|-------|
|                       |                              | FM           | MFM   |
| Write to Command Reg. | Read Busy Bit (Status Bit 0) | 12 μs        | 6 μs  |
| Write to Command Reg. | Read Status Bits 1-7         | 28 μs        | 14 μs |
| Write Any Register    | Read From Diff. Register     | 0            | 0     |

**IBM 3740 FORMAT — 128 BYTES/SECTOR**

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

| NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|-----------------|---------------------------|
| 40              | FF (or 00)*               |
| 6               | 00                        |
| 1               | FC (Index Mark)           |
| 26              | FF (or 00)*               |
| 6               | 00                        |
| 1               | FE (ID Address Mark)      |
| 1               | Track Number              |
| 1               | Side Number (00 or 01)    |
| 1               | Sector Number (1 thru 1A) |
| 1               | 00 (Sector Length)        |
| 1               | F7 (2 CRC's written)      |
| 11              | FF (or 00)*               |
| 6               | 00                        |
| 1               | FB (Data Address Mark)    |
| 128             | Data (IBM uses E5)        |
| 1               | F7 (2 CRC's written)      |
| 27              | FF (or 00)*               |
| 247**           | FF (or 00)*               |

\*Write bracketed field 26 times  
 \*\*Continue writing until FD179X interrupts out.  
 Approx. 247 bytes.  
 1-Optional '00' on 1795/7 only.

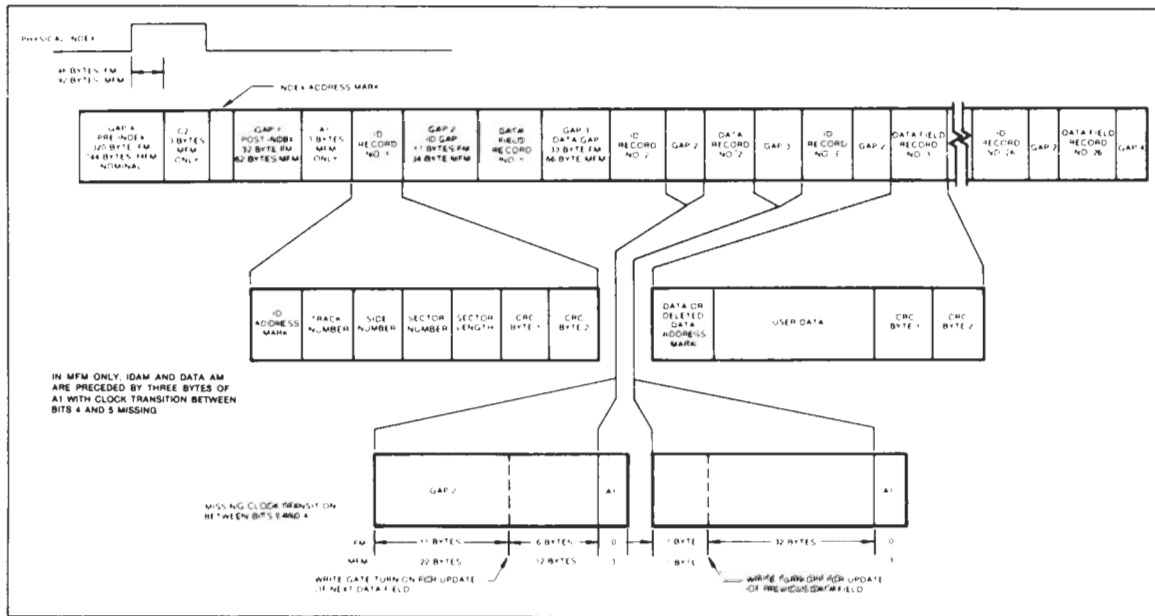
**IBM SYSTEM 34 FORMAT-  
 256 BYTES/SECTOR**

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must

issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

| NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|-----------------|---------------------------|
| 80              | 4E                        |
| 12              | 00                        |
| 3               | F6 (Writes C2)            |
| 1               | FC (Index Mark)           |
| 50              | 4E                        |
| 12              | 00                        |
| 3               | F5 (Writes A1)            |
| 1               | FE (ID Address Mark)      |
| 1               | Track Number (0 thru 4C)  |
| 1               | Side Number (0 or 1)      |
| 1               | Sector Number (1 thru 1A) |
| 1               | 01 (Sector Length)        |
| 1               | F7 (2 CRCs written)       |
| 22              | 4E                        |
| 12              | 00                        |
| 3               | F5 (Writes A1)            |
| 1               | FB (Data Address Mark)    |
| 256             | DATA                      |
| 1               | F7 (2 CRCs written)       |
| 54              | 4E                        |
| 598**           | 4E                        |

\*Write bracketed field 26 times  
 \*\*Continue writing until FD179X interrupts out.  
 Approx. 598 bytes.



**IBM TRACK FORMAT**

**1. NON-IBM FORMATS**

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

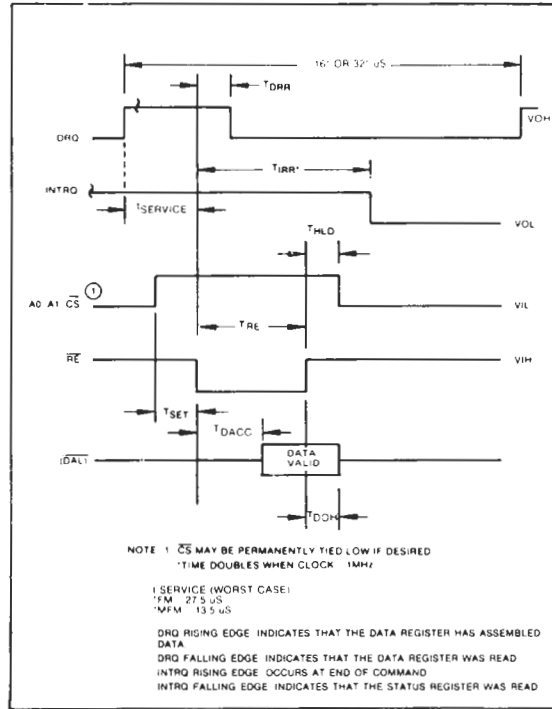
- 1) Sector size must be 128, 256, 512 of 1024 bytes.
- 2) Gap 2 cannot be varied from the IBM format.
- 3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the FD179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FD179X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

|           | FM                        | MFM                                     |
|-----------|---------------------------|---|
| Gap I     | 16 bytes FF               | 32 bytes 4E                             |
| Gap II    | 11 bytes FF               | 22 bytes 4E                             |
| •         | 6 bytes 00                | 12 bytes 00                             |
| •         |                           | 3 bytes A1                              |
| Gap III** | 10 bytes FF<br>4 bytes 00 | 24 bytes 4E<br>8 bytes 00<br>3 bytes A1 |
| Gap IV    | 16 bytes FF               | 16 bytes 4E                             |

\*Byte counts must be exact.

\*\*Byte counts are minimum, except exactly 3 bytes of A1 must be written.



**TIMING CHARACTERISTICS**

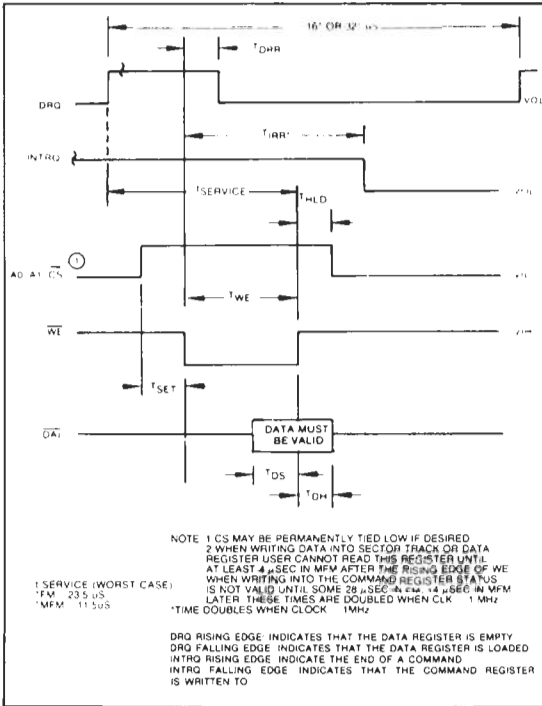
T<sub>A</sub> = 0°C to 70°C, V<sub>DD</sub> = +12V ± .6V, V<sub>SS</sub> = 0V, V<sub>CC</sub> = +5V ± .25V

**READ ENABLE TIMING** (See Note 6, Page 21)

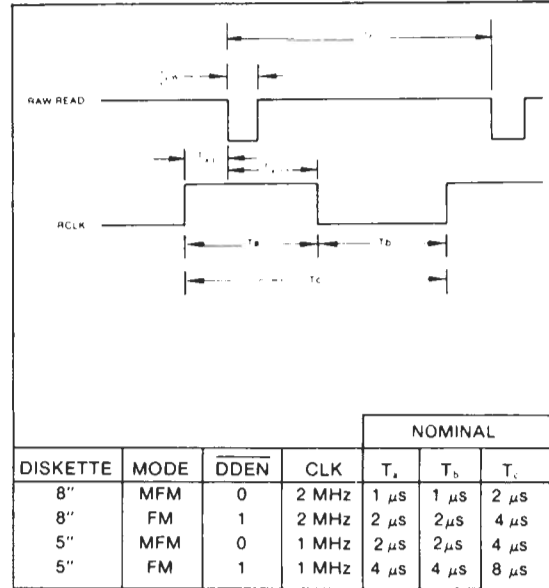
| SYMBOL | CHARACTERISTIC                      | MIN. | TYP. | MAX. | UNITS | CONDITIONS             |
|--------|-------------------------------------|------|------|------|-------|------------------------|
| TSET   | Setup ADDR & CS to $\overline{RE}$  | 50   |      |      | nsec  |                        |
| THLD   | Hold ADDR & CS from $\overline{RE}$ | 10   |      |      | nsec  |                        |
| TRE    | $\overline{RE}$ Pulse Width         | 400  |      |      | nsec  | C <sub>L</sub> = 50,pf |
| TDRR   | DRQ Reset from $\overline{RE}$      |      | 400  | 500  | nsec  |                        |
| TIRR   | INTRQ Reset from $\overline{RE}$    |      | 500  | 3000 | nsec  | See Note 5             |
| TDACC  | Data Access from $\overline{RE}$    |      |      |      | nsec  | C <sub>L</sub> = 50 pf |
| TDOH   | Data Hold From $\overline{RE}$      | 50   |      | 150  | nsec  | C <sub>L</sub> = 50 pf |

**WRITE ENABLE TIMING** (See Note 6, Page 21)

| SYMBOL | CHARACTERISTIC                      | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|--------|-------------------------------------|------|------|------|-------|------------|
| TSET   | Setup ADDR & CS to $\overline{WE}$  | 50   |      |      | nsec  |            |
| THLD   | Hold ADDR & CS from $\overline{WE}$ | 10   |      |      | nsec  |            |
| TWE    | $\overline{WE}$ Pulse Width         | 350  |      |      | nsec  |            |
| TDRR   | DRQ Reset from $\overline{WE}$      |      | 400  | 500  | nsec  |            |
| TIRR   | INTRQ Reset from $\overline{WE}$    |      | 500  | 3000 | nsec  | See Note 5 |
| TDS    | Data Setup to $\overline{WE}$       | 250  |      |      | nsec  |            |
| TDH    | Data Hold from $\overline{WE}$      | 70   |      |      | nsec  |            |



**WRITE ENABLE TIMING**



**INPUT DATA TIMING**

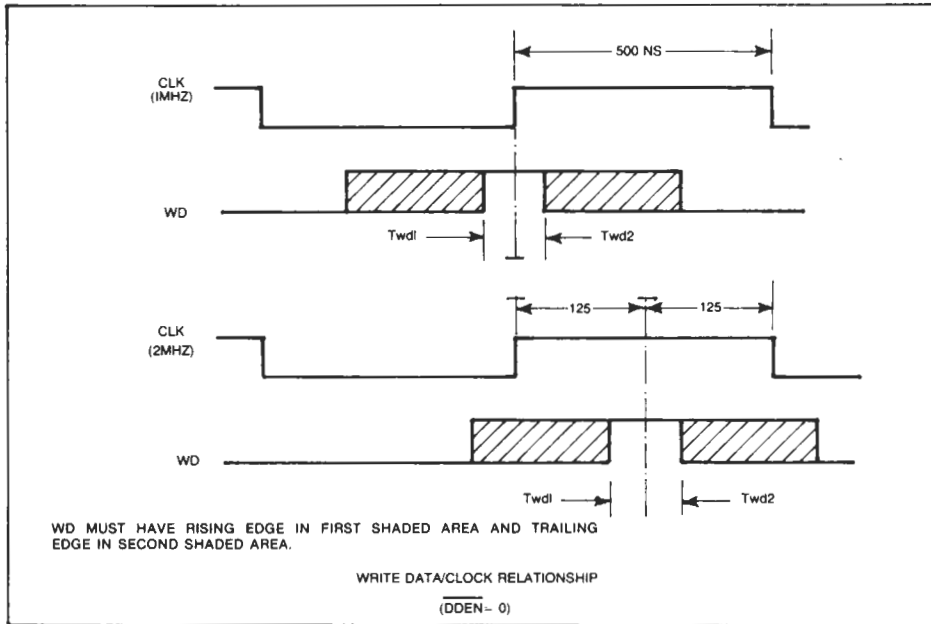
**INPUT DATA TIMING:**

| SYMBOL          | CHARACTERISTIC        | MIN. | TYP. | MAX. | UNITS | CONDITIONS     |
|-----------------|-----------------------|------|------|------|-------|----------------|
| T <sub>pw</sub> | Raw Read Pulse Width  | 100  | 200  |      | nsec  | See Note 1     |
| t <sub>bc</sub> | Raw Read Cycle Time   | 1500 | 2000 |      | nsec  | 1800 ns @ 70°C |
| T <sub>c</sub>  | RCLK Cycle Time       | 1500 | 2000 |      | nsec  | 1800 ns @ 70°C |
| T <sub>X1</sub> | RCLK hold to Raw Read | 40   |      |      | nsec  | See Note 1     |
| T <sub>X2</sub> | Raw Read hold to RCLK | 40   |      |      | nsec  | See Note 1     |

**WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (See Note 6, Page 21)**

| SYMBOL           | CHARACTERISTICS              | MIN. | TYP.      | MAX. | UNITS | CONDITIONS  |
|------------------|------------------------------|------|-----------|------|-------|-------------|
| T <sub>wp</sub>  | Write Data Pulse Width       | 450  | 500       | 550  | nsec  | FM          |
|                  |                              | 150  | 200       | 250  | nsec  | MFM         |
| T <sub>wg</sub>  | Write Gate to Write Data     |      | 2         |      | μsec  | FM          |
|                  |                              |      | 1         |      | μsec  | MFM         |
| T <sub>bc</sub>  | Write data cycle Time        |      | 2,3, or 4 |      | μsec  | ± CLK Error |
| T <sub>s</sub>   | Early (Late) to Write Data   | 125  |           |      | nsec  | MFM         |
| T <sub>h</sub>   | Early (Late) From Write Data | 125  |           |      | nsec  | MFM         |
| T <sub>wf</sub>  | Write Gate off from WD       |      | 2         |      | μsec  | FM          |
|                  |                              |      | 1         |      | μsec  | MFM         |
| T <sub>wd1</sub> | WD Valid to Clk              | 100  |           |      | nsec  | CLK=1 MHZ   |
|                  |                              | 50   |           |      | nsec  | CLK=2 MHZ   |
| T <sub>wd2</sub> | WD Valid after CLK           | 100  |           |      | nsec  | CLK=1 MHZ   |
|                  |                              | 30   |           |      | nsec  | CLK=2 MHZ   |

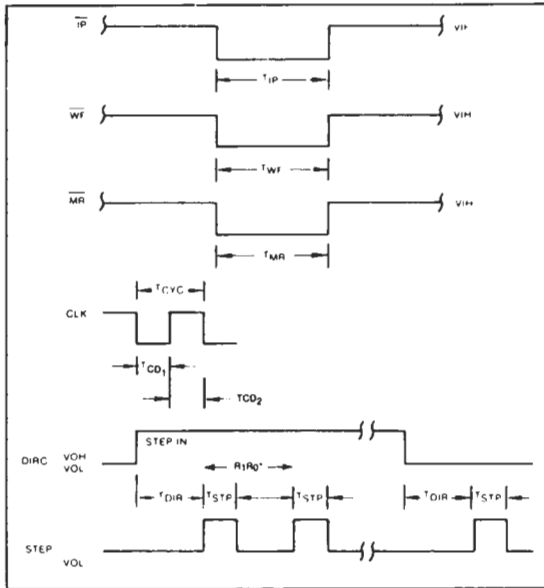




### WRITE DATA TIMING

MISCELLANEOUS TIMING: (Times Double When Clock = 1 MHz) (See Note 6, Page 21)

| SYMBOL           | CHARACTERISTIC           | MIN.   | TYP. | MAX.  | UNITS | CONDITIONS                |
|------------------|--------------------------|--------|------|-------|-------|---------------------------|
| TCD <sub>1</sub> | Clock Duty (low)         | 230    | 250  | 20000 | nsec  |                           |
| TCD <sub>2</sub> | Clock Duty (high)        | 200    | 250  | 20000 | nsec  |                           |
| TSTP             | Step Pulse Output        | 2 or 4 |      |       | μsec  | See Note 5<br>± CLK ERROR |
| TDIR             | Dir Setup to Step        |        | 12   |       | μsec  |                           |
| TMR              | Master Reset Pulse Width | 50     |      |       | μsec  | See Note 5                |
| TIP              | Index Pulse Width        | 10     |      |       | μsec  |                           |
| TWF              | Write Fault Pulse Width  | 10     |      |       | μsec  |                           |



**MISCELLANEOUS TIMING**

\*FROM STEP RATE TABLE

**NOTES:**

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2  $\mu$ s, nominal in MFM and 4  $\mu$ s nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.
6. Output timing readings are at  $V_{OL} = 0.8v$  and  $V_{OH} = 2.0v$ .

**Table 4. STATUS REGISTER SUMMARY**

| BIT | ALL TYPE I COMMANDS | READ ADDRESS | READ SECTOR | READ TRACK | WRITE SECTOR  | WRITE TRACK   |
|-----|---------------------|--------------|-------------|------------|---------------|---------------|
| S7  | NOT READY           | NOT READY    | NOT READY   | NOT READY  | NOT READY     | NOT READY     |
| S6  | WRITE PROTECT       | 0            | 0           | 0          | WRITE PROTECT | WRITE PROTECT |
| S5  | HEAD LOADED         | 0            | RECORD TYPE | 0          | WRITE FAULT   | WRITE FAULT   |
| S4  | SEEK ERROR          | RNF          | RNF         | 0          | RNF           | 0             |
| S3  | CRC ERROR           | CRC ERROR    | CRC ERROR   | 0          | CRC ERROR     | 0             |
| S2  | TRACK 0             | LOST DATA    | LOST DATA   | LOST DATA  | LOST DATA     | LOST DATA     |
| S1  | INDEX PULSE         | DRQ          | DRQ         | DRQ        | DRQ           | DRQ           |
| S0  | BUSY                | BUSY         | BUSY        | BUSY       | BUSY          | BUSY          |

**STATUS FOR TYPE I COMMANDS**

| BIT NAME       | MEANING  |
|----------------|--|
| S7 NOT READY   | This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR. |
| S6 PROTECTED   | When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.   |
| S5 HEAD LOADED | When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.   |
| S4 SEEK ERROR  | When set, the desired track was not verified. This bit is reset to 0 when updated.   |
| S3 CRC ERROR   | CRC encountered in ID field.   |
| S2 TRACK 00    | When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.   |
| S1 INDEX       | When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.   |
| S0 BUSY        | When set command is in progress. When reset no command is in progress.   |

**STATUS FOR TYPE II AND III COMMANDS**

| BIT NAME                       | MEANING  |
|--------------------------------|--|
| S7 NOT READY                   | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready. |
| S6 WRITE PROTECT               | On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.   |
| S5 RECORD TYPE/<br>WRITE FAULT | On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.  |
| S4 RECORD NOT<br>FOUND (RNF)   | When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.   |
| S3 CRC ERROR                   | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.  |
| S2 LOST DATA                   | When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.   |
| S1 DATA REQUEST                | This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.   |
| S0 BUSY                        | When set, command is under execution. When reset, no command is under execution.   |

**ELECTRICAL CHARACTERISTICS**

## Absolute Maximum Ratings

$V_{DD}$  with respect to  $V_{SS}$  (ground): + 15 to - 0.3V  
Voltage to any input with respect to  $V_{SS}$  = + 15 to - 0.3V  
 $I_{CC}$  = 60 MA (35 MA nominal)  
 $I_{DD}$  = 15 MA (10 MA nominal)

Dissipation = 0.6 W

$C_{IN}$  &  $C_{OUT}$  = 15 pF max with all pins grounded except  
one under test.

Operating temperature = 0°C to 70°C

Storage temperature = - 55°C to + 125°C

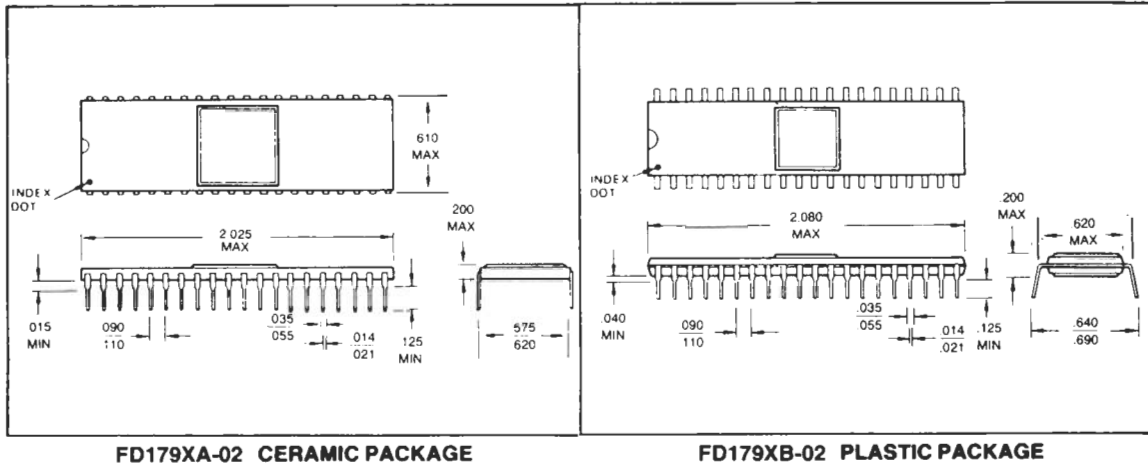
**OPERATING CHARACTERISTICS (DC)**

$T_A$  = 0°C to 70°C,  $V_{DD}$  = + 12V  $\pm$  .6V,  $V_{SS}$  = 0V,  $V_{CC}$  = + 5V  $\pm$  .25V

| SYMBOL   | CHARACTERISTIC      | MIN. | MAX. | UNITS   | CONDITIONS               |
|----------|---------------------|------|------|---------|--------------------------|
| $I_{IL}$ | Input Leakage       |      | 10   | $\mu$ A | $V_{IN} = V_{DD}^{**}$   |
| $I_{OL}$ | Output Leakage      |      | 10   | $\mu$ A | $V_{OUT} = V_{DD}$       |
| $V_{IH}$ | Input High Voltage  | 2.6  |      | V       |                          |
| $V_{IL}$ | Input Low Voltage   |      | 0.8  | V       |                          |
| $V_{OH}$ | Output High Voltage | 2.8  |      | V       | $I_o = -100 \mu$ A       |
| $V_{OL}$ | Output Low Voltage  |      | 0.45 | V       | $I_o = 1.6 \text{ mA}^*$ |
| $P_D$    | Power Dissipation   |      | 0.6  | W       |                          |

\*1792 and 1794  $I_o = 1.0 \text{ mA}$

\*\*Leakage conditions are for input pins without internal pull-up resistors.



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# WESTERN DIGITAL

C O R P O R A T I O N

## WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

### FEATURES

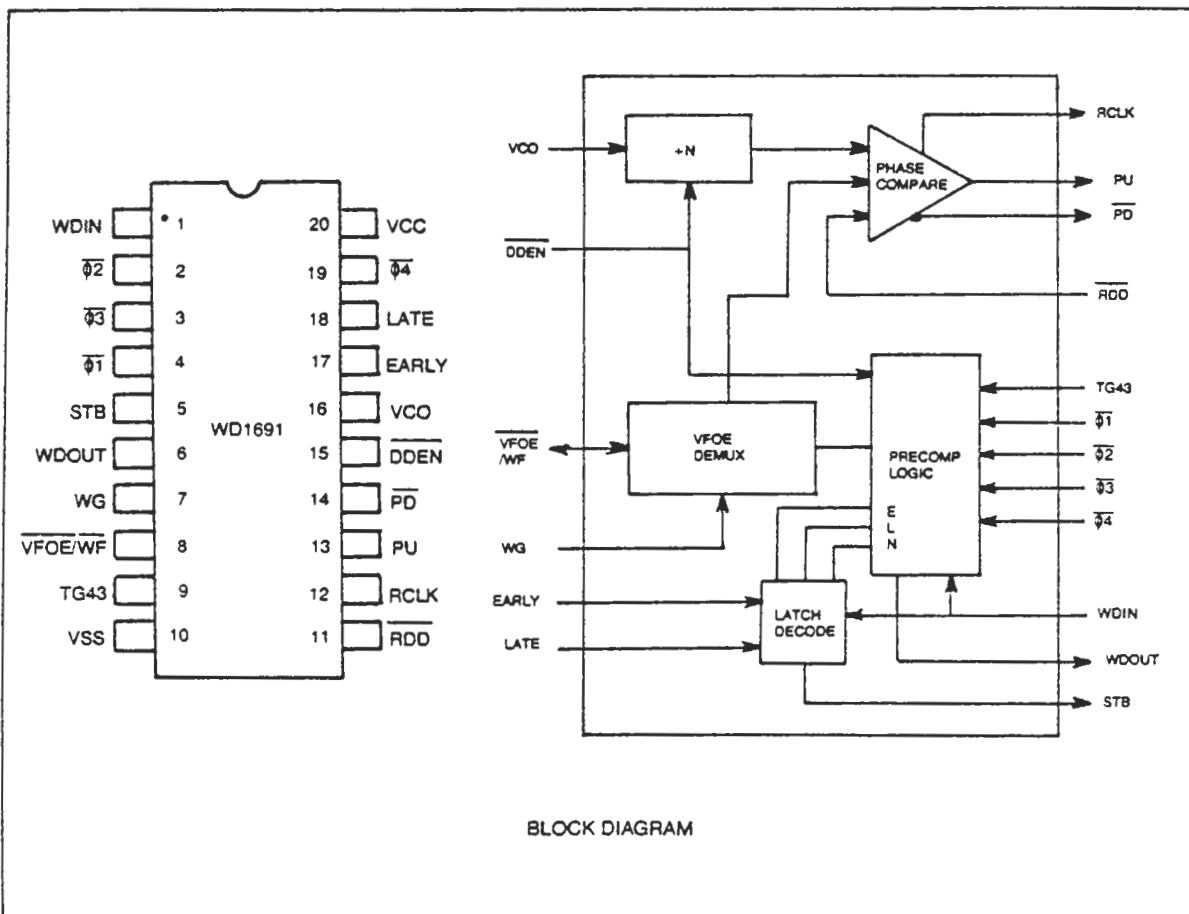
- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

### GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.

October, 1980



| PIN         | NAME                          | SYMBOL  | FUNCTION   |
|-------------|-------------------------------|---|--|
| 1           | WRITE DATA INPUT              | WDIN  | Ties directly to the FD179X WD pin.  |
| 2, 3, 4, 19 | PHASE<br>2, 3, 1, 4           | $\overline{02}$ $\overline{03}$ $\overline{01}$ $\overline{04}$ | 4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.                    |
| 5           | STROBE                        | STB   | Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04. |
| 6           | WRITE DATA OUTPUT             | WDOU  | Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.  |
| 7           | WRITE GATE                    | WG  | Ties directly to the FD179X WG pin.  |
| 8           | VFO ENABLE/<br>WRITE FAULT    | $\overline{\text{VFOE/WF}}$                                     | Ties directly to the FD179X $\overline{\text{VFOE/WF}}$ pin.   |
| 9           | TRACK 43                      | TG43  | Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.  |
| 10          | V <sub>ss</sub>               | V <sub>ss</sub>   | Ground   |
| 11          | READ DATA                     | $\overline{\text{RDD}}$   | Composite clock and data stream input from the drive.  |
| 12          | READ CLOCK                    | RCLK  | RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.  |
| 13          | PUMP UP                       | PU  | Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.   |
| 14          | PUMP DOWN                     | $\overline{\text{PD}}$  | Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.   |
| 15          | Double Density Enable         | $\overline{\text{DDEN}}$  | Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.   |
| 16          | Voltage Controlled Oscillator | VCO   | A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.  |
| 17, 18      | EARLY<br>LATE                 | EARLY<br>LATE   | EARLY and LATE signals from the FD179X, used to determine Write Precompensation.   |
| 20          | V <sub>cc</sub>               | V <sub>cc</sub>   | + 5V $\pm$ 10% power supply  |

**DEVICE DESCRIPTION**

The WD1691 is divided into two sections:

- 1) Data Recovery Circuit
- 2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs:  $\overline{DDEN}$ ,  $\overline{VCO}$ ,  $\overline{RDD}$ , and  $\overline{VFOE/WF}$ ; and three outputs: PU, PD and RCLK. The  $\overline{VFOE/WF}$  input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When  $\overline{VFOE/WF}$  and WRITE GATE are low, the data recovery circuit is enabled. When the  $\overline{RDD}$  line goes Active Low, the PU or PD signals will become active. If the  $\overline{RDD}$  line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic 1, requesting an increase in VCO frequency. If the  $\overline{RDD}$  line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a decrease in VCO frequency. When the leading edge of  $\overline{RDD}$  occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 ( $\overline{DDEN}=1$ ) or a divide-by-8 ( $\overline{DDEN}=0$ ) of the VCO frequency.

| WG | VFOE/WF | RDD | PU+PD  |
|----|---------|-----|--------|
| 1  | X       | X   | HI-Z   |
| 0  | 1       | X   | HI-Z   |
| 0  | 0       | 1   | HI-Z   |
| 0  | 0       | 0   | Enable |

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case,  $\overline{\Phi 1}$ ,  $\overline{\Phi 2}$ ,  $\overline{\Phi 3}$ ,  $\overline{\Phi 4}$ , and STB should be tied together,  $\overline{DDEN}$  left open, and TG43 tied to ground.

In the double-density mode ( $\overline{DDEN}=0$ ), the signals Early and Late are used to select a phase input ( $\overline{\Phi 1} - \overline{\Phi 4}$ ) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation.  $\overline{\Phi 2}$  is used as the write data pulse on nominal (Early=Late= $\overline{\Phi}$ ),  $\overline{\Phi 2}$  is used for early, and  $\overline{\Phi 3}$  is used for late. The leading edge of  $\overline{\Phi 4}$  resets the STB line in anticipation of the next write data pulse. When TG43=0 or  $\overline{DDEN}=1$ , Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic 1) while  $\overline{DDEN}=0$ .

The signals,  $\overline{DDEN}$ , TG43, and  $\overline{RDD}$  have internal pull-up resistors and may be left open if a logic 1 is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of  $\pm 1V$ ; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and PD signals are affected by the width of the RAW READ ( $\overline{RDD}$ ) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns. ( $\overline{VCO} = 4\text{MHz}$ ,  $\overline{DDEN} = 0$ ) or 500ns. ( $\overline{VCO} = 4\text{MHz}$ ,  $\overline{DDEN} = 1$ ), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature under Bias ..... -25° to 70°C  
 Voltage on any pin with respect to Ground (vss) ..... -0.2 to +7V  
 Power Dissipation ..... 1W

Storage Temp.—Ceramic—65°C to +150°C  
 Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

**DC ELECTRICAL CHARACTERISTICS**

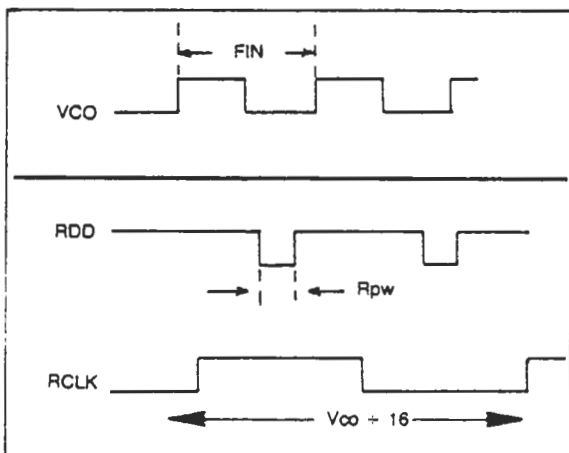
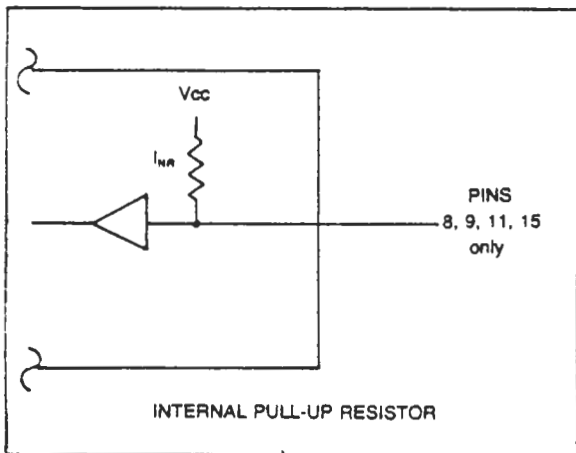
$T_A = \phi$  to 70°C;  $V_{CC} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$

| SYMBOL   | PARAMETER                 | MIN  | TYP | MAX  | UNIT | TEST CONDITIONS      |
|----------|---------------------------|------|-----|------|------|----------------------|
| $V_{IL}$ | Input Low Voltage         | -0.2 |     | +0.8 | V    |                      |
| $V_{IH}$ | Input High Voltage        | 2.0  |     |      | V    |                      |
| $V_{OL}$ | Output Low Voltage        |      |     | 0.45 | V    | $I_{OL} = 3.2MA$     |
| $V_{OH}$ | High Level Output Voltage | 2.4  |     |      | V    | $I_{OH} = -200\mu a$ |
| $V_{CC}$ | Supply Voltage            | 4.5  | 5.0 | 5.5  | V    |                      |
| $I_{CC}$ | Supply Current            |      | 40  | 100  | MA   | All outputs open     |

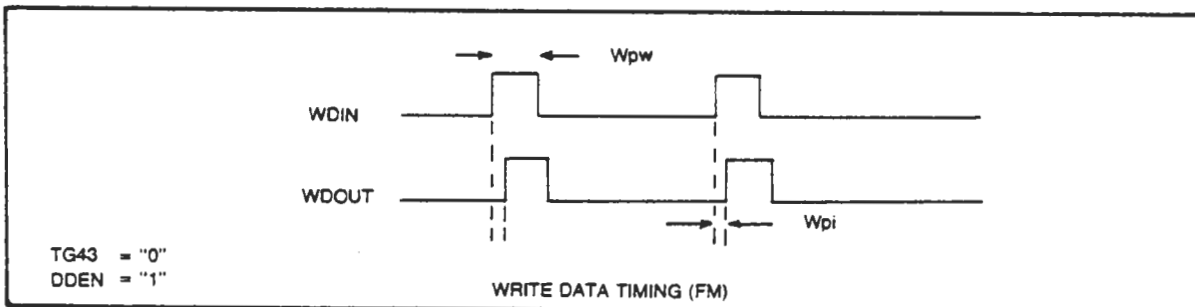
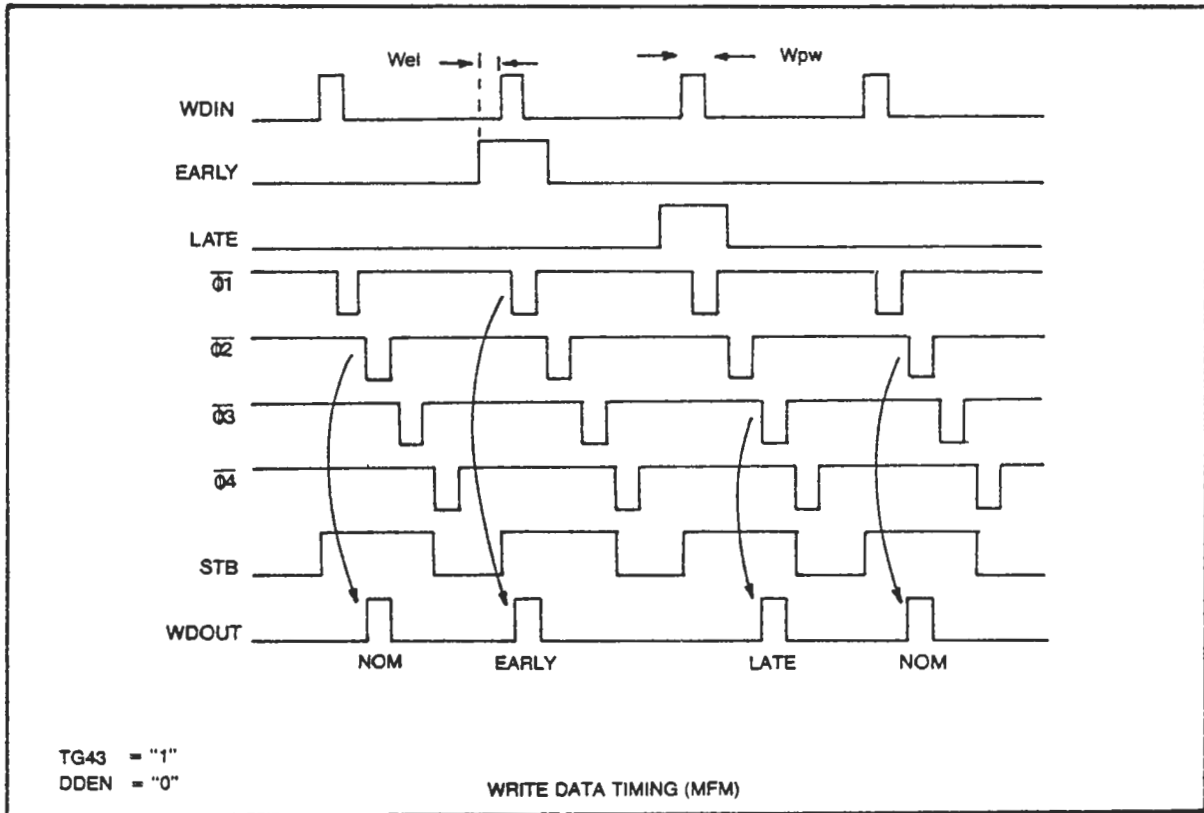
**AC ELECTRICAL CHARACTERISTICS**

$T_A = 0^\circ$  to 70°C;  $V_{CC} = 5V \pm 10\%$ ;  $V_{SS} = 0V$

| SYMBOL   | PARAMETER                    | MIN | TYP | MAX | UNIT       | TEST CONDITIONS       |
|----------|------------------------------|-----|-----|-----|------------|-----------------------|
| $f_{IN}$ | VCO Input Frequency          | .5  | 4   | 6   | MHz        | $\overline{DDEN} = 0$ |
|          |                              | .5  | 2   | 6   | MHz        | $\overline{DDEN} = 1$ |
| $R_{pw}$ | $\overline{RDD}$ Pulse Width | 100 | 200 |     | ns.        |                       |
| $W_{et}$ | EARLY (LATE) to WDIN         | 100 |     |     | ns.        |                       |
| $P_{on}$ | PUMP UP/DN Time              | 0   |     | 250 | ns.        |                       |
| $W_{di}$ | WDIN to WDOUT                |     |     | 80  | ns.        | $\overline{DDEN} = 1$ |
| $I_{NR}$ | Internal Pull-up Resistor    | 4.0 | 6.5 | 10  | K $\Omega$ |                       |







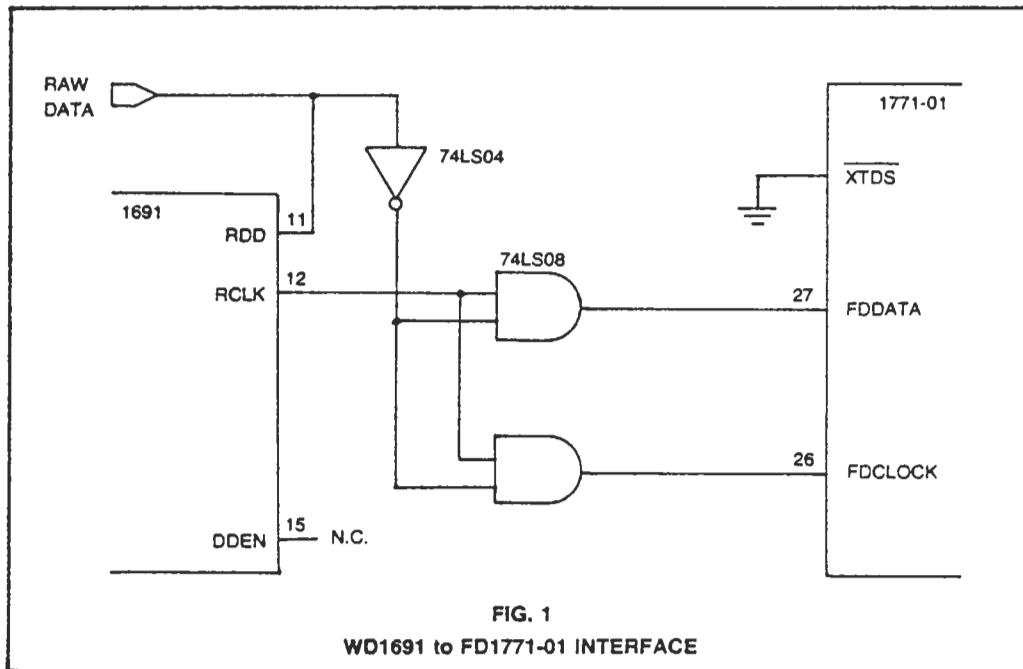
## TYPICAL APPLICATIONS

Figure 1 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 2 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or PD signal, which is integrated by the .33 $\mu$ f capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-01 is also used, providing write precompensation when in double-density, from tracks 44-77. The DDEN line can either be controlled by a toggle switch or a logic level from the host system.

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 ( $\phi$ 1) will be the desired precomp delay from nominal.

The data separator must be adjusted with the  $\overline{\text{RDD}}$  or VFOE/WF line at a Logic 1. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.



## SUBSTITUTING VCO'S

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

- 1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a  $\pm 15\%$  capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about  $\pm 25\%$ , to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.
- 2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is  $-200\mu\text{a}$ . Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of  $-200\mu\text{a}$ .

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

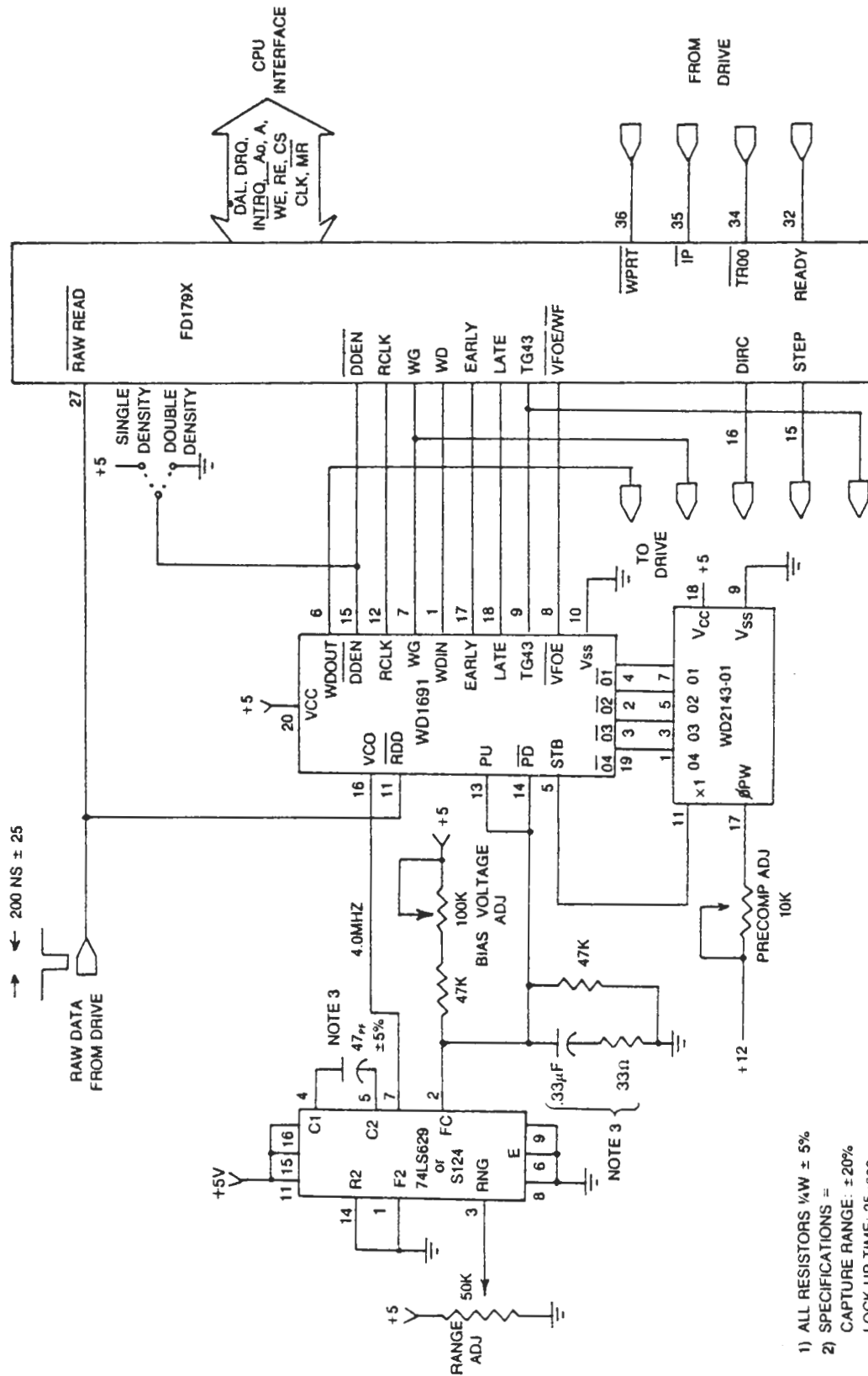
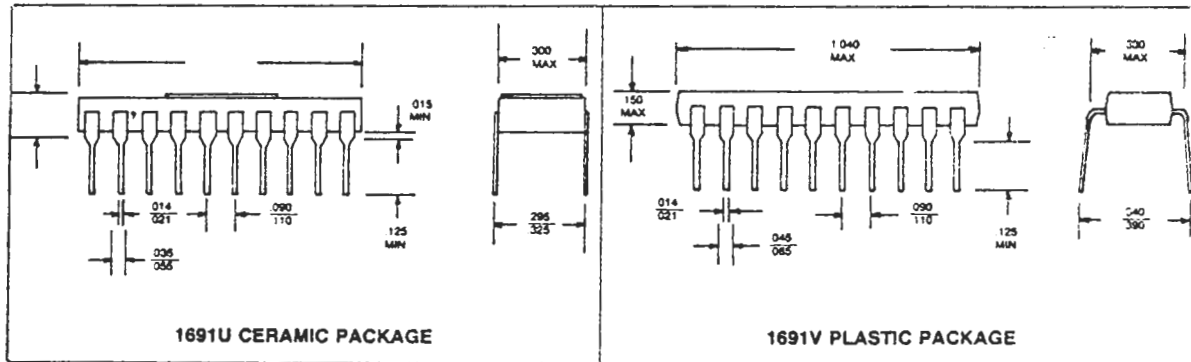


FIG. 2  
8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

- 1) ALL RESISTORS 1/4W ± 5%
- 2) SPECIFICATIONS =  
CAPTURE RANGE: ± 20%  
LOCK-UP TIME: 25µsec  
(ALL ONE'S PATTERN, MFM)
- 3) FOR 5 1/4" 8  
68µf .33µf  
68Ω 33Ω  
80P 47P



This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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# WESTERN DIGITAL

C O R P O R A T I O N

## WD2143-03 Four Phase Clock Generator

### FEATURES

- IMPROVED VERSION OF WD2143-01
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATIBLE
- ON CHIP OSCILLATOR
- TTL CLOCK INPUTS
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR

### GENERAL DESCRIPTION

The WD2143-03 Four-Phase Clock Generator is a MOS/LSI device capable of generating four phase clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the  $\phi$ PW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate  $\phi$ 1PW— $\phi$ 4PW control inputs.

SEPTEMBER, 1981

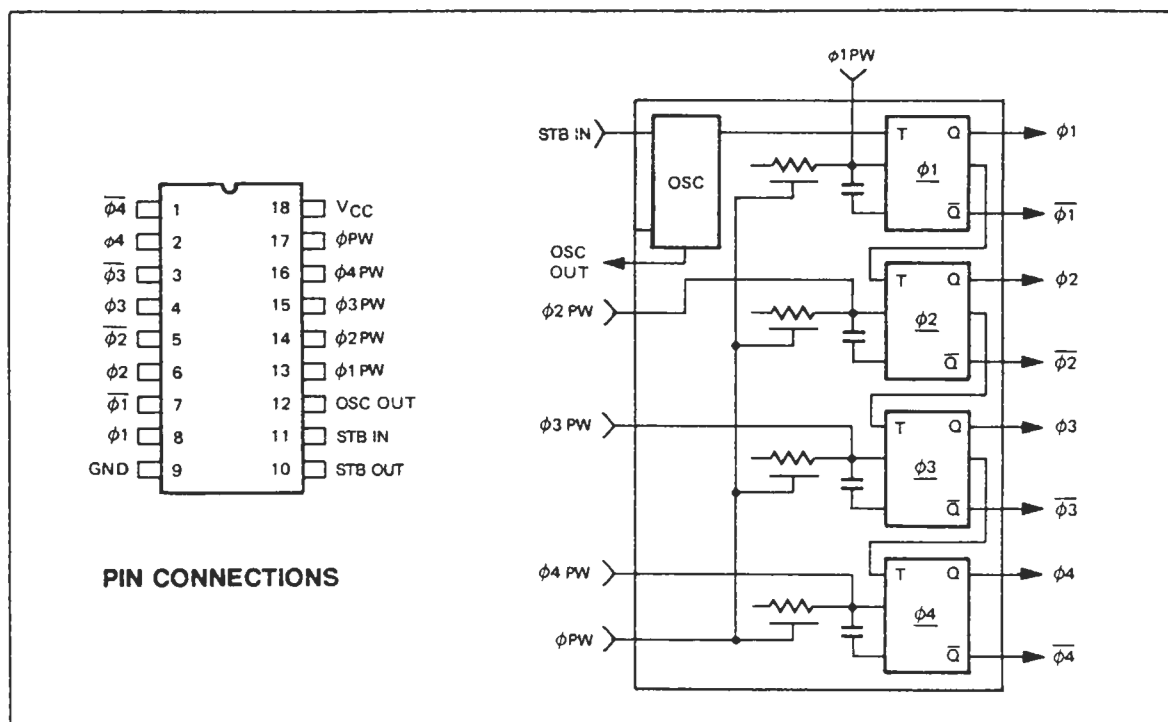


Figure 1 WD2143-03 PIN CONNECTIONS AND BLOCK DIAGRAM

### DEVICE OPERATION

Each of the phase outputs can be controlled individually by tying an external resistor from  $\phi$ 1PW- $\phi$ 4PW to a +5V supply. When it is desired to have  $\phi$ 1 through  $\phi$ 4 outputs the same width, the  $\phi$ 1PW- $\phi$ 4PW inputs should be left open and an external resistor tied from the  $\phi$ PW (Pin 17) input to +12V.

STROBE IN (pin 11) is driven by a TTL square wave with STROBE OUT (pin 10) left open. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

| PIN NUMBER | SYMBOL                                | DESCRIPTION   |
|------------|---------------------------------------|---|
| 1, 3, 5, 7 | $\overline{\phi 1}-\overline{\phi 4}$ | Four phase clock outputs. These outputs are inverted (active low).  |
| 2, 4, 6, 8 | $\phi 1-\phi 4$                       | Four Phase clock outputs. These outputs are true (active high).   |
| 9          | GND                                   | Ground  |
| 10         | STB OUT                               | This pin is left unconnected.   |
| 11         | STB IN                                | Input signal to initiate four-phase clock outputs.  |
| 12         | N.C.                                  | No connection   |
| 13-16      | $\phi 1PW-\phi 4PW$                   | External resistor inputs to control the individual pulse widths of each output. These pins can be left open if $\phi PW$ is used. |
| 17         | $\phi PW$                             | External resistor input to control all phase outputs to the same pulse widths.  |
| 18         | $V_{CC}$                              | +5V $\pm$ 5% power supply input   |

Table 1 PIN DESCRIPTIONS

TYPICAL APPLICATIONS

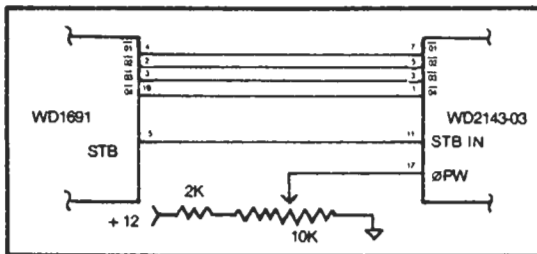


Figure 2 WRITE PRECOMP OPERATION WITH F.S.L. WD1691

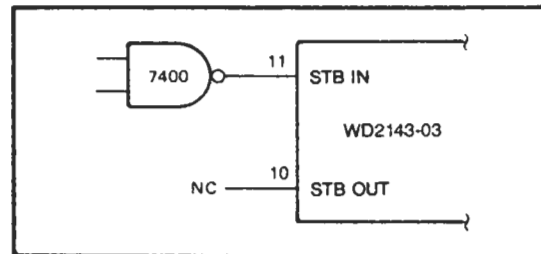


Figure 3 TTL SQUARE WAVE OPERATION

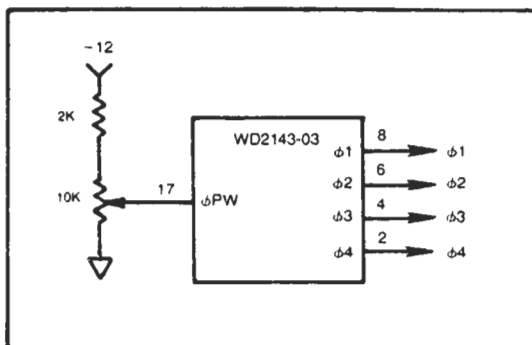


Figure 4 EQUAL PULSE WIDTH OUTPUTS

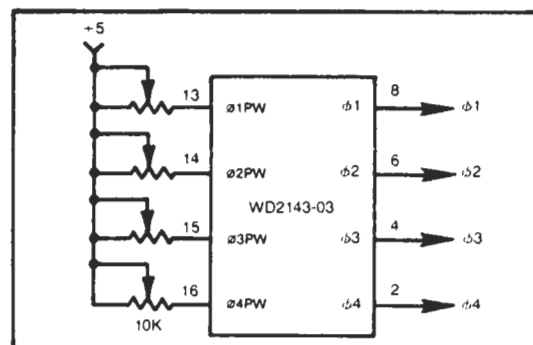


Figure 5 INDIVIDUAL PULSE WIDTH OUTPUTS

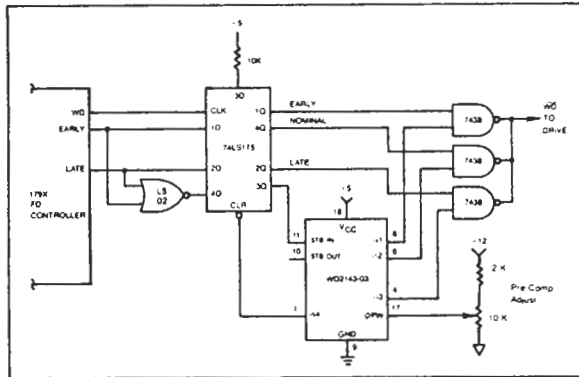


Figure 6 WRITE PRECOMP FOR FLOPPY DISK

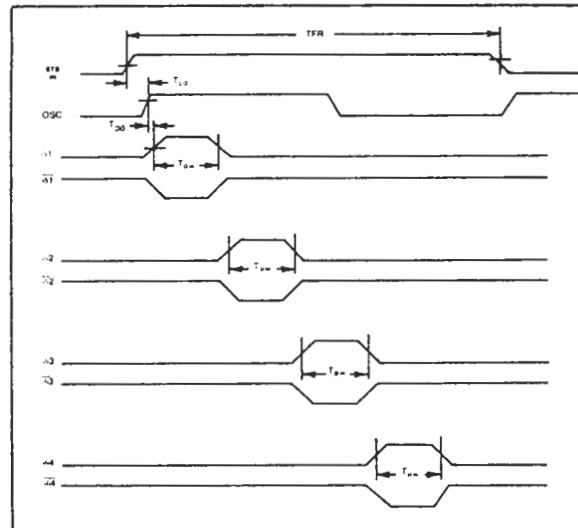


Figure 7 WD2143-03 TIMING DIAGRAM

### SPECIFICATIONS

#### Absolute Maximum Ratings

|  |  |
|--|--|
| Operating Temperature                      | 0° to +70° C                                       |
| Voltage on any pin with respect to Ground* | -0.5 to +7V  |
| Power Dissipation                          | 1 Watt   |
| Storage Temperature                        | plastic -55° to +125° C<br>ceramic -65° to +150° C |

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.

\*Pin 17 = -0.5V to +12V. Increasing voltage on Pin 17 will decrease  $T_{pw}$ .

### DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V \pm 5\%$ ,  $GND = 0V$ ,  $T_A = 0^\circ$  to  $70^\circ C$ .

| SYMBOL   | PARAMETER             | MIN. | MAX. | UNITS | CONDITIONS          |
|----------|-----------------------|------|------|-------|---------------------|
| $V_{ol}$ | TTL low level output  |      | 0.4  | V     | $I_{ol} = 1.6$ ma.  |
| $V_{oh}$ | TTL high level output | 2.4  |      | V     | $I_{oh} = -100$ ua. |
| $V_{il}$ | STB in low voltage    |      | 0.8  | V     |                     |
| $V_{ih}$ | STB in high voltage   | 2.4  |      | V     |                     |
| $I_{cc}$ | Supply Current        |      | 80   | ma    | All outputs open    |

Table 2 DC ELECTRICAL CHARACTERISTICS

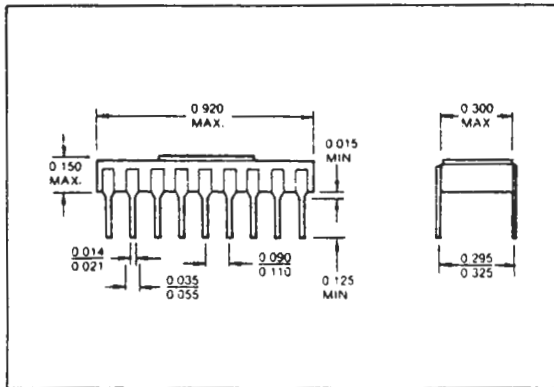
**SWITCHING CHARACTERISTICS**

$V_{CC} = 5V \pm 5\%$ ,  $GND = 0V$   $T_A = 0^\circ$  to  $70^\circ C$

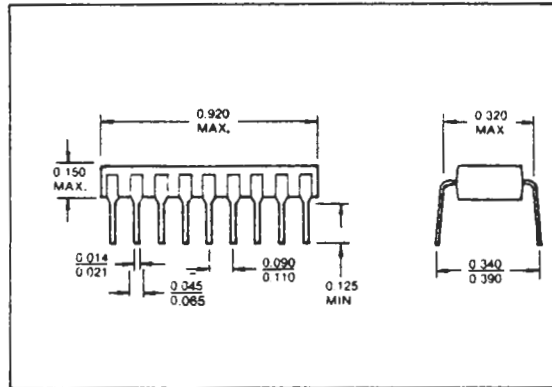
| SYMBOL    | PARAMETER                        | MIN. | MAX. | UNITS | CONDITIONS                  |
|-----------|----------------------------------|------|------|-------|-----------------------------|
| $T_{cd}$  | STB IN to OSC out ( $\uparrow$ ) |      | 70   | NS    |                             |
| $T_{pd}$  | STB OUT to $\phi 1$              |      | 70   | NS    |                             |
| $T_{pw}$  | Pulse Width (any output)         | 100  | 300  | NS    | $CL = 30pf$                 |
| $T_{pr}$  | Rise Time (any output)           |      | 30   | NS    | $CL = 30 pf$                |
| $T_{pf}$  | Fall Time (any output)           |      | 25   | NS    | $CL = 30 pf$                |
| TFR       | STROBE Frequency                 |      | 2.5  | MHz   | combined $T_{pw} = 400 NS.$ |
| $T_{dpw}$ | Pulse Width Differential         |      | 10   | %     | 100-300 NS.                 |

**Table 3 SWITCHING CHARACTERISTICS**

NOTE:  $T_{pw}$  measured at 50%  $V_{OH}$  Point;  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$



**WD2143L-03 CERAMIC PACKAGE**



**WD2143M-03 PLASTIC PACKAGE**

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

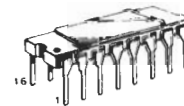
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# MCM6633

**MOS**  
(IN-CHANNEL, SILICON-GATE)  
**32,768-BIT**  
**DYNAMIC RANDOM ACCESS**  
**MEMORY**



L SUFFIX  
CERAMIC PACKAGE  
CASE 690

## 32,768-BIT DYNAMIC RAM

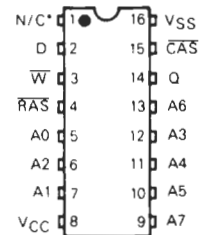
The MCM6633 is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6633 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6633 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 32,768 Words of 1 Bit
- Single + 5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation  
275 mW Maximum (Active)  
30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4516, MCM4517)
- One Half of the 64K RAM MCM6665
- The Operating Half of the MCM6633 is Indicated by Device Marking:  
MCM66330 Tie A7  $\overline{\text{CAS}}$  (A15) Low "0"  
MCM66331 Tie A7  $\overline{\text{CAS}}$  (A15) High "1"

### PIN ASSIGNMENT

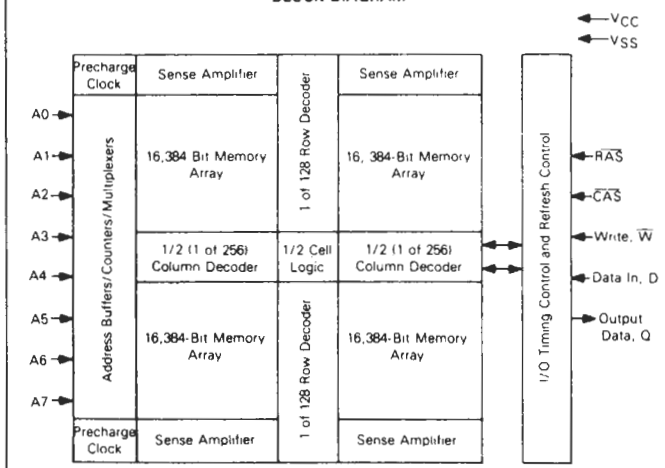


\*For maximum compatibility with MCM6632 and MCM6664, a  $V_{CC}$  trace should go to pin #1.

### PIN NAMES

|                         |                       |
|-------------------------|-----------------------|
| A0-A7                   | Address Input         |
| D                       | Data In               |
| Q                       | Data Out              |
| W                       | Read/Write Input      |
| $\overline{\text{RAS}}$ | Row Address Strobe    |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| $V_{CC}$                | Power (+ 5 V)         |
| $V_{SS}$                | Ground                |

### BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

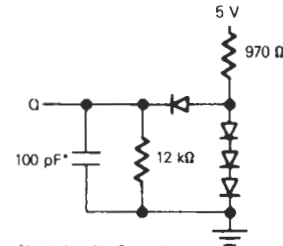
## MCM6633

## ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating   | Symbol                             | Value       | Unit |
|--|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V <sub>SS</sub> (Except V <sub>CC</sub> ) | V <sub>in</sub> , V <sub>out</sub> | -2 to +7    | V    |
| Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>            | V <sub>in</sub> , V <sub>out</sub> | -1 to +7    | V    |
| Operating Temperature Range  | T <sub>A</sub>                     | 0 to +70    | °C   |
| Storage Temperature Range  | T <sub>stg</sub>                   | -65 to +150 | °C   |
| Power Dissipation  | P <sub>D</sub>                     | 1           | W    |
| Data Out Current   | I <sub>out</sub>                   | 50          | mA   |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



\*Includes Jig Capacitance

### DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

## RECOMMENDED OPERATING CONDITIONS

| Parameter                   | Symbol                    | Min             | Typ  | Max | Unit | Notes |   |
|-----------------------------|---------------------------|-----------------|------|-----|------|-------|---|
| Supply Voltage              | MCM6633L15/MCM6633L20     | V <sub>CC</sub> | 4.5  | 5.0 | 5.5  | Vdc   | 1 |
|                             | MCM6633L15-5/MCM6633L20-5 | V <sub>CC</sub> | 4.75 | 5.0 | 5.25 |       |   |
|                             | V <sub>SS</sub>           | 0               | 0    | 0   |      |       |   |
| Logic 1 Voltage, All Inputs | V <sub>IH</sub>           | 2.4             | —    | 7.0 | Vdc  | 1     |   |
| Logic 0 Voltage             | V <sub>IL</sub>           | -2.0            | —    | 0.8 | Vdc  | 1     |   |

## DC CHARACTERISTICS

| Characteristic   | Symbol            | Min | Max | Units | Notes |
|--|-------------------|-----|-----|-------|-------|
| V <sub>CC</sub> Power Supply Current (I <sub>RC</sub> min.)                  | I <sub>CC1</sub>  | —   | 50  | mA    | 4     |
| Standby V <sub>CC</sub> Power Supply Current                                 | I <sub>CC2</sub>  | —   | 5   | mA    | 5     |
| V <sub>CC</sub> Power Supply Current During RAS Only Refresh Cycles          | I <sub>CC3</sub>  | —   | 40  | mA    | —     |
| Input Leakage Current (any input) (0 ≤ V <sub>in</sub> ≤ 5.5) (Except Pin 1) | I <sub>I(L)</sub> | —   | 10  | μA    | —     |
| Output Leakage Current (0 ≤ V <sub>out</sub> ≤ 5.5) (CAS at Logic 1)         | I <sub>O(L)</sub> | —   | 10  | μA    | —     |
| Output Logic 1 Voltage @ I <sub>out</sub> = -4 mA                            | V <sub>OH</sub>   | 2.4 | —   | V     | —     |
| Output Logic 0 Voltage @ I <sub>out</sub> = 4 mA                             | V <sub>OL</sub>   | —   | 0.4 | V     | —     |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)  
(Read, Write, and Read-Modify-Write Cycles)  
(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

| Parameter                                  | Symbol           | MCM6633-15 |       | MCM6633-20 |       | Units | Notes  |
|--|------------------|------------|-------|------------|-------|-------|--------|
|  |                  | Min        | Max   | Min        | Max   |       |        |
| Random Read or Write Cycle Time            | t <sub>RC</sub>  | 300        | —     | 350        | —     | ns    | 8, 9   |
| Read Write Cycle Time                      | t <sub>RWC</sub> | 300        | —     | 350        | —     | ns    | 8, 9   |
| Access Time from Row Address Strobe        | t <sub>RAC</sub> | —          | 150   | —          | 200   | ns    | 10, 12 |
| Access Time from Column Address Strobe     | t <sub>CAC</sub> | —          | 75    | —          | 110   | ns    | 11, 12 |
| Output Buffer and Turn-Off Delay           | t <sub>OFF</sub> | 0          | 30    | 0          | 40    | ns    | 17     |
| Row Address Strobe Precharge Time          | t <sub>RP</sub>  | 120        | —     | 140        | —     | ns    | —      |
| Row Address Strobe Pulse Width             | t <sub>RAS</sub> | 150        | 10000 | 200        | 10000 | ns    | —      |
| Column Address Strobe Pulse Width          | t <sub>CAS</sub> | 75         | 10000 | 110        | 10000 | ns    | —      |
| Row to Column Strobe Lead Time             | t <sub>RCD</sub> | 30         | 75    | 35         | 90    | ns    | 13     |
| Row Address Setup Time                     | t <sub>ASR</sub> | 0          | —     | 0          | —     | ns    | —      |
| Row Address Hold Time                      | t <sub>RAH</sub> | 25         | —     | 30         | —     | ns    | —      |
| Column Address Setup Time                  | t <sub>ASC</sub> | 0          | —     | 0          | —     | ns    | —      |
| Column Address Hold Time                   | t <sub>CAH</sub> | 45         | —     | 55         | —     | ns    | —      |
| Column Address Hold Time Referenced to RAS | t <sub>AR</sub>  | 120        | —     | 155        | —     | ns    | —      |
| Transition Time (Rise and Fall)            | t <sub>T</sub>   | 3          | 50    | 3          | 50    | ns    | 6      |

## MCM6633

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

| Parameter   | Symbol            | MCM6633-15 |     | MCM6633-20 |     | Units | Notes |
|---|-------------------|------------|-----|------------|-----|-------|-------|
|   |                   | Min        | Max | Min        | Max |       |       |
| Read Command Setup Time                                       | t <sub>RCS</sub>  | 0          | —   | 0          | —   | ns    | —     |
| Read Command Hold time  | t <sub>RCH</sub>  | 10         | —   | 10         | —   | ns    | 14    |
| Read Command Hold Time Referenced to $\overline{\text{RAS}}$  | t <sub>RRH</sub>  | 30         | —   | 35         | —   | ns    | 14    |
| Write Command Hold Time                                       | t <sub>WCH</sub>  | 45         | —   | 55         | —   | ns    | —     |
| Write Command Hold Time Referenced to $\overline{\text{RAS}}$ | t <sub>WCR</sub>  | 120        | —   | 155        | —   | ns    | —     |
| Write Command Pulse Width                                     | t <sub>WP</sub>   | 45         | —   | 55         | —   | ns    | —     |
| Write Command to Row Strobe Lead Time                         | t <sub>RWL</sub>  | 45         | —   | 55         | —   | ns    | —     |
| Write Command to Column Strobe Lead Time                      | t <sub>CWL</sub>  | 45         | —   | 55         | —   | ns    | —     |
| Data in Setup Time  | t <sub>DS</sub>   | 0          | —   | 0          | —   | ns    | 15    |
| Data in Hold Time   | t <sub>DH</sub>   | 45         | —   | 55         | —   | ns    | 15    |
| Data in Hold Time Referenced to $\overline{\text{RAS}}$       | t <sub>DHR</sub>  | 120        | —   | 155        | —   | ns    | —     |
| Column to Row Strobe Precharge Time                           | t <sub>CRP</sub>  | -10        | —   | -10        | —   | ns    | —     |
| $\overline{\text{RAS}}$ Hold Time                             | t <sub>RSH</sub>  | 75         | —   | 110        | —   | ns    | —     |
| Refresh Period  | t <sub>RFSH</sub> | —          | 2.0 | —          | 2.0 | ms    | —     |
| $\overline{\text{WRITE}}$ Command Setup Time                  | t <sub>WCS</sub>  | -10        | —   | -10        | —   | ns    | 16    |
| $\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay    | t <sub>CWD</sub>  | 45         | —   | 55         | —   | ns    | 16    |
| $\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay    | t <sub>RWD</sub>  | 125        | —   | 160        | —   | ns    | 16    |
| $\overline{\text{CAS}}$ Hold Time                             | t <sub>CSH</sub>  | 150        | —   | 200        | —   | ns    | —     |

CAPACITANCE (f = 1.0 MHz, T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5 V Periodically Sampled Rather Than 100% Tested)

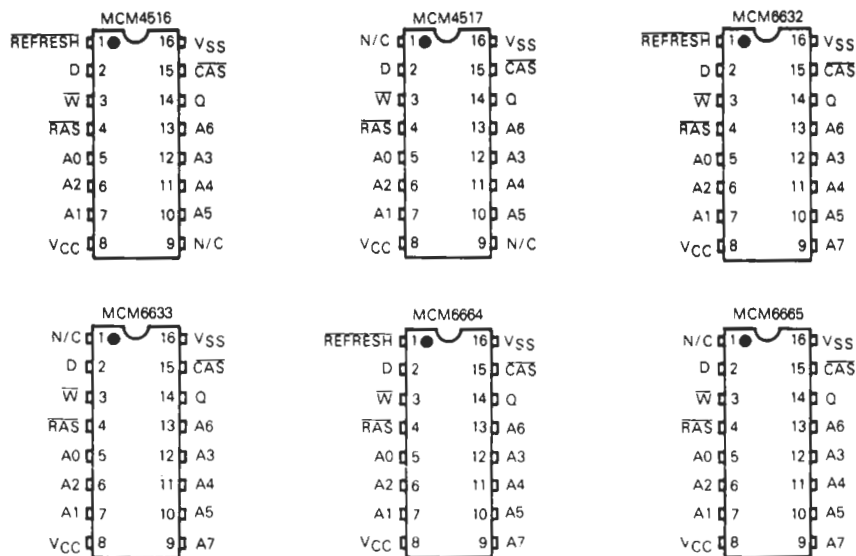
| Parameter   | Symbol          | Typ | Max | Units | Notes |
|---|-----------------|-----|-----|-------|-------|
| Input Capacitance (A0-A7), D  | C <sub>I1</sub> | 4   | 5   | pF    | 7     |
| Input Capacitance $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$ | C <sub>I2</sub> | 8   | 10  | pF    | 7     |
| Output Capacitance (Q) ( $\overline{\text{CAS}} = V_{IH}$ to disable output)                    | C <sub>O</sub>  | 5   | 7   | pF    | 7     |

## NOTES:

- All voltages referenced to V<sub>SS</sub>.
- V<sub>IH</sub> min and V<sub>IL</sub> max are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub>.
- An initial pause of 100  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation guaranteed.
- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Output is disabled (open-circuit) and  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are both at a logic 1.
- The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = \frac{I_{\Delta t}}{\Delta V}$
- The specifications for t<sub>RC</sub> (min), and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C  $\leq$  T<sub>A</sub>  $\leq$  70°C) is assured.
- AC measurements assume t<sub>T</sub> = 5.0 ns.
- Assumes that t<sub>RCD</sub>  $\leq$  t<sub>RCD</sub> (max).
- Assumes that t<sub>RCD</sub>  $\geq$  t<sub>RCD</sub> (max).
- Measured with a current load equivalent to 2 TTL loads (+200  $\mu$ A, -4 mA) and 100 pF (V<sub>OH</sub> = 2.0 V, V<sub>OL</sub> = -0.8 V)
- Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
- Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.
- These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in random write cycles and to  $\overline{\text{WRITE}}$  leading edge in delayed write or read-modify-write cycles.
- t<sub>WCS</sub>, t<sub>CWD</sub>, and t<sub>RWD</sub> are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if t<sub>WCS</sub>  $\geq$  t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t<sub>CWD</sub>  $\geq$  t<sub>CWD</sub> (min) and t<sub>RWD</sub>  $\geq$  t<sub>RWD</sub> (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- t<sub>off</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

### MCM6633

#### PIN ASSIGNMENT COMPARISON



#### PIN VARIATIONS

| Pin Number | MCM4116                  | MCM4516 | MCM4517 | MCM6632 | MCM6663 | MCM6664 | MCM6665 |
|------------|--------------------------|---------|---------|---------|---------|---------|---------|
| 1          | V <sub>BB</sub> (-5 V)   | REFRESH | N/C     | REFRESH | N/C     | REFRESH | N/C     |
| 8          | V <sub>DDI</sub> (+12 V) | VCC     | VCC     | VCC     | VCC     | VCC     | VCC     |
| 9          | V <sub>CC</sub> (+5 V)   | N/C     | N/C     | A7      | A7      | A7      | A7      |

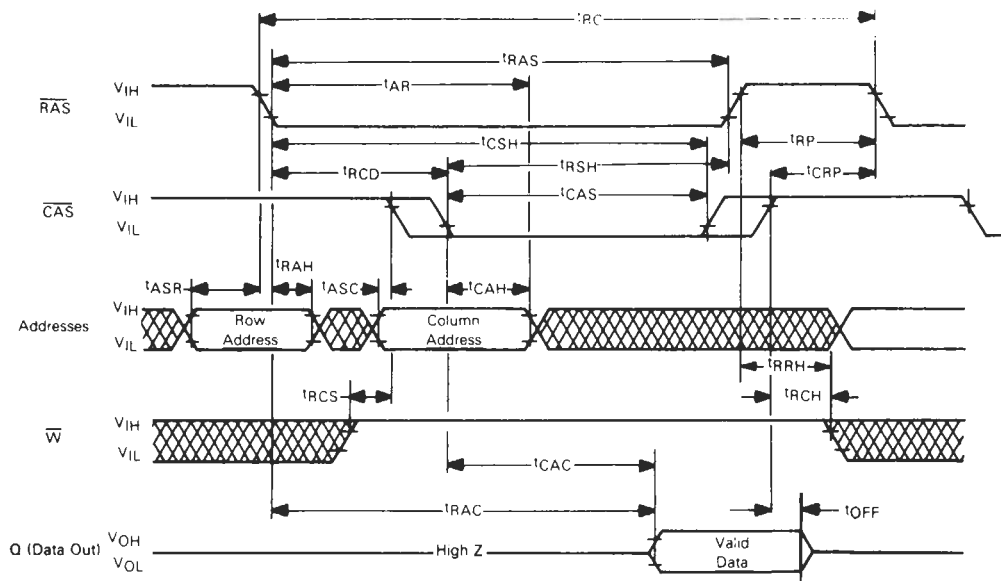
#### ORDERING INSTRUCTIONS

| PART NUMBER | DESCRIPTION                             | SPEED | MARKING*          |
|-------------|---|-------|-------------------|
| MCM6633L15  | 32K RAM<br>Sidebrazed<br>Package<br>"L" | 150   | 66330L15/66331L15 |
| MCM66330L15 |   | 150   | 66330L15          |
| MCM66331L15 |   | 150   | 66331L15          |
| MCM6633L20  |   | 200   | 66330L20/66331L20 |
| MCM66330L20 |   | 200   | 66330L20          |
| MCM66331L20 |   | 200   | 66331L20          |

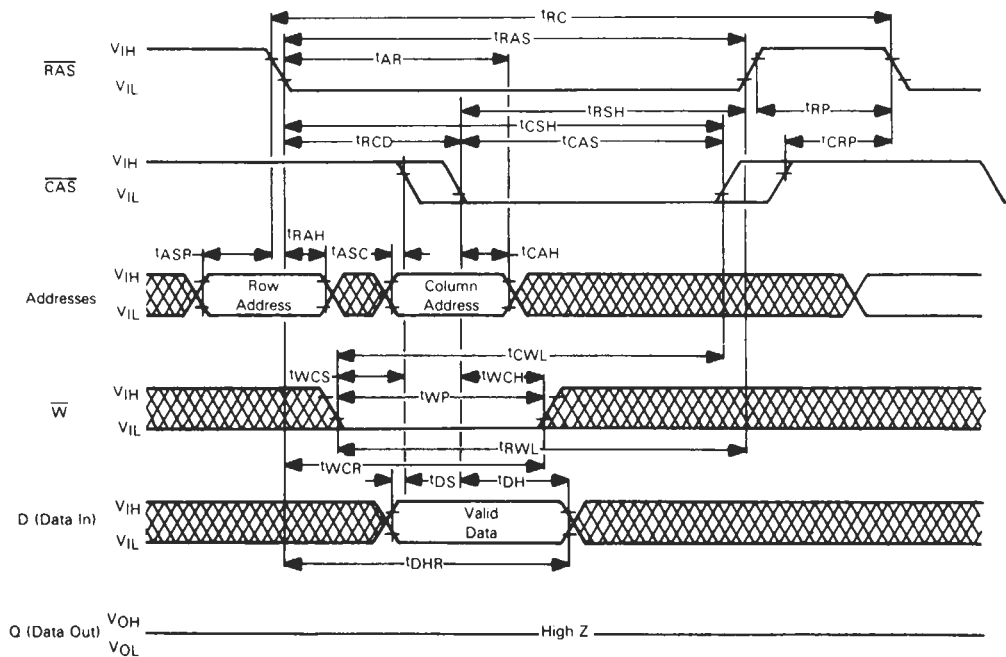
\*MCM66330L20 = Tie A7  $\overline{CAS}$  (A15) Low "0"  
MCM66331L20 = Tie A7  $\overline{CAS}$  (A15) High "1"

MCM6633

READ CYCLE TIMING

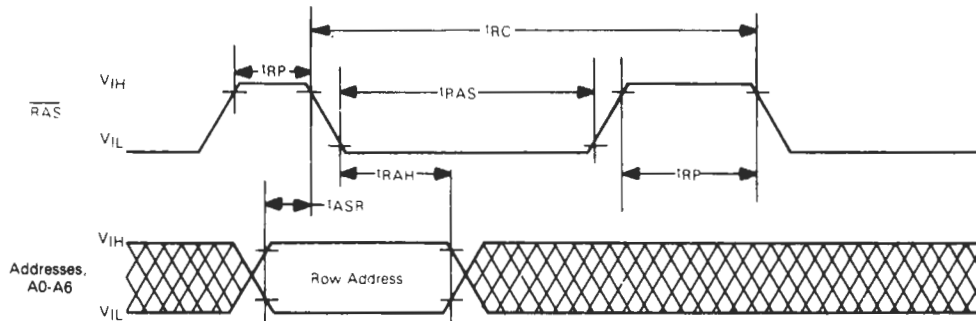


WRITE CYCLE TIMING

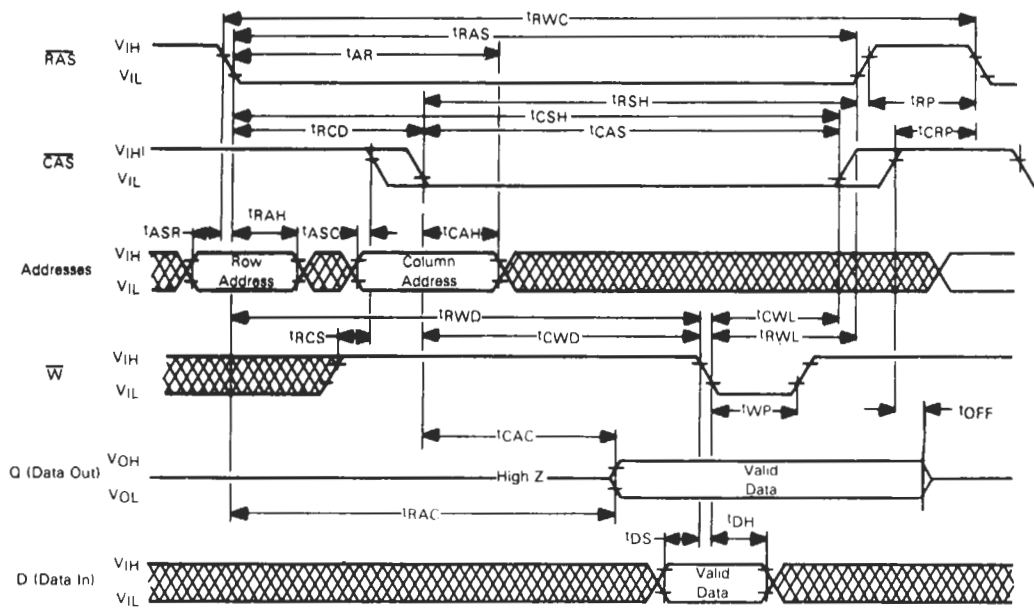


MCM6633

RAS-ONLY REFRESH CYCLE  
(Data-in and Write are Don't Care, CAS is HIGH)

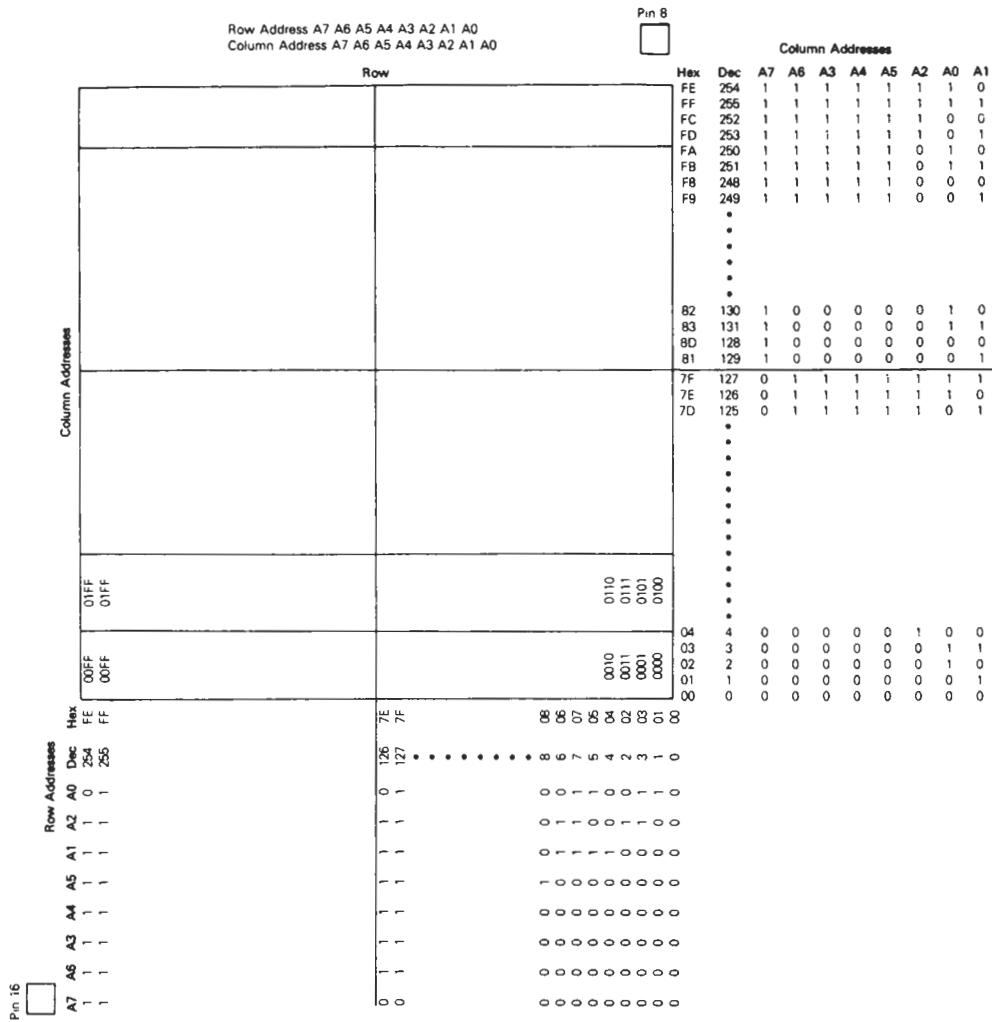


READ-WRITE/READ-MODIFY-WRITE CYCLE



MCM6633

MCM6685 BIT ADDRESS MAP



Data Stored = D<sub>in</sub> • A<sub>0X</sub> • A<sub>1Y</sub>

| Column Address A1 | Row Address A0 | Data Stored |
|-------------------|----------------|-------------|
| 0                 | 0              | Inverted    |
| 0                 | 1              | True        |
| 1                 | 0              | True        |
| 1                 | 1              | Inverted    |

