

# CMOS Logic Data

ON Semiconductor



# CMOS Logic Data

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This book presents technical data for the broad line of CMOS logic integrated circuits and demonstrates ON Semiconductor's continued commitment to Metal-Gate CMOS. Complete specifications are provided in the form of data sheets. In addition, a Product Selector Guide and a Handling and Design Guidelines chapter have been included to familiarize the user with these circuits.

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## **CHAPTER 3**

# **Reliability Audit Program**

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# **“RAP”**

## **Reliability Audit Program For Logic Integrated Circuits**

### **1.0 INTRODUCTION**

The Reliability Audit Program developed in March 1977 is the ON Semiconductor internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are available at all sales offices. Also available is the

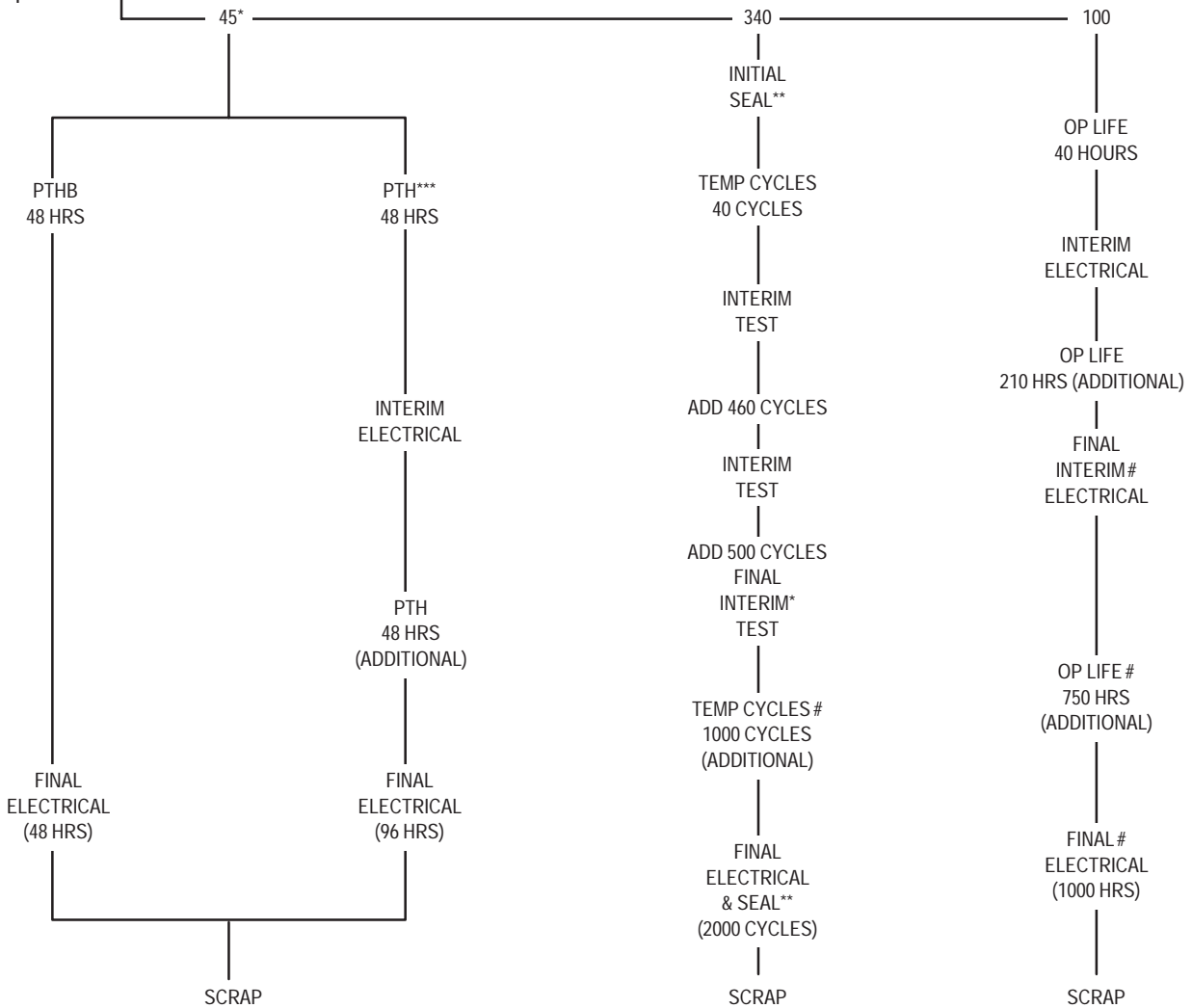
“Reliability and Quality Handbook” which contains data for all ON Semiconductor devices (HBD851/D).

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.



## 2.0 RAP TEST FLOW

Pull 500\* piece sample from lot following Group A acceptance.



#One sample per month for FAST, LS, 10H, 10K, MG CMOS, and HSL CMOS.

\* PTHB or PTH not required for hermetic products: reduce total sample size to 450 pcs.

\*\* Seal (Fine & Gross Leak) required only for hermetic products.

\*\*\* PTH to be used when sockets for PTHB are not available.

## 3.0 TEST CONDITIONS AND COMMENTS

**PTHB** — 15 psig/121°C/100% RH at rated  $V_{CC}$  or  $V_{EE}$  — to be performed on plastic encapsulated devices only.

**TEMP CYCLING** — MIL-STD-883, Method 1010, Condition C, - 65°C/+ 150°C.

**OP LIFE** — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias),  $T_A = 145^\circ\text{C}$ .

### NOTES:

- All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
- Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.

3. Sampling to include all package types routinely.

4. Device types sampled will be by generic type within each logic I/C product family (CMOS, TTL, etc.) and will include all assembly locations (Korea, Philippines, Malaysia, etc.).

5. 16 hrs. PTHB is equivalent to approximately 800 hours of 85°C/85% RH THB for  $V_{CC} \leq 15\text{ V}$ .

6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.

7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

## **CHAPTER 4**

### **B and UB Series Family Data**

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# B AND UB SERIES FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized\* family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- 3–18 volt operational limits
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range
- Direct Interface to High-Speed CMOS
- Maximum input current of  $\pm 1 \mu\text{A}$  at 15 volt power supply over the temperature range
- Parameters specified at 5.0, 10, and 15 volt supply
- Noise margins: B Series
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10 V supply
  - 2.5 V min @ 15 V supply
- UB Series
  - 0.5 V min @ 5.0 V supply
  - 1.0 V min @ 10 V supply
  - 1.0 V min @ 15 V supply

The industry-standardized maximum ratings are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent ON Semiconductor format. The ON Semiconductor format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

- Load Capacitance,  $C_L$ , of 50 pF
- Input Voltage equal to  $V_{SS} - V_{DD}$  (Rail-to-Rail swing)
- Input pulse rise and fall times of 20 ns
- Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage
- Three different supply voltages: 5, 10, and 15 V

## Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose inputs and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

- Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

## Input Voltage

The input voltage specification is interpreted as the worstcase input voltage to produce an output level of “1” or “0”. This “1” or “0” output level is defined as a deviation from the supply ( $V_{DD}$ ) and ground ( $V_{SS}$ ) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

## Noise Margin

The values for input voltages and the defined output deviations lead to the calculated noise margins. Noise margin is defined as the difference between  $V_{IL}$  or  $V_{IH}$  and  $V_{out}$  (output deviation). As an example, for a noninverting buffer at  $V_{DD} = 5.0$  volts:  $V_{IL} = 1.5$  volts and  $V_{out} = 0.5$  volts. Therefore, Noise Margin equals  $V_{IL} - V_{out} = 1.0$  volt. This figure is useful while cascading stages (See Figure 1). With the input to the first stage at a worst-case voltage level ( $V_{IL} = 1.5$  V), the output is guaranteed to be no greater than 0.5 volts with a 5.0 volt supply. Since the maximum allowable logic 0 for the second stage is 1.5 volts, this 0.5 volt output provides a 1.0 volt margin for noise to the next stage.

## Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one low-power Schottky TTL input.

## B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a “Linear” mode to form oscillators, monostables, or amplifiers. The decreased gain results in increased stability and a “cleaner” output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed, since only a single stage is involved.

The B and UB series, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices, such as High-Speed CMOS Logic.

\* Specifications coordinated by EIA/JEDEC Solid-State Products Council.

**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameters	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient), per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

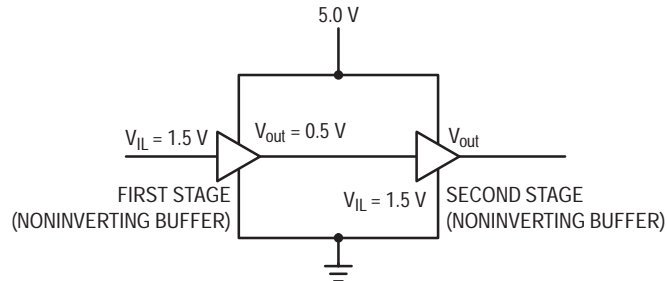


Figure 1.

Table 1. EIA/JEDEC Format for CMOS Industry B and UB Series Specifications

**ELECTRICAL CHARACTERISTICS**

Parameter	Temp Range	$V_{DD}$ (Vdc)	Conditions	Limits						Units				
				$T_{LOW}^*$		+ 25°C		$T_{HIGH}^*$						
				Min	Max	Min	Max	Min	Max					
$I_{DD}$ Quiescent Device Current	GATES	Mil 5 10 15	$V_{in} = V_{SS}$ or $V_{DD}$		0.25 0.5 1.0		0.25 0.5 1.0		7.5 15 30	$\mu$ Adc				
				Comm	5 10 15	All valid input combinations		1.0 2.0 4.0		1.0 2.0 4.0		7.5 15 30	$\mu$ Adc	
							BUFFERS, FLIP-FLOPS	Mil 5 10 15	$V_{IN} = V_{SS}$ or $V_{DD}$		1.0 2.0 4.0		1.0 2.0 4.0	
	Comm	5 10 15	All valid input combinations		4 8 16					4.0 8.0 16.0		30 60 120	$\mu$ Adc	
				MSI	Mil 5 10 15	$V_{IN} = V_{SS}$ or $V_{DD}$					5 10 20		5 10 20	
	Comm	5 10 15	All valid input combinations					20 40 80		20 40 80		150 300 600	$\mu$ Adc	
$V_{OL}$							All	5 10 15	$V_{IN} = V_{SS}$ or $V_{DD}$ $ I_O  < 1 \mu A$		0.05 0.05 0.05		0.05 0.05 0.05	
	$V_{OH}$	All	5 10 15	$V_{IN} = V_{SS}$ or $V_{DD}$ $ I_O  < 1 \mu A$		4.95 9.95 14.95					4.95 9.95 14.95		4.95 9.95 14.95	Vdc

Table 1. EIA/JEDEC Format for CMOS Industry B and UB Series Specifications (continued)

ELECTRICAL CHARACTERISTICS

Parameter		Temp Range	V <sub>DD</sub> (Vdc)	Conditions	Limits						Units
					T <sub>LOW</sub> *		+ 25°C		T <sub>HIGH</sub> *		
					Min	Max	Min	Max	Min	Max	
V <sub>IL</sub>	Input Low Voltage# B Types	All	5	V <sub>O</sub> = 0.5V or 4.5V		1.5		1.5		1.5	Vdc
			10	V <sub>O</sub> = 1.0V or 9.0V		3.0		3.0		3.0	
			15	V <sub>O</sub> = 1.5V or 13.5V  I <sub>O</sub>   < 1 μA		4.0		4.0		4.0	
V <sub>IL</sub>	Input Low Voltage# UB Types	All	5	V <sub>O</sub> = 0.5V or 4.5V		1.0		1.0		1.0	
			10	V <sub>O</sub> = 1.0V or 9.0V		2.0		2.0		2.0	
			15	V <sub>O</sub> = 1.5V or 13.5V  I <sub>O</sub>   < 1 μA		2.5		2.5		2.5	
V <sub>IH</sub>	Input High Voltage# B Types	All	5	V <sub>O</sub> = 0.5V or 4.5V	3.5		3.5		3.5		Vdc
			10	V <sub>O</sub> = 1.0V or 9.0V	7.0		7.0		7.0		
			15	V <sub>O</sub> = 1.5V or 13.5V  I <sub>O</sub>   < 1 μA	11.0		11.0		11.0		
V <sub>IH</sub>	Input High Voltage# UB Types	All	5	V <sub>O</sub> = 0.5V or 4.5V	4.0		4.0		4.0		Vdc
			10	V <sub>O</sub> = 1.0V or 9.0V	8.0		8.0		8.0		
			15	V <sub>O</sub> = 1.5V or 13.5V  I <sub>O</sub>   < 1 μA	12.5		12.5		12.5		
I <sub>OL</sub>	Output Low (Sink) Current	Mil	5	V <sub>O</sub> = 0.4V, V <sub>IN</sub> = 0 or 5V	0.64		0.51		0.36		mAdc
			10	V <sub>O</sub> = 0.5V, V <sub>IN</sub> = 0 or 10V	1.6		1.3		0.9		
			15	V <sub>O</sub> = 1.5V, V <sub>IN</sub> = 0 or 15V	4.2		3.4		2.4		
		Com	5	V <sub>O</sub> = 0.4V, V <sub>IN</sub> = 0 or 5V	0.52		0.44		0.36		mAdc
			10	V <sub>O</sub> = 0.5V, V <sub>IN</sub> = 0 or 10V	1.3		1.1		0.9		
			15	V <sub>O</sub> = 1.5V, V <sub>IN</sub> = 0 or 15V	3.6		3.0		2.4		
I <sub>OH</sub>	Output High (Source) Current	Mil	5	V <sub>O</sub> = 4.6V, V <sub>IN</sub> = 0 or 5V	-0.25		-0.2		-0.14		mAdc
			10	V <sub>O</sub> = 9.5V, V <sub>IN</sub> = 0 or 10V	-0.62		-0.5		-0.35		
			15	V <sub>O</sub> = 13.5V, V <sub>IN</sub> = 0 or 15V	-1.8		-1.5		-1.1		
		Com	5	V <sub>O</sub> = 4.6V, V <sub>IN</sub> = 0 or 5V	-0.2		-0.16		-0.12		mAdc
			10	V <sub>O</sub> = 9.5V, V <sub>IN</sub> = 0 or 10V	-0.5		-0.4		-0.3		
			15	V <sub>O</sub> = 13.5V, V <sub>IN</sub> = 0 or 15V	-1.4		-1.2		-1.0		
I <sub>IN</sub>	Input Current	Mil Comm	15	V <sub>IN</sub> = 0 or 15V		± 0.1		± 0.1		± 1.0	μAdc μAdc
			15	V <sub>IN</sub> = 0 or 15V		± 0.3		± 0.3		± 1.0	
I <sub>oz</sub>	3-State Output Leakage Current	Mil Comm	15	V <sub>IN</sub> = 0 or 15V		± 0.4		± 0.4		± 12	μAdc μAdc
			15	V <sub>IN</sub> = 0 or 15V		± 1.6		± 1.6		± 12	
C <sub>IN</sub>	Input Capacitance per unit load	All	—	Any Input				7.5		pF	

\* T<sub>LOW</sub> = - 55°C for Military temperature range device, - 40°C for Commercial temperature range device.

T<sub>HIGH</sub> = + 125°C for Military temperature range device, + 85°C for Commercial temperature range device.

#Applies for Worst Case input combinations.

Table 2. ON Semiconductor Format for CMOS Industry B and UB Series Specifications

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C		+ 125°C		Unit
			Min	Max	Min	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0.05	—	0.05	Vdc
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
Input Voltage B Types (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	1.5	—	1.5	Vdc
		10	—	3.0	—	3.0	—	3.0	
		15	—	4.0	—	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	—	3.5	—	
		10	7.0	—	7.0	—	7.0	—	
		15	11	—	11	—	11	—	
Input Voltage UB Types (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	1.0	—	1.0	Vdc
		10	—	2.0	—	2.0	—	2.0	
		15	—	2.5	—	2.5	—	2.5	
	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	—	4.0	—	
		10	8.0	—	8.0	—	8.0	—	
		15	12.5	—	12.5	—	12.5	—	
Output Drive Current B Gates (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	—	-0.36	—	
		10	-1.6	—	-1.3	—	-0.9	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	—	0.36	—	
		10	1.6	—	1.3	—	0.9	—	
		15	4.2	—	3.4	—	2.4	—	
Output Drive Current UB Gates (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.2	—	-0.14	—	
		10	-0.62	—	-0.5	—	-0.35	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	—	0.36	—	
		10	1.6	—	1.3	—	0.9	—	
		15	4.2	—	3.4	—	2.4	—	
Output Drive Current Other Devices (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-0.64	—	-0.51	—	-0.36	—	mAdc
		10	-1.6	—	-1.3	—	-0.9	—	
		15	-4.2	—	-3.4	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	—	0.36	—	
		10	1.6	—	1.3	—	0.9	—	
		15	4.2	—	3.4	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	7.5	—	—	pF
Gate Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.25	—	7.5	μAdc
		10	—	0.5	—	0.5	—	15	
		15	—	1.0	—	1.0	—	30	
Flip-Flop and Buffer Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	1.0	—	30	μAdc
		10	—	2.0	—	2.0	—	60	
		15	—	4.0	—	4.0	—	120	
MSI Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	5.0	—	150	μAdc
		10	—	10	—	10	—	300	
		15	—	20	—	20	—	600	
LSI Quiescent Current	I <sub>DD</sub>		See Individual Data Sheets.						

**CHAPTER 5**  
**CMOS Handling and Design Guidelines**

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# HANDLING AND DESIGN GUIDELINES

## HANDLING PRECAUTIONS

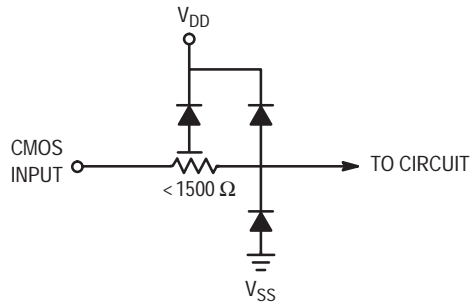
All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for ON Semiconductor CMOS devices is about 900 Å thick and breaks down at a gate–source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection networks shown in Figures 1A and 1B are used on each input to the CMOS device.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to  $V_{DD}$ , shorted to  $V_{SS}$ , or open–circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

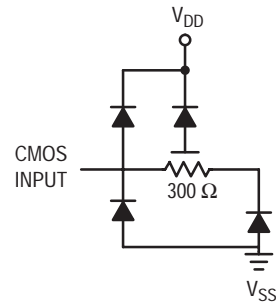
Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to  $V_{DD}$  or  $V_{SS}$ .
3. All low–impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.
5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic “snow”, styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
7. Nylon or other static generating materials should not come in contact with CMOS devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build–up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
9. Cold chambers using  $CO_2$  for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
10. When lead–straightening or hand–soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

## INPUT PROTECTION NETWORK



**Figure 1a. Input Protection Network  
Double Diode**



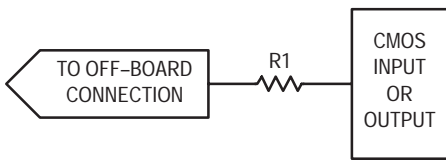
**Figure 1b. Input Protection Network  
Triple Diode**

11. The following steps should be observed during wave solder operations:
  - a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
  - b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
  - c. Operators must comply with precautions previously explained.
  - d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board-cleaning operations:
  - a. Vapor degreasers and baskets must be grounded to an earth ground.
  - b. Brush or spray cleaning should not be used.
  - c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
  - d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
  - e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of  $V_{DD}$  and  $V_{SS}$  before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

### RECOMMENDED FOR READING:

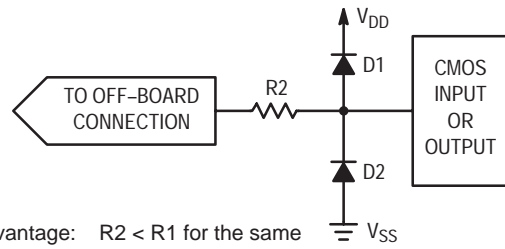
“Total Control of the Static in Your Business”

Available by writing to:  
3M Company  
Static Control Systems  
P.O. Box 2963  
Austin, Texas 78769-2963  
Or by Calling:  
1-800-328-1368



Advantage: Requires minimal board area

Disadvantage:  $R1 > R2$  for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage:  $R2 < R1$  for the same level of protection. Impact on ac and dc characteristics is minimized

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following

- A digital inputs and outputs
- B analog inputs and outputs
- C 3-state outputs
- D bidirectional (I/O) ports

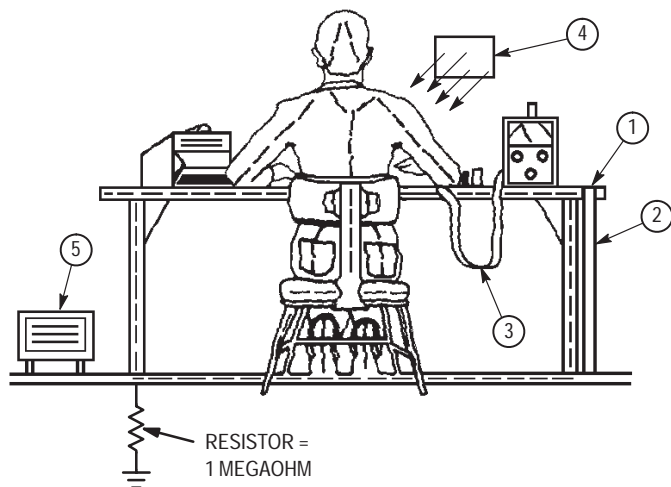
### PROPAGATION DELAY AND RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:

- R = the maximum allowable series resistance in ohms
- t = the maximum tolerable propagation delay or rise time in seconds
- C = the board capacitance plus the driven device's input capacitance in farads
- k = 0.7 for propagation delay calculations
- k = 2.3 for rise time calculations

**Figure 2. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility**



- NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.  
 2. Ground strap.  
 3. Wrist strap in contact with skin.  
 4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.  
 5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

Figure 3. Typical Manufacturing Work Station

## POWER SUPPLIES

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive, conventional power supplies, instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

The *absolute* maximum power supply voltage for 14000 Series Metal-gate CMOS is 18.0 Vdc. Figure 4 offers some insight as to how this specification was derived. In the figure,  $V_S$  is the maximum power supply voltage and  $I_S$  is the sustaining current of the latch-up mode. The value of  $V_S$  was chosen so that the secondary breakdown effect may be avoided.

In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection against

the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

CMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems:

1. The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 5, the battery voltage must be at least 3.7 Volts (3 Volts from the minimum power supply voltage and 0.7 Volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current to less than 10 mA or use the MC14049UB or MC14050B high-to-low voltage translators.
3. Outputs that are subject to voltage levels above  $V_{DD}$  or below  $V_{SS}$  should be protected with a series resistor to limit the current to less than 10 mA or with clamping diodes.

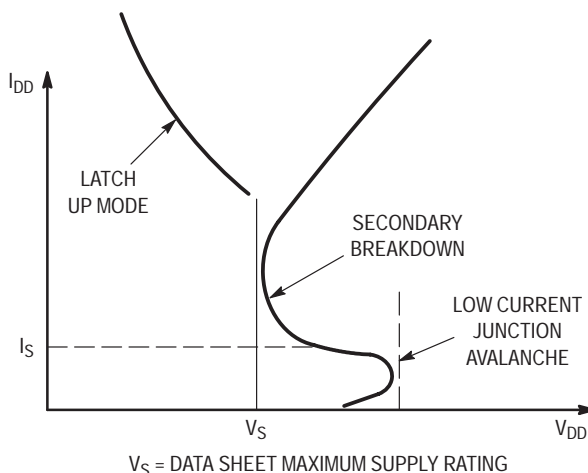


Figure 4. Secondary Breakdown Characteristics

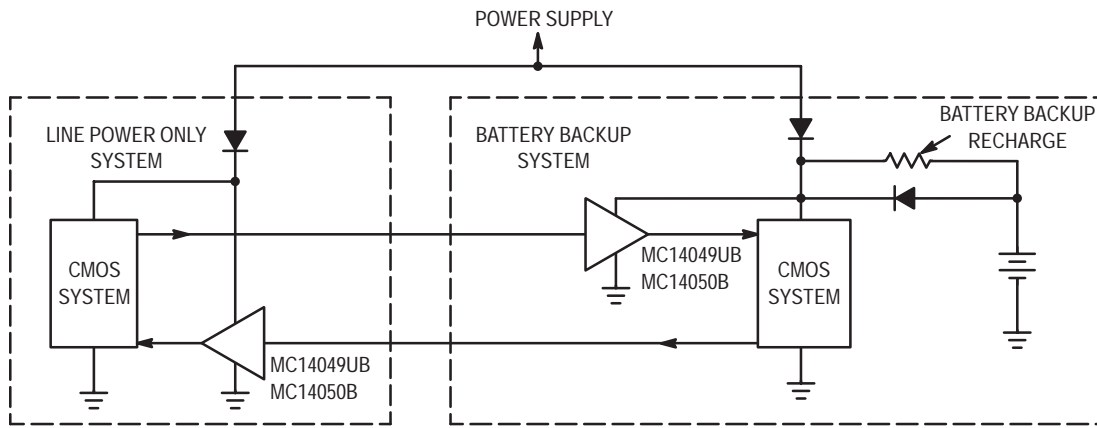


Figure 5. Battery Backup Interface

### INPUTS

All inputs, while in the recommended operating range ( $V_{SS} < V_{in} < V_{DD}$ ) can be modeled as shown in Figure 6. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case,  $1 \mu\text{A}$ , when the inputs are at  $V_{DD}$  or  $V_{SS}$ , and  $V_{DD} = 15.0 \text{ V}$ . This model does not apply to inputs with pull-up or pull-down resistors.

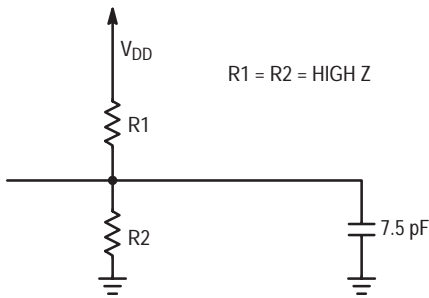


Figure 6. Input Model for  $V_{SS} \leq V_{in} \leq V_{DD}$

When left open-circuited, the inputs may self-bias at or near the typical switchpoint, where both the P-channel and N-channel transistors are conducting, causing excessive current drain. Due to the high gain of the inverters (see Figure 7), the device may also go into oscillation from any noise in the system. Since CMOS devices dissipate the most power during switching, this oscillation can cause very large current drain and undesired switching.

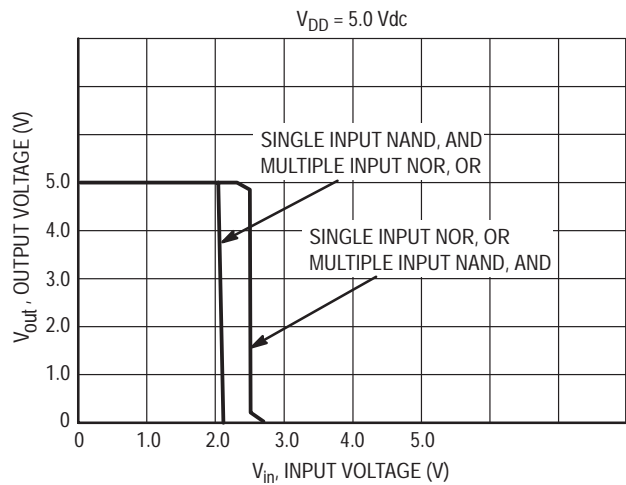


Figure 7. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused inputs should be connected either to  $V_{DD}$  or  $V_{SS}$ . For applications with inputs going to edge connectors, a 100 kilohm resistor to  $V_{SS}$  should be used, as well as a series resistor for static protection and current limiting (Figure 8). The 100 kilohm resistor will help eliminate any static charges that might develop on the printed circuit board. See Figure 2 for other possible protection arrangements.

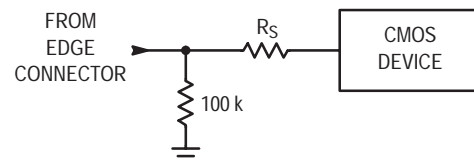
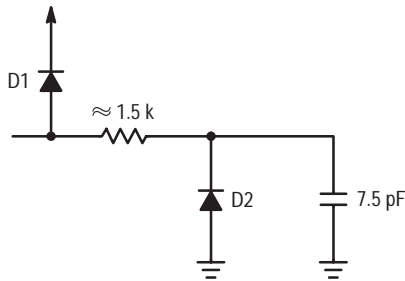


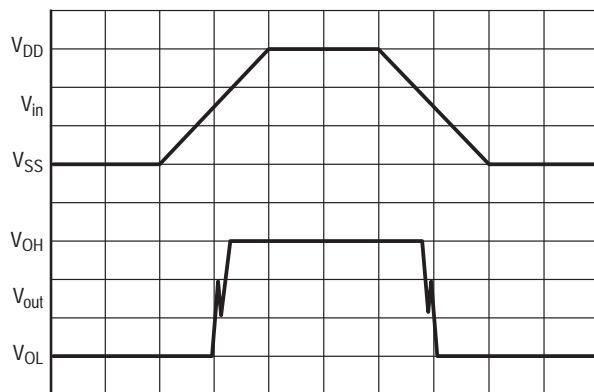
Figure 8. External Protection

For input voltages outside of the recommended operating range, the CMOS input is modeled as in Figure 9. The resistor–diode protection network allows the user greater freedom when designing a worst case system. The device inputs are guaranteed to withstand voltages from  $V_{SS} - 0.5$  V to  $V_{DD} + 0.5$  V and a maximum current of 10 mA. With the above input ratings, most designs will require no special terminations or design considerations.



**Figure 9. Input Model for  $V_{in} > V_{DD}$  or  $V_{in} < V_{SS}$**

Other specifications that should be noted are the maximum input rise and fall times. Figure 10 shows the oscillations that may result from exceeding the 15  $\mu$ s maximum rise and fall time at  $V_{DD} = 5.0$  V, 5  $\mu$ s at 10 V, or 4  $\mu$ s at 15 V. As the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified, and passed through to the output, causing oscillations. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 15  $\mu$ s at 5.0 V, 5  $\mu$ s at 10 V, or 4  $\mu$ s at 15 V, Schmitt–trigger devices such as the MC14093B, MC14584B, MC14106B, HC14, or HC132 are recommended for squaring–up these slow transitions.



**Figure 10. Maximum Rise and Fall Time Violations**

## OUTPUTS

All CMOS B–Series outputs are buffered to insure consistent output voltage and current performance. All buffered outputs have guaranteed output voltages of  $V_{OL} = 0.05$  V and  $V_{OH} = V_{DD} - 0.05$  V for  $V_{in} = V_{DD}$  or  $V_{SS}$  and

$I_{out} = 0$   $\mu$ A. The output drives for all buffered CMOS devices are such that 1 LSTTL load can be driven across the full temperature range.

CMOS outputs are limited to externally forced output voltages of  $V_{SS} - 0.5$  V  $\leq V_{out} \leq V_{DD} + 0.5$  V. When voltages are forced outside of this range, a silicon controlled rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see the explanation of CMOS Latch Up in this section.

The maximum rated output current for most outputs is 10 mA. The output short–circuit currents of these devices typically exceed these limits. Care must be taken not to exceed the maximum ratings found on every data sheet.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), two or more outputs on the same chip may be externally paralleled.

## CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

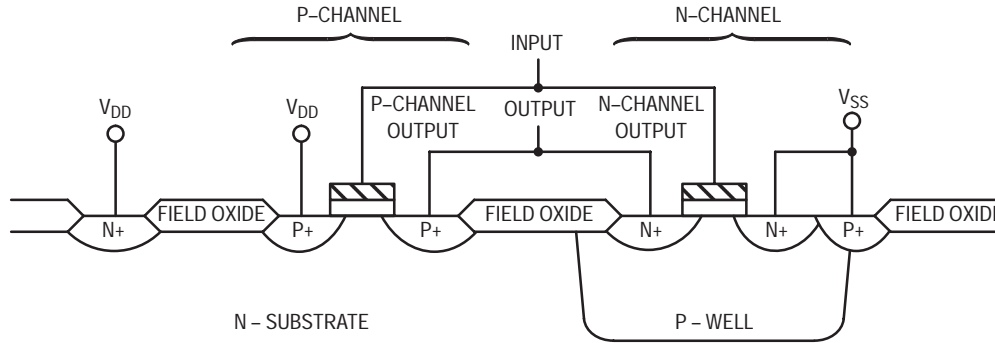
Figure 11 shows the cross–section of a typical CMOS inverter and Figure 12 shows the parasitic bipolar devices. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in saturation, thereby latching the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than  $V_{DD} + 0.5$  V or less than  $V_{SS} - 0.5$  V and have sufficient current to trigger the SCR. The latch–up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below:

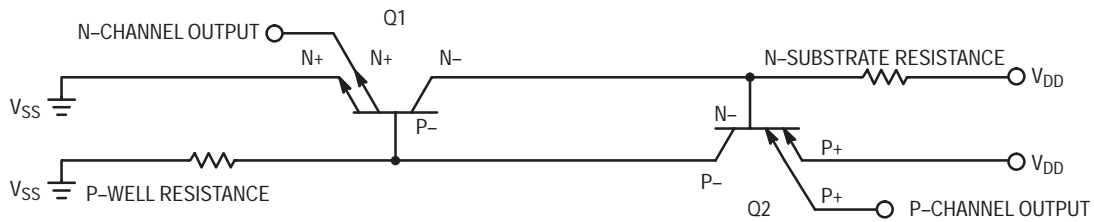
1. Insure that inputs and outputs are limited to the maximum rated values, as follows:  
 $-0.5$  V  $\leq V_{in}$  or  $V_{out} \leq V_{DD} + 0.5$  V (referenced to  $V_{SS}$ )  $|I_{in}$  or  $I_{out}| \leq 10$  mA (unless otherwise indicated on the data sheet)
2. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 10 mA. (See Figure 2).
3. Sequence power supplies so that the inputs or outputs of CMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or

- series resistors may be used in plug-in board applications).
- Voltage regulating or filtering should be used in board design and layout to insure that power-supply lines are free of excessive noise.

- Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.



**Figure 11. CMOS Wafer Cross Section**



**Figure 12. Latch Up Circuit Schematic**

# CHAPTER 6

## CMOS Logic Data Sheets

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# MC14001B Series

## B-Suffix Series CMOS Gates

MC14001B, MC14011B, MC14023B,  
MC14025B, MC14071B, MC14073B,  
MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

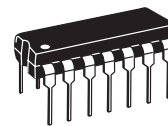
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



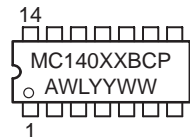
ON Semiconductor

<http://onsemi.com>

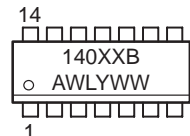
### MARKING DIAGRAMS



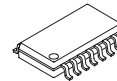
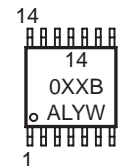
PDIP-14  
P SUFFIX  
CASE 646



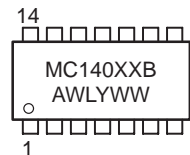
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### DEVICE INFORMATION

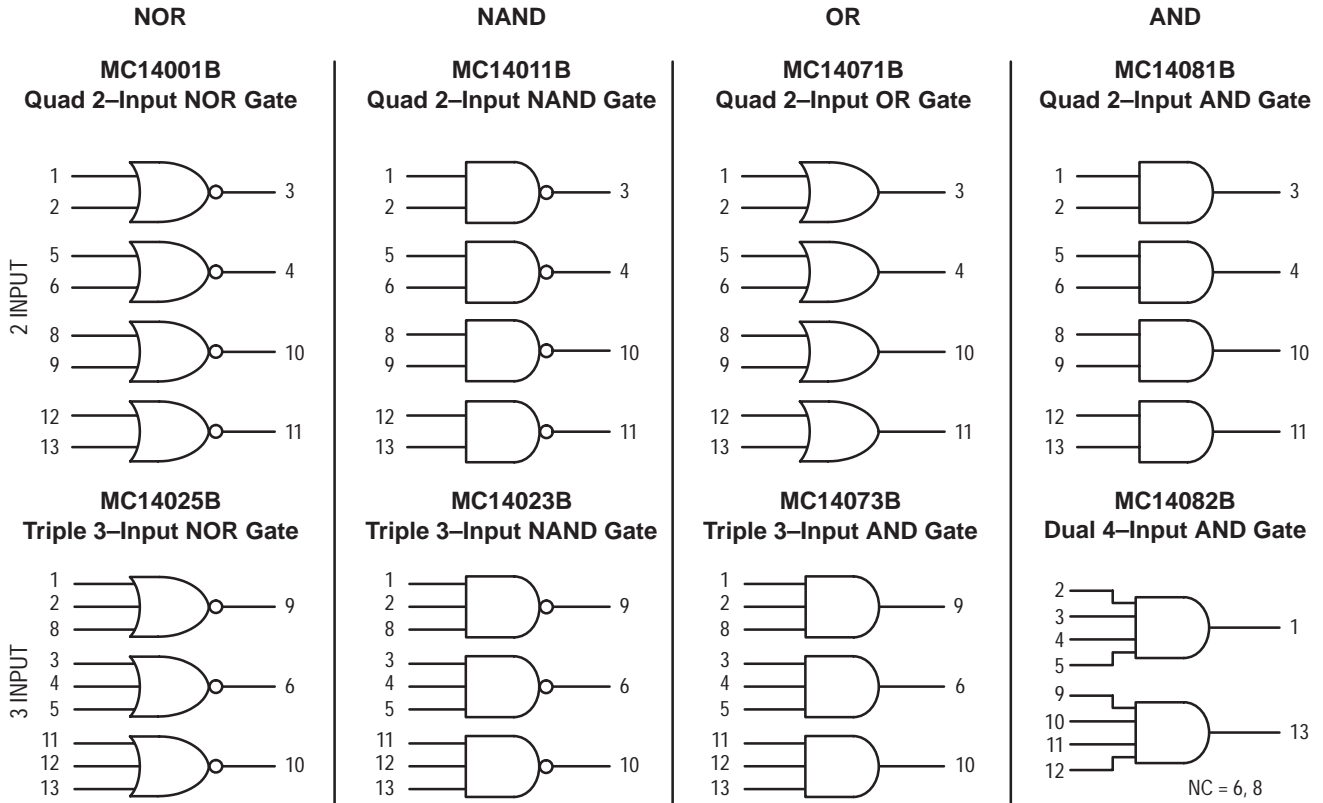
Device	Description
MC14001B	Quad 2-Input NOR Gate
MC14011B	Quad 2-Input NAND Gate
MC14023B	Triple 3-Input NAND Gate
MC14025B	Triple 3-Input NOR Gate
MC14071B	Quad 2-Input OR Gate
MC14073B	Triple 3-Input AND Gate
MC14081B	Quad 2-Input AND Gate
MC14082B	Dual 4-Input AND Gate

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 39 of this data sheet.

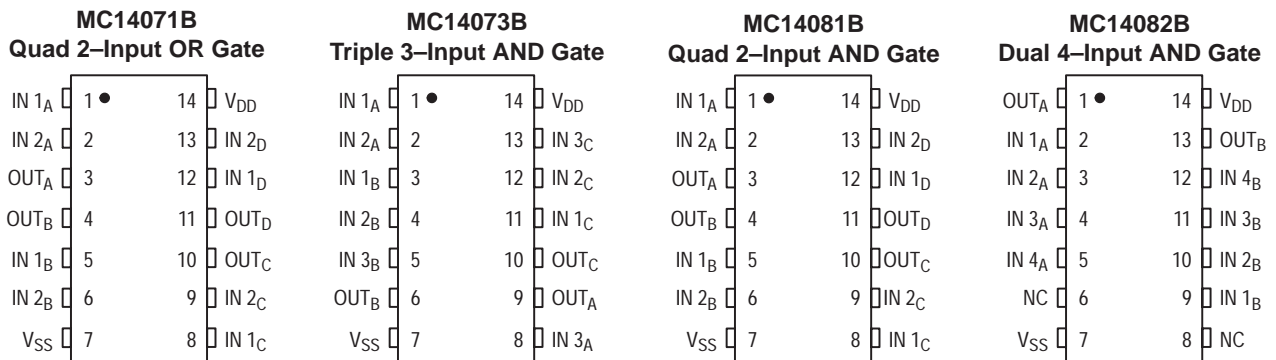
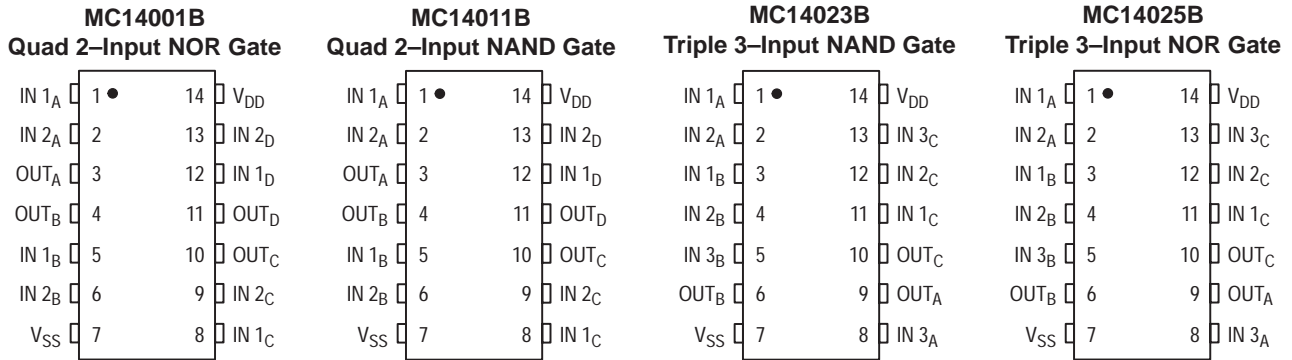
# MC14001B Series

## LOGIC DIAGRAMS



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7  
 FOR ALL DEVICES

## PIN ASSIGNMENTS



NC = NO CONNECTION

# MC14001B Series

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	“0” Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  “1” Level ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	$V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  Sink ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	$I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu$ Adc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Gate, $C_L = 50$ pF)	$I_T$	5.0 10 15	$I_T = (0.3 \mu A/kHz) f + I_{DD}/N$ $I_T = (0.6 \mu A/kHz) f + I_{DD}/N$ $I_T = (0.9 \mu A/kHz) f + I_{DD}/N$							$\mu$ Adc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001 \times$  the number of exercised gates per package.

# MC14001B Series

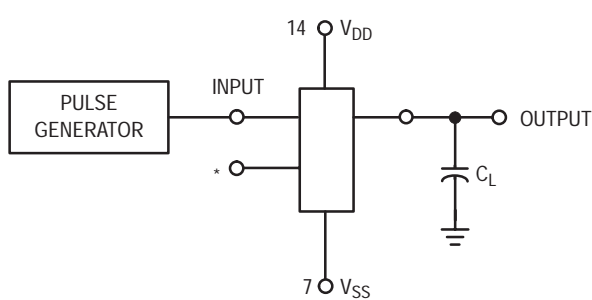
## B-SERIES GATE SWITCHING TIMES

**SWITCHING CHARACTERISTICS (6.)** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

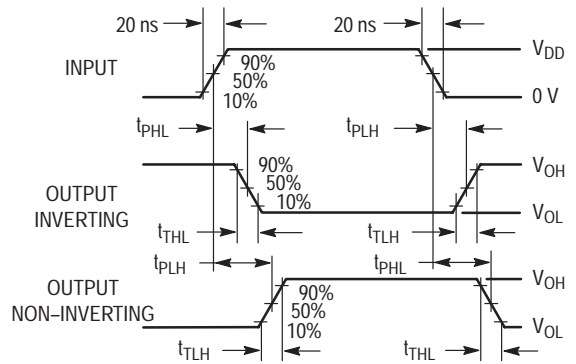
Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time, All B-Series Gates $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time, All B-Series Gates $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time MC14001B, MC14011B only $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 27 \text{ ns}$ All Other 2, 3, and 4 Input Gates $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$ 8-Input Gates (MC14068B, MC14078B) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	125 50 40  160 65 50  200 80 60	250 100 80  300 130 100  350 150 110	ns

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



\*All unused inputs of AND, NAND gates must be connected to  $V_{DD}$ .  
 All unused inputs of OR, NOR gates must be connected to  $V_{SS}$ .

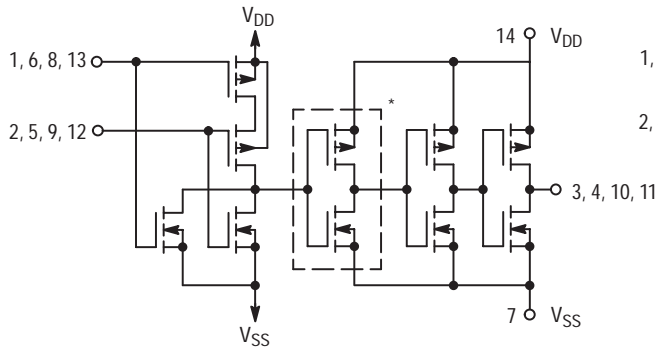


**Figure 1. Switching Time Test Circuit and Waveforms**

# MC14001B Series

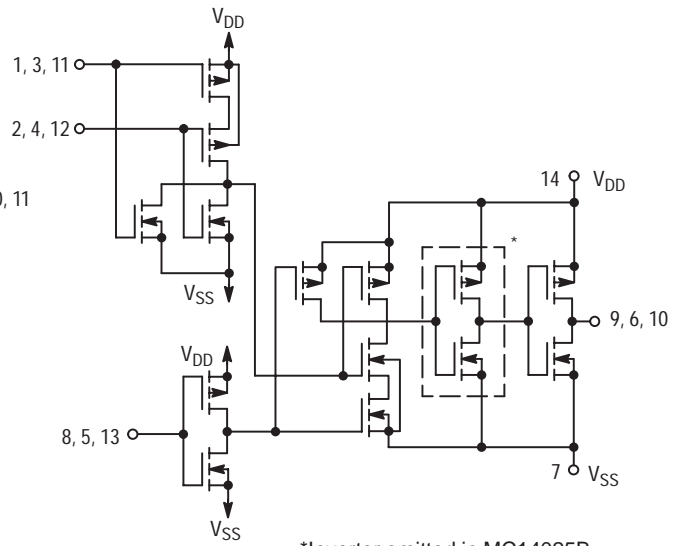
## CIRCUIT SCHEMATIC NOR, OR GATES

**MC14001B, MC14071B**  
One of Four Gates Shown



\*Inverter omitted in MC14001B

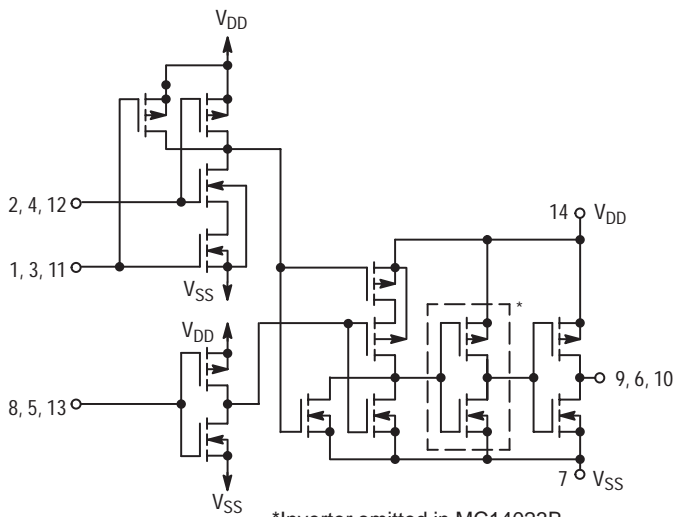
**MC14025B**  
One of Three Gates Shown



\*Inverter omitted in MC14025B

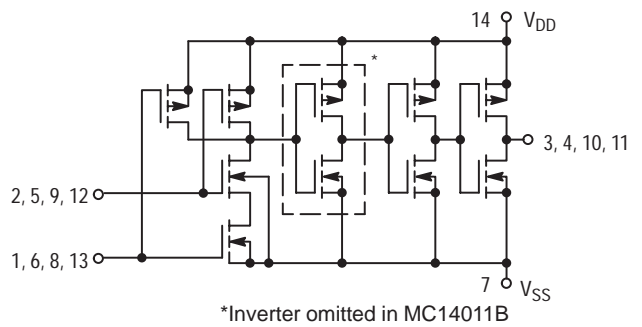
## CIRCUIT SCHEMATIC NAND, AND GATES

**MC14023B, MC14073B**  
One of Three Gates Shown



\*Inverter omitted in MC14023B

**MC14011B, MC14081B**  
One of Four Gates Shown

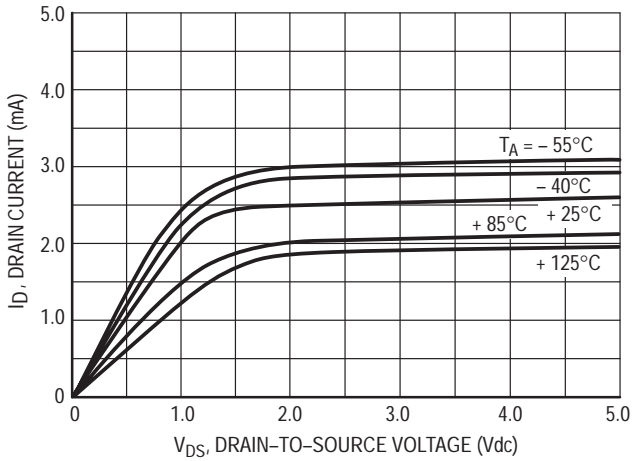


\*Inverter omitted in MC14011B

# MC14001B Series

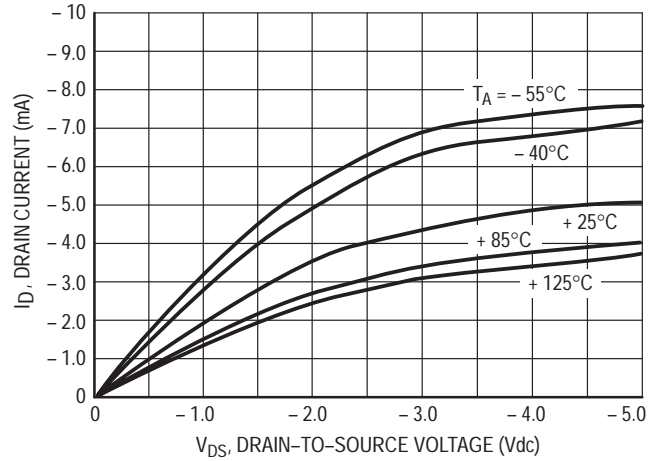
## TYPICAL B-SERIES GATE CHARACTERISTICS

**N-CHANNEL DRAIN CURRENT (SINK)**

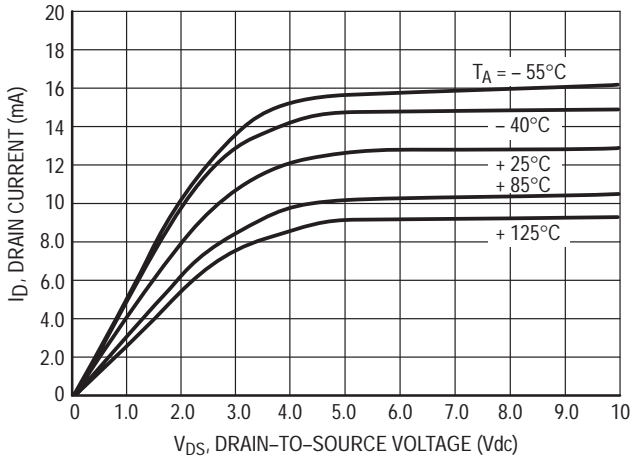


**Figure 2.  $V_{GS} = 5.0$  Vdc**

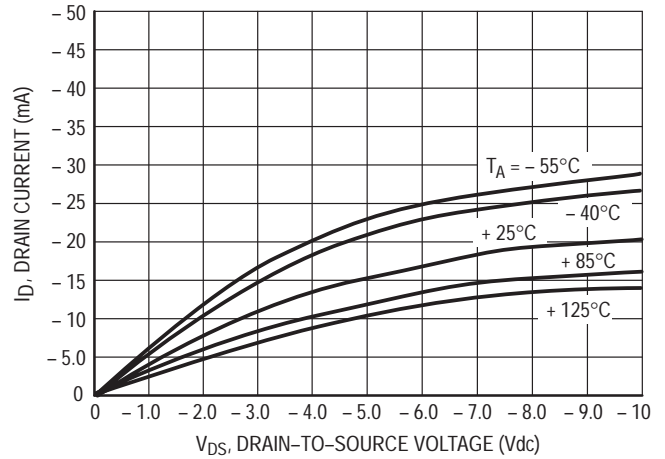
**P-CHANNEL DRAIN CURRENT (SOURCE)**



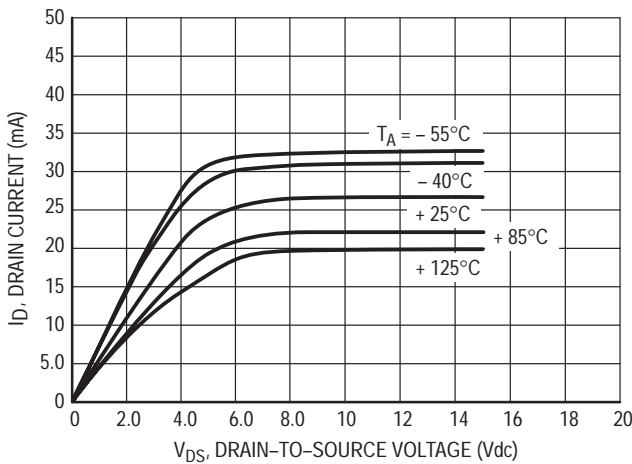
**Figure 3.  $V_{GS} = -5.0$  Vdc**



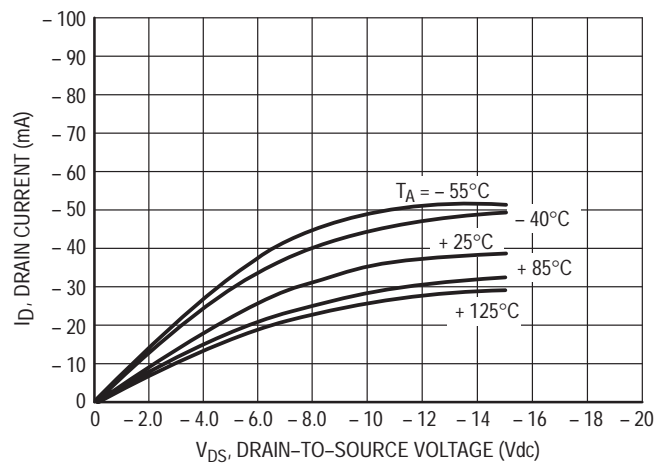
**Figure 4.  $V_{GS} = 10$  Vdc**



**Figure 5.  $V_{GS} = -10$  Vdc**



**Figure 6.  $V_{GS} = 15$  Vdc**



**Figure 7.  $V_{GS} = -15$  Vdc**

These typical curves are not guarantees, but are design aids.  
Caution: The maximum rating for output current is 10 mA per pin.

# MC14001B Series

## TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

### VOLTAGE TRANSFER CHARACTERISTICS

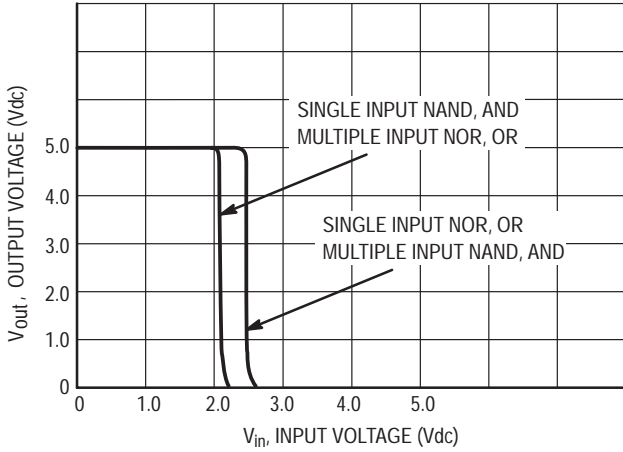


Figure 8.  $V_{DD} = 5.0 \text{ Vdc}$

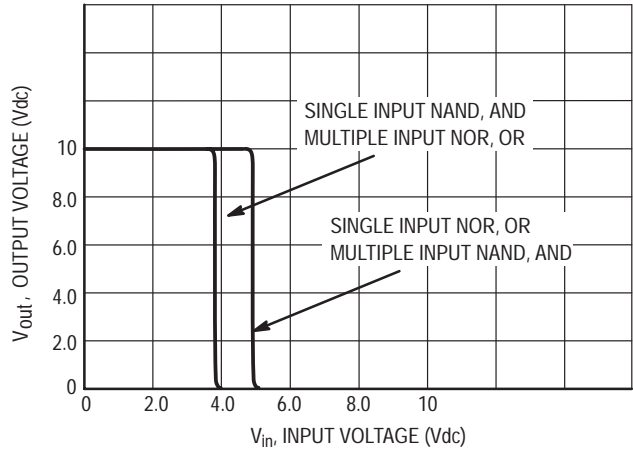


Figure 9.  $V_{DD} = 10 \text{ Vdc}$

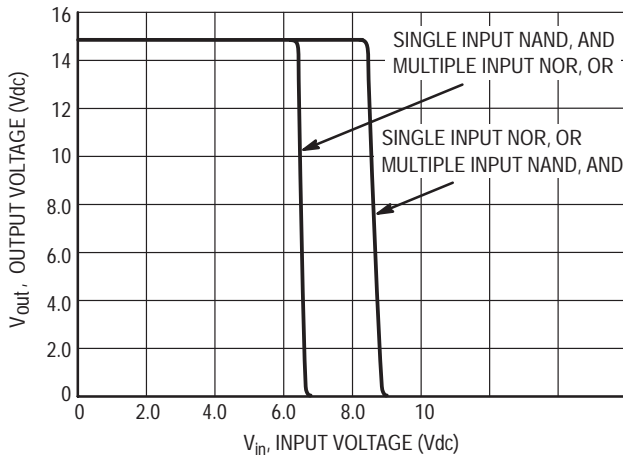


Figure 10.  $V_{DD} = 15 \text{ Vdc}$

### DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal “1” or “0” input level which does not produce output state change(s). The typical and guaranteed limit values of the input values  $V_{IL}$  and  $V_{IH}$  for the output(s) to be at a fixed voltage  $V_O$  are given in the Electrical Characteristics table.  $V_{IL}$  and  $V_{IH}$  are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the “1” and “0” levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply

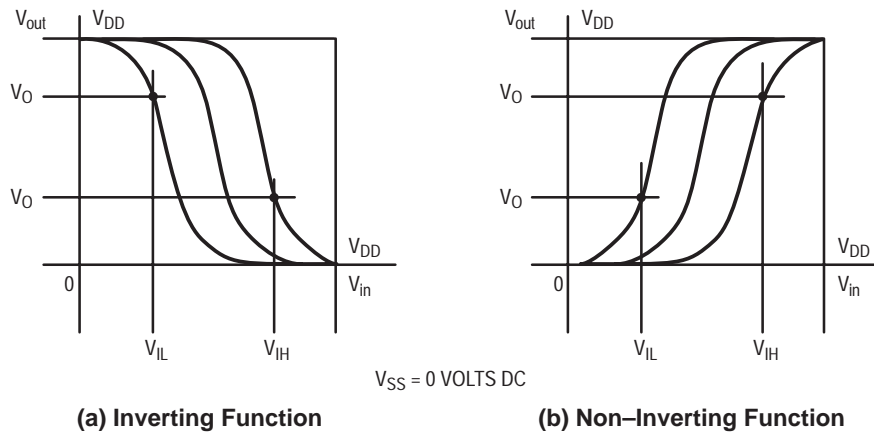


Figure 11. DC Noise Immunity

## MC14001B Series

### ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14001BCP	PDIP-14	2000 Units per Box
MC14001BD	SOIC-14	2750 Units per Box
MC14001BDR2	SOIC-14	2500 Units / Tape & Reel
MC14001BDT	TSSOP-14	96 Units per Rail
MC14001BDTR2	TSSOP-14	96 Units per Rail
MC14011BCP	PDIP-14	2000 Units per Box
MC14011BD	SOIC-14	2750 Units per Box
MC14011BDR2	SOIC-14	2500 Units / Tape & Reel
MC14011BDT	TSSOP-14	96 Units per Rail
MC14011BDTEL	TSSOP-14	2000 Units / Tape & Reel
MC14011BDTR2	TSSOP-14	50 Units per Rail
MC14023BCP	PDIP-14	2000 Units per Box
MC14023BD	SOIC-14	2750 Units per Box
MC14023BDR2	SOIC-14	2500 Units / Tape & Reel
MC14025BCP	PDIP-14	2000 Units per Box
MC14025BD	SOIC-14	2750 Units per Box
MC14025BDR2	SOIC-14	2500 Units / Tape & Reel

### ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14071BCP	PDIP-14	2000 Units per Box
MC14071BD	SOIC-14	55 Units per Rail
MC14071BDR2	SOIC-14	2500 Units / Tape & Reel
MC14071BDT	TSSOP-14	96 Units per Rail
MC14071BDTR2	TSSOP-14	96 Units per Rail
MC14073BCP	PDIP-14	2000 Units per Box
MC14073BD	SOIC-14	55 Units per Rail
MC14073BDR2	SOIC-14	2500 Units / Tape & Reel
MC14081BCP	PDIP-14	2000 Units per Box
MC14081BD	SOIC-14	55 Units per Rail
MC14081BDR2	SOIC-14	2500 Units / Tape & Reel
MC14081BDT	TSSOP-14	96 Units per Rail
MC14081BDTR2	TSSOP-14	2500 Units / Tape & Reel
MC14082BCP	PDIP-14	2000 Units per Box
MC14082BD	SOIC-14	55 Units per Rail
MC14082BDR2	SOIC-14	2500 Units / Tape & Reel

For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.



# MC14001UB, MC14011UB

## UB-Suffix Series CMOS Gates

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

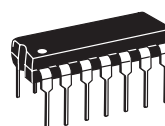


**ON Semiconductor**

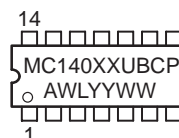
<http://onsemi.com>

## MC14001UB Quad 2-Input NOR Gate MC14011UB Quad 2-Input NAND Gate

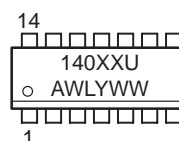
### MARKING DIAGRAMS



**PDIP-14  
P SUFFIX  
CASE 646**



**SOIC-14  
D SUFFIX  
CASE 751A**



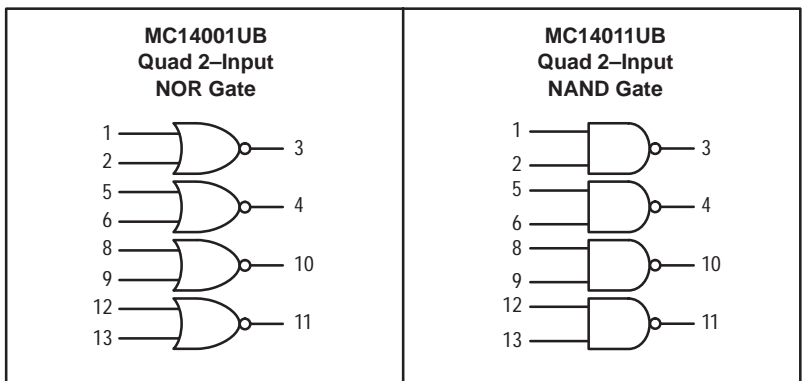
XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14001UBCP	PDIP-14	2000/Box
MC14001UBD	SOIC-14	55/Rail
MC14001UBDR2	SOIC-14	2500/Tape & Reel
MC14011UBCP	PDIP-14	2000/Box
MC14011UBD	SOIC-14	55/Rail
MC14011UBDR2	SOIC-14	2500/Tape & Reel

# MC14001UB, MC14011UB

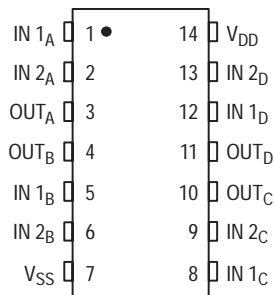
## LOGIC DIAGRAMS



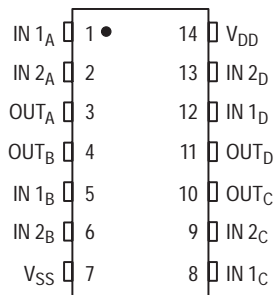
$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7  
 FOR ALL DEVICES

## PIN ASSIGNMENTS

**MC14001UB**  
Quad 2-Input NOR Gate



**MC14011UB**  
Quad 2-Input NAND Gate



# MC14001UB, MC14011UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc	
		10	—	2.0	—	4.50	2.0	—	2.0		
		15	—	2.5	—	6.75	2.5	—	2.5		
	"1" Level (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	I <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
			10	8.0	—	8.0	5.50	—	8.0	—	
			15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
	Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc	
		10	—	0.5	—	0.0010	0.5	—	15		
		15	—	1.0	—	0.0015	1.0	—	30		
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Gate C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /N							μAdc	
10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /N										
15	I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub> /N										

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μH (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

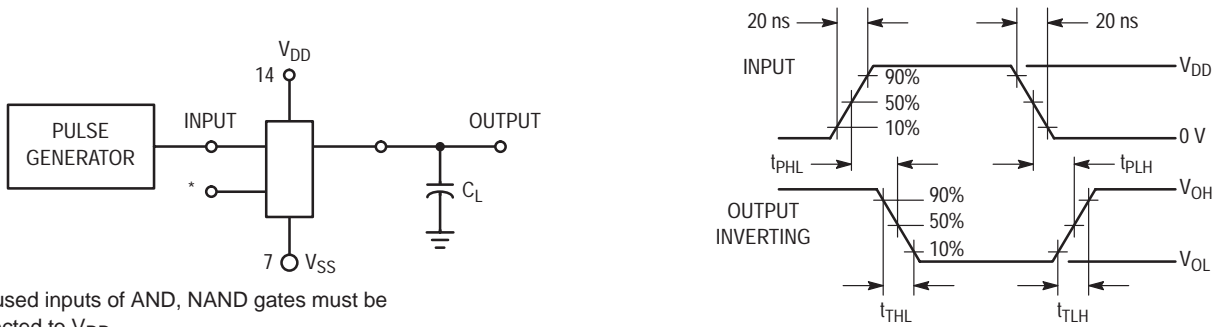
# MC14001UB, MC14011UB

## SWITCHING CHARACTERISTICS (6.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 22 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.50 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	90 50 40	180 100 80	ns

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

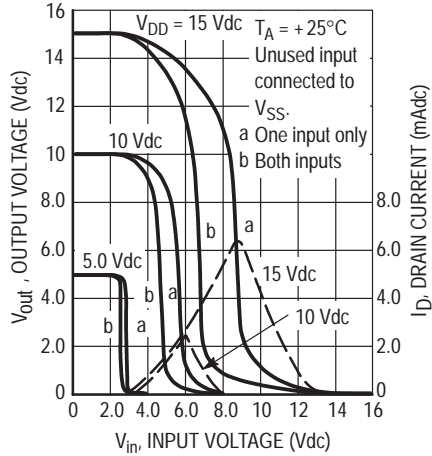
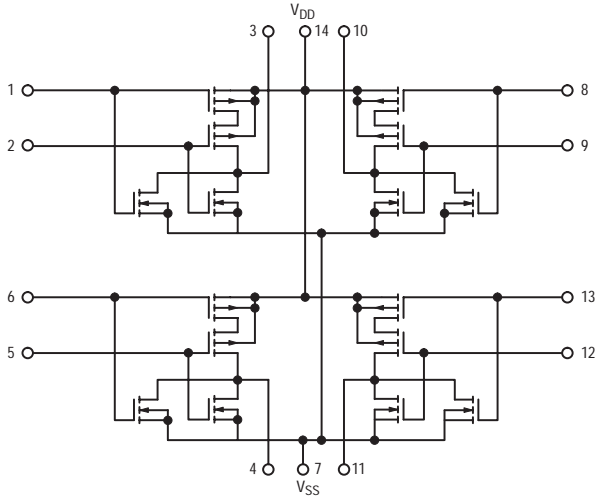


\*All unused inputs of AND, NAND gates must be connected to  $V_{DD}$ .  
 All unused inputs of OR, NOR gates must be connected to  $V_{SS}$ .

Figure 1. Switching Time Test Circuit and Waveforms

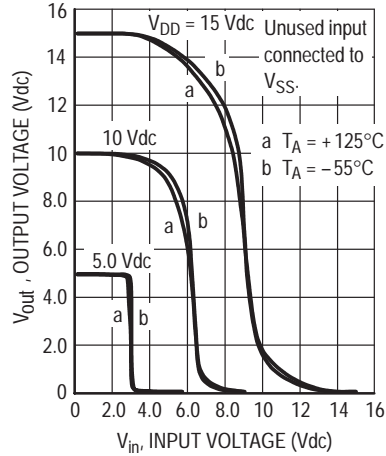
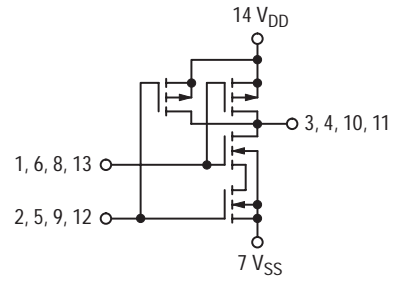
# MC14001UB, MC14011UB

## MC14001UB CIRCUIT SCHEMATIC

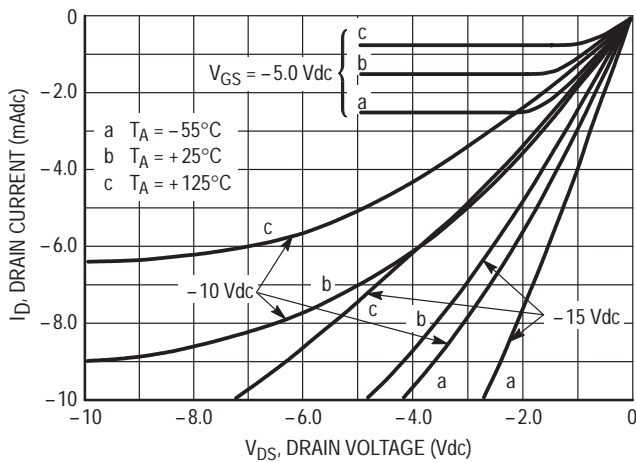


**Figure 2. Typical Voltage and Current Transfer Characteristics**

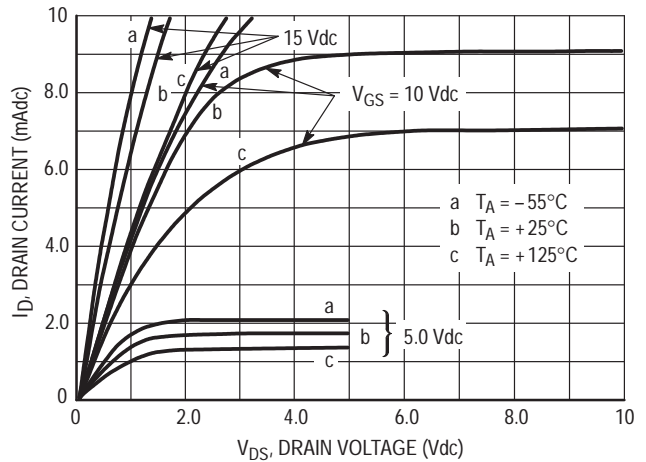
## MC14011UB CIRCUIT SCHEMATIC (1/4 of Device Shown)



**Figure 3. Typical Voltage Transfer Characteristics versus Temperature**



**Figure 4. Typical Output Source Characteristics**



**Figure 5. Typical Output Sink Characteristics**

# MC14007UB

## Dual Complementary Pair Plus Inverter

The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

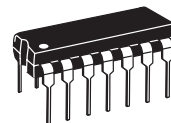
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



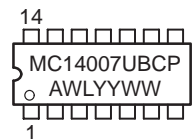
ON Semiconductor

<http://onsemi.com>

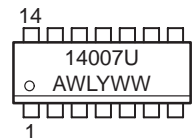
### MARKING DIAGRAMS



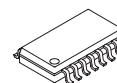
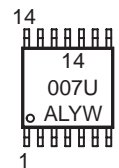
PDIP-14  
P SUFFIX  
CASE 646



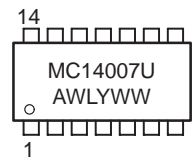
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

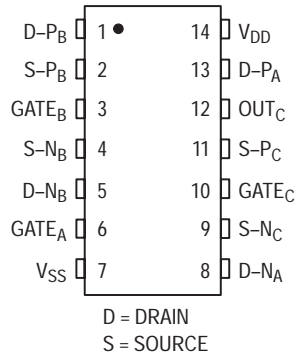
### ORDERING INFORMATION

Device	Package	Shipping
MC14007UBCP	PDIP-14	2000/Box
MC14007UBD	SOIC-14	55/Rail
MC14007UBDR2	SOIC-14	2500/Tape & Reel
MC14007UBDT	TSSOP-14	96/Rail
MC14007UBF	SOEIAJ-14	See Note 1.
MC14007UBFEL	SOEIAJ-14	See Note 1.

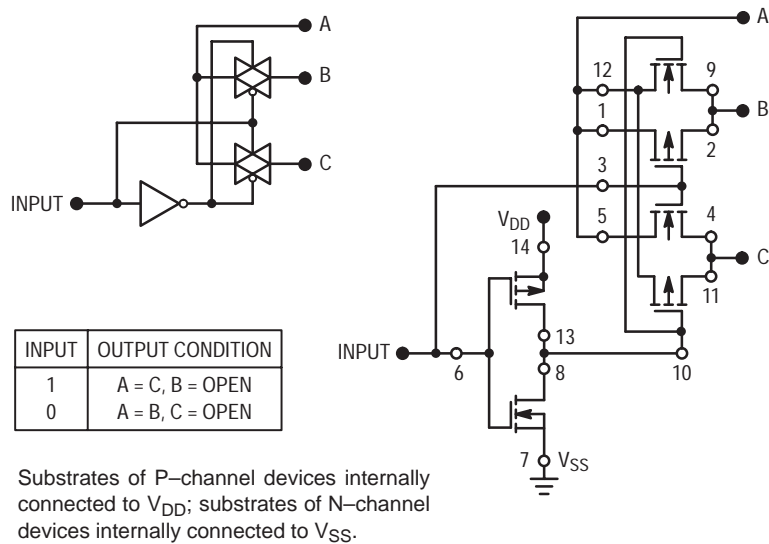
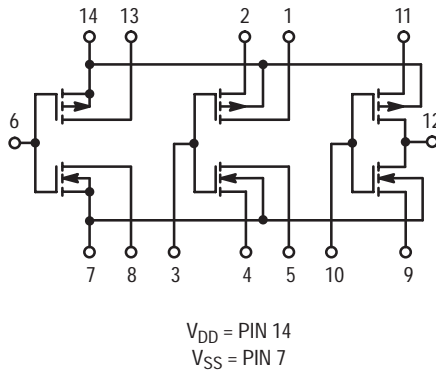
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14007UB

## PIN ASSIGNMENT



## SCHEMATIC



**Figure 1. Typical Application: 2-Input Analog Multiplexer**

# MC14007UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage  $(V_O = 4.5 \text{ Vdc})$ $(V_O = 9.0 \text{ Vdc})$ $(V_O = 13.5 \text{ Vdc})$  $(V_O = 0.5 \text{ Vdc})$ $(V_O = 1.0 \text{ Vdc})$ $(V_O = 1.5 \text{ Vdc})$	"0" Level  $V_{IL}$	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level  $V_{IH}$	5.0	4.0	—	4.0	2.75	—	4.0	—	
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current  $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$  $(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Source  $I_{OH}$	5.0	-3.0	—	-2.4	-5.0	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-1.0	—	-0.36	—	
		10	-1.6	—	-1.3	-2.5	—	-0.9	—	
	Sink  $I_{OL}$	5.0	0.64	—	0.51	1.0	—	0.36	—	
		10	1.6	—	1.3	2.5	—	0.9	—	
		15	4.2	—	3.4	10	—	2.4	—	
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{Adc}$
Input Capacitance $(V_{in} = 0)$	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu\text{Adc}$
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Gate) ( $C_L = 50 \text{ pF}$ )	$I_T$	5.0	$I_T = (0.7 \mu\text{A/kHz}) f + I_{DD}/6$							$\mu\text{Adc}$
		10	$I_T = (1.4 \mu\text{A/kHz}) f + I_{DD}/6$							
		15	$I_T = (2.2 \mu\text{A/kHz}) f + I_{DD}/6$							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.003$ .

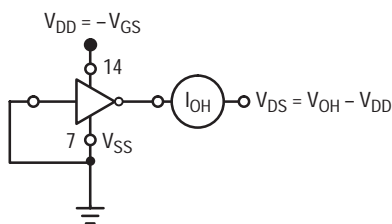


# MC14007UB

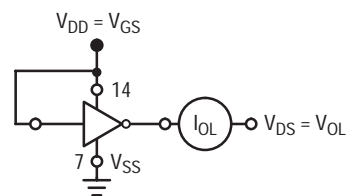
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (1.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.4 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	90 45 35	180 90 70	ns
Output Fall Time $t_{THL} = (1.2 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.4 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	75 40 30	150 80 60	ns
Turn-Off Delay Time $t_{PLH} = (1.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{PLH} = (0.2 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 17.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	60 30 25	125 75 55	ns
Turn-On Delay Time $t_{PHL} = (1.0 \text{ ns/pF}) C_L + 10 \text{ ns}$ $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	60 30 25	125 75 55	ns

7. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.  
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

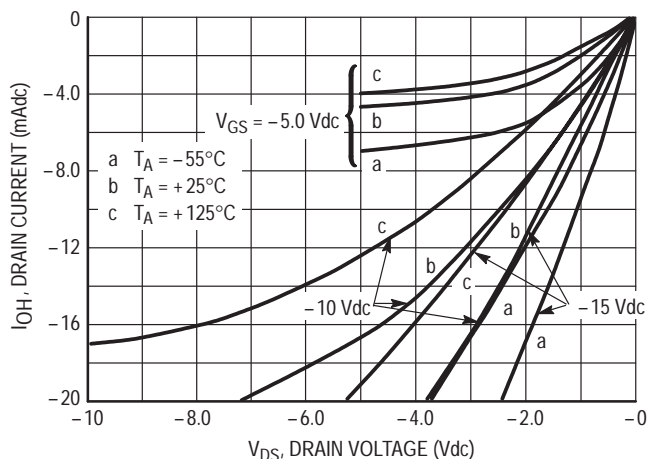


Figure 2. Typical Output Source Characteristics

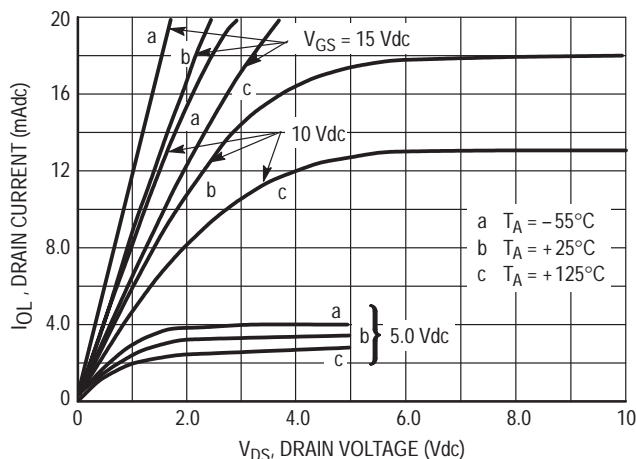


Figure 3. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.  
Caution: The maximum current rating is 10 mA per pin.

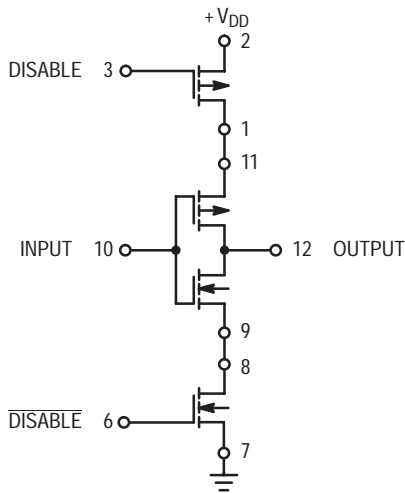
# MC14007UB



Figure 4. Switching Time and Power Dissipation Test Circuit and Waveforms

## APPLICATIONS

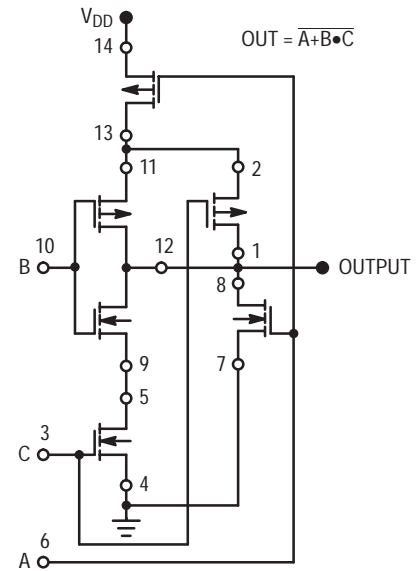
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 5. 3-State Buffer



Substrates of P-channel devices internally connected to V<sub>DD</sub>;  
Substrates of N-channel devices internally connected to V<sub>SS</sub>.

Figure 6. AOI Functions Using Tree Logic

# MC14008B

## 4-Bit Full Adder

The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

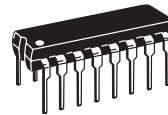
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



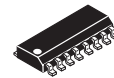
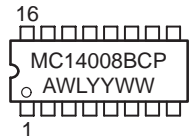
ON Semiconductor

<http://onsemi.com>

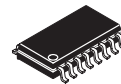
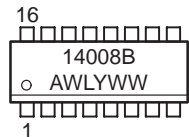
### MARKING DIAGRAMS



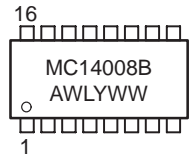
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14008BCP	PDIP-16	2000/Box
MC14008BDR2	SOIC-16	2500/Tape & Reel
MC14008BF	SOEIAJ-16	See Note 1.

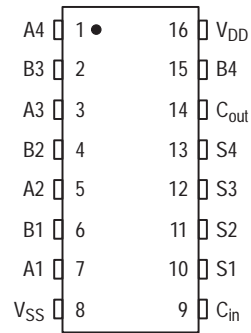
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14008B

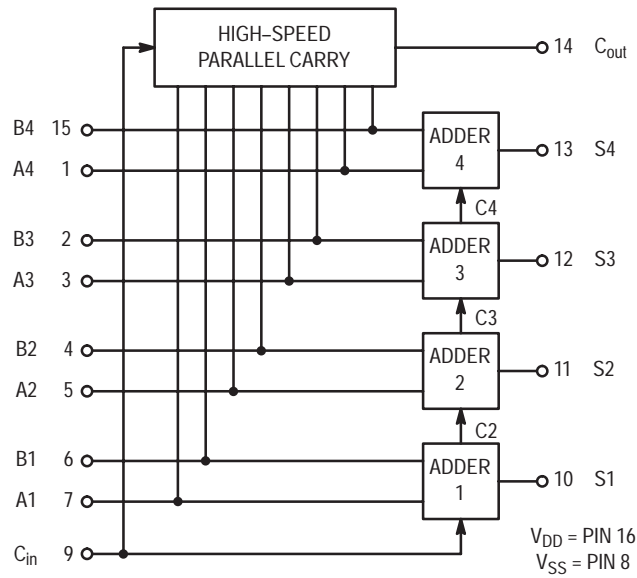
## TRUTH TABLE (One Stage)

C <sub>in</sub>	B	A	C <sub>out</sub>	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

## PIN ASSIGNMENT



## BLOCK DIAGRAM



# MC14008B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“0” Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	“1” Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.7 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (3.4 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (5.0 μA/kHz) f + I <sub>DD</sub>								

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.005.

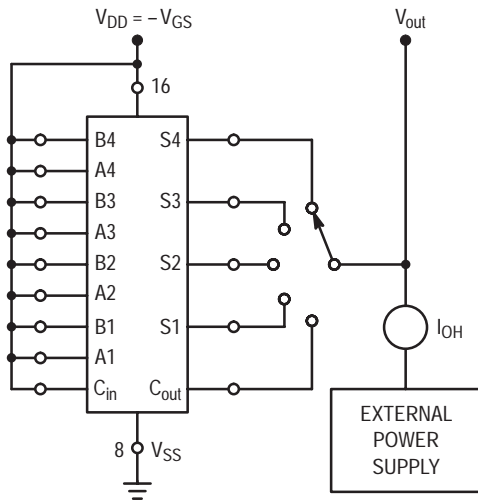
# MC14008B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

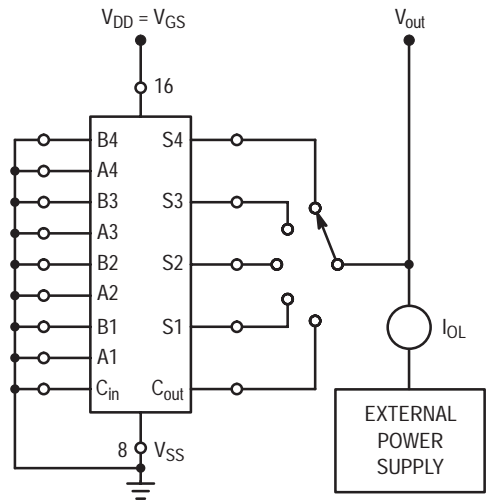
Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Sum in to Sum Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 127 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Sum In to Carry Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ Carry In to Sum Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 290 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ Carry In to Carry Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 85 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —  — — —	400 160 115  305 145 110  375 155 115  170 75 55	800 320 230  610 290 220  750 310 230  340 150 110	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



**Figure 1. Typical Source Current Characteristics Test Circuit**



**Figure 2. Typical Sink Current Characteristics Test Circuit**

# MC14008B

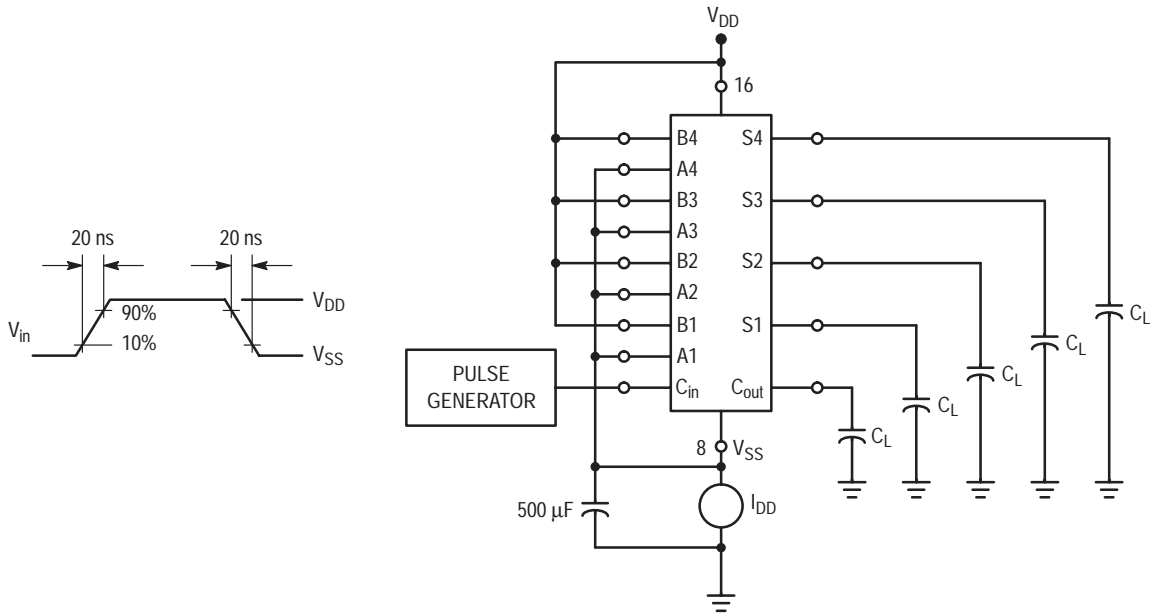


Figure 3. Dynamic Power Dissipation Test Circuit and Waveform

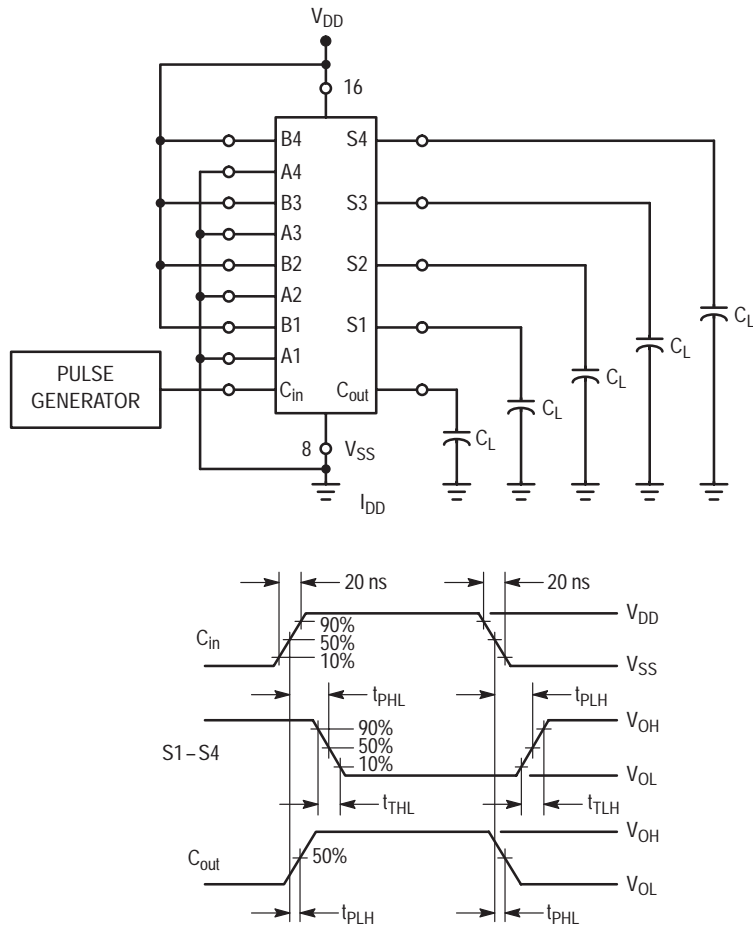


Figure 4. Switching Time Test Circuit and Waveforms

# MC14008B

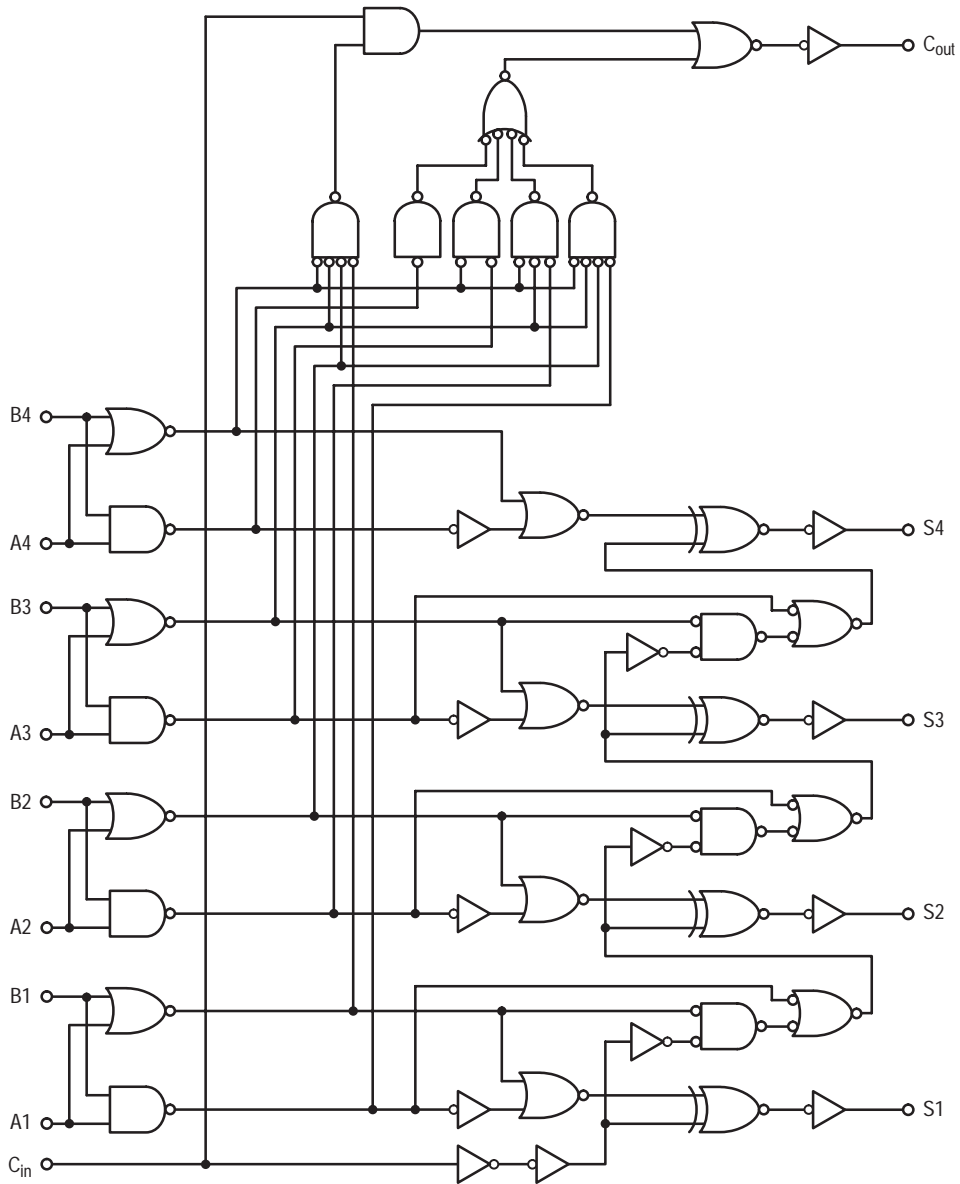
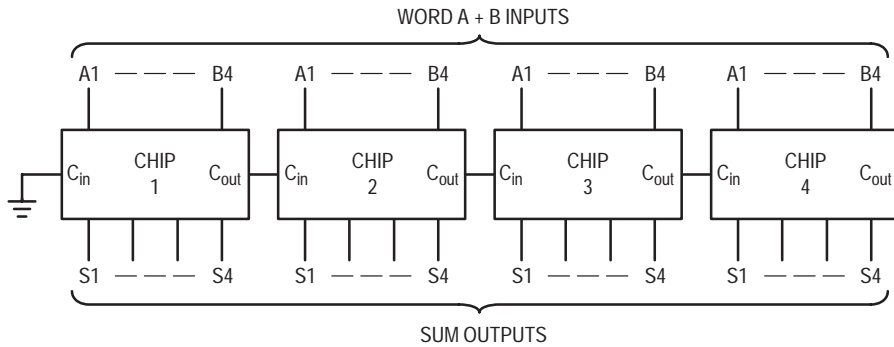


Figure 5. Logic Diagram

## TYPICAL APPLICATION



Calculation of 16-bit adder speed:

$$t_p \text{ total} = t_p (\text{Sum to Carry}) + t_p (\text{Carry to Sum}) + 2 t_p (\text{Carry to Carry})$$

The guaranteed 16-bit adder speed at 10 V, 25°C,  $C_L = 50 \text{ pF}$  is:

$$t_p \text{ total} = 290 + 310 + 300 = 900 \text{ ns}$$

Figure 6. Using the MC14008B in a 16-Bit Adder Configuration



# MC14013B

## Dual Type D Flip-Flop

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and  $\bar{Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design  
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

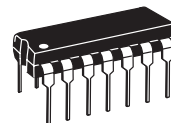
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



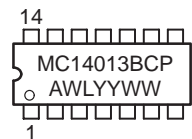
ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



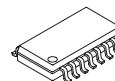
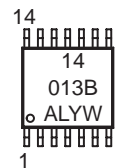
PDIP-14  
P SUFFIX  
CASE 646



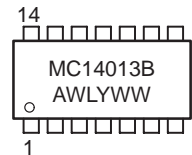
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week




### ORDERING INFORMATION

Device	Package	Shipping
MC14013BCP	PDIP-14	2000/Box
MC14013BD	SOIC-14	55/Rail
MC14013BDR2	SOIC-14	2500/Tape & Reel
MC14013BDT	TSSOP-14	96/Rail
MC14013BDTR2	TSSOP-14	2500/Tape & Reel
MC14013BF	SOEIAJ-14	See Note 1.
MC14013BFEL	SOEIAJ-14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14013B

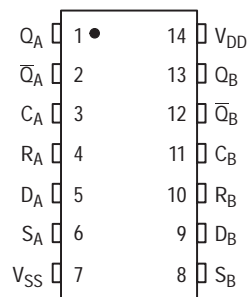
## TRUTH TABLE

Inputs				Outputs	
Clock <sup>†</sup>	Data	Reset	Set	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

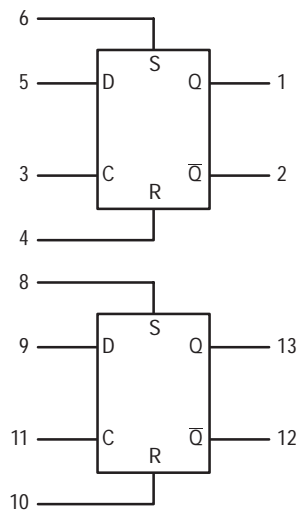
No  
Change

X = Don't Care  
† = Level Change

## PIN ASSIGNMENT



## BLOCK DIAGRAM



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7

# MC14013B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc	
		10	—	2.0	—	0.004	2.0	—	60		
		15	—	4.0	—	0.006	4.0	—	120		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.75 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.5 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.3 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10									
		15									

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14013B

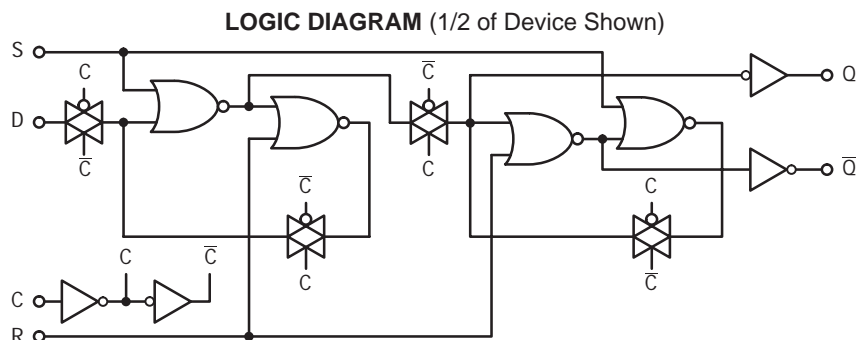
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q, $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Set to Q, $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Reset to Q, $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	175 75 50  175 75 50  225 100 75	350 150 100  350 150 100  450 200 150	ns
Setup Times (9.)	$t_{su}$	5.0 10 15	40 20 15	20 10 7.5	— — —	ns
Hold Times (9.)	$t_h$	5.0 10 15	40 20 15	20 10 7.5	— — —	ns
Clock Pulse Width	$t_{WL}$ , $t_{WH}$	5.0 10 15	250 100 70	125 50 35	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	4.0 10 14	2.0 5.0 7.0	MHz
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Set and Reset Pulse Width	$t_{WL}$ , $t_{WH}$	5.0 10 15	250 100 70	125 50 35	— — —	ns
Removal Times Set  Reset	$t_{rem}$	5 10 15  5 10 15	80 45 35  50 30 25	0 5 5  -35 -10 -5	— — —  — — —	ns

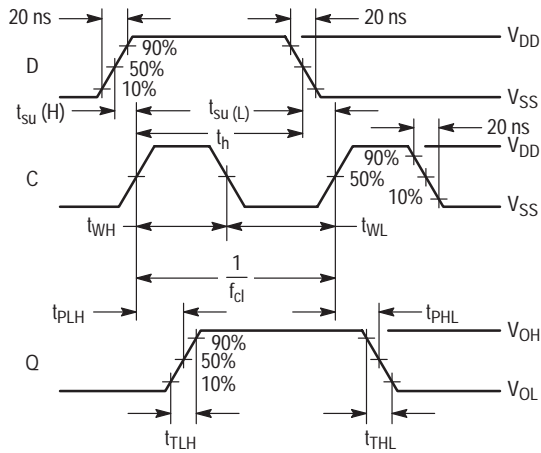
7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

9. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.

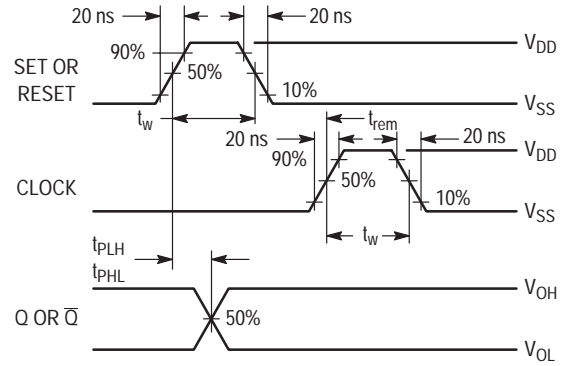


# MC14013B



Inputs R and S low.

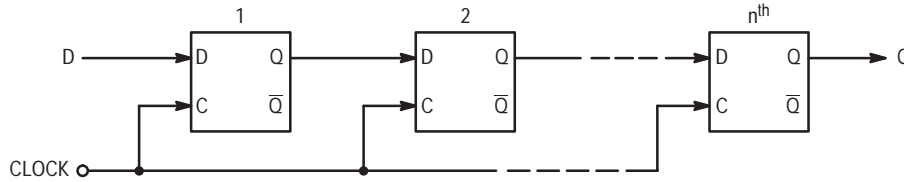
**Figure 1. Dynamic Signal Waveforms (Data, Clock, and Output)**



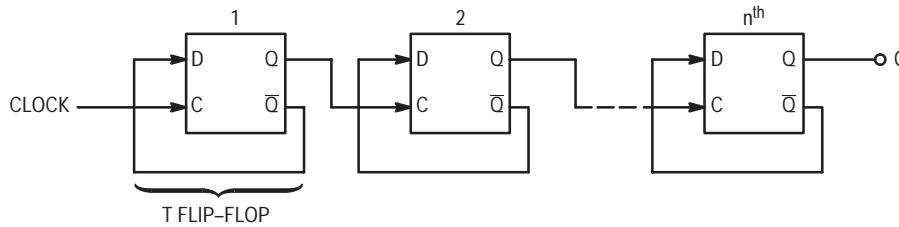
**Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)**

## TYPICAL APPLICATIONS

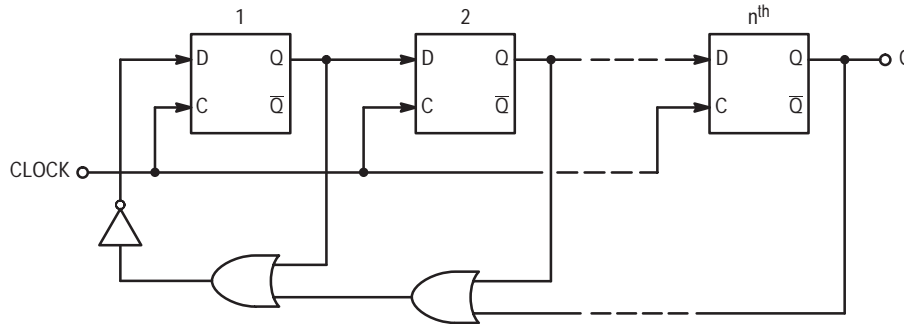
### n-STAGE SHIFT REGISTER



### BINARY RIPPLE UP-COUNTER (Divide-by- $2^n$ )



### MODIFIED RING COUNTER (Divide-by- $(n+1)$ )



# MC14014B, MC14021B

## 8-Bit Static Shift Register

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- “Q” Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

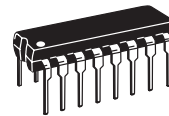
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



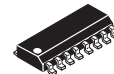
ON Semiconductor

<http://onsemi.com>

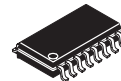
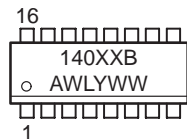
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14014BCP	PDIP-16	2000/Box
MC14014BD	SOIC-16	48/Rail
MC14014BDR2	SOIC-16	2500/Tape & Reel
MC14014BF	SOEIAJ-16	See Note 1.
MC14014BFEL	SOEIAJ-16	See Note 1.
MC14021BCP	PDIP-16	2000/Box
MC14021BD	SOIC-16	48/Rail
MC14021BDR2	SOIC-16	2500/Tape & Reel
MC14021BF	SOEIAJ-16	See Note 1.
MC14021BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14014B, MC14021B

## TRUTH TABLE

### SERIAL OPERATION:

t	Clock	D <sub>S</sub>	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	↗	0	0	0	?	?
n+1	↗	1	0	1	0	?
n+2	↗	0	0	0	1	0
n+3	↗	1	0	1	0	1
	↘	X	0	Q6	Q7	Q8

### PARALLEL OPERATION:

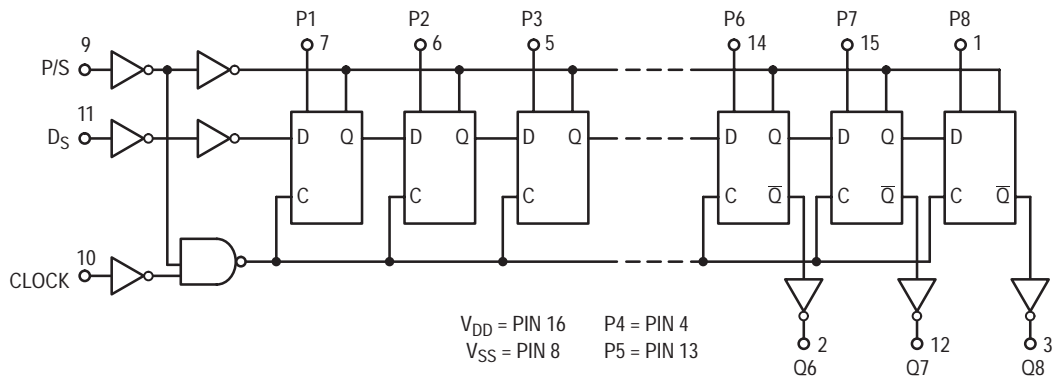
Clock		D <sub>S</sub>	P/S	P <sub>n</sub>	*Q <sub>n</sub>
MC14014B	MC14021B				
↗		X	1	0	0
↗		X	1	1	1

\*Q6, Q7, & Q8 are available externally  
X = Don't Care

## PIN ASSIGNMENT

P8	1 ●	16	V <sub>DD</sub>
Q6	2	15	P7
Q8	3	14	P6
P4	4	13	P5
P3	5	12	Q7
P2	6	11	D <sub>S</sub>
P1	7	10	C
V <sub>SS</sub>	8	9	P/S

## LOGIC DIAGRAM



# MC14014B, MC14021B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level   "1" Level	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
15			—	0.05	—	0	0.05	—	0.05	—	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
			10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—	
			15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—	
	Sink	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15			4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	µAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	15	—	0.015	15	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.75 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.50 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.25 µA/kHz) f + I <sub>DD</sub>							µAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.0015.



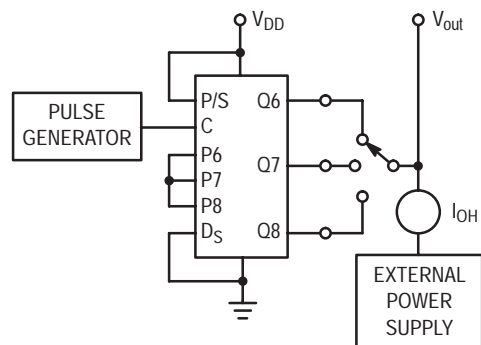
# MC14014B, MC14021B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Clock to Q, P/S to Q) $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	400 170 115	800 340 230	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	400 175 135	150 75 40	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Parallel/Serial Control Pulse Width	$t_{WH}$	5.0 10 15	400 175 135	150 75 40	— — —	ns
Setup Time P/S to Clock	$t_{su}$	5.0 10 15	200 100 80	100 50 40	— — —	ns
Hold Time Clock to P/S	$t_h$	5.0 10 15	20 20 25	-2.5 -10 0	— — —	ns
Setup Time Data (Parallel or Serial) to Clock or P/S	$t_{su}$	5.0 10 15	350 80 60	150 50 30	— — —	ns
Hold Time Clock to $D_S$	$t_h$	5.0 10 15	45 35 35	0 0 5	— — —	ns
Hold Time Clock to $P_n$	$t_h$	5.0 10 15	50 45 45	25 20 20	— — —	ns
Input Clock Rise Time	$t_{r(cl)}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Preset output under test to a logic "1" level.

Figure 1. Output Source Current Test Circuit

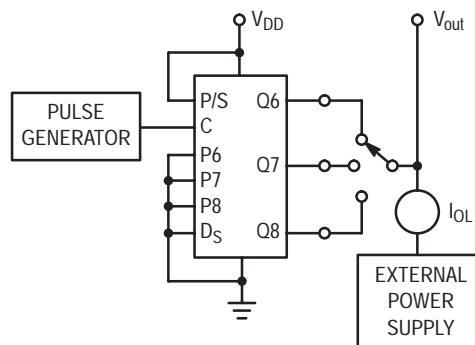


Figure 2. Output Sink Current Test Circuit

# MC14014B, MC14021B

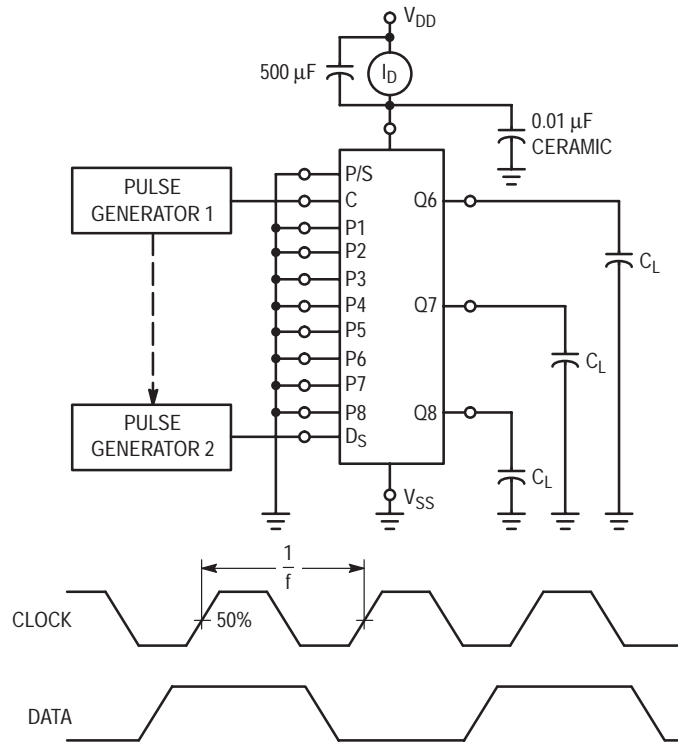


Figure 3. Power Dissipation Test Circuit and Waveform

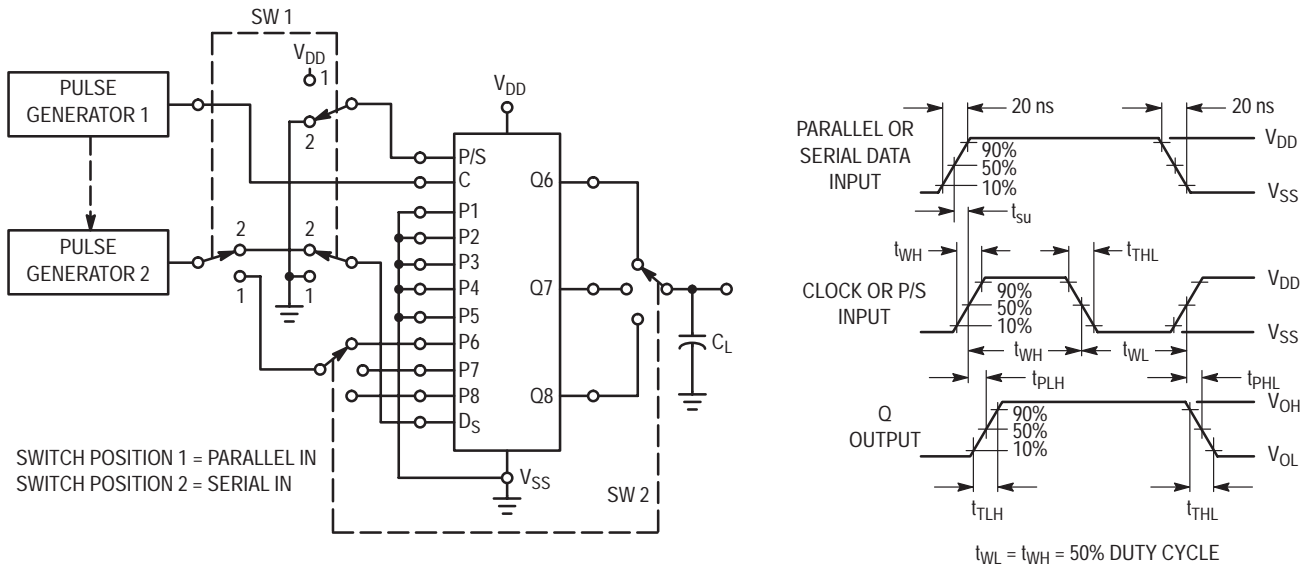


Figure 4. Switching Time Test Circuit and Waveforms

# MC14015B

## Dual 4-Bit Static Shift Register

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design —  
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

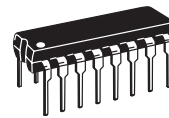
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



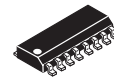
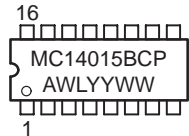
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### MARKING DIAGRAMS



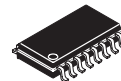
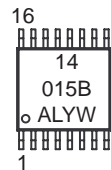
PDIP-16  
P SUFFIX  
CASE 648



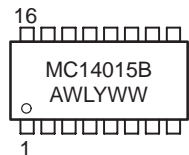
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14015BCP	PDIP-16	2000/Box
MC14015BD	SOIC-16	48/Rail
MC14015BDR2	SOIC-16	2500/Tape & Reel
MC14015BDT	TSSOP-16	2000/Tape & Reel
MC14015BF	SOEIAJ-16	See Note 1.
MC14015BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14015B

## TRUTH TABLE

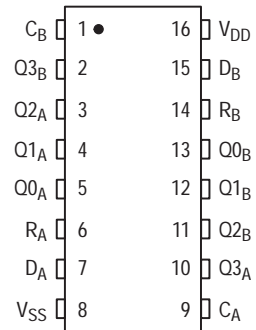
C	D	R	Q0	Q <sub>n</sub>
↗	0	0	0	Q <sub>n-1</sub>
↗	1	0	1	Q <sub>n-1</sub>
↘	X	0	No Change	No Change
X	X	1	0	0

X = Don't Care

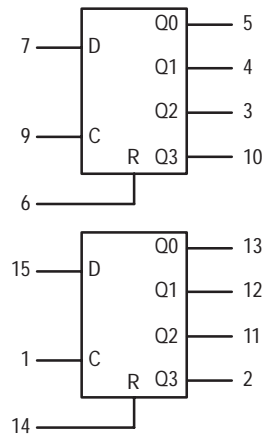
Q<sub>n</sub> = Q0, Q1, Q2, or Q3, as applicable.

Q<sub>n-1</sub> = Output of prior stage.

## PIN ASSIGNMENT



## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16

V<sub>SS</sub> = PIN 8

# MC14015B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or .05 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—	
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.2 µA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (2.4 µA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (3.6 µA/kHz)f + I <sub>DD</sub>							µAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14015B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock, Data to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 225 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	310 125 90  460 180 120	750 250 170  750 250 170	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	400 175 135	185 85 55	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.0 6.0 7.5	1.5 3.0 3.75	MHz
Clock Pulse Rise and Fall Times	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Reset Pulse Width	$t_{WH}$	5.0 10 15	400 160 120	200 80 60	— — —	ns
Setup Time	$t_{su}$	5.0 10 15	350 100 75	100 50 40	— — —	ns

7. The formulas given are for typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

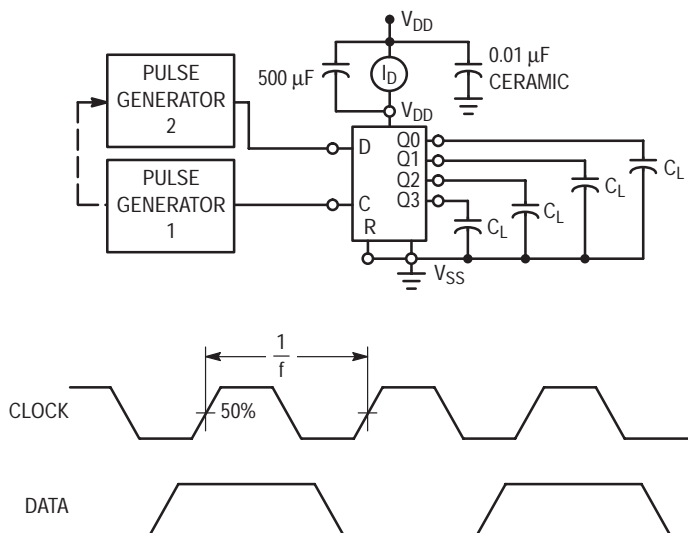


Figure 1. Power Dissipation Test Circuit and Waveform

# MC14015B

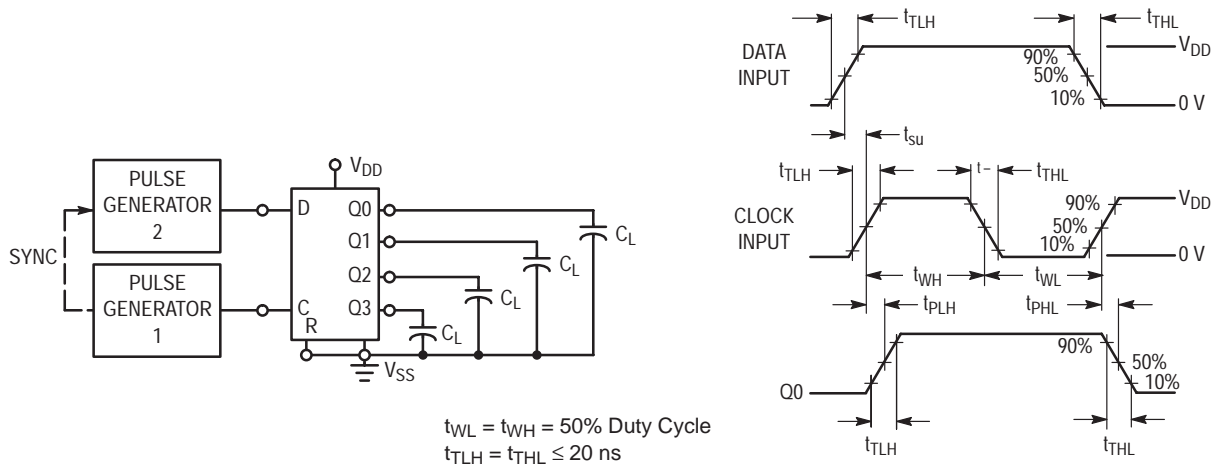


Figure 2. Switching Test Circuit and Waveforms

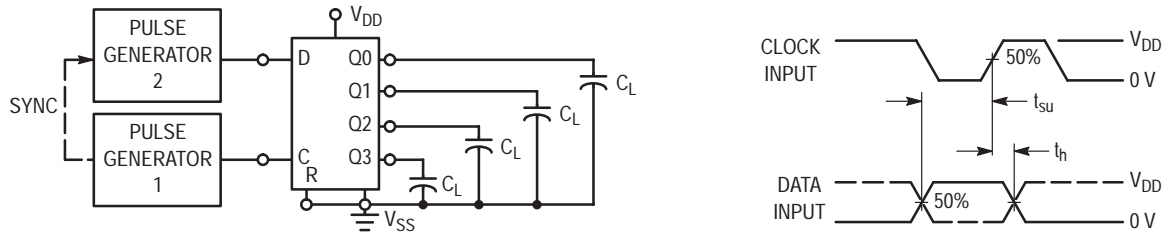
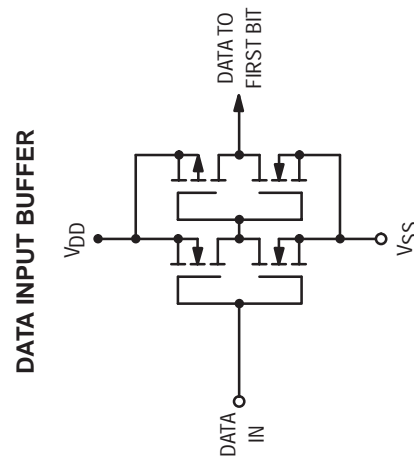
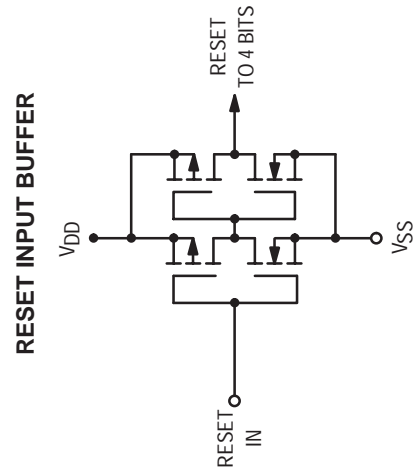
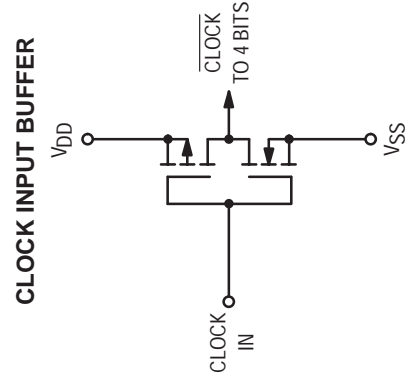
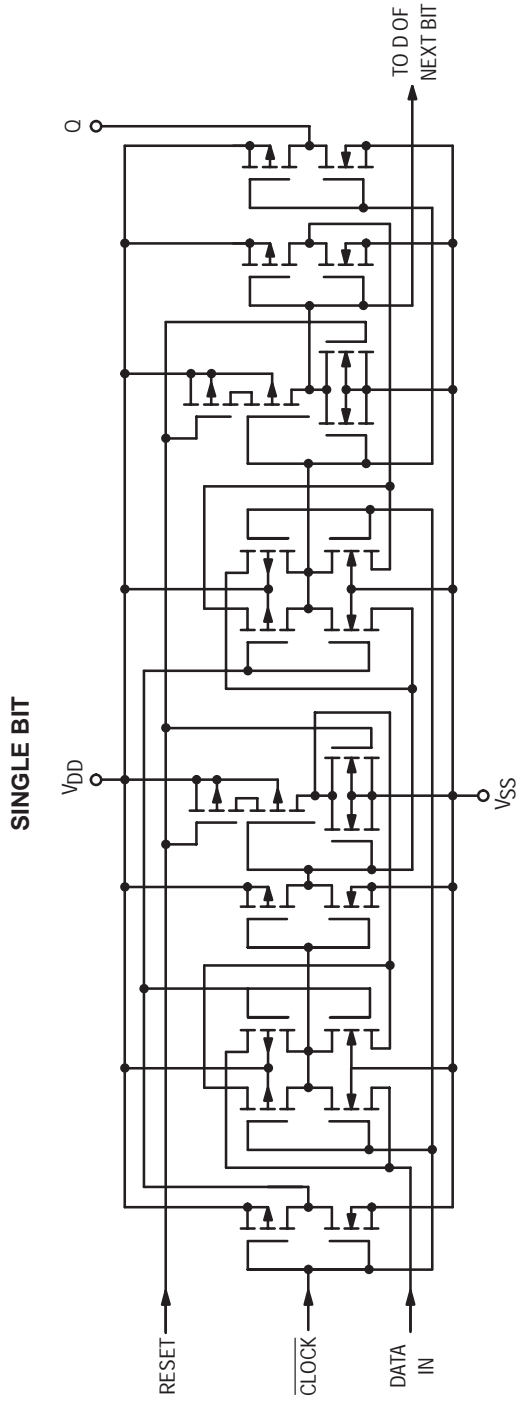


Figure 3. Setup and Hold Time Test Circuit and Waveforms

# MC14015B

## CIRCUIT SCHEMATICS

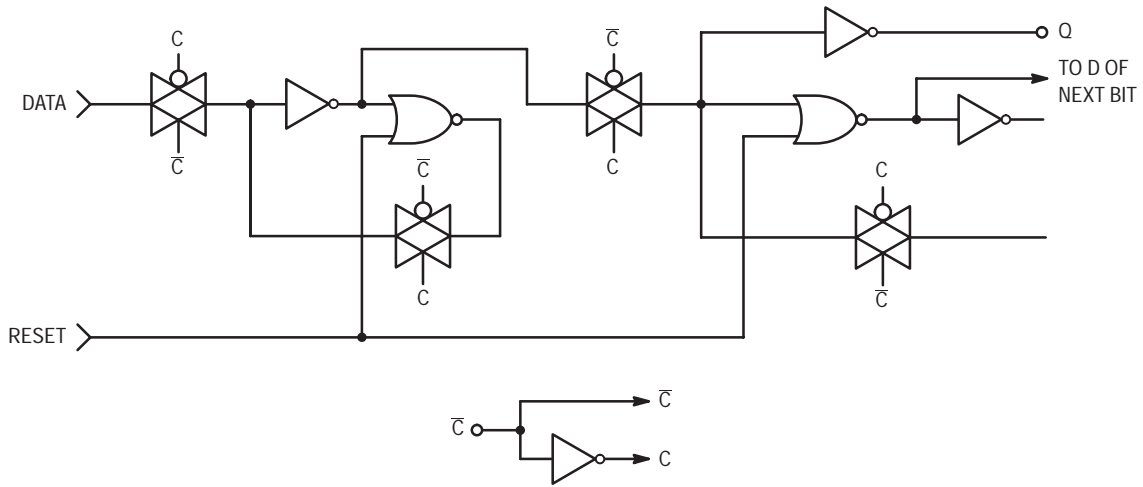




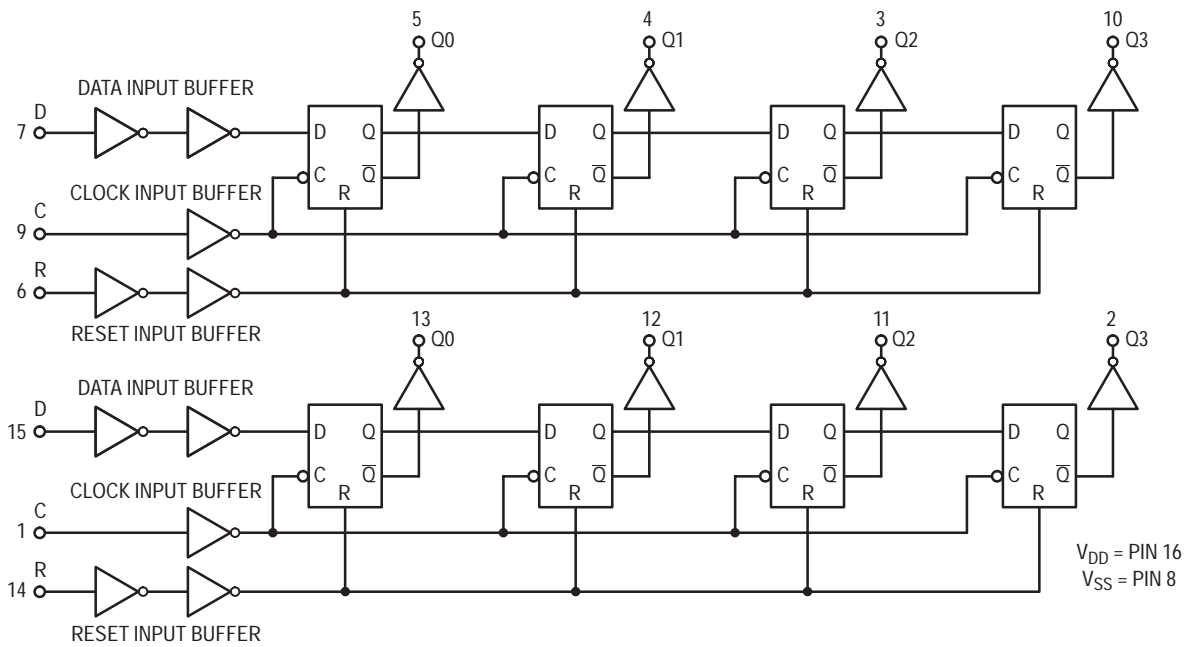
# MC14015B

## LOGIC DIAGRAMS

### SINGLE BIT



### COMPLETE DEVICE



# MC14016B

## Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise —  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  typical
- Pin-for-Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower  $R_{ON}$ , Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Control Pin	$\pm 10$	mA
$I_{SW}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

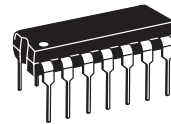
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



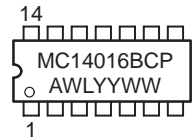
ON Semiconductor

<http://onsemi.com>

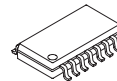
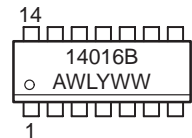
### MARKING DIAGRAMS



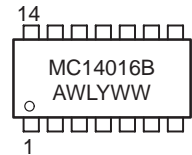
PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

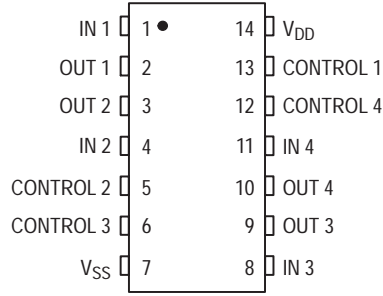
### ORDERING INFORMATION

Device	Package	Shipping
MC14016BCP	PDIP-14	2000/Box
MC14016BD	SOIC-14	55/Rail
MC14016BDR2	SOIC-14	2500/Tape & Reel
MC14016BF	SOEIAJ-14	See Note 1.
MC14016BFEL	SOEIAJ-14	See Note 1.

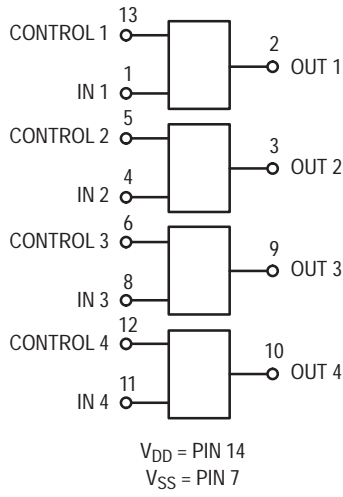
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14016B

## PIN ASSIGNMENT



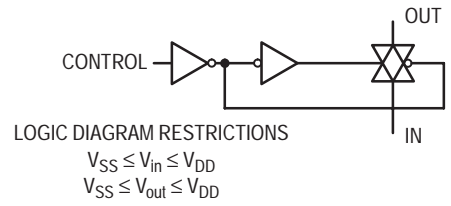
## BLOCK DIAGRAM



Control	Switch
0 = V <sub>SS</sub>	Off
1 = V <sub>DD</sub>	On

## LOGIC DIAGRAM

(1/4 OF DEVICE SHOWN)



# MC14016B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Figure	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Input Voltage Control Input	1	$V_{IL}$	5.0	—	—	—	1.5	0.9	—	—	Vdc
			10	—	—	—	1.5	0.9	—	—	
			15	—	—	—	1.5	0.9	—	—	
		$V_{IH}$	5.0	—	—	3.0	2.0	—	—	—	Vdc
			10	—	—	8.0	6.0	—	—	—	
			15	—	—	13	11	—	—	—	
Input Current Control	—	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
Input Capacitance Control Switch Input Switch Output Feed Through	—	$C_{in}$	—	—	—	—	5.0	—	—	—	pF
			—	—	—	—	5.0	—	—	—	
			—	—	—	—	5.0	—	—	—	
			—	—	—	—	0.2	—	—	—	
Quiescent Current (Per Package) (5.)	2,3	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu\text{A}$
			10	—	0.5	—	0.0010	0.5	—	15	
			15	—	1.0	—	0.0015	1.0	—	30	
"ON" Resistance ( $V_C = V_{DD}$ , $R_L = 10\text{ k}\Omega$ ) ( $V_{in} = + 5.0\text{ Vdc}$ ) ( $V_{in} = - 5.0\text{ Vdc}$ ) $V_{SS} = - 5.0\text{ Vdc}$ ( $V_{in} = \pm 0.25\text{ Vdc}$ )  ( $V_{in} = + 7.5\text{ Vdc}$ ) ( $V_{in} = - 7.5\text{ Vdc}$ ) $V_{SS} = - 7.5\text{ Vdc}$ ( $V_{in} = \pm 0.25\text{ Vdc}$ )  ( $V_{in} = + 10\text{ Vdc}$ ) ( $V_{in} = + 0.25\text{ Vdc}$ ) $V_{SS} = 0\text{ Vdc}$ ( $V_{in} = + 5.6\text{ Vdc}$ )  ( $V_{in} = + 15\text{ Vdc}$ ) ( $V_{in} = + 0.25\text{ Vdc}$ ) $V_{SS} = 0\text{ Vdc}$ ( $V_{in} = + 9.3\text{ Vdc}$ )	4,5,6	$R_{ON}$	5.0	—	600	—	300	660	—	840	Ohms
			5.0	—	600	—	300	660	—	840	
			5.0	—	600	—	280	660	—	840	
			7.5	—	360	—	240	400	—	520	
			7.5	—	360	—	240	400	—	520	
			7.5	—	360	—	180	400	—	520	
			10	—	600	—	260	660	—	840	
			10	—	600	—	310	660	—	840	
			10	—	600	—	310	660	—	840	
			15	—	360	—	260	400	—	520	
			15	—	360	—	260	400	—	520	
			15	—	360	—	300	400	—	520	
$\Delta$ "ON" Resistance Between any 2 circuits in a common package ( $V_C = V_{DD}$ ) ( $V_{in} = \pm 5.0\text{ Vdc}$ , $V_{SS} = - 5.0\text{ Vdc}$ ) ( $V_{in} = \pm 7.5\text{ Vdc}$ , $V_{SS} = - 7.5\text{ Vdc}$ )	—	$\Delta R_{ON}$	5.0	—	—	—	15	—	—	—	Ohms
			7.5	—	—	—	10	—	—	—	
Input/Output Leakage Current ( $V_C = V_{SS}$ ) ( $V_{in} = + 7.5$ , $V_{out} = - 7.5\text{ Vdc}$ ) ( $V_{in} = - 7.5$ , $V_{out} = + 7.5\text{ Vdc}$ )	—	—	7.5	—	$\pm 0.1$	—	$\pm 0.0015$	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
			7.5	—	$\pm 0.1$	—	$\pm 0.0015$	$\pm 0.1$	—	$\pm 1.0$	

NOTE: All unused inputs must be returned to  $V_{DD}$  or  $V_{SS}$  as appropriate for the circuit application.

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. For voltage drops across the switch ( $\Delta V_{switch}$ ) > 600 mV (> 300 mV at high temperature), excessive  $V_{DD}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{DD}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

# MC14016B

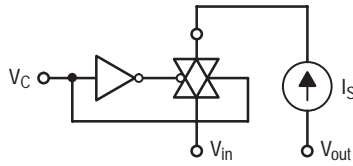
## ELECTRICAL CHARACTERISTICS (6.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Figure	Symbol	V <sub>DD</sub> Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Time ( $V_{SS} = 0 \text{ Vdc}$ ) $V_{in}$ to $V_{out}$ ( $V_C = V_{DD}$ , $R_L = 10 \text{ k}\Omega$ )	7	$t_{PLH}$ ,	5.0	—	15	45	ns
		$t_{PHL}$	10 15	— —	7.0 6.0	15 12	
Control to Output ( $V_{in} \leq 10 \text{ Vdc}$ , $R_L = 10 \text{ k}\Omega$ )	8	$t_{PHZ}$ ,	5.0	—	34	90	ns
		$t_{PLZ}$ ,	10	—	20	45	
		$t_{PZH}$ ,	15	—	15	35	
		$t_{PZL}$					
Crosstalk, Control to Output ( $V_{SS} = 0 \text{ Vdc}$ ) ( $V_C = V_{DD}$ , $R_{in} = 10 \text{ k}\Omega$ , $R_{out} = 10 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )	9	—	5.0	—	30	—	mV
			10	—	50	—	
			15	—	100	—	
Crosstalk between any two switches ( $V_{SS} = 0 \text{ Vdc}$ ) ( $R_L = 1.0 \text{ k}\Omega$ , $f = 1.0 \text{ MHz}$ , crosstalk = $20 \log_{10} \frac{V_{out1}}{V_{out2}}$ )	—	—	5.0	—	-80	—	dB
Noise Voltage ( $V_{SS} = 0 \text{ Vdc}$ ) ( $V_C = V_{DD}$ , $f = 100 \text{ Hz}$ )  ( $V_C = V_{DD}$ , $f = 100 \text{ kHz}$ )	10,11	—	5.0	—	24	—	nV/ $\sqrt{\text{Cycle}}$
			10	—	25	—	
			15	—	30	—	
			5.0	—	12	—	
			10	—	12	—	
			15	—	15	—	
Second Harmonic Distortion ( $V_{SS} = -5.0 \text{ Vdc}$ ) ( $V_{in} = 1.77 \text{ Vdc}$ , RMS Centered @ $0.0 \text{ Vdc}$ , $R_L = 10 \text{ k}\Omega$ , $f = 1.0 \text{ kHz}$ )	—	—	5.0	—	0.16	—	%
Insertion Loss ( $V_C = V_{DD}$ , $V_{in} = 1.77 \text{ Vdc}$ , $V_{SS} = -5.0 \text{ Vdc}$ , RMS centered = $0.0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )  $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	12	—	5.0	—	2.3	—	dB
				—	0.2	—	
				—	0.1	—	
				—	0.05	—	
				—			
Bandwidth (-3.0 dB) ( $V_C = V_{DD}$ , $V_{in} = 1.77 \text{ Vdc}$ , $V_{SS} = -5.0 \text{ Vdc}$ , RMS centered @ $0.0 \text{ Vdc}$ ) ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	12,13	BW	5.0	—	54	—	MHz
				—	40	—	
				—	38	—	
				—	37	—	
				—			
OFF Channel Feedthrough Attenuation ( $V_{SS} = -5.0 \text{ Vdc}$ ) ( $V_C = V_{SS}$ , $20 \log_{10} \frac{V_{out}}{V_{in}} = -50 \text{ dB}$ ) ( $R_L = 1.0 \text{ k}\Omega$ ) ( $R_L = 10 \text{ k}\Omega$ ) ( $R_L = 100 \text{ k}\Omega$ ) ( $R_L = 1.0 \text{ M}\Omega$ )	—	—	5.0	—	1250	—	kHz
				—	140	—	
				—	18	—	
				—	2.0	—	
				—			

6. The formulas given are for typical characteristics only at  $25^\circ\text{C}$ .

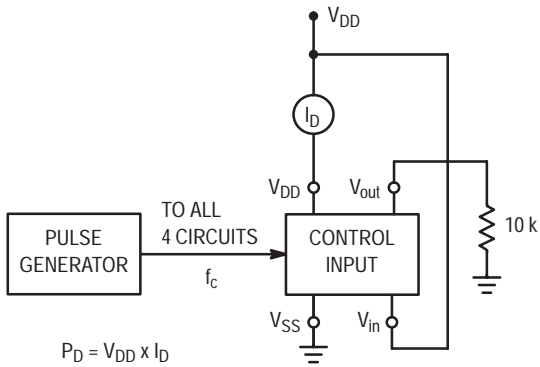
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14016B

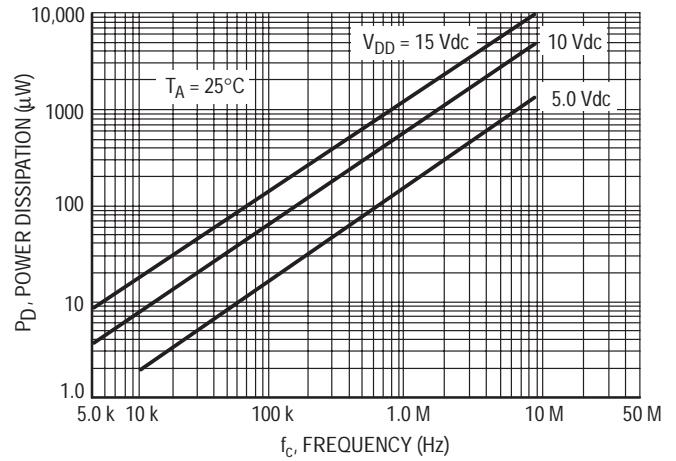


$V_{IL}$ :  $V_C$  is raised from  $V_{SS}$  until  $V_C = V_{IL}$ .  
 at  $V_C = V_{IL}$ :  $I_S = \pm 10 \mu A$  with  $V_{in} = V_{SS}$ ,  $V_{out} = V_{DD}$  or  $V_{in} = V_{DD}$ ,  $V_{out} = V_{SS}$ .  
 $V_{IH}$ : When  $V_C = V_{IH}$  to  $V_{DD}$ , the switch is ON and the  $R_{ON}$  specifications are met.

**Figure 1. Input Voltage Test Circuit**

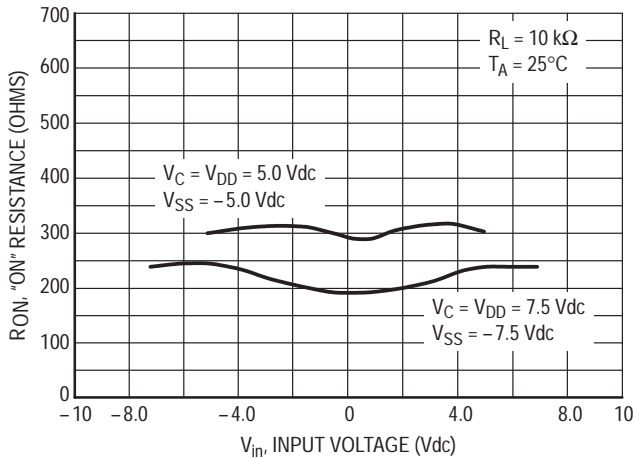


**Figure 2. Quiescent Power Dissipation Test Circuit**

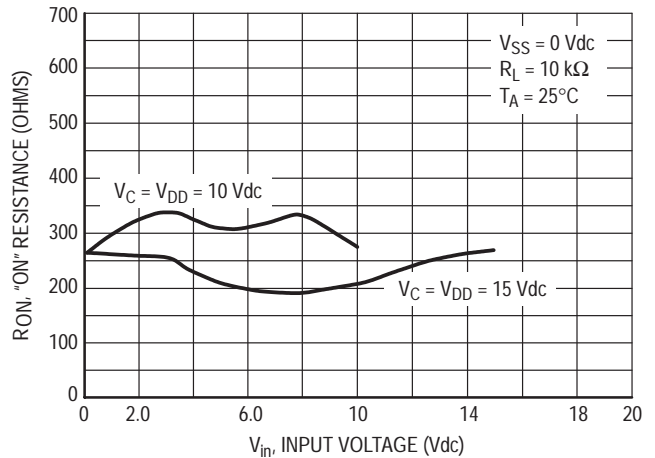


**Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)**

## TYPICAL $R_{ON}$ versus INPUT VOLTAGE



**Figure 4.  $V_{SS} = -5.0 V$  and  $-7.5 V$**



**Figure 5.  $V_{SS} = 0 V$**

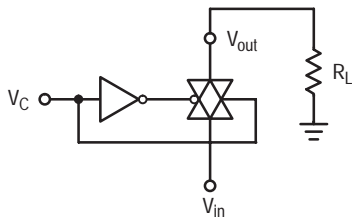


Figure 6.  $R_{ON}$  Characteristics Test Circuit

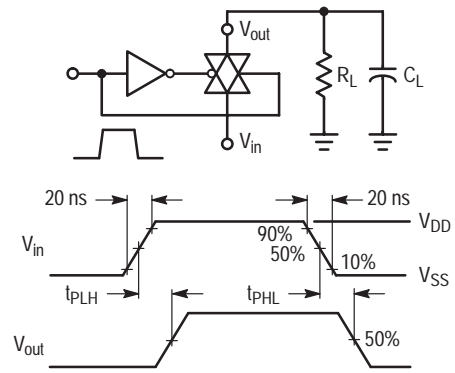


Figure 7. Propagation Delay Test Circuit and Waveforms

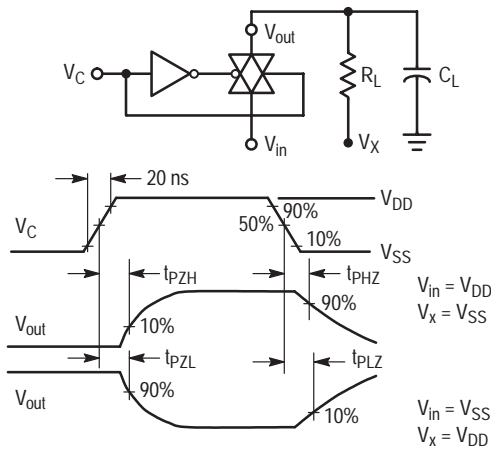


Figure 8. Turn-On Delay Time Test Circuit and Waveforms

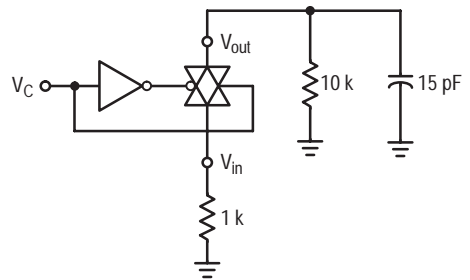


Figure 9. Crosstalk Test Circuit

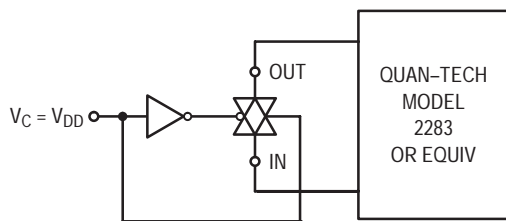


Figure 10. Noise Voltage Test Circuit

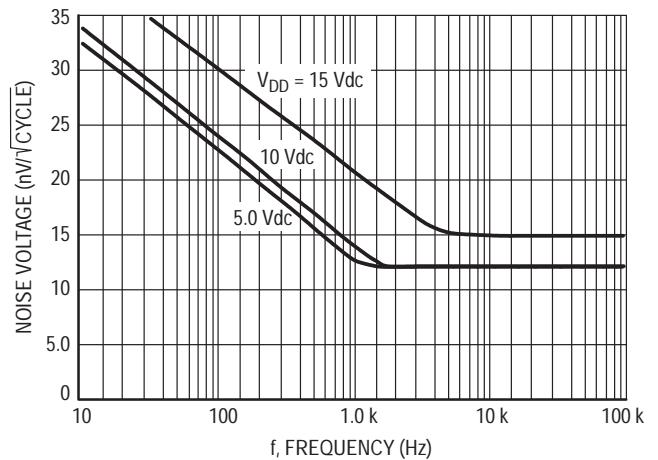


Figure 11. Typical Noise Characteristics

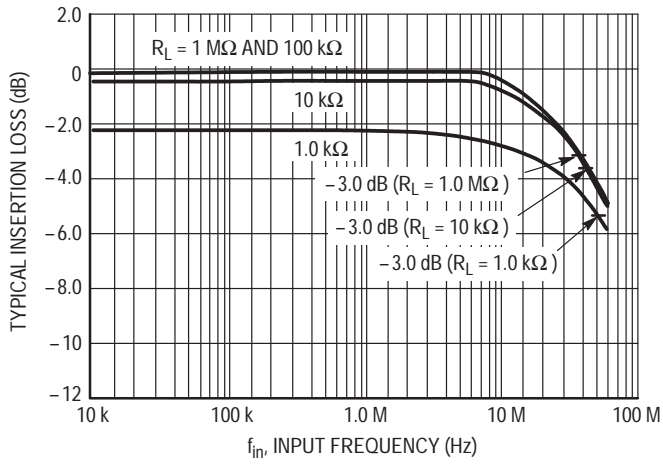


Figure 12. Typical Insertion Loss/Bandwidth Characteristics

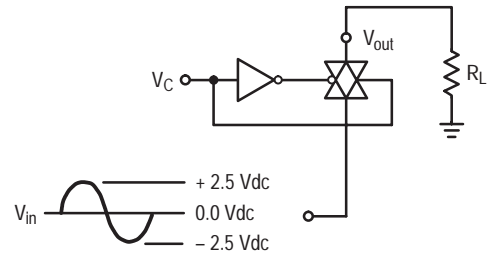


Figure 13. Frequency Response Test Circuit

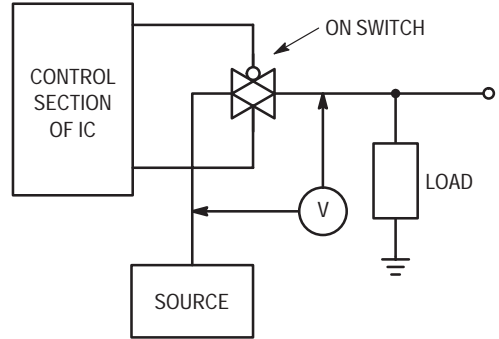


Figure 14.  $\Delta V$  Across Switch



# MC14016B

## APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V logic high at the control inputs; V<sub>SS</sub> = GND = 0 V logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>SS</sub>. The analog voltage must not swing higher than V<sub>DD</sub> or lower than V<sub>SS</sub>.

The example shows a 5 V<sub>p-p</sub> signal which allows no margin at either peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>SS</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.

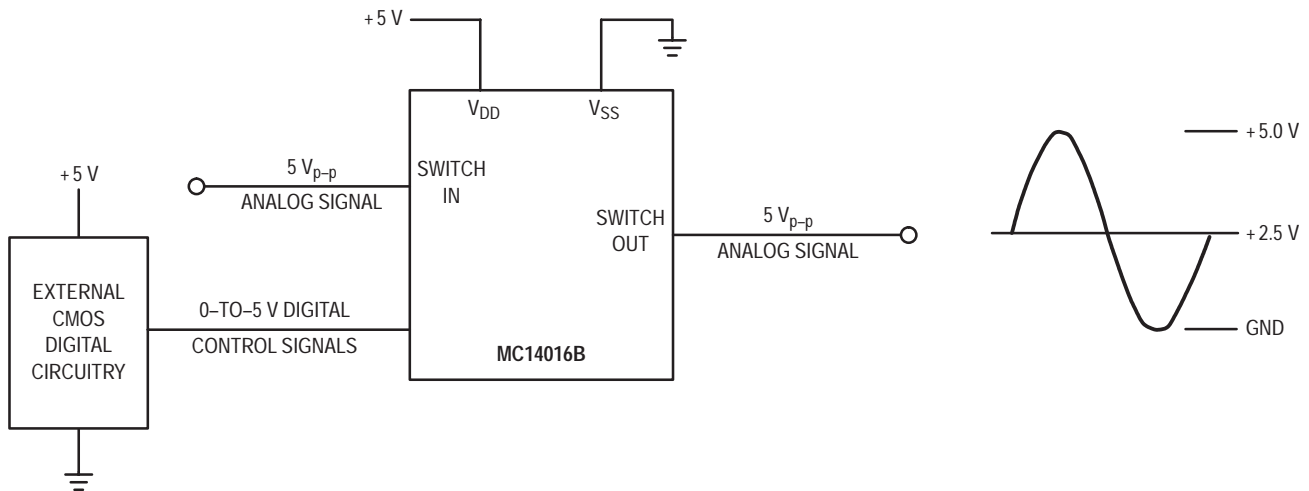


Figure A. Application Example



Figure B. External Germanium or Schottky Clipping Diodes

# MC14017B

## Decade Counter

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

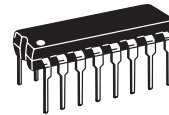
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



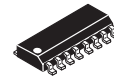
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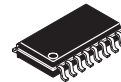
### MARKING DIAGRAMS



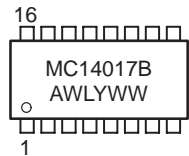
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

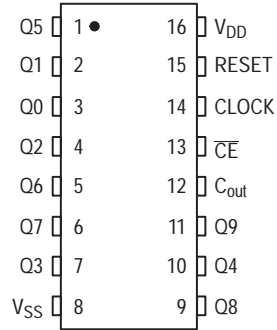
### ORDERING INFORMATION

Device	Package	Shipping
MC14017BCP	PDIP-16	2000/Box
MC14017BD	SOIC-16	48/Rail
MC14017BDR2	SOIC-16	2500/Tape & Reel
MC14017BF	SOEIAJ-16	See Note 1.
MC14017BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14017B

## PIN ASSIGNMENT

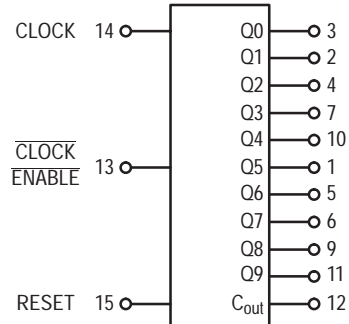


## FUNCTIONAL TRUTH TABLE (Positive Logic)

Clock	Clock Enable	Reset	Decode Output=n
0	X	0	n
X	1	0	n
X	X	1	Q0
↗	0	0	n+1
↘	X	0	n
X	↗	0	n
1	↘	0	n+1

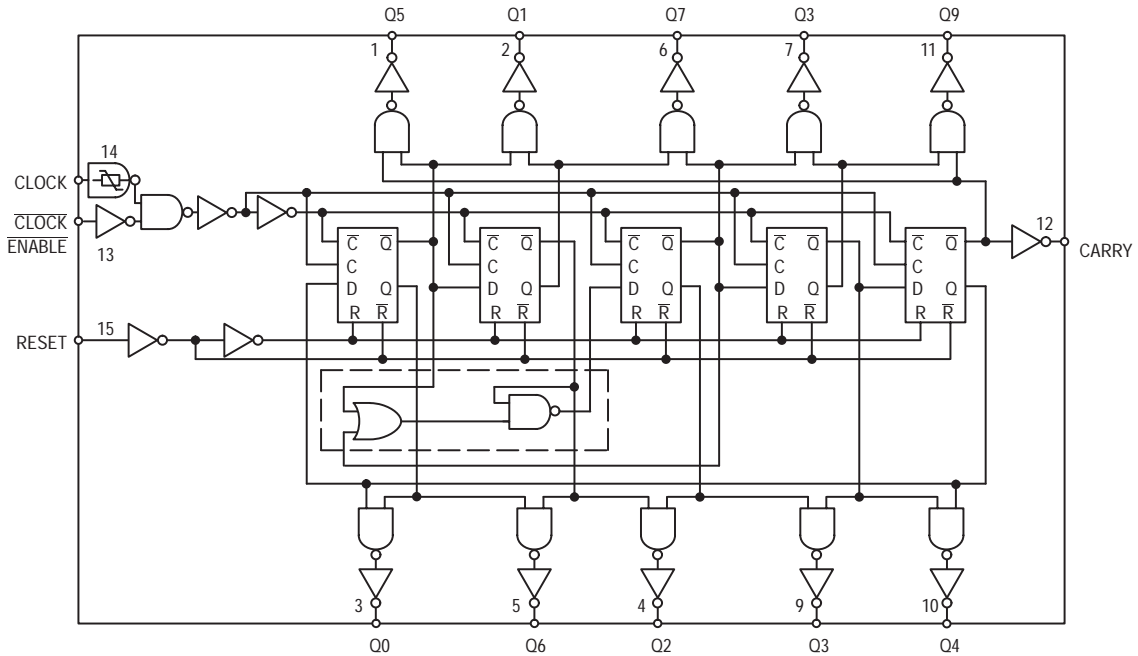
X = Don't Care. If n < 5 Carry = "1",  
Otherwise = "0".

## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

## LOGIC DIAGRAM



# MC14017B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
15		4.2	—	3.4	8.8	—	2.4	—			
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.27 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.55 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.83 μA/kHz) f + I <sub>DD</sub>							μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.0011.

# MC14017B

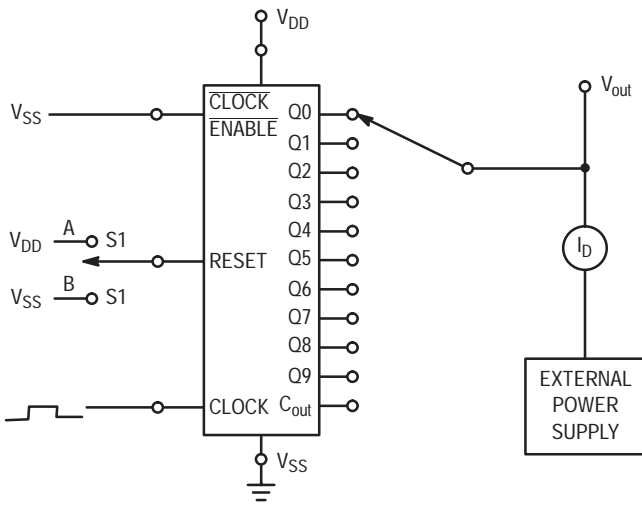
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to $C_{out}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Turn-Off Delay Time Reset to $C_{out}$ $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	$t_{w(H)}$	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	$t_{w(H)}$	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			—
Clock Enable Setup Time	$t_{su}$	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	$t_{rem}$	5.0 10 15	420 200 140	260 100 70	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14017B



	Output Sink Drive	Output Source Drive
Decode Outputs	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
$V_{GS} =$	$V_{DD}$	$-V_{DD}$
$V_{DS} =$	$V_{out}$	$V_{out} - V_{DD}$

Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

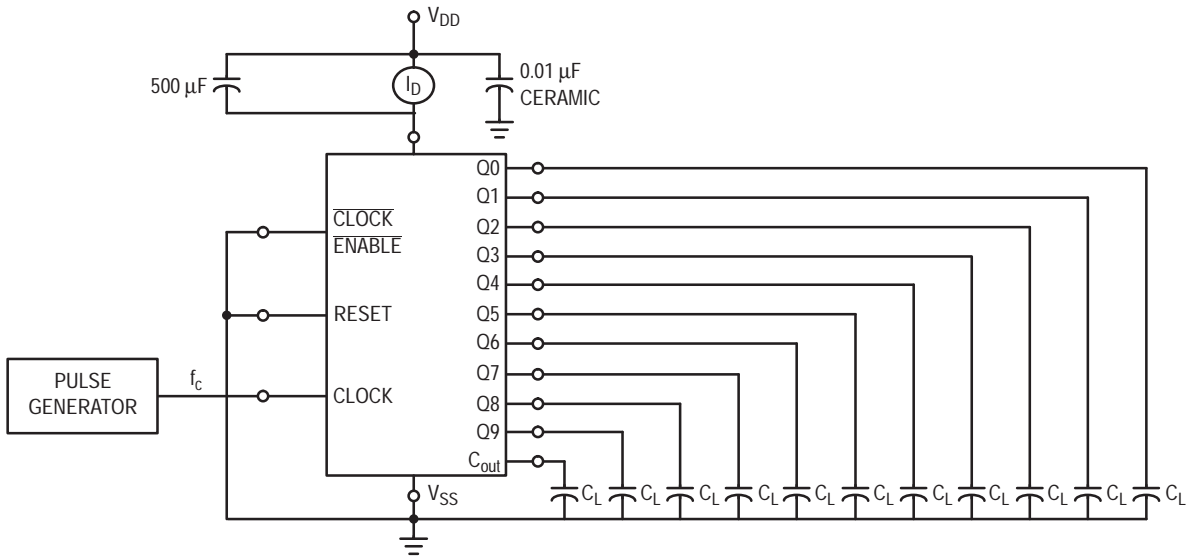


Figure 2. Typical Power Dissipation Test Circuit

# MC14017B

## APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

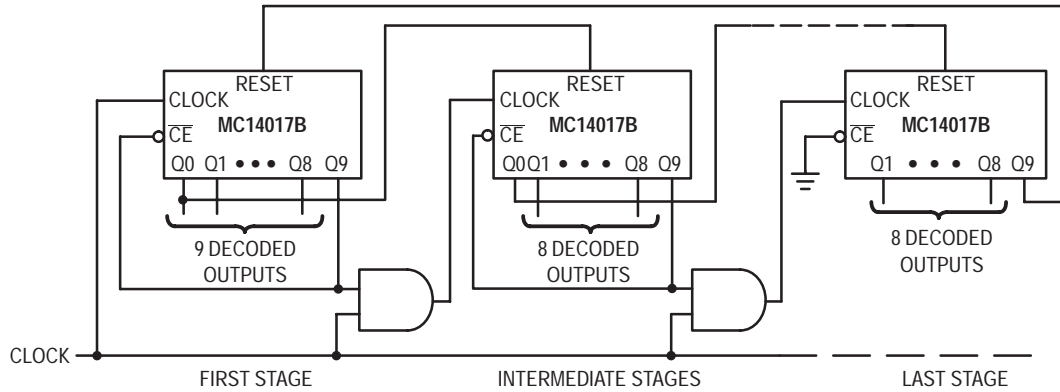


Figure 3. Counter Expansion

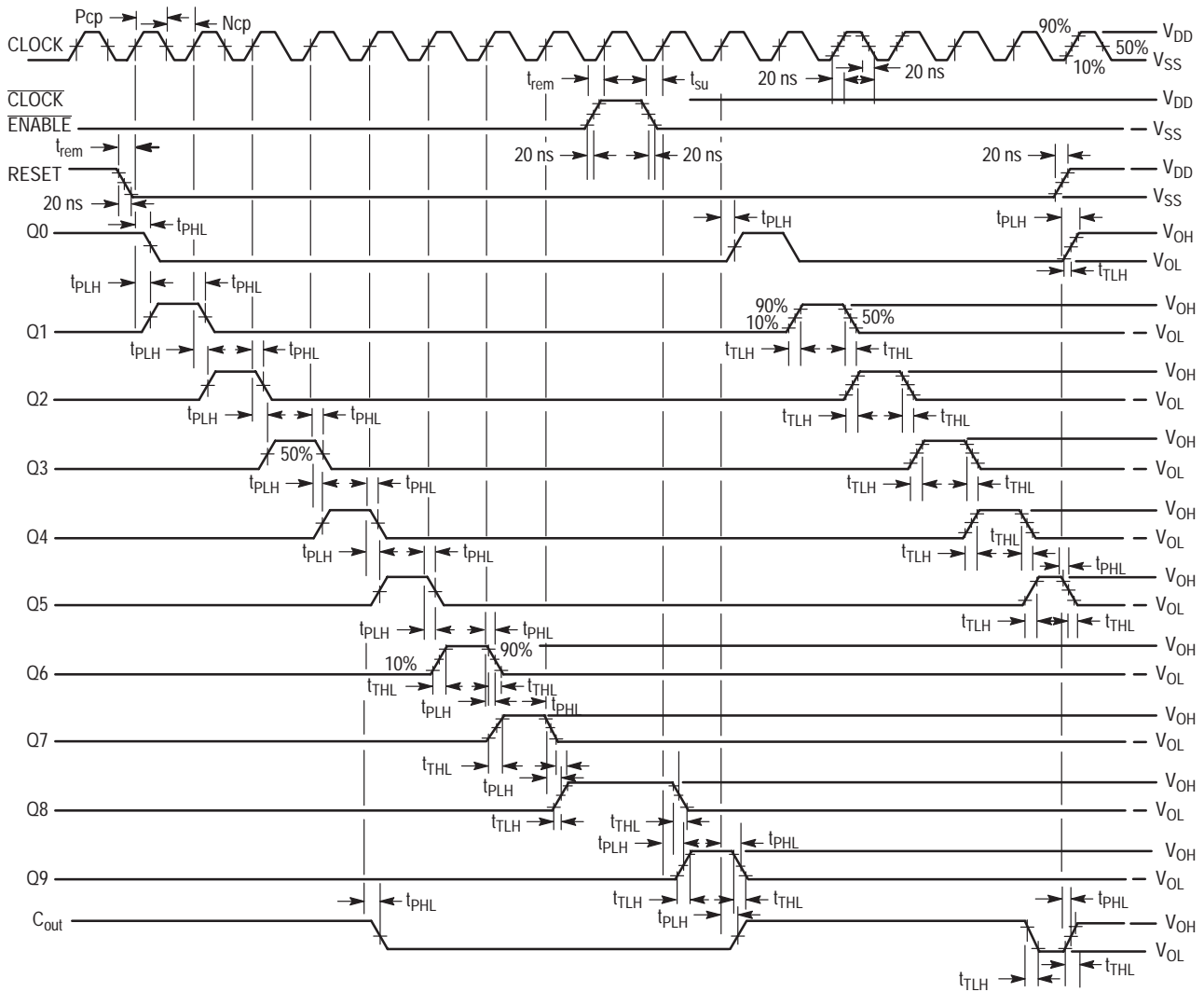


Figure 4. AC Measurement Definition and Functional Waveforms

# MC14018B

## Pre-settable Divide-By-N Counter

The MC14018B contains five Johnson counter stages which are asynchronously pre-settable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Pre-setting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective  $\bar{Q}$  outputs (inverted). A logic 1 on the reset input will cause all  $\bar{Q}$  outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate  $\bar{Q}$  outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

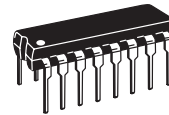
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



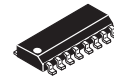
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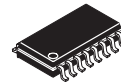
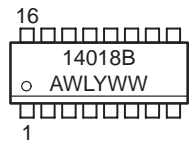
### MARKING DIAGRAMS



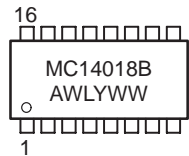
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14018BCP	PDIP-16	2000/Box
MC14018BD	SOIC-16	48/Rail
MC14018BDR2	SOIC-16	2500/Tape & Reel
MC14018BF	SOEIAJ-16	See Note 1.
MC14018BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.





# MC14018B

## PIN ASSIGNMENT

$D_{in}$	1	●	16	$V_{DD}$
JAM 1	2		15	R
JAM 2	3		14	C
$\bar{Q}2$	4		13	$\bar{Q}5$
$\bar{Q}1$	5		12	JAM 5
$\bar{Q}3$	6		11	$\bar{Q}4$
JAM 3	7		10	PE
$V_{SS}$	8		9	JAM 4

## FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\bar{Q}_n$
	0	0	X	$\bar{Q}_n$
	0	0	X	$\bar{D}_n^*$
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

\* $D_n$  is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

# MC14018B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level  “1” Level	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
15			—	0.05	—	0	0.05	—	0.05	—	
V <sub>in</sub> = 0 or V <sub>DD</sub>	“1” Level	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	“0” Level	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
15			—	4.0	—	6.75	4.0	—	4.0	—	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“1” Level	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
10			- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
15			- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub>							μAdc	
10	I <sub>T</sub> = (0.7 μA/kHz) f + I <sub>DD</sub>										
15	I <sub>T</sub> = (1.0 μA/kHz) f + I <sub>DD</sub>										

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14018B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 102 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 72 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	310 120 85	620 240 170	ns
Reset to $\bar{Q}$ $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$		5.0 10 15	— — —	370 150 100	740 300 200	ns
Preset Enable to $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$		5.0 10 15	— — —	370 150 100	740 300 200	ns
Setup Time Data (Pin 1) to Clock	$t_{su}$	5.0 10 15	200 100 80	0 0 0	— — —	ns
Jam Inputs to Preset Enable		5.0 10 15	200 100 80	0 0 0	— — —	ns
Data (Jam Inputs)–to–Preset Enable Hold Time	$t_h$	5.0 10 15	540 500 480	270 250 240	— — —	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	400 200 160	200 100 80	— — —	ns
Reset or Preset Enable Pulse Width	$t_{WH}$	5.0 10 15	290 130 110	145 65 55	— — —	ns
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.5 6.5 8.0	1.25 3.25 4.0	MHz

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

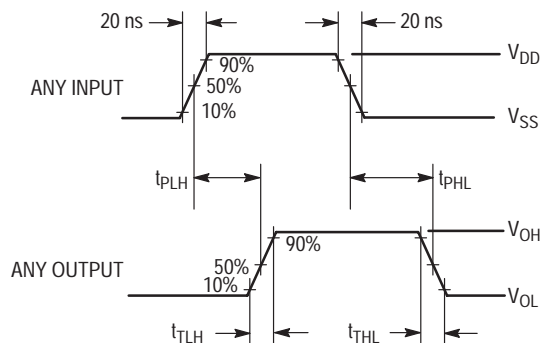
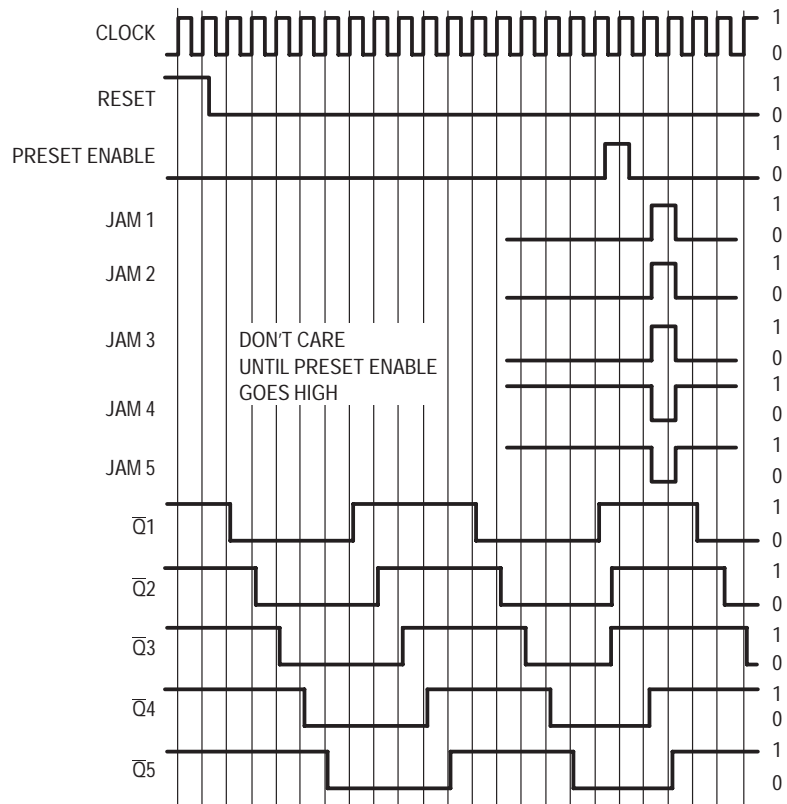


Figure 1. Switching Time Waveforms

# MC14018B

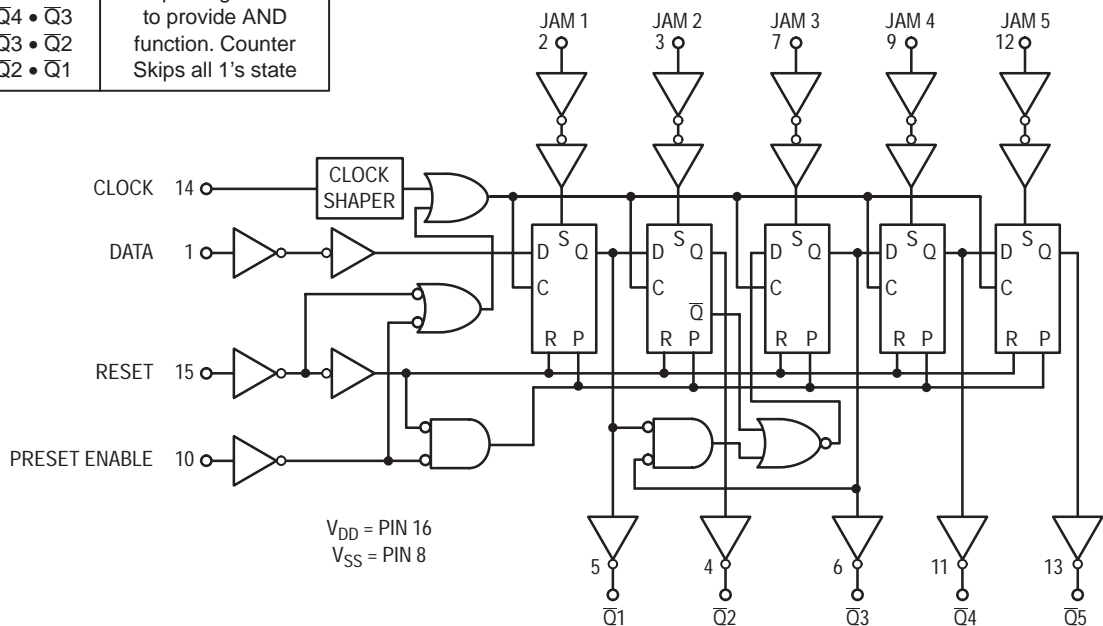
**TIMING DIAGRAM**  
( $\bar{Q}5$  Connected to Data Input)



**FUNCTION SELECTION**

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	$\bar{Q}5$ $\bar{Q}4$ $\bar{Q}3$ $\bar{Q}2$ $\bar{Q}1$	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	$\bar{Q}5 \cdot \bar{Q}4$ $\bar{Q}4 \cdot \bar{Q}3$ $\bar{Q}3 \cdot \bar{Q}2$ $\bar{Q}2 \cdot \bar{Q}1$	Gate package needed to provide AND function. Counter Skips all 1's state

**LOGIC DIAGRAM**



# MC14020B

## 14-Bit Binary Counter

The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

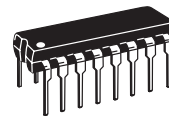
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



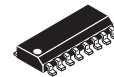
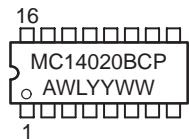
ON Semiconductor

<http://onsemi.com>

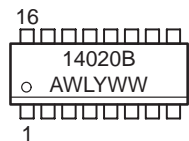
### MARKING DIAGRAMS



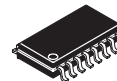
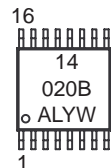
PDIP-16  
P SUFFIX  
CASE 648



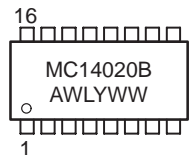
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14020BCP	PDIP-16	2000/Box
MC14020BD	SOIC-16	48/Rail
MC14020BDR2	SOIC-16	2500/Tape & Reel
MC14020BDT	TSSOP-16	96/Rail
MC14020BF	SOEIAJ-16	See Note 1.
MC14020BFEL	SOEIAJ-16	See Note 1.



- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14020B

## PIN ASSIGNMENT

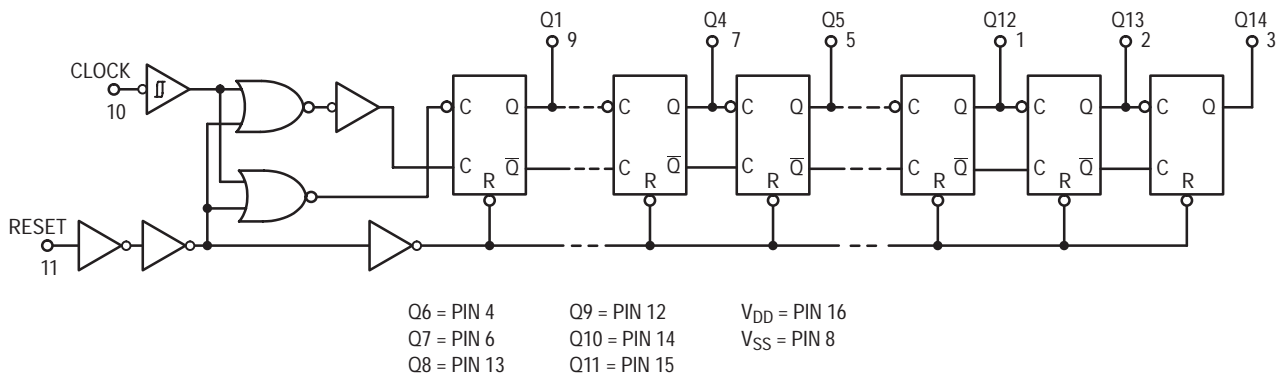
Q12	1	16	V <sub>DD</sub>
Q13	2	15	Q11
Q14	3	14	Q10
Q6	4	13	Q8
Q5	5	12	Q9
Q7	6	11	R
Q4	7	10	C
V <sub>SS</sub>	8	9	Q1

## TRUTH TABLE

Clock	Reset	Output State
	0	No Change
	0	Advance to Next State
X	1	All Outputs are Low

X = Don't Care

## LOGIC DIAGRAM



# MC14020B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
15		4.2	—	3.4	8.8	—	2.4	—			
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.42 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (0.85 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (1.43 μA/kHz)f + I <sub>DD</sub>							μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14020B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

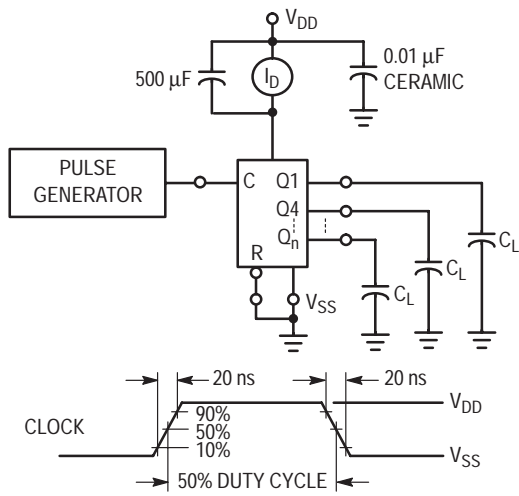
Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 175 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	260 115 80	520 230 160	ns
Clock to Q14 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 1735 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 772 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 535 \text{ ns}$		5.0 10 15	— — —	1820 805 560	3900 1725 1200	ns
Propagation Delay Time Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	500 165 125	140 55 38	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.0 6.0 8.0	1.0 3.0 4.0	MHz
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			—
Reset Pulse Width	$t_{WL}$	5.0 10 15	3000 550 420	320 120 80	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	130 50 30	65 25 15	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

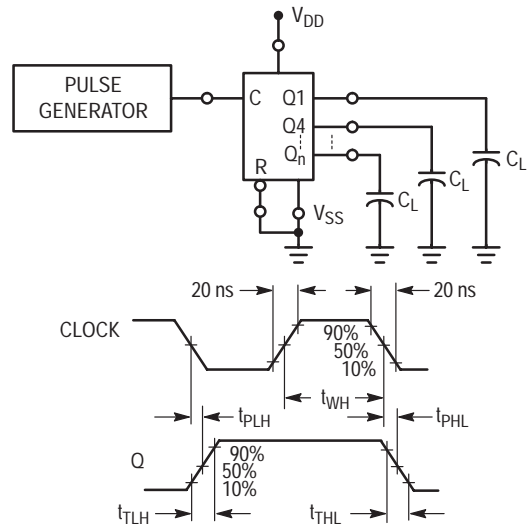
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



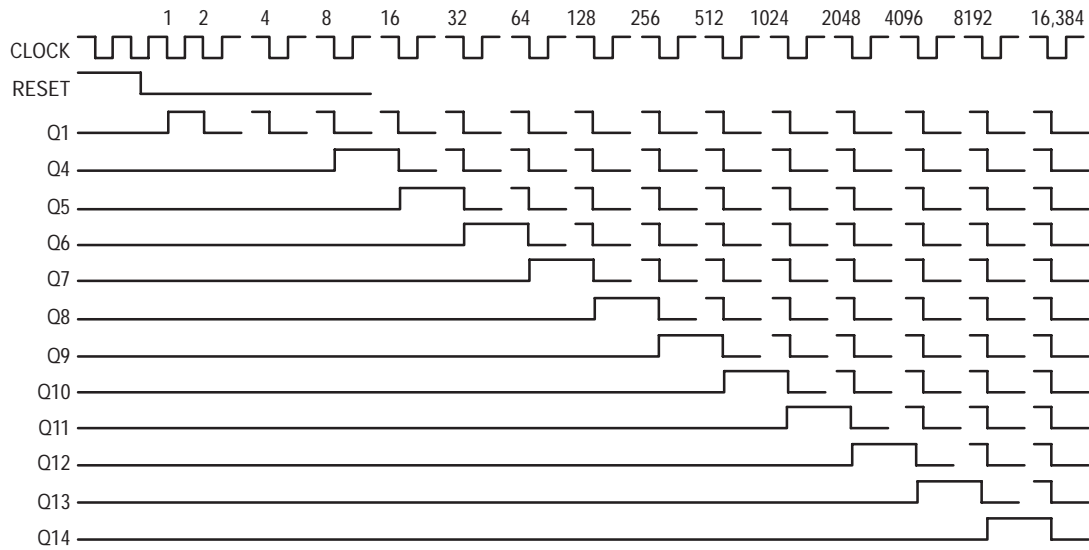
# MC14020B



**Figure 1. Power Dissipation Test Circuit and Waveform**



**Figure 2. Switching Time Test Circuit and Waveforms**



**Figure 3. Timing Diagram**

# MC14022B

## Octal Counter

The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B
- Triple Diode Protection on All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

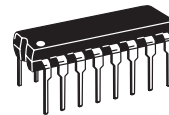
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



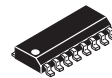
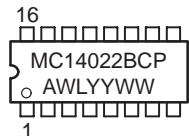
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### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



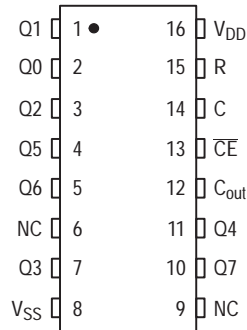
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14022BCP	PDIP-16	2000/Box
MC14022BD	SOIC-16	2400/Box
MC14022BDR2	SOIC-16	2500/Tape & Reel

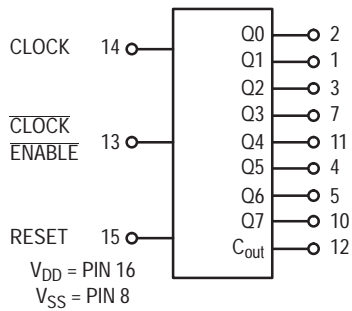
# MC14022B

## PIN ASSIGNMENT



NC = NO CONNECTION

## BLOCK DIAGRAM



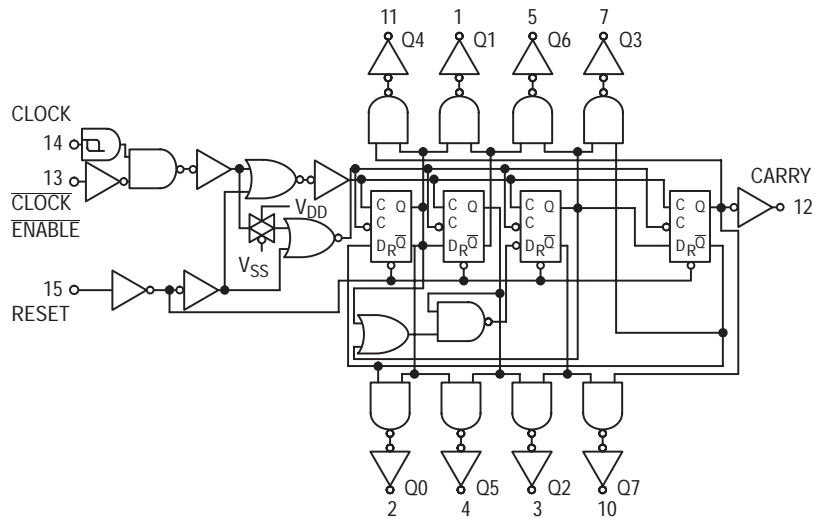
NC = PIN 6, 9

## FUNCTIONAL TRUTH TABLE (Positive Logic)

Clock	Clock Enable	Reset	Output=n
0	X	0	n
X	1	0	n
↗	0	0	n+1
↘	X	0	n
1	↘	0	n+1
X	↗	0	n
X	X	1	Q0

X = Don't Care. If  $n < 4$  Carry = 1, Otherwise = 0.

## LOGIC DIAGRAM



# MC14022B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3-)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.28 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (0.56 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (0.85 μA/kHz)f + I <sub>DD</sub>							μAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.00125.

# MC14022B

## SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ <sup>(7.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to C <sub>out</sub> $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	275 125 95	1000 460 350	ns
Turn-Off Delay Time Reset to C <sub>out</sub> $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	$t_{WH}$	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			—
Clock Enable Setup Time	$t_{su}$	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	$t_{rem}$	5.0 10 15	420 200 140	260 100 70	— — —	ns

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14022B

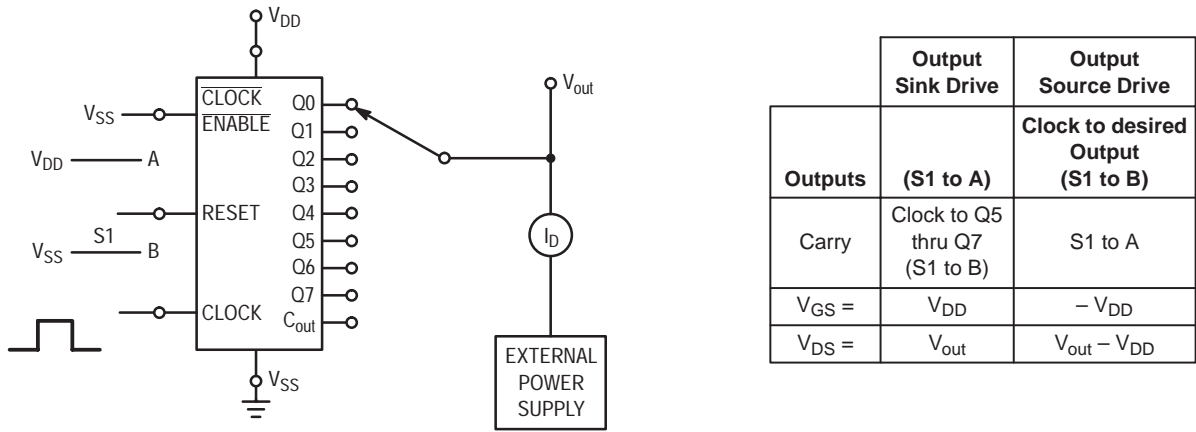


Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

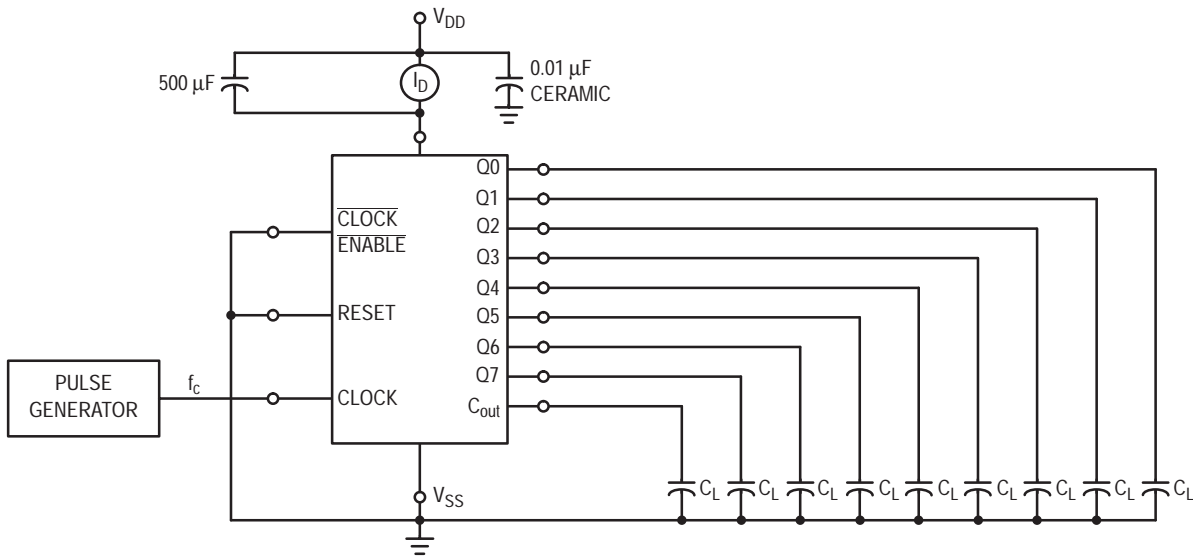


Figure 2. Typical Power Dissipation Test Circuit

## APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

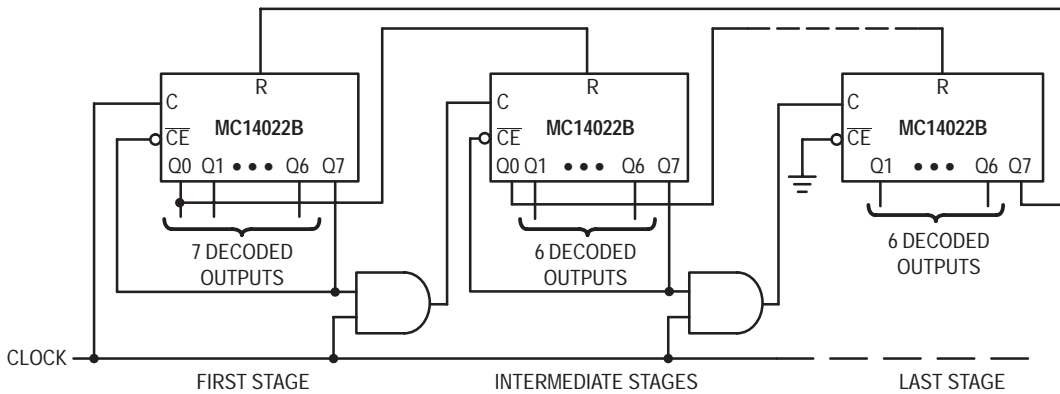


Figure 3. Counter Expansion

# MC14022B

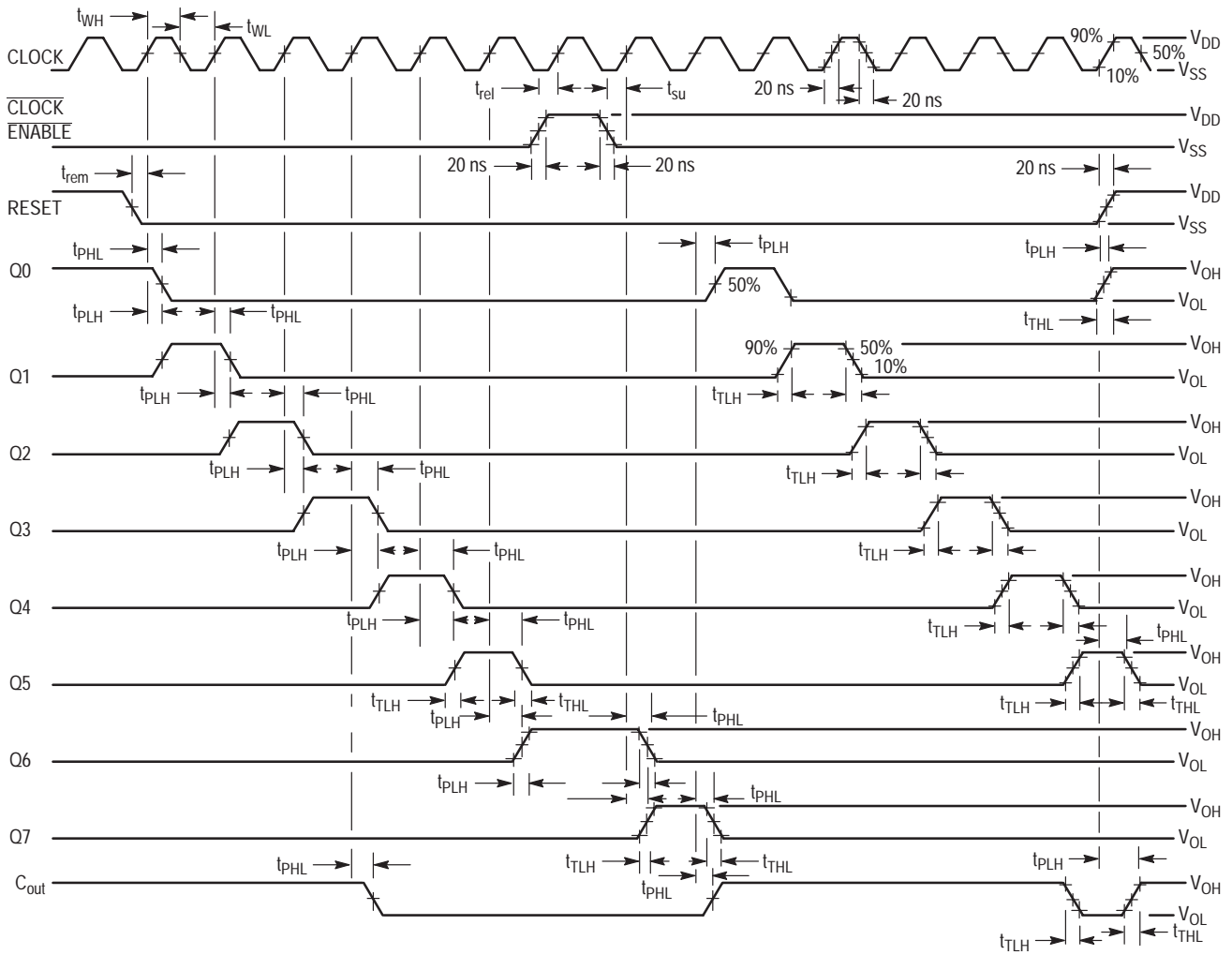


Figure 4. AC Measurement Definition and Functional Waveforms

# MC14024B

## 7-Stage Ripple Counter

The MC14024B is a 7-stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

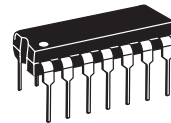
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



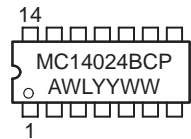
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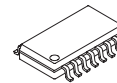
### MARKING DIAGRAMS



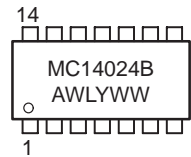
PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14024BCP	PDIP-14	2000/Box
MC14024BD	SOIC-14	2750/Box
MC14024BDR2	SOIC-14	2500/Tape & Reel
MC14024BF	SOEIAJ-14	See Note 1.
MC14024BFEL	SOEIAJ-14	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

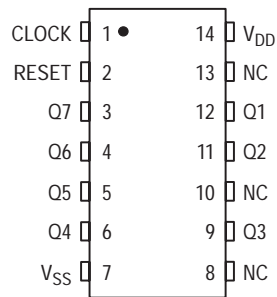


# MC14024B

## TRUTH TABLE

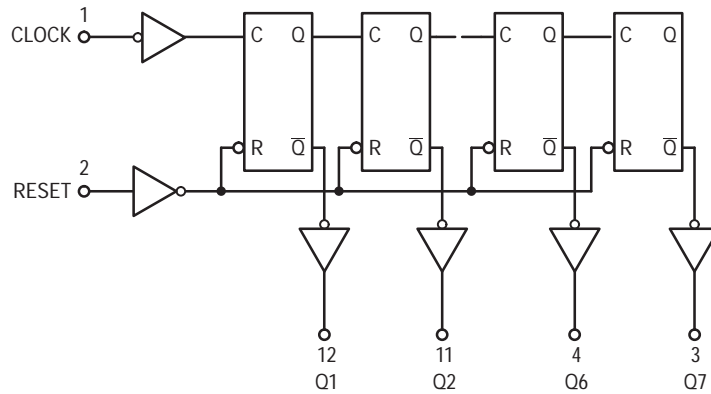
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
↗	0	No Change
↗	1	All Outputs Low
↘	0	Advance One Count
↘	1	All Outputs Low

## PIN ASSIGNMENT



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7  
 NC = NO CONNECTION

## LOGIC DIAGRAM



$Q3$  = PIN 9  
 $Q4$  = PIN 6  
 $Q5$  = PIN 5

# MC14024B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level  “1” Level	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
15			—	0.05	—	0	0.05	—	0.05	—	
V <sub>in</sub> = 0 or V <sub>DD</sub>	“1” Level	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	“0” Level	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
15			—	4.0	—	6.75	4.0	—	4.0	—	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“1” Level	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
10			- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
15			- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	µAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.31 µA/kHz) f + I <sub>DD</sub>							µAdc	
		10	I <sub>T</sub> = (0.60 µA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (1.89 µA/kHz) f + I <sub>DD</sub>								

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14024B

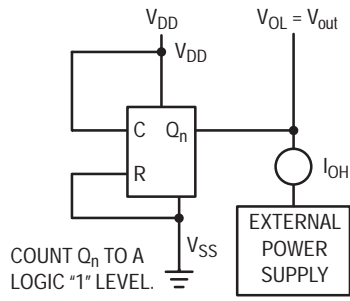
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 295 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$ Clock to Q7 $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 915 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 367 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 275 \text{ ns}$ Reset to $Q_n$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	380 150 110  1000 400 300  500 250 180	600 230 175  2000 750 565  800 400 300	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	500 165 125	200 60 40	— — —	ns
Reset Pulse Width	$t_{WH}$	5.0 10 15	600 350 260	375 200 150	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	625 190 145	250 75 50	— — —	ns
Clock Input Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	— — —	1.0 8.0 200	s ms $\mu\text{s}$
Input Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.5 8.0 12	1.0 3.0 4.0	MHz

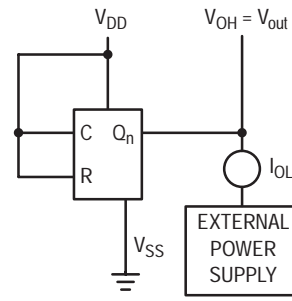
7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

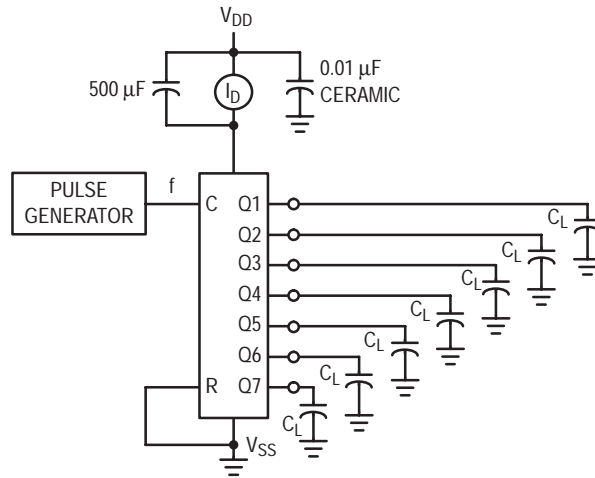
# MC14024B



**Figure 1. Typical Output Source Characteristics Test Circuit**

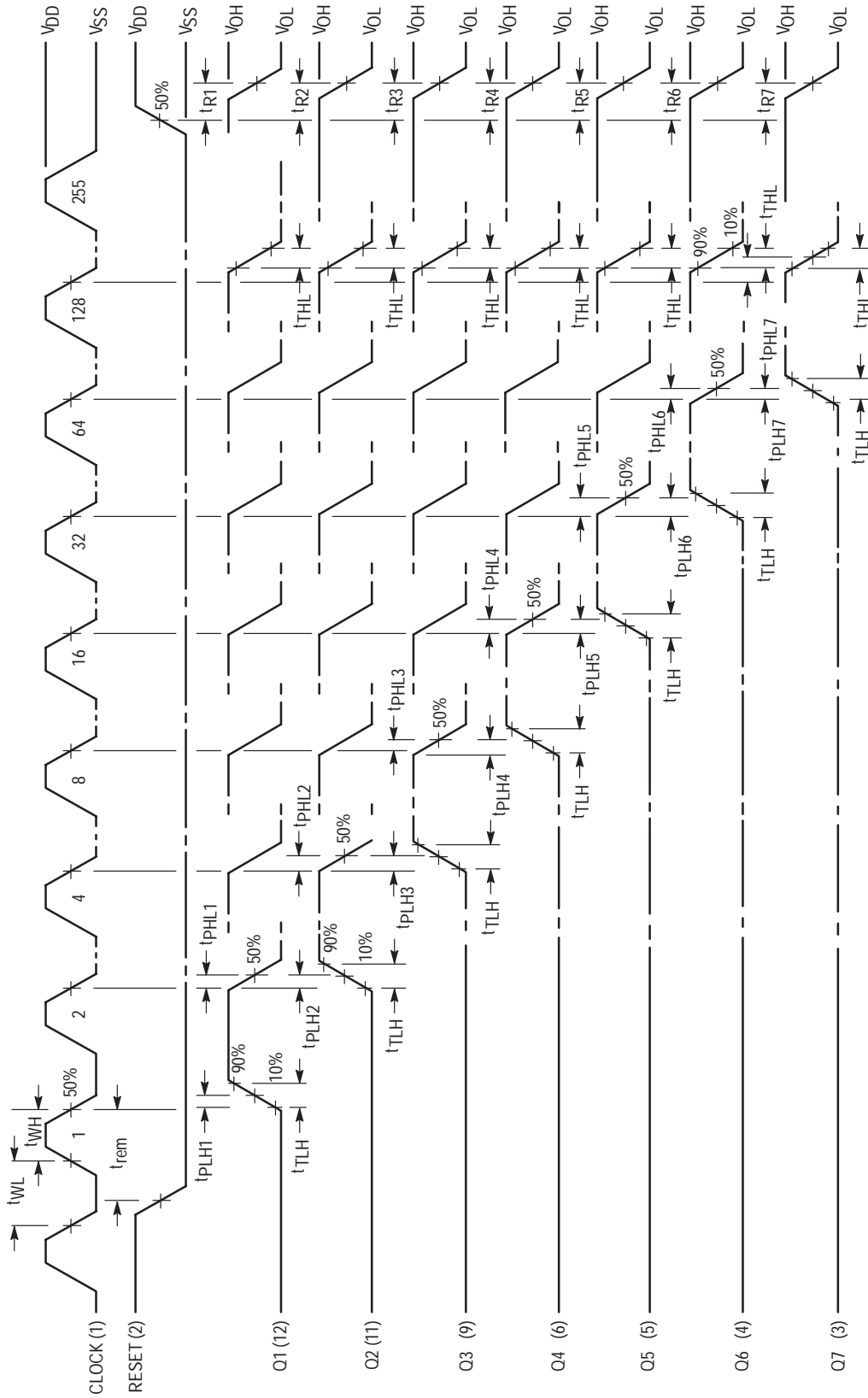


**Figure 2. Typical Output Sink Characteristics Test Circuit**



**Figure 3. Power Dissipation Test Circuit**

# MC14024B



Input  $t_{TLH}$  and  $t_{THL} = 20$  ns

Figure 4. Functional Waveforms

# MC14027B

## Dual J-K Flip-Flop

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design —  
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

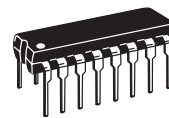
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



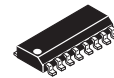
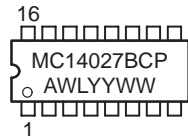
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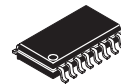
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14027BCP	PDIP-16	2000/Box
MC14027BD	SOIC-16	2400/Box
MC14027BDR2	SOIC-16	2500/Tape & Reel
MC14027BF	SOEIAJ-16	See Note 1.
MC14027BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14027B

## TRUTH TABLE

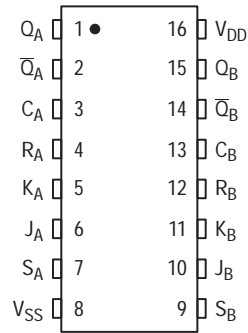
Inputs					Outputs*		
C†	J	K	S	R	Q <sub>n</sub> ‡	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
↗	1	X	0	0	0	1	0
↗	X	0	0	0	1	1	0
↗	0	X	0	0	0	0	1
↗	X	1	0	0	1	0	1
↗	1	1	0	0	Q <sub>0</sub>	Q̄ <sub>0</sub>	Q <sub>0</sub>
↘	X	X	0	0	X	Q <sub>n</sub>	Q̄ <sub>n</sub>
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

X = Don't Care  
† = Level Change

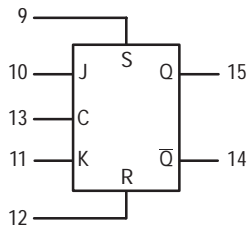
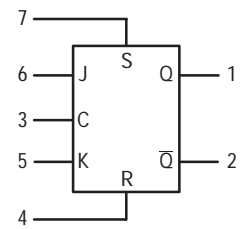
‡ = Present State  
\* = Next State

No  
Change

## PIN ASSIGNMENT



## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

# MC14027B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.



# MC14027B

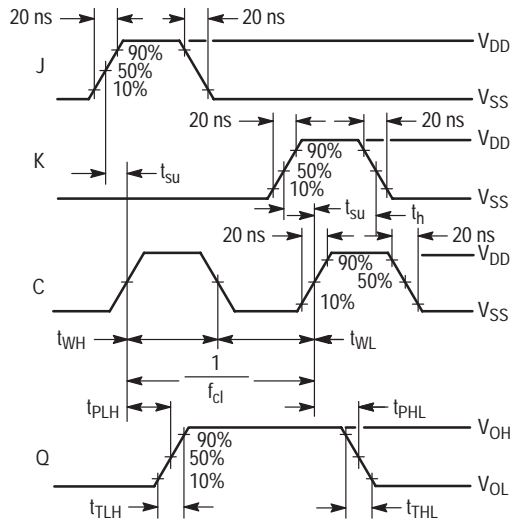
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Times** Clock to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Set to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ Reset to Q, Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	175 75 50  175 75 50  350 100 75	350 150 100  350 150 100  450 200 150	ns
Setup Times	$t_{su}$	5.0 10 15	140 50 35	70 25 17	— — —	ns
Hold Times	$t_h$	5.0 10 15	140 50 35	70 25 17	— — —	ns
Clock Pulse Width	$t_{WH}, t_{WL}$	5.0 10 15	330 110 75	165 55 38	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.0 9.0 13	1.5 4.5 6.5	MHz
Clock Pulse Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Removal Times  Set  Reset	$t_{rem}$	5 10 15  5 10 15	90 45 35  50 25 20	10 5 3  -30 -15 -10	— — —  — — —	ns
Set and Reset Pulse Width	$t_{WH}$	5.0 10 15	250 100 70	125 50 35	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

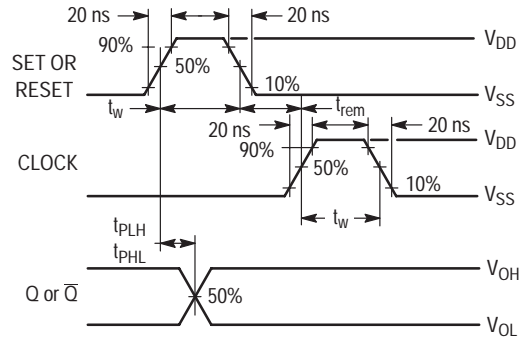
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14027B



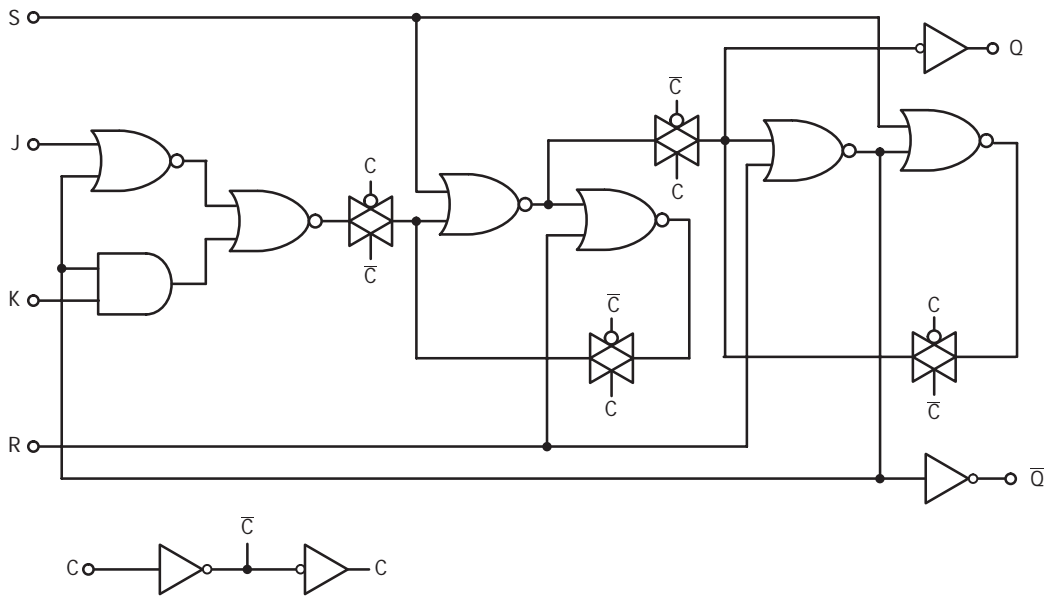
Inputs R and S low.  
 For the measurement of  $t_{WH}$ ,  $1/f_{cl}$ , and  $P_D$   
 the Inputs J and K are kept high.

**Figure 1. Dynamic Signal Waveforms (J, K, Clock, and Output)**



**Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)**

## LOGIC DIAGRAM (1/2 of Device Shown)



# MC14028B

## BCD-To-Decimal Decoder Binary-To-Octal Decoder

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

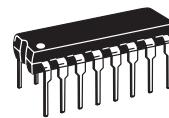
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



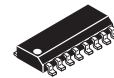
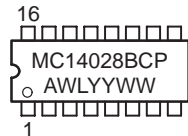
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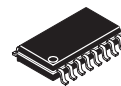
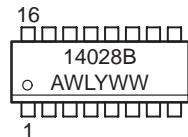
### MARKING DIAGRAMS



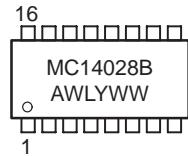
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

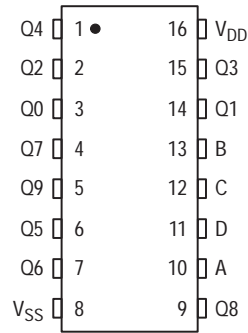
### ORDERING INFORMATION

Device	Package	Shipping
MC14028BCP	PDIP-16	2000/Box
MC14028BD	SOIC-16	2400/Box
MC14028BDR2	SOIC-16	2500/Tape & Reel
MC14028BF	SOEIAJ-16	See Note 1.
MC14028BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14028B

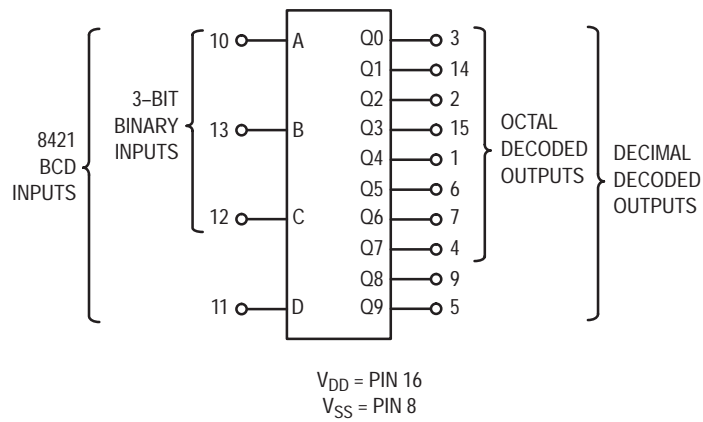
## PIN ASSIGNMENT



## TRUTH TABLE

D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

## BLOCK DIAGRAM



# MC14028B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0  "1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub>							μAdc
10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub>									
15	I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub>									

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

## SWITCHING CHARACTERISTICS<sup>(7.)</sup> (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

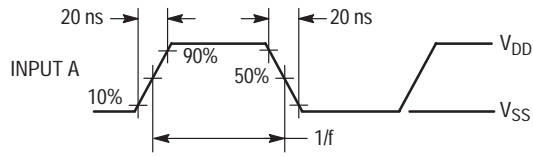
Characteristic	Symbol	V <sub>DD</sub>	Min	Typ <sup>(8.)</sup>	Max	Unit
Output Rise and Fall Time t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time t <sub>PLH</sub> , t <sub>PHL</sub> = (1.7 ns/pF) C <sub>L</sub> + 215 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.66 ns/pF) C <sub>L</sub> + 97 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.5 ns/pF) C <sub>L</sub> + 65 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	—	300	600	ns
		10	—	130	260	
		15	—	90	180	

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14028B

Inputs B, C, and D switching in respect to a BCD code.



All outputs connected to respective  $C_L$  loads.  $f$  in respect to a system clock.

Inputs A, B, and D low.

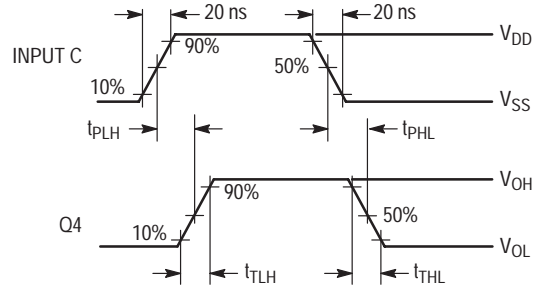
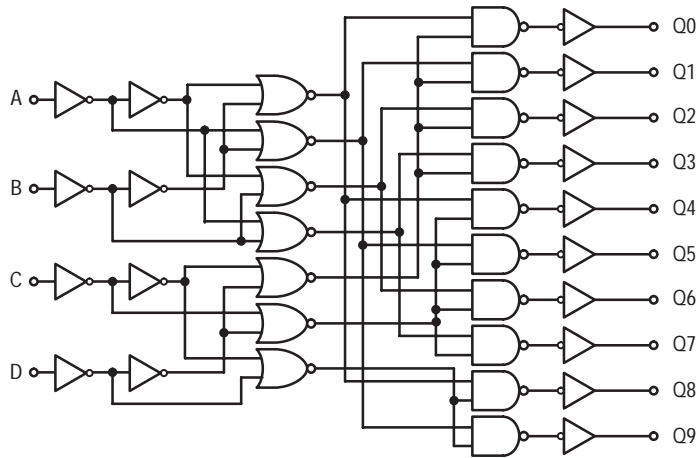


Figure 1. Dynamic Signal Waveforms

## LOGIC DIAGRAM



# MC14028B

## APPLICATIONS INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

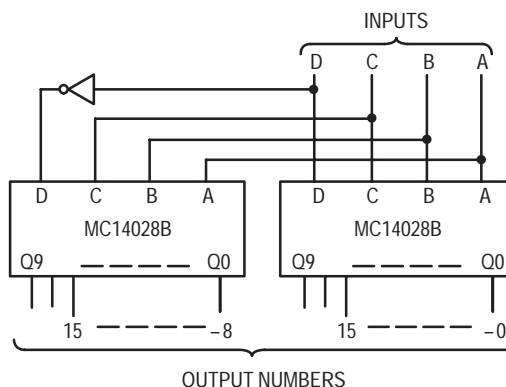


Figure 2. Code Conversion Circuit and Truth Table

Inputs				Output Numbers																Code and Redefined Output Numbers						
																				Hexadecimal			Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0				0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1				1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0		2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3		3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4		4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2				3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1			4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2			
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5				
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6				5
1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	10	12	7	9			6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5		6
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6		7
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7		7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8		8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9		9

# MC14028B

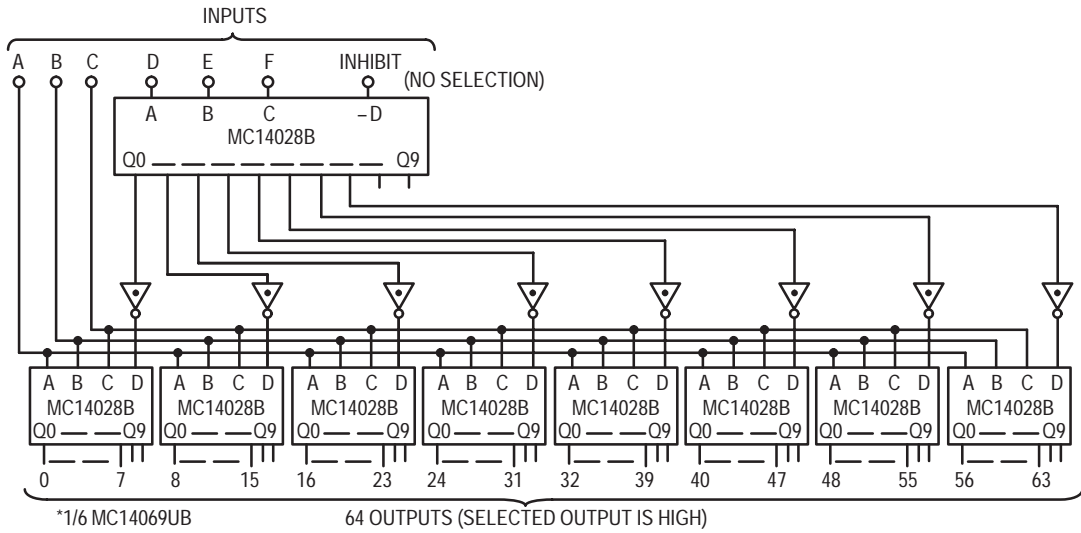


Figure 3. Six-Bit Binary 1-of-64 Decoder

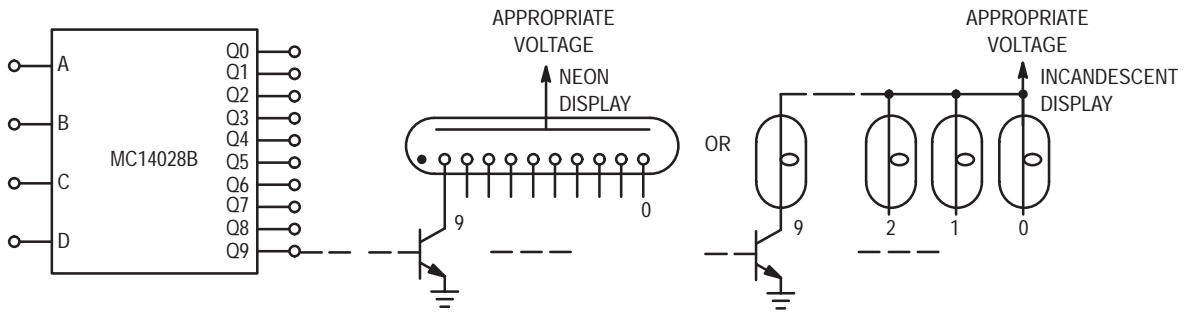


Figure 4. Decimal Digit Display Application



# MC14029B

## Binary/Decade Up/Down Counter

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

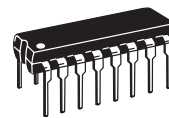
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



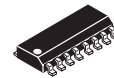
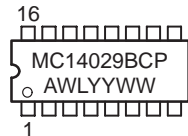
ON Semiconductor

<http://onsemi.com>

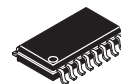
### MARKING DIAGRAMS



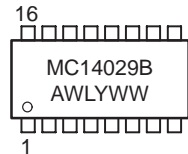
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14029BCP	PDIP-16	2000/Box
MC14029BD	SOIC-16	2400/Box
MC14029BDR2	SOIC-16	2500/Tape & Reel
MC14029BF	SOEIAJ-16	See Note 1.
MC14029BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14029B

## PIN ASSIGNMENT

PE	1 ●	16	V <sub>DD</sub>
Q3	2	15	CLK
P3	3	14	Q2
P0	4	13	P2
C <sub>in</sub>	5	12	P1
Q0	6	11	Q1
C <sub>out</sub>	7	10	U/D
V <sub>SS</sub>	8	9	B/D

## TRUTH TABLE

Carry In	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink I <sub>OL</sub>	10	-1.6	—	-1.3	-2.25	—	-0.9	—	mAdc
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.58 μA/kHz) f + I <sub>DD</sub>							μAdc
10	I <sub>T</sub> = (1.20 μA/kHz) f + I <sub>DD</sub>									
15	I <sub>T</sub> = (1.70 μA/kHz) f + I <sub>DD</sub>									

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14029B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	All Types			Unit	
			Min	Typ (8.)	Max		
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns	
Propagation Delay Time Clk to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	200 100 90	400 200 180	ns	
Clk to $\overline{C_{out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	250 130 85	500 260 190	ns	
$\overline{C_{in}}$ to $\overline{C_{out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	175 50 50	360 120 100	ns	
PE to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	235 100 80	470 200 160	ns	
PE to $\overline{C_{out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	320 145 105	640 290 210	ns	
Clock Pulse Width	$t_{W(cl)}$	5.0 10 15	180 80 60	90 40 30	— — —	ns	
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	4.0 8.0 10	2.0 4.0 5.0	MHz	
Preset Removal Time The Preset Signal must be low prior to a positive-going transition of the clock.	$t_{rem}$	5.0 10 15	160 80 60	80 40 30	— — —	ns	
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$	
$\overline{C_{in}}$ Setup Time	$t_{su}$	5.0 10 15	150 60 40	75 30 20	— — —	ns	
Up/Down Setup Time		5.0 10 15	340 140 100	170 70 50	— — —	ns	
Binary/Decade Setup Time		5.0 10 15	320 140 100	160 70 50	— — —	ns	
Preset Enable Pulse Width		$t_w$	5.0 10 15	130 70 50	65 35 25	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14029B

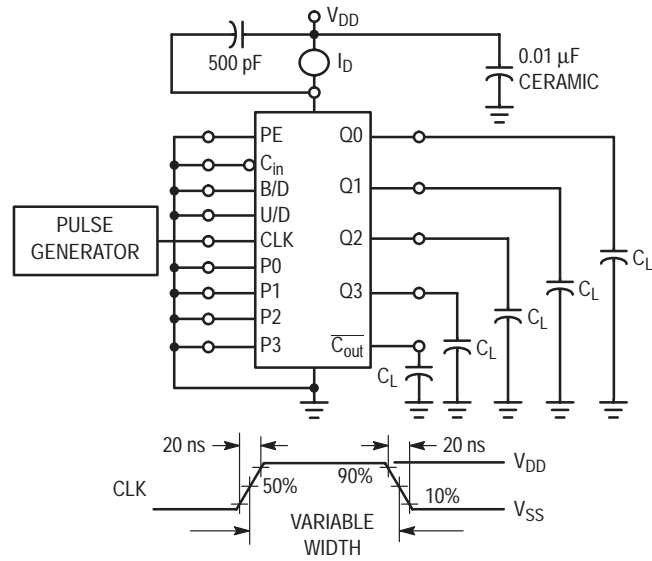


Figure 1. Power Dissipation Test Circuit and Waveform

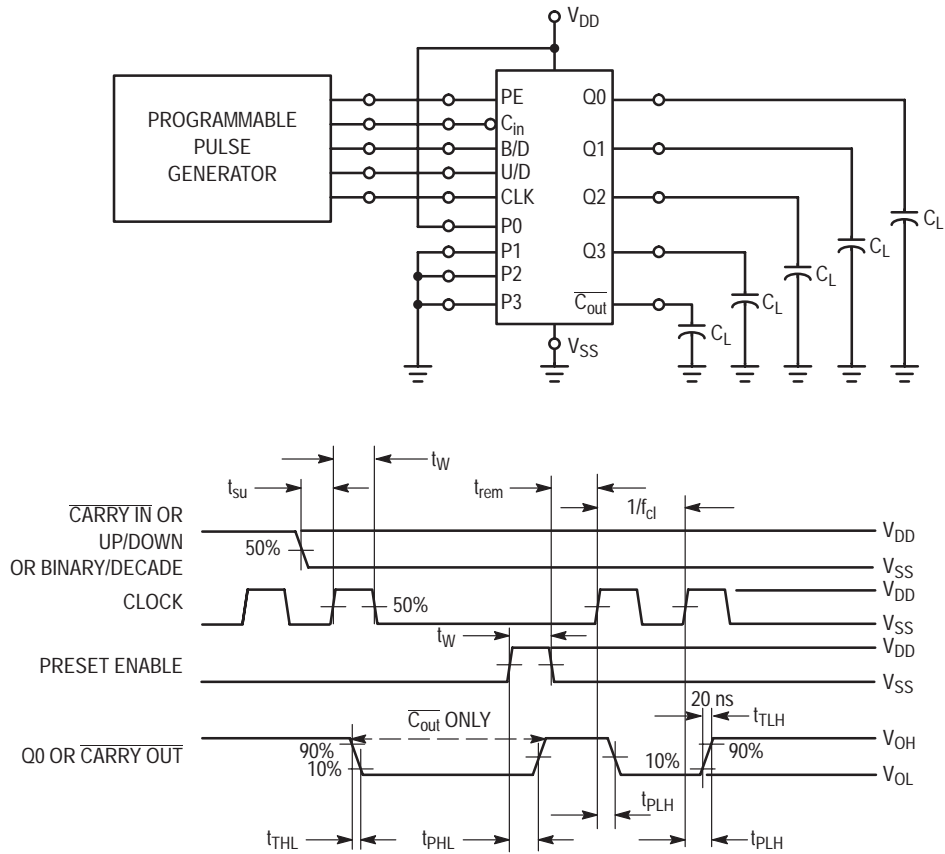
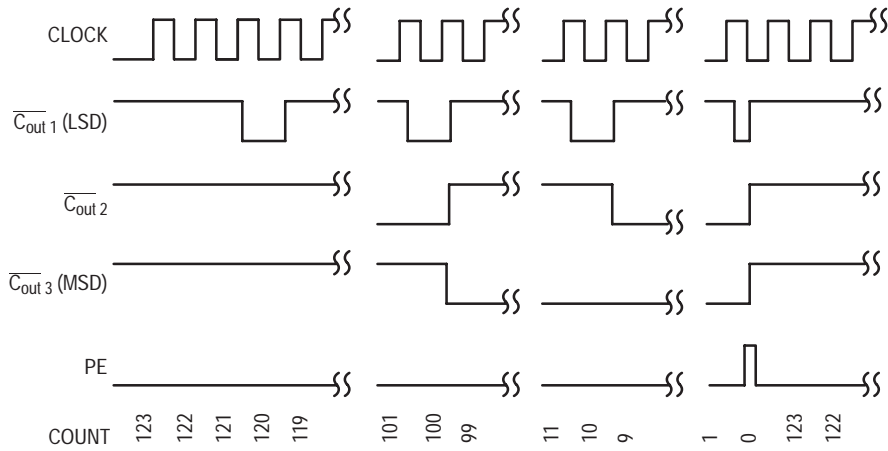
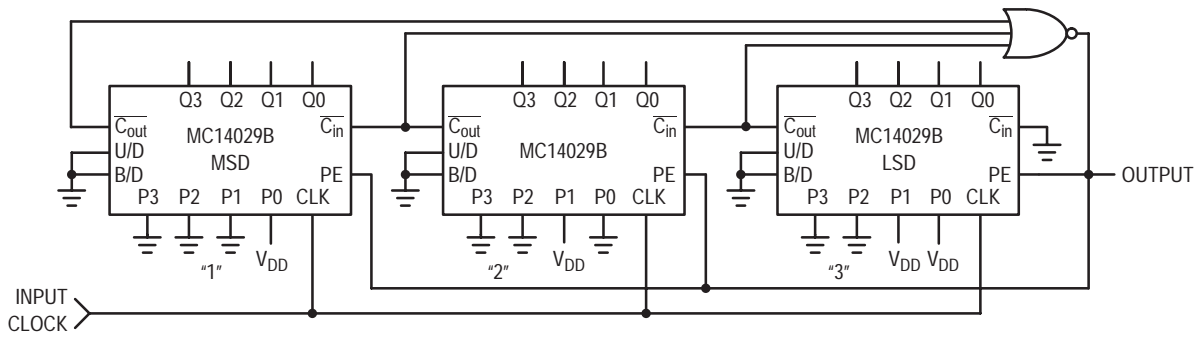
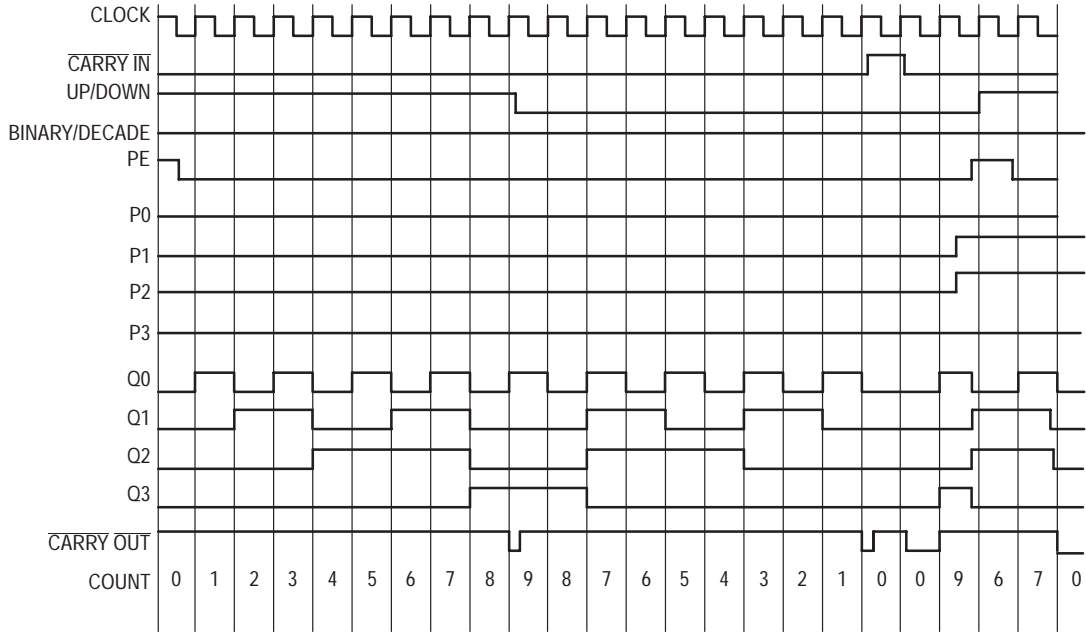


Figure 2. Switching Time Test Circuit and Waveforms

# MC14029B

## TIMING DIAGRAM

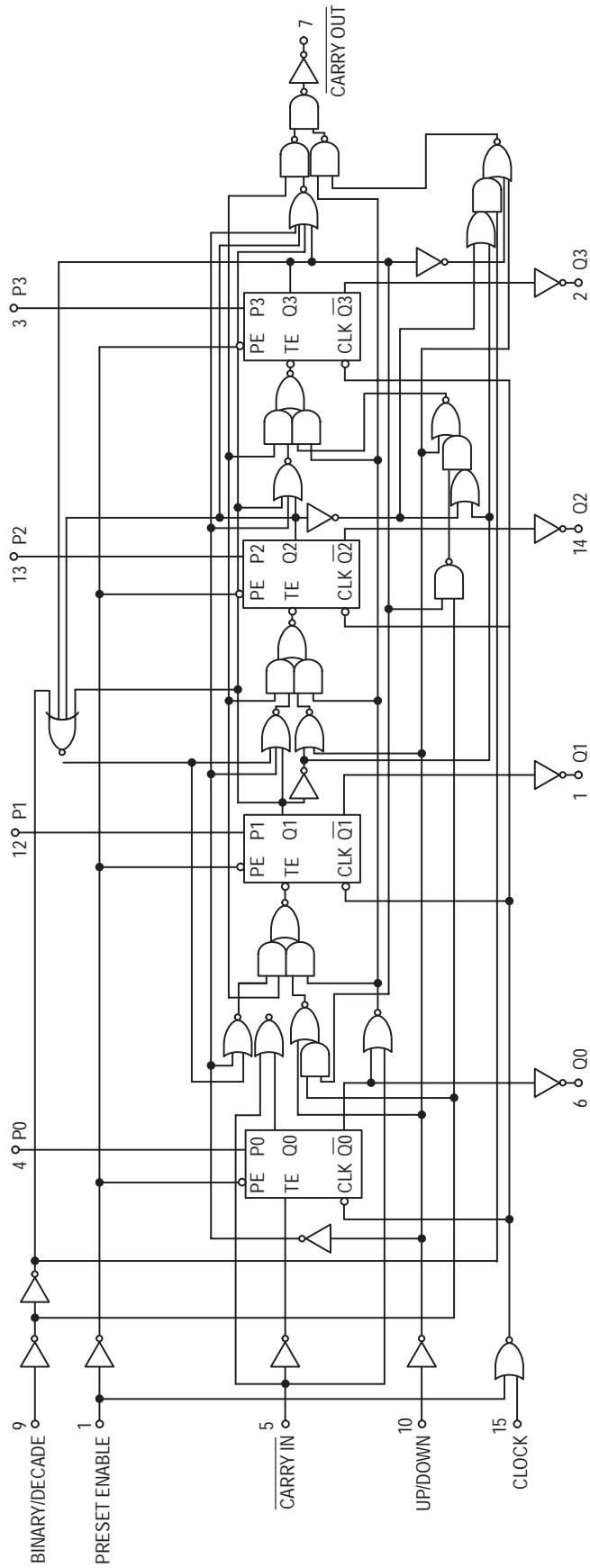


\* $t_W \cong 900 \text{ ns} @ V_{DD} = 5 \text{ V}$

Figure 3. Divide by N BCD Down Counter and Timing Diagram (Shown for N = 123)

# MC14029B

## LOGIC DIAGRAM



# MC14040B

## 12-Bit Binary Counter

The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

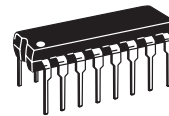
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



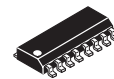
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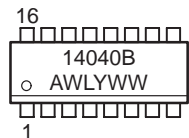
### MARKING DIAGRAMS



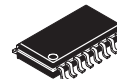
PDIP-16  
P SUFFIX  
CASE 648



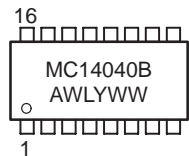
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

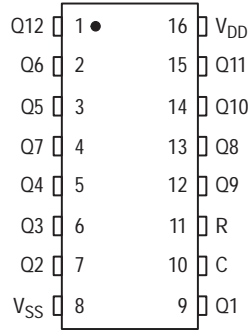
### ORDERING INFORMATION

Device	Package	Shipping
MC14040BCP	PDIP-16	2000/Box
MC14040BD	SOIC-16	2400/Box
MC14040BDR2	SOIC-16	2500/Tape & Reel
MC14040BDT	TSSOP-16	96/Rail
MC14040BF	SOEIAJ-16	See Note 1.
MC14040BFEL	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14040B

## PIN ASSIGNMENT

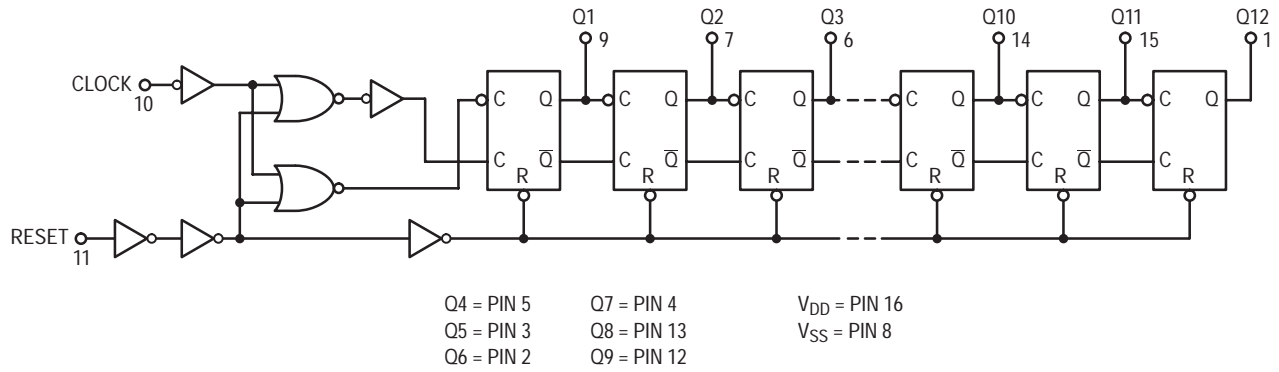


## TRUTH TABLE

Clock	Reset	Output State
	0	No Change
	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

## LOGIC DIAGRAM





# MC14040B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage  $(V_O = 4.5$ or $0.5$ Vdc) $(V_O = 9.0$ or $1.0$ Vdc) $(V_O = 13.5$ or $1.5$ Vdc)  $(V_O = 0.5$ or $4.5$ Vdc) $(V_O = 1.0$ or $9.0$ Vdc) $(V_O = 1.5$ or $13.5$ Vdc)	"0" Level  $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level  $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current  Source $(V_{OH} = 2.5$ Vdc) $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc)  Sink $(V_{OL} = 0.4$ Vdc) $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc)	$I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance $(V_{in} = 0)$	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	$\mu$ Adc
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (0.42 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (0.85 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.43 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

# MC14040B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $T_{TLH}$ , $T_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $T_{TLH}$ , $T_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $T_{TLH}$ , $T_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$ Clock to Q12 $t_{PHL}$ , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 2415 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 867 \text{ ns}$ $t_{PHL}$ , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 475 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	260 115 80	520 230 160	ns
Propagation Delay Time Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 485 \text{ ns}$ $t_{PHL} = (0.86 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	385 150 115	140 55 38	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			ns
Reset Pulse Width	$t_{WH}$	5.0 10 15	960 360 270	320 120 80	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	130 50 30	65 25 15	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

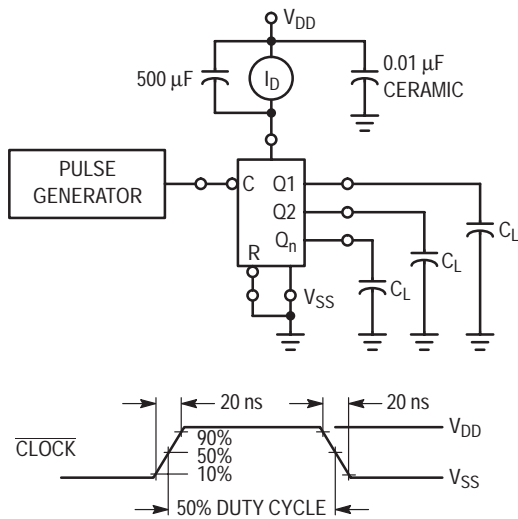


Figure 1. Power Dissipation Test Circuit and Waveform

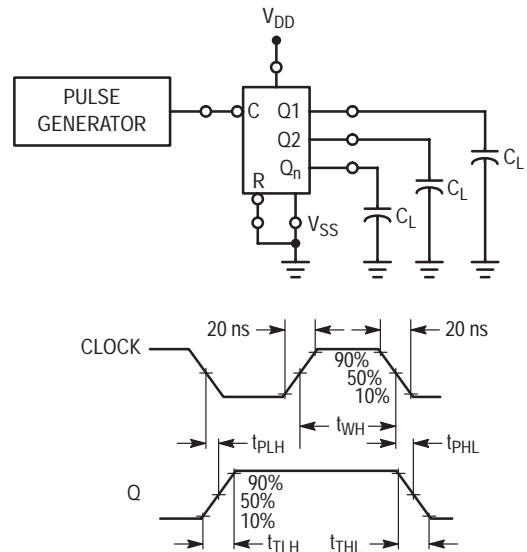


Figure 2. Switching Time Test Circuit and Waveforms

# MC14040B

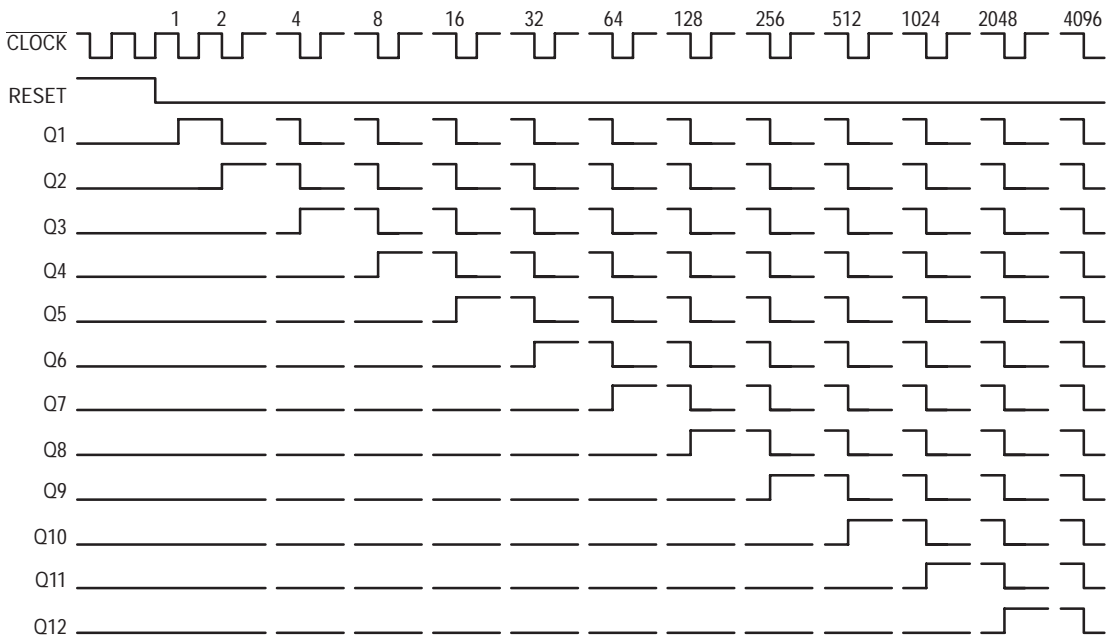


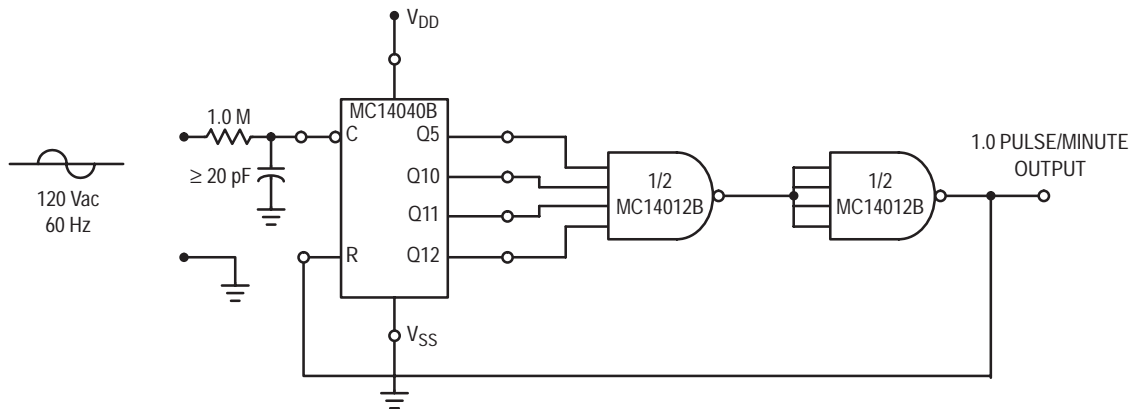
Figure 3. Timing Diagram

## APPLICATIONS INFORMATION

### TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting

outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



# MC14042B

## Quad Transparent Latch

The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and  $\bar{Q}$  during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and  $\bar{Q}$  Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

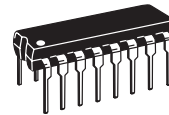
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



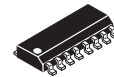
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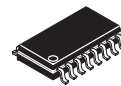
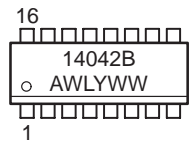
### MARKING DIAGRAMS



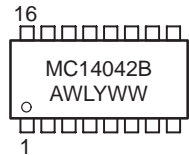
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

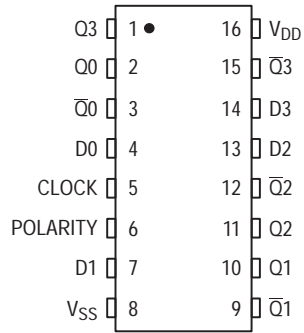
### ORDERING INFORMATION

Device	Package	Shipping
MC14042BCP	PDIP-16	2000/Box
MC14042BD	SOIC-16	2400/Box
MC14042BDR2	SOIC-16	2500/Tape & Reel
MC14042BF	SOEIAJ-16	See Note 1.
MC14042BFEL	SOEIAJ-16	See Note 1.
MC14042BFR1	SOEIAJ-16	See Note 1.
MC14042BFR2	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14042B

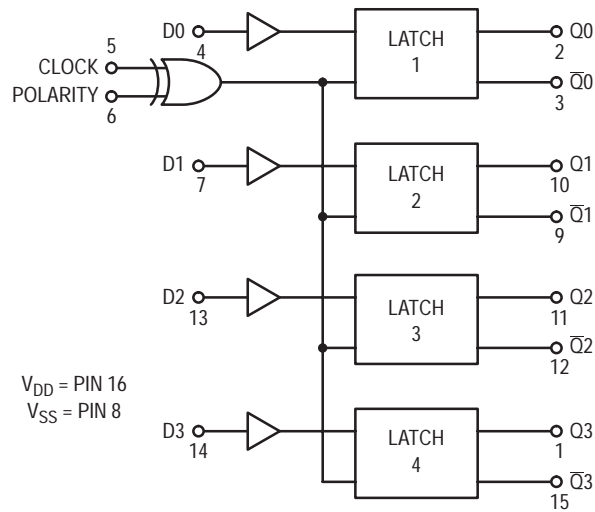
## PIN ASSIGNMENT



## TRUTH TABLE

Clock	Polarity	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

## LOGIC DIAGRAM



# MC14042B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.0 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (2.0 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (3.0 μA/kHz) f + I <sub>DD</sub>							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14042B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, D to Q, $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	220 90 60	440 180 120	ns
Propagation Delay Time, Clock to Q, $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	220 90 60	440 180 120	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	300 100 80	150 50 40	— — —	ns
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Hold Time	$t_h$	5.0 10 15	100 50 40	50 25 20	— — —	ns
Setup Time	$t_{su}$	5.0 10 15	50 30 25	0 0 0	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

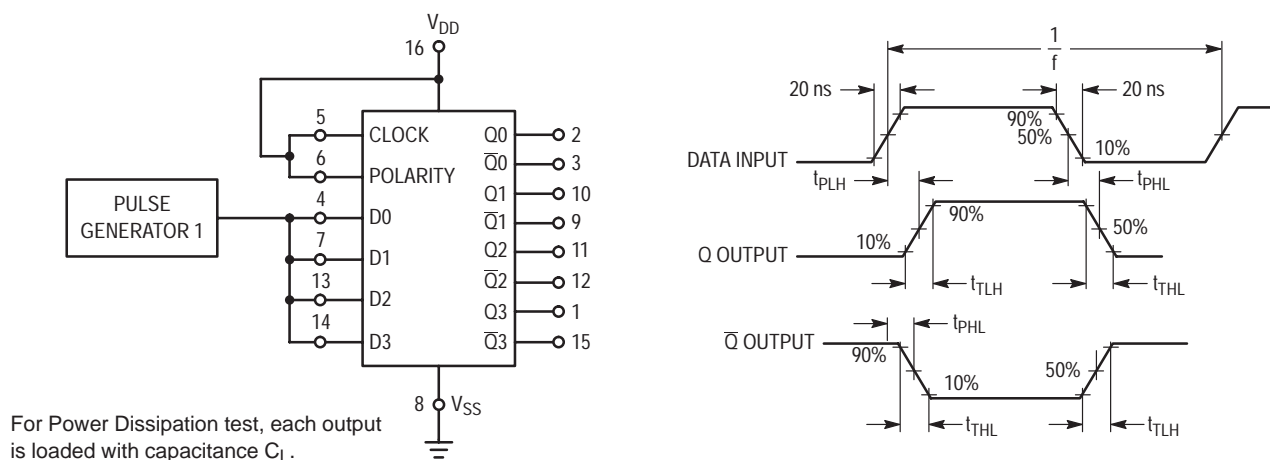
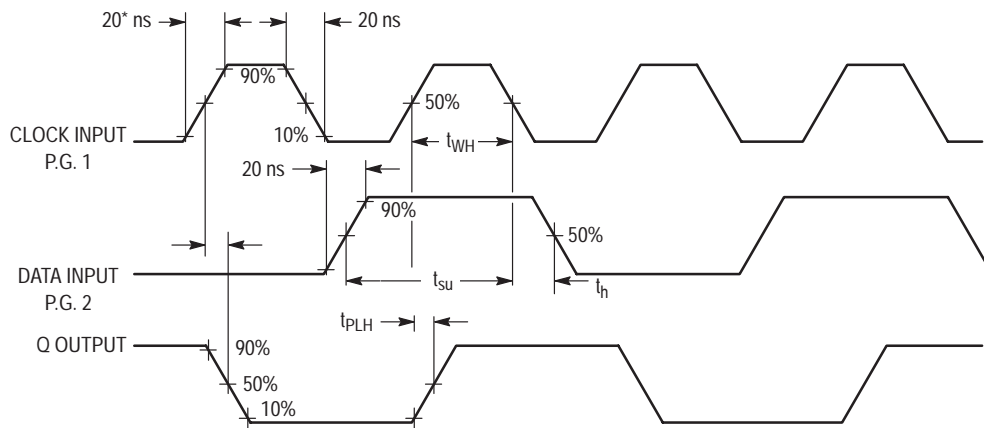
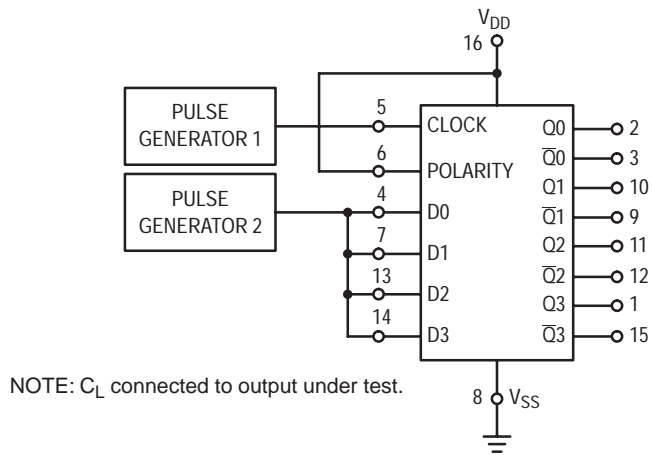


Figure 1. AC and Power Dissipation Test Circuit and Timing Diagram (Data to Output)

# MC14042B



\*Input clock rise time is 20 ns except for maximum rise time test.

**Figure 2. AC Test Circuit and Timing Diagram  
(Clock to Output)**



# MC14043B, MC14044B

## CMOS MSI

### Quad R–S Latches

The MC14043B and MC14044B quad R–S latches are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

#### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	–0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	–0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	–55 to +125	°C
$T_{stg}$	Storage Temperature Range	–65 to +150	°C
$T_L$	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

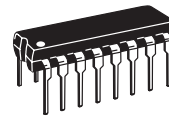
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



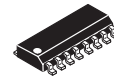
ON Semiconductor

<http://onsemi.com>

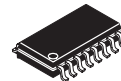
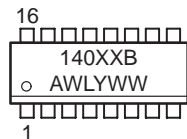
#### MARKING DIAGRAMS



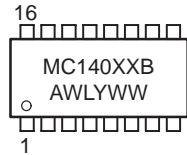
PDIP–16  
P SUFFIX  
CASE 648



SOIC–16  
D SUFFIX  
CASE 751B



SOEIAJ–16  
F SUFFIX  
CASE 966



XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

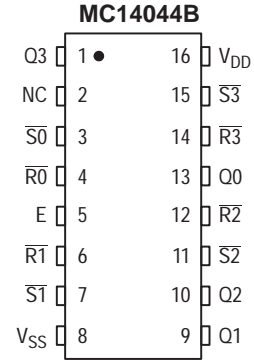
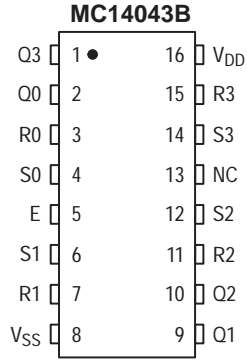
#### ORDERING INFORMATION

Device	Package	Shipping
MC14043BCP	PDIP–16	2000/Box
MC14043BD	SOIC–16	2400/Box
MC14043BDR2	SOIC–16	2500/Tape & Reel
MC14043BF	SOEIAJ–16	See Note 1.
MC14043BFEL	SOEIAJ–16	See Note 1.
MC14044BCP	PDIP–16	2000/Box
MC14044BD	SOIC–16	2400/Box
MC14044BDR2	SOIC–16	2500/Tape & Reel

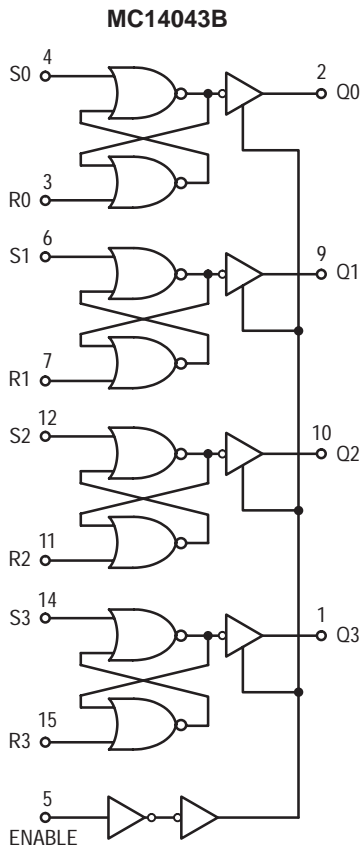
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14043B, MC14044B

## PIN ASSIGNMENT



NC = NO CONNECTION

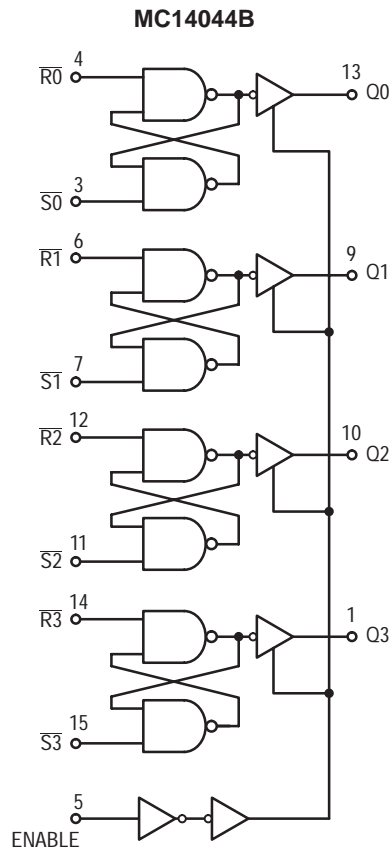


V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8  
NC = PIN 13

### TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8  
NC = PIN 2

### TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

# MC14043B, MC14044B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.58 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (1.15 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (1.73 μA/kHz) f + I <sub>DD</sub>							
Three-State Output Leakage Current	I <sub>TL</sub>	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14043B, MC14044B

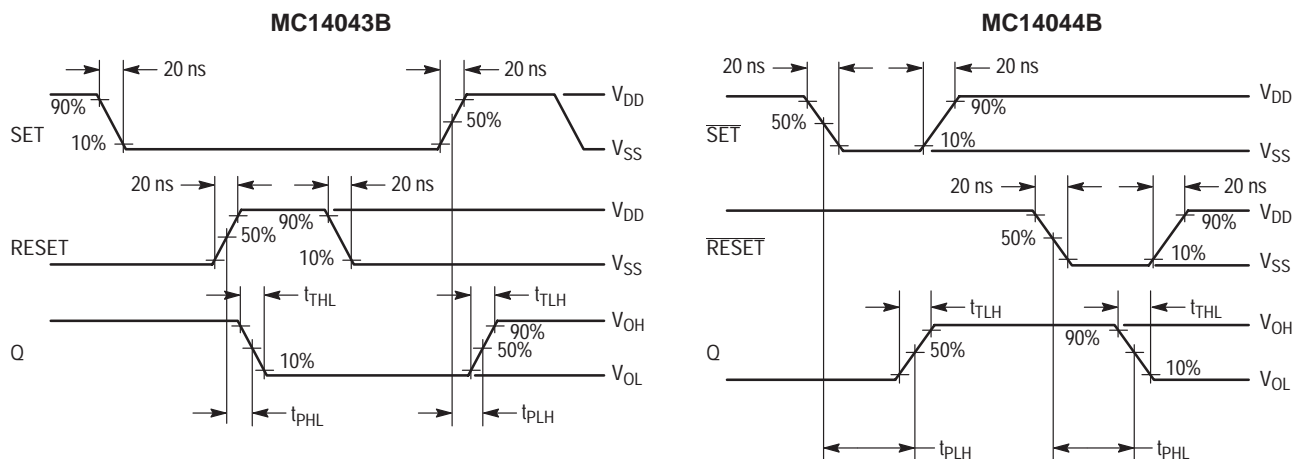
## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	$t_{PLH}$   $t_{PHL}$	5.0 10 15 5.0 10 15	— — — — — —	175 75 60 175 75 60	350 175 120 350 175 120	ns   ns
Set, $\overline{\text{Set}}$ Pulse Width	$t_W$	5.0 10 15	200 100 70	80 40 30	— — —	ns
Reset, $\overline{\text{Reset}}$ Pulse Width	$t_W$	5.0 10 15	200 100 70	80 40 30	— — —	ns
Three-State Enable/Disable Delay	$t_{PLZ}$ , $t_{PHZ}$ , $t_{PZL}$ , $t_{PZH}$	5.0 10 15	— — —	150 80 55	300 160 110	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## AC WAVEFORMS

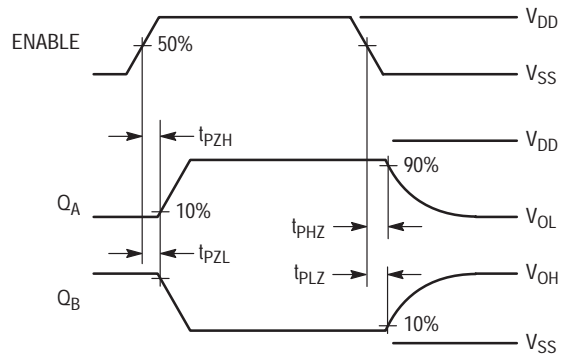
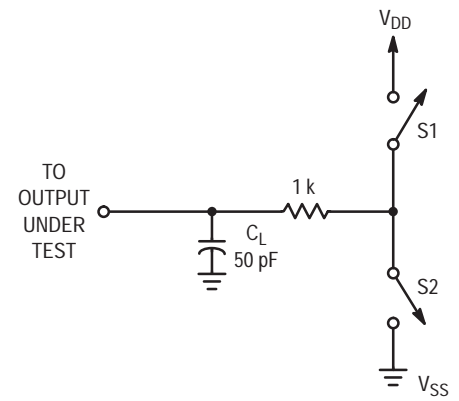


# MC14043B, MC14044B

## THREE-STATE ENABLE/DISABLE DELAYS

### Set, Reset, Enable, and Switch Conditions for 3-State Tests

Test	Enable	S1	S2	Q	MC14043B		MC14044B	
					S	R	$\bar{S}$	$\bar{R}$
$t_{PZH}$		Open	Closed	A	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{DD}$
$t_{PZL}$		Closed	Open	B	$V_{SS}$	$V_{DD}$	$V_{DD}$	$V_{SS}$
$t_{PHZ}$		Open	Closed	A	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{DD}$
$t_{PLZ}$		Closed	Open	B	$V_{SS}$	$V_{DD}$	$V_{DD}$	$V_{SS}$



# MC14046B

## Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA<sub>in</sub> and PCB<sub>in</sub>. Input PCA<sub>in</sub> can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1<sub>out</sub>, and maintains 90° phase shift at the center frequency between PCA<sub>in</sub> and PCB<sub>in</sub> signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, PC2<sub>out</sub> and LD, and maintains a 0° phase shift between PCA<sub>in</sub> and PCB<sub>in</sub> signals (duty cycle is immaterial). The linear VCO produces an output signal VCO<sub>out</sub> whose frequency is determined by the voltage of input VCO<sub>in</sub> and the capacitor and resistors connected to pins C1<sub>A</sub>, C1<sub>B</sub>, R1, and R2. The source-follower output SF<sub>out</sub> with an external resistor is used where the VCO<sub>in</sub> signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>) (Note 2.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub>	Input Voltage Range (All Inputs)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 3.)	500	mW
T <sub>A</sub>	Operating Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C



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**MARKING DIAGRAMS**

**PDIP-16**  
**P SUFFIX**  
**CASE 648**

**SOIC-16**  
**DW SUFFIX**  
**CASE 751G**

**SOEIAJ-16**  
**F SUFFIX**  
**CASE 966**

A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14046BCP	PDIP-16	2000/Box
MC14046BDW	SOIC-16	2350/Box
MC14046BDWR2	SOIC-16	1000/Tape & Reel
MC14046BF	SOEIAJ-16	See Note 1.
MC14046BFEL	SOEIAJ-16	See Note 1.

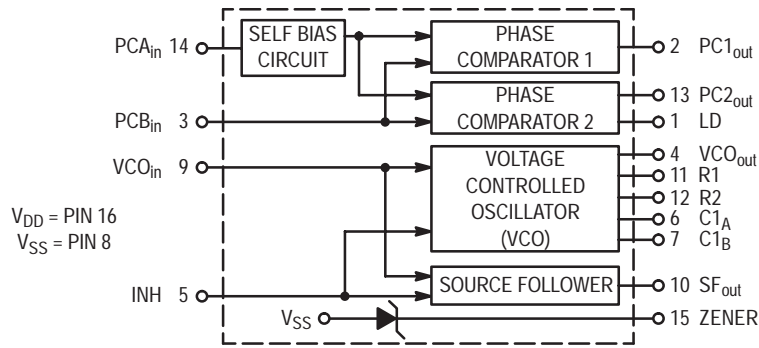
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

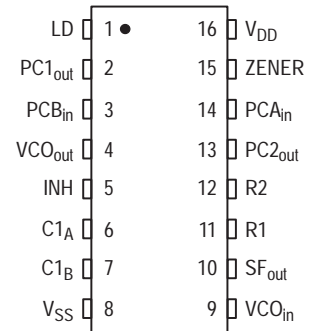
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

# MC14046B

## BLOCK DIAGRAM



## PIN ASSIGNMENT



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (4.)	"0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current	Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
			10	-0.25	—	-0.2	-0.36	—	-0.14	—	
			15	-0.62	—	-0.5	-0.9	—	-0.35	—	
			15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
			10	1.6	—	1.3	2.25	—	0.9	—	
15			4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) Inh = PCA <sub>in</sub> = V <sub>DD</sub> , Zener = VCO <sub>in</sub> = 0 V, PCB <sub>in</sub> = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (Inh = "0", f <sub>o</sub> = 10 kHz, C <sub>L</sub> = 50 pF, R1 = 1.0 MΩ, R2 = ∞, R <sub>SF</sub> = ∞, and 50% Duty Cycle)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.46 μA/kHz) f + I <sub>DD</sub>							mAdc	
		10	I <sub>T</sub> = (2.91 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (4.37 μA/kHz) f + I <sub>DD</sub>								

4. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc  
2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc  
2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

5. To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left( \frac{V_{CO_{in}} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2} \right)^{3/4} + 1.6 \times \left( \frac{V_{CO_{in}} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left( \frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu\text{A}, C_L \text{ in pF, } V_{CO_{in}}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and } R1, R2, R_{SF} \text{ in M}\Omega, C_L \text{ on VCO}_{out}$$

# MC14046B

## ELECTRICAL CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	350 150 110	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 37	175 75 55	ns

### PHASE COMPARATORS 1 and 2

Input Resistance — $PCA_{in}$	$R_{in}$	5.0 10 15	1.0 0.2 0.1	2.0 0.4 0.2	— — —	$M\Omega$
— $PCB_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$
Minimum Input Sensitivity AC Coupled — $PCA_{in}$ C series = 1000 pF, f = 50 kHz	$V_{in}$	5.0 10 15	— — —	200 400 700	300 600 1050	mV p-p
DC Coupled — $PCA_{in}$ , $PCB_{in}$	—	5 to 15	See Noise Immunity			

### VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency ( $VCO_{in} = V_{DD}$ , $C1 = 50 \text{ pF}$ $R1 = 5.0 \text{ k}\Omega$ , and $R2 = \infty$ )	$f_{max}$	5.0 10 15	0.5 1.0 1.4	0.7 1.4 1.9	— — —	MHz
Temperature — Frequency Stability ( $R2 = \infty$ )	—	5.0 10 15	— — —	0.12 0.04 0.015	— — —	%/°C
Linearity ( $R2 = \infty$ ) ( $VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $R1 > 10 \text{ k}\Omega$ ) ( $VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $R1 > 400 \text{ k}\Omega$ ) ( $VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $R1 \geq 1000 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.0 1.0 1.0	— — —	%
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — $VCO_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$

### SOURCE-FOLLOWER

Offset Voltage ( $VCO_{in}$ minus $SF_{out}$ , $RSF > 500 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.65 1.65 1.65	2.2 2.2 2.2	V
Linearity ( $VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ ) ( $VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ ) ( $VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $RSF > 50 \text{ k}\Omega$ )	—	5.0 10 15	— — —	0.1 0.6 0.8	— — —	%

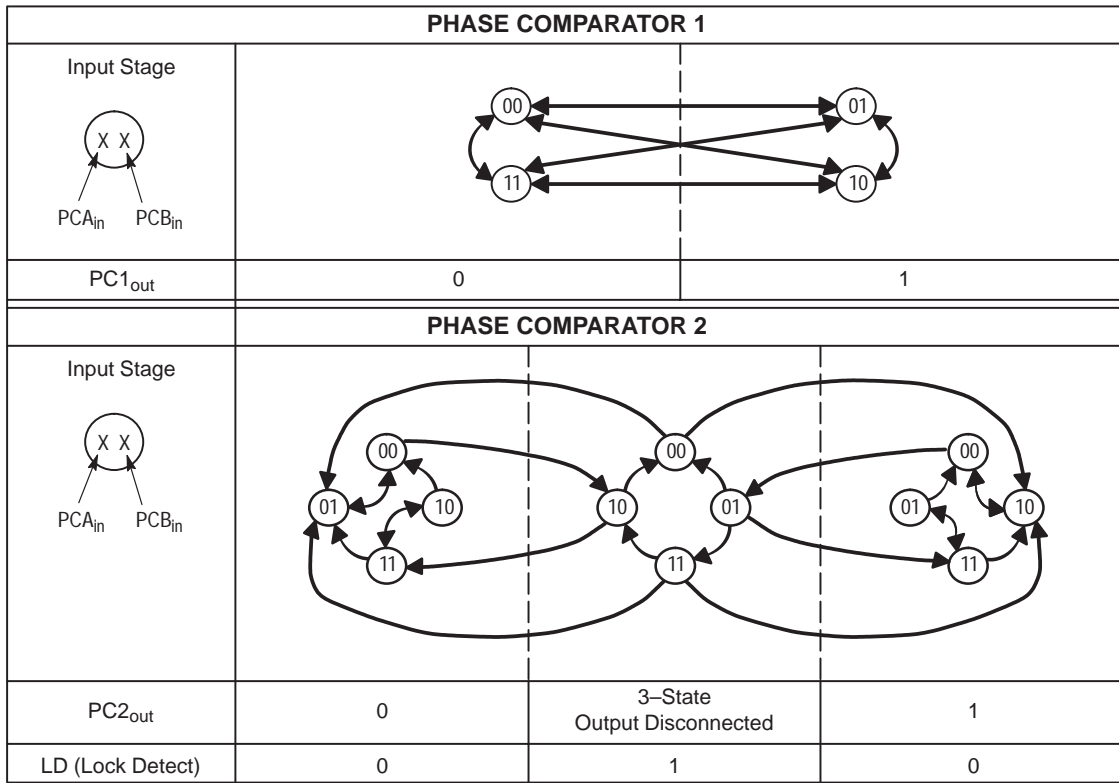
### ZENER DIODE

Zener Voltage ( $I_z = 50 \mu\text{A}$ )	$V_Z$	—	6.7	7.0	7.3	V
Dynamic Resistance ( $I_z = 1.0 \text{ mA}$ )	$R_Z$	—	—	100	—	$\Omega$

6. The formula given is for the typical characteristics only.



# MC14046B



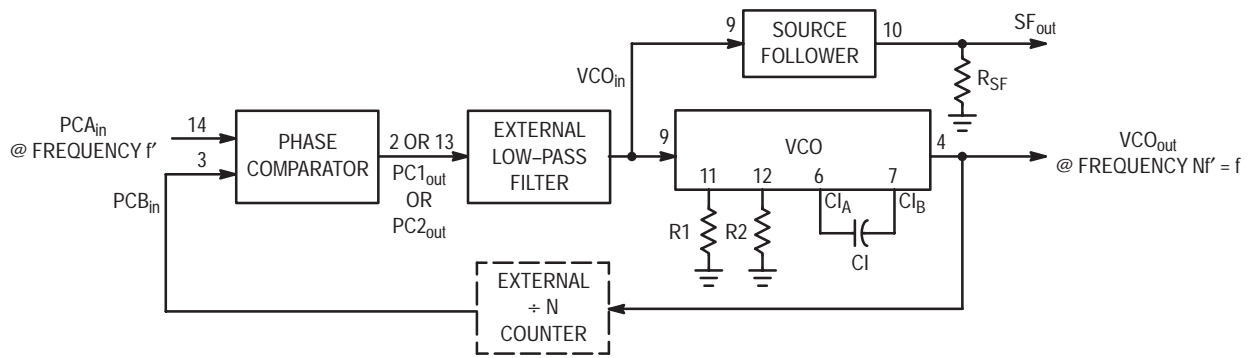
Refer to Waveforms in Figure 3.

**Figure 1. Phase Comparators State Diagrams**

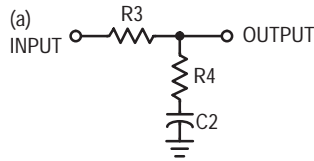
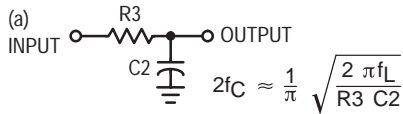
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA <sub>in</sub> .	VCO in PLL system adjusts to center frequency (f <sub>0</sub> ).	VCO in PLL system adjusts to minimum frequency (f <sub>min</sub> ).
Phase angle between PCA <sub>in</sub> and PCB <sub>in</sub> .	90° at center frequency (f <sub>0</sub> ), approaching 0° and 180° at ends of lock range (2f <sub>L</sub> )	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f <sub>L</sub> ).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2f <sub>L</sub> = full VCO frequency range = f <sub>max</sub> - f <sub>min</sub> .	
Capture frequency range (2f <sub>C</sub> ).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f <sub>C</sub> ≤ f <sub>L</sub>	f <sub>C</sub> = f <sub>L</sub>
Center frequency (f <sub>0</sub> ).	The frequency of VCO <sub>out</sub> , when VCO <sub>in</sub> = 1/2 V <sub>DD</sub>	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (V_{CO} \text{ input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (V_{CO} \text{ input} = V_{DD})$ <p>Where: 10K ≤ R<sub>1</sub> ≤ 1 M                      10K ≤ R<sub>2</sub> ≤ 1 M                      100pF ≤ C<sub>1</sub> ≤ .01 μF</p>	
Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.		

**Figure 2. Design Information**

# MC14046B



## Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} - \frac{N}{2\pi \Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} - R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

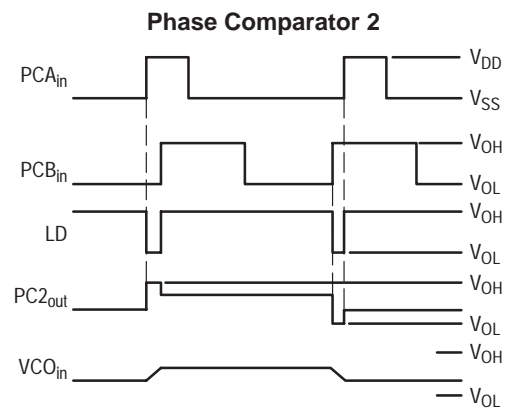
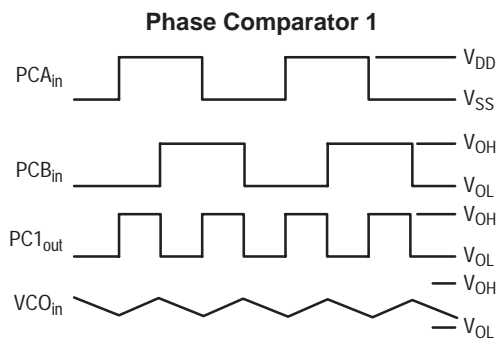
NOTE: Sometimes R3 is split into two series resistors each  $R_3 \div 2$ . A capacitor  $C_C$  is then placed from the midpoint to ground. The value for  $C_C$  should be such that the corner frequency of this network does not significantly affect  $\omega_n$ . In Figure B, the ratio of R3 to R4 sets the damping,  $R_4 \approx (0.1)(R_3)$  for optimum results.

## LOW-PASS FILTER

Definitions:  $N$  = Total division ratio in feedback loop  
 $K\phi = V_{DD}/\pi$  for Phase Comparator 1  
 $K\phi = V_{DD}/4\pi$  for Phase Comparator 2  
 $KVCO = \frac{2\pi \Delta f_{VCO}}{V_{DD} - 2V}$   
 for a typical design  $\omega_n \approx \frac{2\pi f_r}{10}$  (at phase detector input)  
 $\zeta \approx 0.707$

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi KVCO}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K\phi KVCO}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi KVCO}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K\phi KVCO})$
$F(s) = \frac{1}{R_3 C_2 S + 1}$	$F(s) = \frac{R_3 C_2 S + 1}{S(R_3 C_2 + R_4 C_2) + 1}$

## Waveforms



Note: for further information, see:

- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przedpelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

Figure 3. General Phase-Locked Loop Connections and Waveforms

# MC14049B, MC14050B

## Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage,  $V_{DD}$ .

The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS-to-TTL/DTL converter ( $V_{DD} = 5.0\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ ,  $I_{OL} \geq 3.2\text{ mA}$ ).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- $V_{IN}$  can exceed  $V_{DD}$
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	$\pm 45$	mA
$P_D$	Power Dissipation, per Package (Note 3.) (Plastic) (SOIC)	825 740	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: See Figure 3.

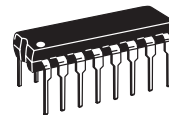
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18\text{ V}$  and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



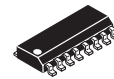
ON Semiconductor

<http://onsemi.com>

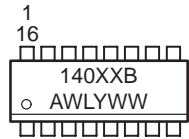


PDIP-16  
P SUFFIX  
CASE 648

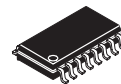
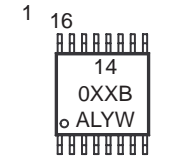
### MARKING DIAGRAMS



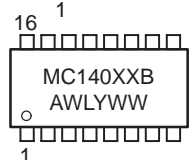
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

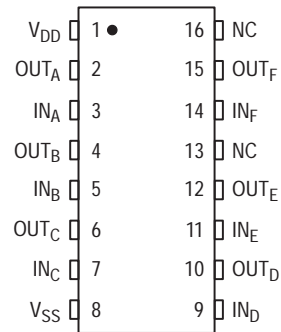
### ORDERING INFORMATION

Device	Package	Shipping
MC14049BCP	PDIP-16	2000/Box
MC14049BD	SOIC-16	2400/Box
MC14049BDR2	SOIC-16	2500/Tape & Reel
MC14049BF	SOEIAJ-16	See Note 1.
MC14050BCP	PDIP-16	2000/Box
MC14050BD	SOIC-16	2400/Box
MC14050BDR2	SOIC-16	2500/Tape & Reel
MC14050BDTEL	TSSOP-16	2000/Tape & Reel
MC14050BF	SOEIAJ-16	See Note 1.
MC14050BFEL	SOEIAJ-16	See Note 1.

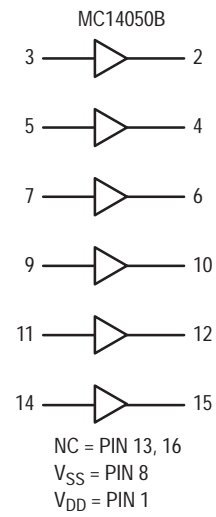
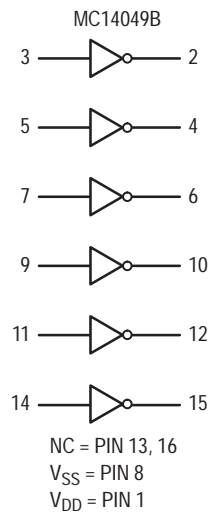
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14049B, MC14050B

## PIN ASSIGNMENT



## LOGIC DIAGRAM



# MC14049B, MC14050B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		+ 25°C			+ 125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub>  V <sub>in</sub> = 0	"0" Level  V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level  V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level  V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level  V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source  I <sub>OH</sub>	5.0	-1.6	—	-1.25	-2.5	—	-1.0	—	mAdc
		10	-1.6	—	-1.30	-2.6	—	-1.0	—	
		15	-4.7	—	-3.75	-10	—	-3.0	—	
	Sink  I <sub>OL</sub>	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
		10	10	—	8.0	16	—	6.6	—	
		15	30	—	24	40	—	19	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, per package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.5 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (5.3 μA/kHz) f + I <sub>DD</sub>							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at + 25°C

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

Where: I<sub>T</sub> is in μA (per Package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency and k = 0.002.

# MC14049B, MC14050B

## AC SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = +25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	160 80 60	ns
Output Fall Time $t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$ $t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$ $t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	80 40 30	140 80 60	ns
Propagation Delay Time $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	40 20 15	80 40 30	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

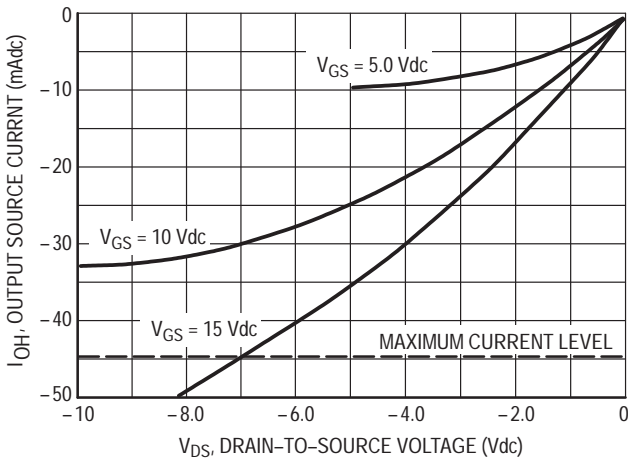
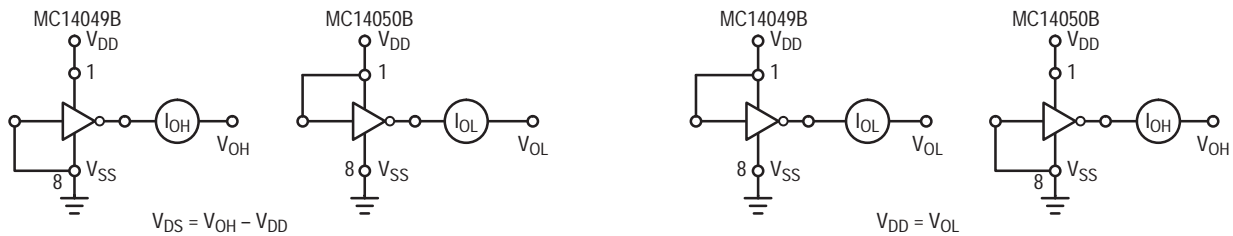


Figure 1. Typical Output Source Characteristics

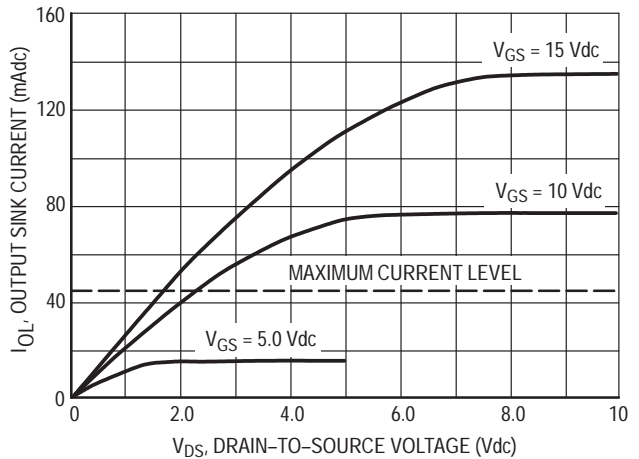


Figure 2. Typical Output Sink Characteristics

# MC14049B, MC14050B

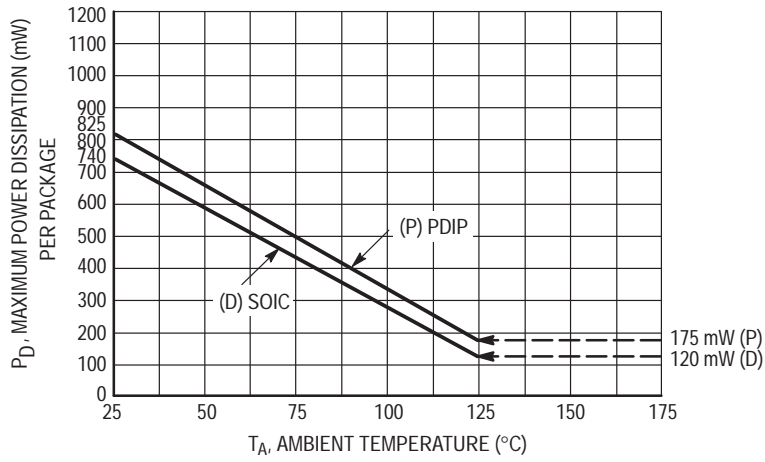


Figure 3. Ambient Temperature Power Derating

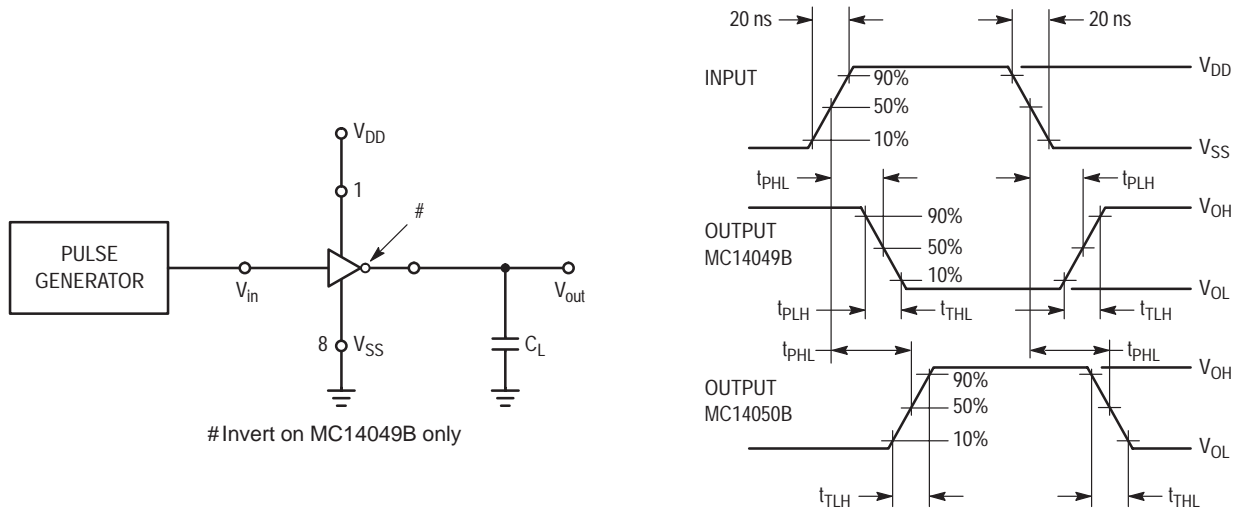


Figure 4. Switching Time Test Circuit and Waveforms

# MC14049UB

## Hex Buffers

The MC14049UB hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic-level conversion using only one supply voltage,  $V_{DD}$ . The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS-to-TTL/DTL converters ( $V_{DD} = 5.0\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ ,  $I_{OL} \geq 3.2\text{ mA}$ ). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- $V_{IN}$  can exceed  $V_{DD}$
- Improved ESD Protection on All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	+45	mA
$P_D$	Power Dissipation, per Package (Note 3.)	825 740	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
All Packages: See Figure 4.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18\text{ V}$  and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

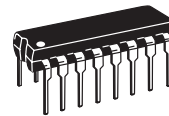
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



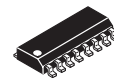
ON Semiconductor

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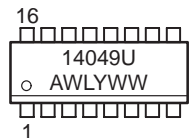
### MARKING DIAGRAMS



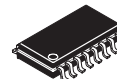
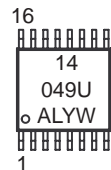
PDIP-16  
P SUFFIX  
CASE 648



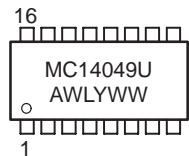
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

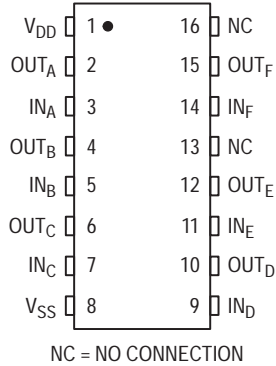
Device	Package	Shipping
MC14049UBCP	PDIP-16	2000/Box
MC14049UBD	SOIC-16	2400/Box
MC14049UBDR2	SOIC-16	2500/Tape & Reel
MC14049UBDT	TSSOP-16	96/Rail
MC14049UBDTR2	TSSOP-16	2500/Tape & Reel
MC14049UBF	SOEIAJ-16	See Note 1.
MC14049UBFEL	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

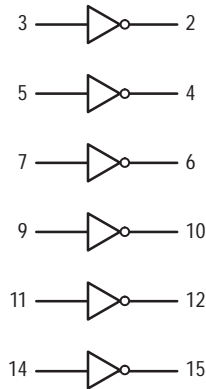


# MC14049UB

## PIN ASSIGNMENT

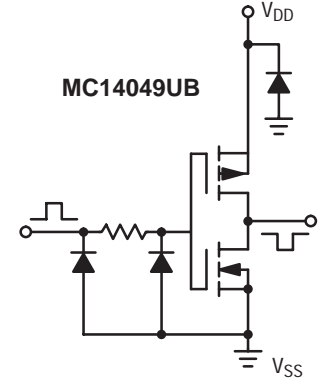


## LOGIC DIAGRAM MC14049UB



NC = PIN 13, 16  
V<sub>SS</sub> = PIN 8  
V<sub>DD</sub> = PIN 1

## CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
(V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.6	—	-1.25	-2.5	—	-1.0	—	mAdc
		10	-1.6	—	-1.3	-2.6	—	-1.0	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink I <sub>OL</sub>	5.0	3.75	—	3.2	6.0	—	2.6	—	mAdc
		10	10	—	8.0	16	—	6.6	—	
(V <sub>OL</sub> = 1.5 Vdc)		15	30	—	24	40	—	19	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	10	20	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current <sup>(5.)</sup> (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.5 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (5.3 μA/kHz) f + I <sub>DD</sub>							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14049UB

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (0.8 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{TLH} = (0.27 \text{ ns/pF}) C_L + 26.5 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	160 100 60	ns
Output Fall Time $t_{THL} = (0.3 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.12 \text{ ns/pF}) C_L + 14 \text{ ns}$ $t_{THL} = (0.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.38 \text{ ns/pF}) C_L + 61 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH} = (0.11 \text{ ns/pF}) C_L + 24.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	80 40 30	120 65 50	ns
Propagation Delay Time $t_{PHL} = (0.38 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PHL} = (0.12 \text{ ns/pF}) C_L + 9 \text{ ns}$ $t_{PHL} = (0.11 \text{ ns/pF}) C_L + 4.5 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	30 15 10	60 30 20	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

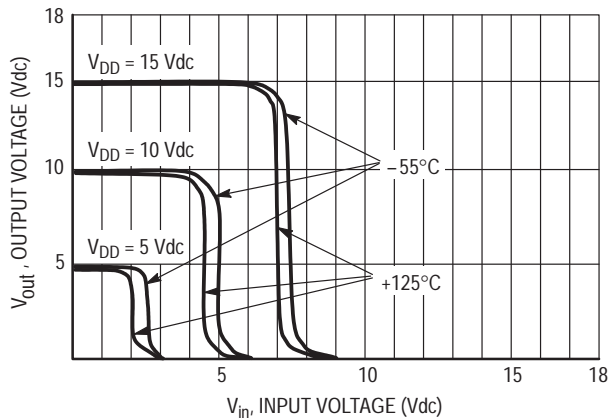


Figure 1. Typical Voltage Transfer Characteristics versus Temperature

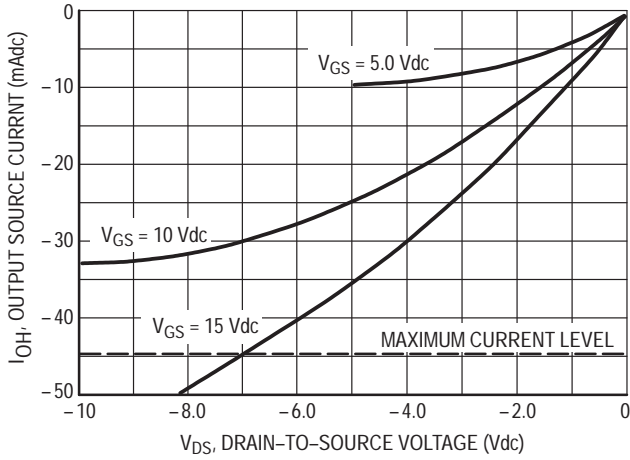
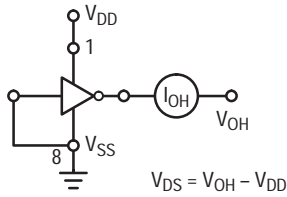


Figure 2. Typical Output Source Characteristics

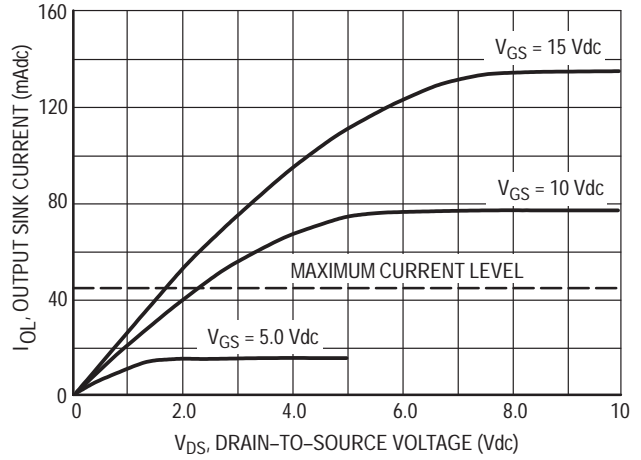
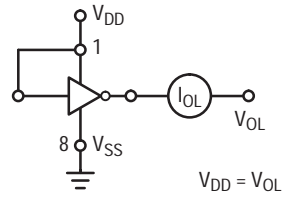


Figure 3. Typical Output Sink Characteristics

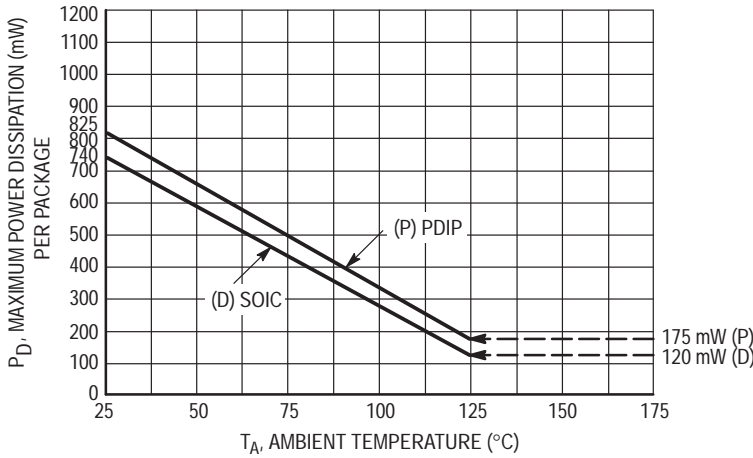


Figure 4. Ambient Temperature Power Derating

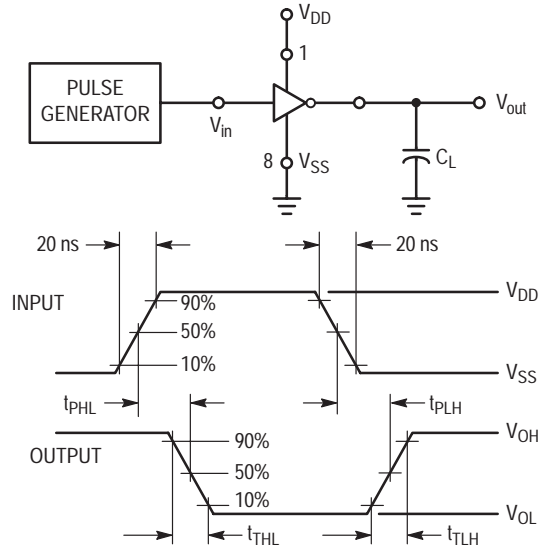


Figure 5. Switching Time Test Circuit and Waveforms

# MC14051B, MC14052B, MC14053B

## Analog Multiplexers/Demultiplexers

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 to 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-noise – 12 nV/ $\sqrt{\text{Cycle}}$ ,  $f \geq 1.0$  kHz Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower  $R_{ON}$ , Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

### MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage (Referenced to $V_{EE}$ , $V_{SS} \geq V_{EE}$ )	-0.5 to +18.0	V
$V_{in}$ , $V_{out}$	Input or Output Voltage Range (DC or Transient) (Referenced to $V_{SS}$ for Control Inputs and $V_{EE}$ for Switch I/O)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Control Pin	$\pm 10$	mA
$I_{SW}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

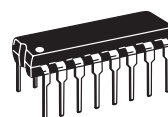
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$ ,  $V_{EE}$  or  $V_{DD}$ ). Unused outputs must be left open.



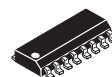
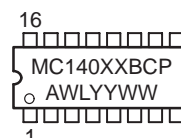
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### MARKING DIAGRAMS



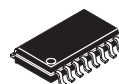
PDIP-16  
P SUFFIX  
CASE 648



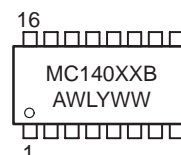
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



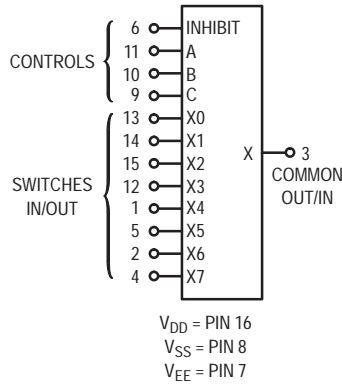
XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

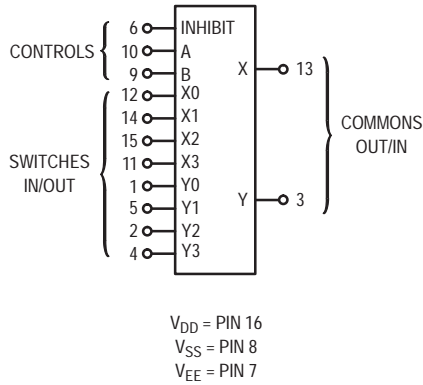
See detailed ordering and shipping information in the package dimensions section on page 163 of this data sheet.

# MC14051B, MC14052B, MC14053B

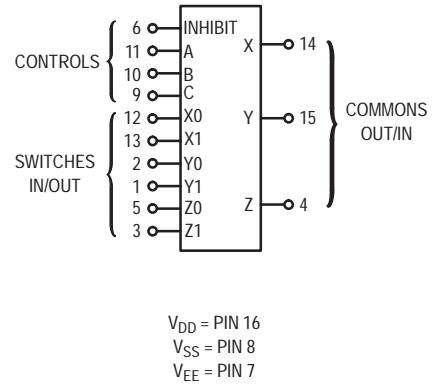
**MC14051B**  
8-Channel Analog  
Multiplexer/Demultiplexer



**MC14052B**  
Dual 4-Channel Analog  
Multiplexer/Demultiplexer

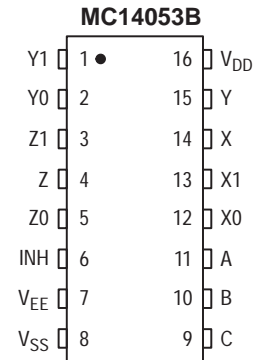
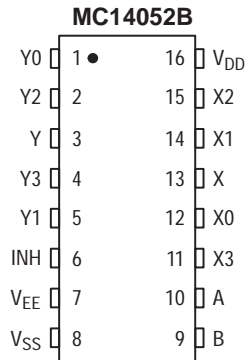
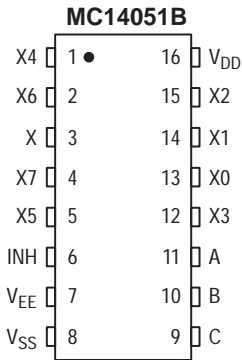


**MC14053B**  
Triple 2-Channel Analog  
Multiplexer/Demultiplexer



Note: Control Inputs referenced to  $V_{SS}$ , Analog Inputs and Outputs reference to  $V_{EE}$ .  $V_{EE}$  must be  $\leq V_{SS}$ .

## PIN ASSIGNMENT



# MC14051B, MC14052B, MC14053B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (3.)	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0	18	3.0	—	18	3.0	18	V	
Quiescent Current Per Package	I <sub>DD</sub>	5.0	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV (4.)	—	5.0	—	0.005	5.0	—	150	μA	
		10		—	10	—	0.010	10	—	300		
		15		—	20	—	0.015	20	—	600		
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical						(0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>		μA

### CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	—	1.5	—	2.25	1.5	—	1.5	V
		10		—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V <sub>IH</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5	—	3.5	2.75	—	3.5	—	V
		10		7.0	—	7.0	5.50	—	7.0	—	
		15		11	—	11	8.25	—	11	—	
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V<sub>EE</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>PP</sub>
Recommended Static or Dynamic Voltage Across the Switch (4.) (Figure 5)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0	ΔV <sub>switch</sub> ≤ 500 mV (4.) V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	—	800	—	250	1050	—	1200	Ω
		10		—	400	—	120	500	—	520	
		15		—	220	—	80	280	—	300	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (Figure 10)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Inhibit = V <sub>DD</sub>	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—	Inhibit = V <sub>DD</sub> (MC14051B) (MC14052B) (MC14053B)	—	—	—	60	—	—	—	pF
				—	—	—	32	—	—		
				—	—	—	17	—	—		
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	—	Pins Not Adjacent Pins Adjacent	—	—	—	0.15	—	—	—	pF
				—	—	—	0.47	—	—	—	

3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

4. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn, i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14051B, MC14052B, MC14053B

## ELECTRICAL CHARACTERISTICS <sup>(5)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ ) ( $V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ <sup>(6)</sup> All Types	Max	Unit		
Propagation Delay Times (Figure 6) Switch Input to Switch Output ( $R_L = 10 \text{ k}\Omega$ ) MC14051 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$ MC14052 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 21.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 7.0 \text{ ns}$ MC14053 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 16.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 4.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 3.0 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0	35	90	ns		
		10	15	40			
		15	12	30			
		5.0	30	75	ns		
		10	12	30			
		15	10	25			
		5.0	25	65	ns		
		10	8.0	20			
		15	6.0	15			
		Inhibit to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ ) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level MC14051B	$t_{PHZ}, t_{PLZ},$ $t_{PZH}, t_{PZL}$	5.0	350	700	ns
				10	170	340	
				15	140	280	
MC14052B	5.0			300	600	ns	
10	155			310			
15	125			250			
MC14053B	5.0			275	550	ns	
10	140			280			
15	110			220			
Control Input to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ ) MC14051B	$t_{PLH}, t_{PHL}$	5.0	360	720	ns		
		10	160	320			
		15	120	240			
		MC14052B	5.0	325	650	ns	
		10	130	260			
		15	90	180			
		MC14053B	5.0	300	600	ns	
		10	120	240			
		15	80	160			
Second Harmonic Distortion ( $R_L = 10 \text{ k}\Omega$ , $f = 1 \text{ kHz}$ ) $V_{in} = 5 V_{PP}$	—	10	0.07	—	%		
Bandwidth (Figure 7) ( $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $C_L = 50 \text{ pF}$ $20 \text{ Log } (V_{out}/V_{in}) = -3 \text{ dB}$ )	BW	10	17	—	MHz		
Off Channel Feedthrough Attenuation (Figure 7) $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p $f_{in} = 4.5 \text{ MHz}$ — MC14051B $f_{in} = 30 \text{ MHz}$ — MC14052B $f_{in} = 55 \text{ MHz}$ — MC14053B	—	10	-50	—	dB		
Channel Separation (Figure 8) ( $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $f_{in} = 3.0 \text{ MHz}$ )	—	10	-50	—	dB		
Crosstalk, Control Input to Common O/I (Figure 9) ( $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$ Control $t_{TLH} = t_{THL} = 20 \text{ ns}$ , Inhibit = $V_{SS}$ )	—	10	75	—	mV		

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14051B, MC14052B, MC14053B

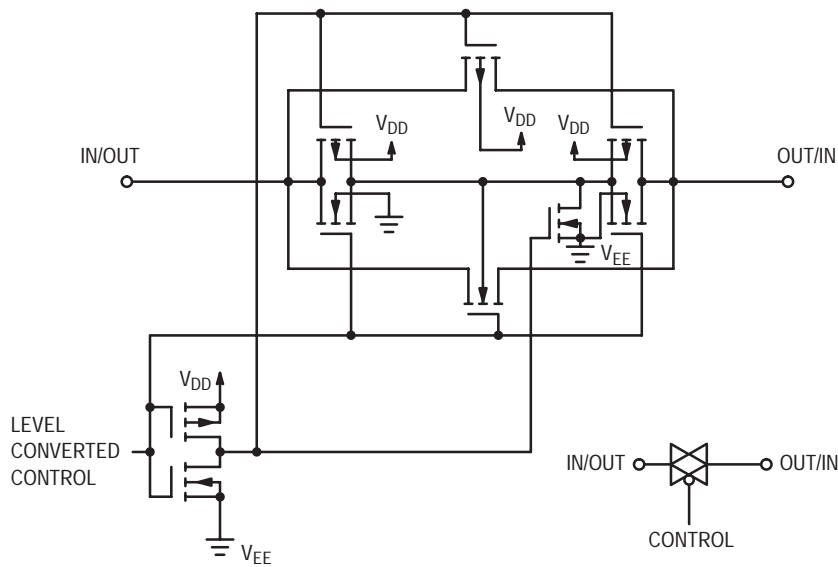


Figure 1. Switch Circuit Schematic

## TRUTH TABLE

Control Inputs			ON Switches		
Inhibit	Select		MC14051B	MC14052B	MC14053B
	C*	B A			
0	0	0 0	X0	Y0 X0	Z0 Y0 X0
0	0	0 1	X1	Y1 X1	Z0 Y0 X1
0	0	1 0	X2	Y2 X2	Z0 Y1 X0
0	0	1 1	X3	Y3 X3	Z0 Y1 X1
0	1	0 0	X4		Z1 Y0 X0
0	1	0 1	X5		Z1 Y0 X1
0	1	1 0	X6		Z1 Y1 X0
0	1	1 1	X7		Z1 Y1 X1
1	x	x x	None	None	None

\*Not applicable for MC14052  
x = Don't Care

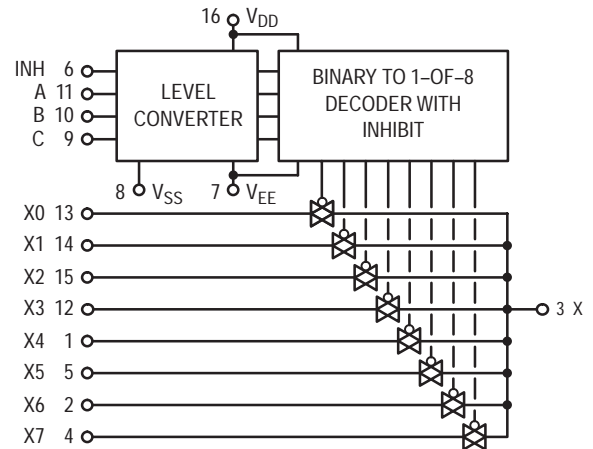


Figure 2. MC14051B Functional Diagram

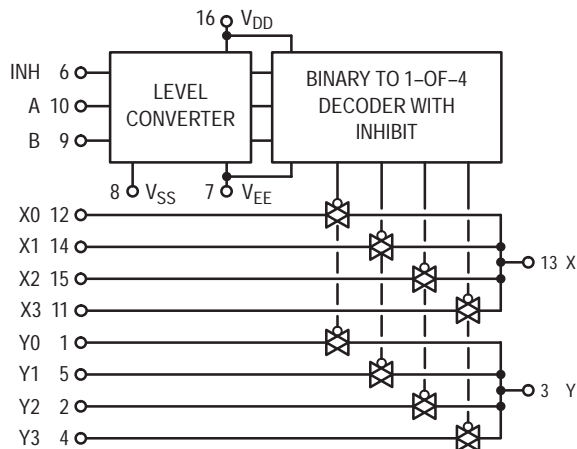


Figure 3. MC14052B Functional Diagram

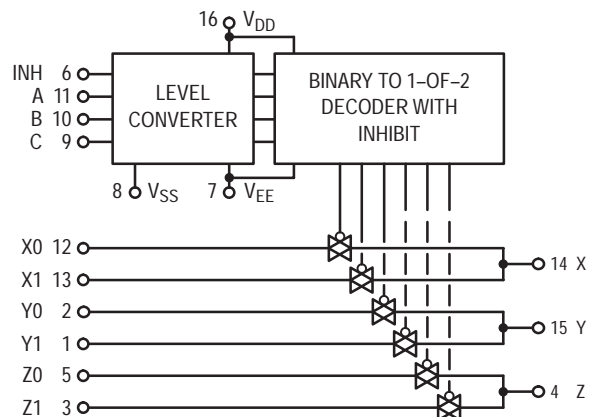


Figure 4. MC14053B Functional Diagram



TEST CIRCUITS

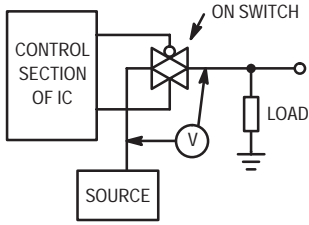


Figure 5.  $\Delta V$  Across Switch

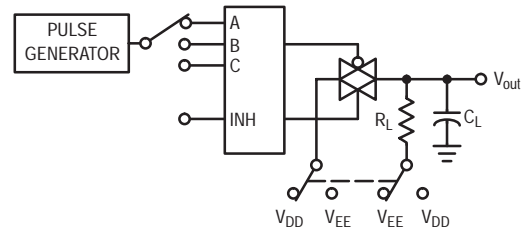


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

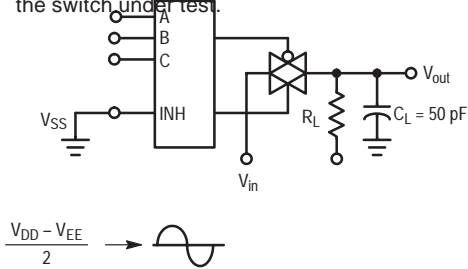


Figure 7. Bandwidth and Off-Channel Feedthrough Attenuation

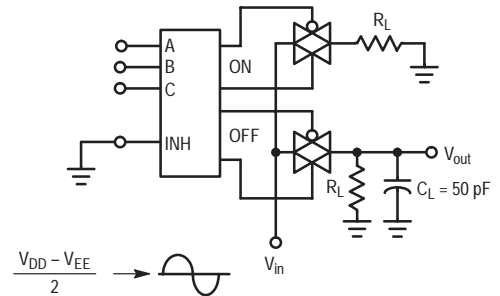


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

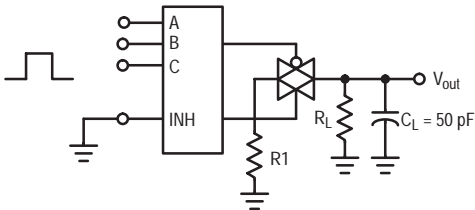


Figure 9. Crosstalk, Control Input to Common O/I

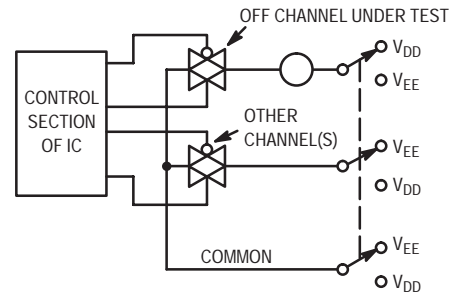


Figure 10. Off Channel Leakage

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

# MC14051B, MC14052B, MC14053B

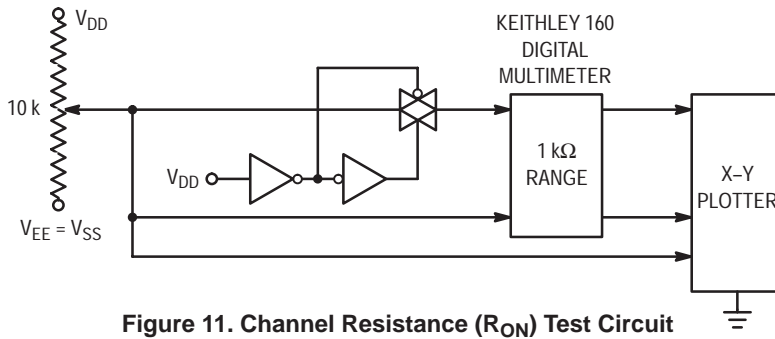


Figure 11. Channel Resistance ( $R_{ON}$ ) Test Circuit

## TYPICAL RESISTANCE CHARACTERISTICS

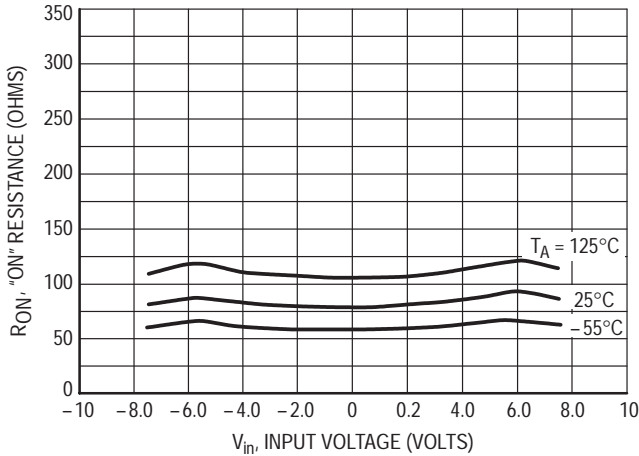


Figure 12.  $V_{DD} = 7.5\text{ V}$ ,  $V_{EE} = -7.5\text{ V}$

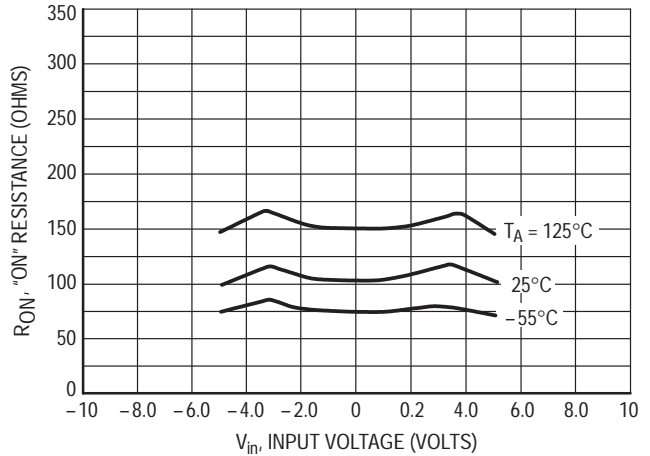


Figure 13.  $V_{DD} = 5.0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$

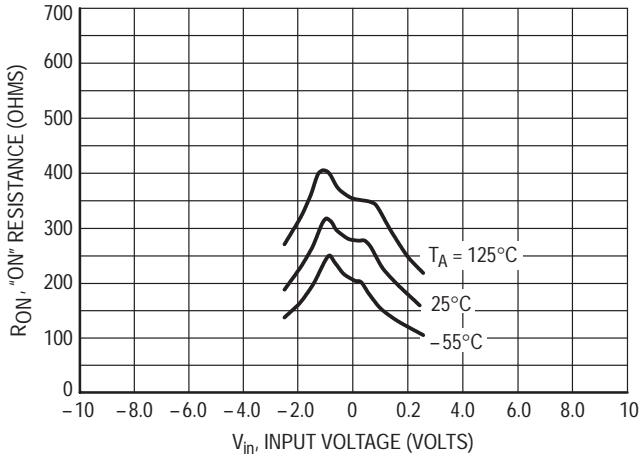


Figure 14.  $V_{DD} = 2.5\text{ V}$ ,  $V_{EE} = -2.5\text{ V}$

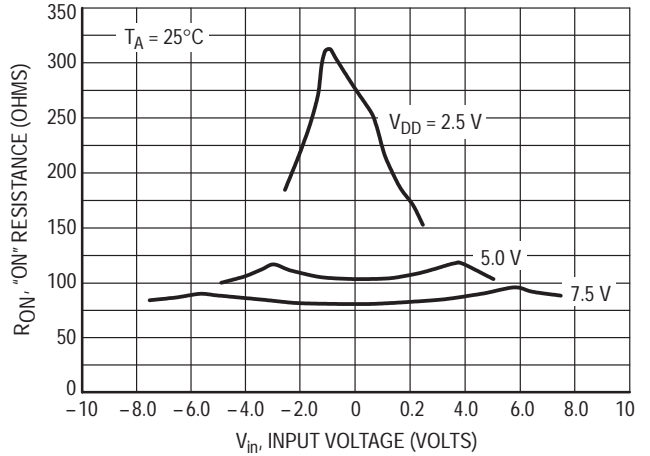


Figure 15. Comparison at  $25^\circ\text{C}$ ,  $V_{DD} = -V_{EE}$

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above V<sub>SS</sub>. The V<sub>EE</sub> voltage determines the maximum swing below V<sub>SS</sub>. For the example, V<sub>DD</sub> - V<sub>SS</sub> = 5 V maximum swing above V<sub>SS</sub>; V<sub>SS</sub> - V<sub>EE</sub> = 5 V maximum swing below V<sub>SS</sub>. The example shows a ±4.5 V signal which allows a 1/2 volt margin at each

peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to V<sub>EE</sub>. For example, V<sub>DD</sub> = +10 V, V<sub>SS</sub> = +5 V, and V<sub>EE</sub> = -3 V is acceptable. See the Table below.

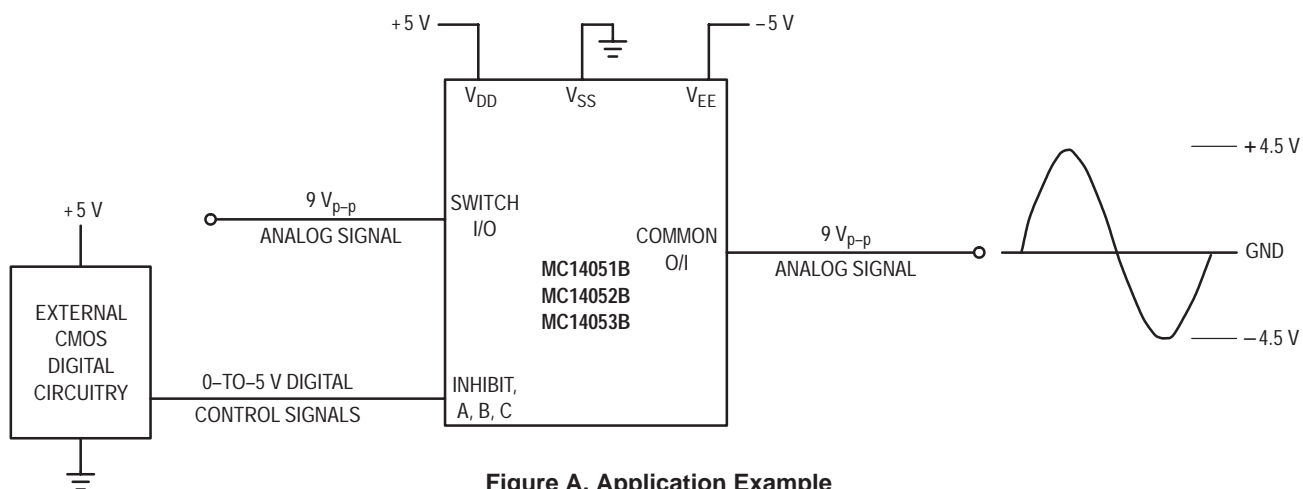


Figure A. Application Example

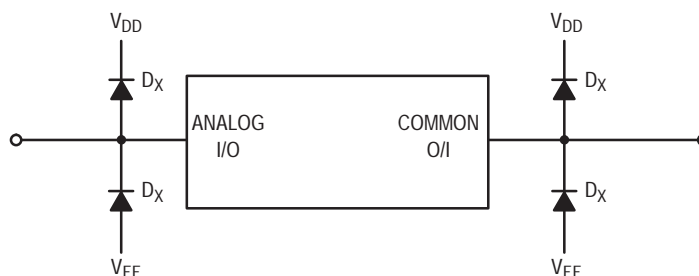


Figure B. External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	- 8	+ 8/0	+ 8 to - 8 = 16 V <sub>p-p</sub>
+ 5	0	- 12	+ 5/0	+ 5 to - 12 = 17 V <sub>p-p</sub>
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V <sub>p-p</sub>
+ 5	0	- 5	+ 5/0	+ 5 to - 5 = 10 V <sub>p-p</sub>
+ 10	+ 5	- 5	+ 10/+ 5	+ 10 to - 5 = 15 V <sub>p-p</sub>

## MC14051B, MC14052B, MC14053B

### ORDERING & SHIPPING INFORMATION:

Device	Package	Shipping
MC14051BCP	PDIP-16	2000 Units per Box
MC14051BD	SOIC-16	48 Units per Rail
MC14051BDR2	SOIC-16	2500 Units / Tape & Reel
MC14051BDT	TSSOP-16	96 Units per Rail
MC14051BDTEL	TSSOP-16	2000 Units / Tape & Reel
MC14051BDTR2	TSSOP-16	2500 Units / Tape & Reel
MC14051BF	SOEIAJ-16	See Note 7.
MC14051BFEL	SOEIAJ-16	See Note 7.
MC14052BCP	PDIP-16	2000 Units per Box
MC14052BD	SOIC-16	48 Units per Rail
MC14052BDR2	SOIC-16	2500 Units / Tape & Reel
MC14052BDT	TSSOP-16	96 Units per Rail
MC14052BDTR2	TSSOP-16	2500 Units / Tape & Reel
MC14052BF	SOEIAJ-16	See Note 7.
MC14052BFEL	SOEIAJ-16	See Note 7.

### ORDERING & SHIPPING INFORMATION:

MC14053BCP	PDIP-16	2000 Units per Box
MC14053BD	SOIC-16	48 Units per Rail
MC14053BDR2	SOIC-16	2500 Units / Tape & Reel
MC14053BDT	TSSOP-16	96 Units per Rail
MC14053BDTEL	TSSOP-16	2000 Units / Tape & Reel
MC14053BDTR2	TSSOP-16	2500 Units / Tape & Reel
MC14053BF	SOEIAJ-16	See Note 7.
MC14053BFEL	SOEIAJ-16	See Note 7.

7. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14060B

## 14-Bit Binary Counter and Oscillator

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4060B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

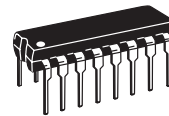
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



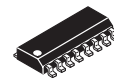
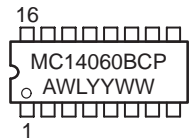
ON Semiconductor

<http://onsemi.com>

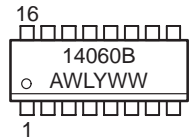
### MARKING DIAGRAMS



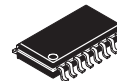
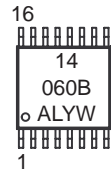
PDIP-16  
P SUFFIX  
CASE 648



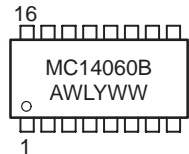
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14060BCP	PDIP-16	2000/Box
MC14060BD	SOIC-16	2400/Box
MC14060BDR2	SOIC-16	2500/Tape & Reel
MC14060BDT	TSSOP-16	96/Rail
MC14060BDTR2	TSSOP-16	2500/Tape & Reel
MC14060BF	SOEIAJ-16	See Note 1.
MC14060BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14060B

## PIN ASSIGNMENT

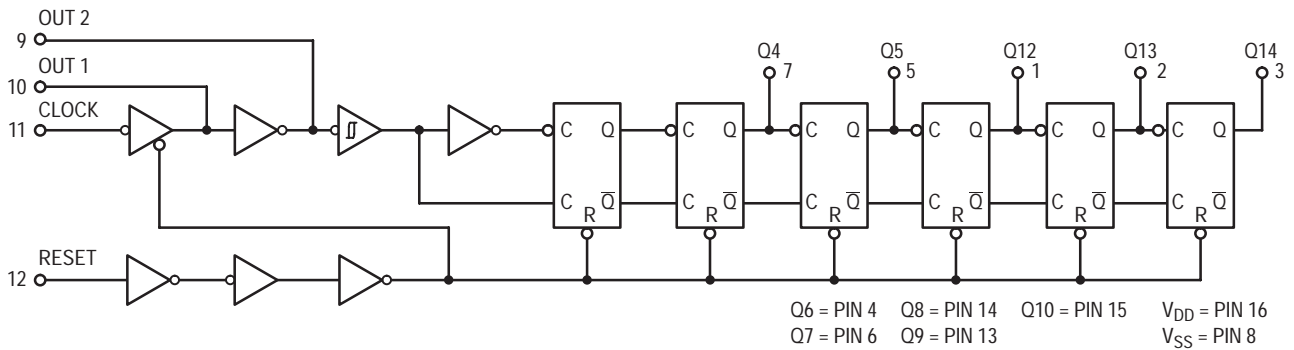
Q12	1 •	16	V <sub>DD</sub>
Q13	2	15	Q10
Q14	3	14	Q8
Q6	4	13	Q9
Q5	5	12	RESET
Q7	6	11	CLOCK
Q4	7	10	OUT 1
V <sub>SS</sub>	8	9	OUT 2

## TRUTH TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

X = Don't Care

## LOGIC DIAGRAM



# MC14060B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 V) (V <sub>O</sub> = 9.0 or 1.0 V) (V <sub>O</sub> = 13.5 or 1.5 V)  (V <sub>O</sub> = 0.5 or 4.5 V) (V <sub>O</sub> = 1.0 or 9.0 V) (V <sub>O</sub> = 1.5 or 13.5 V)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	V
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	V
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.0	—	11.0	8.25	—	11.0	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (For Input 11 (V <sub>O</sub> = 9.0 Vdc) and Output 10) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V <sub>OH</sub> = 2.5 V) (Except Source (V <sub>OH</sub> = 4.6 V) Pins 9 and 10) (V <sub>OH</sub> = 9.5 V) (V <sub>OH</sub> = 13.5 V)  (V <sub>OL</sub> = 0.4 V) Sink (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mA
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μA
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.25 μA/kHz) f + I <sub>DD</sub>							μA
		10	I <sub>T</sub> = (0.54 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (0.85 μA/kHz) f + I <sub>DD</sub>							

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14060B

## SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ (7.)	Max	Unit	
Output Rise Time (Counter Outputs)	t <sub>TLH</sub>	5.0	—	40	200	ns	
		10	—	25	100		
		15	—	20	80		
Output Fall Time (Counter Outputs)	t <sub>THL</sub>	5.0	—	50	200	ns	
		10	—	30	100		
		15	—	20	80		
Propagation Delay Time Clock to Q4	t <sub>PLH</sub> t <sub>PHL</sub>	5.0	—	415	740	ns	
		10	—	175	300		
		15	—	125	200		
	Clock to Q14		5.0	—	1.5	2.7	μs
			10	—	0.7	1.3	
			15	—	0.4	1.0	
Clock Pulse Width	t <sub>wH</sub>	5.0	100	65	—	ns	
		10	40	30	—		
		15	30	20	—		
Clock Pulse Frequency	f <sub>φ</sub>	5.0	—	5	3.5	MHz	
		10	—	14	8		
		15	—	17	12		
Clock Rise and Fall Time	t <sub>TLH</sub> t <sub>THL</sub>	5.0	No Limit			ns	
		10					
		15					
Reset Pulse Width	t <sub>w</sub>	5.0	120	40	—	ns	
		10	60	15	—		
		15	40	10	—		
Propagation Delay Time Reset to On	t <sub>PHL</sub>	5.0	—	170	350	ns	
		10	—	80	160		
		15	—	60	100		

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

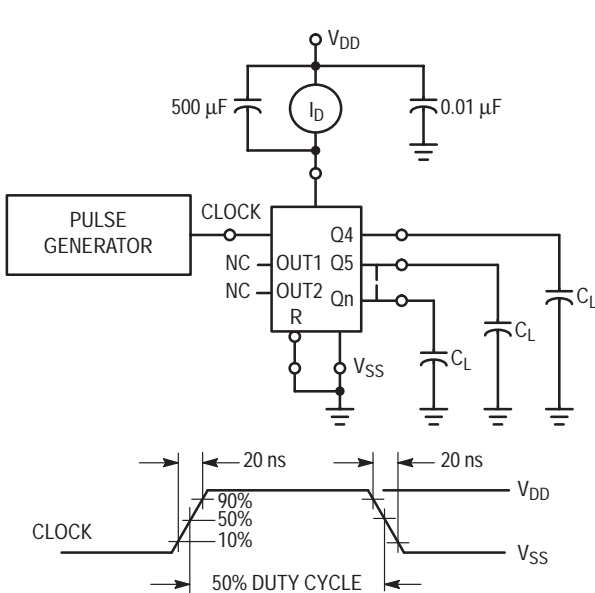


Figure 1. Power Dissipation Test Circuit and Waveform

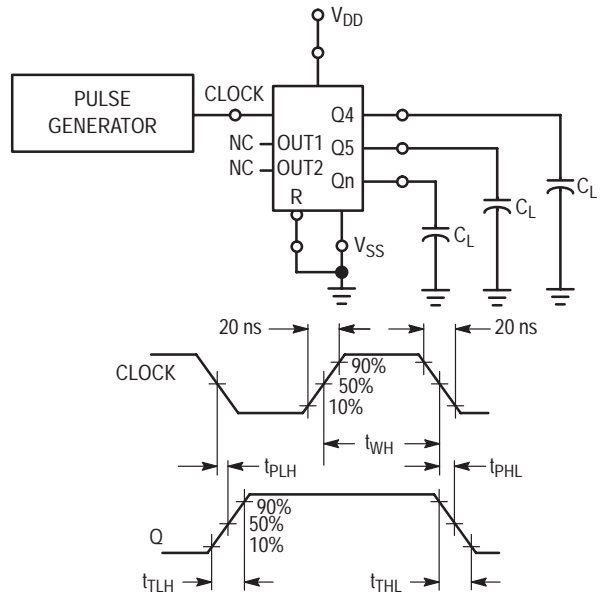
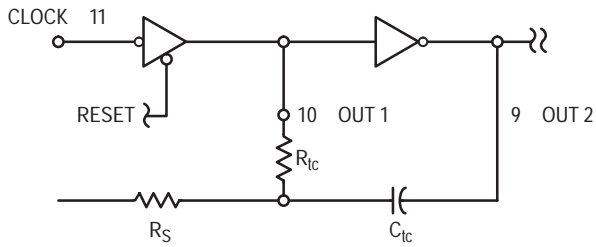


Figure 2. Switching Time Test Circuit and Waveforms



# MC14060B



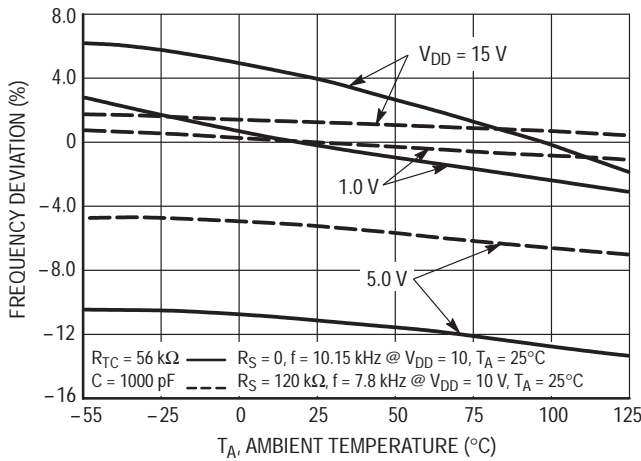
$$f \approx \frac{1}{2.3 R_{TC} C_{TC}}$$

if  $1 \text{ kHz} \leq f \leq 100 \text{ kHz}$   
and  $2R_{TC} < R_S < 10R_{TC}$   
(f in Hz, R in ohms, C in farads)

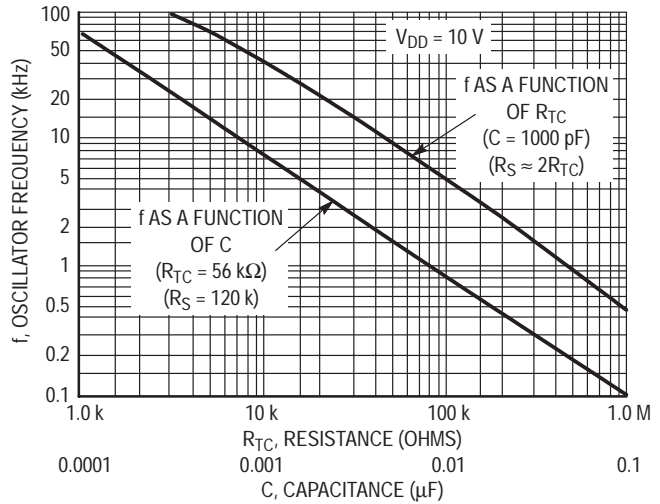
The formula may vary for other frequencies. Recommended maximum value for the resistors in  $1 \text{ M}\Omega$ .

**Figure 3. Oscillator Circuit Using RC Configuration**

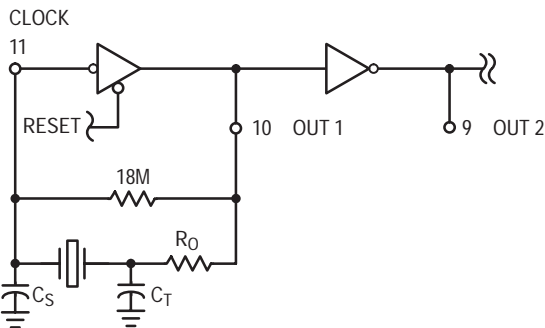
## TYPICAL RC OSCILLATOR CHARACTERISTICS



**Figure 4. RC Oscillator Stability**



**Figure 5. RC Oscillator Frequency as a Function of  $R_{TC}$  and C**



**Figure 6. Typical Crystal Oscillator Circuit**

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	32	kHz
Equivalent Resistance, $R_S$	1.0	6.2	$k\Omega$
External Resistor/Capacitor Values			
$R_0$	47	750	$k\Omega$
$C_T$	82	82	pF
$C_S$	20	20	pF
Frequency Stability			
Frequency Changes as a Function of $V_{DD}$ ( $T_A = 25^\circ\text{C}$ )			
$V_{DD}$ Change from 5.0 V to 10 V	+ 6.0	+ 2.0	ppm
$V_{DD}$ Change from 10 V to 15 V	+ 2.0	+ 2.0	ppm
Frequency Change as a Function of Temperature ( $V_{DD} = 10 \text{ V}$ )			
$T_A$ Change from $-55^\circ\text{C}$ to $+25^\circ\text{C}$ Complete Oscillator (8.)	+ 100	+ 120	ppm
$T_A$ Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ Complete Oscillator (8.)	- 160	- 560	ppm

8. Complete oscillator includes crystal, capacitors, and resistors.

**Figure 7. Typical Data for Crystal Oscillator Circuit**

# MC14066B

## Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise —  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  typical
- Pin-for-Pin Replacement for CD4016, MC14016B
- For Lower  $R_{ON}$ , Use The HC4066 High-Speed CMOS Device

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Control Pin	$\pm 10$	mA
$I_{SW}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

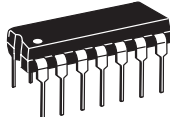
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.




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


**PDIP-14**  
P SUFFIX  
CASE 646

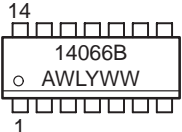
**MARKING DIAGRAMS**




14  
MC14066BCP  
AWLYYWW  
1




**SOIC-14**  
D SUFFIX  
CASE 751A



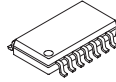
14  
14066B  
AWLYYWW  
1



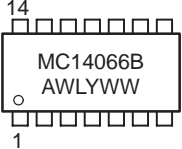
**TSSOP-14**  
DT SUFFIX  
CASE 948G



14  
14  
066B  
ALYW  
1



**SOEIAJ-14**  
F SUFFIX  
CASE 965



14  
MC14066B  
AWLYYWW  
1

A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

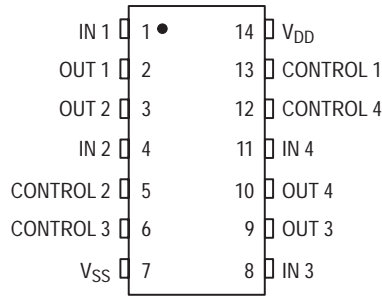
### ORDERING INFORMATION

Device	Package	Shipping
MC14066BCP	PDIP-14	2000/Box
MC14066BD	SOIC-14	55/Rail
MC14066BDR2	SOIC-14	2500/Tape & Reel
MC14066BDT	TSSOP-14	96/Rail
MC14066BDTEL	TSSOP-14	2000/Tape & Reel
MC14066BDTR2	TSSOP-14	2500/Tape & Reel
MC14066BF	SOEIAJ-14	See Note 1.
MC14066BFEL	SOEIAJ-14	See Note 1.

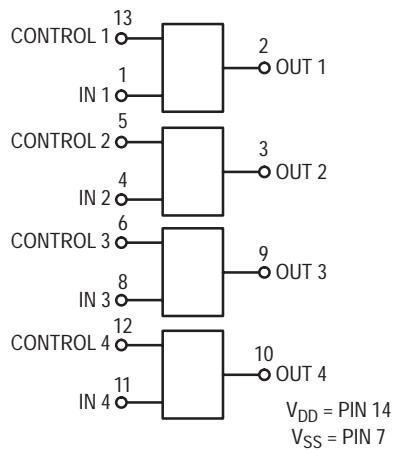
- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14066B

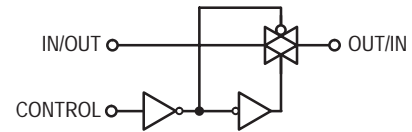
## PIN ASSIGNMENT



## BLOCK DIAGRAM



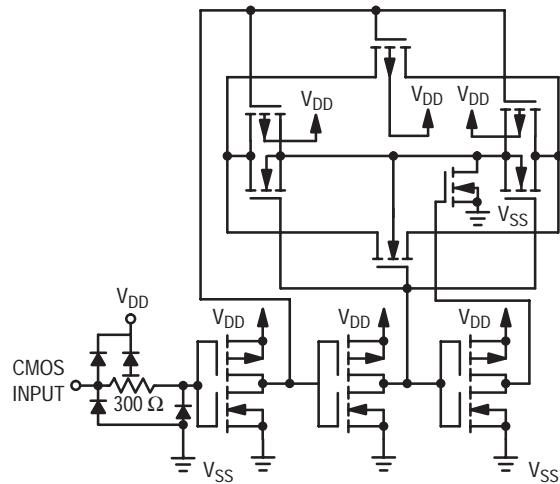
## LOGIC DIAGRAM AND TRUTH TABLE (1/4 OF DEVICE SHOWN)



Control	Switch
0 = $V_{SS}$	OFF
1 = $V_{DD}$	ON

Logic Diagram Restrictions  
 $V_{SS} \leq V_{in} \leq V_{DD}$   
 $V_{SS} \leq V_{out} \leq V_{DD}$

## CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



# MC14066B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV <sup>(5)</sup>	—	0.25	—	0.005	0.25	—	7.5	μA
		10		—	0.5	—	0.010	0.5	—	15	
		15		—	1.0	—	0.015	1.0	—	30	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>						μA	

### CONTROL INPUTS (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	—	1.5	—	2.25	1.5	—	1.5	V
		10		—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V <sub>IH</sub>	5.0	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5	—	3.5	2.75	—	3.5	—	V
		10		7.0	—	7.0	5.50	—	7.0	—	
		15		11	—	11	8.25	—	11	—	
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN AND OUT (Voltages Referenced to V<sub>SS</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 1)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0	ΔV <sub>switch</sub> ≤ 500 mV <sup>(5)</sup> , V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	—	800	—	250	1050	—	1200	Ω
		10		—	400	—	120	500	—	520	
		15		—	220	—	80	280	—	300	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (Figure 6)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	C <sub>I/O</sub>	—		—	—	—	0.47	—	—	—	pF

4. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
5. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14066B

## ELECTRICAL CHARACTERISTICS (6.) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (7.)	Max	Unit
Propagation Delay Times Input to Output ( $R_L = 10$ k $\Omega$ ) $t_{PLH}$ , $t_{PHL} = (0.17$ ns/pF) $C_L + 15.5$ ns $t_{PLH}$ , $t_{PHL} = (0.08$ ns/pF) $C_L + 6.0$ ns $t_{PLH}$ , $t_{PHL} = (0.06$ ns/pF) $C_L + 4.0$ ns	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	20 10 7.0	40 20 15	ns
Control to Output ( $R_L = 1$ k $\Omega$ ) (Figure 2) Output "1" to High Impedance	$t_{PHZ}$	5.0 10 15	— — —	40 35 30	80 70 60	ns
Output "0" to High Impedance	$t_{PLZ}$	5.0 10 15	— — —	40 35 30	80 70 60	ns
High Impedance to Output "1"	$t_{PZH}$	5.0 10 15	— — —	60 20 15	120 40 30	ns
High Impedance to Output "0"	$t_{PZL}$	5.0 10 15	— — —	60 20 15	120 40 30	ns
Second Harmonic Distortion ( $V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ k $\Omega$ , $f = 1.0$ kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) ( $R_L = 1$ k $\Omega$ , 20 Log ( $V_{out}/V_{in}$ ) = -3 dB, $C_L = 50$ pF, $V_{in} = 5$ V $_{p-p}$ )	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) ( $V_{in} = 5$ V $_{p-p}$ , $R_L = 1$ k $\Omega$ , $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	-50	—	dB
Channel Separation (Figure 4) ( $V_{in} = 5$ V $_{p-p}$ , $R_L = 1$ k $\Omega$ , $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	-50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) ( $R_1 = 1$ k $\Omega$ , $R_L = 10$ k $\Omega$ , Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV $_{p-p}$

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TEST CIRCUITS

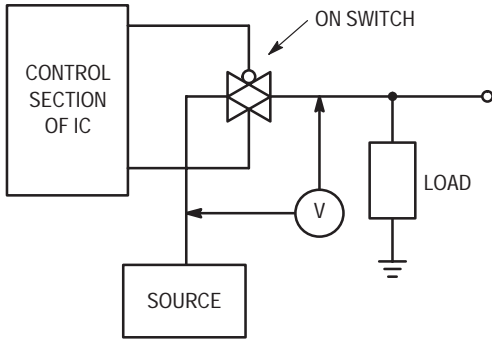


Figure 1.  $\Delta V$  Across Switch

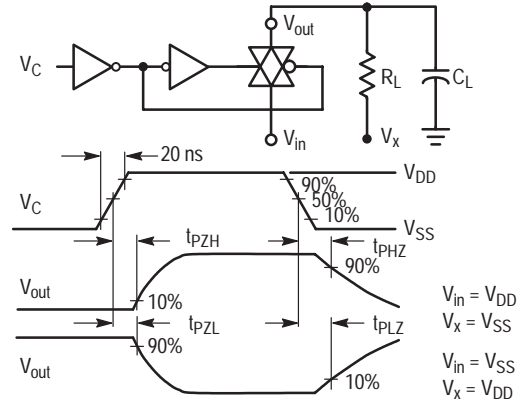


Figure 2. Turn-On Delay Time Test Circuit and Waveforms

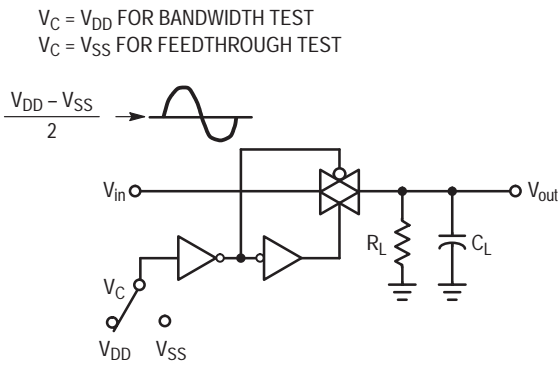


Figure 3. Bandwidth and Feedthrough Attenuation

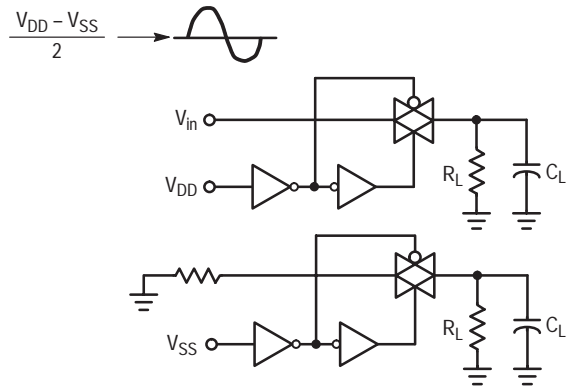


Figure 4. Channel Separation

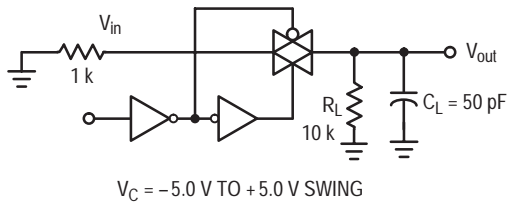


Figure 5. Crosstalk, Control to Output

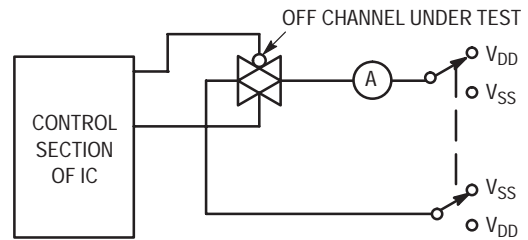


Figure 6. Off Channel Leakage

# MC14066B

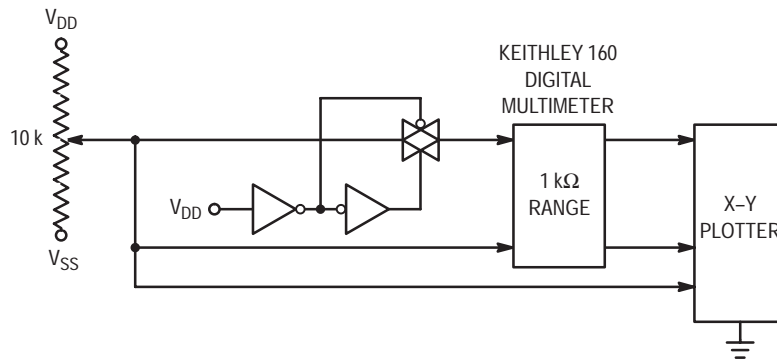


Figure 7. Channel Resistance ( $R_{ON}$ ) Test Circuit

## TYPICAL RESISTANCE CHARACTERISTICS

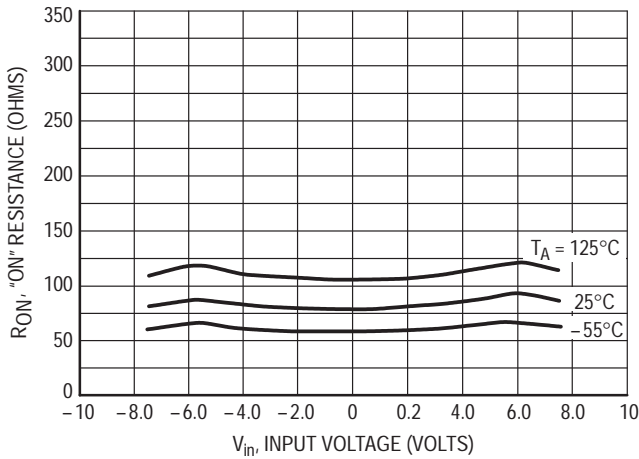


Figure 8.  $V_{DD} = 7.5 \text{ V}$ ,  $V_{SS} = -7.5 \text{ V}$

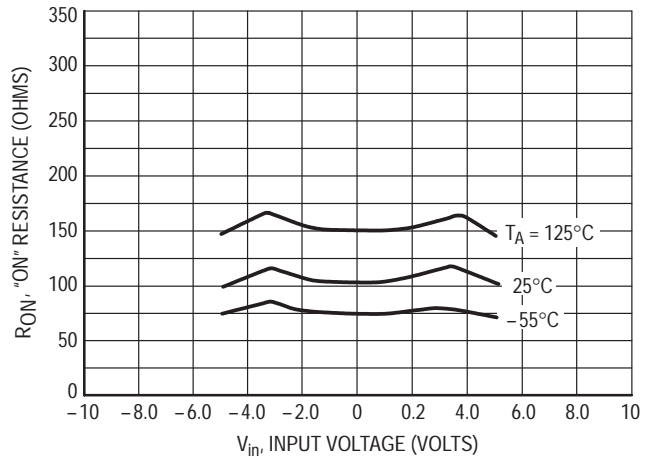


Figure 9.  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = -5.0 \text{ V}$

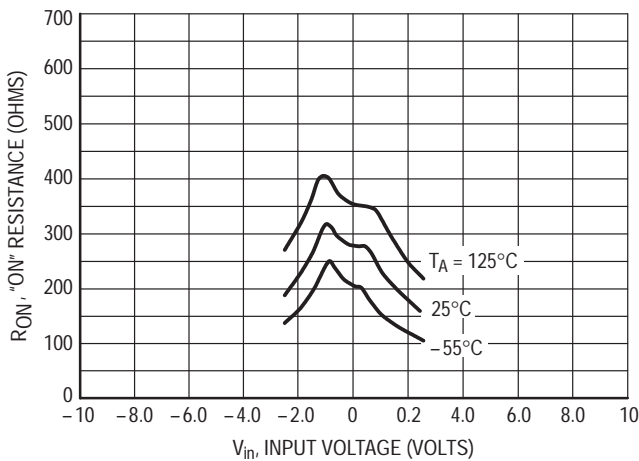


Figure 10.  $V_{DD} = 2.5 \text{ V}$ ,  $V_{SS} = -2.5 \text{ V}$

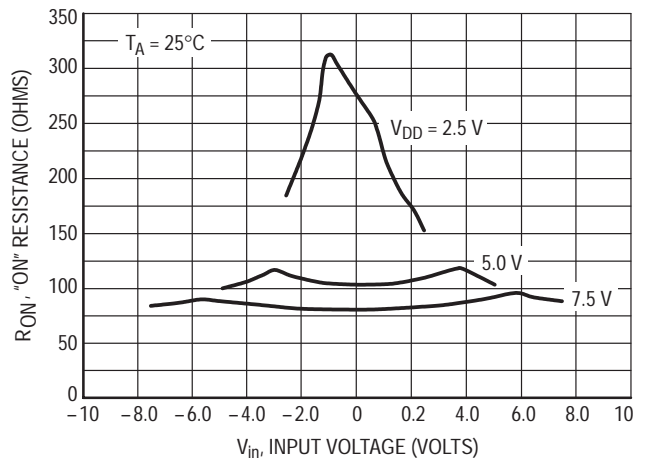


Figure 11. Comparison at  $25^\circ\text{C}$ ,  $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 volt digital control signal is used to directly control a 5 volt peak–to–peak analog signal.

The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage, the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5\text{ V} =$  logic high at the control inputs;  $V_{SS} = \text{GND} = 0\text{ V} =$  logic low.

The maximum analog signal level is determined by  $V_{DD}$  and  $V_{SS}$ . The analog voltage must not swing higher than  $V_{DD}$  or lower than  $V_{SS}$ .

The example shows a 5 volt peak–to–peak signal which allows no margin at either peak. If voltage transients above

$V_{DD}$  and/or below  $V_{SS}$  are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between  $V_{DD}$  and  $V_{SS}$  is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between  $V_{DD}$  and  $V_{SS}$ .

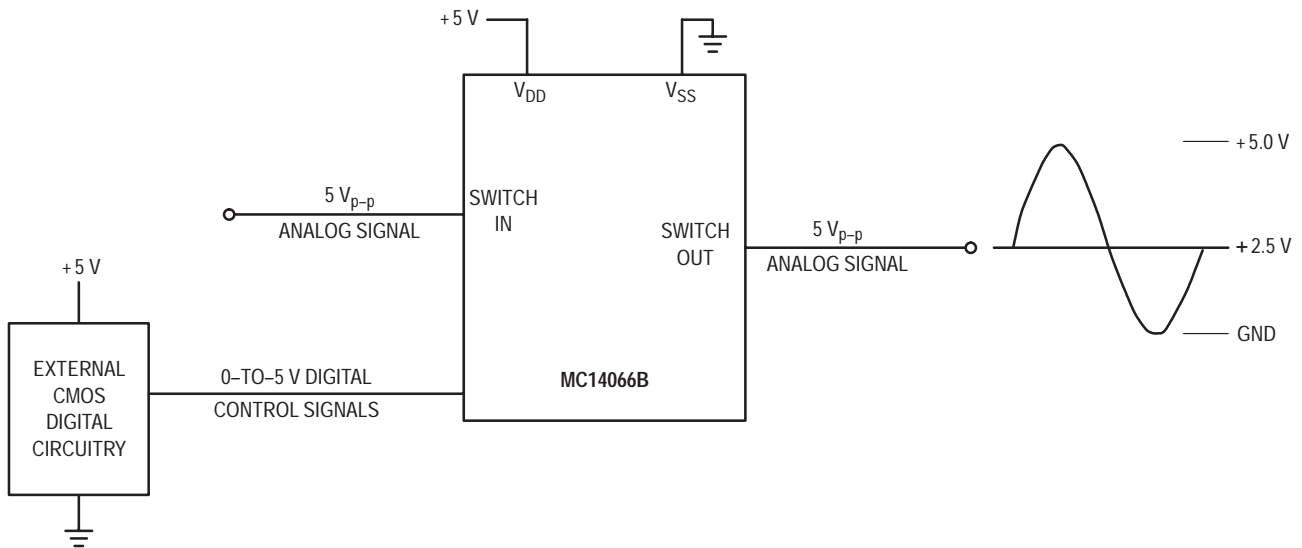


Figure A. Application Example

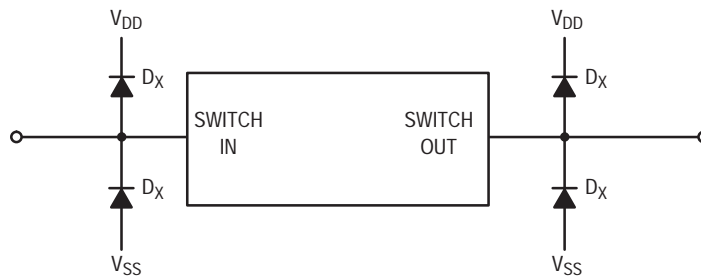


Figure B. External Germanium or Schottky Clipping Diodes



# MC14067B

## Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	- 55 to + 125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

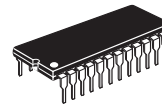
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



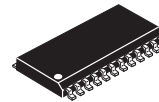
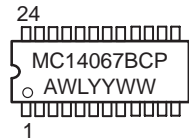
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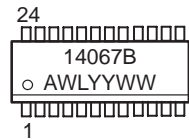
### MARKING DIAGRAMS



PDIP-24  
P SUFFIX  
CASE 709



SOIC-24  
DW SUFFIX  
CASE 751E



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

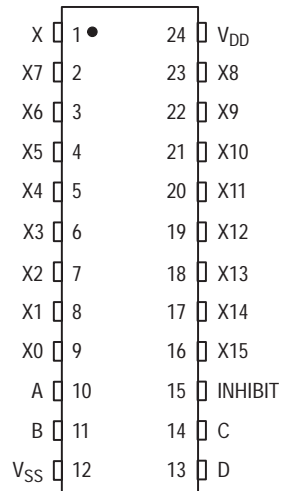
Device	Package	Shipping
MC14067BCP	PDIP-24	15/Rail
MC14067BDW	SOIC-24	30/Rail
MC14067BDWR2	SOIC-24	1000/Tape & Reel

# MC14067B

MC14067 TRUTH TABLE

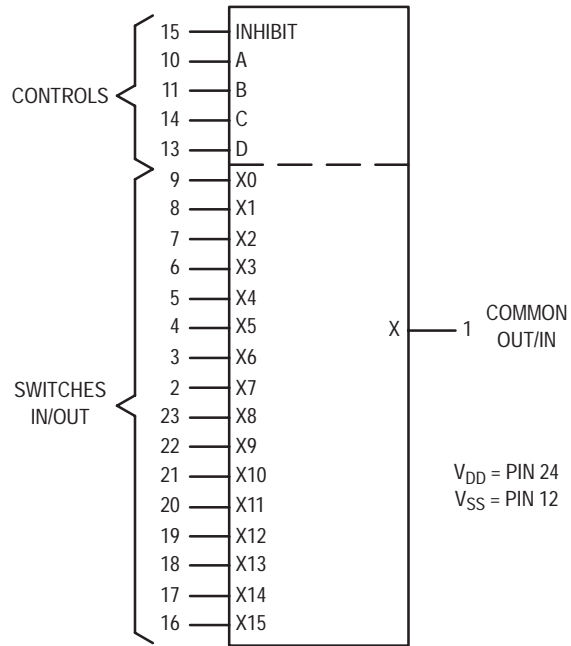
Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

MC14067B  
PIN ASSIGNMENT

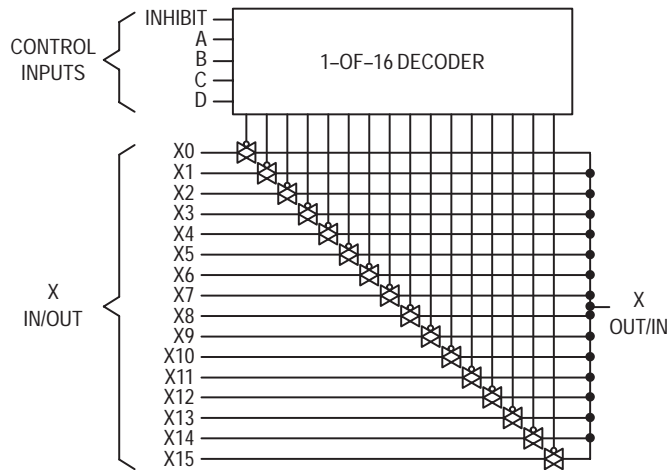


# MC14067B

## MC14067B 16-Channel Analog Multiplexer/Demultiplexer



### MC14067 FUNCTIONAL DIAGRAM



# MC14067B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
<b>SUPPLY REQUIREMENTS</b> (Voltages Referenced to V <sub>SS</sub> )											
Power Supply Voltage Range	V <sub>DD</sub>	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV <sup>(4.)</sup>	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>							μA
<b>CONTROL INPUTS — INHIBIT, A, B, C, D</b> (Voltages Referenced to V <sub>SS</sub> )											
Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF
<b>SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y</b> (Voltages Referenced to V <sub>SS</sub> )											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch <sup>(4.)</sup> (Figure 1)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV <sup>(4.)</sup> , V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> 0 to V <sub>DD</sub> (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 2)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Inhibit = V <sub>DD</sub>	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—	Inhibit = V <sub>DD</sub> (MC14067B) (MC14097B)	— —	— —	— —	100 60	— —	— —	— —	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	— —	Pins Not Adjacent Pins Adjacent	—	—	—	0.47	—	—	—	pF

3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

4. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14067B

## ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> - V <sub>SS</sub> V <sub>dc</sub>	Typ <sup>(5.)</sup>	Max	Unit
Propagation Delay Times Channel Input-to-Channel Output (R <sub>L</sub> = 200 kΩ) MC14067B	t <sub>PLH</sub> , t <sub>PHL</sub> (Figure 3)	5.0	35	90	ns
		10	15	40	
		15	12	30	
Control Input-to-Channel Output Channel Turn-On Time (R <sub>L</sub> = 10 kΩ) MC14067B	t <sub>PZH</sub> , t <sub>PZL</sub> (Figure 4)	5.0	240	600	ns
		10	115	290	
		15	75	190	
Channel Turn-Off Time (R <sub>L</sub> = 300 kΩ) MC14067B	t <sub>PHZ</sub> , t <sub>PLZ</sub> (Figure 4)	5.0	250	625	ns
		10	120	300	
		15	75	190	
Any Pair of Address Inputs to Output MC14067B	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	280	700	ns
		10	115	290	
		15	85	215	
Second Harmonic Distortion (R <sub>L</sub> = 10 kΩ, f = 1 kHz, V <sub>in</sub> = 5 V <sub>p-p</sub> )	—	10	0.3	—	%
ON Channel Bandwidth [R <sub>L</sub> = 1 kΩ, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] 20 Log <sub>10</sub> (V <sub>out</sub> /V <sub>in</sub> ) = -3 dB MC14067B	BW (Figure 5)	10	15	—	MHz
Off Channel Feedthrough Attenuation [R <sub>L</sub> = 1 kΩ, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] f <sub>in</sub> = 20 MHz - MC14067B	— (Figure 5)	10	-40	—	dB
Channel Separation [R <sub>L</sub> = 1 kΩ, V <sub>in</sub> = 1/2 (V <sub>DD</sub> - V <sub>SS</sub> ) p-p (sine-wave)] f <sub>in</sub> = 20 MHz	— (Figure 6)	10	-40	—	dB
Crosstalk, Control Inputs-to-Common O/I (R <sub>1</sub> = 1 kΩ, R <sub>L</sub> = 10 kΩ, Control t <sub>r</sub> = t <sub>f</sub> = 20 ns, Inhibit = V <sub>SS</sub> )	— (Figure 7)	10	30	—	mV

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

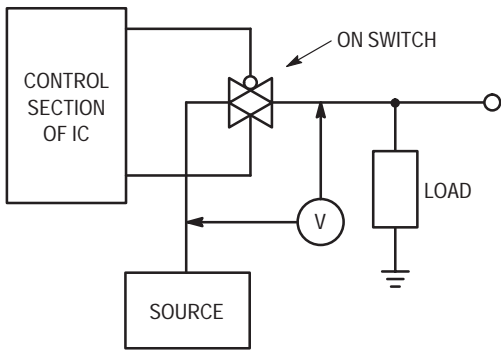


Figure 1.  $\Delta V$  Across Switch

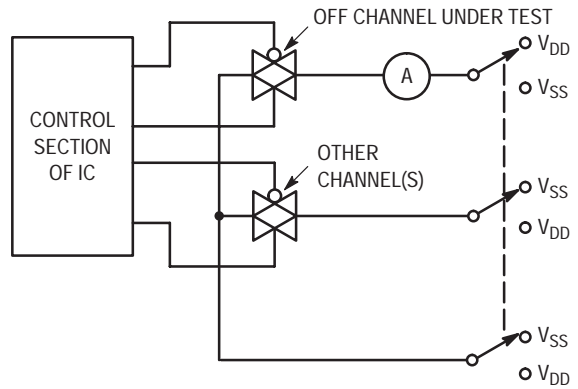


Figure 2. Off Channel Leakage

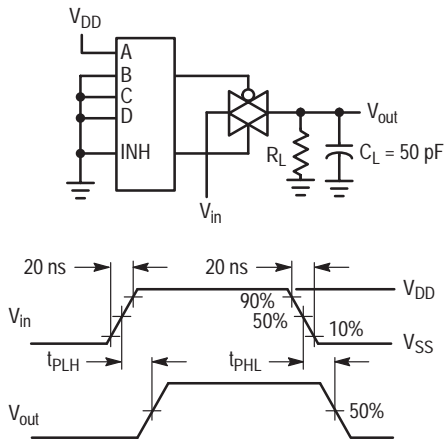


Figure 3. Propagation Delay Test Circuit and Waveforms  $V_{in}$  to  $V_{out}$

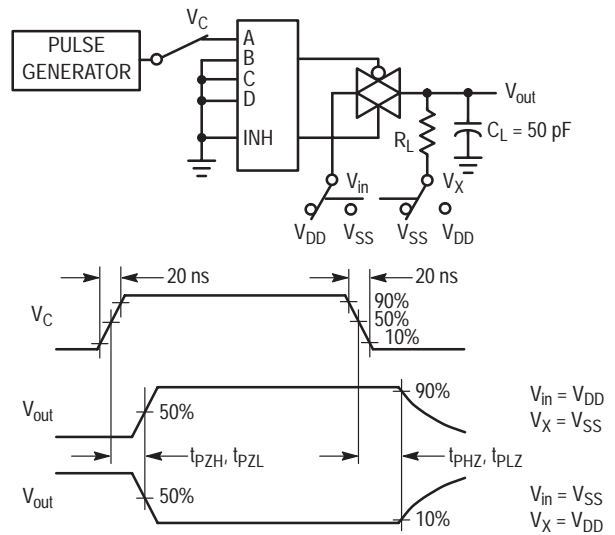
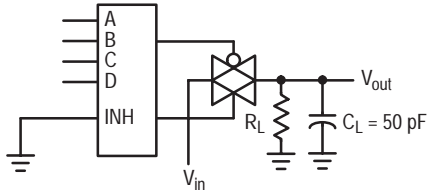


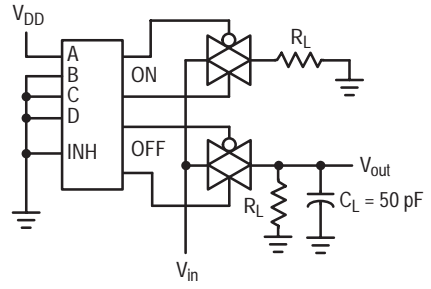
Figure 4. Turn-On and Delay Turn-Off Test Circuit and Waveforms

# MC14067B

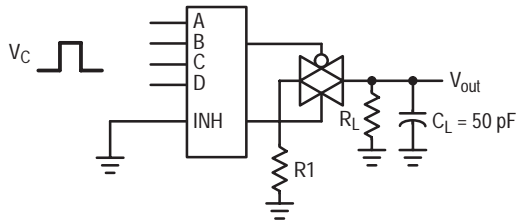
A, B, and C inputs used to turn ON or OFF the switch under test.



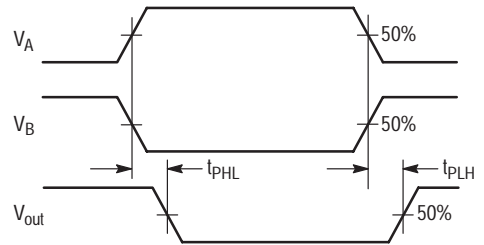
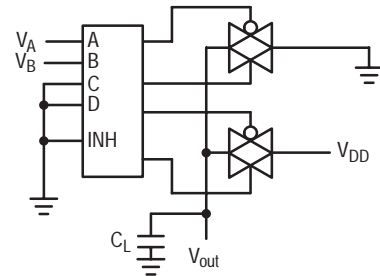
**Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation**



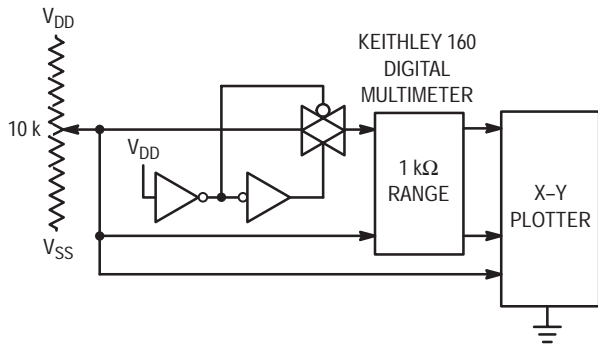
**Figure 6. Channel Separation (Adjacent Channels Used for Setup)**



**Figure 7. Crosstalk, Control to Common O/I**



**Figure 9. Propagation Delay, Any Pair of Address Inputs to Output**



**Figure 8. Channel Resistance ( $R_{ON}$ ) Test Circuit**

TYPICAL RESISTANCE CHARACTERISTICS

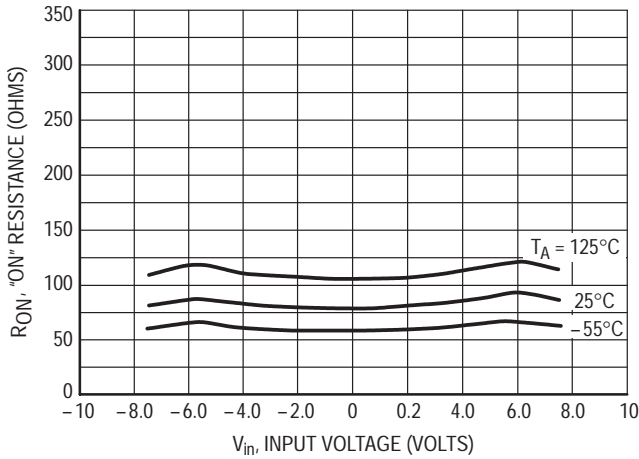


Figure 10.  $V_{DD} = 7.5\text{ V}$ ,  $V_{SS} = -7.5\text{ V}$

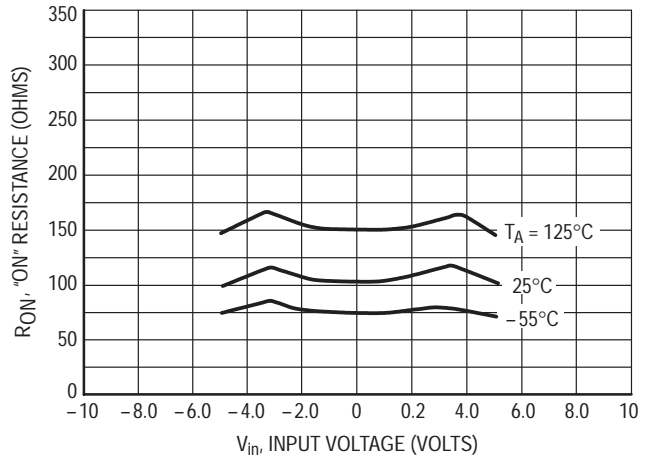


Figure 11.  $V_{DD} = 5.0\text{ V}$ ,  $V_{SS} = -5.0\text{ V}$

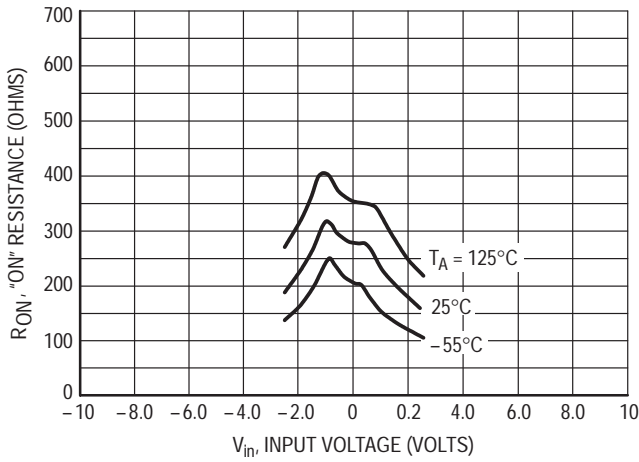


Figure 12.  $V_{DD} = 2.5\text{ V}$ ,  $V_{SS} = -2.5\text{ V}$

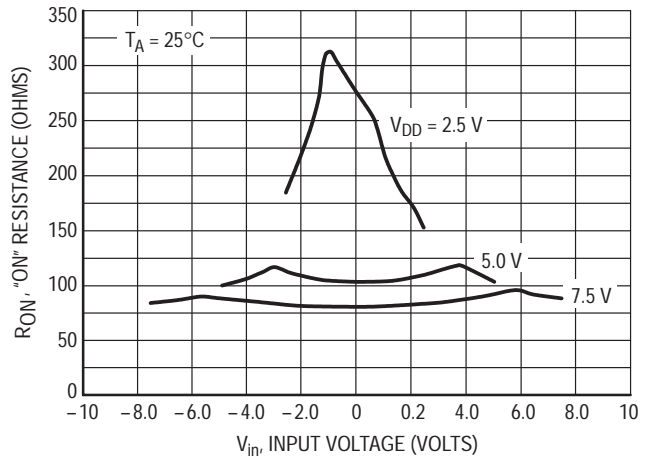


Figure 13. Comparison at  $25^\circ\text{C}$ ,  $V_{DD} = -V_{SS}$



APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0-to-5 volt Digital Control signal is used to directly control a 5 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>SS</sub>. The analog voltage must swing neither higher than V<sub>DD</sub> nor lower than V<sub>SS</sub>. The example shows a 5 V<sub>p-p</sub>

signal which allows no margin at either peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>SS</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>SS</sub> is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V<sub>DD</sub> and V<sub>SS</sub>.

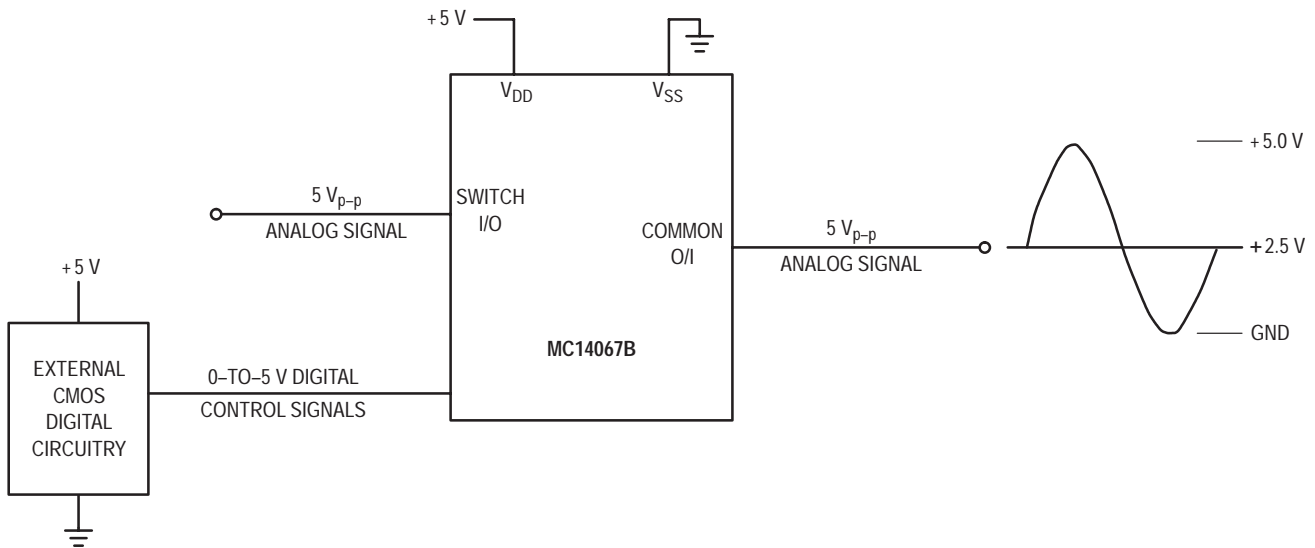


Figure A. Application Example

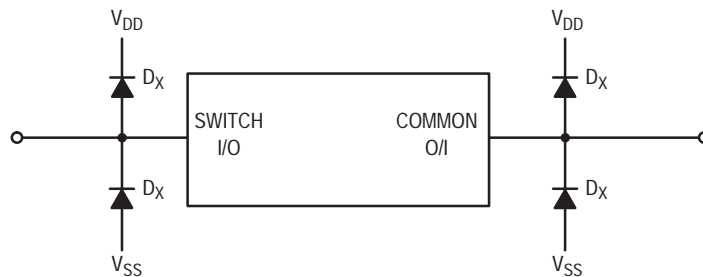


Figure B. External Germanium or Schottky Clipping Diodes

# MC14069UB

## Hex Inverter

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor

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**MARKING DIAGRAMS**

**PDIP-14**  
**P SUFFIX**  
**CASE 646**

MC14069UBCP  
AWLYYWW

**SOIC-14**  
**D SUFFIX**  
**CASE 751A**

14069U  
AWLYYWW

**TSSOP-14**  
**DT SUFFIX**  
**CASE 948G**

14  
069U  
ALYW

**SOEIAJ-14**  
**F SUFFIX**  
**CASE 965**

MC14069U  
AWLYYWW

A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

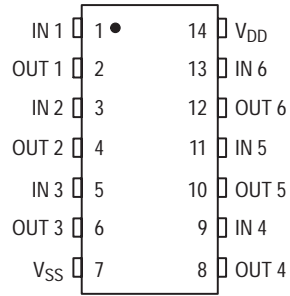
### ORDERING INFORMATION

Device	Package	Shipping
MC14069UBCP	PDIP-14	2000/Box
MC14069UBD	SOIC-14	2750/Box
MC14069UBDR2	SOIC-14	2500/Tape & Reel
MC14069UBDT	TSSOP-14	96/Rail
MC14069UBDTEL	TSSOP-14	2000/Tape & Reel
MC14069UBDTR2	TSSOP-14	2500/Tape & Reel
MC14069UBF	SOEIAJ-14	See Note 1.
MC14069UBFEL	SOEIAJ-14	See Note 1.

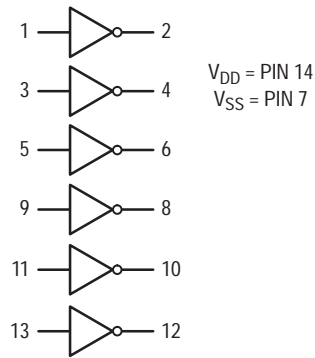
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14069UB

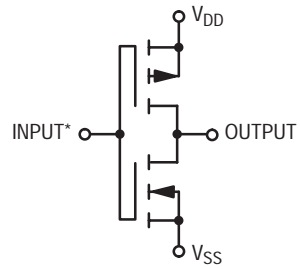
## PIN ASSIGNMENT



## LOGIC DIAGRAM



## CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



\*Double diode protection on all inputs not shown.

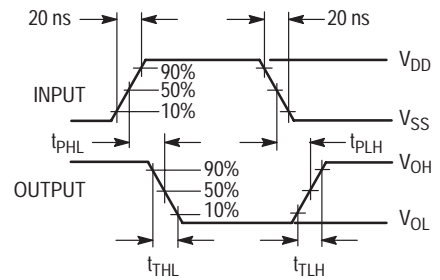
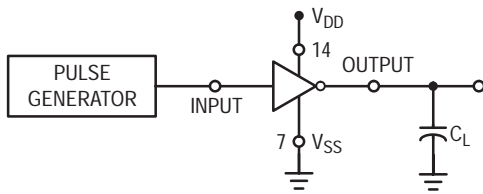


Figure 1. Switching Time Test Circuit and Waveforms

# MC14069UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub>  V <sub>in</sub> = 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 Vdc) (V <sub>O</sub> = 9.0 Vdc) (V <sub>O</sub> = 13.5 Vdc)  (V <sub>O</sub> = 0.5 Vdc) (V <sub>O</sub> = 1.0 Vdc) (V <sub>O</sub> = 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
		15	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Gate) (C <sub>L</sub> = 50 pF)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub> /6							μAdc
10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> /6									
15	I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub> /6									
Output Rise and Fall Times (5.) (C <sub>L</sub> = 50 pF) t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.60 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.40 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	—	—	—	100	200	—	—	ns
		10	—	—	—	50	100	—	—	
		15	—	—	—	40	80	—	—	
		—	—	—	—	—	—	—	—	
Propagation Delay Times (5.) (C <sub>L</sub> = 50 pF) t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 20 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 22 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 17 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	—	—	—	65	125	—	—	ns
		10	—	—	—	40	75	—	—	
		15	—	—	—	30	55	—	—	
		—	—	—	—	—	—	—	—	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14070B, MC14077B

## CMOS SSI

### Quad Exclusive “OR” and “NOR” Gates

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B and CD4070B Types
- MC14077B — Replacement for CD4077B Type

#### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C

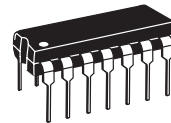
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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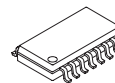
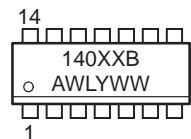


PDIP-14  
P SUFFIX  
CASE 646

#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



SOEIAJ-14  
F SUFFIX  
CASE 965



XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

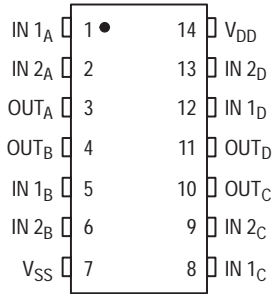
#### ORDERING INFORMATION

Device	Package	Shipping
MC140XXBCP	PDIP-14	2000/Box
MC140XXBD	SOIC-14	2750/Box
MC140XXBDR2	SOIC-14	2500/Tape & Reel
MC140XXBF	SOEIAJ-14	See Note 1.
MC140XXBFEL	SOEIAJ-14	See Note 1.

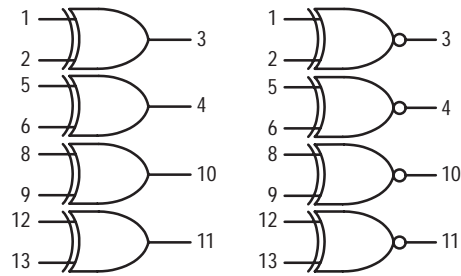
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14070B, MC14077B

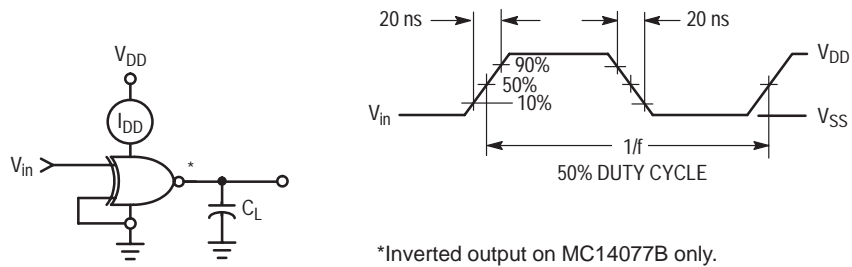
## PIN ASSIGNMENT



<b>MC14070B</b>	<b>MC14077B</b>
<b>QUAD Exclusive OR</b>	<b>QUAD Exclusive NOR</b>
<b>Gate</b>	<b>Gate</b>

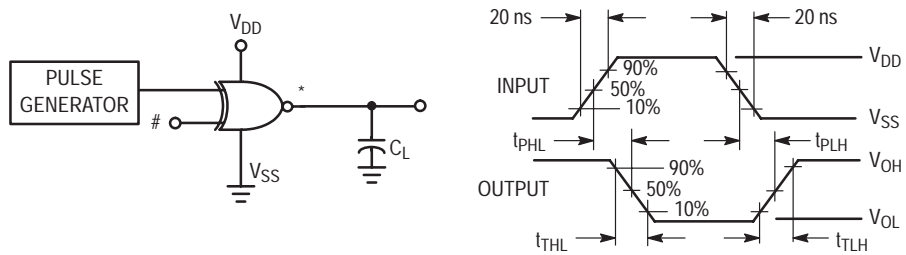


V<sub>DD</sub> = PIN 14  
V<sub>SS</sub> = PIN 7  
(BOTH DEVICES)



\*Inverted output on MC14077B only.

**Figure 1. Power Dissipation Test Circuit and Waveform**



\*Inverted output on MC14077B only.

#Connect unused input to V<sub>DD</sub> for MC14070B, to V<sub>SS</sub> for MC14077B.

**Figure 2. Switching Time Test Circuit and Waveforms**

# MC14070B, MC14077B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—	
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.3 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (0.9 μA/kHz) f + I <sub>DD</sub>							
Output Rise and Fall Times (5.) (C <sub>L</sub> = 50 pF) t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.60 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.40 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	—	—	—	100	200	—	—	ns
		10	—	—	—	50	100	—	—	
		15	—	—	—	40	80	—	—	
		—	—	—	—	—	—	—	—	
Propagation Delay Times (5.) (C <sub>L</sub> = 50 pF) t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 130 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 57 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 37 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0	—	—	—	175	350	—	—	ns
		10	—	—	—	75	150	—	—	
		15	—	—	—	55	110	—	—	
		—	—	—	—	—	—	—	—	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I<sub>T</sub> is in μH (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14076B

## 4-Bit D-Type Register with Three-State Outputs

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master root is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

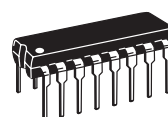
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



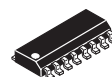
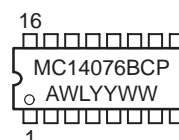
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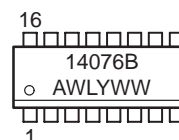
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

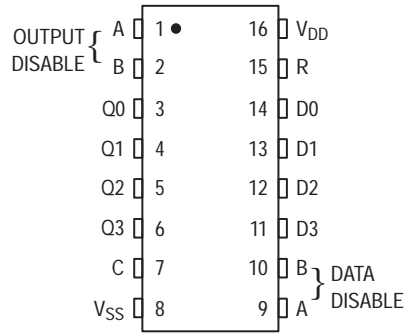
### ORDERING INFORMATION

Device	Package	Shipping
MC14076BCP	PDIP-16	2000/Box
MC14076BD	SOIC-16	2400/Box
MC14076BDR2	SOIC-16	2500/Tape & Reel

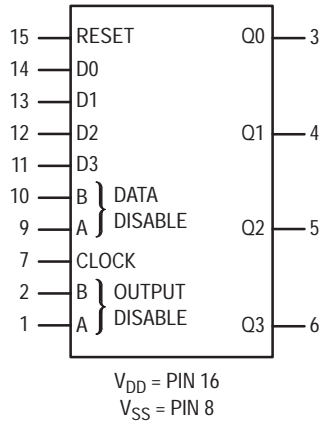


# MC14076B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## FUNCTION TABLE

Inputs						Output Q
Reset	Clock	Data Disable		Data D		
		A	B			
1	X	X	X	X	0	
0	0	X	X	X	$Q_n$	
0	$\nearrow$	1	X	X	$Q_n$	
0	$\nearrow$	X	1	X	$Q_n$	
0	$\nearrow$	0	0	0	0	
0	$\nearrow$	0	0	1	1	

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.  
X = Don't Care.

# MC14076B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  "1" Level ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	$V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  Sink ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	$I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mA <sub>dc</sub>
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mA <sub>dc</sub>
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μA <sub>dc</sub>
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	μA <sub>dc</sub>
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (0.75 \mu\text{A/kHz}) f + I_{DD}$							μA <sub>dc</sub>
		10	$I_T = (1.50 \mu\text{A/kHz}) f + I_{DD}$							
		15	$I_T = (2.25 \mu\text{A/kHz}) f + I_{DD}$							
Three-State Leakage Current	$I_{TL}$	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μA <sub>dc</sub>

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in μA (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.002$ .

# MC14076B

## SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ <sup>(7.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	300 125 90  300 125 90	600 250 180  600 250 180	ns
3-State Propagation Delay, Output "1" or "0" to High Impedance	$t_{PHZ}$ , $t_{PLZ}$	5.0 10 15	— — —	150 60 45	300 120 90	ns
3-State Propagation Delay, High Impedance to "1" or "0" Level	$t_{PZH}$ , $t_{PZL}$	5.0 10 15	— — —	200 80 60	400 160 120	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	260 110 80	130 55 40	— — —	ns
Reset Pulse Width	$t_{WH}$	5.0 10 15	370 150 110	185 75 55	— — —	ns
Data Setup Time	$t_{su}$	5.0 10 15	30 10 4	15 5 2	— — —	ns
Data Hold Time	$t_h$	5.0 10 15	130 60 50	65 30 25	— — —	ns
Data Disable Setup Time	$t_{su}$	5.0 10 15	220 80 50	110 40 25	— — —	ns
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.6 9.0 12	1.8 4.5 6.0	MHz

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14076B

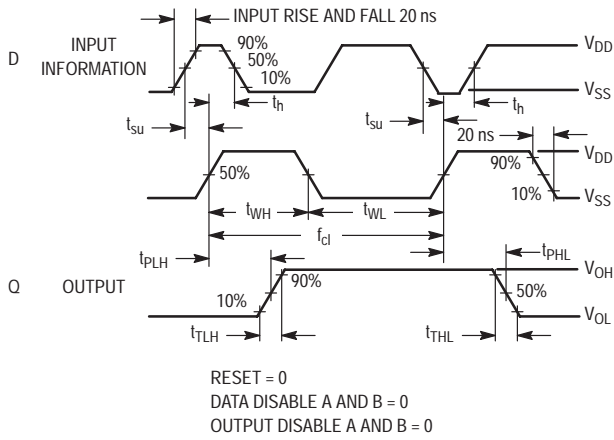


Figure 1. Timing Diagram

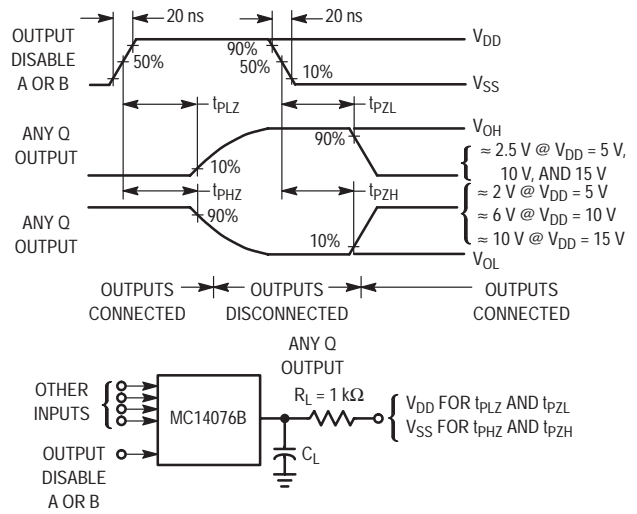
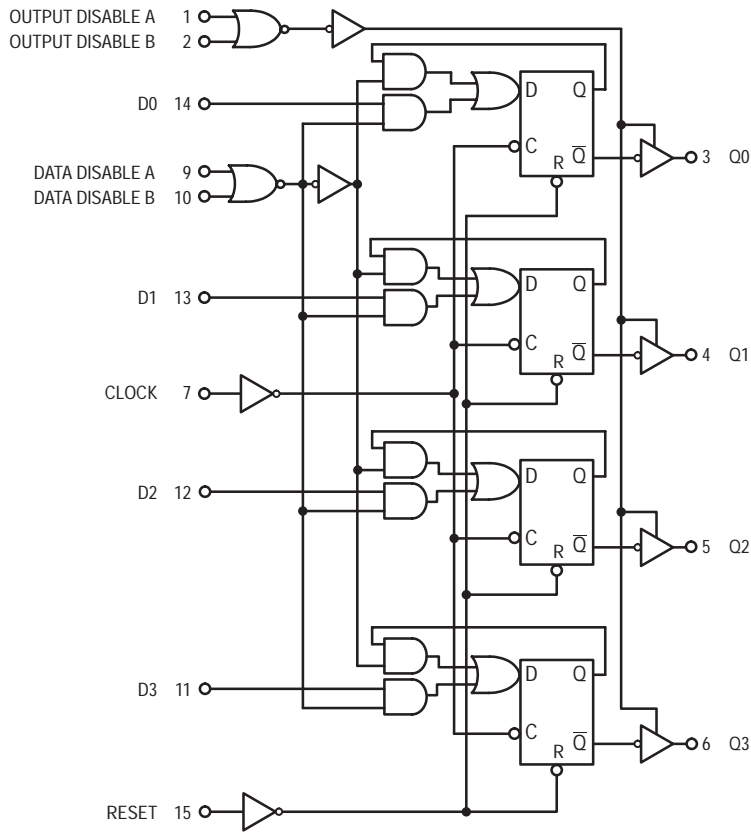


Figure 2. Three-State Propagation Delay Waveshape and Circuit

## EQUIVALENT FUNCTIONAL BLOCK DIAGRAM



# MC14093B

## Quad 2-Input “NAND” Schmitt Trigger

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to “square up” slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B
- Independent Schmitt-Trigger at each Input

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

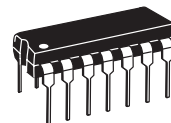
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



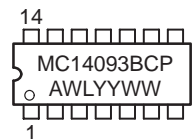
ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



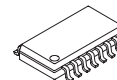
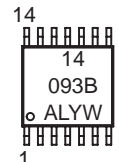
PDIP-14  
P SUFFIX  
CASE 646



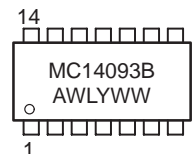
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

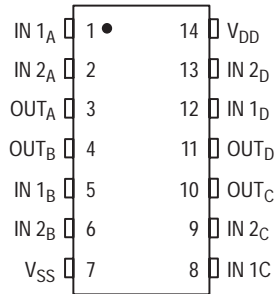
### ORDERING INFORMATION

Device	Package	Shipping
MC14093BCP	PDIP-14	2000/Box
MC14093BD	SOIC-14	2750/Box
MC14093BDR2	SOIC-14	2500/Tape & Reel
MC14093BDT	TSSOP-14	96/Rail
MC14093BDTEL	TSSOP-14	2000/Tape & Reel
MC14093BDTR2	TSSOP-14	2500/Tape & Reel
MC14093BF	SOEIAJ-14	See Note 1.
MC14093BFEL	SOEIAJ-14	See Note 1.

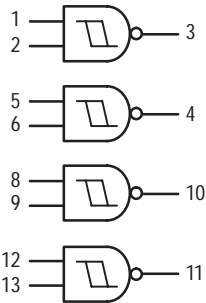
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14093B

## PIN ASSIGNMENT

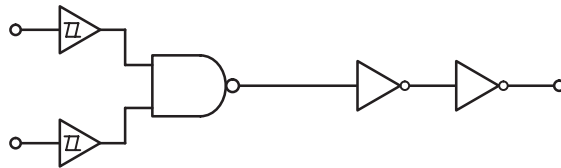


## LOGIC DIAGRAM



V<sub>DD</sub> = PIN 14  
V<sub>SS</sub> = PIN 7

## EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



# MC14093B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.2 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (3.6 μA/kHz) f + I <sub>DD</sub>							
Hysteresis Voltage	V <sub>H†</sub>	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
		10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
		15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive-Going  Negative-Going	V <sub>T+</sub>	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
		10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
	V <sub>T-</sub>	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	Vdc
		10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14093B

## SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	125 50 40	250 100 80	ns

7. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

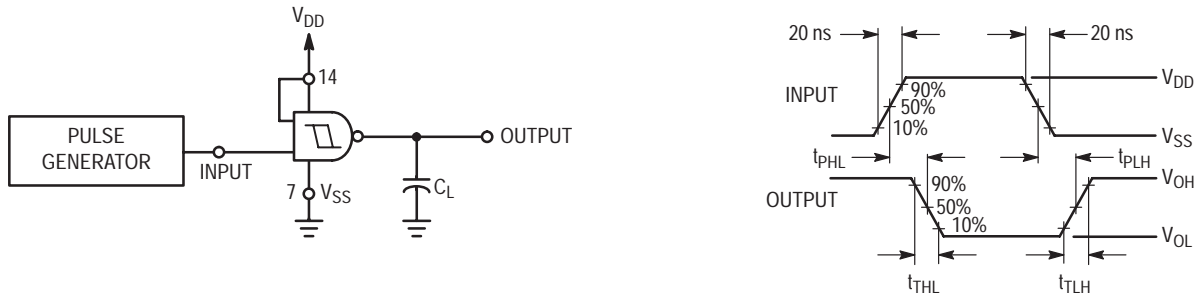


Figure 1. Switching Time Test Circuit and Waveforms

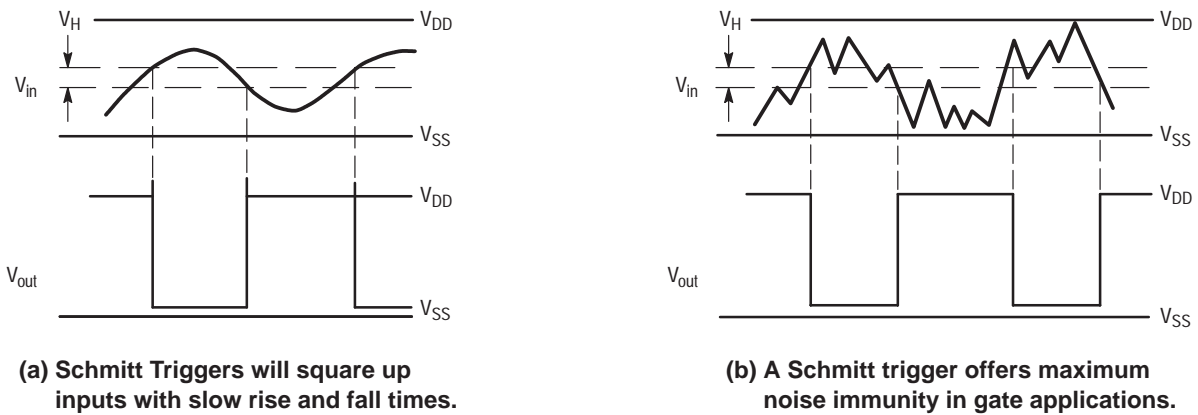
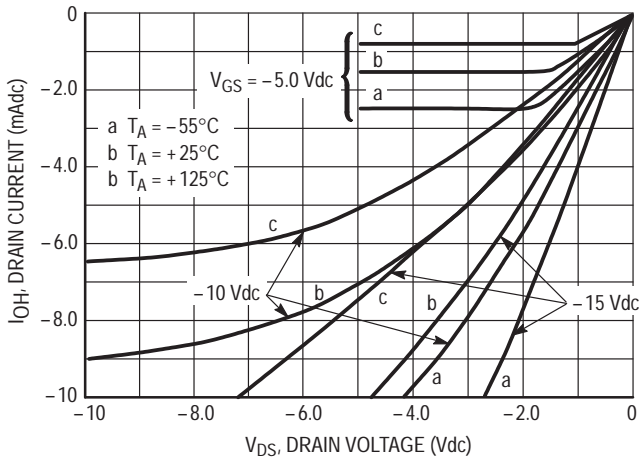
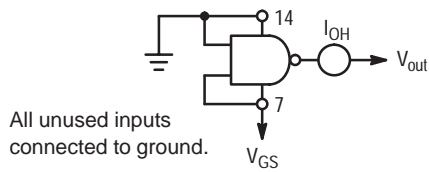


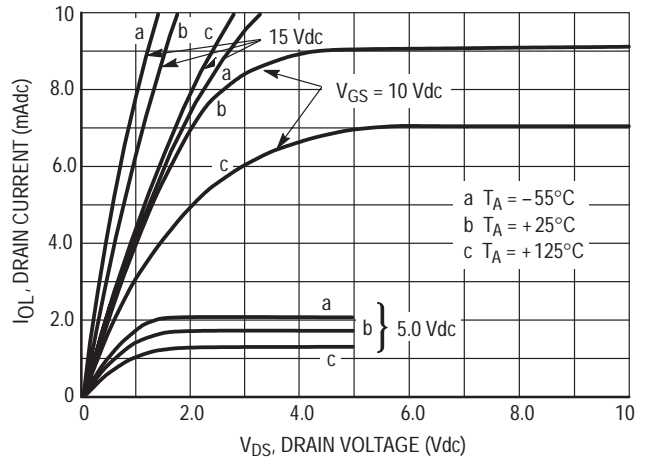
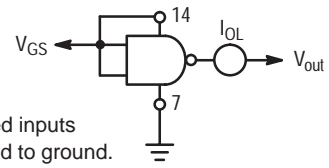
Figure 2. Typical Schmitt Trigger Applications



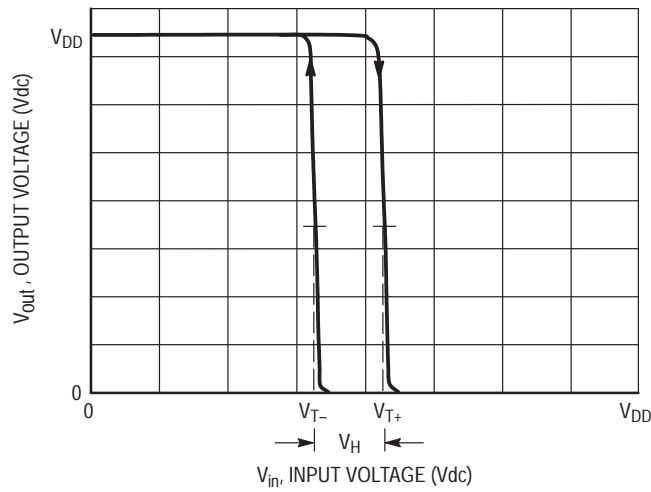
# MC14093B



**Figure 3. Typical Output Source Characteristics Test Circuit**



**Figure 4. Typical Output Sink Characteristics Test Circuit**



**Figure 5. Typical Transfer Characteristics**

# MC14094B

## 8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The  $Q_5$  output data is for use in high-speed cascaded systems. The  $Q'_5$  output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

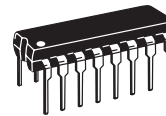


**ON Semiconductor**

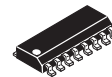
Formerly a Division of Motorola

<http://onsemi.com>

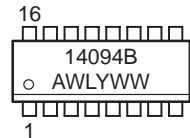
### MARKING DIAGRAMS



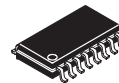
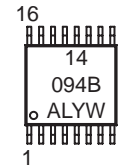
PDIP-16  
P SUFFIX  
CASE 648



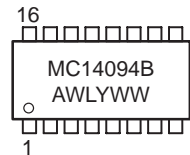
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

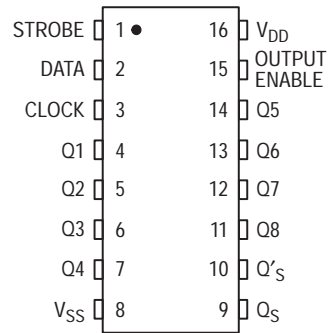
### ORDERING INFORMATION

Device	Package	Shipping
MC14094BCP	PDIP-16	2000/Box
MC14094BD	SOIC-16	48/Rail
MC14094BDR2	SOIC-16	2500/Tape & Reel
MC14094BDT	TSSOP-16	96/Rail
MC14094BDTR2	TSSOP-16	2500/Tape & Reel
MC14094BF	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14094B

## PIN ASSIGNMENT



Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q <sub>N</sub>	Q <sub>S</sub> *	Q'S
	0	X	X	Z	Z	Q7	No Chg.
	0	X	X	Z	Z	No Chg.	Q7
	1	0	X	No Chg.	No Chg.	Q7	No Chg.
	1	1	0	0	Q <sub>N</sub> -1	Q7	No Chg.
	1	1	1	1	Q <sub>N</sub> -1	Q7	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance    X = Don't Care

\* At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q<sub>S</sub>.

# MC14094B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage  $V_O = 4.5$ or $0.5$ Vdc $V_O = 9.0$ or $1.0$ Vdc $V_O = 13.5$ or $1.5$ Vdc  $V_O = 0.5$ or $4.5$ Vdc $V_O = 1.0$ or $9.0$ Vdc $V_O = 1.5$ or $13.5$ Vdc	"0" Level  $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level  $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current  Source $V_{OH} = 2.5$ Vdc $V_{OH} = 4.6$ Vdc $V_{OH} = 9.5$ Vdc $V_{OH} = 13.5$ Vdc  Sink $V_{OL} = 0.4$ Vdc $V_{OL} = 0.5$ Vdc $V_{OL} = 1.5$ Vdc	$I_{OH}$	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
15		4.2	—	3.4	8.8	—	2.4	—			
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc	
Input Capacitance $(V_{in} = 0)$	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (4.1 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc	
		10	$I_T = (14 \mu\text{A/kHz}) f + I_{DD}$								
		15	$I_T = (140 \mu\text{A/kHz}) f + I_{DD}$								
3-State Output Leakage Current	$I_{TL}$	15	—	$\pm 0.1$	—	$\pm 0.0001$	$\pm 0.1$	—	$\pm 3.0$	$\mu$ A	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

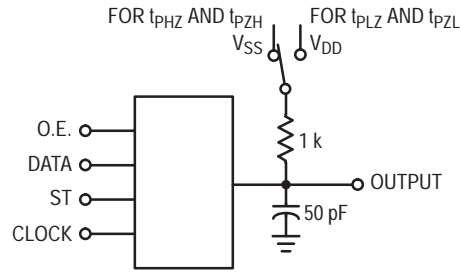
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu$ A (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

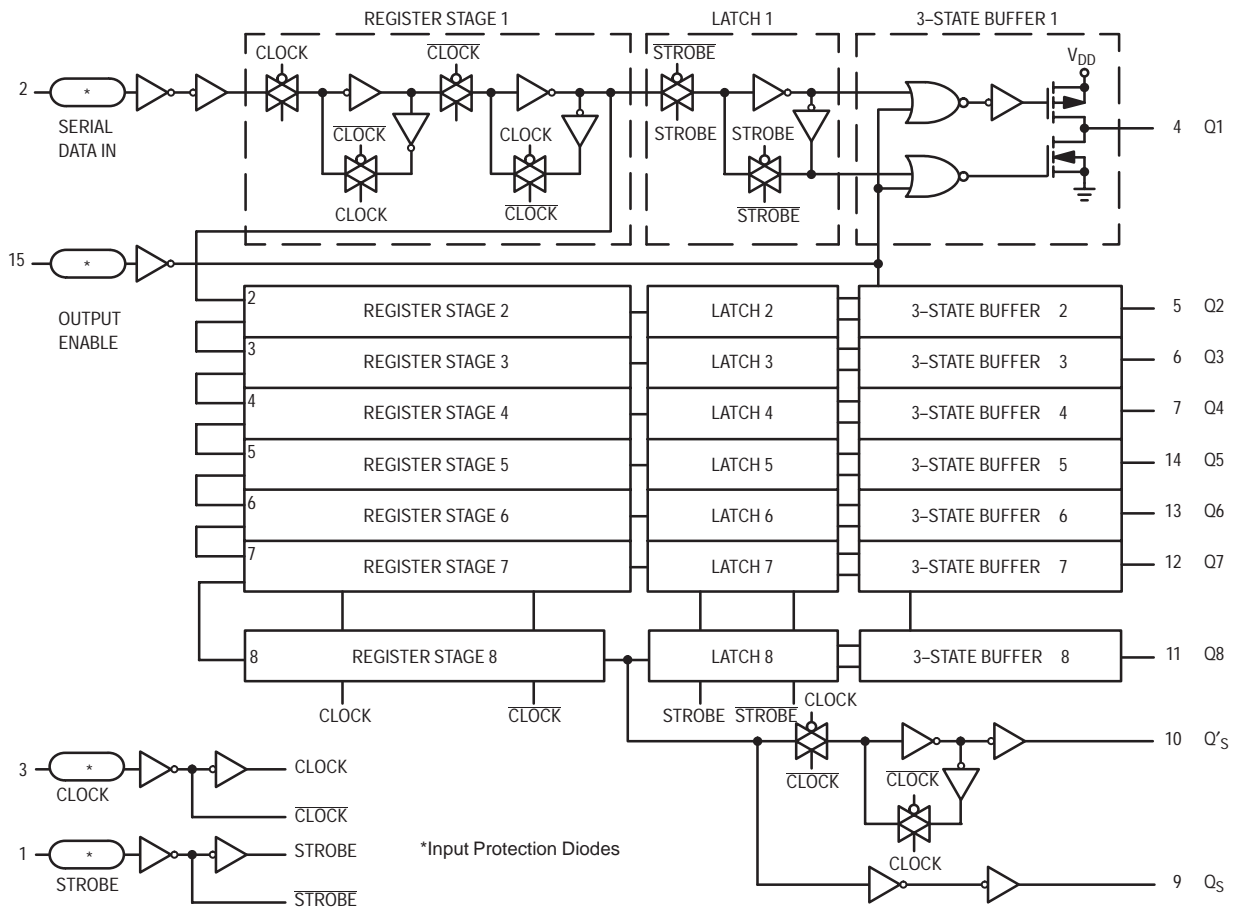


# MC14094B

## 3-STATE TEST CIRCUIT

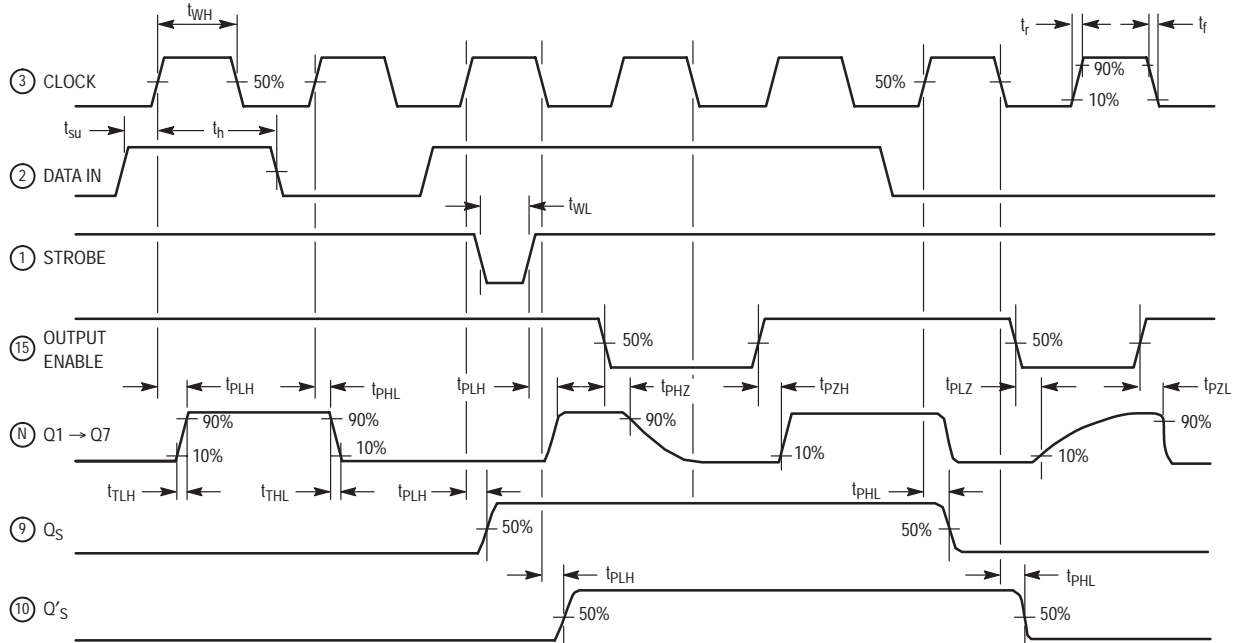


## BLOCK DIAGRAM



# MC14094B

## DYNAMIC TIMING DIAGRAM



# MC14099B

## 8-Bit Addressable Latches

The MC14099B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

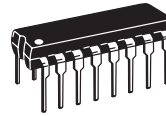
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



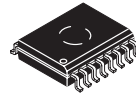
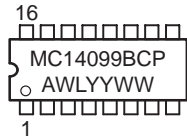
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<http://onsemi.com>

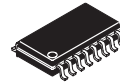
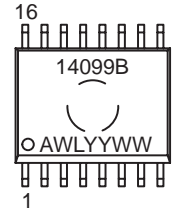
### MARKING DIAGRAMS



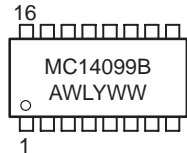
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
DW SUFFIX  
CASE 751G



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

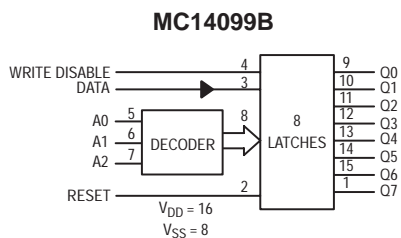
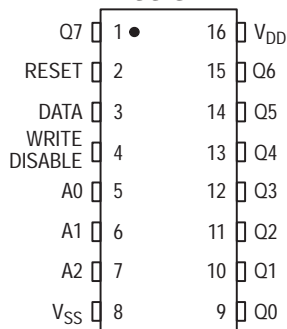
Device	Package	Shipping
MC14099BCP	PDIP-16	2000/Box
MC14099BDW	SOIC-16	2350/Box
MC14099BDWR2	SOIC-16	1000/Tape & Reel
MC14099BF	SOEIAJ-16	See Note 1.
MC14099BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.



# MC14099B

## PIN ASSIGNMENT



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Input Capacitance MC14599B — Data (pin 3) (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	15	22.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.5 μA/kHz) f + I <sub>DD</sub>							μAdc
10	I <sub>T</sub> = (3.0 μA/kHz) f + I <sub>DD</sub>									
15	I <sub>T</sub> = (4.5 μA/kHz) f + I <sub>DD</sub>									

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14099B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

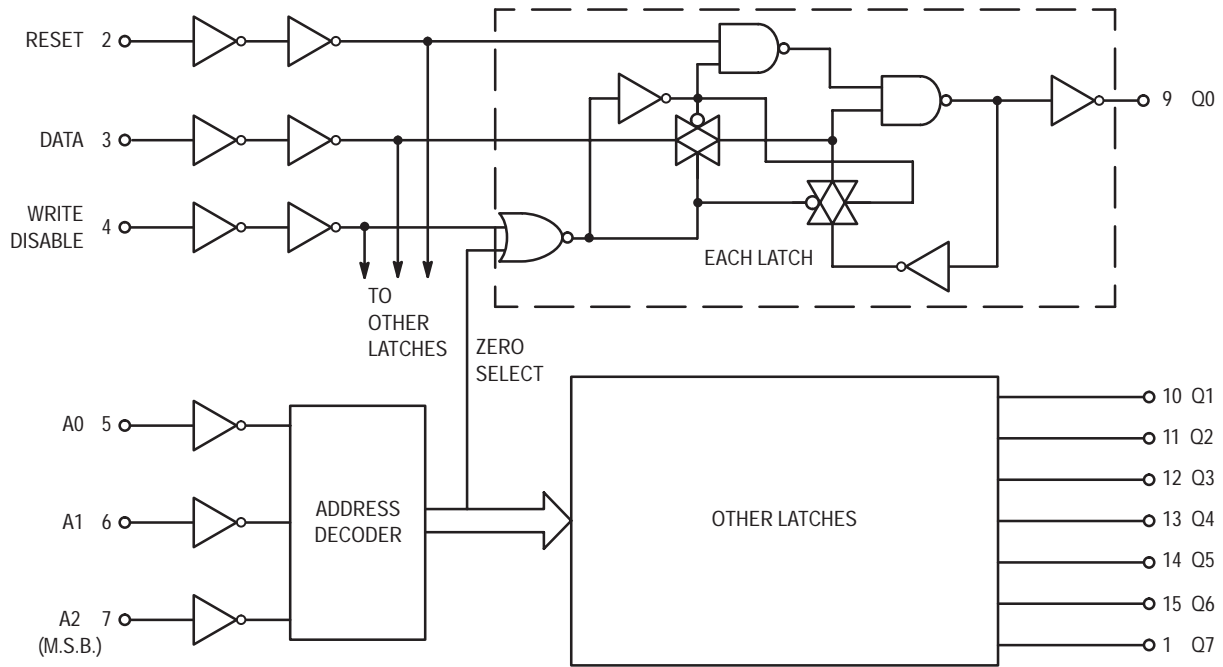
Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Data to Output Q	$t_{PHL},$ $t_{PLH}$	5.0 10 15	— — —	200 75 50	400 150 100	ns
Write Disable to Output Q		5.0 10 15	— — —	200 80 60	400 160 120	ns
Reset to Output Q		5.0 10 15	— — —	175 80 65	350 160 130	ns
CE to Output Q (MC14599B only)		5.0 10 15	— — —	225 100 75	450 200 150	ns
Propagation Delay Time, MC14599B only Chip Enable, Write/Read to Data	$t_{PHL},$ $t_{PLH}$	5.0 10 15	— — —	200 80 65	400 160 130	ns
Address to Data		5.0 10 15	— — —	200 90 75	400 180 150	ns
Pulse Widths Reset	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	150 75 50	75 40 25	— — —	ns
Write Disable		5.0 10 15	320 160 120	160 80 60	— — —	ns
Set Up Time Data to Write Disable	$t_{su}$	5.0 10 15	100 50 35	50 25 20	— — —	ns
Hold Time Write Disable to Data	$t_h$	5.0 10 15	150 75 50	75 40 25	— — —	ns
Set Up Time Address to Write Disable	$t_{su}$	5.0 10 15	100 80 40	45 30 10	— — —	ns
Removal Time Write Disable to Address	$t_{rem}$	5.0 10 15	0 0 0	- 80 - 40 - 40	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14099B

## MC14099B FUNCTION DIAGRAM



### TRUTH TABLE

Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	$Q_n^*$
0	1	Data	Reset †
1	0	$Q_n^*$	$Q_n^*$
1	1	Reset	Reset

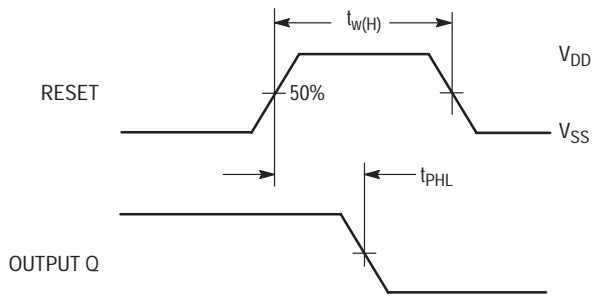
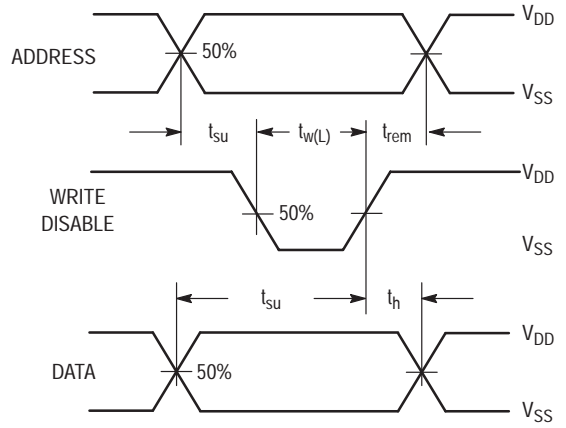
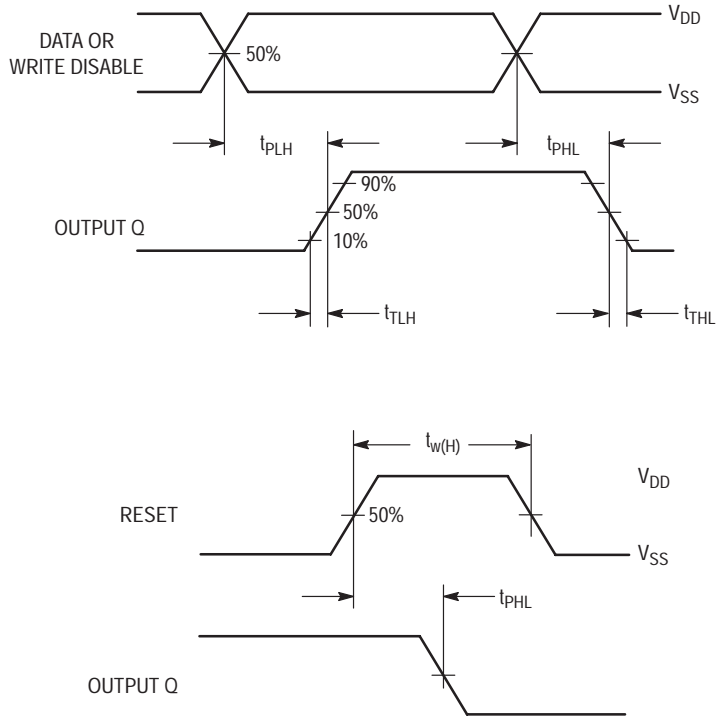
\* $Q_n$  is previous state of latch.

†Reset to zero state.

**CAUTION:** To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

# MC14099B

## SWITCHING WAVEFORMS



# MC14106B

## Hex Schmitt Trigger

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to “square up” slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

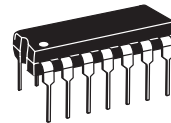
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



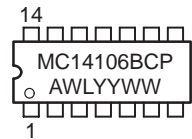
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<http://onsemi.com>

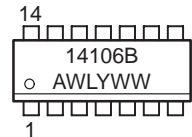
### MARKING DIAGRAMS



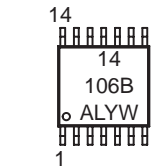
PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



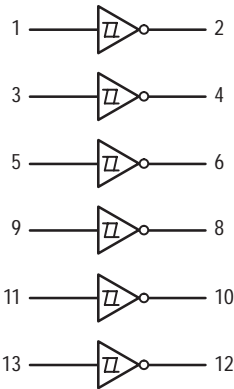
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14106BCP	PDIP-14	2000/Box
MC14106BD	SOIC-14	55/Rail
MC14106BDR2	SOIC-14	2500/Tape & Reel
MC14106BDT	TSSOP-14	96/Rail
MC14106BDTR2	TSSOP-14	2500/Tape & Reel

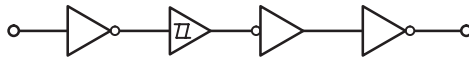
# MC14106B

## LOGIC DIAGRAM



$V_{DD}$  = PIN 14  
 $V_{SS}$  = PIN 7

## EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



# MC14106B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$  $V_{in} = 0$	"0" Level $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Hysteresis Voltage	$V_H^{(6.)}$	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
		10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
		15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive-Going  Negative-Going	$V_{T+}$	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
		10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
	$V_{T-}$	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	
		10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Source $I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu$ Adc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (1.8 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.6 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (5.4 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

6.  $V_H = V_{T+} - V_{T-}$  (But maximum variation of  $V_H$  is specified as less than  $V_{T+ \text{ max}} - V_{T- \text{ min}}$ ).

# MC14106B

## SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (7.)	Max	Unit
Output Rise Time	$t_{TLH}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	$t_{THL}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	$t_{PLH}$ , $t_{PHL}$	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

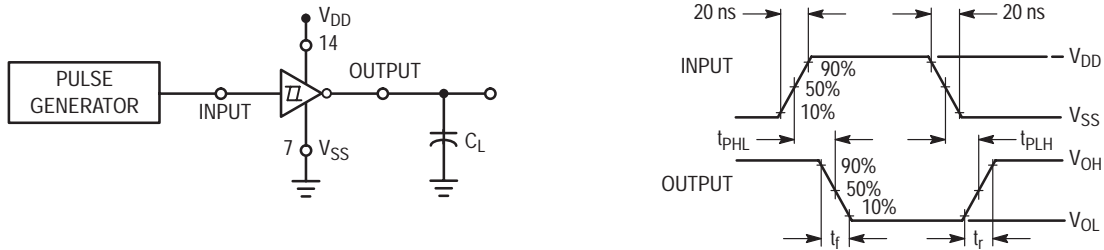


Figure 1. Switching Time Test Circuit and Waveforms

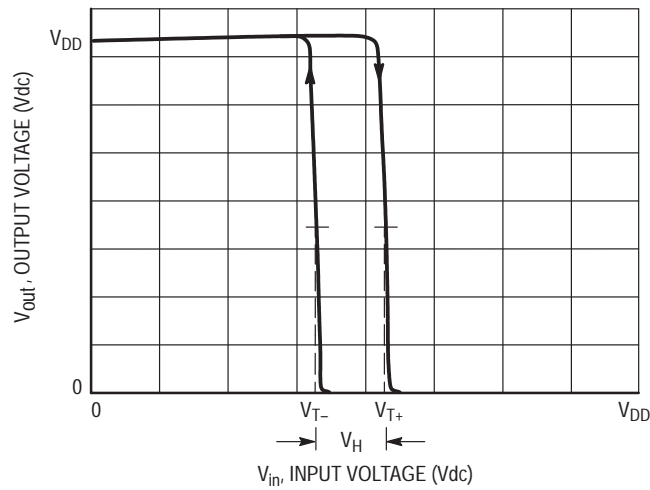


Figure 2. Typical Transfer Characteristics



# MC14106B

## APPLICATIONS

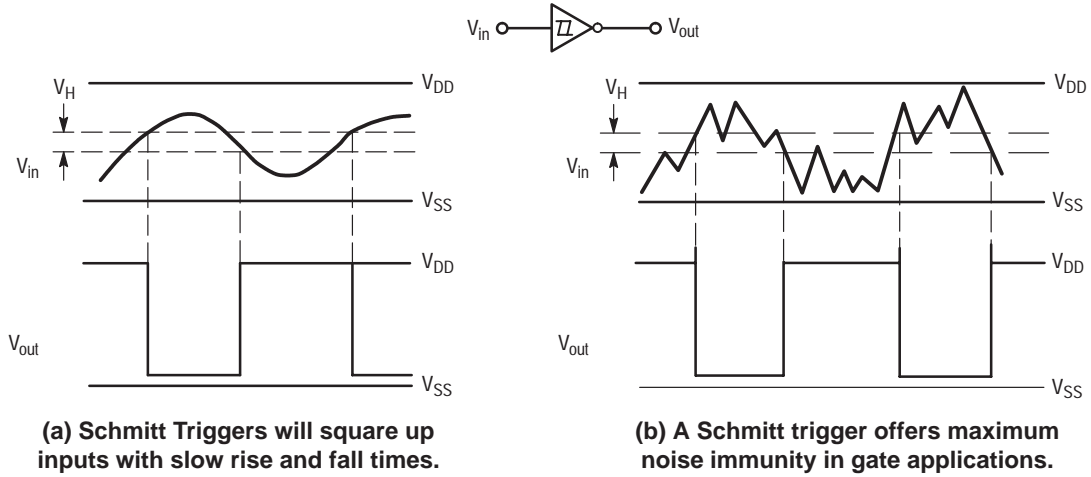
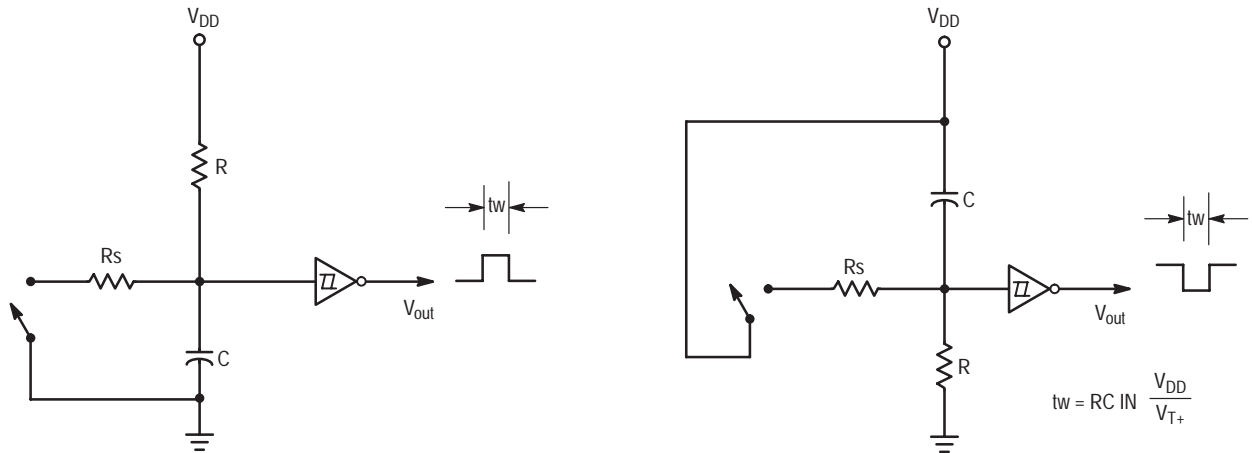


Figure 3.



Useful as Pushbutton/Keyboard Debounce Circuit.

Figure 4. Monostable Multivibrator

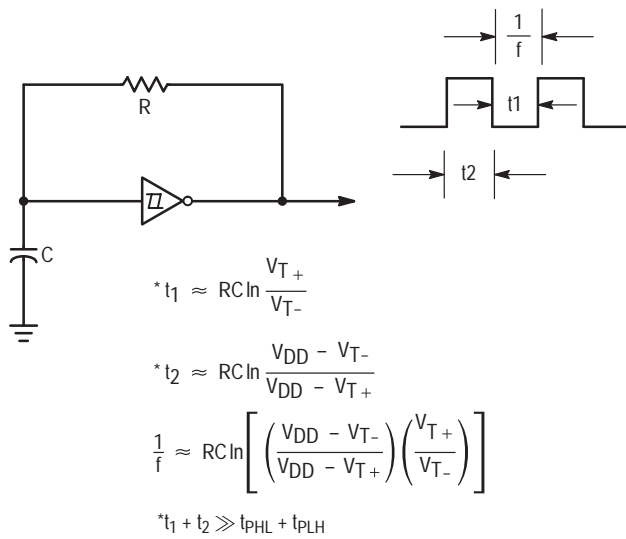


Figure 5. Astable Multivibrator

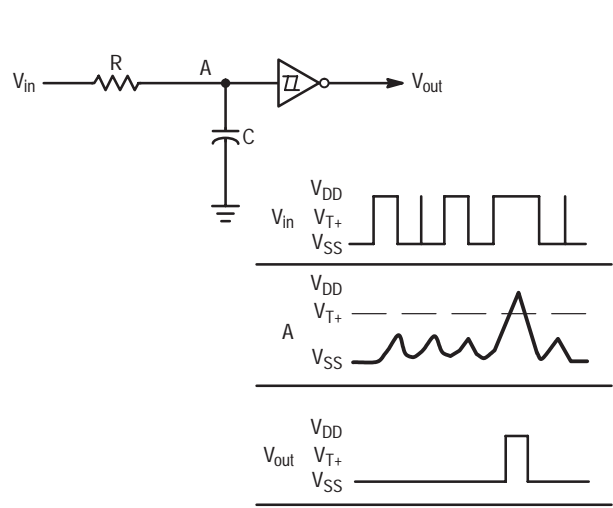


Figure 6. Integrator

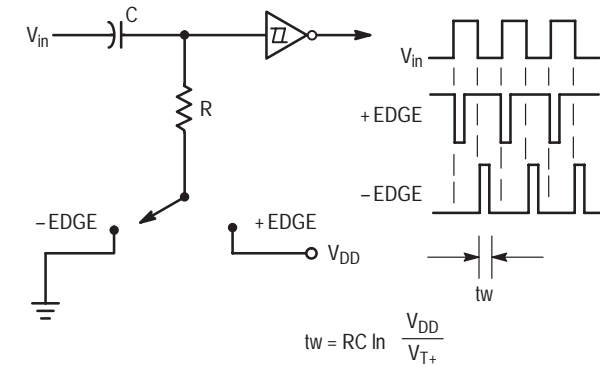


Figure 7. Differentiator

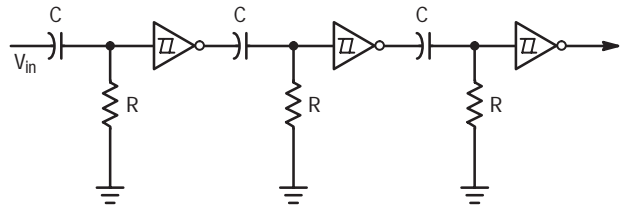


Figure 8. Positive Edge Time Delay Circuit

# MC14174B

## Hex Type D Flip-Flop

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

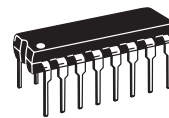
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



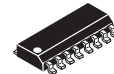
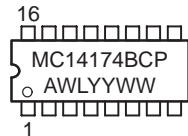
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<http://onsemi.com>

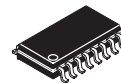
### MARKING DIAGRAMS



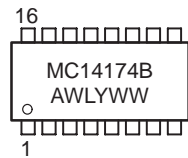
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

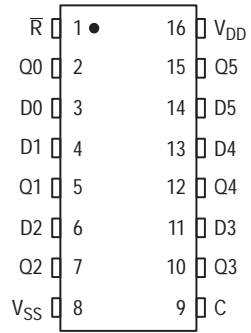
### ORDERING INFORMATION

Device	Package	Shipping
MC14174BCP	PDIP-16	2000/Box
MC14174BD	SOIC-16	48/Rail
MC14174BDR2	SOIC-16	2500/Tape & Reel
MC14174BF	SOEIAJ-16	See Note 1.
MC14174BFEL	SOEIAJ-16	See Note 1.

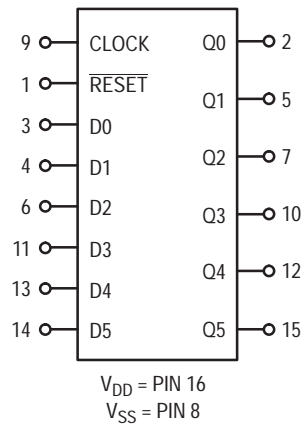
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14174B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## TRUTH TABLE (Positive Logic)

Inputs			Output
Clock	Data	Reset	Q
	0	1	0
	1	1	1
	X	1	Q
X	X	0	0

No Change

X = Don't Care

# MC14174B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.1 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.3 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.7 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.003.

# MC14174B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

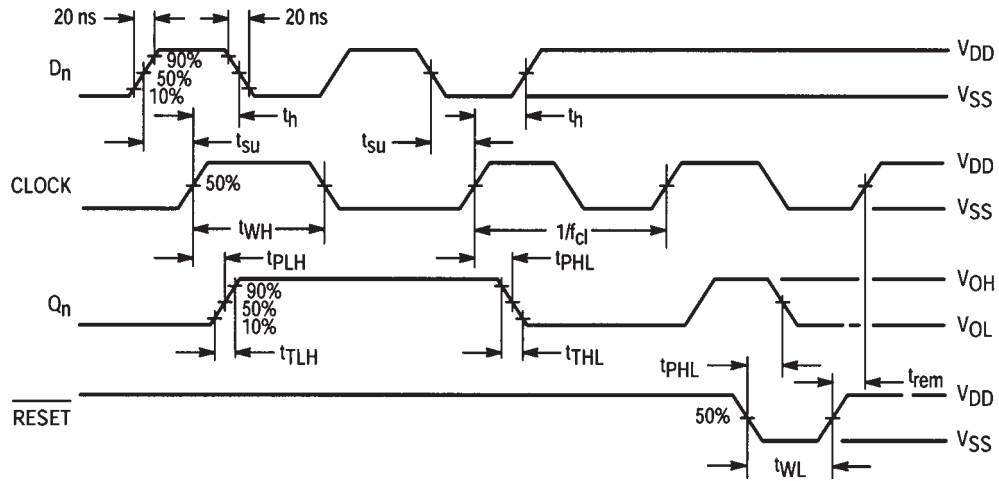
Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — Clock to Q $t_{PLH}$ , $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 64 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 52 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	210 85 65	400 160 120	ns
Propagation Delay Time — Reset to Q $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 79 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	250 100 75	500 200 150	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	150 90 70	75 45 35	— — —	ns
Reset Pulse Width	$t_{WL}$	5.0 10 15	200 100 80	100 50 40	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	7.0 12 15.5	2.0 5.0 6.5	mHz
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Data Setup Time	$t_{su}$	5.0 10 15	40 20 15	20 10 0	— — —	ns
Data Hold Time	$t_h$	5.0 10 15	80 40 30	40 20 15	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	250 100 80	125 50 40	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

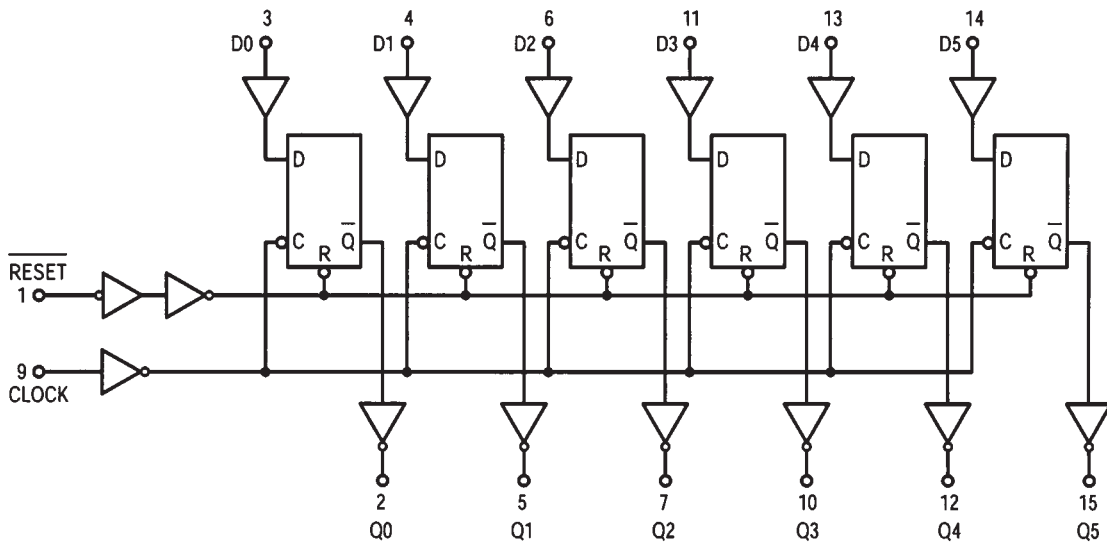
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14174B

## TIMING DIAGRAM



## FUNCTIONAL BLOCK DIAGRAM



# MC14175B

## Quad Type D Flip-Flop

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input (R) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and  $\bar{Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

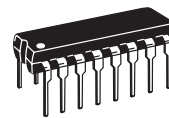
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



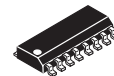
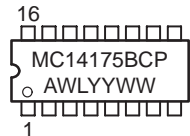
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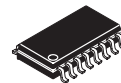
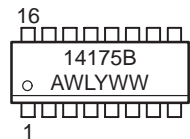
### MARKING DIAGRAMS



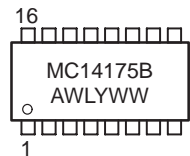
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

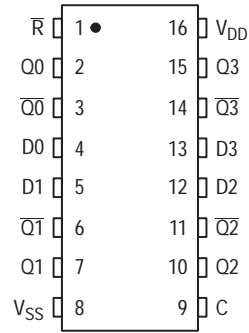
Device	Package	Shipping
MC14175BCP	PDIP-16	2000/Box
MC14175BD	SOIC-16	48/Rail
MC14175BDR2	SOIC-16	2500/Tape & Reel
MC14175BF	SOEIAJ-16	See Note 1.
MC14175BFEL	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

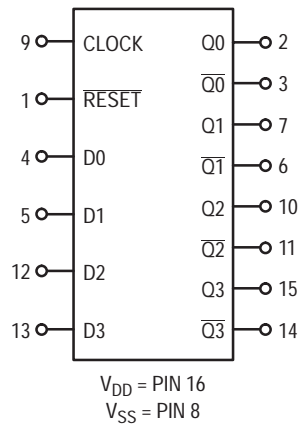


# MC14175B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## TRUTH TABLE

Inputs			Outputs	
Clock	Data	Reset	Q	Q
	0	1	0	1
	1	1	1	0
	X	1	Q	Q
X	X	0	0	1

No Change

X = Don't Care

# MC14175B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.7 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.4 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.0 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14175B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

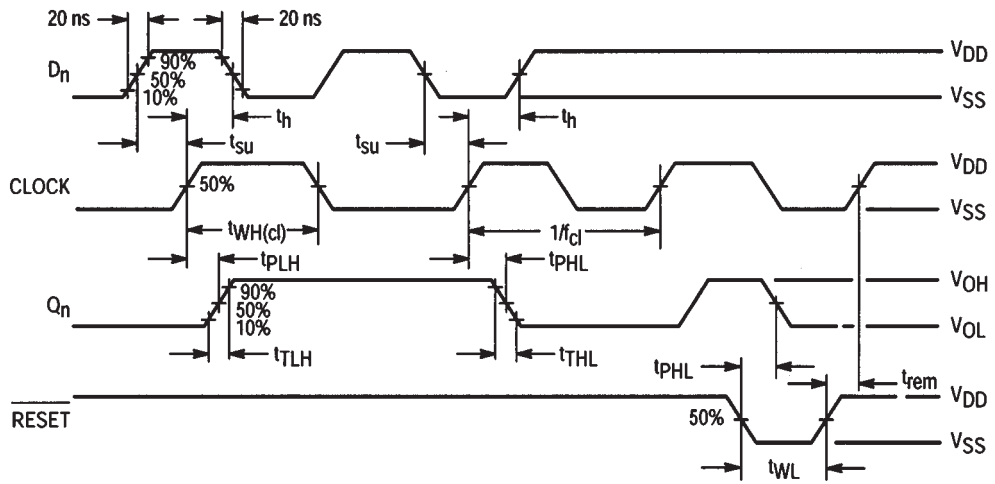
Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — Clock to Q, Q $t_{PLH}$ , $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 175 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 72 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	220 90 70	400 160 120	ns
Propagation Delay Time — Reset to Q, Q $t_{PHL} = (0.9 \text{ ns/pF}) C_L + 280 \text{ ns}$ $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 112 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$	$t_{PHL}$ , $t_{PLH}$	5.0 10 15	— — —	325 130 100	500 200 150	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	250 100 75	110 45 35	— — —	ns
Reset Pulse Width	$t_{WL}$	5.0 10 15	200 80 60	100 40 30	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	4.5 11 14	2.0 5.0 6.5	mHz
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Data Setup Time	$t_{su}$	5.0 10 15	120 50 40	60 25 20	— — —	ns
Data Hold Time	$t_h$	5.0 10 15	80 40 30	40 20 15	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	250 100 80	125 50 40	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

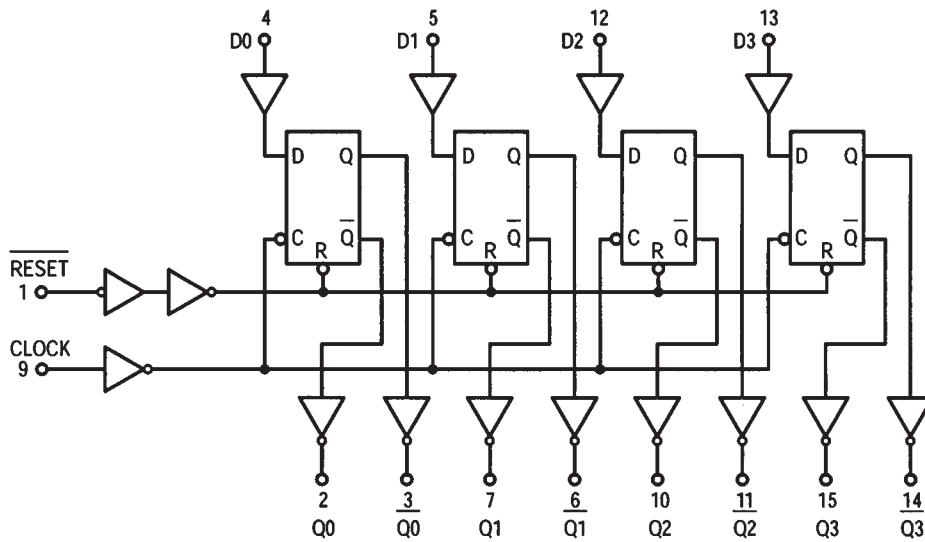
8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14175B

## TIMING DIAGRAM



## FUNCTIONAL BLOCK DIAGRAM



# MC14490

## Hex Contact Bounce Eliminator

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the “make” and the “break” of a contact closure. The clock for operation of the MC14490 is derived from an internal R–C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

NOTE: Immediately after power-up, the outputs of the MC14490 are in indeterminate states.

- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R–C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both “Make” and “Break” Contacts
- Does Not Require “Form C” (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	–0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	–0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	±10	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	–55 to +125	°C
$T_{stg}$	Storage Temperature Range	–65 to +150	°C
$T_L$	Lead Temperature (8–Second Soldering)	260	°C

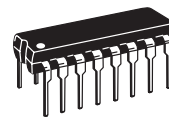
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C



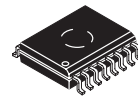
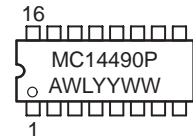
ON Semiconductor

<http://onsemi.com>

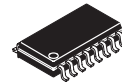
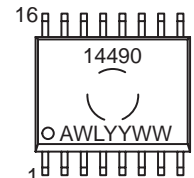
### MARKING DIAGRAMS



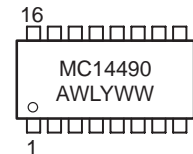
PDIP–16  
P SUFFIX  
CASE 648



SOIC–16  
DW SUFFIX  
CASE 751G



SOEIAJ–16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14490DW	SOIC–16	47/Rail
MC14490DWR2	SOIC–16	1000/Tape & Reel
MC14490F	SOEIAJ–16	See Note 1.
MC14490FEL	SOEIAJ–16	See Note 1.
MC14490P	PDIP–16	25/Rail

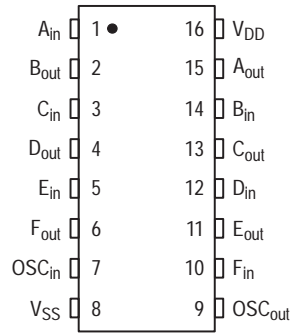
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

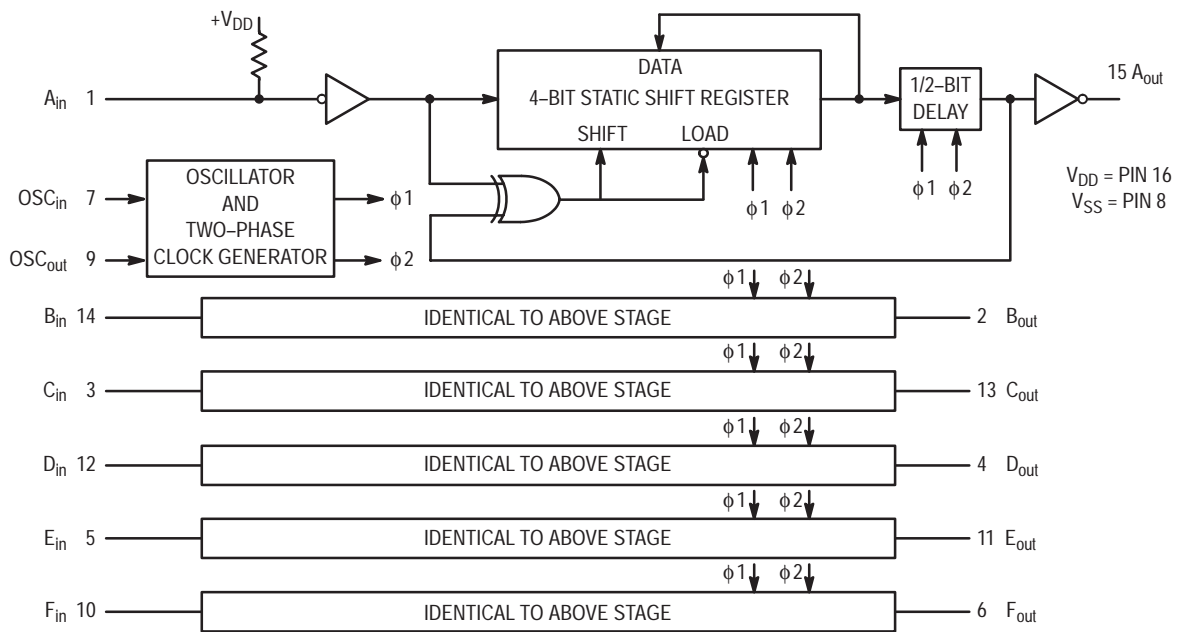
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# MC14490

## PIN ASSIGNMENT



## BLOCK DIAGRAM



# MC14490

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—		
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	"0" Level $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level" $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—		
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current Oscillator Output ( $V_{OH} = 2.5$ V) ( $V_{OH} = 4.6$ V) ( $V_{OH} = 9.5$ V) ( $V_{OH} = 13.5$ V)  Debounce Outputs ( $V_{OH} = 2.5$ V) ( $V_{OH} = 4.6$ V) ( $V_{OH} = 9.5$ V) ( $V_{OH} = 13.5$ V)  Oscillator Output ( $V_{OL} = 0.4$ V) ( $V_{OL} = 0.5$ V) ( $V_{OL} = 1.5$ V)  Debounce Outputs ( $V_{OL} = 0.4$ V) ( $V_{OL} = 0.5$ V) ( $V_{OL} = 1.5$ V)	Source $I_{OH}$	5.0	-0.6	—	-0.5	-1.5	—	-0.4	—	mAdc	
		5.0	-0.12	—	-0.1	-0.3	—	-0.08	—		
		10	-0.23	—	-0.2	-0.8	—	-0.16	—		
		15	-1.4	—	-1.2	-3.0	—	-1.0	—		
		5.0	-0.9	—	-0.75	-2.2	—	-0.6	—		
		5.0	-0.19	—	-0.16	-0.46	—	-0.12	—		
	10	-0.6	—	-0.5	-1.2	—	-0.4	—			
	15	1.8	—	-1.5	-4.5	—	-1.2	—			
	Sink $I_{OL}$	5.0	0.36	—	0.3	0.9	—	0.24	—		mAdc
		10	0.9	—	0.75	2.3	—	0.6	—		
		15	4.2	—	3.5	10	—	2.8	—		
		5.0	2.6	—	2.2	4.0	—	1.8	—		
10		4.0	—	3.3	9.0	—	2.7	—			
15		12	—	10	35	—	8.1	—			
Input Current Debounce Inputs ( $V_{in} = V_{DD}$ )	$I_{IH}$	15	—	2.0	—	0.2	2.0	—	11	$\mu$ Adc	
Input Current Oscillator — Pin 7 ( $V_{in} = V_{SS}$ or $V_{DD}$ )	$I_{in}$	15	—	$\pm 620$	—	$\pm 255$	$\pm 400$	—	$\pm 250$	$\mu$ Adc	
Pullup Resistor Source Current Debounce Inputs ( $V_{in} = V_{SS}$ )	$I_{IL}$	5.0	175	375	140	190	255	70	225	$\mu$ Adc	
		10	340	740	280	380	500	145	440		
		15	505	1100	415	570	750	215	660		
Input Capacitance	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current ( $V_{in} = V_{SS}$ or $V_{DD}$ , $I_{out} = 0$ $\mu$ A)	$I_{SS}$	5.0	—	150	—	40	100	—	90	$\mu$ Adc	
		10	—	280	—	90	225	—	180		
		15	—	840	—	225	650	—	550		

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14490

## SWITCHING CHARACTERISTICS (5.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (6.)	Max	Unit
Output Rise Time All Outputs	$t_{TLH}$	5.0	—	180	360	ns
		10	—	90	180	
		15	—	65	130	
Output Fall Time Oscillator Output	$t_{THL}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
	$t_{THL}$	5.0	—	60	120	
		10	—	30	60	
		15	—	20	40	
Propagation Delay Time Oscillator Input to Debounce Outputs	$t_{PHL}$	5.0	—	285	570	ns
		10	—	120	240	
		15	—	95	190	
	$t_{PLH}$	5.0	—	370	740	
		10	—	160	320	
		15	—	120	240	
Clock Frequency (50% Duty Cycle) (External Clock)	$f_{cl}$	5.0	—	2.8	1.4	MHz
		10	—	6	3.0	
		15	—	9	4.5	
Setup Time (See Figure 1)	$t_{su}$	5.0	100	50	—	ns
		10	80	40	—	
		15	60	30	—	
Maximum External Clock Input Rise and Fall Time Oscillator Input	$t_r, t_f$	5.0	No Limit			ns
		10				
		15				
Oscillator Frequency $OSC_{out}$ $C_{ext} \geq 100 \text{ pF}^*$  Note: These equations are intended to be a design guide. Laboratory experimentation may be required. Formulas are typically $\pm 15\%$ of actual frequencies.	$f_{osc, typ}$	5.0				Hz
		10				
		15				

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

### \*POWER-DOWN CONSIDERATIONS

Large values of  $C_{ext}$  may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA, therefore the turn-off time of the power supply must not be faster than  $t = (V_{DD} - V_{SS}) \cdot C_{ext} / (10 \text{ mA})$ . For example, If  $V_{DD} - V_{SS} = 15 \text{ V}$  and  $C_{ext} = 1 \mu\text{F}$ , the power supply must turn off no faster than  $t = (15 \text{ V}) \cdot (1 \mu\text{F}) / 10 \text{ mA} = 1.5 \text{ ms}$ . This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

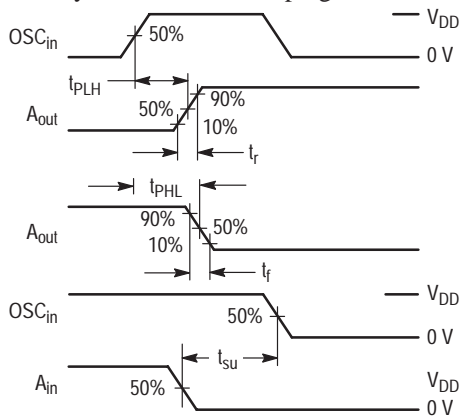


Figure 1. Switching Waveforms

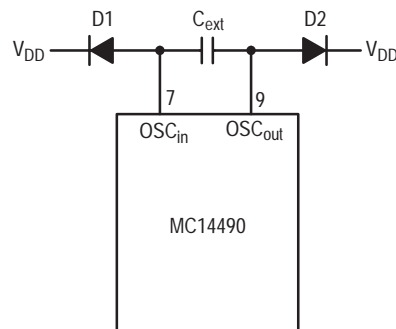


Figure 2. Discharge Protection During Power Down



## THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4-1/2-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is closed, (see Figure 4) the low level is inverted, and the shift register is loaded with a high on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3-1/2 to 4-1/2 clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+1 a low is loaded into the first bit. Just after N+1, when the input bounces low, all bits are set to a high. At N+2 nothing happens because the input and output are low and all bits of the shift register are high. At time N+3 and thereafter the input signal is a high, clean signal. At the positive edge of N+6 the output goes high as a result of four lows being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

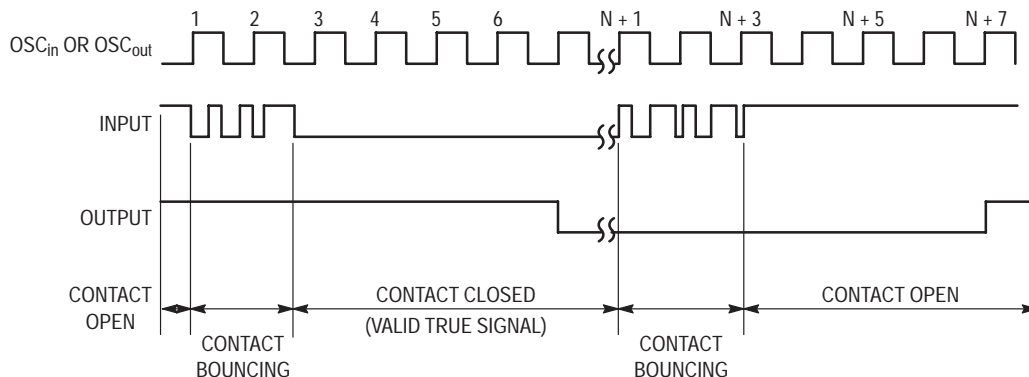


Figure 3. Timing Diagram

## MC14490

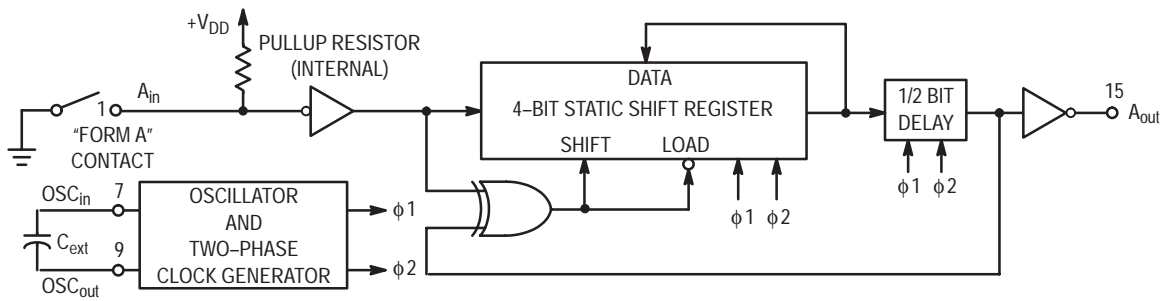


Figure 4. Typical "Form A" Contact Debounce Circuit (Only One Debouncer Shown)

## OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built-in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between  $V_{DD}$  and the input.

Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when  $V_{DD}$  is below 5 V. At this voltage, the input should be driven with

paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When  $V_{DD}$  is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

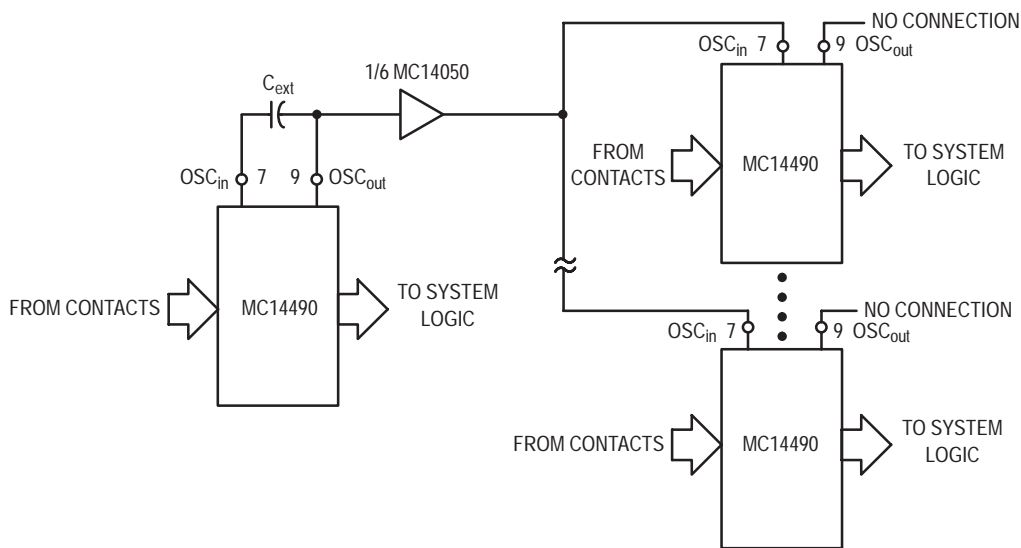


Figure 5. Typical Single Oscillator Debounce System

TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

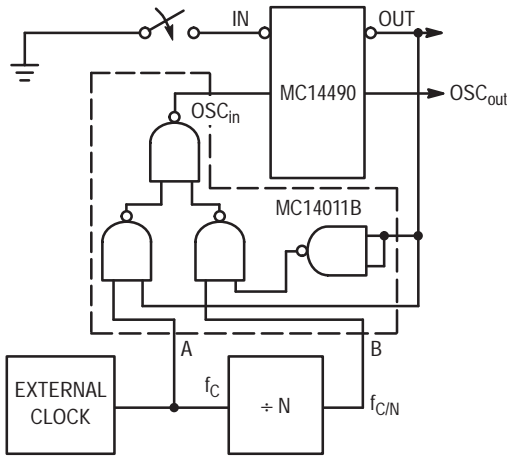


Figure 6. Fast Attack/Slow Release Circuit

LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

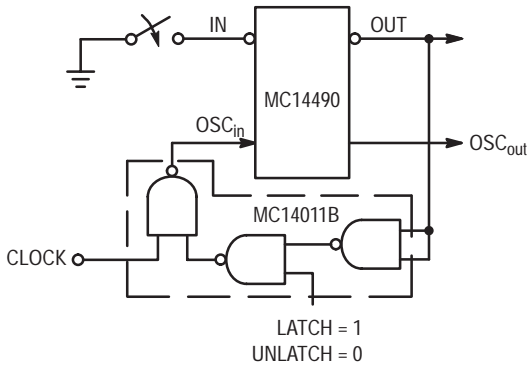


Figure 7. Latched Output Circuit

MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal  $\overline{AB}$  as shown in Figures 9 and 10. The signal  $\overline{AB}$  is four clock periods in length. If the inverter is switched to the A output, the pulse  $\overline{AB}$  will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

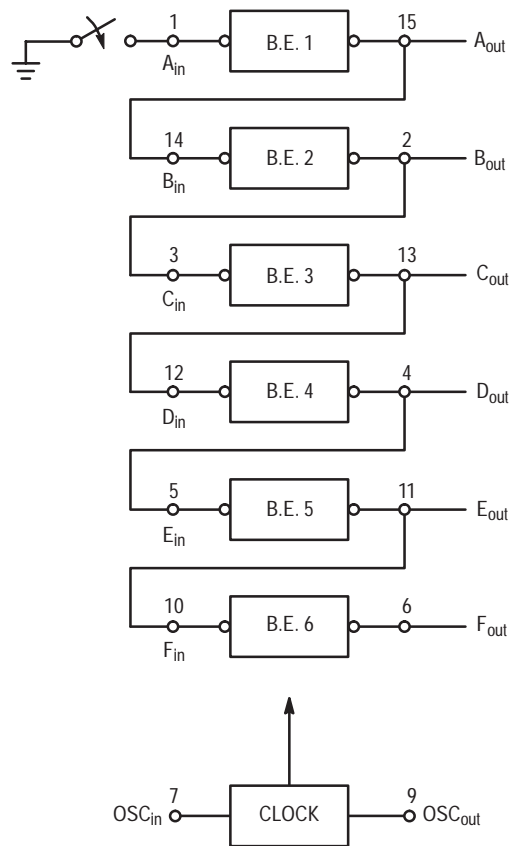


Figure 8. Multiple Timing Circuit Connections

# MC14490

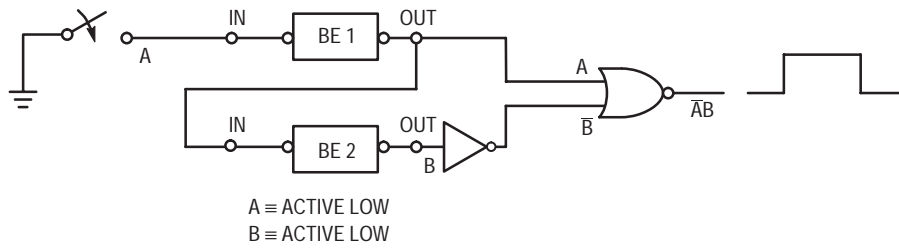


Figure 9. Single Pulse Output Circuit

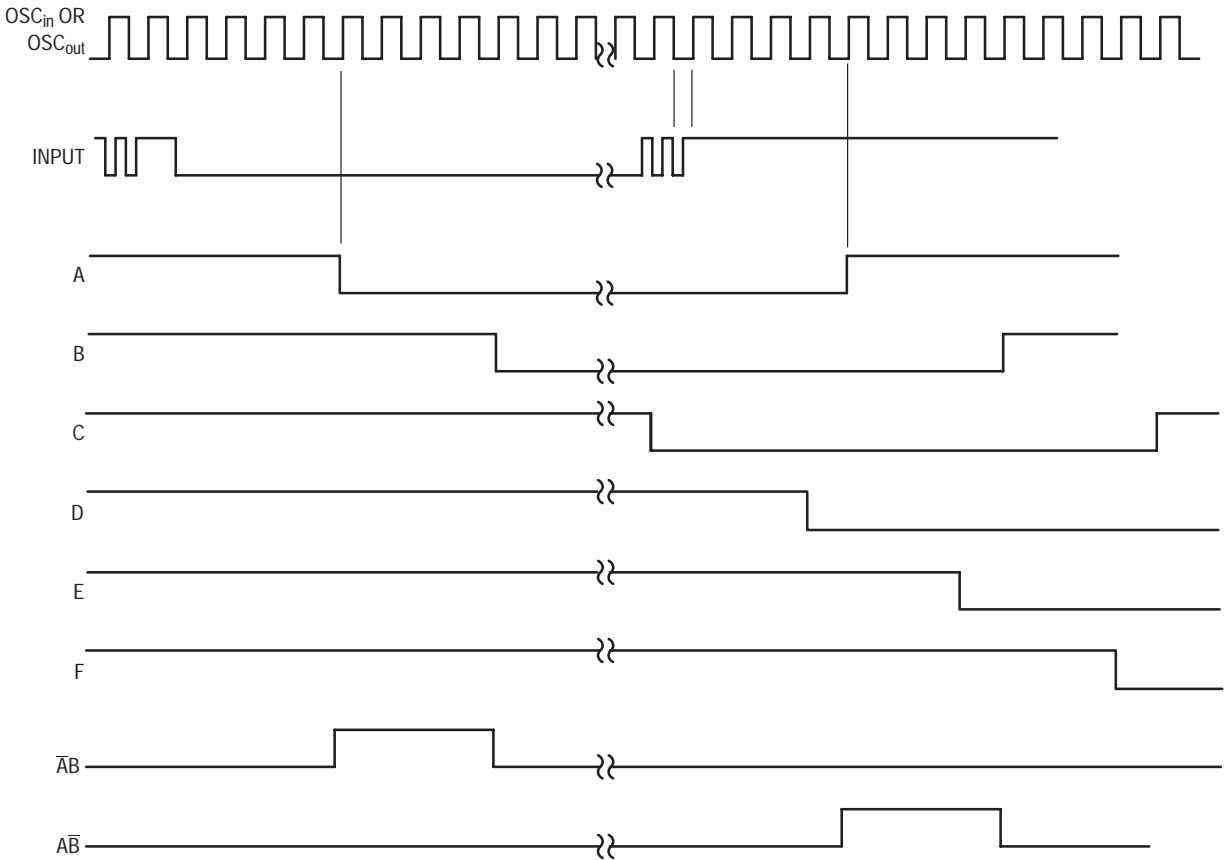


Figure 10. Multiple Output Signal Timing Diagram

# MC14503B

## Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

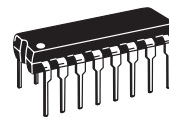
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



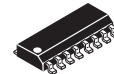
ON Semiconductor

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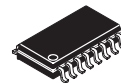
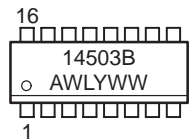
### MARKING DIAGRAMS



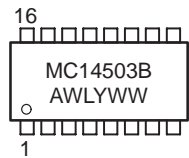
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

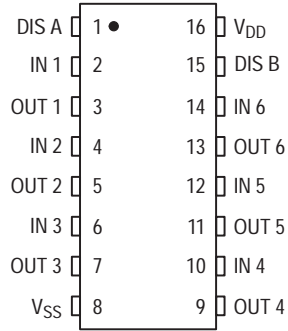
### ORDERING INFORMATION

Device	Package	Shipping
MC14503BCP	PDIP-16	2000/Box
MC14503BD	SOIC-16	48/Rail
MC14503BDR2	SOIC-16	2500/Tape & Reel
MC14503BF	SOEIAJ-16	See Note 1.
MC14503BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14503B

## PIN ASSIGNMENT

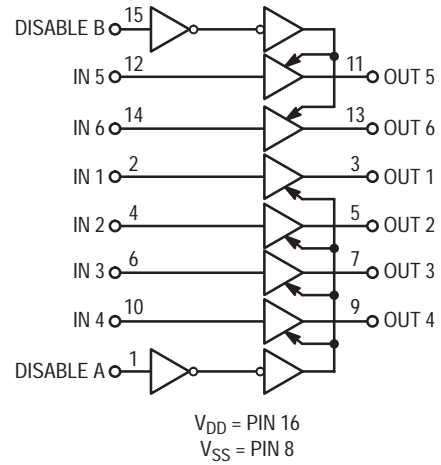


## TRUTH TABLE

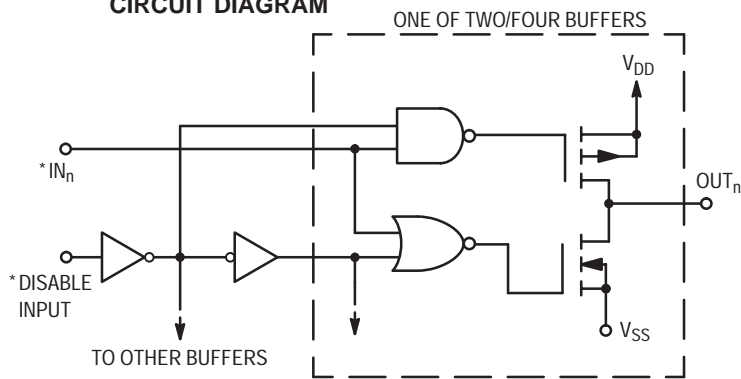
$In_n$	Appropriate Disable Input	$Out_n$
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

## LOGIC DIAGRAM



## CIRCUIT DIAGRAM



\*Diode protection on all inputs (not shown)

# MC14503B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = 0  V <sub>in</sub> = V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 3.6 or 1.4 Vdc) (V <sub>O</sub> = 7.2 or 2.8 Vdc) (V <sub>O</sub> = 11.5 or 3.5 Vdc)  (V <sub>O</sub> = 1.4 or 3.6 Vdc) (V <sub>O</sub> = 2.8 or 7.2 Vdc) (V <sub>O</sub> = 3.5 or 11.5 Vdc)	“0” Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	4.5	-4.3	—	-3.6	-5.0	—	-2.5	—	mAdc
		5.0	-5.8	—	-4.8	-6.1	—	-3.0	—	
		5.0	-1.2	—	-1.02	-1.4	—	-0.7	—	
		10	-3.1	—	-2.6	-3.7	—	-1.8	—	
		15	-8.2	—	-6.8	-14.1	—	-4.8	—	
	Sink I <sub>OL</sub>	4.5	2.2	—	1.8	2.1	—	1.2	—	
5.0	2.6	—	2.1	2.3	—	1.3	—			
10	6.5	—	5.5	6.2	—	3.8	—			
15	19.2	—	16.1	25	—	11.2	—			
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>Q</sub>	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)	I <sub>T</sub>	5.0	I <sub>T</sub> = (2.5 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (6.0 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (10 μA/kHz) f + I <sub>DD</sub>							
Three-State Output Leakage Current	I <sub>TL</sub>	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μAdc

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.006.

# MC14503B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ $V_{CC}$	All Types		Unit
			Typ (8.)	Max	
Output Rise Time $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	$t_{TLH}$	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time $t_{THL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{THL} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	$t_{THL}$	5.0 10 15	45 23 18	90 45 35	ns
Turn-Off Delay Time, all Outputs $t_{PLH} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PLH} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{PLH}$	5.0 10 15	75 35 25	150 70 50	ns
Turn-On Delay Time, all Outputs $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{PHL}$	5.0 10 15	75 35 25	150 70 50	ns
3-State Propagation Delay Time Output "1" to High Impedance	$t_{PHZ}$	5.0 10 15	75 40 35	150 80 70	ns
Output "0" to High Impedance	$t_{PLZ}$	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to "1" Level	$t_{PZH}$	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to "0" Level	$t_{PZL}$	5.0 10 15	100 35 25	200 70 50	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

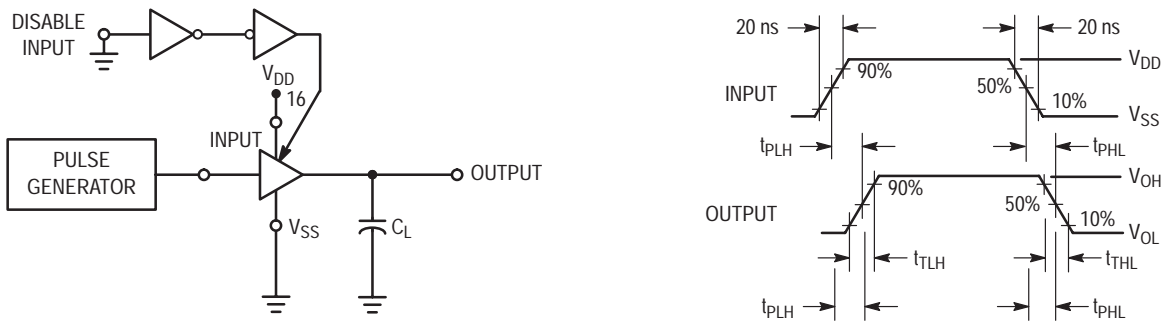
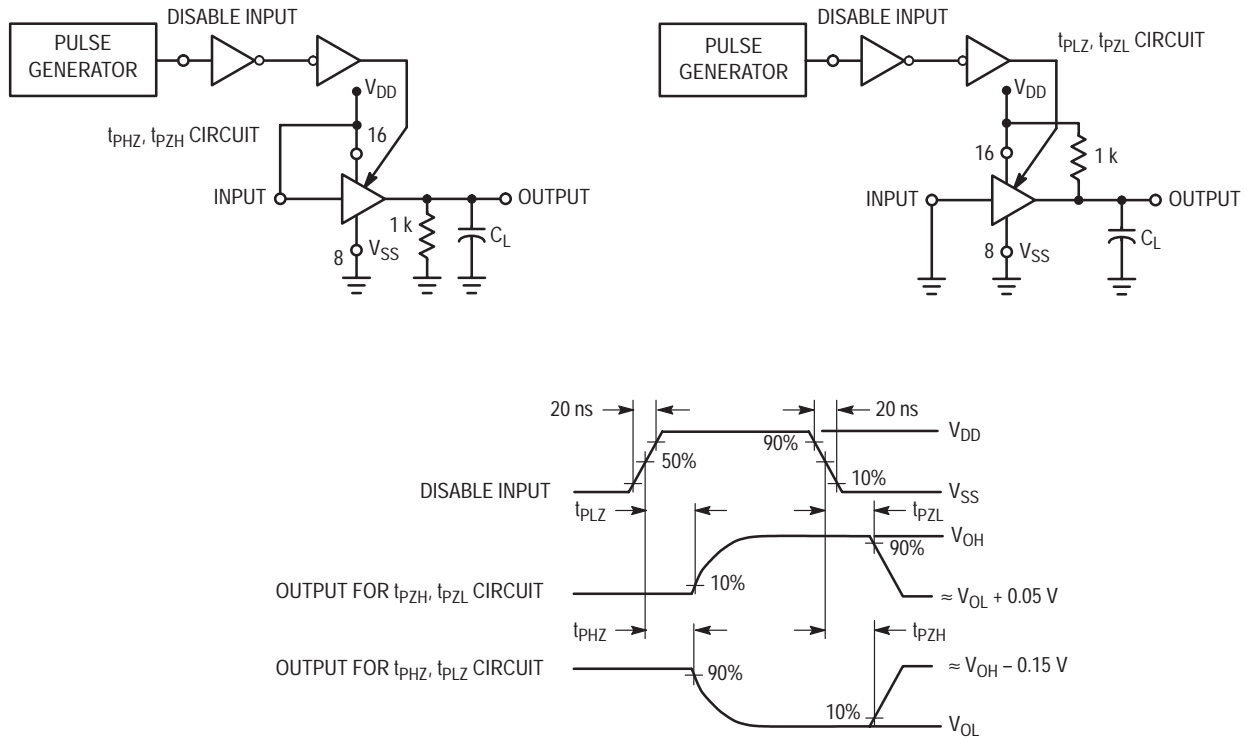


Figure 1. Switching Time Test Circuit and Waveforms ( $t_{TLH}$ ,  $t_{THL}$ ,  $t_{PHL}$ , and  $t_{PLH}$ )



# MC14503B



**Figure 2.3—State AC Test Circuit and Waveforms (t<sub>PLZ</sub>, t<sub>PHZ</sub>, t<sub>PZH</sub>, t<sub>PZL</sub>)**

# MC14504B

## Hex Level Shifter for TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels  $V_{DD}$  and  $V_{CC}$ . The  $V_{CC}$  level sets the input signal levels while  $V_{DD}$  selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for  $V_{DD}$  and  $V_{CC}$
- Diode Protected Inputs to  $V_{SS}$
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

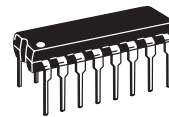
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



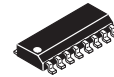
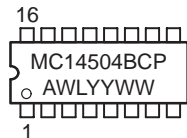
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<http://onsemi.com>

### MARKING DIAGRAMS



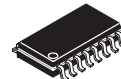
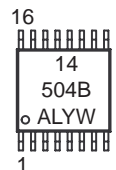
PDIP-16  
P SUFFIX  
CASE 648



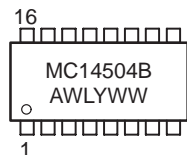
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

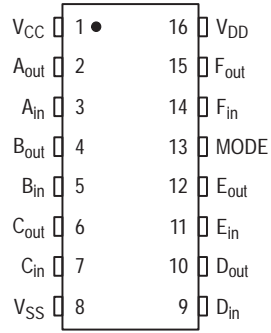
### ORDERING INFORMATION

Device	Package	Shipping
MC14504BCP	PDIP-16	2000/Box
MC14504BD	SOIC-16	48/Rail
MC14504BDR2	SOIC-16	2500/Tape & Reel
MC14504BDT	TSSOP-16	96/Rail
MC14504BF	SOEIAJ-16	See Note 1.
MC14504BFEL	SOEIAJ-16	See Note 1.

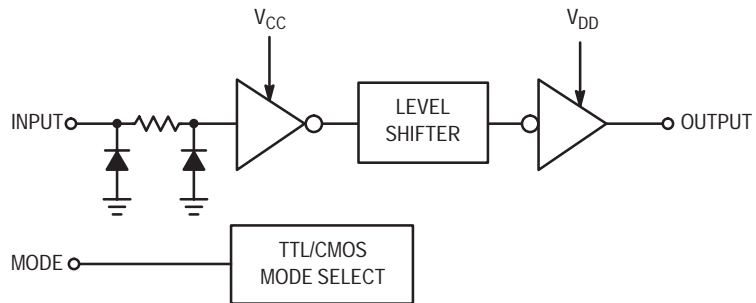
- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14504B

## PIN ASSIGNMENT



## LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 ( $V_{CC}$ )	TTL	CMOS
0 ( $V_{SS}$ )	CMOS	CMOS

1/6 of package shown.

# MC14504B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{CC}$ Vdc	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage $V_{in} = 0\text{ V}$  $V_{in} = V_{CC}$	"0" Level $V_{OL}$	—	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		—	10	—	0.05	—	0	0.05	—	0.05	
		—	15	—	0.05	—	0	0.05	—	0.05	
	"1" Level $V_{OH}$	—	5.0	4.95	—	4.95	5.0	—	4.95	—	
		—	10	9.95	—	9.95	10	—	9.95	—	
		—	15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level ( $V_{OL} = 1.0\text{ Vdc}$ ) TTL-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) TTL-CMOS ( $V_{OL} = 1.0\text{ Vdc}$ ) CMOS-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) CMOS-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) CMOS-CMOS	$V_{IL}$	5.0	10	—	0.8	—	1.3	0.8	—	0.8	Vdc
		5.0	15	—	0.8	—	1.3	0.8	—	0.8	
		5.0	10	—	1.5	—	2.25	1.5	—	1.4	
		5.0	15	—	1.5	—	2.25	1.5	—	1.5	
		10	15	—	3.0	—	4.5	3.0	—	2.9	
		10	15	—	3.0	—	4.5	3.0	—	2.9	
Input Voltage "1" Level ( $V_{OH} = 9.0\text{ Vdc}$ ) TTL-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) TTL-CMOS ( $V_{OH} = 9.0\text{ Vdc}$ ) CMOS-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) CMOS-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) CMOS-CMOS	$V_{IH}$	5.0	10	2.0	—	2.0	1.5	—	2.0	—	Vdc
		5.0	15	2.0	—	2.0	1.5	—	2.0	—	
		5.0	10	3.6	—	3.5	2.75	—	3.5	—	
		5.0	15	3.6	—	3.5	2.75	—	3.5	—	
		10	15	7.1	—	7.0	5.5	—	7.0	—	
		10	15	7.1	—	7.0	5.5	—	7.0	—	
Output Drive Current ( $V_{OH} = 2.5\text{ Vdc}$ ) ( $V_{OH} = 4.6\text{ Vdc}$ ) ( $V_{OH} = 9.5\text{ Vdc}$ ) ( $V_{OH} = 13.5\text{ Vdc}$ )  ( $V_{OL} = 0.4\text{ Vdc}$ ) ( $V_{OL} = 0.5\text{ Vdc}$ ) ( $V_{OL} = 1.5\text{ Vdc}$ )	Source $I_{OH}$	—	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		—	5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		—	10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		—	15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink $I_{OL}$	—	5.0	0.64	—	0.51	0.88	—	0.36	—	
		—	10	1.6	—	1.3	2.25	—	0.9	—	
—		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	—	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{Adc}$
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) CMOS-CMOS Mode	$I_{DD}$ or $I_{CC}$	—	5.0	—	0.05	—	0.0005	0.05	—	1.5	$\mu\text{Adc}$
		—	10	—	0.10	—	0.0010	0.10	—	3.0	
		—	15	—	0.20	—	0.0015	0.20	—	6.0	
Quiescent Current (Per Package) TTL-CMOS Mode	$I_{DD}$	5.0	5.0	—	0.5	—	0.0005	0.5	—	3.8	$\mu\text{Adc}$
		5.0	10	—	1.0	—	0.0010	1.0	—	7.5	
		5.0	15	—	2.0	—	0.0015	2.0	—	15	
Quiescent Current (Per Package) TTL-CMOS Mode	$I_{CC}$	5.0	5.0	—	5.0	—	2.5	5.0	—	6.0	mAdc
		5.0	10	—	5.0	—	2.5	5.0	—	6.0	
		5.0	15	—	5.0	—	2.5	5.0	—	6.0	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14504B

## SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	Shifting Mode	V <sub>CC</sub> Vdc	V <sub>DD</sub> Vdc	Limits			Unit
					Min	Typ <sup>(5)</sup>	Max	
Propagation Delay, High to Low	t <sub>PHL</sub>	TTL – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	—	140	280	ns
			5.0	15	—	140	280	
		CMOS – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	—	120	240	
			5.0	15	—	120	240	
			10	15	—	70	140	
		CMOS – CMOS V <sub>CC</sub> > V <sub>DD</sub>	10	5.0	—	185	370	
15	5.0		—	185	370			
15	10		—	175	350			
Propagation Delay, Low to High	t <sub>PLH</sub>	TTL – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	—	170	340	ns
			5.0	15	—	160	320	
		CMOS – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	—	170	340	
			5.0	15	—	170	340	
			10	15	—	100	200	
		CMOS – CMOS V <sub>CC</sub> > V <sub>DD</sub>	10	5.0	—	275	550	
15	5.0		—	275	550			
15	10		—	145	290			
Output Rise and Fall Time	t <sub>TLH</sub> , t <sub>TFL</sub>	ALL	—	5.0	—	100	200	ns
			—	10	—	50	100	
			—	15	—	40	80	

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

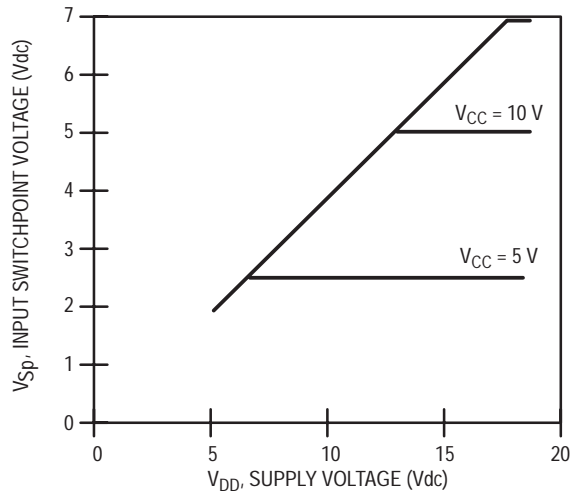


Figure 1. Input Switchpoint CMOS to CMOS Mode

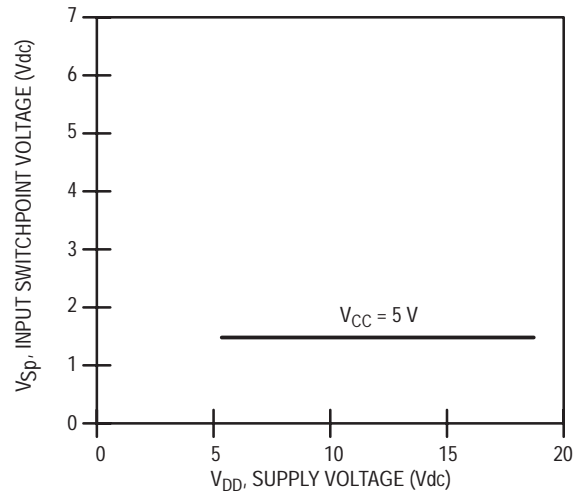


Figure 2. Input Switchpoint TTL to CMOS Mode

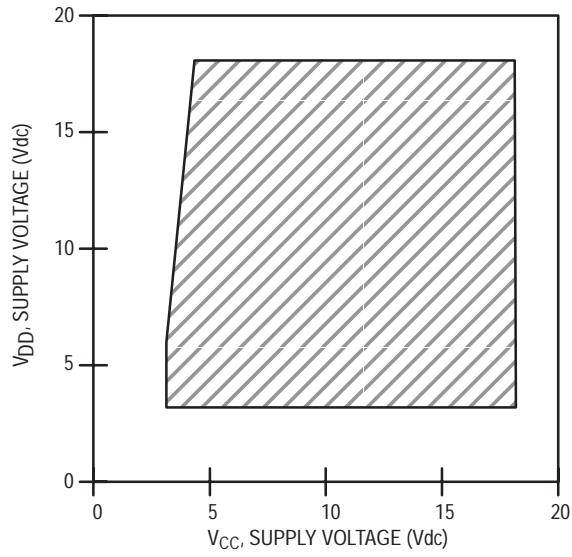


Figure 3. Operating Boundary CMOS to CMOS Mode

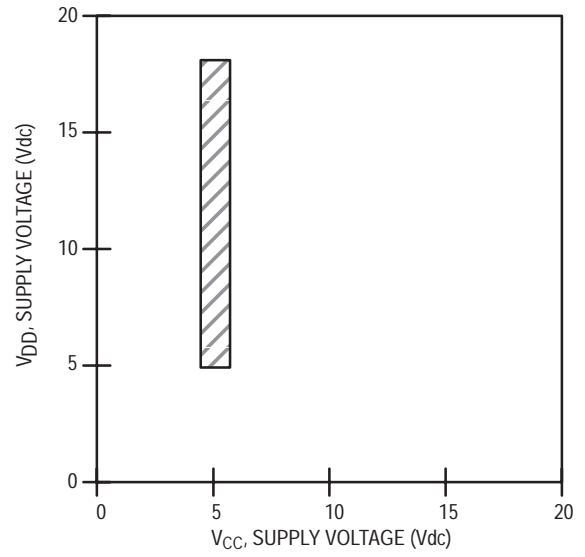


Figure 4. Operating Boundary TTL to CMOS Mode

# MC14511B

## BCD-To-Seven Segment Latch/Decoder/Driver

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ( $\overline{LT}$ ), blanking ( $\overline{BI}$ ), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (2.)

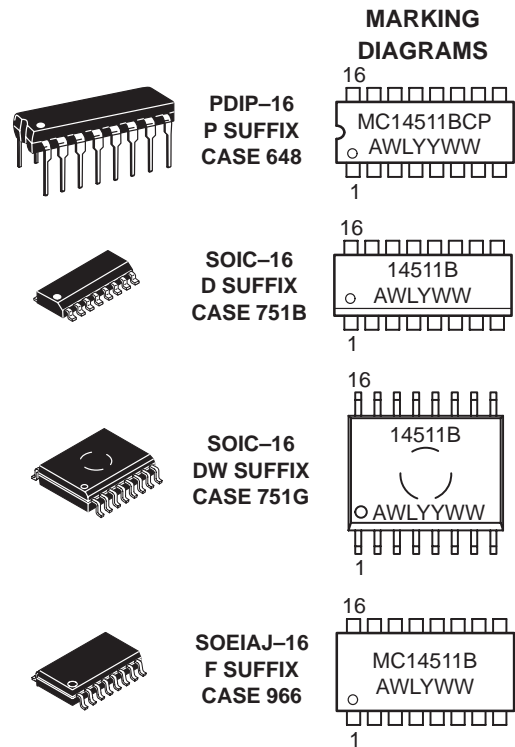
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
I	DC Current Drain per Input Pin	10	mA
$P_D$	Power Dissipation, per Package (3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$I_{OHmax}$	Maximum Output Drive Current (Source) per Output	25	mA
$P_{OHmax}$	Maximum Continuous Output Power (Source) per Output (4.)	50	mA

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C
4.  $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$



ON Semiconductor

<http://onsemi.com>



A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14511BCP	PDIP-16	2000/Box
MC14511BD	SOIC-16	48/Rail
MC14511BDW	SOIC-16	47/Rail
MC14511BDWR2	SOIC-16	1000/Tape & Reel
MC14511BF	SOEIAJ-16	See Note 1.
MC14511BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

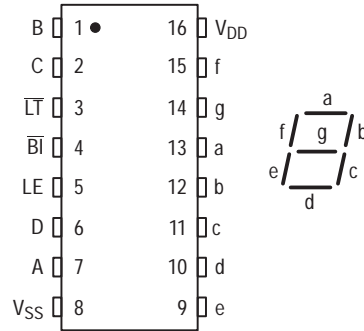
# MC14511B

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if  $V_{in}$  and  $V_{out}$  are not constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

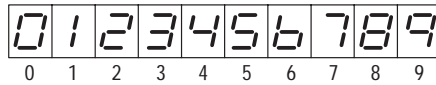
Due to the sourcing capability of this circuit, damage can occur to the device if  $V_{DD}$  is applied, and the outputs are shorted to  $V_{SS}$  and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).

## PIN ASSIGNMENT



## DISPLAY



## TRUTH TABLE

Inputs								Outputs						
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	1	1	1	1	1	0	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

\* Depends upon the BCD code previously applied when LE = 0



# MC14511B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(5.)</sup>	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	V <sub>OH</sub>	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc	
		10	9.1	—	9.1	9.58	—	9.1	—		
		15	14.1	—	14.1	14.59	—	14.1	—		
Input Voltage # (V <sub>O</sub> = 3.8 or 0.5 Vdc) (V <sub>O</sub> = 8.8 or 1.0 Vdc) (V <sub>O</sub> = 13.8 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 3.8 Vdc) (V <sub>O</sub> = 1.0 or 8.8 Vdc) (V <sub>O</sub> = 1.5 or 13.8 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Voltage Source (I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5.0 mA) (I <sub>OH</sub> = 10 mA) (I <sub>OH</sub> = 15 mA) (I <sub>OH</sub> = 20 mA) (I <sub>OH</sub> = 25 mA)  (I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5.0 mA) (I <sub>OH</sub> = 10 mA) (I <sub>OH</sub> = 15 mA) (I <sub>OH</sub> = 20 mA) (I <sub>OH</sub> = 25 mA)  (I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5.0 mA) (I <sub>OH</sub> = 10 mA) (I <sub>OH</sub> = 15 mA) (I <sub>OH</sub> = 20 mA) (I <sub>OH</sub> = 25 mA)	V <sub>OH</sub>	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc	
		10	9.1	—	9.1	9.58	—	9.1	—		Vdc
			—	—	—	9.26	—	—	—		
			9.0	—	9.0	9.17	—	8.6	—		
	15	—	—	—	9.04	—	—	—	Vdc		
		8.6	—	8.6	8.90	—	8.2	—			
		—	—	—	8.70	—	—	—			
		14.1	—	14.1	14.59	—	14.1	—			
		—	—	—	14.27	—	—	—			
	10	—	—	—	14.18	—	13.6	—	Vdc		
		14	—	14	14.18	—	—	—			
		—	—	—	14.07	—	—	—			
13.6		—	13.6	13.95	—	13.2	—				
15	—	—	—	13.70	—	—	—	Vdc			
	—	—	—	—	—	—	—				
	—	—	—	—	—	—	—				
	—	—	—	—	—	—	—				
Output Drive Current (V <sub>OL</sub> = 0.4 V) (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) V <sub>in</sub> = 0 or V <sub>DD</sub> , I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current <sup>(6.)</sup> <sup>(7.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.9 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (3.8 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (5.7 μA/kHz) f + I <sub>DD</sub>								

5. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc

2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc

2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

6. The formulas given are for the typical characteristics only at 25°C.

7. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in Vdc, and f in kHz is input frequency.

# MC14511B

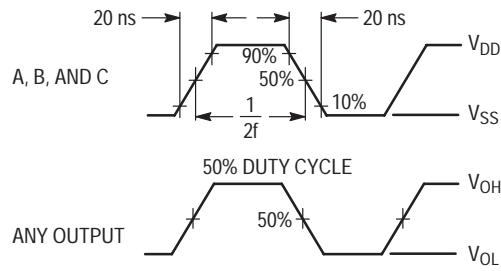
## SWITCHING CHARACTERISTICS <sup>(8.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{TLH} = (0.20 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	40 30 25	80 60 50	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	125 75 65	250 150 130	ns
Data Propagation Delay Time $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$  $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	$t_{PLH}$   $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	640 250 175  720 290 200	1280 500 350  1440 580 400	ns
Blank Propagation Delay Time $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 585 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 187.5 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 142.5 \text{ ns}$  $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	$t_{PLH}$   $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	600 200 150  485 200 160	750 300 220  970 400 320	ns
Lamp Test Propagation Delay Time $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$  $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	$t_{PLH}$   $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	313 125 90  313 125 90	625 250 180  625 250 180	ns
Setup Time	$t_{su}$	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	$t_h$	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	$t_{WL}$	5.0 10 15	520 220 130	260 110 65	— — —	ns

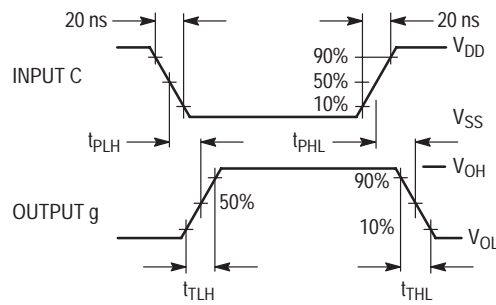
8. The formulas given are for the typical characteristics only.

# MC14511B

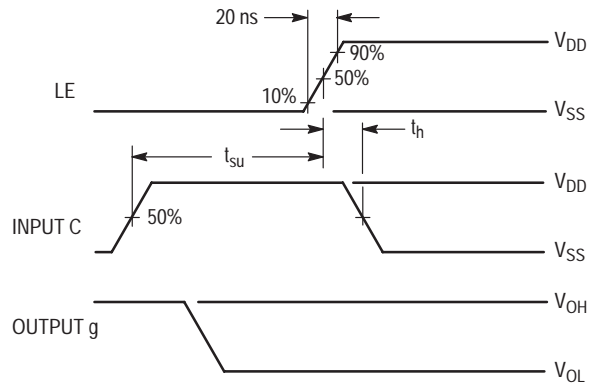
Input LE low, and Inputs D,  $\overline{B1}$  and  $\overline{L1}$  high.  
 f in respect to a system clock.  
 All outputs connected to respective  $C_L$  loads.



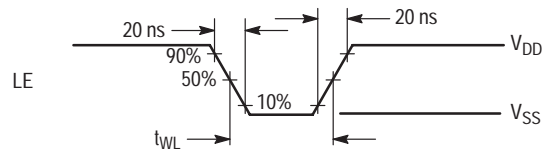
**Figure 1. Dynamic Power Dissipation Signal Waveforms**



**(a) Inputs D and LE low, and Inputs A, B,  $\overline{B1}$  and  $\overline{L1}$  high.**



**(b) Input D low, Inputs A, B,  $\overline{B1}$  and  $\overline{L1}$  high.**



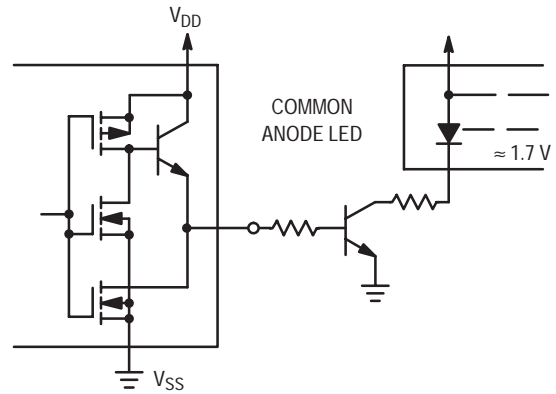
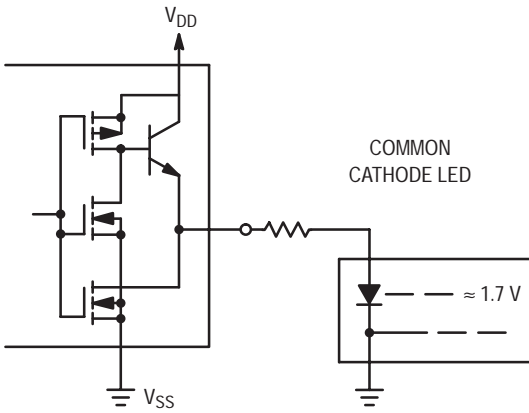
**(c) Data DCBA strobed into latches.**

**Figure 2. Dynamic Signal Waveforms**

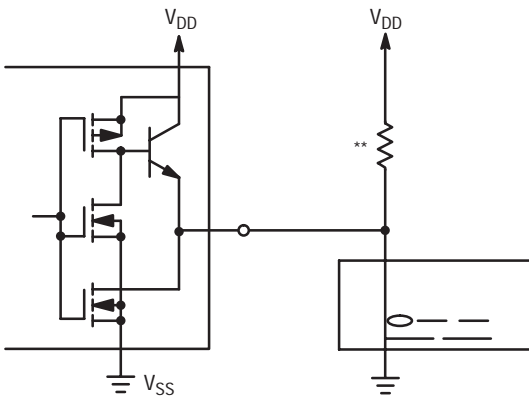
# MC14511B

## CONNECTIONS TO VARIOUS DISPLAY READOUTS

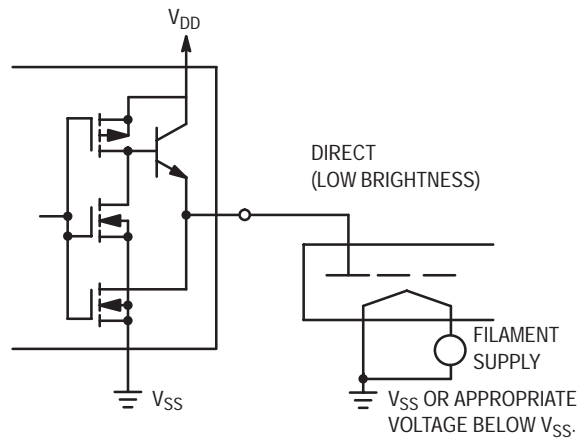
### LIGHT EMITTING DIODE (LED) READOUT



### INCANDESCENT READOUT

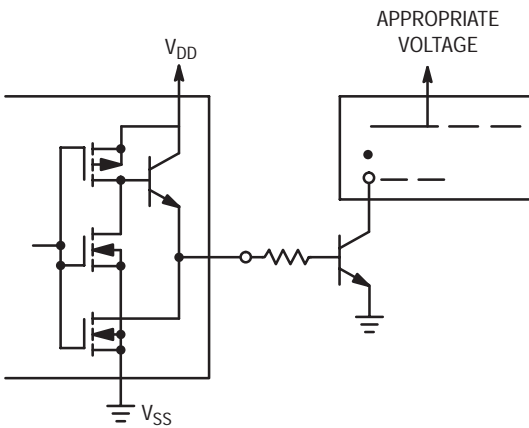


### FLUORESCENT READOUT

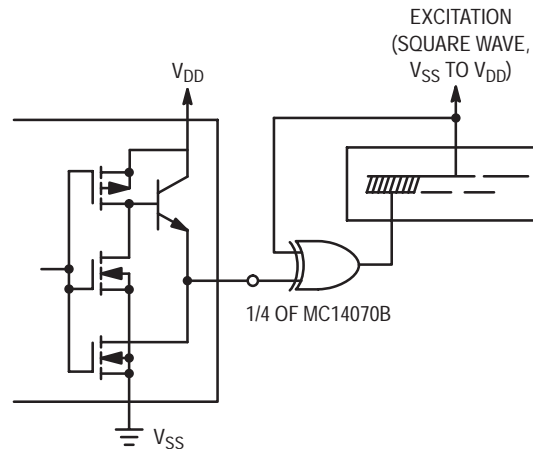


(CAUTION: Maximum working voltage = 18.0 V)

### GAS DISCHARGE READOUT



### LIQUID CRYSTAL (LCD) READOUT

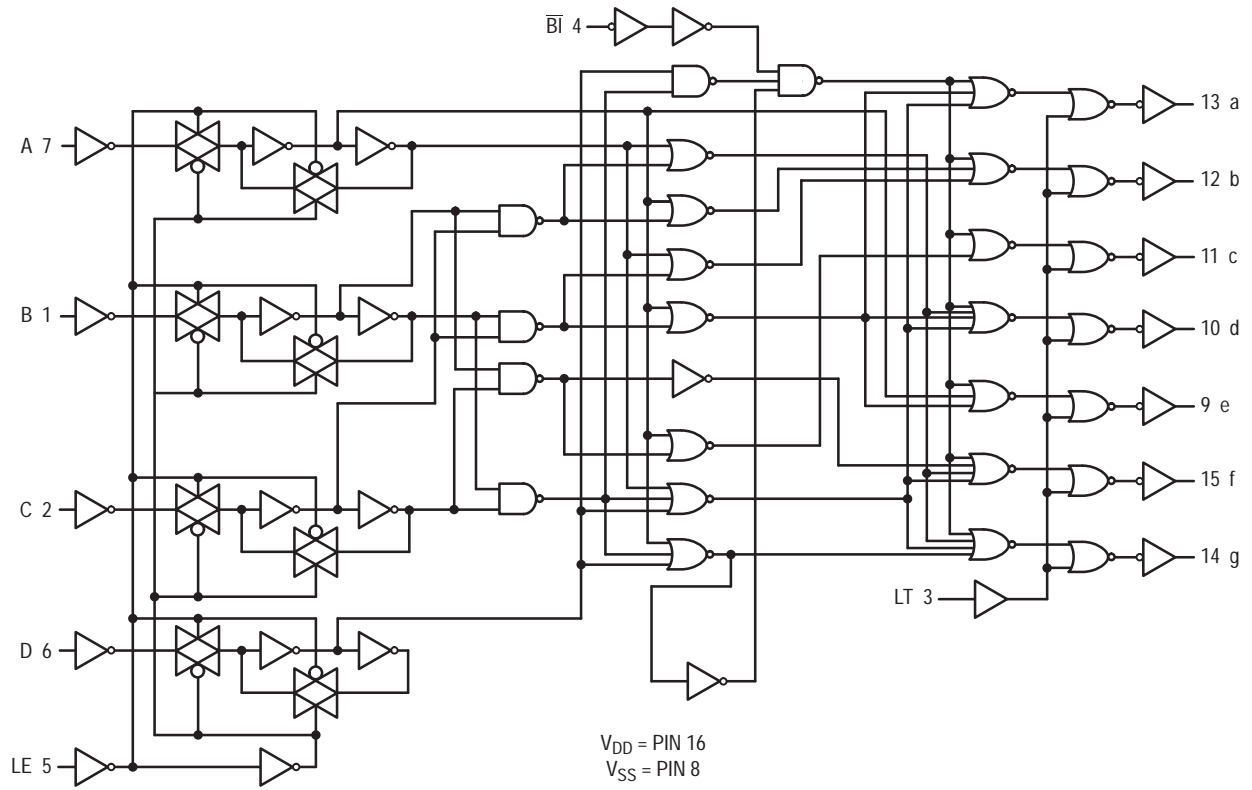


\*\* A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

# MC14511B

## LOGIC DIAGRAM



# MC14512B

## 8-Channel Data Selector

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

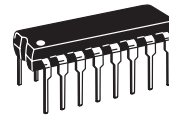
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



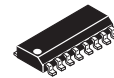
ON Semiconductor

<http://onsemi.com>

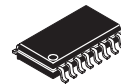
### MARKING DIAGRAMS



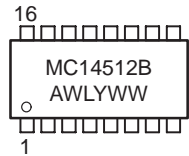
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14512BCP	PDIP-16	2000/Box
MC14512BD	SOIC-16	48/Rail
MC14512BDR2	SOIC-16	2500/Tape & Reel
MC14512BF	SOEIAJ-16	See Note 1.
MC14512BFL1	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14512B

## TRUTH TABLE

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

## PIN ASSIGNMENT

X0	1	16	V <sub>DD</sub>
X1	2	15	DIS
X2	3	14	Z
X3	4	13	C
X4	5	12	B
X5	6	11	A
X6	7	10	INH
V <sub>SS</sub>	8	9	X7

# MC14512B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05	—		
V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
			5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
			10	-1.6	—	-1.3	-2.25	—	-0.9	—	
	Sink	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>								
Three-State Leakage Current	I <sub>TL</sub>	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.



# MC14512B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ , See Figure 1)

Characteristic	Symbol	$V_{DD}$	All Types		Unit
			Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0	100	200	ns
		10	50	100	
		15	40	80	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	$t_{PLH}$	5.0	330	650	ns
		10	125	250	
		15	85	170	
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	$t_{PHL}$	5.0	330	650	ns
		10	125	250	
		15	85	170	
3-State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	$t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}$	5.0	60	150	ns
		10	35	100	
		15	30	75	

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

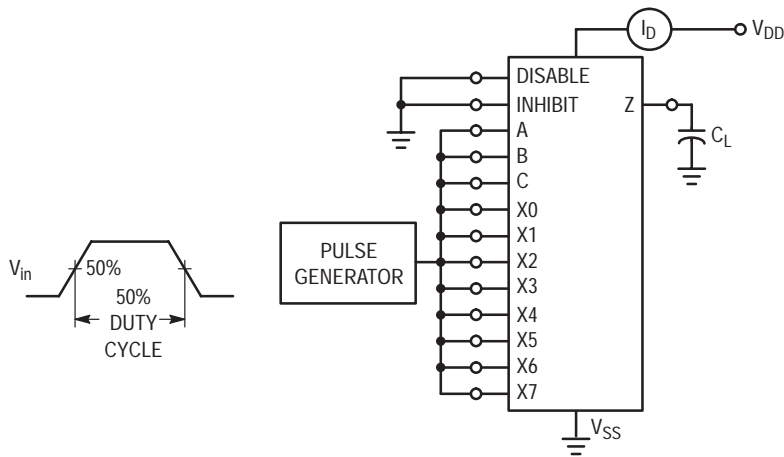


Figure 1. Power Dissipation Test Circuit and Waveform

# MC14512B

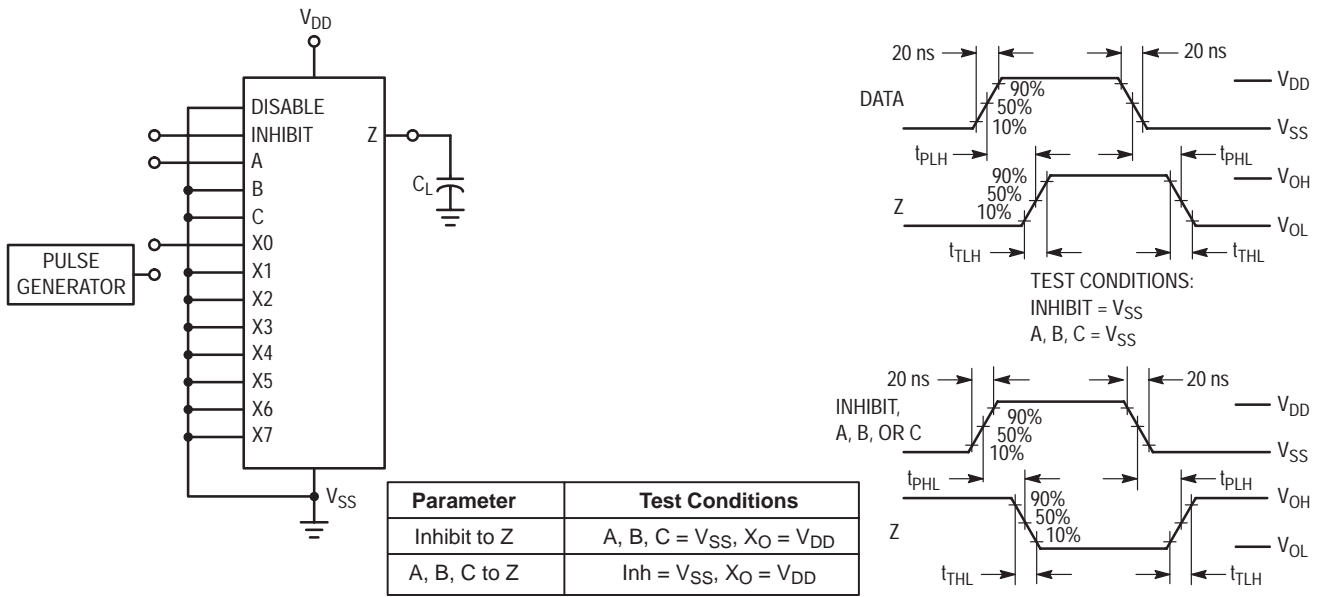


Figure 2. AC Test Circuit and Waveforms

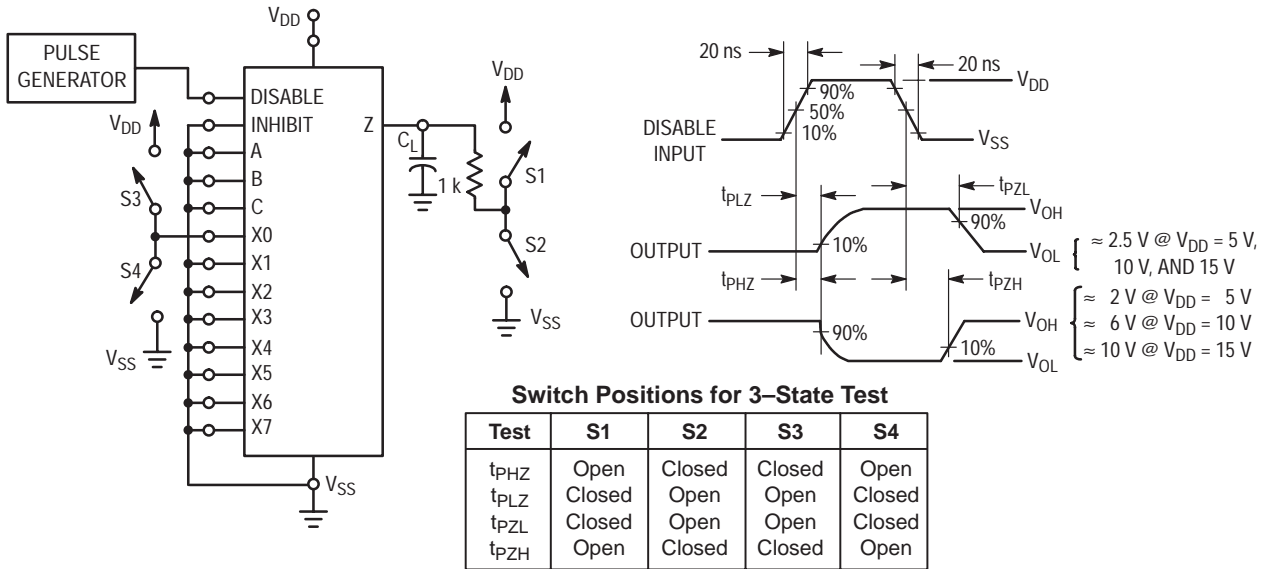
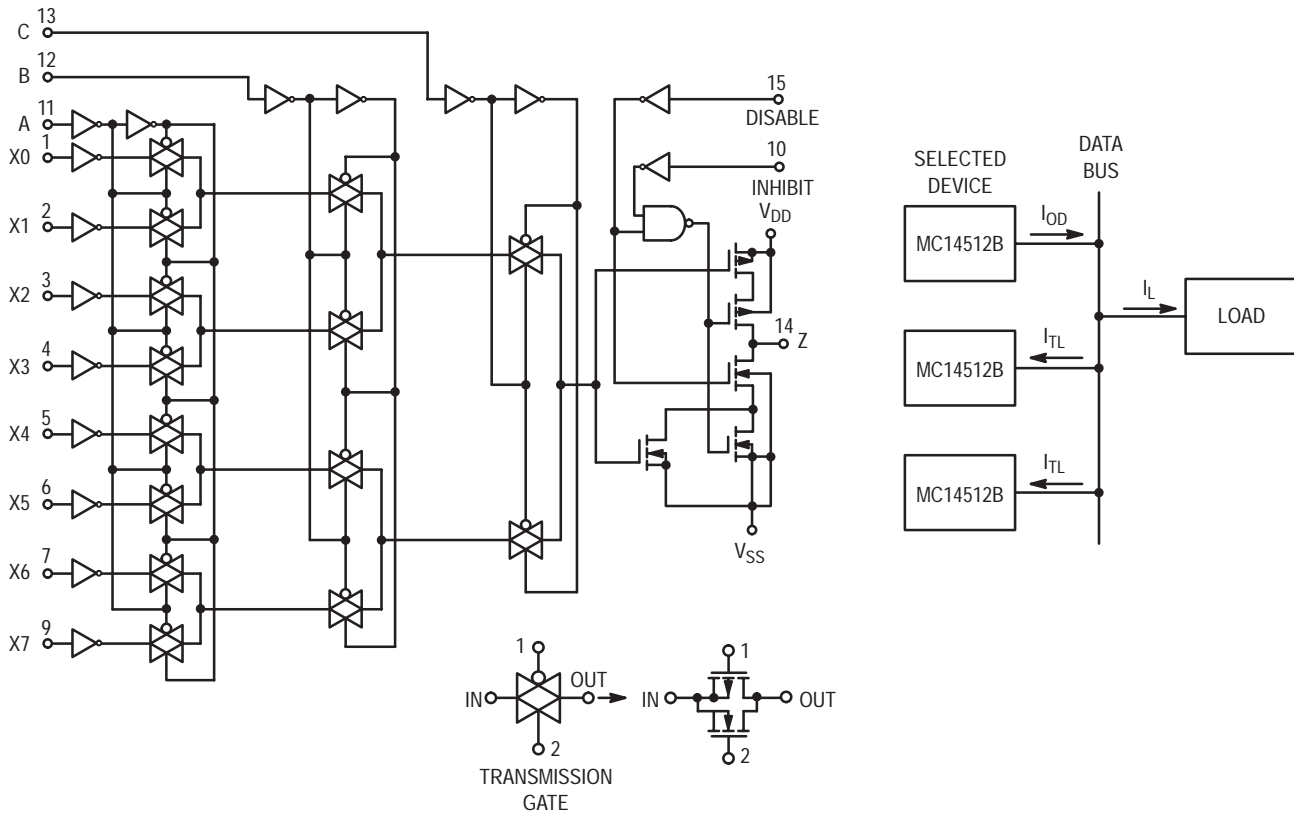


Figure 3. 3-State AC Test Circuit and Waveform

# MC14512B

## LOGIC DIAGRAM



### 3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance “off” state. The number of 8-bit data selectors,  $N$ , that may be connected to a bus line is determined from the output drive current,  $I_{OD}$ , 3-state or disable output leakage current,  $I_{TL}$ , and the load current,  $I_L$ , required to drive the bus line

(including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

$N$  must be calculated for both high and low logic state of the bus line.

# MC14513B

## BCD-To-Seven Segment Latch/Decoder/Driver

### CMOS MSI (Low-Power Complementary MOS)

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test ( $\overline{LT}$ ), blanking ( $\overline{BI}$ ), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

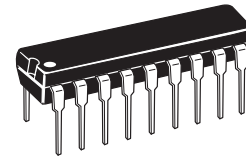
#### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
I	DC Current Drain per Input Pin	10	mA
$P_D$	Power Dissipation, per Package (2.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$I_{OHmax}$	Maximum Continuous Output Drive Current (Source) per Output	25	mA
$P_{OHmax}$	Maximum Continuous Output Power (Source) per Output (3.)	50	mW



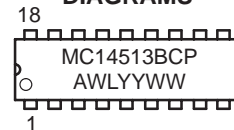
ON Semiconductor

<http://onsemi.com>



#### MARKING DIAGRAMS

PDIP-18  
P SUFFIX  
CASE 707



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MC14513BCP	PDIP-18	20/Rail

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if  $V_{in}$  and  $V_{out}$  are not constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

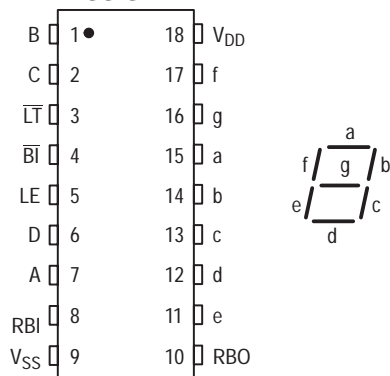
Due to the sourcing capability of this circuit, damage can occur to the device if  $V_{DD}$  is applied, and the outputs are shorted to  $V_{SS}$  and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).

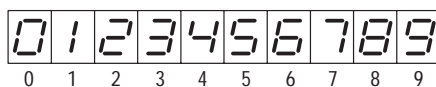
1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C  
From 65°C To 125°C
3.  $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

# MC14513B

## PIN ASSIGNMENT



## DISPLAY



## TRUTH TABLE

Inputs								Outputs								
RBI	LE	B $\bar{I}$	L $\bar{T}$	D	C	B	A	RBO	a	b	c	d	e	f	g	Display
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†				*				*

X = Don't Care

†RBO = RBI ( $\bar{D} \bar{C} \bar{B} \bar{A}$ ), indicated by other rows of table

\*Depends upon the BCD code previously applied when LE = 0

# MC14513B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max		
Output Voltage — Segment Outputs "0" Level $V_{in} = V_{DD}$ or 0	$V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{in} = 0$ or $V_{DD}$	$V_{OH}$	5.0	4.1	—	4.1	5.0	—	4.1		—
			10	9.1	—	9.1	10	—	9.1		—
			15	14.1	—	14.1	15	—	14.1		—
Output Voltage — RBO Output "0" Level $V_{in} = V_{DD}$ or 0	$V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{in} = 0$ or $V_{DD}$	$V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage <sup>(4.)</sup> "0" Level ( $V_O = 3.8$ or $0.5$ Vdc) ( $V_O = 8.8$ or $1.0$ Vdc) ( $V_O = 13.8$ or $1.5$ Vdc)	$V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level ( $V_O = 0.5$ or $3.8$ Vdc) ( $V_O = 1.0$ or $8.8$ Vdc) ( $V_O = 1.5$ or $13.8$ Vdc)	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Voltage — Segments Source	$V_{OH}$	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc	
			( $I_{OH} = 5.0$ mA)	—	—	—	4.24	—	—		—
			( $I_{OH} = 10$ mA)	3.9	—	3.9	4.12	—	3.5		—
			( $I_{OH} = 15$ mA)	—	—	—	3.94	—	—		—
			( $I_{OH} = 20$ mA)	3.4	—	3.4	3.70	—	3.0		—
			( $I_{OH} = 25$ mA)	—	—	—	3.54	—	—		—
		10	( $I_{OH} = 0$ mA)	9.1	—	9.1	9.58	—	9.1	—	Vdc
			( $I_{OH} = 5.0$ mA)	—	—	—	9.26	—	—	—	
			( $I_{OH} = 10$ mA)	9.0	—	9.0	9.17	—	8.6	—	
			( $I_{OH} = 15$ mA)	—	—	—	9.04	—	—	—	
			( $I_{OH} = 20$ mA)	8.6	—	8.6	8.90	—	8.2	—	
			( $I_{OH} = 25$ mA)	—	—	—	8.75	—	—	—	
		15	( $I_{OH} = 0$ mA)	14.1	—	14.1	14.59	—	14.1	—	Vdc
			( $I_{OH} = 5.0$ mA)	—	—	—	14.27	—	—	—	
			( $I_{OH} = 10$ mA)	14	—	14	14.18	—	13.6	—	
			( $I_{OH} = 15$ mA)	—	—	—	14.07	—	—	—	
			( $I_{OH} = 20$ mA)	13.6	—	13.6	13.95	—	13.2	—	
			( $I_{OH} = 25$ mA)	—	—	—	13.80	—	—	—	

(continued)

# MC14513B

## ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Drive Current — RBO Output (V <sub>OH</sub> = 2.5 V) Source (V <sub>OH</sub> = 9.5 V) (V <sub>OH</sub> = 13.5 V)  (V <sub>OL</sub> = 0.4 V) Sink (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	I <sub>OH</sub>	5.0	-0.40	—	-0.32	-0.64	—	-0.22	—	mAdc
		10	-0.21	—	-0.17	-0.34	—	-0.12	—	
		15	-0.81	—	-0.66	-1.30	—	-0.46	—	
	I <sub>OL</sub>	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
		10	0.47	—	0.38	0.75	—	0.26	—	
		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments (V <sub>OL</sub> = 0.4 V) Sink (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V <sub>in</sub> = 0 or V <sub>DD</sub> , I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.9 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.8 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (5.7 μA/kHz) f + I <sub>DD</sub>							

4. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc

2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc

2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in Vdc, and f in kHz is input frequency.

Input LE and RBI low, and Inputs D,  $\overline{BI}$  and  $\overline{LT}$  high.  
f in respect to a system clock.

All outputs connected to respective C<sub>L</sub> loads.

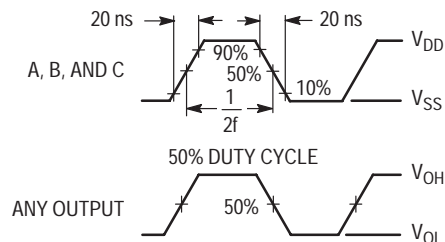


Figure 1. Dynamic Power Dissipation Signal Waveforms

# MC14513B

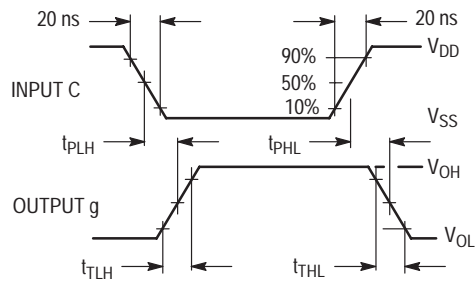
## SWITCHING CHARACTERISTICS <sup>(7.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time — Segment Outputs	$t_{TLH}$	5.0 10 15	— — —	40 30 25	80 60 50	ns
Output Rise Time — RBO Output	$t_{TLH}$	5.0 10 15	— — —	480 240 190	960 480 380	ns
Output Fall Time — Segment Outputs <sup>(7.)</sup> $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	125 75 65	250 150 130	ns
Output Fall Time — RBO Outputs $t_{THL} = (3.25 \text{ ns/pF}) C_L + 107.5 \text{ ns}$ $t_{THL} = (1.35 \text{ ns/pF}) C_L + 67.5 \text{ ns}$ $t_{THL} = (0.95 \text{ ns/pF}) C_L + 62.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	270 135 110	540 270 220	ns
Propagation Delay Time — A, B, C, D Inputs <sup>(7.)</sup> $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$  $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	640 250 175	1280 500 350	ns
	$t_{PHL}$	5.0 10 15	— — —	720 290 200	1440 580 400	ns
Propagation Delay Time — RBI and $\overline{BI}$ Inputs <sup>(7.)</sup> $t_{PLH} = (1.05 \text{ ns/pF}) C_L + 547.5 \text{ ns}$ $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 135 \text{ ns}$  $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	600 200 150	750 300 220	ns
	$t_{PHL}$	5.0 10 15	— — —	485 200 160	970 400 320	ns
Propagation Delay Time — $\overline{LT}$ Input <sup>(7.)</sup> $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$  $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	313 125 90	625 250 180	ns
	$t_{PHL}$	5.0 10 15	— — —	313 125 90	625 250 180	ns
Setup Time	$t_{su}$	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	$t_h$	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0 10 15	520 220 130	260 110 65	— — —	ns

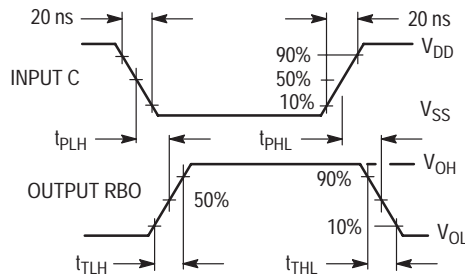
7. The formulas given are for the typical characteristics only.



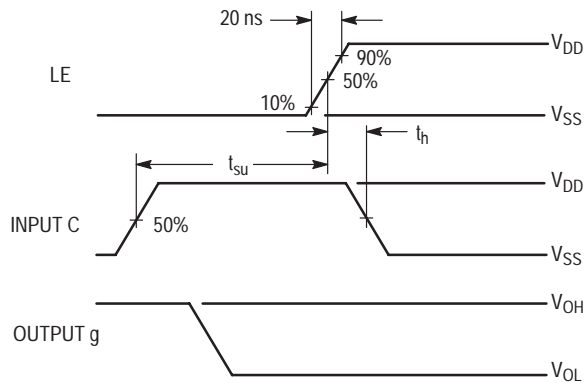
# MC14513B



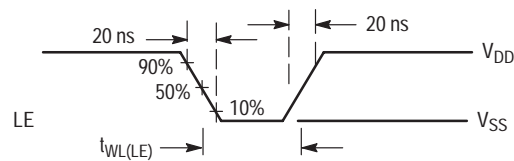
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B,  $\overline{BI}$  and  $\overline{LT}$  high.



b. Inputs A, B, D and LE low, and Inputs RBI,  $\overline{BI}$  and  $\overline{LT}$  high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B,  $\overline{BI}$  and  $\overline{LT}$  high.



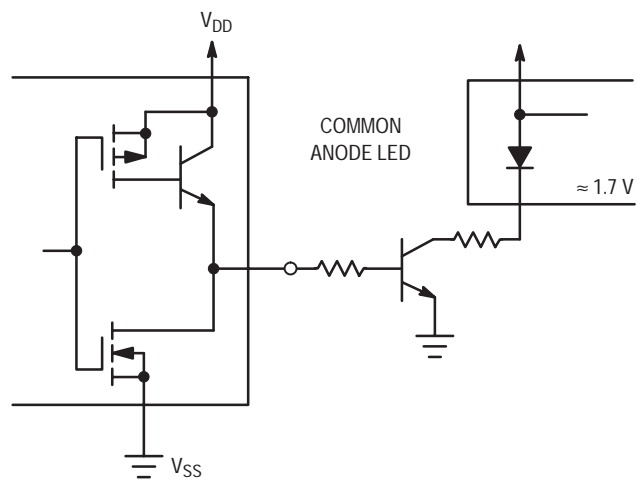
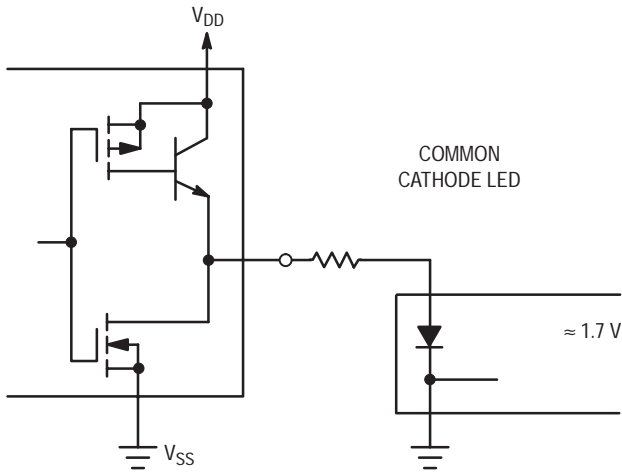
d. Pulse Width: Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

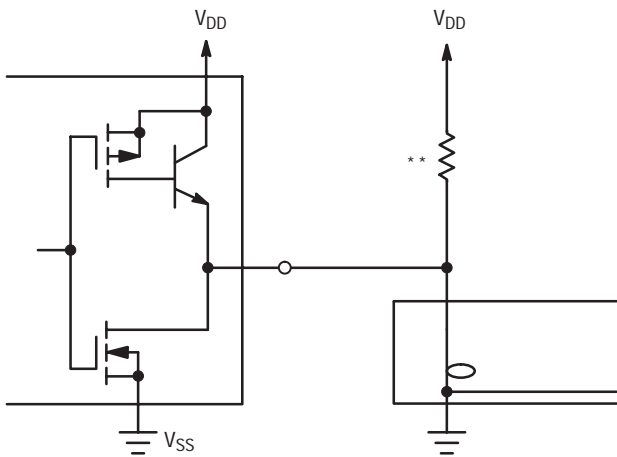
# MC14513B

## CONNECTIONS TO VARIOUS DISPLAY READOUTS

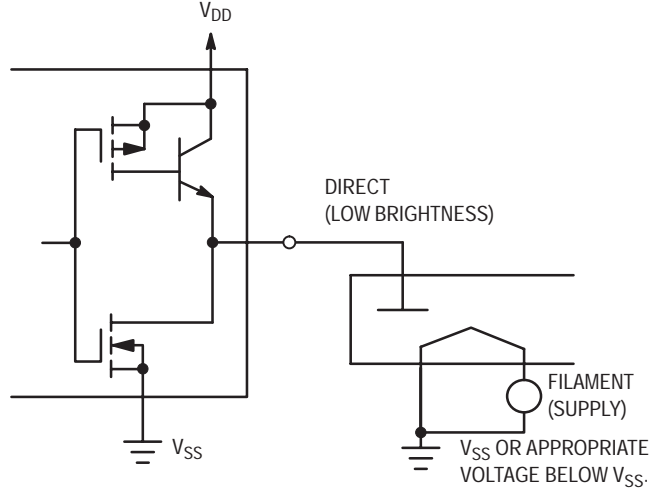
### LIGHT EMITTING DIODE (LED) READOUT



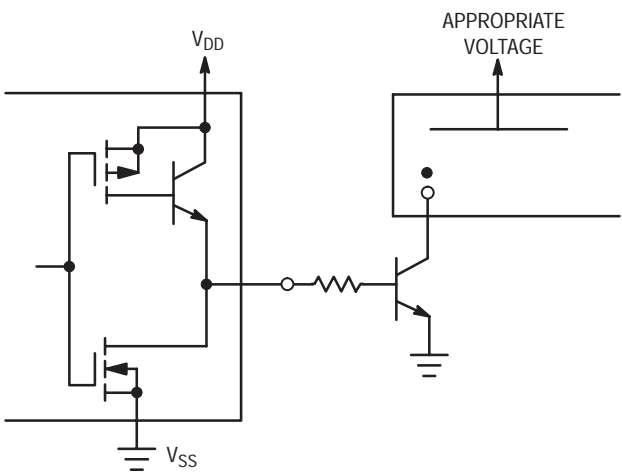
### INCANDESCENT READOUT



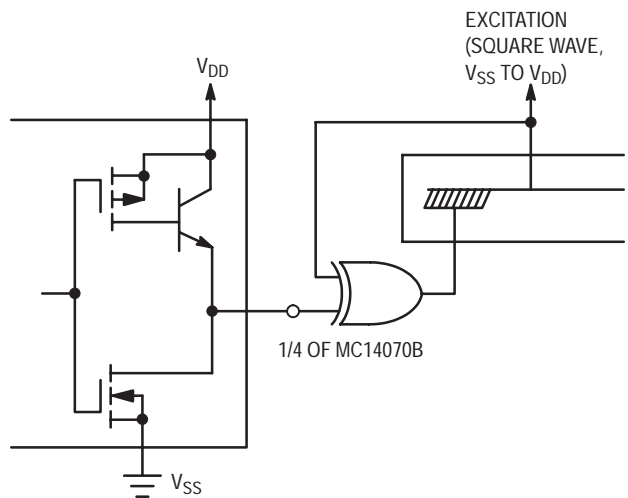
### FLUORESCENT READOUT



### GAS DISCHARGE READOUT



### LIQUID CRYSTAL (LC) READOUT

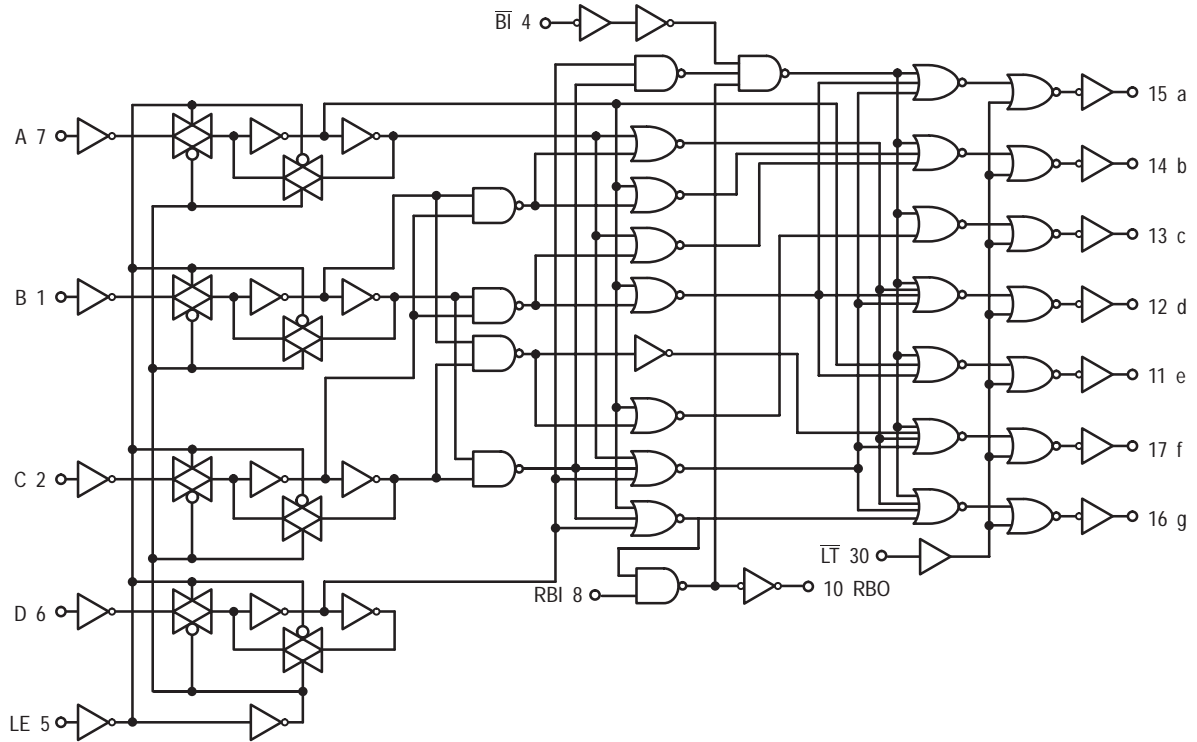


\*\* A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC's not recommended for life of LC readouts.

# MC14513B

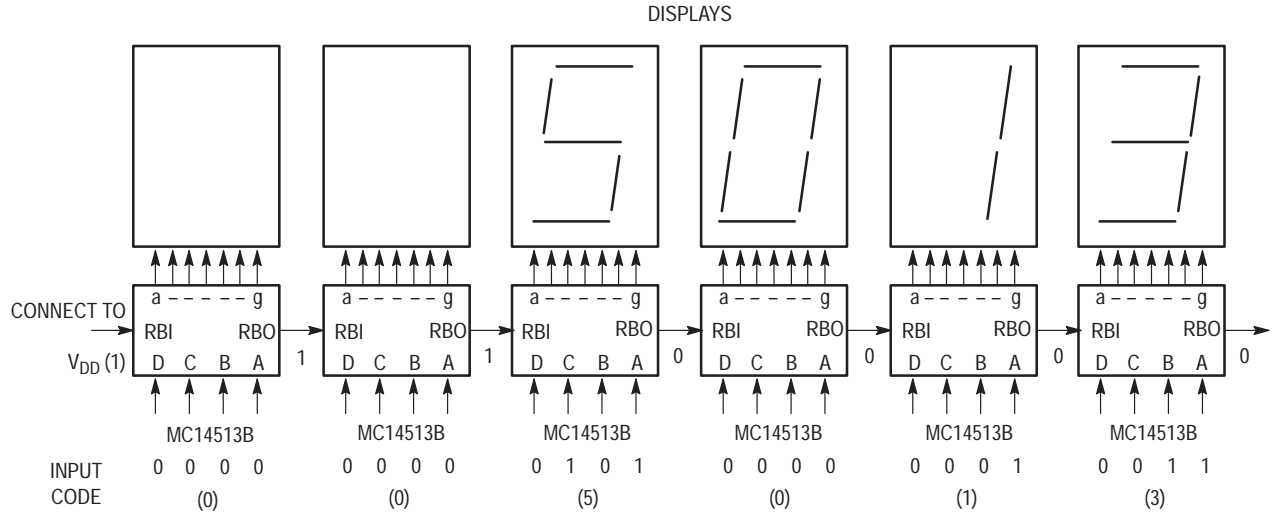
## LOGIC DIAGRAM



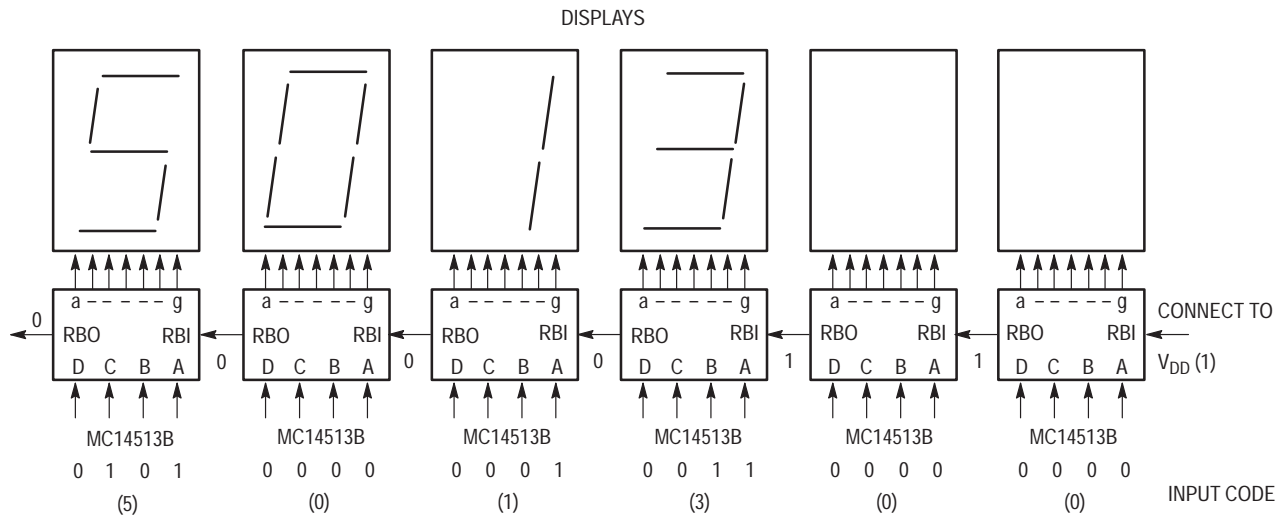
# MC14513B

## TYPICAL APPLICATIONS FOR RIPPLE BLANKING

### LEADING EDGE ZERO SUPPRESSION



### TRAILING EDGE ZERO SUPPRESSION



# MC14514B, MC14515B

## 4-Bit Transparent Latch/4-to-16 Line Decoder

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical “1” at the selected output, whereas the MC14515B (output active low option) presents a logical “0” at the selected output. The latches are R–S type flip–flops which hold the last input data presented prior to the strobe transition from “1” to “0”. These high and low options of a 4–bit latch/4 to 16 line decoder are constructed with N–channel and P–channel enhancement mode devices in a single monolithic structure. The latches are R–S type flip–flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	–0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	–0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	–55 to +125	°C
$T_{stg}$	Storage Temperature Range	–65 to +150	°C
$T_L$	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

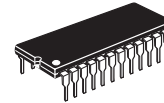
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



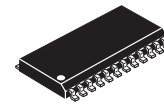
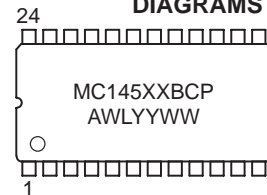
ON Semiconductor

<http://onsemi.com>



PDIP–24  
P SUFFIX  
CASE 709

### MARKING DIAGRAMS



SOIC–24  
DW SUFFIX  
CASE 751E



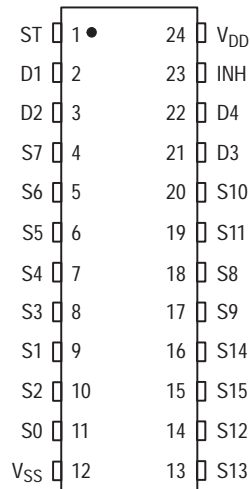
XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14514BCP	PDIP–24	15/Rail
MC14514BDW	SOIC–24	30/Rail
MC14514BDWR2	SOIC–24	1000/Tape & Reel
MC14515BCP	PDIP–24	15/Rail
MC14515BDW	SOIC–24	30/Rail
MC14515BDWR2	SOIC–24	1000/Tape & Reel

# MC14514B, MC14515B

## PIN ASSIGNMENT



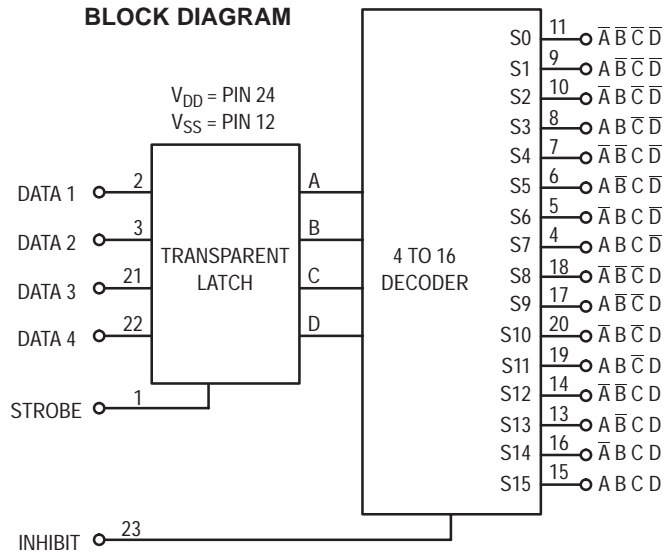
DECODE TRUTH TABLE (Strobe = 1)\*

Inhibit	Data Inputs				Selected Output MC14514 = Logic "1" MC14515 = Logic "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

\*Strobe = 0, Data is latched

## BLOCK DIAGRAM



# MC14514B, MC14515B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>TL</sub>	5.0	I <sub>T</sub> = (1.35 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.70 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (4.05 μA/kHz) f + I <sub>DD</sub>							μAdc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14514B, MC14515B

## SWITCHING CHARACTERISTICS (6.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	All Types			Unit
			Min	Typ (7.)	Max	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time; Data, Strobe to S $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.86 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	550 225 150	1100 450 300	ns
Inhibit Propagation Delay Times $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	400 150 100	800 300 200	ns
Setup Time Data to Strobe	$t_{su}$	5.0 10 15	250 100 75	125 50 38	— — —	ns
Hold Time Strobe to Data	$t_h$	5.0 10 15	-20 0 10	-100 -40 -30	— — —	ns
Strobe Pulse Width	$t_{WH}$	5.0 10 15	350 100 75	175 50 38	— — —	ns

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

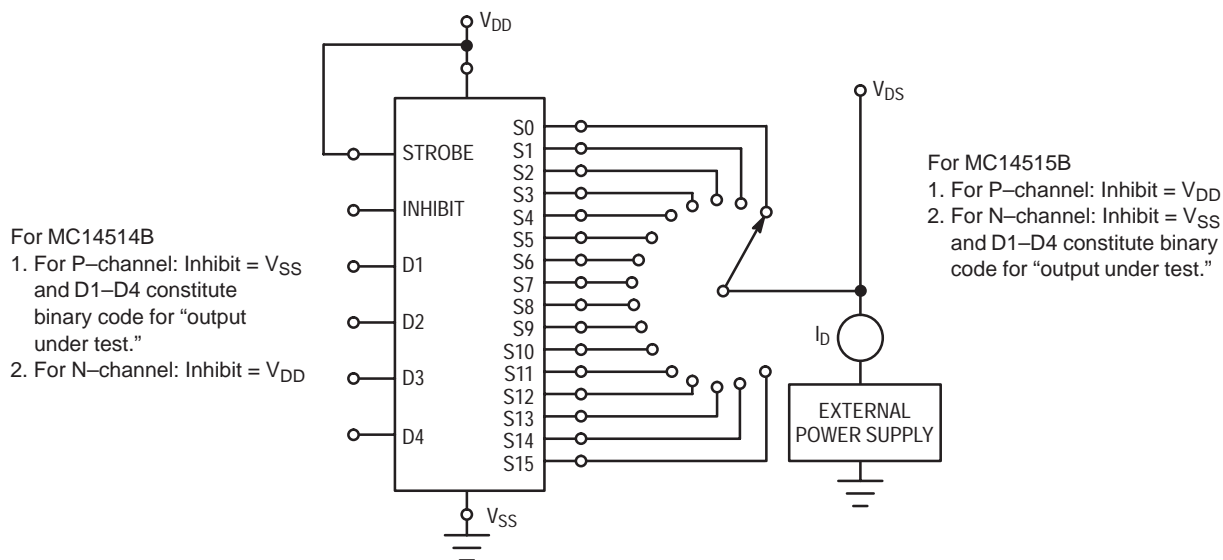


Figure 1. Drain Characteristics Test Circuit



## MC14514B, MC14515B

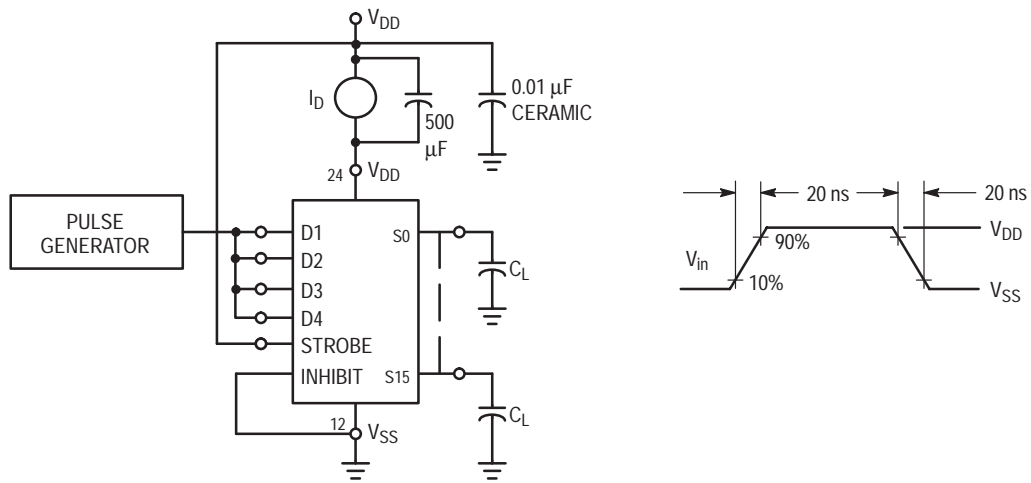


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

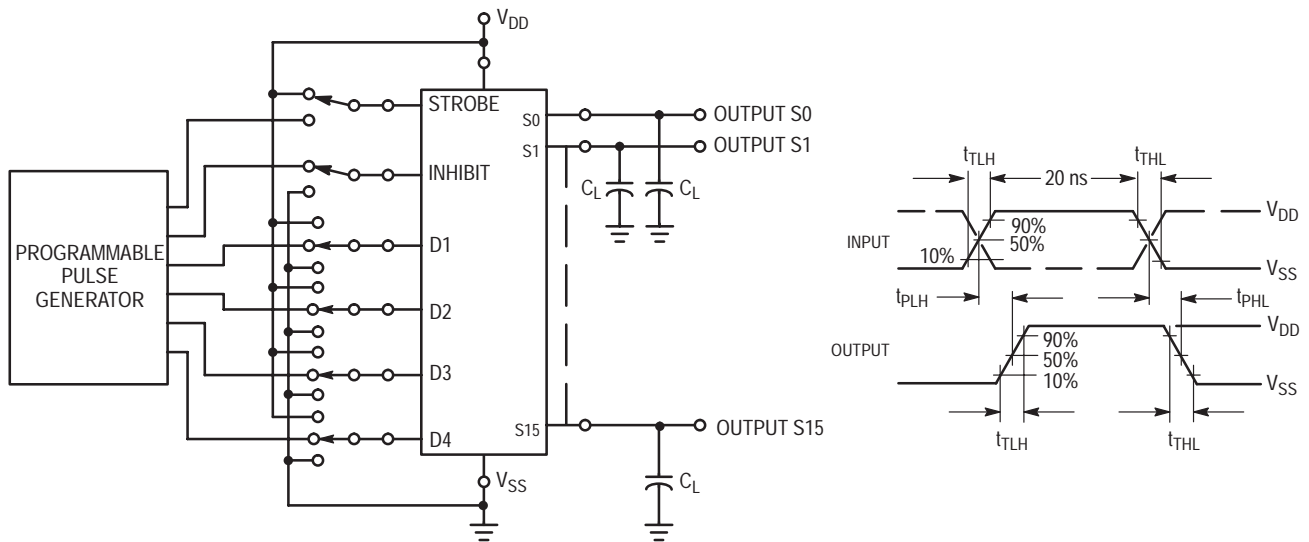
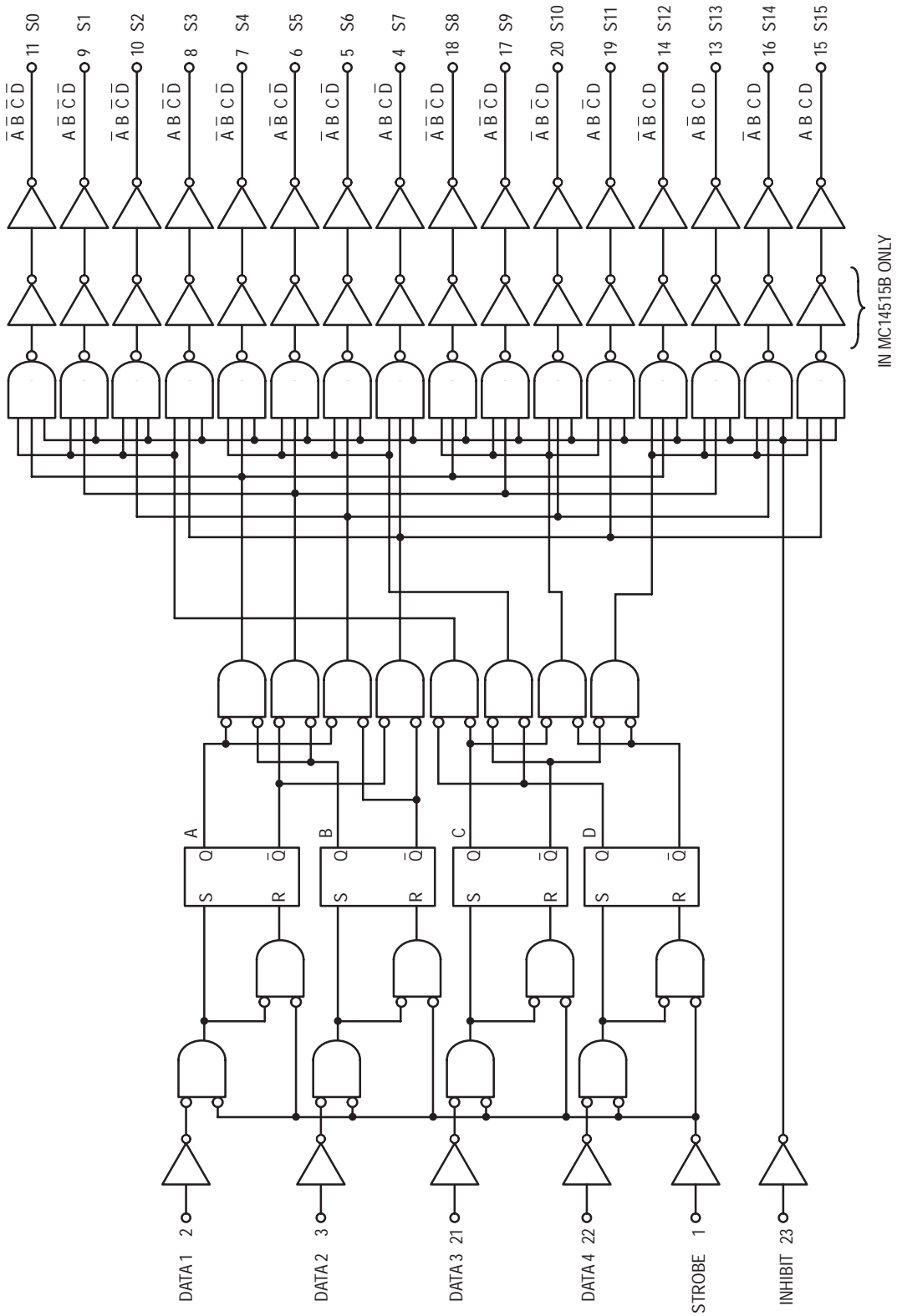


Figure 3. Switching Time Test Circuit and Waveforms

# MC14514B, MC14515B

## LOGIC DIAGRAM



# MC14514B, MC14515B

## COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

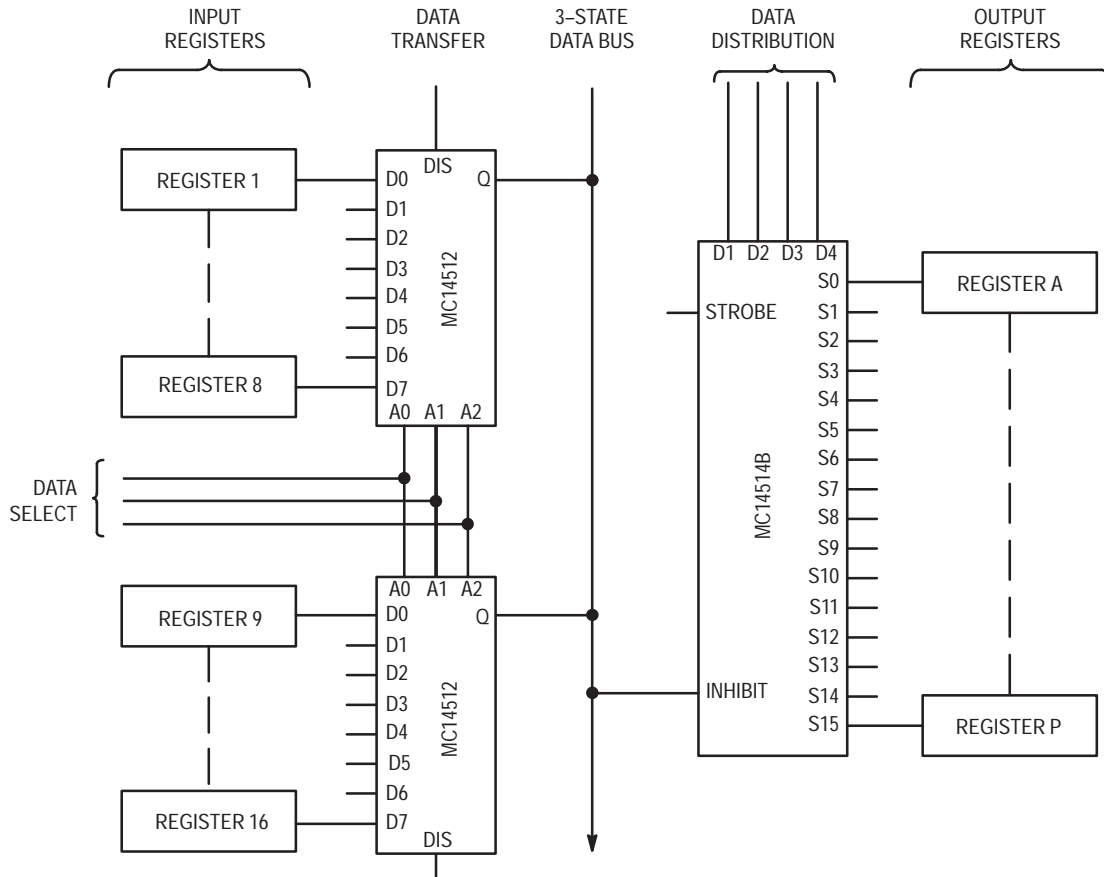
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight

times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

### DATA ROUTING SYSTEM



# MC14516B

## Binary Up/Down Counter

The MC14516B synchronous up/down binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the Carry Out to the Carry In of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

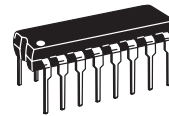
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$



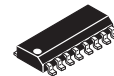
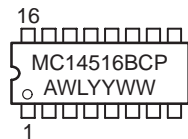
ON Semiconductor

<http://onsemi.com>

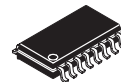
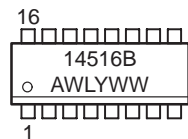
### MARKING DIAGRAMS



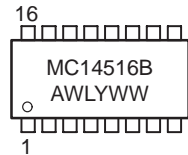
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14516BCP	PDIP-16	2000/Box
MC14516BD	SOIC-16	48/Rail
MC14516BDR2	SOIC-16	2500/Tape & Reel
MC14516BF	SOEIAJ-16	See Note 1.
MC14516BFEL	SOEIAJ-16	See Note 1.

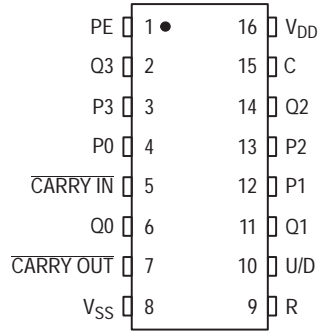
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

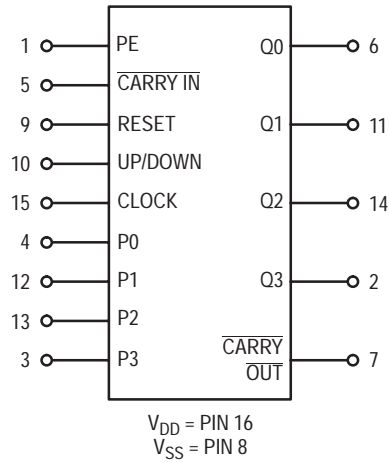
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# MC14516B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0	$\nearrow$	Count Up
0	0	0	0	$\searrow$	Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

NOTE: When counting up, the  $\overline{\text{Carry Out}}$  signal is normally high and is low only when Q0 through Q3 are high and  $\overline{\text{Carry In}}$  is low. When counting down,  $\overline{\text{Carry Out}}$  is low only when Q0 through Q3 and  $\overline{\text{Carry In}}$  are low.

# MC14516B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage  $V_O = 4.5$ or $0.5$ Vdc $V_O = 9.0$ or $1.0$ Vdc $V_O = 13.5$ or $1.5$ Vdc  $V_O = 0.5$ or $4.5$ Vdc $V_O = 1.0$ or $9.0$ Vdc $V_O = 1.5$ or $13.5$ Vdc	"0" Level  $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level  $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current  Source $V_{OH} = 2.5$ Vdc $V_{OH} = 4.6$ Vdc $V_{OH} = 9.5$ Vdc $V_{OH} = 13.5$ Vdc  Sink $V_{OL} = 0.4$ Vdc $V_{OL} = 0.5$ Vdc $V_{OL} = 1.5$ Vdc	$I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc
Input Capacitance $(V_{in} = 0)$	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (0.58 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.20 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (1.70 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

# MC14516B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$  Clock to $\overline{\text{Carry Out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$  $\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$  Preset or Reset to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$  Preset or Reset to $\overline{\text{Carry Out}}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	315 130 100	630 260 200	ns
Reset Pulse Width	$t_w$	5.0 10 15	380 200 160	190 100 80	— — —	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	350 170 140	200 100 75	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.0 6.0 8.0	1.5 3.0 4.0	MHz

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an Indication of the IC's potential performance.

# MC14516B

## SWITCHING CHARACTERISTICS <sup>(9.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ ) (continued)

Characteristic	Symbol	$V_{DD}$	All Types			Unit
			Min	Typ <sup>(10.)</sup>	Max	
Preset or Reset Removal Time The Preset or Reset signal must be low prior to a positive-going transition of the clock.	$t_{rem}$	5.0	650	325	—	ns
		10	230	115	—	
		15	180	90	—	
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0	—	—	15	$\mu\text{s}$
		10	—	—	5	
		15	—	—	4	
Setup Time Carry In to Clock	$t_{su}$	5.0	260	130	—	ns
		10	120	60	—	
		15	100	50	—	
Hold Time Clock to Carry In	$t_h$	5.0	0	-60	—	ns
		10	20	-20	—	
		15	20	0	—	
Setup Time Up/Down to Clock	$t_{su}$	5.0	500	250	—	ns
		10	200	100	—	
		15	150	75	—	
Hold Time Clock to Up/Down	$t_h$	5.0	-70	-160	—	ns
		10	-10	-60	—	
		15	0	-40	—	
Setup Time Pn to PE	$t_{su}$	5.0	-40	-120	—	ns
		10	-30	-70	—	
		15	-25	-50	—	
Hold Time PE to Pn	$t_h$	5.0	480	240	—	ns
		10	420	210	—	
		15	420	210	—	
Preset Enable Pulse Width	$t_{WH}$	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	

9. The formulas given are for the typical characteristics only at 25°C.

10. Data labelled "Typ" is not to be used for design purposes but is intended as an Indication of the IC's potential performance.



# MC14516B

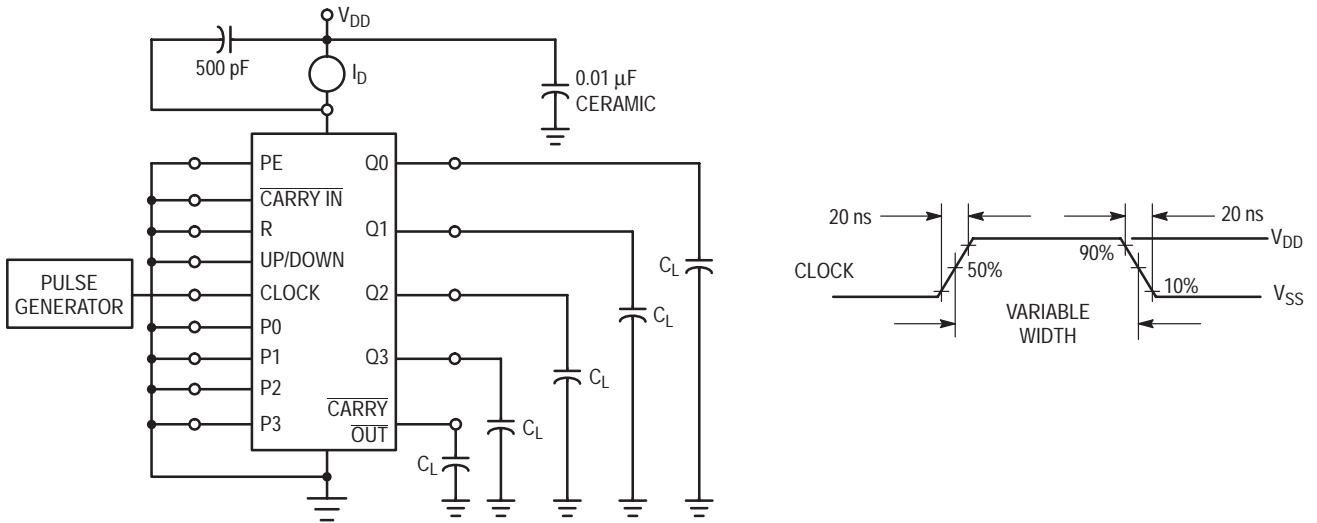
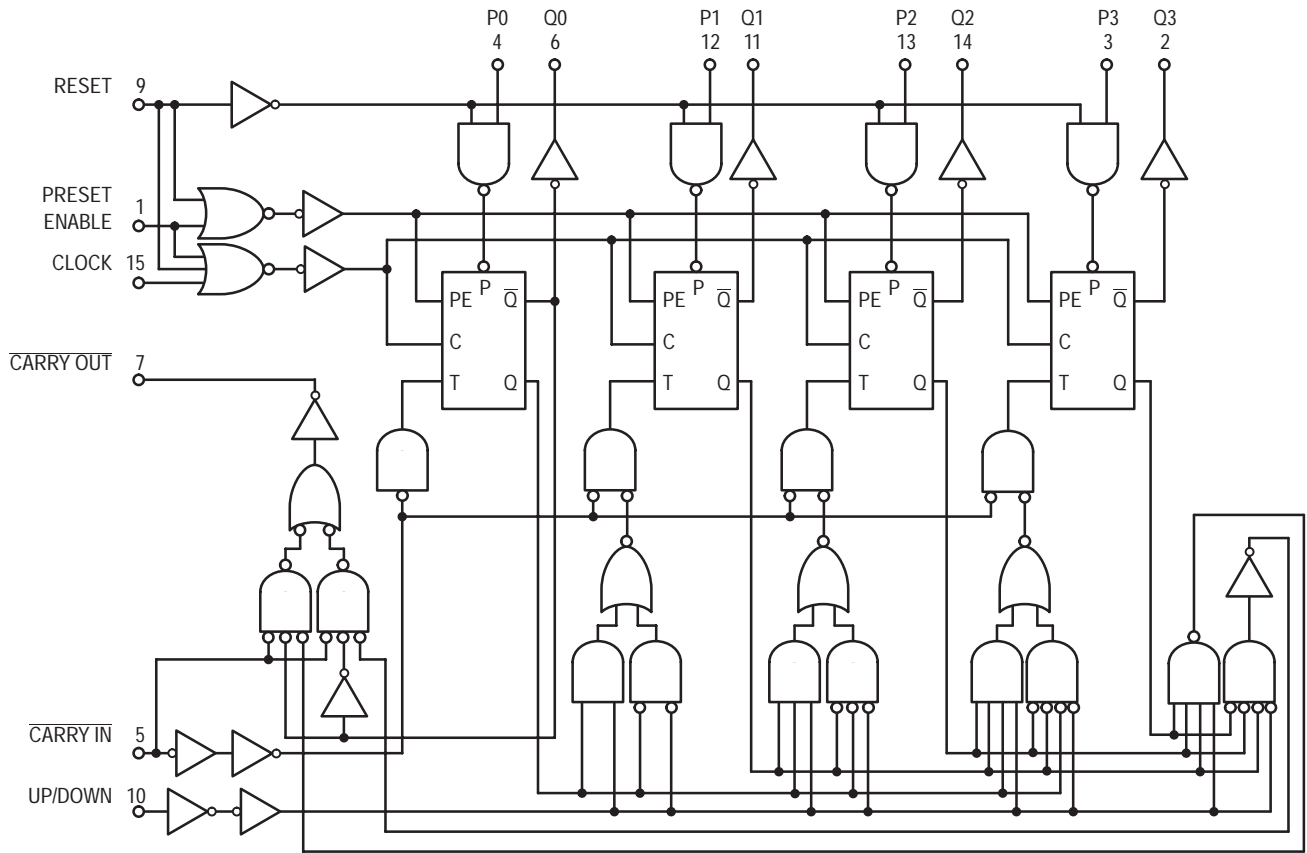


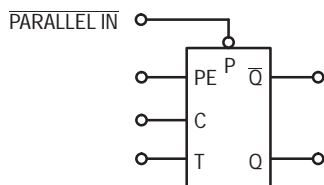
Figure 1. Power Dissipation Test Circuit and Waveform

## LOGIC DIAGRAM



# MC14516B

## TOGGLE FLIP-FLOP



## FLIP-FLOP FUNCTIONAL TRUTH TABLE

Preset Enable	Clock	T	$Q_{n+1}$
1	X	X	Parallel In
0		0	$Q_n$
0		1	$\bar{Q}_n$
0		X	$Q_n$

X = Don't Care

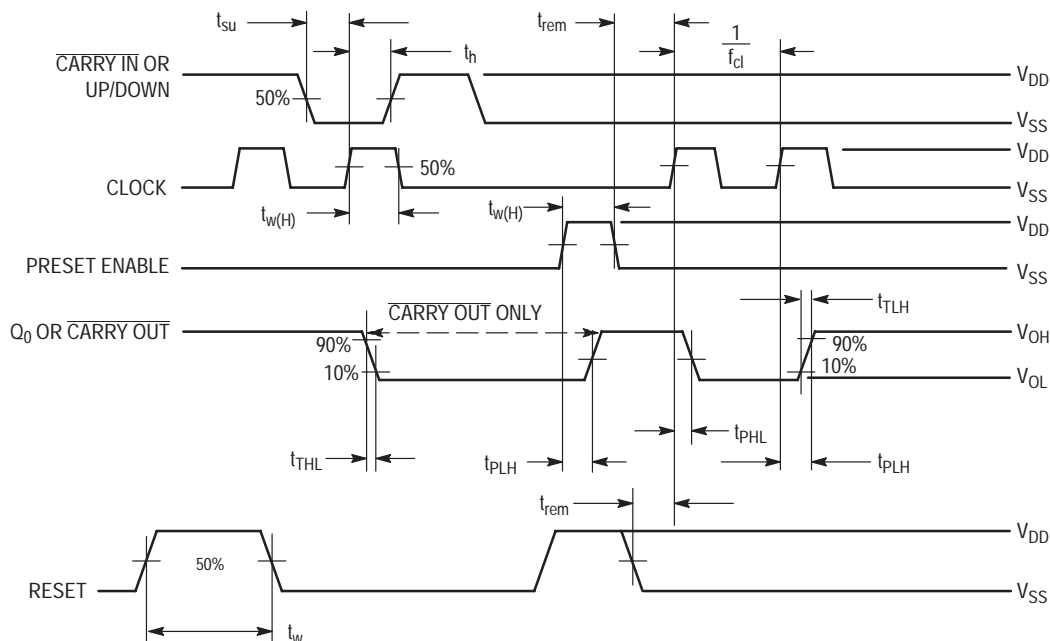


Figure 2. Switching Time Waveforms

## PIN DESCRIPTIONS

### INPUTS

**P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3)** — Data on these inputs is loaded into the counter when PE is taken high.

**Carry In, (Pin 5)** — This active-low input is used when Cascading stages. Carry In is usually connected to  $\bar{C}$ arry Out of the previous stage. While high, Clock is inhibited.

**Clock, (Pin 15)** — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

### OUTPUTS

**Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2)** — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

**Carry Out, (Pin 7)** — Used when cascading stages,  $\bar{C}$ arry Out is usually connected to  $\bar{C}$ arry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

### CONTROLS

**PE, Preset Enable, (Pin 1)** — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

**R, Reset, (Pin 9)** — Asynchronously resets the Q outputs to a low state. This pin is active high and inhibits the clock when high.

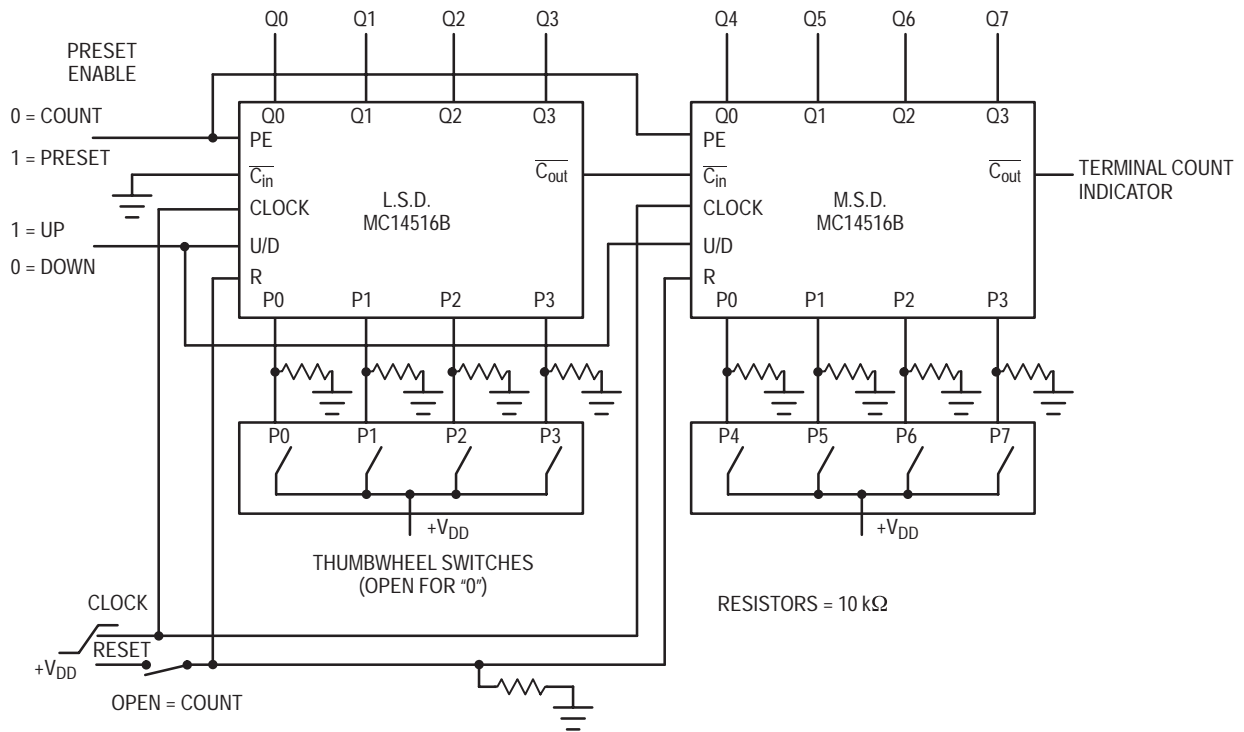
**Up/Down, (Pin 10)** — Controls the direction of count, high for up count, low for down count.

### SUPPLY PINS

**VSS, Negative Supply Voltage, (Pin 8)** — This pin is usually connected to ground.

**VDD, Positive Supply Voltage, (Pin 16)** — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

# MC14516B

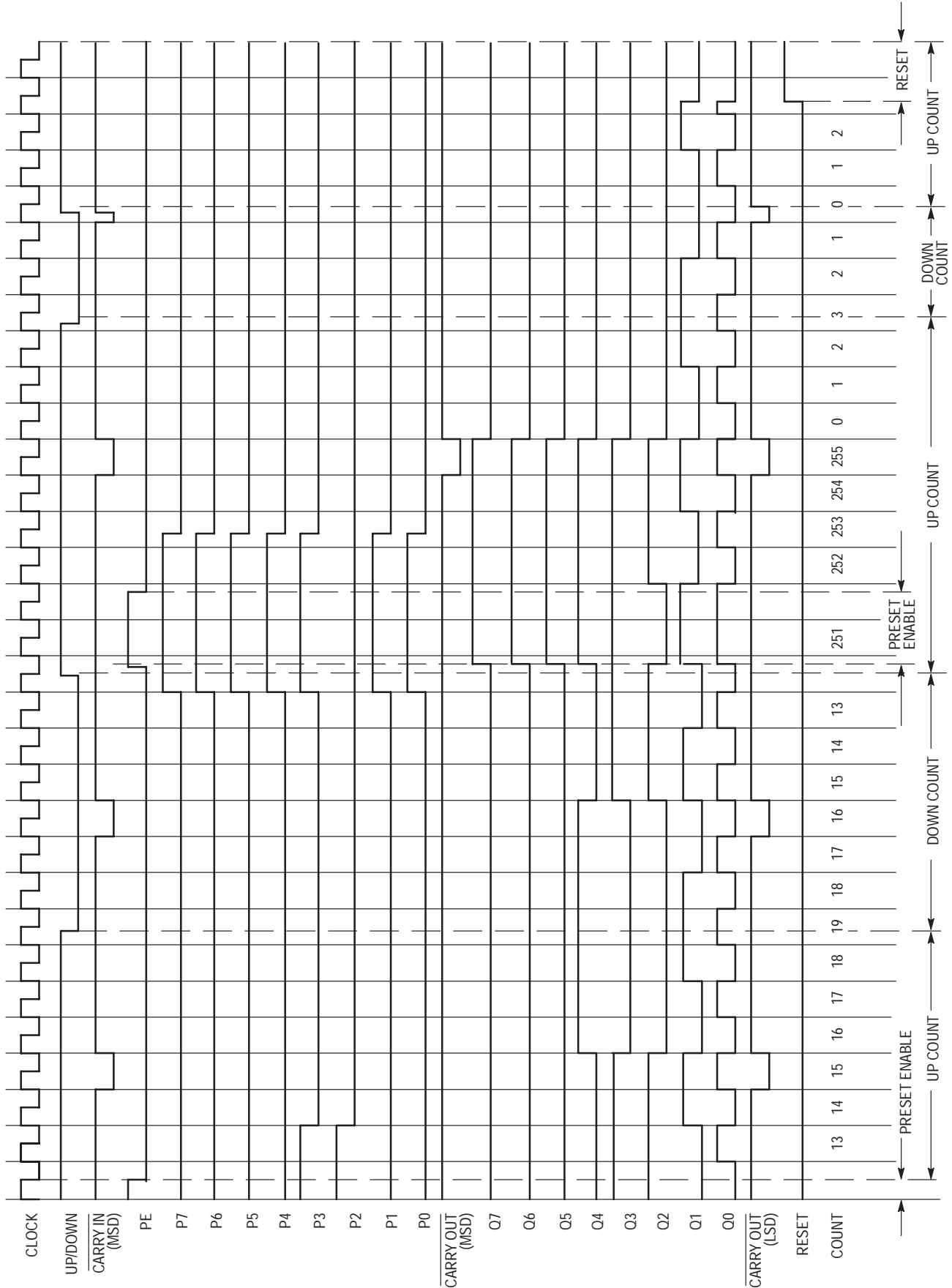


NOTE: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while  $\overline{C_{in}}$  is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode),  $\overline{C_{out}}$  goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

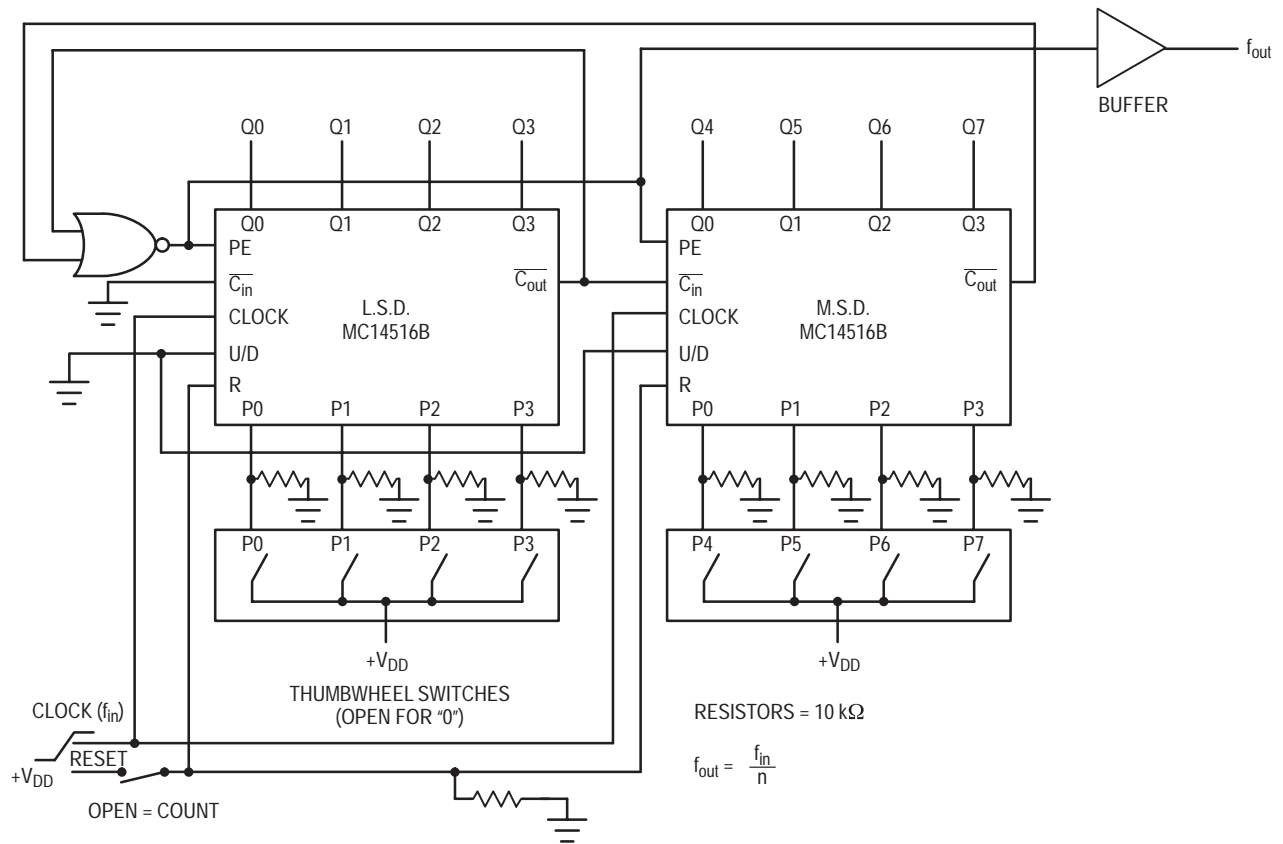
Figure 3. Presettable Cascaded 8-Bit Up/Down Counter

# MC14516B

## TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



# MC14516B



NOTE: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

**Figure 4. Programmable Cascaded Frequency Divider**

# MC14517B

## Dual 64-Bit Static Shift Register

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

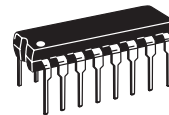
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



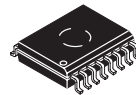
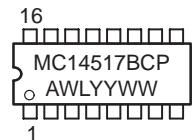
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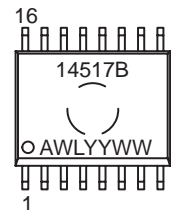


PDIP-16  
P SUFFIX  
CASE 648

### MARKING DIAGRAMS



SOIC-16  
DW SUFFIX  
CASE 751G



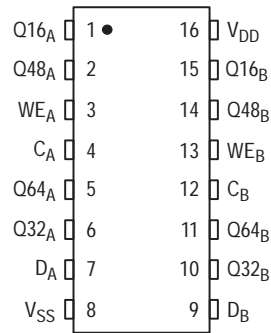
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14517BCP	PDIP-16	2000/Box
MC14517BDW	SOIC-16	47/Rail
MC14517BDWR2	SOIC-16	1000/Tape & Reel

# MC14517B

## PIN ASSIGNMENT



**FUNCTIONAL TRUTH TABLE** (X = Don't Care)

Clock	Write Enable	Data	16-Bit Tap	32-Bit Tap	48-Bit Tap	64-Bit Tap
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
↗	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↗	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
↘	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↘	1	X	High Impedance	High Impedance	High Impedance	High Impedance

# MC14517B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (4.2 μA/kHz) f + I <sub>DD</sub>							μAdc	
		10	I <sub>T</sub> = (8.8 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (13.7 μA/kHz) f + I <sub>DD</sub>								
Three-State Leakage Current	I <sub>TL</sub>	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	μAdc	

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.



# MC14517B

## SWITCHING CHARACTERISTICS (6.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (7.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.65 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 390 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 115 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	475 210 140	770 300 215	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	330 125 100	170 75 60	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.0 6.7 8.3	1.5 4.0 5.3	MHz
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	See Note (8.)			—
Data to Clock Setup Time	$t_{su}$	5.0 10 15	0 10 15	-40 -15 0	— — —	ns
Data to Clock Hold Time	$t_h$	5.0 10 15	150 75 35	75 25 10	— — —	ns
Write Enable to Clock Setup Time	$t_{su}$	5.0 10 15	400 200 110	170 65 50	— — —	ns
Write Enable to Clock Release Time	$t_{rel}$	5.0 10 15	380 180 100	160 55 40	— — —	ns

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

8. When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

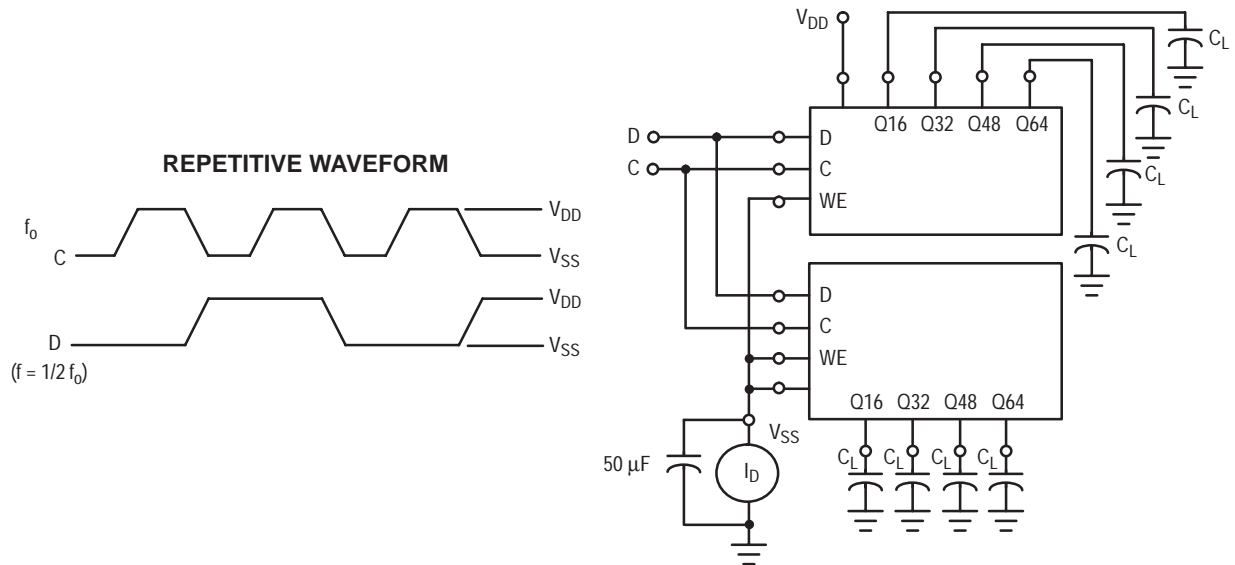
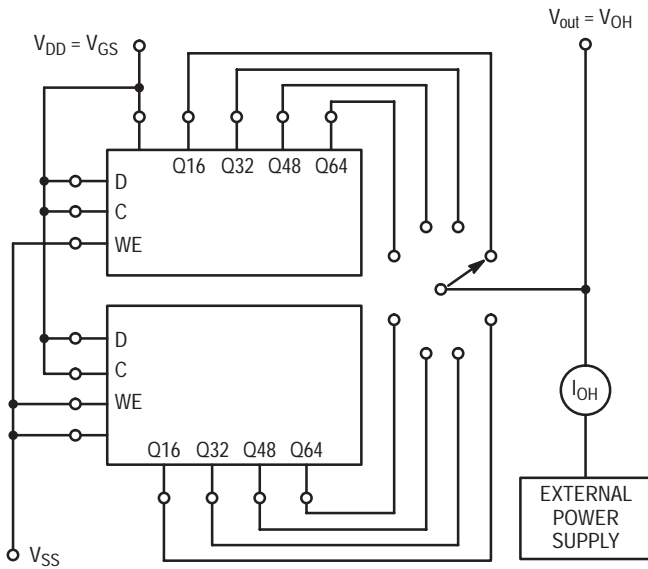


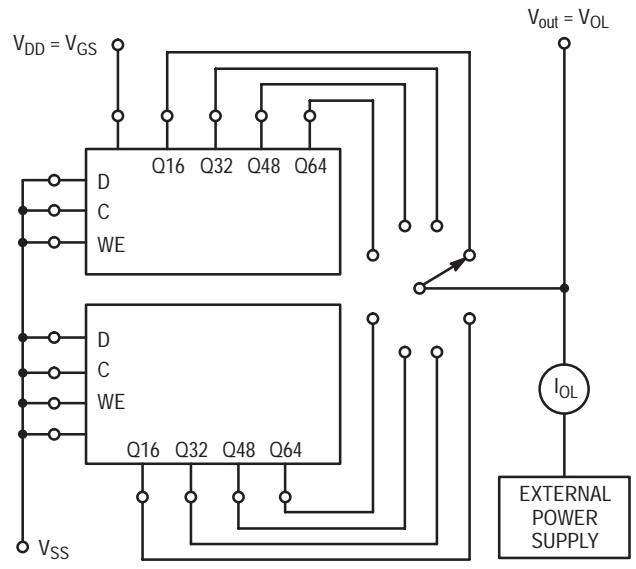
Figure 1. Power Dissipation Test Circuit and Waveform

# MC14517B



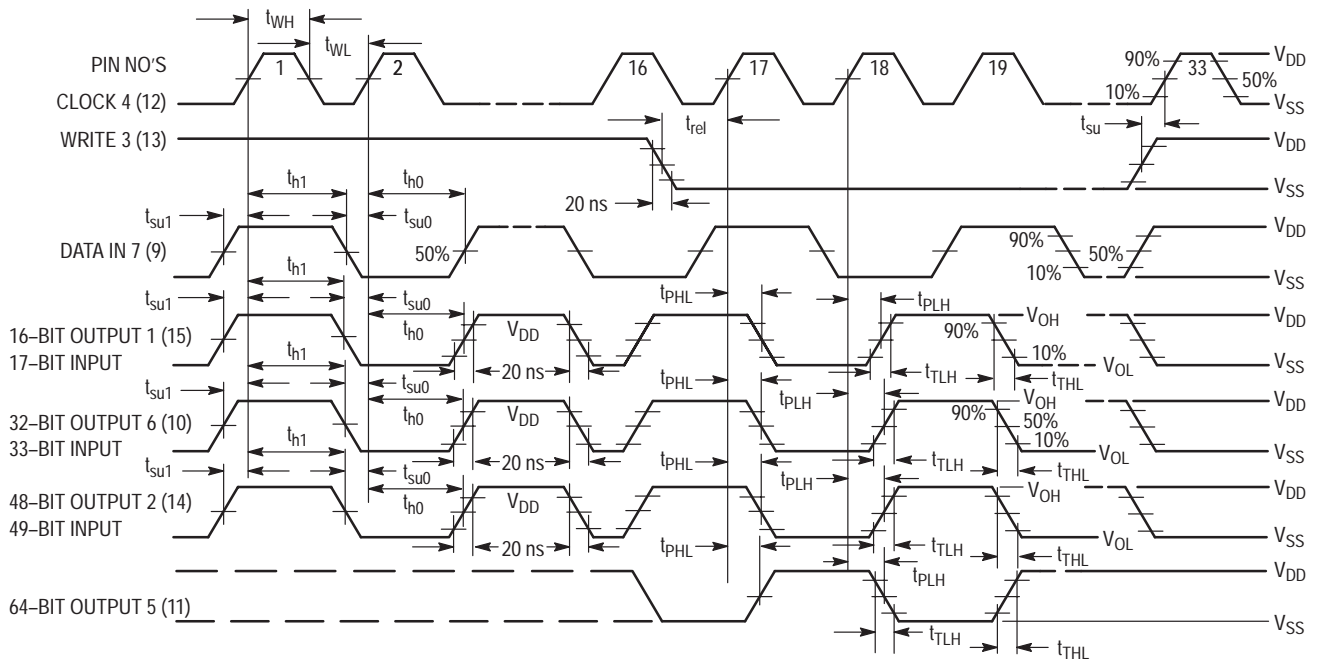
(Output being tested should be in the high-logic state)

**Figure 2. Typical Output Source Current Characteristics Test Circuit**



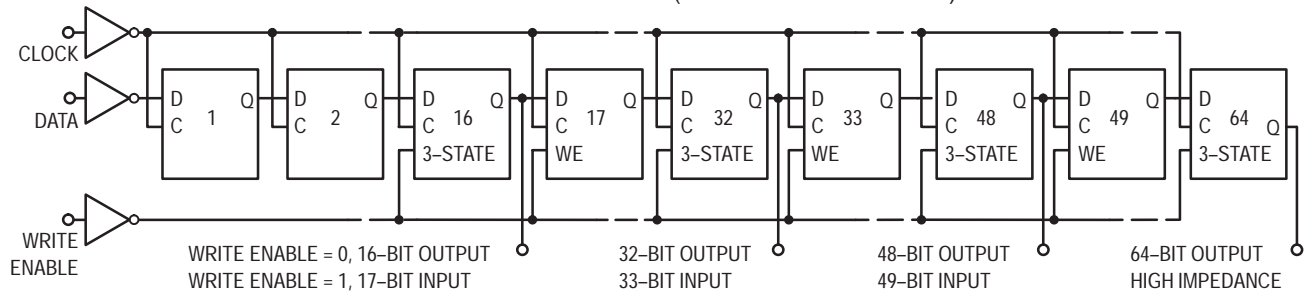
(Output being tested should be in the low-logic state)

**Figure 3. Typical Output Sink Current Characteristics Test Circuit**



**Figure 4. AC Test Waveforms**

## EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



# MC14518B

## Dual Up Counters

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

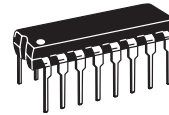
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



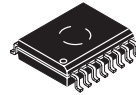
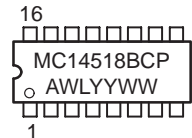
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<http://onsemi.com>

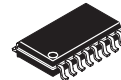
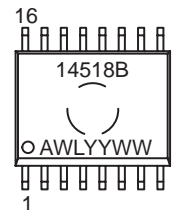


PDIP-16  
P SUFFIX  
CASE 648

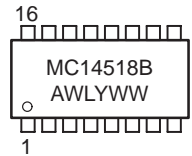
### MARKING DIAGRAMS



SOIC-16  
DW SUFFIX  
CASE 751G



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

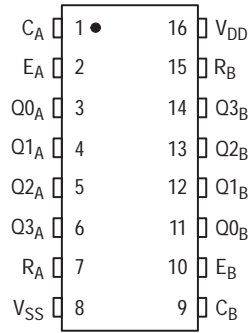
### ORDERING INFORMATION

Device	Package	Shipping
MC14518BCP	PDIP-16	2000/Box
MC14518BDW	SOIC-16	47/Rail
MC14518BDWR2	SOIC-16	1000/Tape & Reel
MC14518BF	SOEIAJ-16	See Note 1.
MC14518BFEL	SOEIAJ-16	See Note 1.

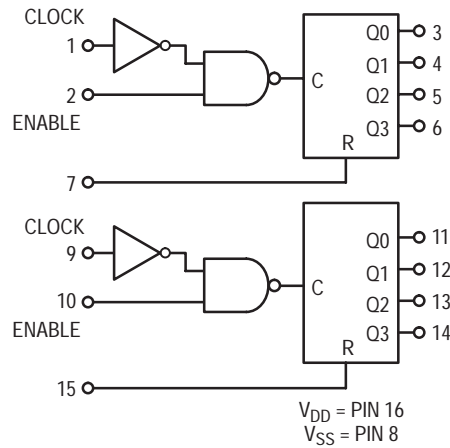
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14518B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## TRUTH TABLE

Clock	Enable	Reset	Action
↗	1	0	Increment Counter
0	↘	0	Increment Counter
↘	X	0	No Change
X	↗	0	No Change
↗	0	0	No Change
1	↘	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

# MC14518B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
$V_{in} = 0$ or $V_{DD}$	"1" Level $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)	"0" Level $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)	Source $I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc	
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (0.6 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc	
10	$I_T = (1.2 \mu\text{A/kHz}) f + I_{DD}$										
15	$I_T = (1.7 \mu\text{A/kHz}) f + I_{DD}$										

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.002$ .

# MC14518B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q/Enable to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$  Reset to Q $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 95 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$        $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	280 115 80  330 130 90	560 230 160  650 230 170	ns
Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	200 100 70	100 50 35	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.5 6.0 8.0	1.5 3.0 4.0	MHz
Clock or Enable Rise and Fall Time	$t_{THL}$ , $t_{TLH}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Enable Pulse Width	$t_{WH(E)}$	5.0 10 15	440 200 140	220 100 70	— — —	ns
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	280 120 90	125 55 40	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	-5 15 20	-45 -15 -5	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

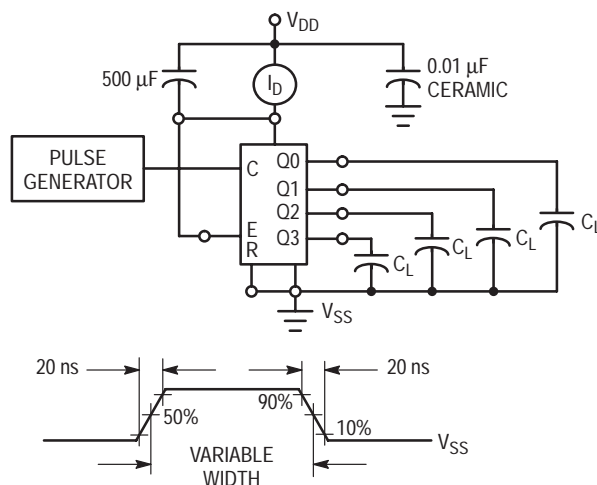


Figure 1. Power Dissipation Test Circuit and Waveform

# MC14518B

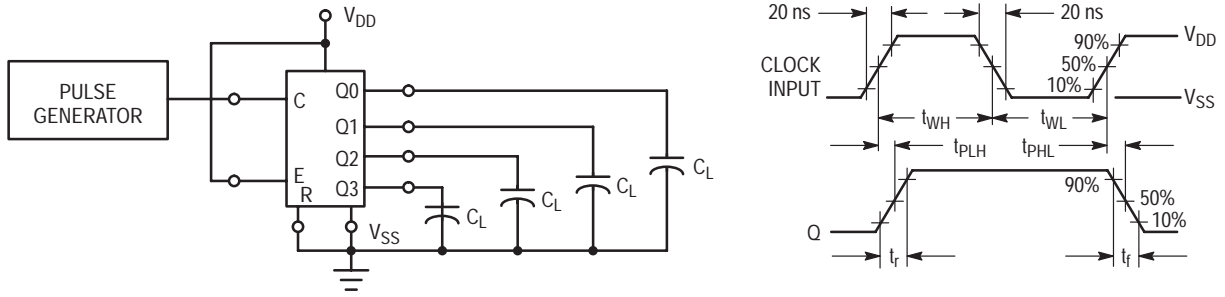


Figure 2. Switching Time Test Circuit and Waveforms

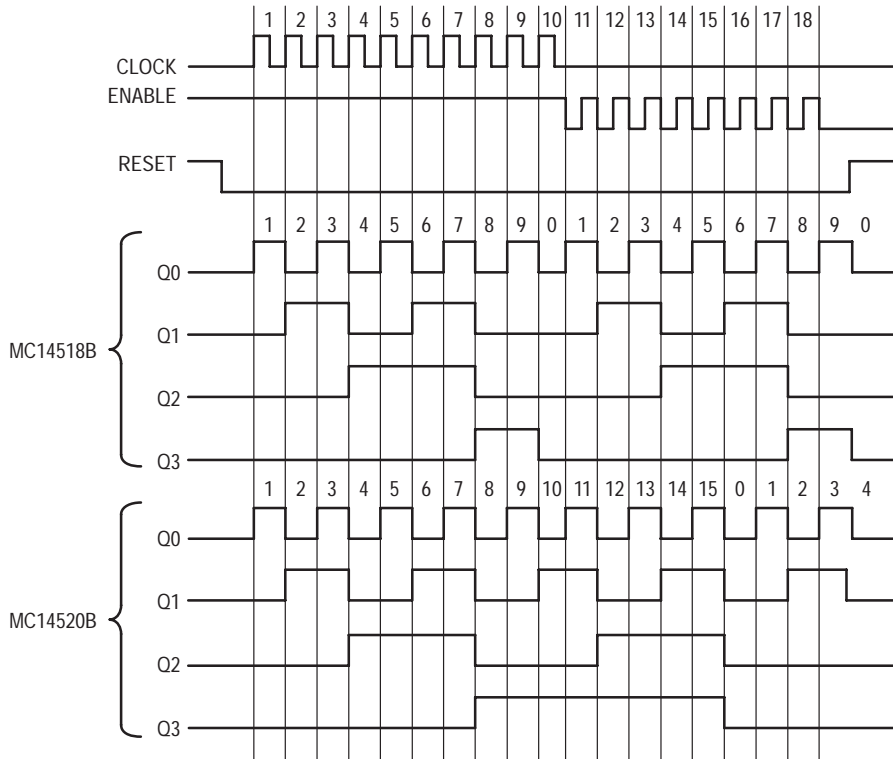


Figure 3. Timing Diagram

# MC14518B

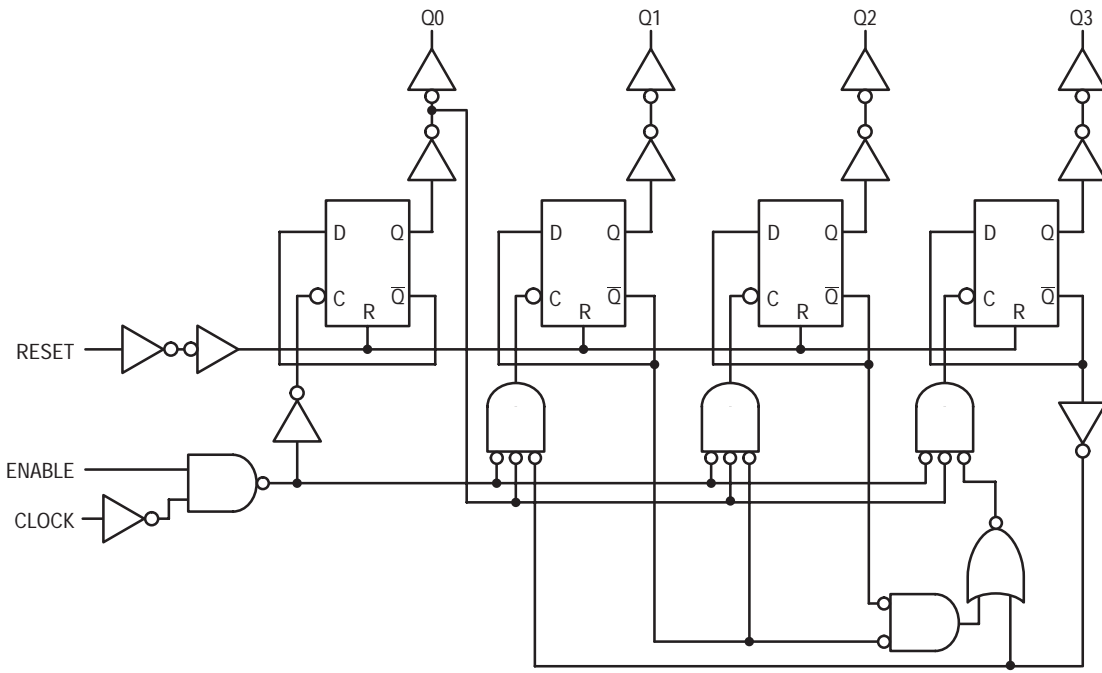


Figure 4. Decade Counter (MC14518B) Logic Diagram  
(1/2 of Device Shown)

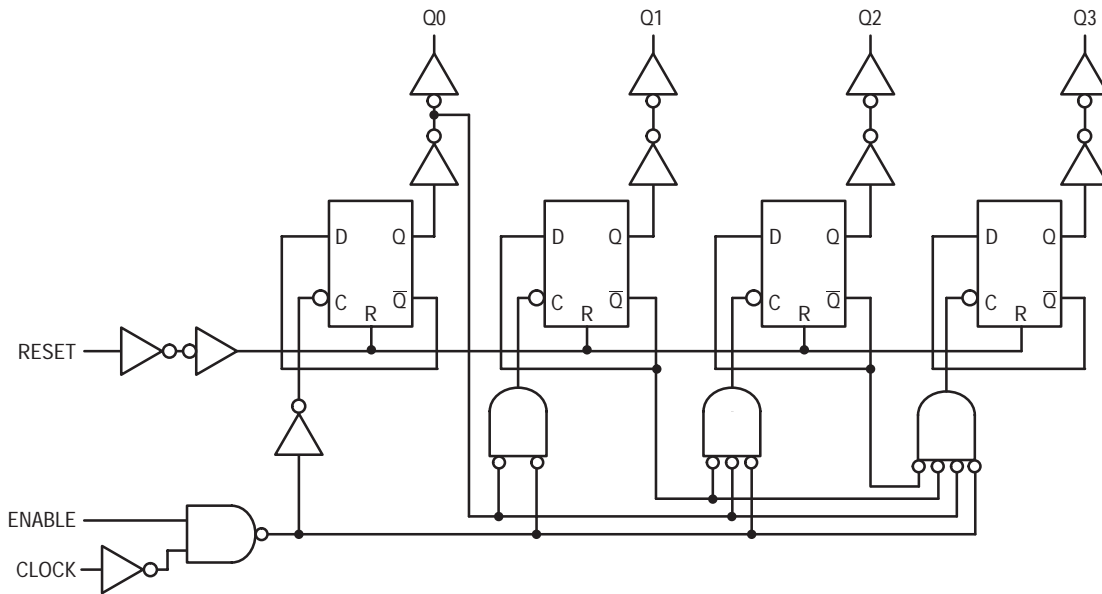


Figure 5. Binary Counter (MC14520B) Logic Diagram  
(1/2 of Device Shown)



# MC14521B

## 24-Stage Frequency Divider

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to  $2^{24} = 16,777,216$ . The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- $V_{DD}'$  and  $V_{SS}'$  Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

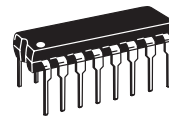
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



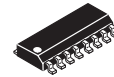
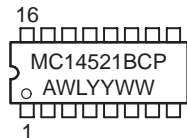
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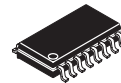
### MARKING DIAGRAMS



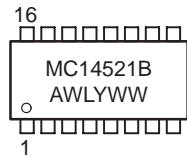
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

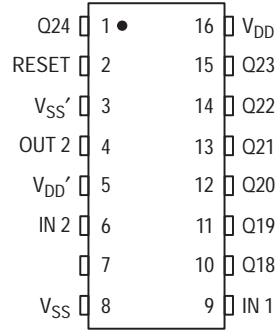
### ORDERING INFORMATION

Device	Package	Shipping
MC14521BCP	PDIP-16	2000/Box
MC14521BD	SOIC-16	48/Rail
MC14521BDR2	SOIC-16	2500/Tape & Reel
MC14521BF	SOEIAJ-16	See Note 1.
MC14521BFEL	SOEIAJ-16	See Note 1.
MC14521BFR2	SOEIAJ-16	See Note 1.

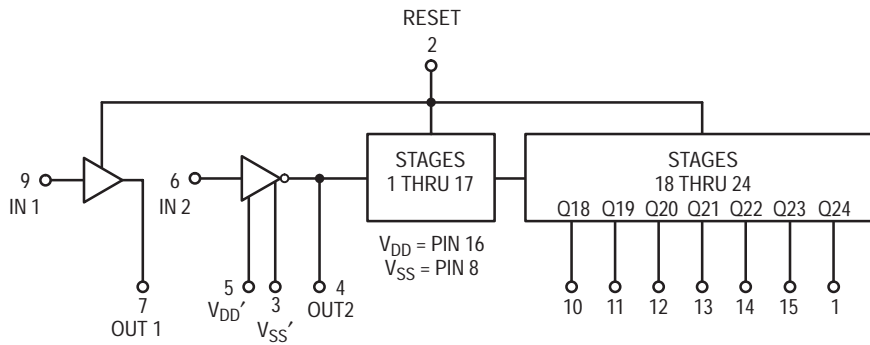
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14521B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



Output	Count Capacity
Q18	2 <sup>18</sup> = 262,144
Q19	2 <sup>19</sup> = 524,288
Q20	2 <sup>20</sup> = 1,048,576
Q21	2 <sup>21</sup> = 2,097,152
Q22	2 <sup>22</sup> = 4,194,304
Q23	2 <sup>23</sup> = 8,388,608
Q24	2 <sup>24</sup> = 16,777,216

# MC14521B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 4 & 7 (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) Pins 1, 10, (V <sub>OH</sub> = 9.5 Vdc) 11, 12, 13, 14 (V <sub>OH</sub> = 13.5 Vdc) and 15  (V <sub>OL</sub> = 0.4 Vdc) Sink (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
		15	-1.8	—	-1.5	-3.5	—	-1.1	—		
		5.0	-3.0	—	-2.4	-4.2	—	-1.7	—		mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
		5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.42 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.85 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.40 μA/kHz) f + I <sub>DD</sub>							μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.003.

# MC14521B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time (Counter Outputs) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q18 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 4415 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 1667 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1275 \text{ ns}$ Clock to Q24 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2167 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1675 \text{ ns}$	$t_{PHL}, t_{PLH}$	5.0 10 15  5.0 10 15	— — —  — — —	4.5 1.7 1.3  6.0 2.2 1.7	9.0 3.5 2.7  12 4.5 3.5	$\mu\text{s}$
Propagation Delay Time Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1215 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 467 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 350 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	1300 500 375	2600 1000 750	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	385 150 120	140 55 40	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.5 9.0 12	2.0 5.0 6.5	MHz
Clock Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1400 600 450	700 300 225	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	30 0 -40	-200 -160 -110	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

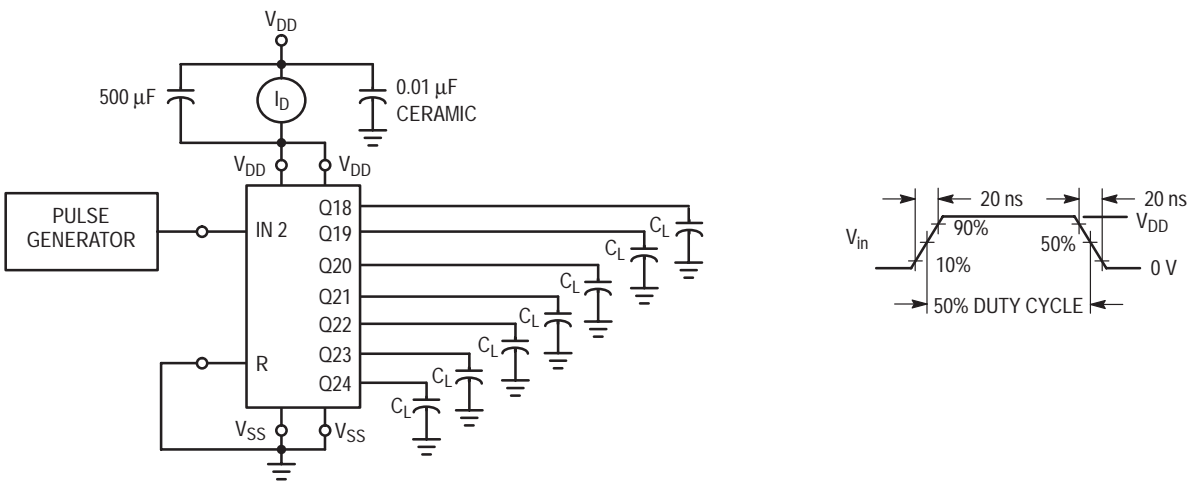


Figure 1. Power Dissipation Test Circuit and Waveform

# MC14521B

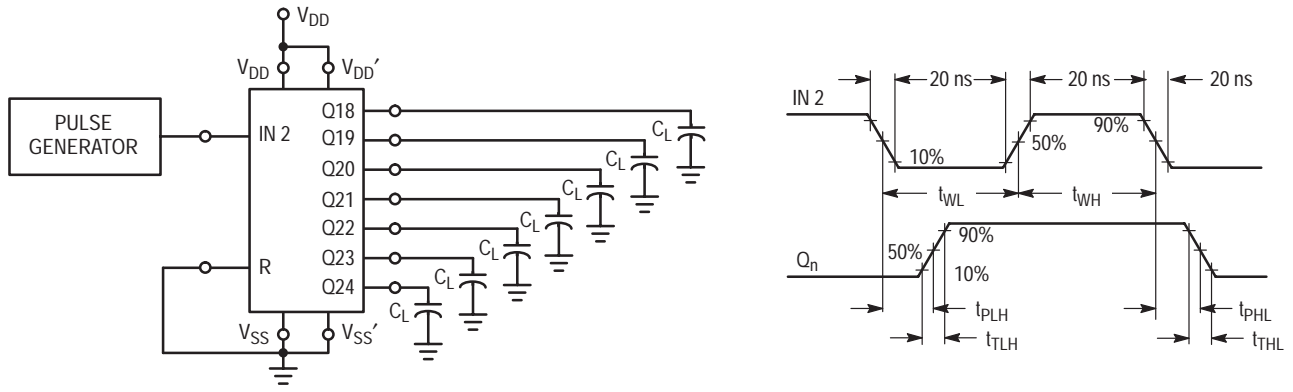
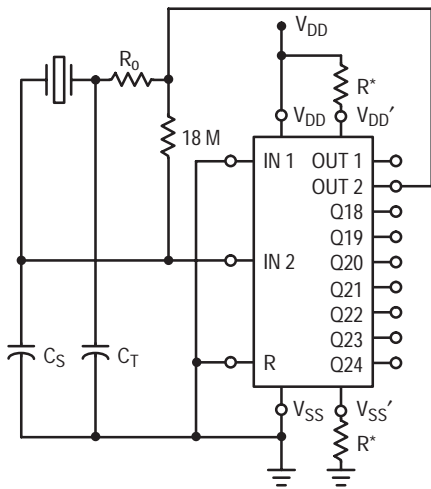


Figure 2. Switching Time Test Circuit and Waveforms



\*Optional for low power operation,  
 $10 \text{ k}\Omega \leq R \leq 70 \text{ k}\Omega$ .

Figure 3. Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	50 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, $R_S$	1.0	6.2	$\text{k}\Omega$
External Resistor/Capacitor Values			
$R_o$	47	750	$\text{k}\Omega$
$C_T$	82	82	pF
$C_S$	20	20	pF
Frequency Stability			
Frequency Change as a Function of $V_{DD}$ ( $T_A = 25^\circ\text{C}$ )			
$V_{DD}$ Change from 5.0 V to 10 V	+ 6.0	+ 2.0	ppm
$V_{DD}$ Change from 10 V to 15 V	+ 2.0	+ 2.0	ppm
Frequency Change as a Function of Temperature ( $V_{DD} = 10 \text{ V}$ )			
$T_A$ Change from $-55^\circ\text{C}$ to $+25^\circ\text{C}$	- 4.0	- 2.0	ppm
MC14521 only	+ 100	+ 120	ppm
Complete Oscillator*			
$T_A$ Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$	- 2.0	- 2.0	ppm
MC14521 only	- 160	- 560	ppm
Complete Oscillator*			

\*Complete oscillator includes crystal, capacitors, and resistors.

Figure 4. Typical Data for Crystal Oscillator Circuit

# MC14521B

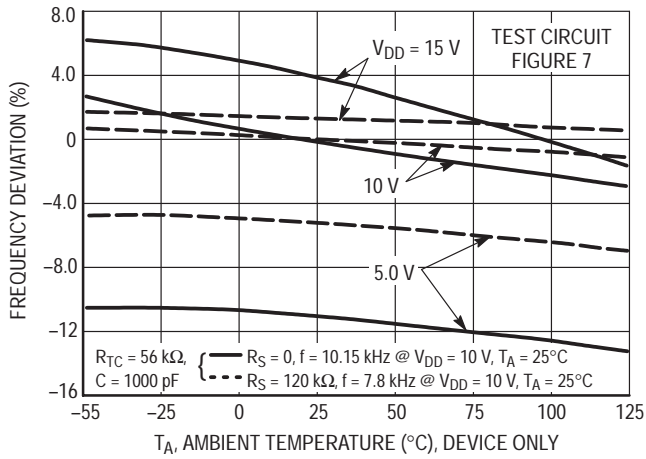


Figure 5. RC Oscillator Stability

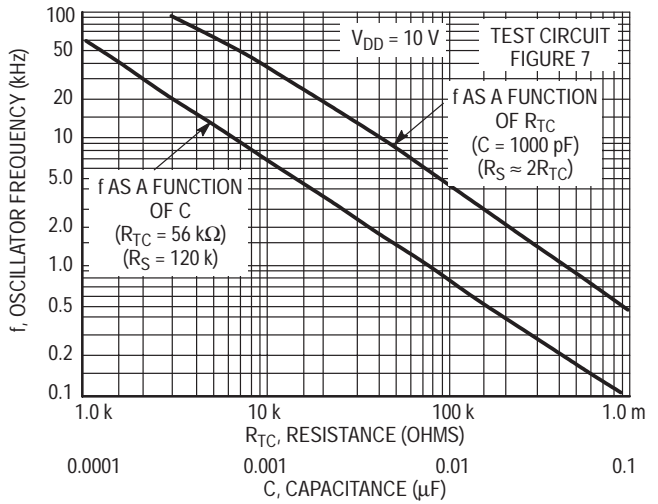


Figure 6. RC Oscillator Frequency as a Function of  $R_{TC}$  and  $C$

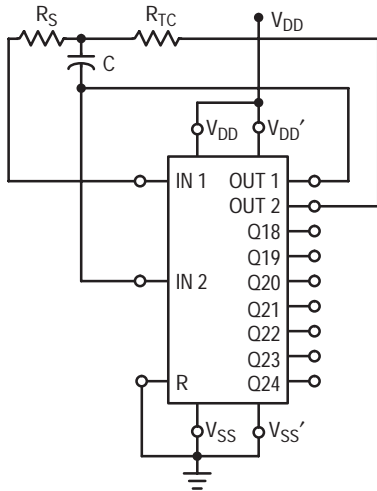


Figure 7. RC Oscillator Circuit

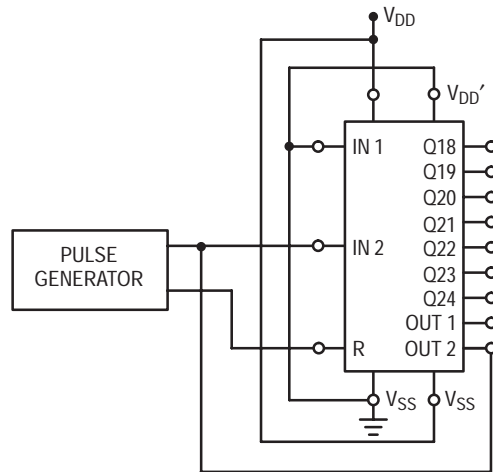


Figure 8. Functional Test Circuit

# MC14521B

## FUNCTIONAL TEST SEQUENCE

	Inputs		Outputs			Comments			
	Reset	In 2	Out 2	V <sub>SS</sub> '	V <sub>DD</sub> '		Q18 thru Q24		
<p>A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.</p>	1	0	0	V <sub>DD</sub>	Gnd	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together.		
	0	1	1				First "0" to "1" transition on In 2, Out 2 node.		
	0	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.		
	1	1	1				1	The 255th "0" to "1" transition.	
	0	0	0				1	1	
	1	0	0				1	1	Counter converted back to 24-stages in series mode.
	1	0	0				1	1	Out 2 converts back to an output.
	0	1	1				0	0	Counter ripples from an all "1" state to an all "0" stage.





# MC14526B

## Presettable 4-Bit Down Counters

The MC14526B binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

This device is presettable, cascadable, synchronous down counter with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

This complementary MOS counter can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

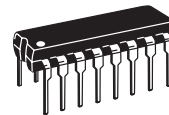
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



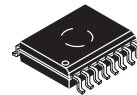
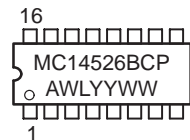
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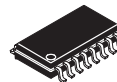
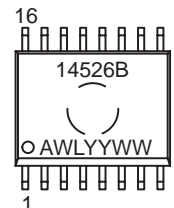


PDIP-16  
P SUFFIX  
CASE 648

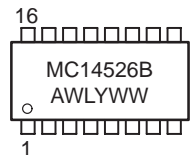
### MARKING DIAGRAMS



SOIC-16  
DW SUFFIX  
CASE 751G



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

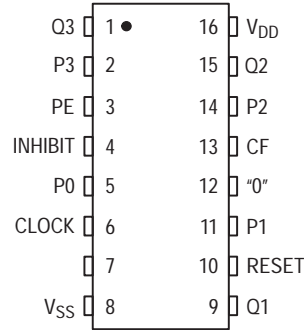
### ORDERING INFORMATION

Device	Package	Shipping
MC14526BCP	PDIP-16	2000/Box
MC14526BDW	SOIC-16	47/Rail
MC14526BDWR2	SOIC-16	1000/Tape & Reel
MC14526BF	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14526B

## PIN ASSIGNMENT



## FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
	L	H	L	X	L	Decrement inhibited
L	L		L	X	L	Decrement inhibited
	L	L	L	L	L	No change** (inactive edge)
H	L		L	L	L	No change** (inactive edge)
	L	L	L	L	L	Decrement**
H	L		L	L	L	Decrement**

X = Don't Care

NOTES:

\* Output "0" is low when reset goes high only if PE and CF are low.

\*\* Output "0" is high when reset is low, only if CF is high and count is 0000.

# MC14526B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.7 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.4 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.1 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14526B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$ (Figures 4, 5)	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time (Inhibit Used as Negative Edge Clock) Clock or Inhibit to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$ Clock or Inhibit to "0" $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 155 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$ (Figures 4, 5, 6)	5.0 10 15  5.0 10 15	— — —  — — —	550 225 160  240 130 100	1100 450 320  480 260 200	ns
Propagation Delay Time Pn to Q	$t_{PLH}$ , $t_{PHL}$ (Figures 4, 7)	5.0 10 15	— — —	260 120 100	520 240 200	ns
Propagation Delay Time Reset to Q	$t_{PHL}$  (Figure 8)	5.0 10 15	— — —	250 110 80	500 220 160	ns
Propagation Delay Time Preset Enable to "0"	$t_{PHL}$ , $t_{PLH}$ (Figures 4, 9)	5.0 10 15	— — —	220 100 80	440 200 160	ns
Clock or Inhibit Pulse Width	$t_w$  (Figures 5, 6)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Frequency (with PE = low)	$f_{max}$  (Figures 4, 5, 6)	5.0 10 15	— — —	2.0 5.0 6.6	1.5 3.0 4.0	MHz
Clock or Inhibit Rise and Fall Time	$t_r$ , $t_f$ (Figures 5, 6)	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Setup Time Pn to Preset Enable	$t_{su}$  (Figure 10)	5.0 10 15	90 50 40	40 15 10	— — —	ns
Hold Time Preset Enable to Pn	$t_h$  (Figure 10)	5.0 10 15	30 30 30	-15 -5 0	— — —	ns
Preset Enable Pulse Width	$t_w$  (Figure 10)	5.0 10 15	250 100 80	125 50 40	— — —	ns
Reset Pulse Width	$t_w$  (Figure 8)	5.0 10 15	350 250 200	175 125 100	— — —	ns
Reset Removal Time	$t_{rem}$  (Figure 8)	5.0 10 15	10 20 30	-110 -30 -20	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

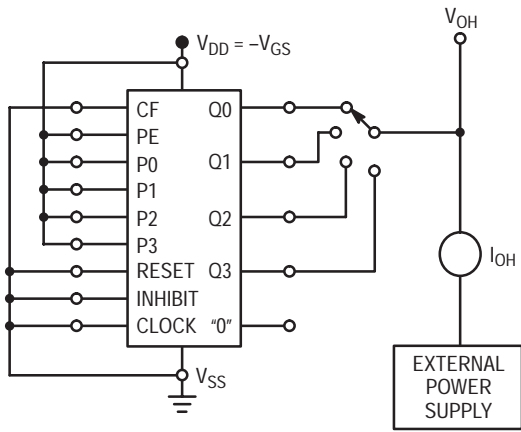


Figure 1. Typical Output Source Characteristics Test Circuit

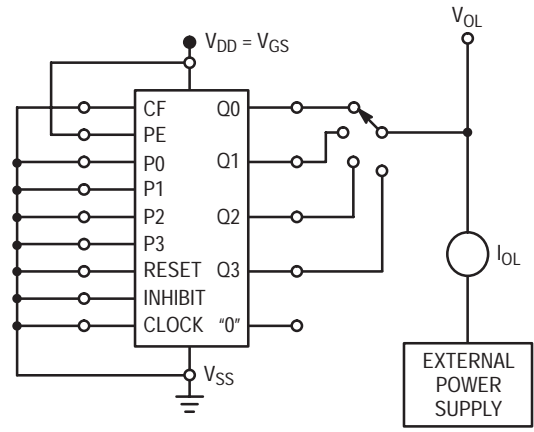


Figure 2. Typical Output Sink Characteristics Test Circuit

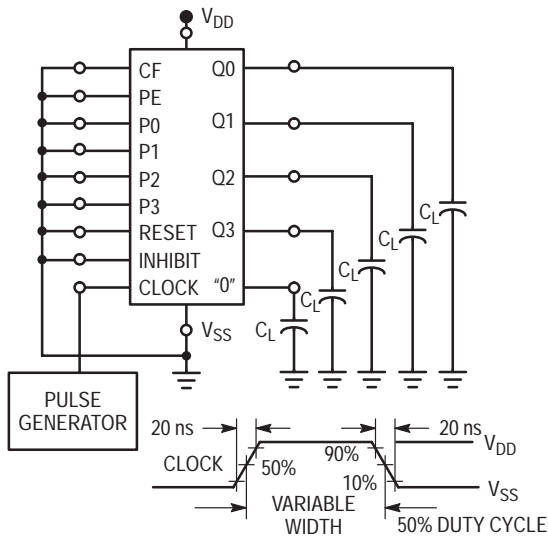
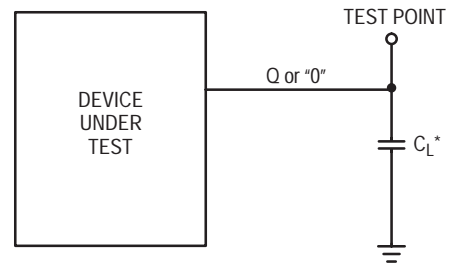


Figure 3. Power Dissipation



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

SWITCHING WAVEFORMS

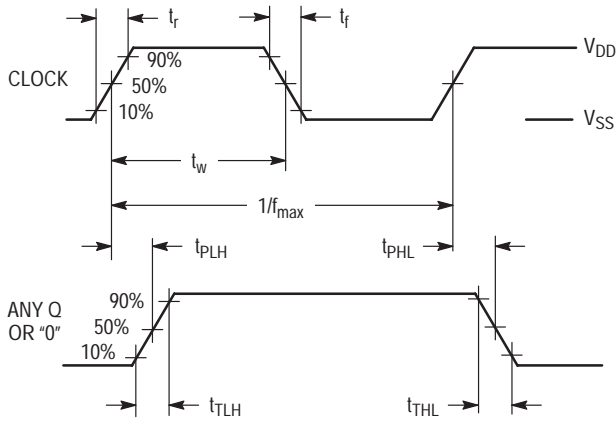


Figure 5.

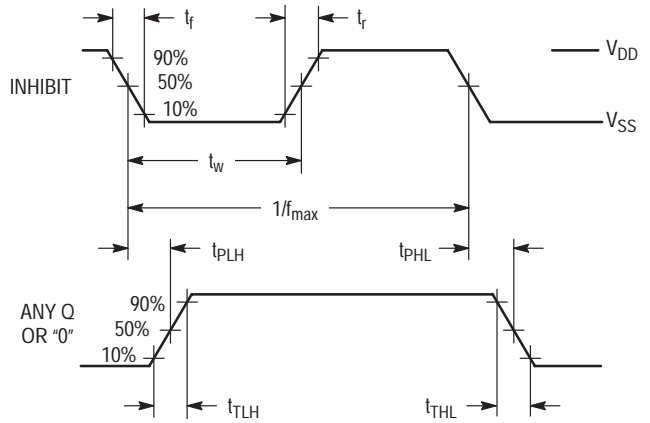


Figure 6.

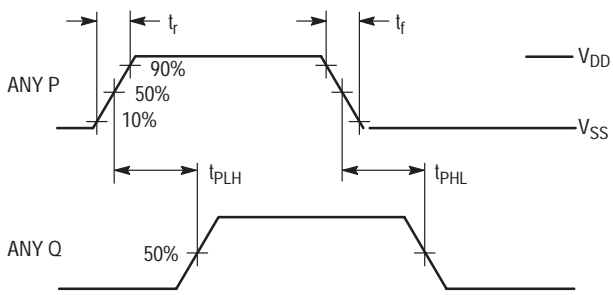


Figure 7.

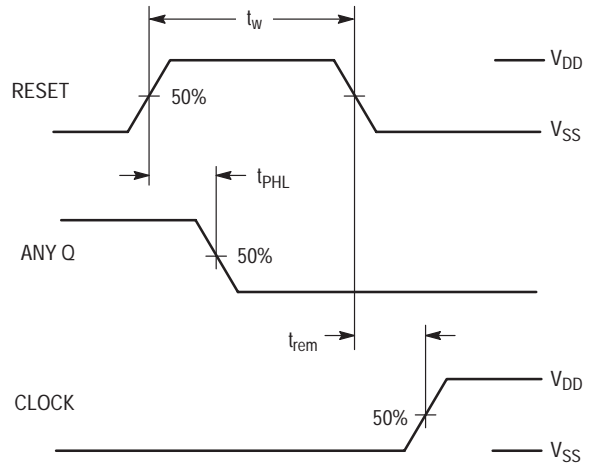


Figure 8.

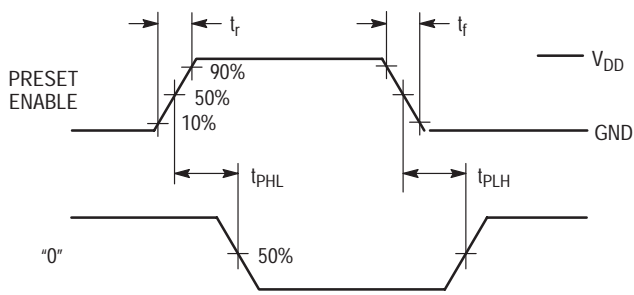


Figure 9.

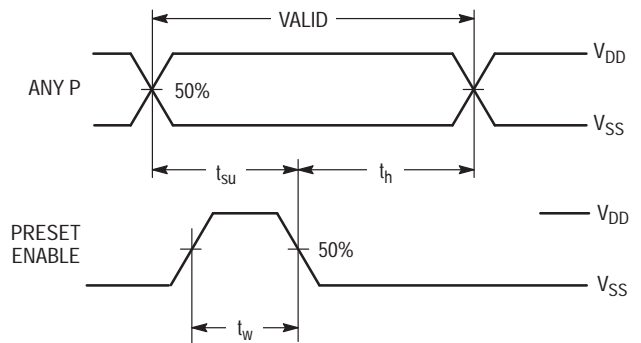


Figure 10.

## PIN DESCRIPTIONS

**Preset Enable (Pin 3)** — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

**Inhibit (Pin 4)** — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

**Clock (Pin 6)** — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

**Reset (Pin 10)** — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the “0” output to go high.

**“0” (Pin 12)** — The “0” (Zero) output issues a pulse one clock period wide when the counter reaches terminal count ( $Q0 = Q1 = Q2 = Q3 = \text{low}$ ) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value

other than all zeroes, the “0” output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

**Cascade Feedback (Pin 13)** — If the Cascade Feedback input is high, a high level is generated at the “0” output when the count is all zeroes. If Cascade Feedback is low, the “0” output depends on the Preset Enable input level. See the Function Table.

**P0, P1, P2, P3 (Pins 5, 11, 14, 2)** — These are the preset data inputs. P0 is the LSB.

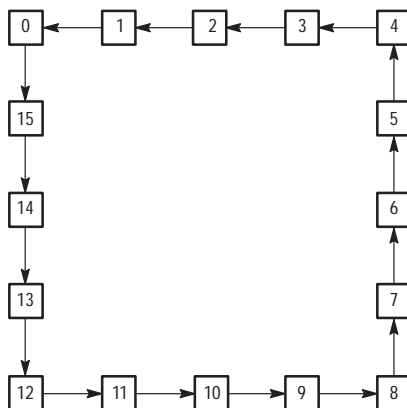
**Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1)** — These are the synchronous counter outputs. Q0 is the LSB.

**V<sub>SS</sub> (Pin 8)** — The most negative power supply potential. This pin is usually ground.

**V<sub>DD</sub> (Pin 16)** — The most positive power supply potential. V<sub>DD</sub> may range from 3 to 18 V with respect to V<sub>SS</sub>.

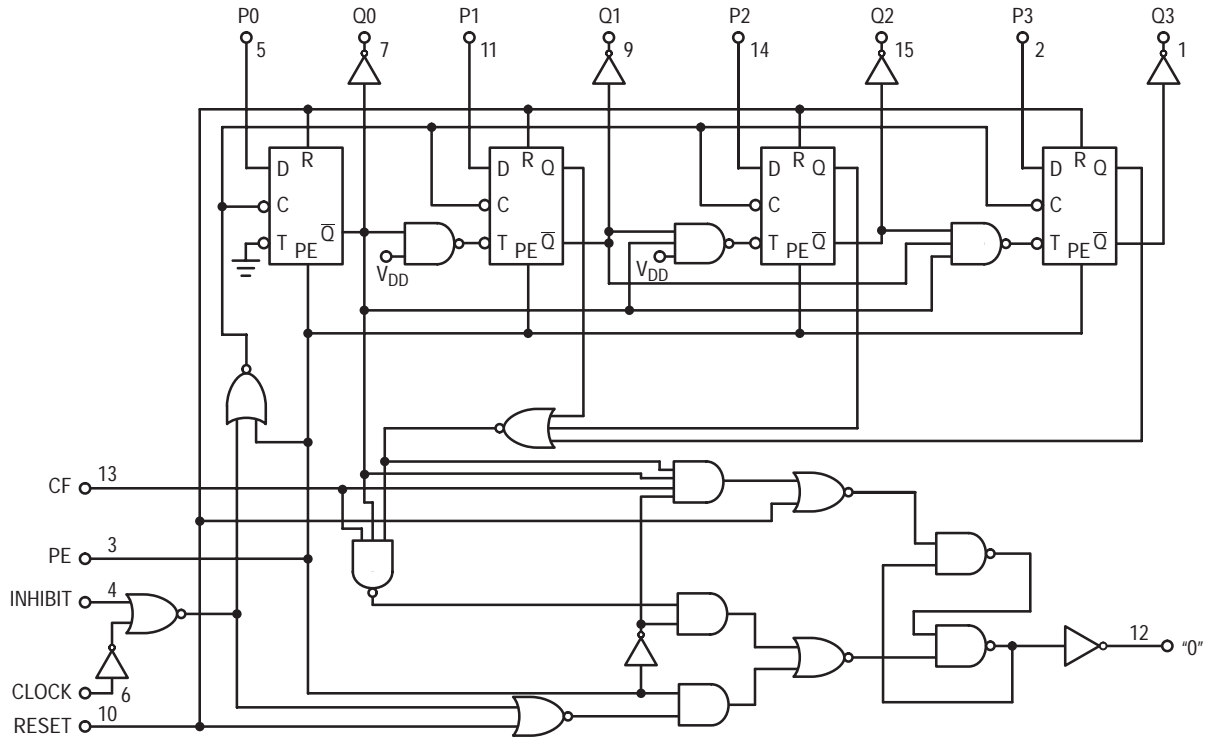
## STATE DIAGRAM

MC14526B



# MC14526B

## MC14526B LOGIC DIAGRAM (Binary Down Counter)





APPLICATIONS INFORMATION

Divide-By-N, Single Stage

Figure 11 shows a single stage divide-by-N application.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide-By-N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non-zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. N = 1).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

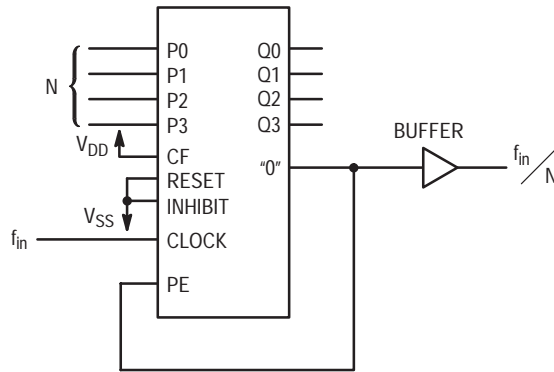


Figure 11. ÷ N Counter

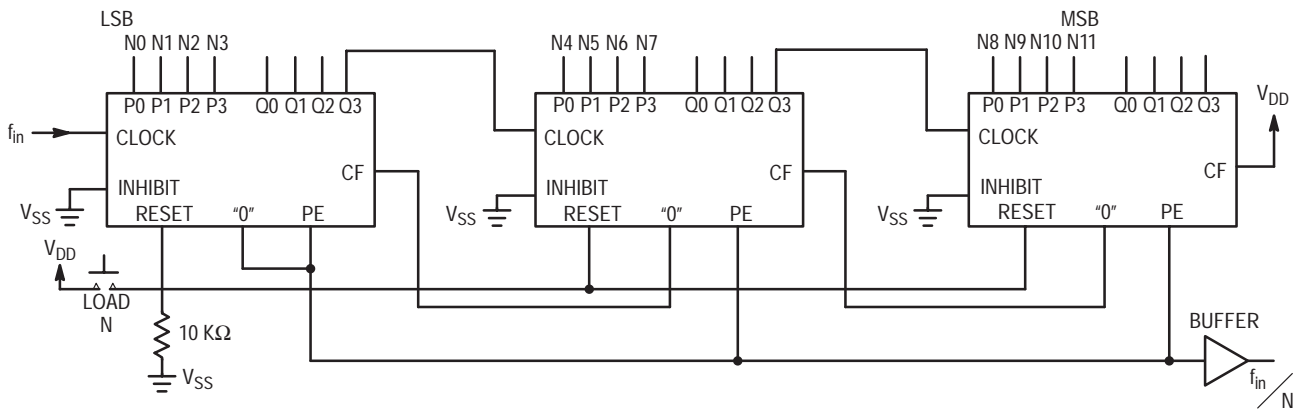


Figure 12. 3 Stages Cascaded

# MC14528B

## Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components,  $C_X$  and  $R_X$ .

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

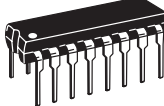
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor

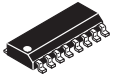
<http://onsemi.com>

### MARKING DIAGRAMS



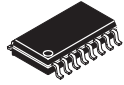
**PDIP-16**  
**P SUFFIX**  
**CASE 648**

16  
□□□□□□□□  
MC14528BCP  
○ AWLYYYWW  
□□□□□□□□  
1



**SOIC-16**  
**D SUFFIX**  
**CASE 751B**

16  
□□□□□□□□  
14528B  
○ AWLYYYWW  
□□□□□□□□  
1



**SOEIAJ-16**  
**F SUFFIX**  
**CASE 966**

16  
□□□□□□□□  
MC14528B  
AWLYYYWW  
○  
□□□□□□□□  
1

A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

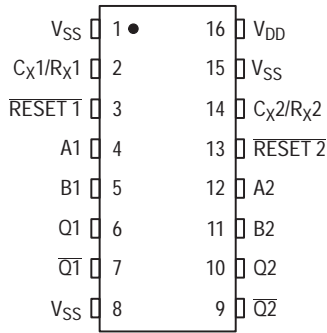
### ORDERING INFORMATION

Device	Package	Shipping
MC14528BCP	PDIP-16	2000/Box
MC14528BD	SOIC-16	48/Rail
MC14528BDR2	SOIC-16	2500/Tape & Reel
MC14528BF	SOEIAJ-16	See Note 1.
MC14528BFEL	SOEIAJ-16	See Note 1.

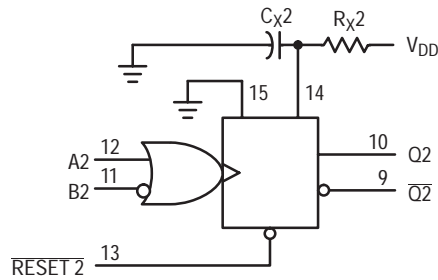
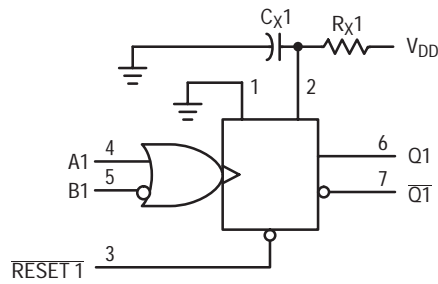
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14528B

## PIN ASSIGNMENT

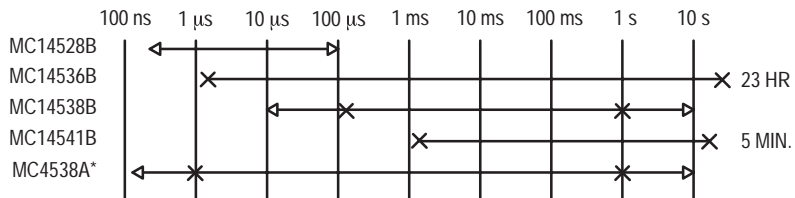


## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
 V<sub>SS</sub> = PIN 1, PIN 8, PIN 15  
 R<sub>X</sub> AND C<sub>X</sub> ARE EXTERNAL COMPONENTS

## ONE-SHOT SELECTION GUIDE



\*LIMITED OPERATING VOLTAGE (2-6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ←————→  
 RECOMMENDED PULSE WIDTH RANGE ×————×

# MC14528B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current at an external load Capacitance (C <sub>L</sub> ) and at external timing capacitance (C <sub>X</sub> ), use the formula — (5.)	I <sub>T</sub>	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2] \times 10^{-3}$ where: I <sub>T</sub> in μA (per circuit), C <sub>L</sub> and C <sub>X</sub> in pF, R <sub>X</sub> in megohms, V <sub>DD</sub> in Vdc, f in kHz is input frequency.							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.  
 5. The formulas given are for the typical characteristics only at 25°C.

# MC14528B

## SWITCHING CHARACTERISTICS <sup>(8.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$C_X$ pF	$R_X$ k $\Omega$	$V_{DD}$ Vdc	Min	Typ <sup>(9.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	—	—	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	15	5.0	5.0 10 15	— — —	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	1000	10	5.0 10 15	— — —	705 290 210	— — —	ns
Input Pulse Width — A or B	$t_{WH}$	15	5.0	5.0 10 15	150 75 55	70 30 30	— — —	ns
	$t_{WL}$	1000	10	5.0 10 15	— — —	70 30 30	— — —	ns
Output Pulse Width — Q or $\bar{Q}$ (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate $V_{DD}$ level.)	$t_W$	15	5.0	5.0 10 15	— — —	550 350 300	— — —	ns
Output Pulse Width — Q or $\bar{Q}$ (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]$ <sup>(6.)</sup> )	$t_W$	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	$\mu\text{s}$
Pulse Width Match between Circuits in the same package	$t_1 - t_2$	10,000	10	5.0 10 15	— — —	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\bar{\text{Reset}}$ to Q or $\bar{Q}$	$t_{PLH},$ $t_{PHL}$	15	5.0	5.0 10 15	— — —	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	— — —	1000 300 250	— — —	ns
Retrigger Time	$t_{rr}$	15	5.0	5.0 10 15	0 0 0	— — —	— — —	ns
		1000	10	5.0 10 15	0 0 0	— — —	— — —	ns
External Timing Resistance	$R_X$	—	—	—	5.0	—	1000	k $\Omega$
External Timing Capacitance	$C_X$	—	—	—	No Limits <sup>(7.)</sup>			$\mu\text{F}$

6.  $R_X$  is in Ohms,  $C_X$  is in farads,  $V_{DD}$  and  $V_{SS}$  in volts,  $PW_{out}$  in seconds.

7. If  $C_X > 15 \mu\text{F}$ , Use Discharge Protection Diode  $D_X$ , per Fig. 9.

8. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

9. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14528B

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\bar{Q}$
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	Not Triggered

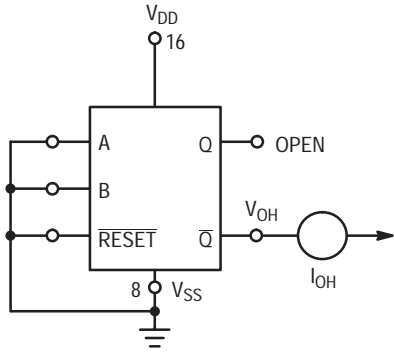


Figure 1. Output Source Current Test Circuit

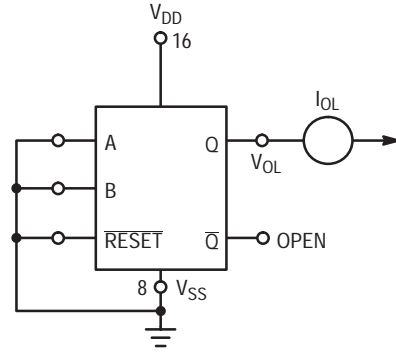


Figure 2. Output Sink Current Test Circuit

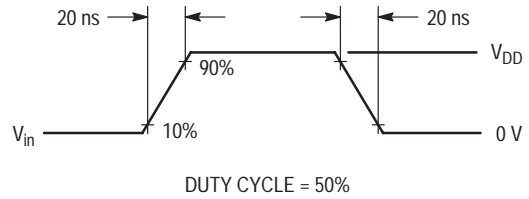
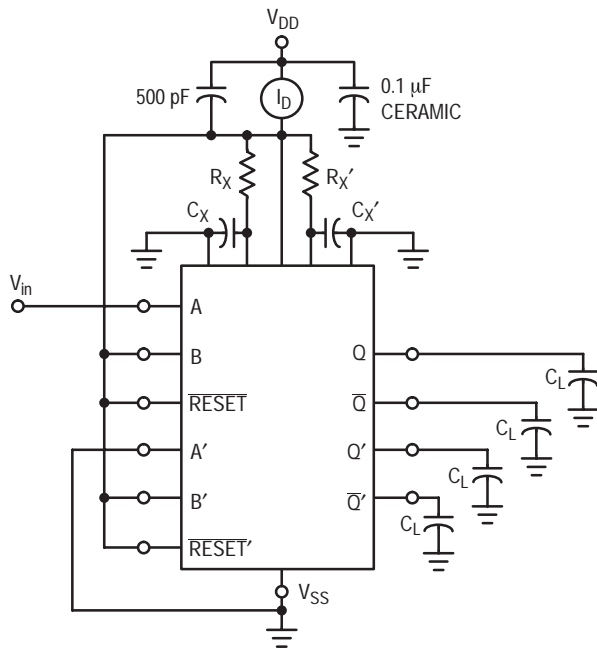
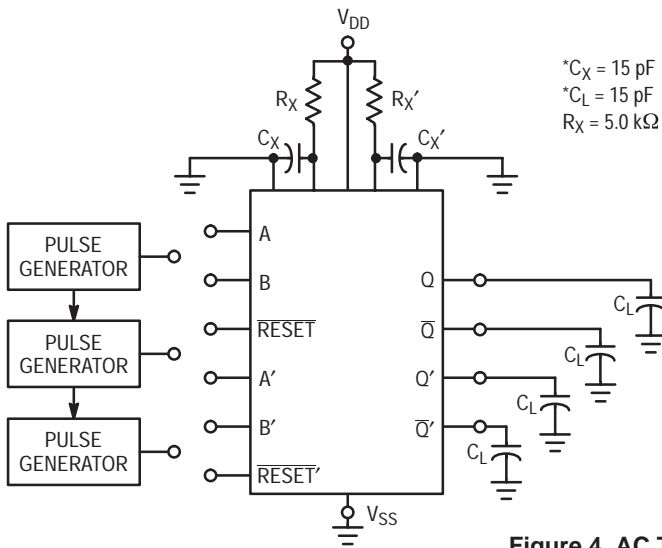


Figure 3. Power Dissipation Test Circuit and Waveforms

# MC14528B



## INPUT CONNECTIONS

Characteristics	Reset	A	B
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ $t_W$	$V_{DD}$	PG1	$V_{DD}$
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ $t_W$	$V_{DD}$	$V_{SS}$	PG2
$t_{PLH(R)}$ , $t_{PHL(R)}$ , $t_W$	PG3	PG1	PG2

\*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

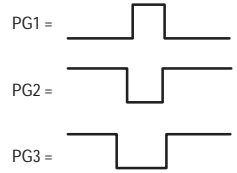


Figure 4. AC Test Circuit

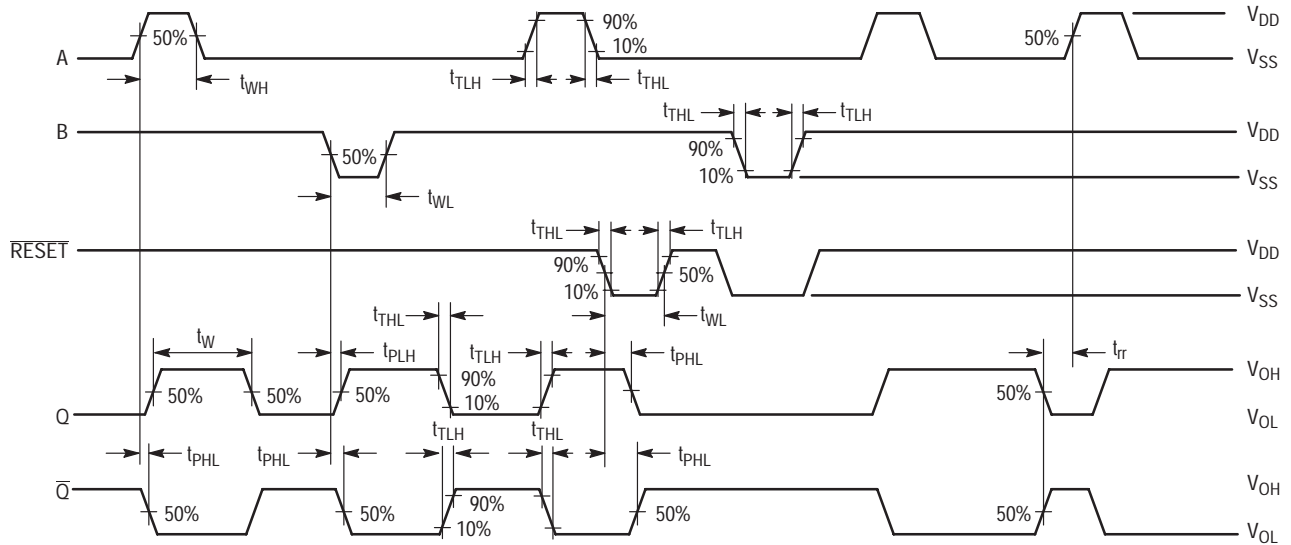


Figure 5. AC Test Waveforms

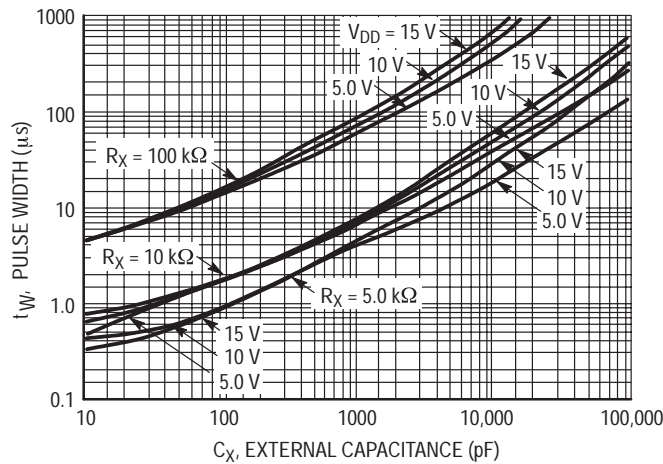


Figure 6. Pulse Width versus  $C_X$

TYPICAL APPLICATIONS

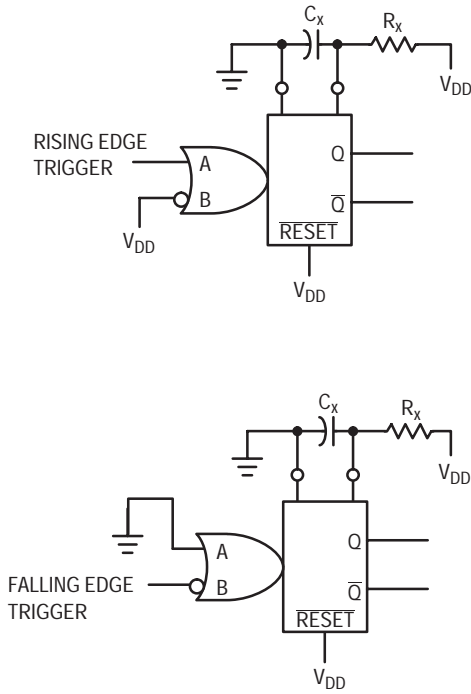


Figure 7. Retriggerable Monostables Circuitry

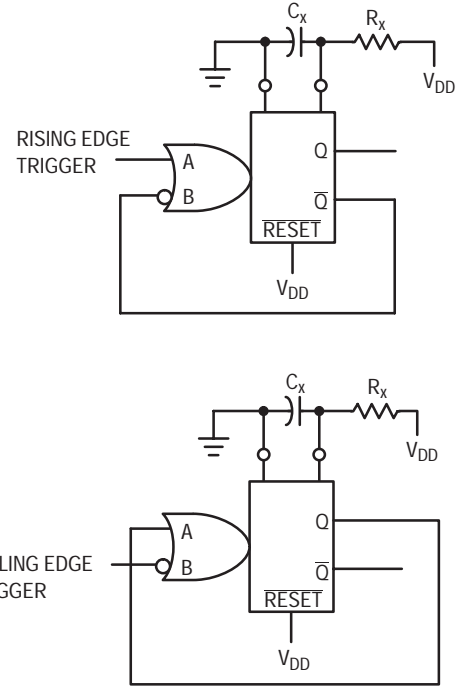


Figure 8. Non-Retriggerable Monostables Circuitry

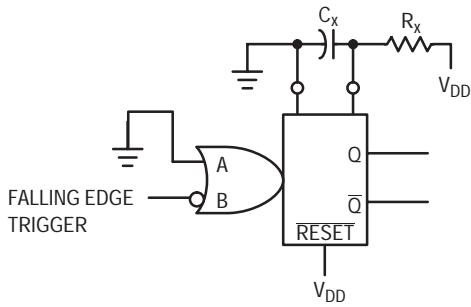


Figure 9. Use of a Diode to Limit Power Down Current Surge

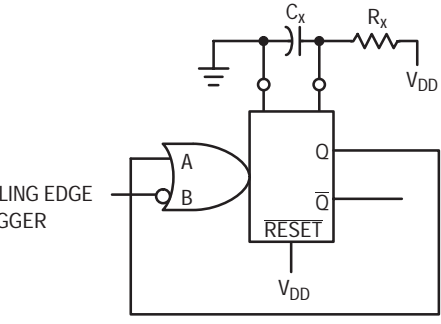


Figure 10. Connection of Unused Sections



# MC14532B

## 8-Bit Priority Encoder

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input ( $E_{in}$ ) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output ( $E_{out}$ ).

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

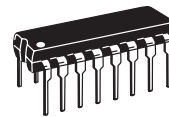
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



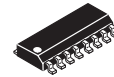
ON Semiconductor

<http://onsemi.com>

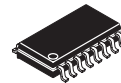


PDIP-16  
P SUFFIX  
CASE 648

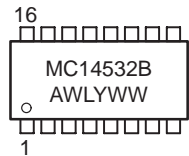
### MARKING DIAGRAMS



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

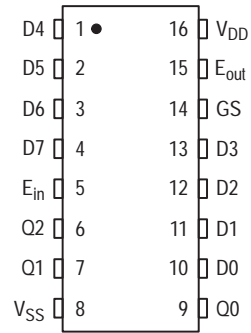
### ORDERING INFORMATION

Device	Package	Shipping
MC14532BCP	PDIP-16	2000/Box
MC14532BD	SOIC-16	48/Rail
MC14532BDR2	SOIC-16	2500/Tape & Reel
MC14532BF	SOEIAJ-16	See Note 1.
MC14532BFEL	SOEIAJ-16	See Note 1.
MC14532BFR1	SOEIAJ-16	See Note 1.

- For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14532B

## PIN ASSIGNMENT



## TRUTH TABLE

Input									Output				
E <sub>in</sub>	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E <sub>out</sub>
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

# MC14532B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.74 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.65 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.73 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.005.

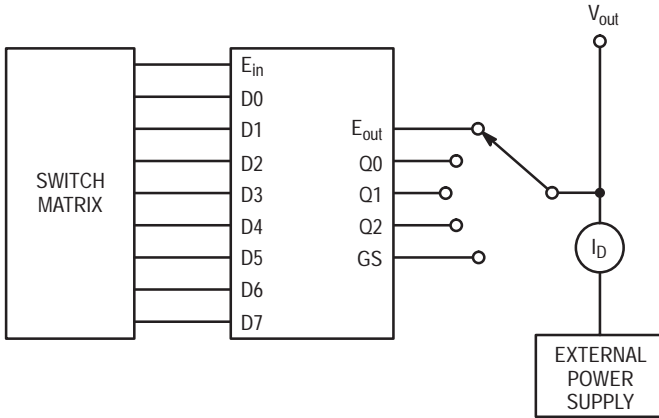
# MC14532B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — $E_{in}$ to $E_{out}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 120 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	205 110 80	410 220 160	ns
Propagation Delay Time — $E_{in}$ to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	175 90 65	350 180 130	ns
Propagation Delay Time — $E_{in}$ to $Q_n$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PHL}, t_{PLH}$	5.0 10 15	— — —	280 140 100	560 280 200	ns
Propagation Delay Time — $D_n$ to $Q_n$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	300 170 110	600 340 220	ns
Propagation Delay Time — $D_n$ to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	280 140 100	560 280 200	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Output Under Test	$V_{GS} = V_{DD}$ $V_{DS} = V_{out}$ Sink Current		$V_{GS} = -V_{DD}$ $V_{DS} = V_{out} - V_{DD}$ Source Current		
	D0 thru D7	$E_{in}$	D0 thru D6	D7	$E_{in}$
$E_{out}$	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

Figure 1. Typical Sink and Source Current Characteristics

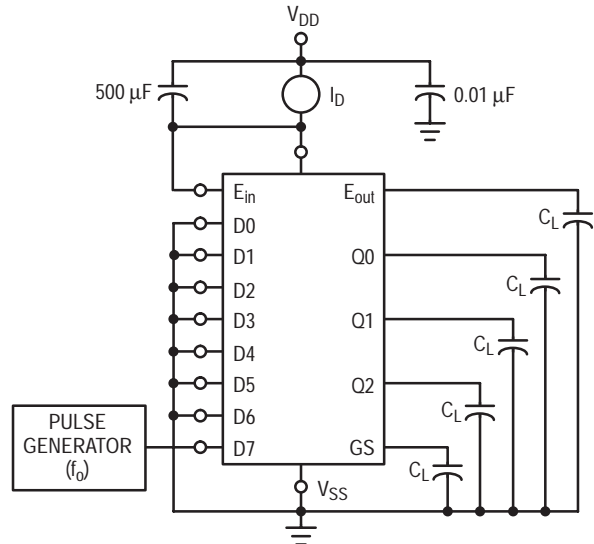


Figure 2. Typical Power Dissipation Test Circuit

# MC14532B

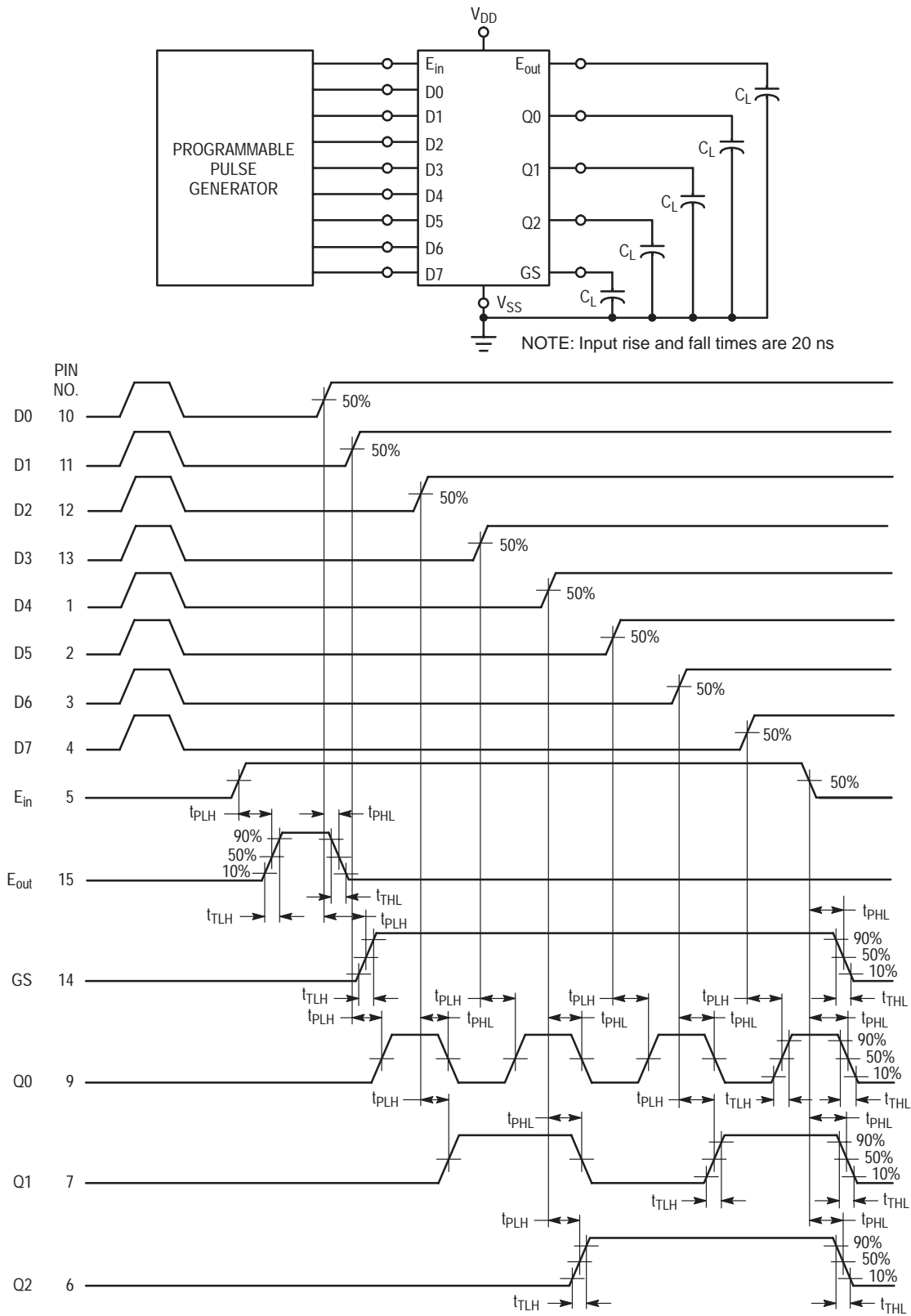


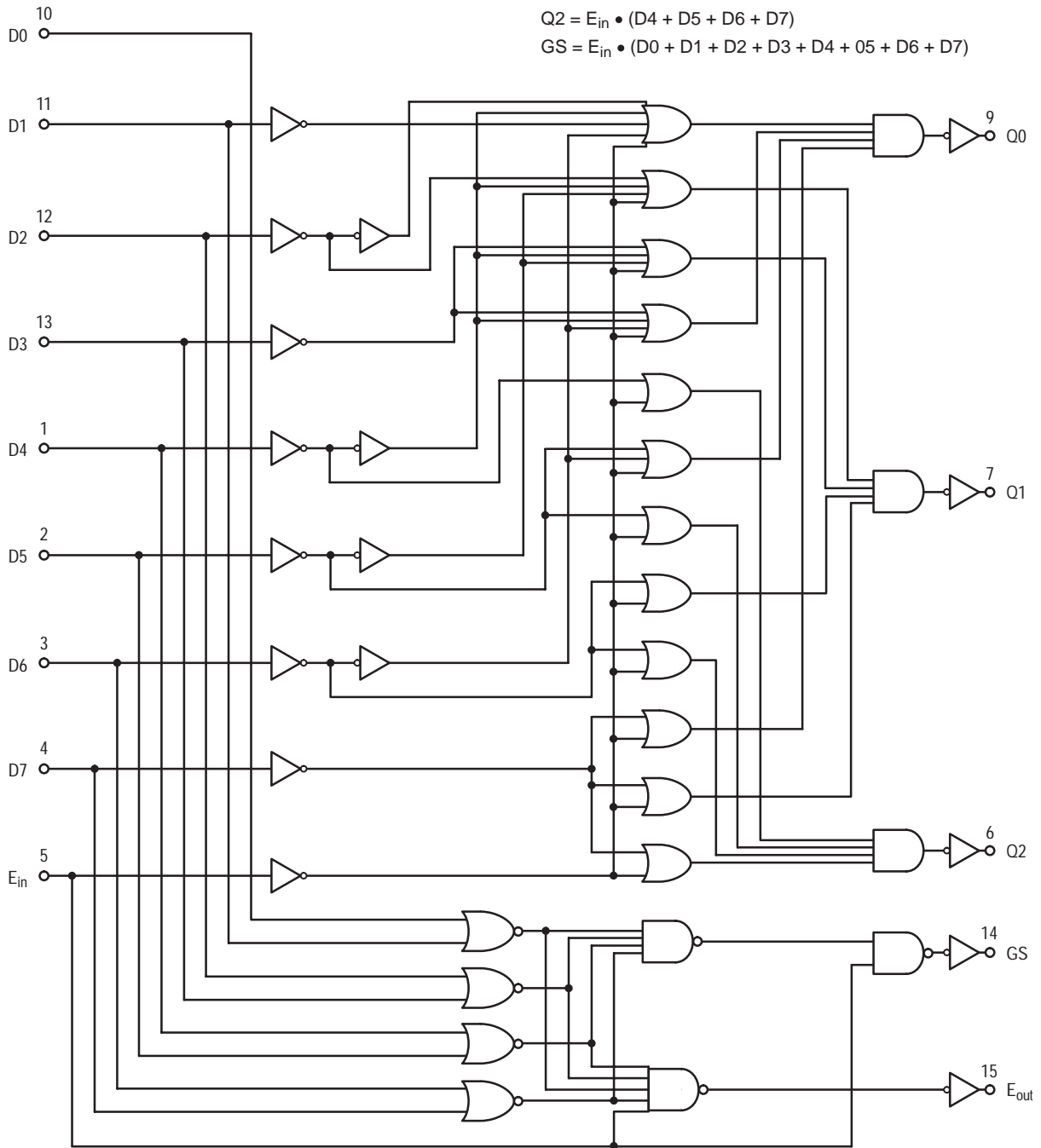
Figure 3. AC Test Circuit and Waveforms

# MC14532B

## LOGIC DIAGRAM (Positive Logic)

## LOGIC EQUATIONS

$$E_{out} = E_{in} \cdot \bar{D}0 \cdot \bar{D}1 \cdot \bar{D}2 \cdot \bar{D}3 \cdot \bar{D}4 \cdot \bar{D}5 \cdot \bar{D}6 \cdot \bar{D}7$$
$$Q0 = E_{in} \cdot (D1 \cdot \bar{D}2 \cdot \bar{D}4 \cdot \bar{D}6 + D3 \cdot \bar{D}4 \cdot \bar{D}6 + D5 \cdot \bar{D}6 + D7)$$
$$Q1 = E_{in} \cdot (D2 \cdot \bar{D}4 \cdot \bar{D}5 + D3 \cdot \bar{D}4 \cdot \bar{D}5 + D6 + D7)$$
$$Q2 = E_{in} \cdot (D4 + D5 + D6 + D7)$$
$$GS = E_{in} \cdot (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$$



## MC14532B

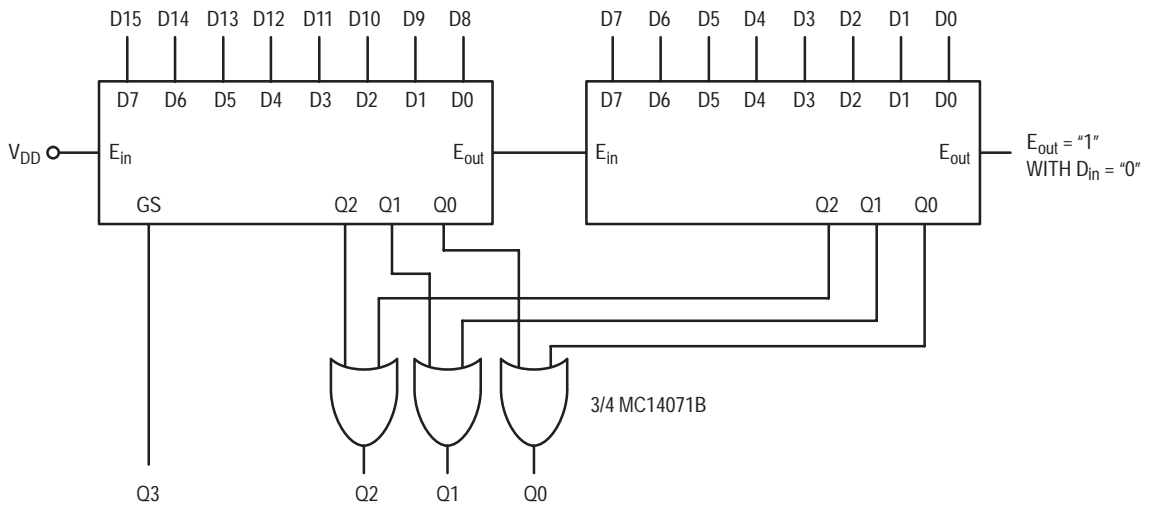


Figure 4. Two MC14532B's Cascaded for 4–Bit Output

### DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at  $V_{DD} = 10\text{ V}$ ) is applied to the MC14520B. A compromise between  $I_{bias}$  for the MC1710 and  $\Delta R$  between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if  $R = 33\text{ k ohms}$ ,  $C \approx 0.03\text{ }\mu\text{F}$ ). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

### ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

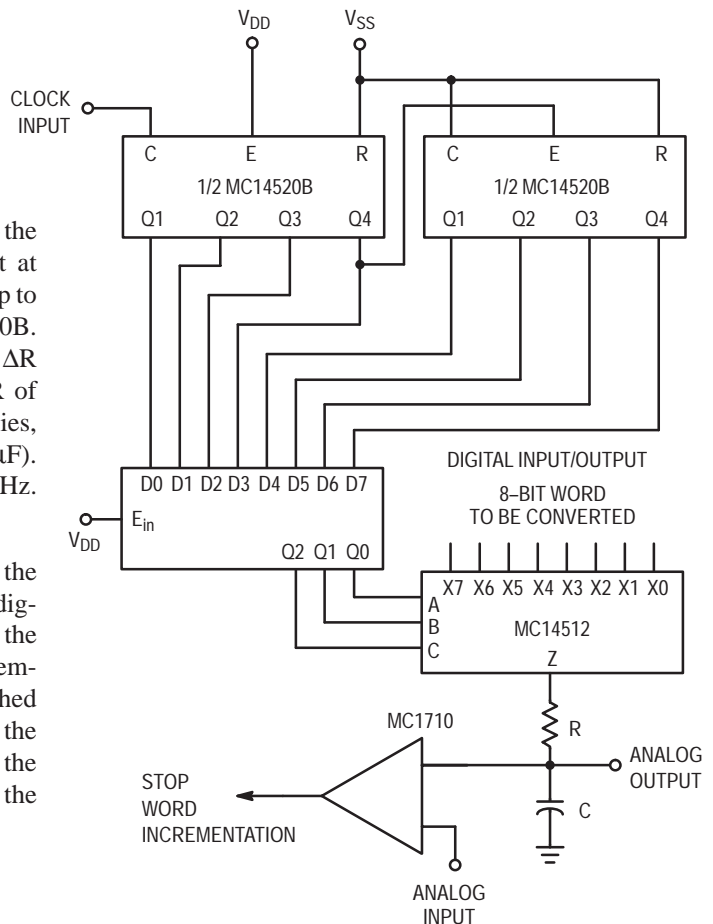


Figure 5. Digital to Analog and Analog to Digital Converter

# MC14536B

## Programmable Timer

The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages — Will Count From  $2^0$  to  $2^{24}$
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

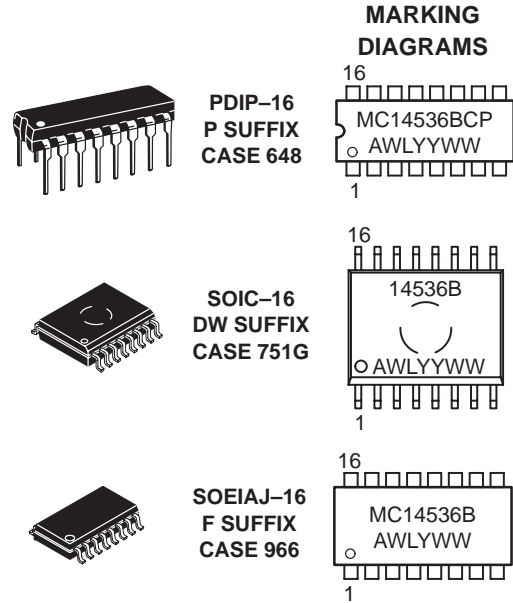
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor

<http://onsemi.com>



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14536BCP	PDIP-16	2000/Box
MC14536BDW	SOIC-16	47/Rail
MC14536BDWR2	SOIC-16	1000/Tape & Reel
MC14536BF	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

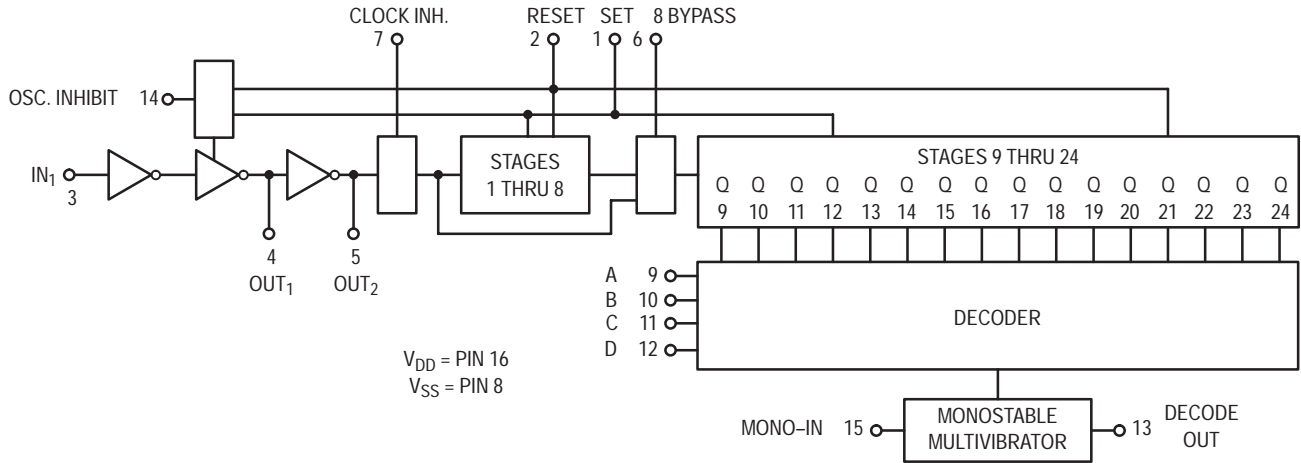


# MC14536B

## PIN ASSIGNMENT

SET	1 ●	16	V <sub>DD</sub>
RESET	2	15	MONO IN
IN 1	3	14	OSC INH
OUT 1	4	13	DECODE
OUT 2	5	12	D
8-BYPASS	6	11	C
CLOCK INH	7	10	B
V <sub>SS</sub>	8	9	A

## BLOCK DIAGRAM



# MC14536B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(4.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current  Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub> Pins 4 & 5	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.25	-0.36	—	-0.14	—	
		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	I <sub>OH</sub> Pin 13	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
	Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.50 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.30 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.55 μA/kHz) f + I <sub>DD</sub>						μAdc	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.003.

# MC14536B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time (Pin 13) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1, 8-Bypass (Pin 6) High $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1715 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 617 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 425 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	1800 650 450	3600 1300 1000	ns
Clock to Q1, 8-Bypass (Pin 6) Low $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3715 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1467 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 1075 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	3.8 1.5 1.1	7.6 3.0 2.3	$\mu\text{s}$
Clock to Q16 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 6915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2967 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2175 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	7.0 3.0 2.2	14 6.0 4.5	$\mu\text{s}$
Reset to $Q_n$ $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1415 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 567 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 425 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	1500 600 450	3000 1200 900	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	600 200 170	300 100 85	— — —	ns
Clock Pulse Frequency (50% Duty Cycle)	$f_{cl}$	5.0 10 15	— — —	1.2 3.0 5.0	0.4 1.5 2.0	MHz
Clock Rise and Fall Time	$t_{TLH},$ $t_{THL}$	5.0 10 15	No Limit			—
Reset Pulse Width	$t_{WH}$	5.0 10 15	1000 400 300	500 200 150	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## PIN DESCRIPTIONS

## INPUTS

**SET (Pin 1)** — A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip–flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on  $IN_1$  causes Decode Out to go low. The counter's flip–flop stages begin counting on the second negative clock transition of  $IN_1$ . When Set is high, the on–chip RC oscillator is disabled. This allows for very low–power standby operation.

**RESET (Pin 2)** — A high on Reset asynchronously forces Decode Out to a low level; all 24 flip–flop stages are also reset to a low level. Like the Set input, Reset disables the on–chip RC oscillator for standby operation.

**$IN_1$  (Pin 3)** — The device's internal counters advance on the negative–going edge of this input.  $IN_1$  may be used as an external clock input or used in conjunction with  $OUT_1$  and  $OUT_2$  to form an RC oscillator. When an external clock is used, both  $OUT_1$  and  $OUT_2$  may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

**8–BYPASS (Pin 6)** — A high on this input causes the first 8 flip–flop stages to be bypassed. This device essentially becomes a 16–stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

**CLOCK INHIBIT (Pin 7)** — A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start–up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at  $IN_1$ .

**OSC INHIBIT (Pin 14)** — A high level on this pin stops the RC oscillator which allows for very low–power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

**MONO–IN (Pin 15)** — Used as the timing pin for the on–chip monostable multivibrator. If the Mono–In input is connected to  $V_{SS}$ , the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono–In and  $V_{DD}$ . This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to  $V_{SS}$ , the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 k $\Omega$  to 100 k $\Omega$  and the capacitor value should be limited to a maximum of 1000 pf. (See figures 3, 4, 5, and 10).

**A, B, C, D (Pins 9, 10, 11, 12)** — These inputs select the flip–flop stage to be connected to Decode Out. (See the truth tables.)

## OUTPUTS

**$OUT_1$ ,  $OUT_2$  (Pin 4, 5)** — Outputs used in conjunction with  $IN_1$  to form an RC oscillator. These outputs are buffered and may be used for  $2^0$  frequency division of an external clock.

**DECODE OUT (Pin 13)** — Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

## TEST MODE

The test mode configuration divides the 24 flip–flop stages into three 8–stage sections to facilitate a fast test sequence. The test mode is enabled when 8–Bypass, Set and Reset are at a high level. (See Figure 8.)










# MC14536B

## TRUTH TABLES

Input					Stage Selected for Decode Out
8-Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
0	1	1	0	0	21
0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

Input					Stage Selected for Decode Out
8-Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

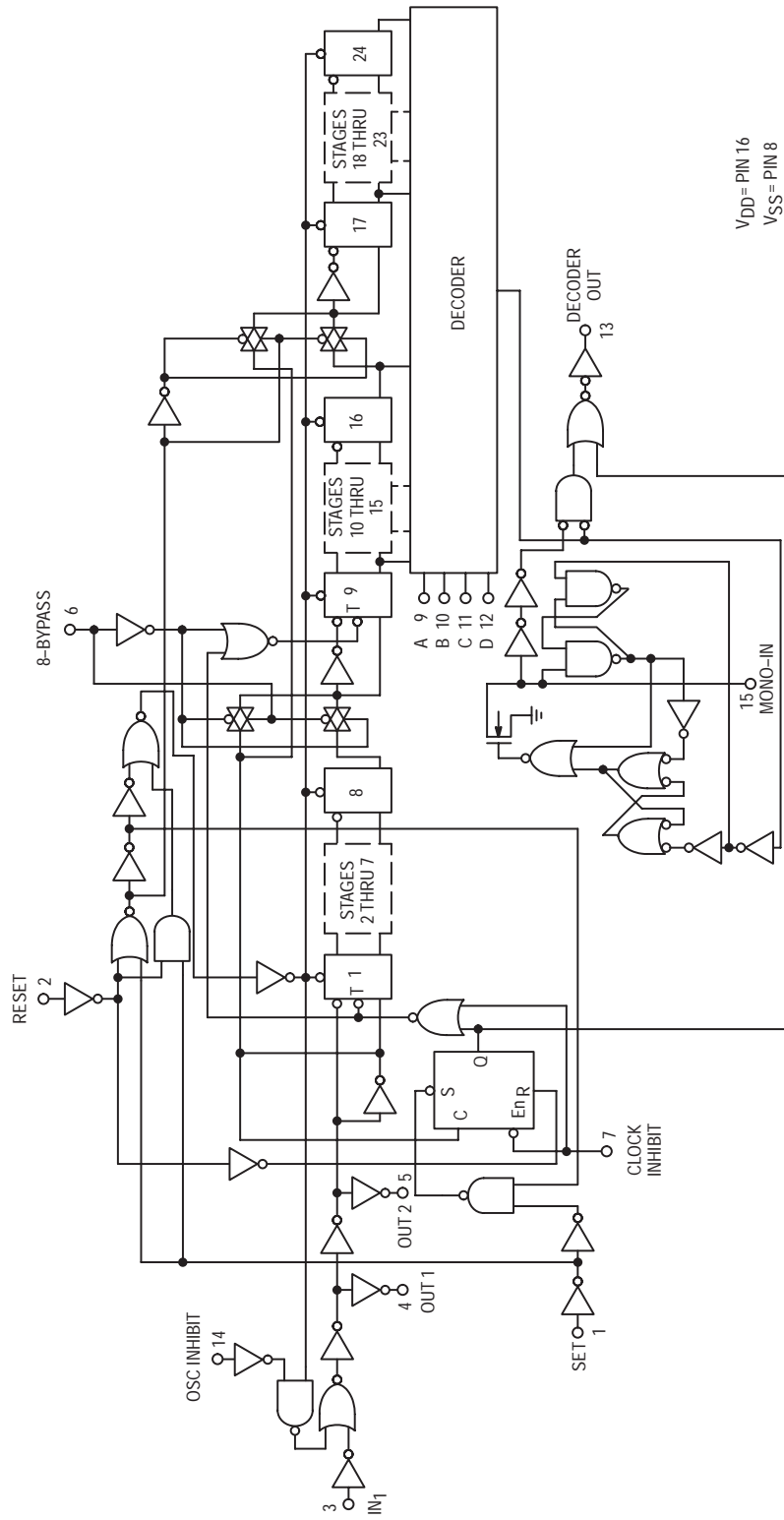
## FUNCTION TABLE

In <sub>1</sub>	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
	0	0	0	0			No Change
	0	0	0	0			Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	—	—	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0				Advance to next state

X = Don't Care

# MC14536B

## LOGIC DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

**TYPICAL RC OSCILLATOR CHARACTERISTICS**  
(For Circuit Diagram See Figure 11 In Application)

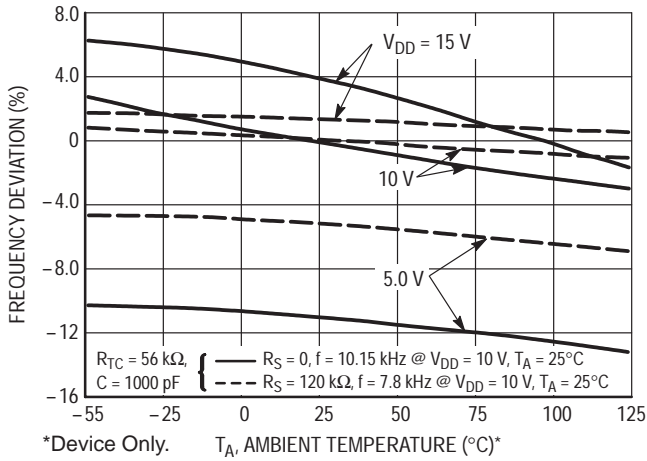


Figure 1. RC Oscillator Stability

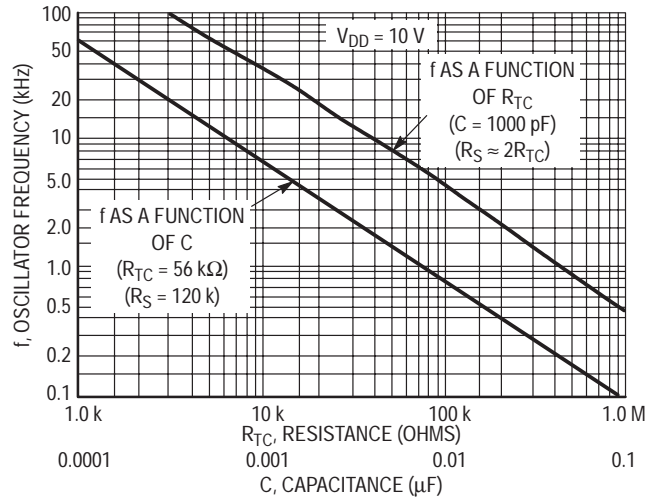


Figure 2. RC Oscillator Frequency as a Function of  $R_{TC}$  and C

**MONOSTABLE CHARACTERISTICS**  
(For Circuit Diagram See Figure 10 In Application)

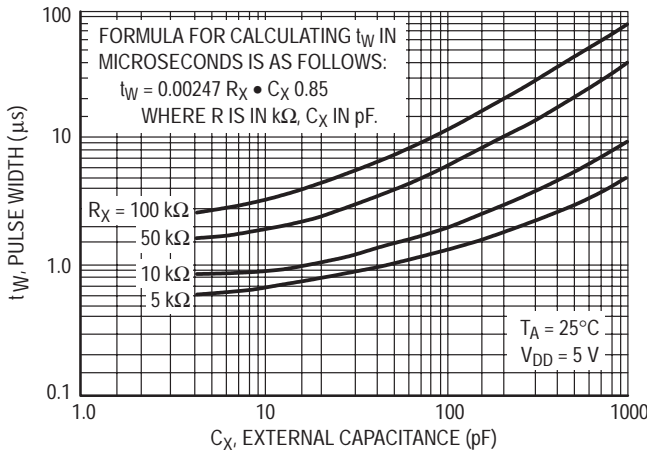


Figure 3. Typical  $C_X$  versus Pulse Width @  $V_{DD} = 5.0 V$

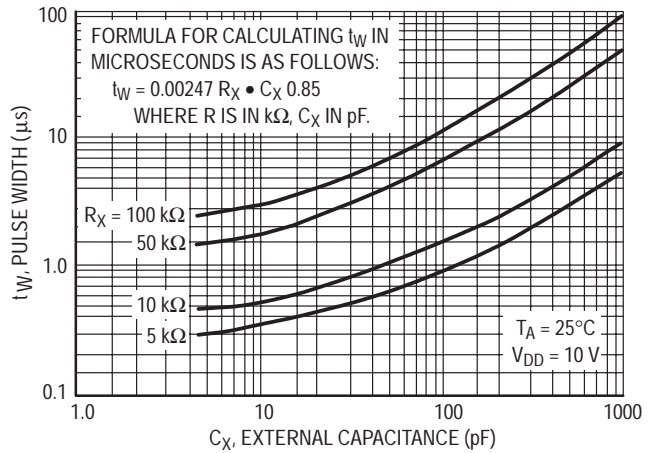


Figure 4. Typical  $C_X$  versus Pulse Width @  $V_{DD} = 10 V$

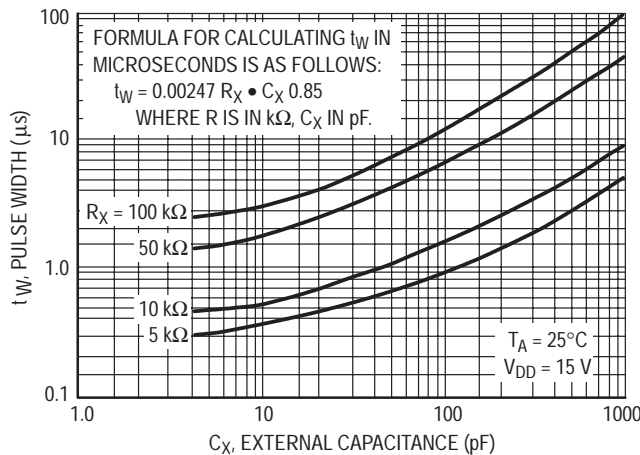


Figure 5. Typical  $C_X$  versus Pulse Width @  $V_{DD} = 15 V$

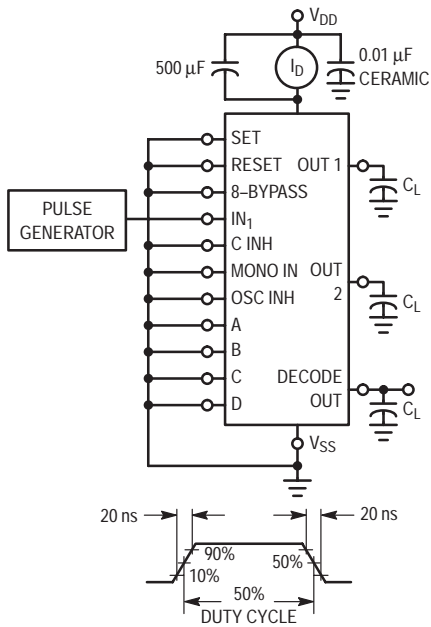


Figure 6. Power Dissipation Test Circuit and Waveform

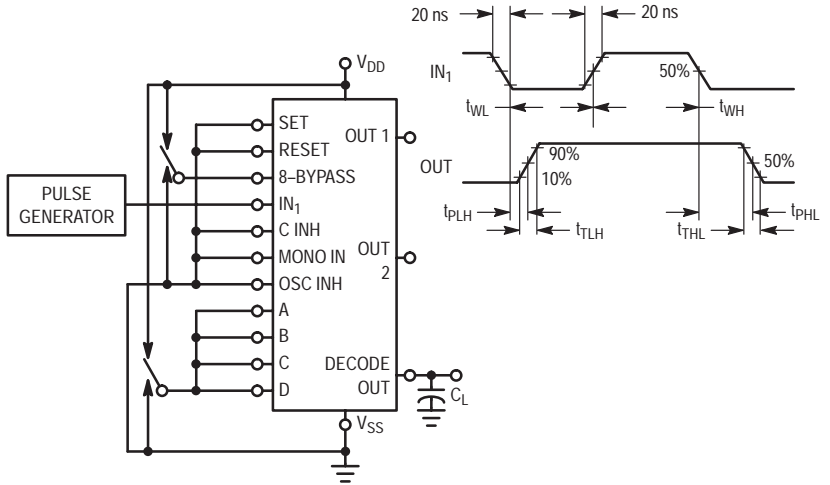


Figure 7. Switching Time Test Circuit and Waveforms

**FUNCTIONAL TEST SEQUENCE**

Test function (Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a “1”. The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In<sub>1</sub> which will cause the counter to ripple from an all “1” state to an all “0” state.

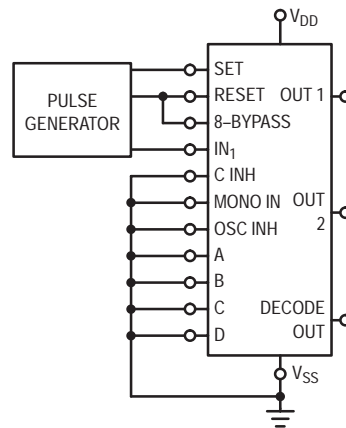


Figure 8. Functional Test Circuit

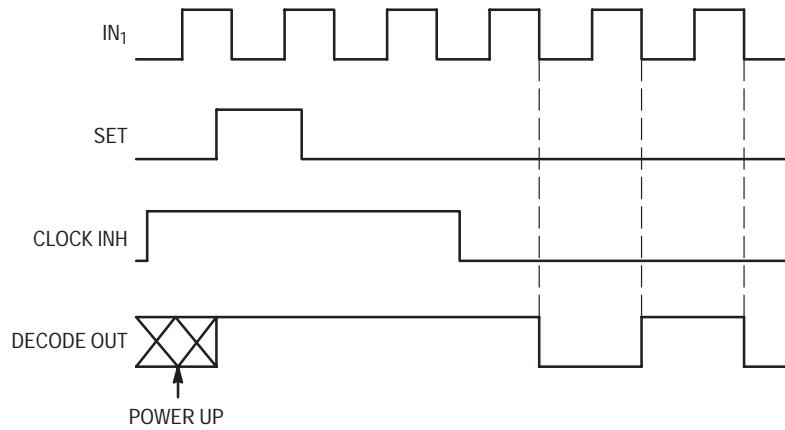
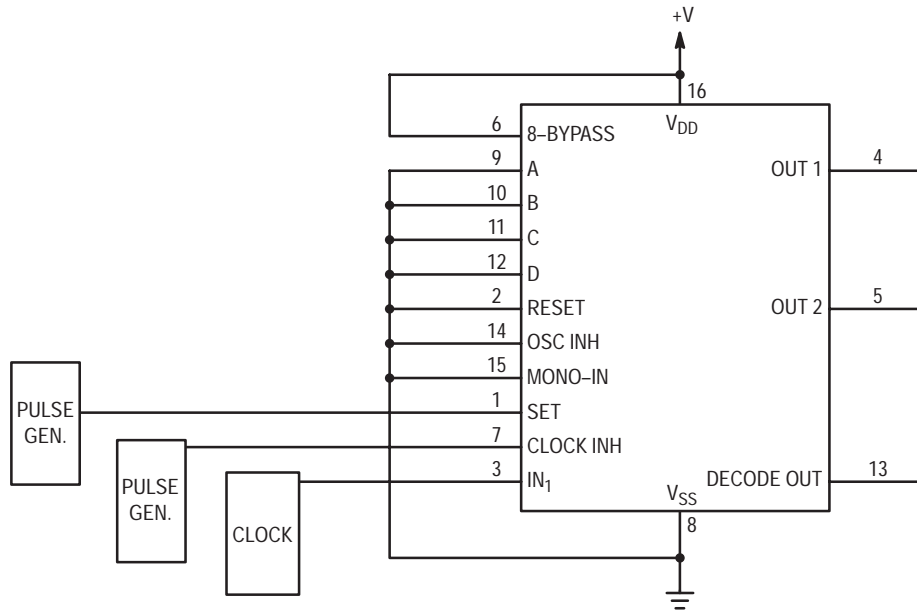


# MC14536B

## FUNCTIONAL TEST SEQUENCE

Inputs				Outputs	Comments
In <sub>1</sub>	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8 stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 — — —	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In <sub>1</sub> Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

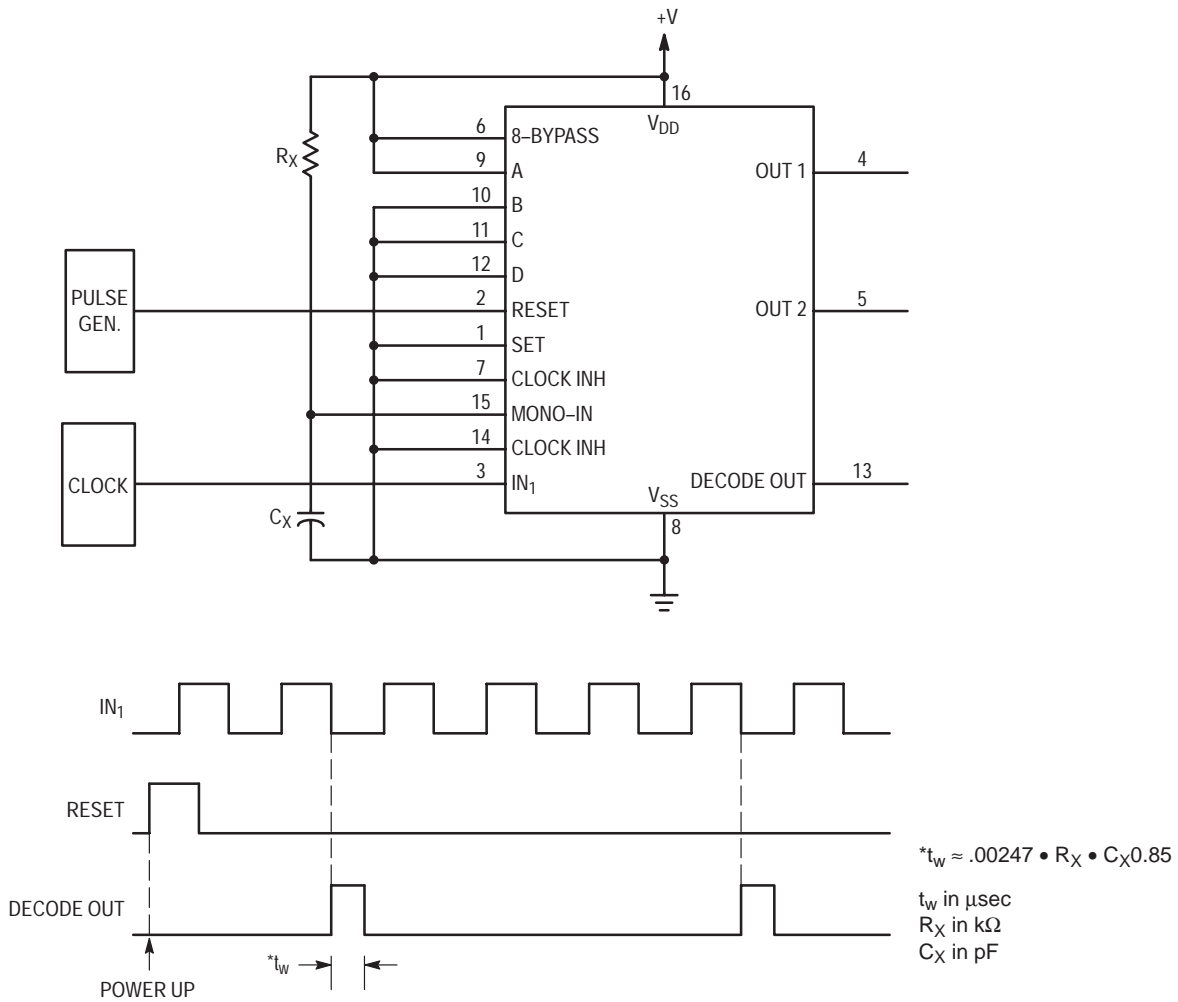
# MC14536B



NOTE: When power is first applied to the device, Decode Out can be either at a high or low state. On the rising edge of a Set pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because Clock Inh is held high, the clock source on the input pin has no effect on the output. Once Clock Inh is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-Bypass, A, B, C, and D inputs, and the clock input period. A  $2^n$  frequency division (where  $n$  = the number of stages selected from the truth table) is obtainable at Decode Out. A  $2^0$ -divided output of  $IN_1$  can be obtained at  $OUT_1$  and  $OUT_2$ .

**Figure 9. Time Interval Configuration Using an External Clock, Set, and Clock Inhibit Functions (Divide-by-2 Configured)**

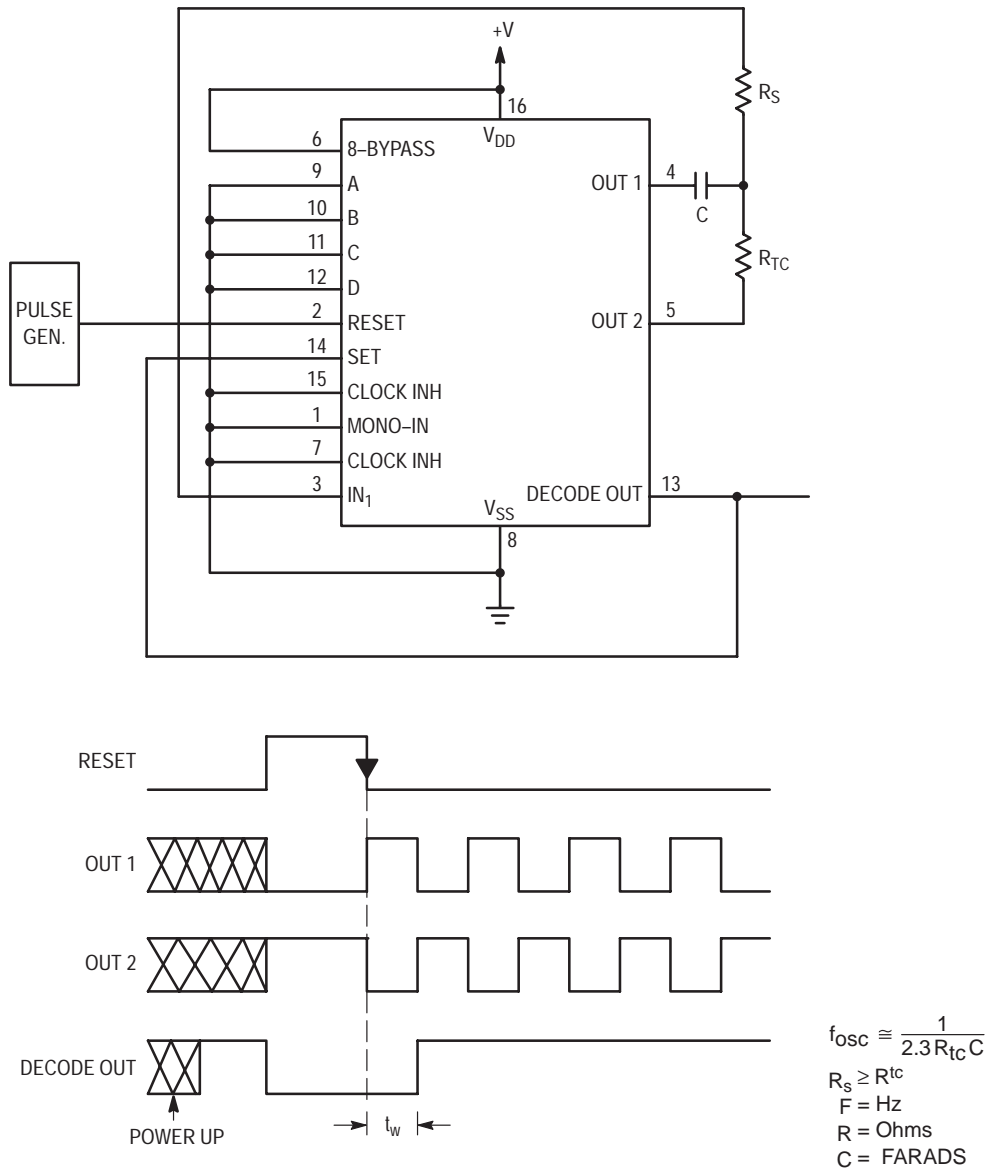
# MC14536B



NOTE: When Power is first applied to the device with the Reset input going high, Decode Out initializes low. Bringing the Reset input low enables the chip's internal counters. After Reset goes low, the  $2^{n/2}$  negative transition of the clock input causes Decode Out to go high. Since the Mono-In input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at  $2^n \times$  (the clock period) intervals where  $n =$  the number of stages selected from the truth table.

**Figure 10. Time Interval Configuration Using an External Clock, Reset, and Output Monostable to Achieve a Pulse Output (Divide-by-4 Configured)**

# MC14536B



NOTE: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, Decode Out initializes to a high state. Because this output is tied directly to the Osc-Inh input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the Reset pulse will cause the output to go low. This in turn causes Osc-Inh to go low. However, while Reset is high, the oscillator is still disabled (i.e.: standby condition). After Reset goes low, the output remains low for 2<sup>1/2</sup> of the oscillator's period. After the part times out, the output again goes high.

**Figure 11. Time Interval Configuration Using On-Chip RC Oscillator and Reset Input to Initiate Time Interval (Divide-by-2 Configured)**

# MC14538B

## Dual Precision Retriggerable/Resetable Monostable Multivibrator

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components,  $C_X$  and  $R_X$ .

Output Pulse Width =  $(C_X)(R_X)$  where:

$R_X$  is in  $k\Omega$

$C_X$  is in  $\mu F$

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10  $\mu s$  to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538A for Pulse Widths Less Than 10  $\mu s$  with Supplies Up to 6 V.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

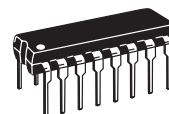
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



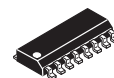
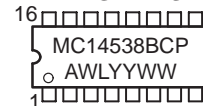
ON Semiconductor

<http://onsemi.com>

### MARKING DIAGRAMS



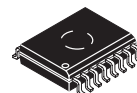
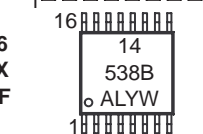
PDIP-16  
P SUFFIX  
CASE 648



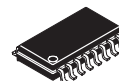
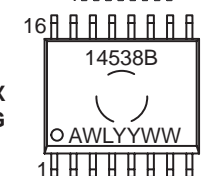
SOIC-16  
D SUFFIX  
CASE 751B



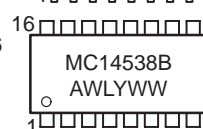
TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC-16  
DW SUFFIX  
CASE 751G



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

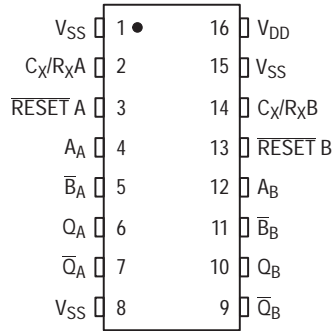
### ORDERING INFORMATION

Device	Package	Shipping
MC14538BCP	PDIP-16	2000/Box
MC14538BD	SOIC-16	48/Rail
MC14538BDR2	SOIC-16	2500/Tape & Reel
MC14538BDT	TSSOP-16	96/Rail
MC14538BDTR2	TSSOP-16	2500/Tape & Reel
MC14538BDW	SOIC-16	47/Rail
MC14538BDWR2	SOIC-16	1000/Tape & Reel
MC14538BF	SOEIAJ-16	See Note 1.
MC14538BFEL	SOEIAJ-16	See Note 1.

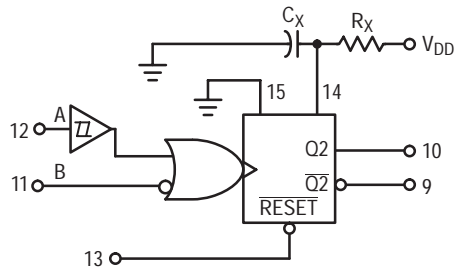
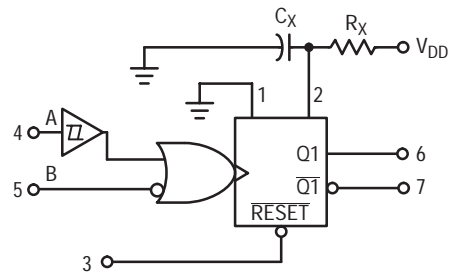
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14538B

## PIN ASSIGNMENT



## BLOCK DIAGRAM

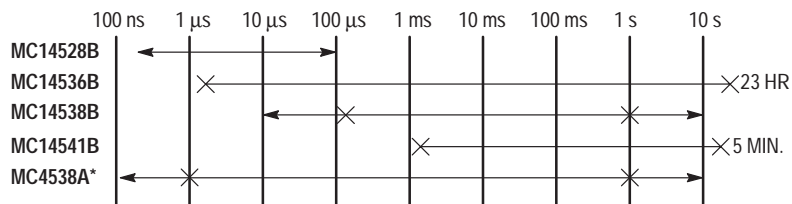


R<sub>X</sub> AND C<sub>X</sub> ARE EXTERNAL COMPONENTS.

V<sub>DD</sub> = PIN 16

V<sub>SS</sub> = PIN 8, PIN 1, PIN 15

## ONE-SHOT SELECTION GUIDE



\*LIMITED OPERATING VOLTAGE (2 - 6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ← →  
 RECOMMENDED PULSE WIDTH RANGE × — ×

# MC14538B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current, Pin 2 or 14	I <sub>in</sub>	15	—	±0.05	—	±0.00001	±0.05	—	±0.5	μAdc
Input Current, Other Inputs	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance, Pin 2 or 14	C <sub>in</sub>	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Q = Low, $\bar{Q}$ = High	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current, Active State (Both) (Per Package) Q = High, $\bar{Q}$ = Low	I <sub>DD</sub>	5.0	—	2.0	—	0.04	0.20	—	2.0	mAdc
		10	—	2.0	—	0.08	0.45	—	2.0	
		15	—	2.0	—	0.13	0.70	—	2.0	
Total Supply Current at an external load capacitance (C <sub>L</sub> ) and at external timing network (R <sub>X</sub> , C <sub>X</sub> ) (5.)	I <sub>T</sub>	5.0 10	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I <sub>T</sub> in μA (one monostable switching only), C <sub>X</sub> in μF, C <sub>L</sub> in pF, R <sub>X</sub> in k ohms, and f in Hz is the input frequency.							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

# MC14538B

## SWITCHING CHARACTERISTICS (6.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (7.)	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$  Reset to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	300 150 100  250 125 95	600 300 220  500 250 190	ns   ns
Input Rise and Fall Times Reset  B Input  A Input	$t_r, t_f$	5 10 15  5 10 15  5 10 15	— — —  — — —  — — —	— — —  300 1.2 0.4  No Limit	15 5 4  1.0 0.1 0.05  —	$\mu\text{s}$  ms  —
Input Pulse Width A, B, or Reset	$t_{WH},$ $t_{WL}$	5.0 10 15	170 90 80	85 45 40	— — —	ns
Retrigger Time	$t_{rr}$	5.0 10 15	0 0 0	— — —	— — —	ns
Output Pulse Width — Q or $\bar{Q}$ Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}$ , $R_X = 100 \text{ k}\Omega$  $C_X = 0.1 \mu\text{F}$ , $R_X = 100 \text{ k}\Omega$  $C_X = 10 \mu\text{F}$ , $R_X = 100 \text{ k}\Omega$	T	5.0 10 15  5.0 10 15  5.0 10 15	198 200 202  9.3 9.4 9.5  0.91 0.92 0.93	210 212 214  9.86 10 10.14  0.965 0.98 0.99	230 232 234  10.5 10.6 10.7  1.03 1.04 1.06	$\mu\text{s}$  ms  s
Pulse Width Match between circuits in the same package. $C_X = 0.1 \mu\text{F}$ , $R_X = 100 \text{ k}\Omega$	100 [[ $(T_1 - T_2)/T_1$ ]]	5.0 10 15	— — —	$\pm 1.0$ $\pm 1.0$ $\pm 1.0$	$\pm 5.0$ $\pm 5.0$ $\pm 5.0$	%

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

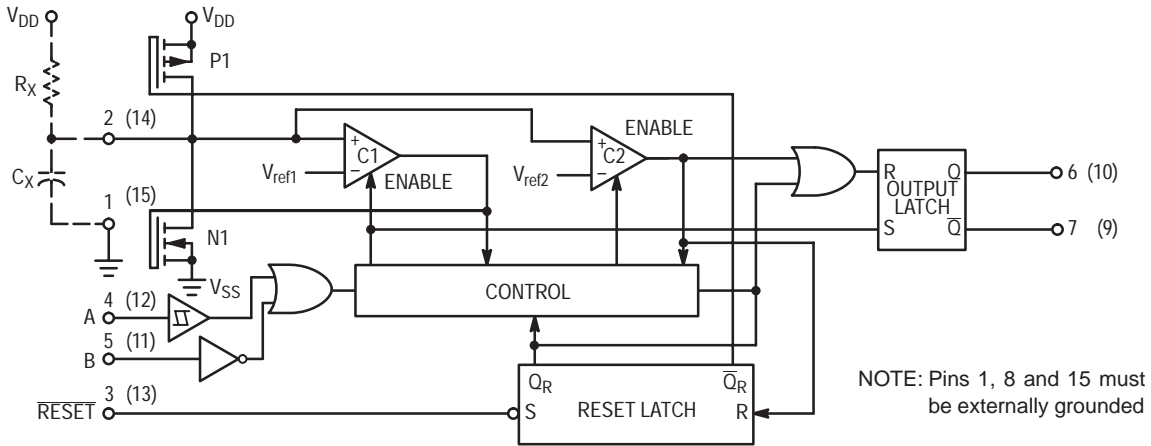


# MC14538B

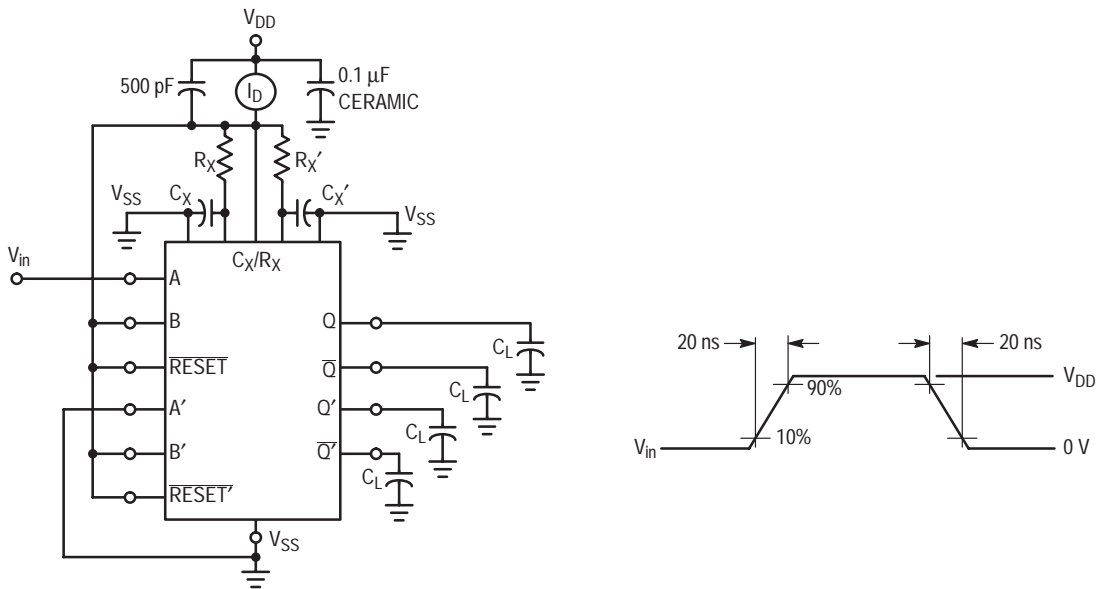
## OPERATING CONDITIONS

External Timing Resistance	$R_X$	—	5.0	—	(8.)	$k\Omega$
External Timing Capacitance	$C_X$	—	0	—	No Limit (9.)	$\mu F$

8. The maximum usable resistance  $R_X$  is a function of the leakage of the capacitor  $C_X$ , leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for  $R_X > 1 M\Omega$ .
9. If  $C_X > 15 \mu F$ , use discharge protection diode per Fig. 11.

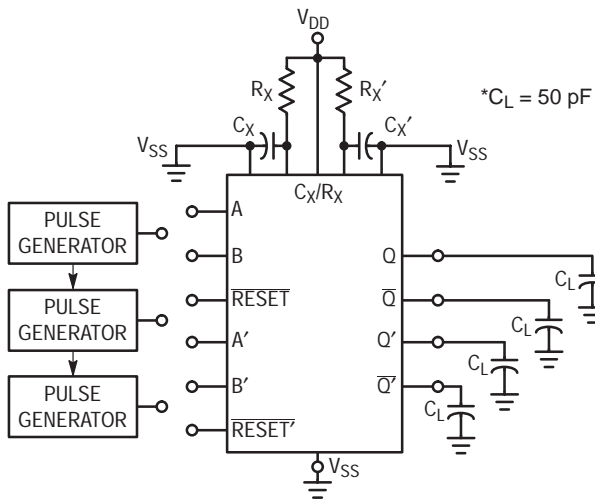


**Figure 1. Logic Diagram  
(1/2 of Device Shown)**



**Figure 2. Power Dissipation Test Circuit and Waveforms**

# MC14538B



## INPUT CONNECTIONS

Characteristics	Reset	A	B
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	PG1	$V_{DD}$
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	$V_{SS}$	PG2
$t_{PLH(R)}$ , $t_{PHL(R)}$ , $t_{WH}$ , $t_{WL}$	PG3	PG1	PG2

\*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

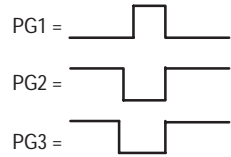


Figure 3. Switching Test Circuit

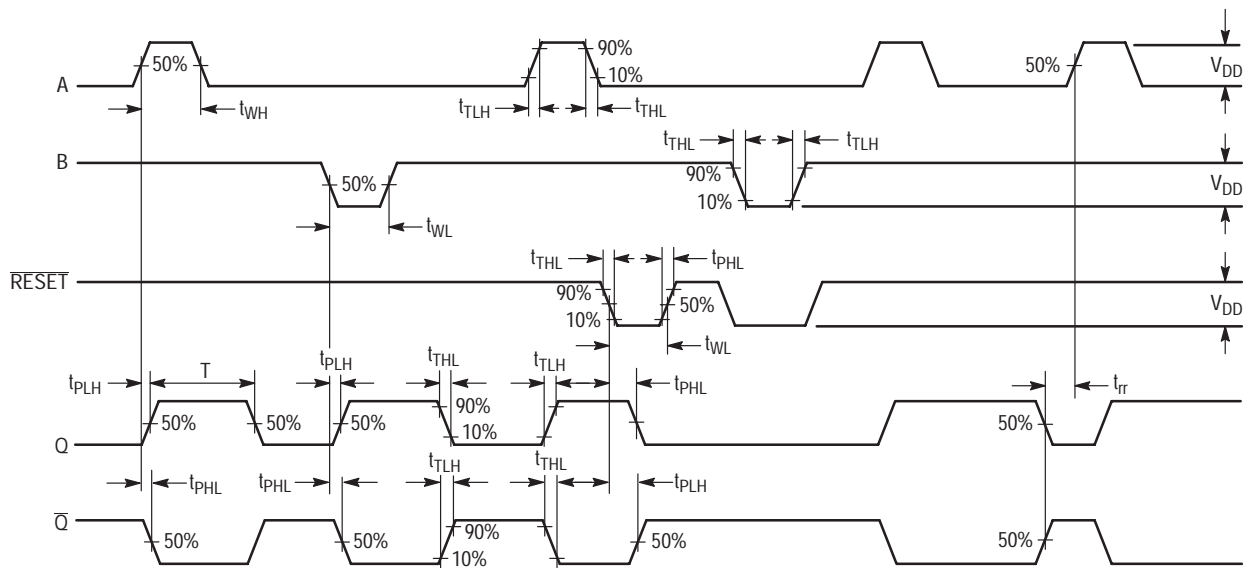


Figure 4. Switching Test Waveforms

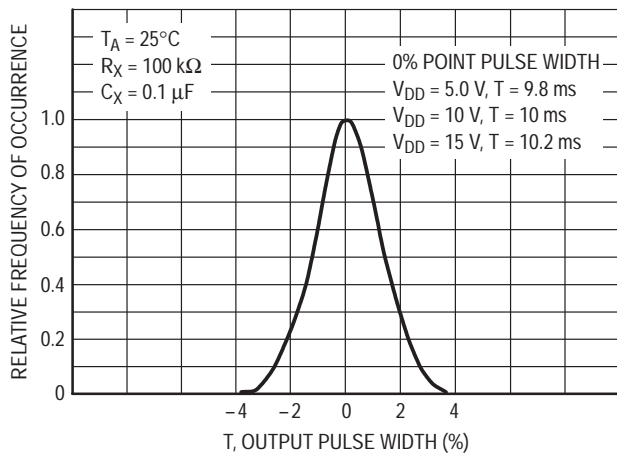


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

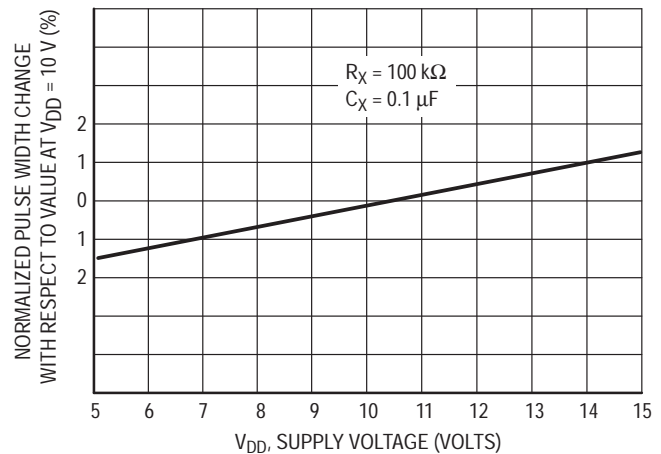


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage  $V_{DD}$

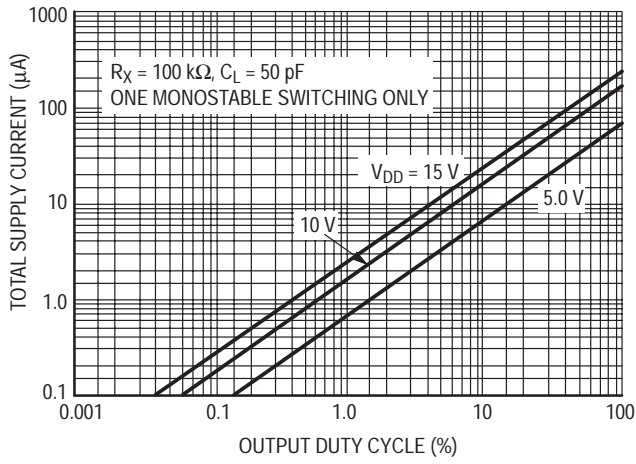


Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

		Inputs		Outputs	
Reset		A	B	Q	$\bar{Q}$
H			H		
H		L			
H			L	Not Triggered	Not Triggered
H		H		Not Triggered	Not Triggered
H		L, H,	H	Not Triggered	Not Triggered
H		L	L, H,	Not Triggered	Not Triggered
L		X	X	L	H
		X	X	Not Triggered	Not Triggered

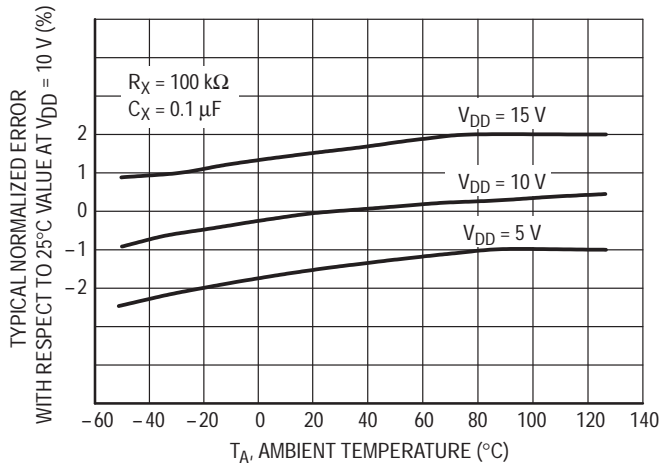


Figure 8. Typical Error of Pulse Width Equation versus Temperature

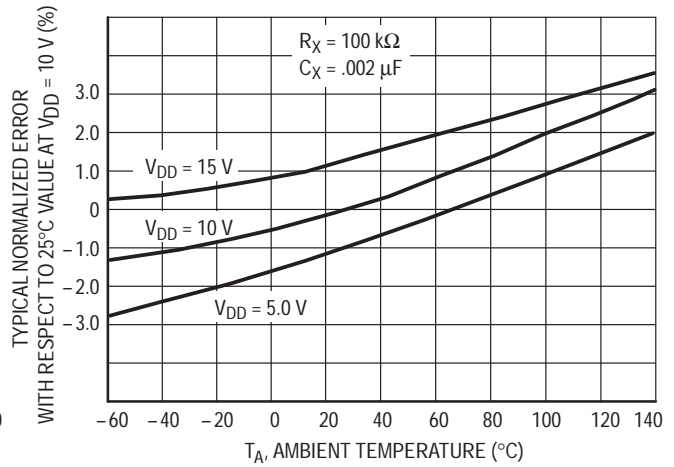


Figure 9. Typical Error of Pulse Width Equation versus Temperature

## THEORY OF OPERATION

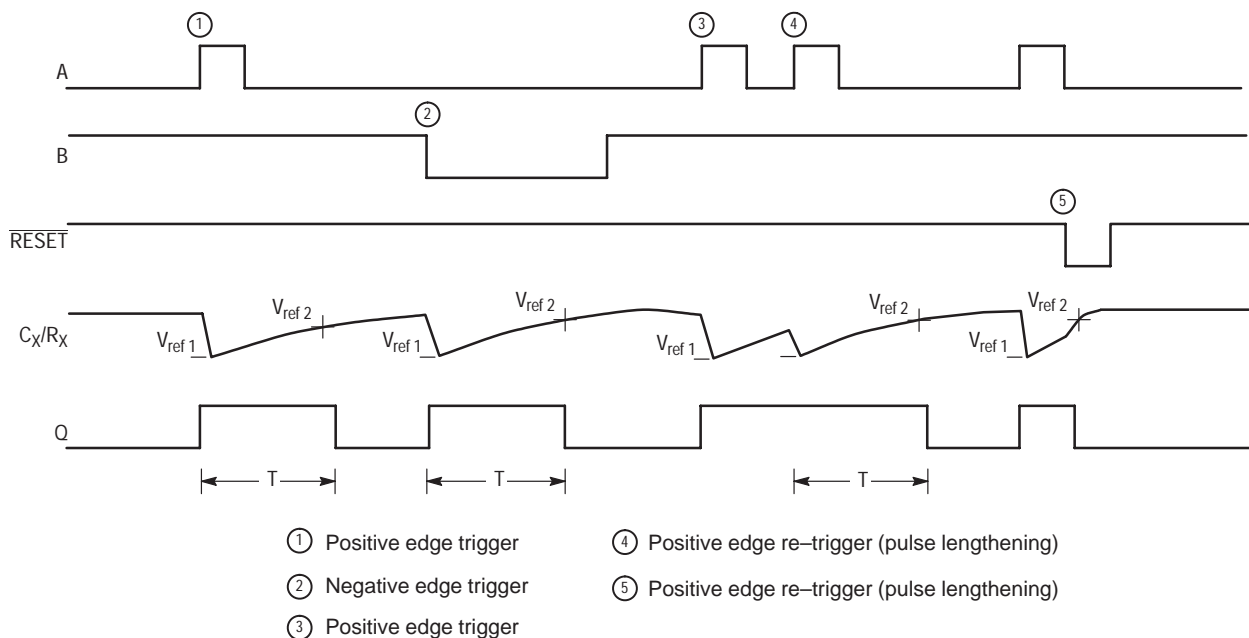


Figure 10. Timing Operation

## TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor  $C_X$  completely charged to  $V_{DD}$ . When the trigger input A goes from  $V_{SS}$  to  $V_{DD}$  (while inputs B and  $\overline{\text{Reset}}$  are held to  $V_{DD}$ ) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1. At the same time the output latch is set. With transistor N1 on, the capacitor  $C_X$  rapidly discharges toward  $V_{SS}$  until  $V_{ref1}$  is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor  $C_X$  begins to charge through the timing resistor,  $R_X$ , toward  $V_{DD}$ . When the voltage across  $C_X$  equals  $V_{ref2}$ , comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state,  $C_X$  is fully charged to  $V_{DD}$  causing the current through resistor  $R_X$  to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of  $C_X$ ,  $R_X$ , or the duty cycle of the input waveform.

## RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs followed by another valid trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from  $V_{ref1}$ , but has not yet reached  $V_{ref2}$ , will cause an increase in output pulse width T. When a valid retrigger is initiated, the voltage at  $C_X/R_X$  will again drop to  $V_{ref1}$  before progressing along the RC charging curve toward  $V_{DD}$ . The Q output will remain high until time T, after the last valid retrigger.

## RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on  $\overline{\text{Reset}}$  sets the reset latch and causes the capacitor to be fast charged to  $V_{DD}$  by turning on transistor P1. When the voltage on the capacitor reaches  $V_{ref2}$ , the reset latch will clear, and will then be ready to accept another pulse. If the  $\overline{\text{Reset}}$  input is held low, any trigger inputs that occur will be inhibited and the Q and  $\overline{Q}$  outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the  $\overline{\text{Reset}}$  input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

## POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing

the MC14538B is powered down, the capacitor voltage may discharge from  $V_{DD}$  through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the  $V_{DD}$  supply must not be faster than  $(V_{DD}) \cdot (C) / (10 \text{ mA})$ . For example, if  $V_{DD} = 10 \text{ V}$  and  $C_X = 10 \mu\text{F}$ , the  $V_{DD}$  supply should discharge no faster than  $(10 \text{ V}) \times (10 \mu\text{F}) / (10 \text{ mA}) = 10 \text{ ms}$ . This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{DD}$  to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode,  $D_X$ , connected as shown in Fig. 11.

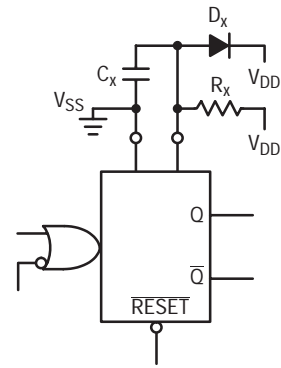


Figure 11. Use of a Diode to Limit Power Down Current Surge

TYPICAL APPLICATIONS

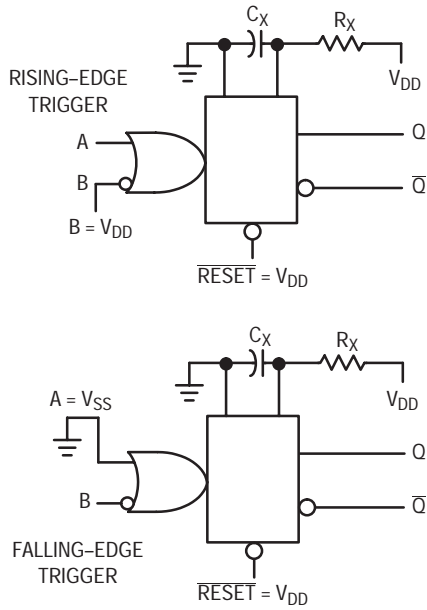


Figure 12. Retriggerable Monostables Circuitry

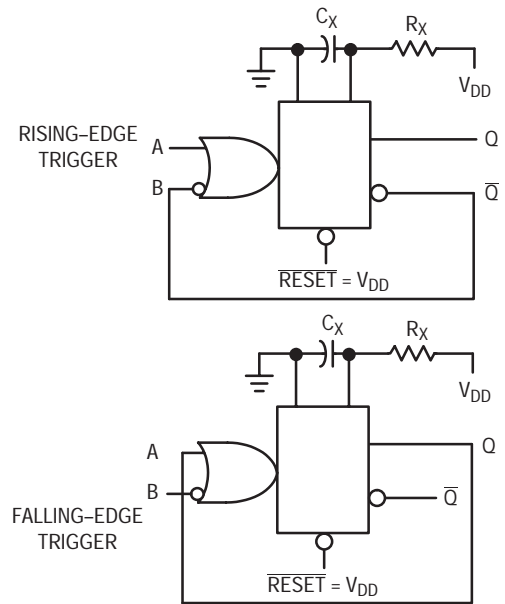


Figure 13. Non-Retriggerable Monostables Circuitry

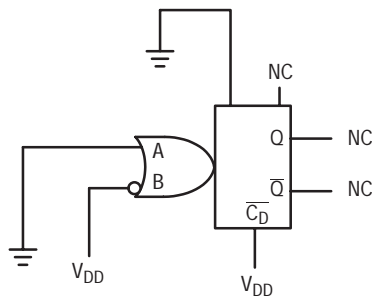


Figure 14. Connection of Unused Sections

# MC14541B

## Programmable Timer

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified  $V_{DD}$  range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency ( $f_{osc}$ ) with the  $n^{th}$  stage frequency being  $f_{osc}/2^n$ .

- Available Outputs  $2^8$ ,  $2^{10}$ ,  $2^{13}$  or  $2^{16}$
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator ( $\pm 2\%$  accuracy over temperature range and  $\pm 20\%$  supply and  $\pm 3\%$  over processing at  $< 10$  kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as  $2^n$  Frequency Divider or Single Transition Timer
- $Q/\bar{Q}$  Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 =  $V_{DD}$ )  
= 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 =  $V_{SS}$ )

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

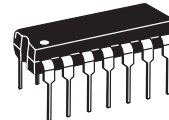
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient)	$\pm 10$ (per Pin)	mA
$I_{out}$	Output Current (DC or Transient)	$\pm 45$ (per Pin)	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

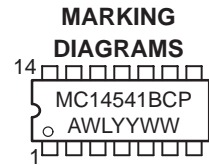


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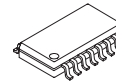
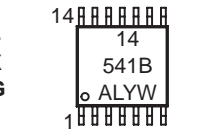
PDIP-14  
P SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14541BCP	PDIP-14	2000/Box
MC14541BD	SOIC-14	55/Rail
MC14541BDR2	SOIC-14	2500/Tape & Reel
MC14541BDT	TSSOP-14	96/Rail
MC14541BDTR2	TSSOP-14	2500/Tape & Reel
MC14541BF	SOEIAJ-14	See Note 1.
MC14541BFEL	SOEIAJ-14	See Note 1.

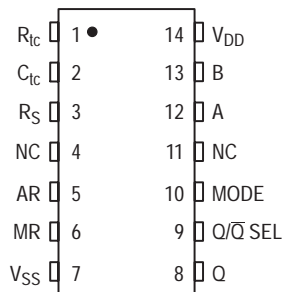
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# MC14541B

## PIN ASSIGNMENT



NC = NO CONNECTION

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max		
Output Voltage "0" Level V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
10		9.95	—	9.95	10	—	9.95	—			
15		14.95	—	14.95	15	—	14.95	—			
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
15		—	4.0	—	6.75	4.0	—	4.0			
"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
10		7.0	—	7.0	5.50	—	7.0	—			
15		11	—	11	8.25	—	11	—			
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-7.96	—	-6.42	-12.83	—	-4.49	—	mAdc
			10	-4.19	—	-3.38	-6.75	—	-2.37	—	
15			-16.3	—	-13.2	-26.33	—	-9.24	—		
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	1.93	—	1.56	3.12	—	1.09	—	mAdc
10			4.96	—	4.0	8.0	—	2.8	—		
15			19.3	—	15.6	31.2	—	10.9	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Auto Reset Quiescent Current (Pin 5 is low)	I <sub>DDR</sub>	10	—	250	—	30	250	—	1500	μAdc	
15		—	500	—	82	500	—	2000			
Supply Current <sup>(5.)</sup> <sup>(6.)</sup> (Dynamic plus Quiescent)	I <sub>D</sub>	5.0	I <sub>D</sub> = (0.4 μA/kHz) f + I <sub>DD</sub>							μAdc	
10		I <sub>D</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>									
15		I <sub>D</sub> = (1.2 μA/kHz) f + I <sub>DD</sub>									

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. When using the on chip oscillator the total supply current (in μAdc) becomes: I<sub>T</sub> = I<sub>D</sub> + 2 C<sub>tc</sub> V<sub>DD</sub> f × 10<sup>-3</sup> where I<sub>D</sub> is in μA, C<sub>tc</sub> is in pF, V<sub>DD</sub> in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power-on with automatic reset enabled is typically 50 μA @ V<sub>DD</sub> = 10 Vdc.

# MC14541B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay, Clock to Q ( $2^8$ Output) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 875 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	3.5 1.25 0.9	10.5 3.8 2.9	$\mu\text{s}$
Propagation Delay, Clock to Q ( $2^{16}$ Output) $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 3467 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2475 \text{ ns}$	$t_{PHL}, t_{PLH}$	5.0 10 15	— — —	6.0 3.5 2.5	18 10 7.5	$\mu\text{s}$
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Clock Pulse Frequency (50% Duty Cycle)	$f_{cl}$	5.0 10 15	— — —	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	$t_{WH(R)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Master Reset Removal Time	$t_{rem}$	5.0 10 15	420 200 200	210 100 100	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

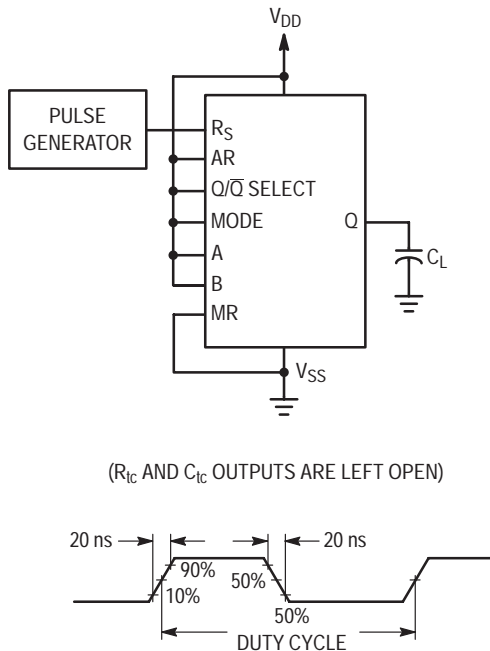


Figure 1. Power Dissipation Test Circuit and Waveform

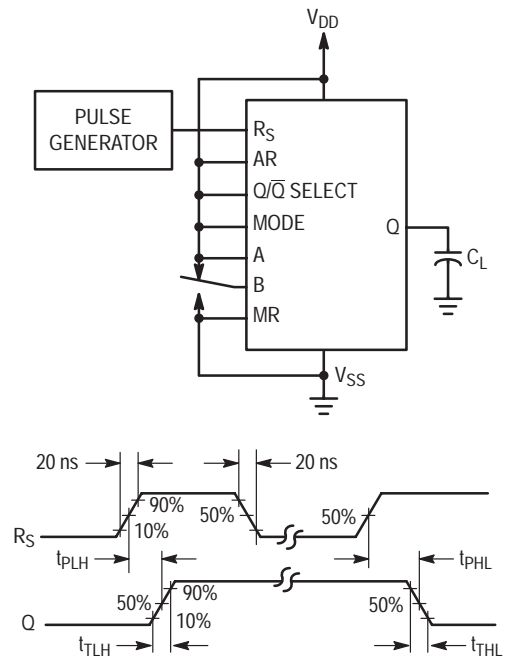
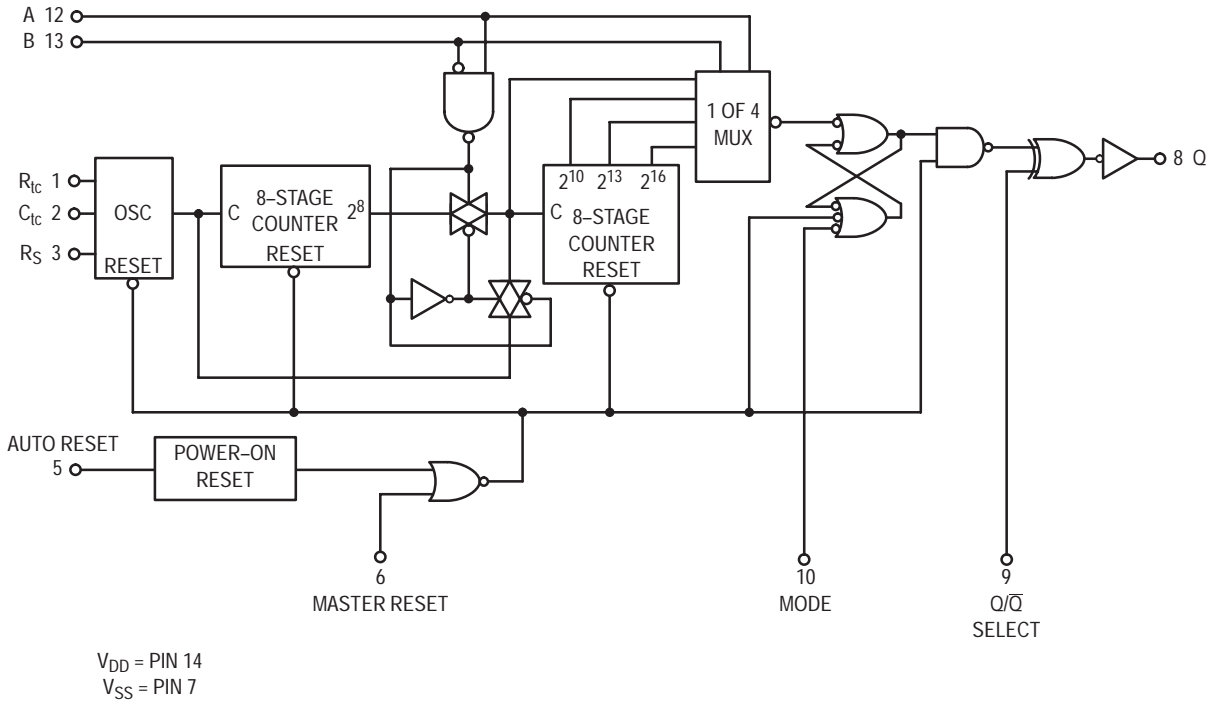


Figure 2. Switching Time Test Circuit and Waveforms



# MC14541B

## EXPANDED BLOCK DIAGRAM

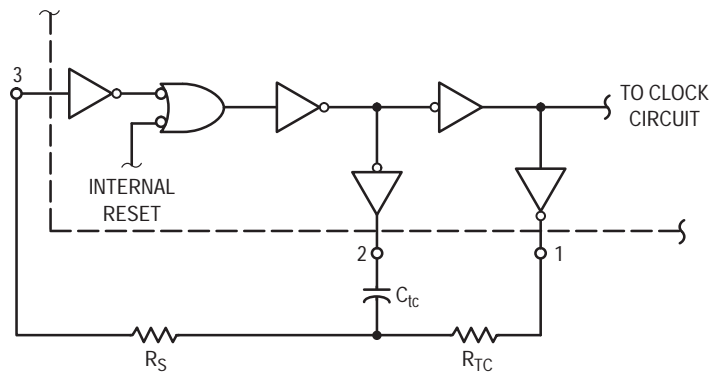


**FREQUENCY SELECTION TABLE**

A	B	Number of Counter Stages n	Count $2^n$
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

**TRUTH TABLE**

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
$Q/\bar{Q}$ , 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode



**Figure 3. Oscillator Circuit Using RC Configuration**

TYPICAL RC OSCILLATOR CHARACTERISTICS

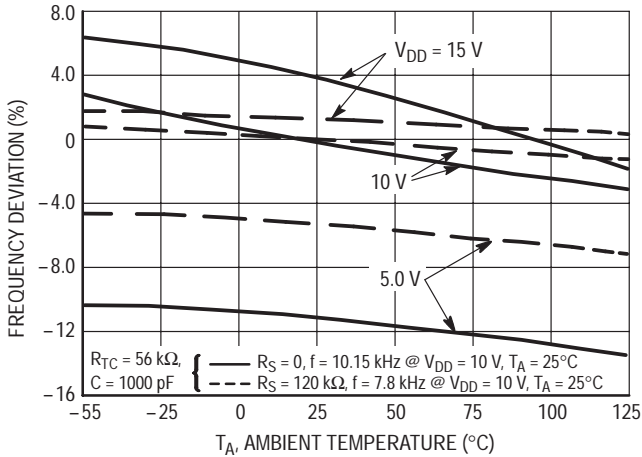


Figure 4. RC Oscillator Stability

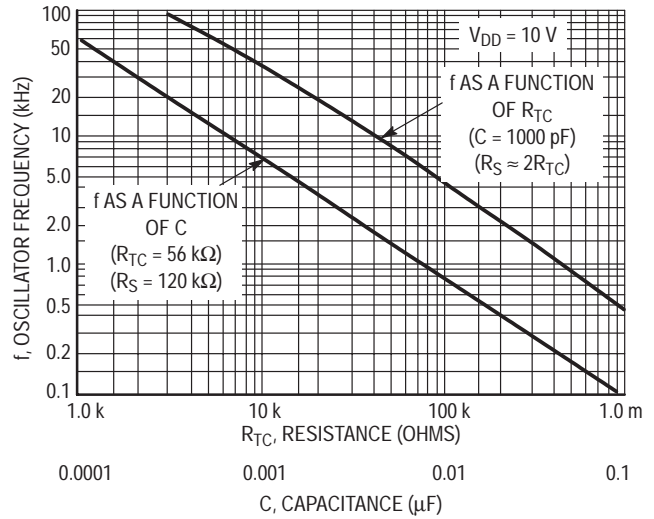


Figure 5. RC Oscillator Frequency as a Function of  $R_{tc}$  and  $C_{tc}$

OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a “1” provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad \text{if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and  $R_S \approx 2 R_{tc}$  where  $R_S \geq 10 \text{ k}\Omega$

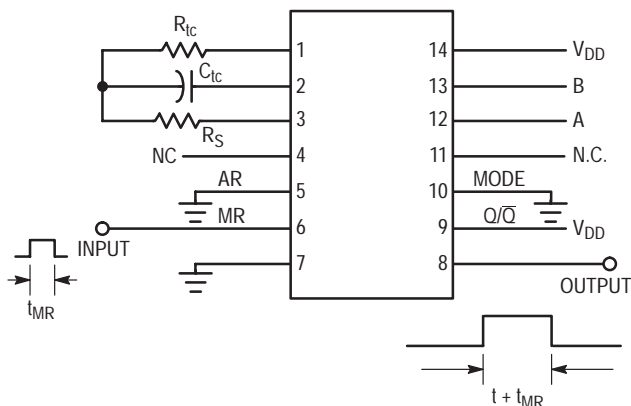
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages ( $2^8$ ,  $2^{10}$ ,  $2^{13}$  and  $2^{16}$ ). The  $2^n$  counts as shown in the Frequency Selection Table represents the Q output of the  $N^{\text{th}}$  stage of the counter. When A is “1”,  $2^{16}$  is selected for both states of B. However,

when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting  $2^8$ ).

The  $Q/\bar{Q}$  select output control pin provides for a choice of output level. When the counter is in a reset condition and  $Q/\bar{Q}$  select pin is set to a “0” the Q output is a “0”, correspondingly when  $Q/\bar{Q}$  select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the  $R_S$  flip-flop (see Expanded Block Diagram) resets, counting commences, and after  $2^{n-1}$  counts the  $R_S$  flip-flop sets which causes the output to change state. Hence, after another  $2^{n-1}$  counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

# MC14543B

## BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving 2 Low-power TTL Loads, 1 Low-power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to  $V_{SS}$ ).
- Chip Complexity: 207 FETs or 52 Equivalent Gates

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

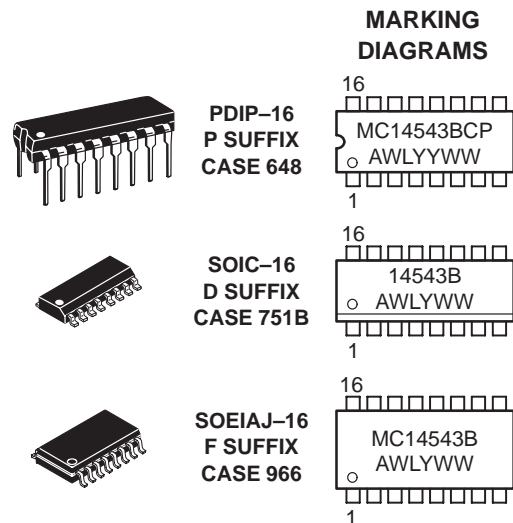
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	DC Input Current per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$I_{OHmax}$ $I_{OLmax}$	Maximum Continuous Output Drive Current (Source or Sink)	10 (per Output)	mA
$P_{OHmax}$ $P_{OLmax}$	Maximum Continuous Output Power (Source or Sink) (4.)	70 (per Output)	mW

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$
4.  $P_{OHmax} = I_{OH} (V_{OH} - V_{DD})$  and  $P_{OLmax} = I_{OL} (V_{OL} - V_{SS})$



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A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14543BCP	PDIP-16	2000/Box
MC14543BD	SOIC-16	48/Rail
MC14543BDR2	SOIC-16	2500/Tape & Reel
MC14543BF	SOEIAJ-16	See Note 1.
MC14543BFEL	SOEIAJ-16	See Note 1.

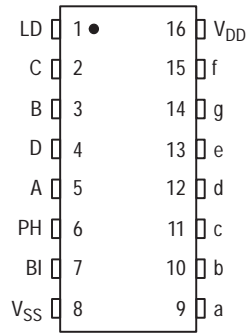
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# MC14543B

## PIN ASSIGNMENT



## TRUTH TABLE

Inputs							Outputs							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	†	†				Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

\* = For liquid crystal readouts, apply a square wave to Ph

For common cathode LED readouts, select Ph = 0

For common anode LED readouts, select Ph = 1

\*\* = Depends upon the BCD code previously applied when LD = 1

# MC14543B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(5.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“0” Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 0.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 9.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	—	—	—	-10.1	—	—	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		10	—	—	—	10.1	—	—	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
		15	—	±0.1	—	±0.00001	±0.1	—	±1.0	
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V <sub>in</sub> = 0 or V <sub>DD</sub> , I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current <sup>(6.)</sup> <sup>(7.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.1 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (4.7 μA/kHz) f + I <sub>DD</sub>							

5. Noise immunity specified for worst-case input combination.

Noise Margin for both “1” and “0” level = 1.0 V min @ V<sub>DD</sub> = 5.0 V  
2.0 V min @ V<sub>DD</sub> = 10 V  
2.5 V min @ V<sub>DD</sub> = 15 V

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in V, and f in kHz is input frequency.

7. The formulas given are for the typical characteristics only at 25°C.

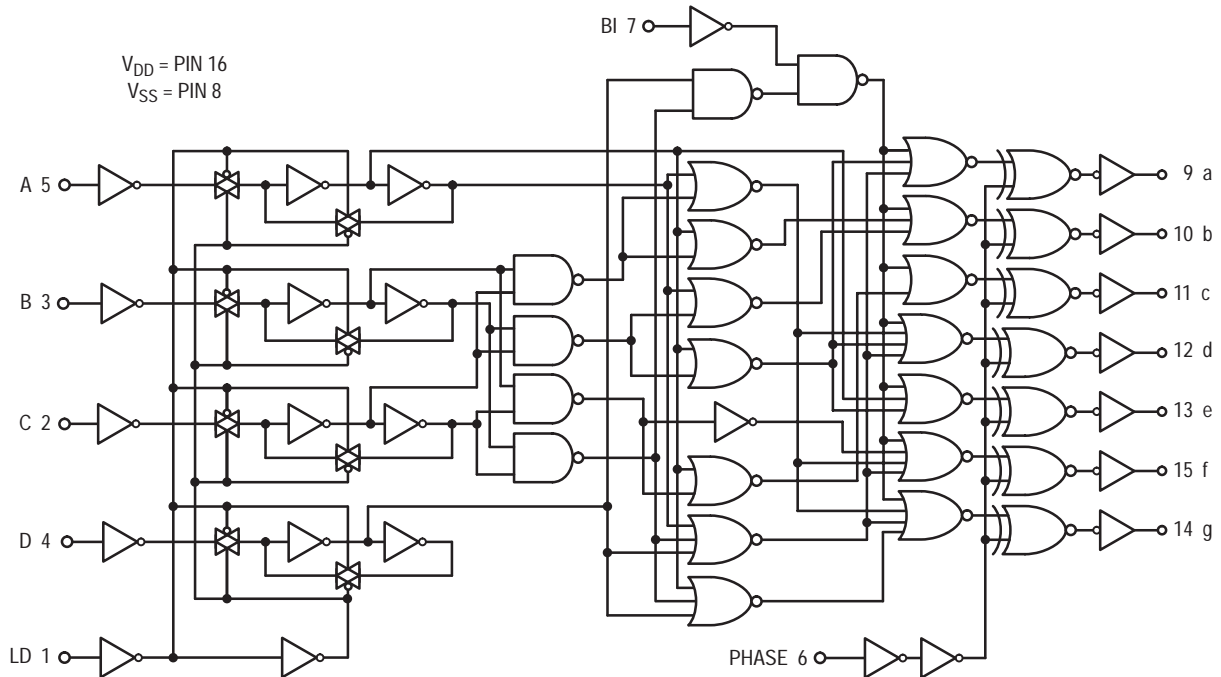
# MC14543B

## SWITCHING CHARACTERISTICS (8.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	605 250 185	1210 500 370	ns
Turn-On Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 420 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 172 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	505 205 155	1650 660 495	ns
Setup Time	$t_{su}$	5.0 10 15	350 450 500		— — —	ns
Hold Time	$t_h$	5.0 10 15	40 30 20		— — —	ns
Latch Disable Pulse Width (Strobing Data)	$t_{WH}$	5.0 10 15	250 100 80	125 50 40	— — —	ns

8. The formulas given are for the typical characteristics only.

### LOGIC DIAGRAM



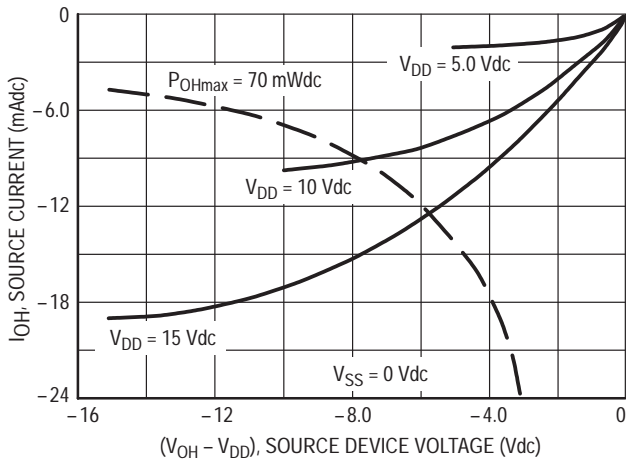


Figure 1. Typical Output Source Characteristics

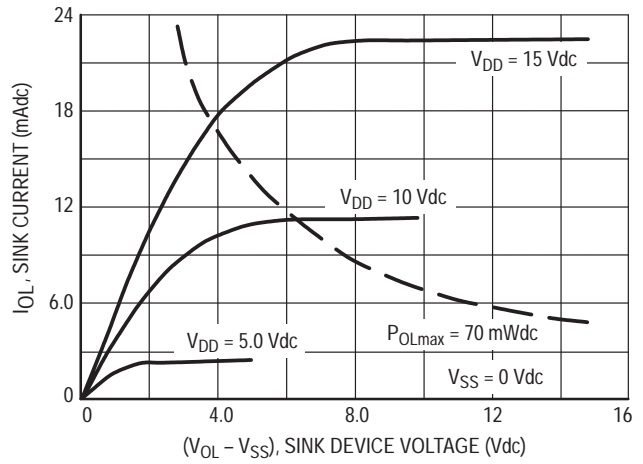


Figure 2. Typical Output Sink Characteristics

Inputs BI and Ph low, and Inputs D and LD high.  
f in respect to a system clock.

All outputs connected to respective  $C_L$  loads.

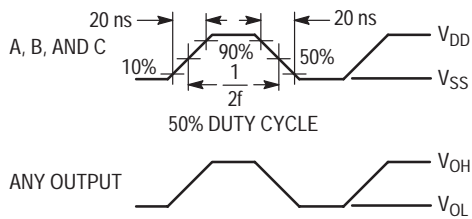
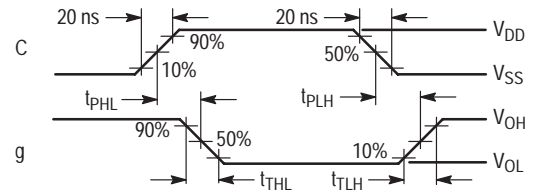
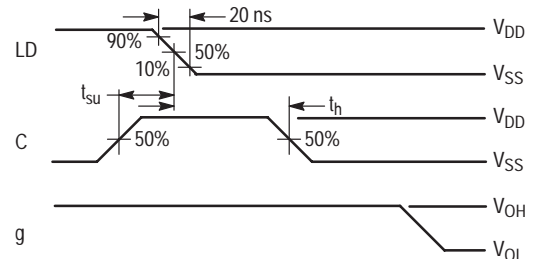


Figure 3. Dynamic Power Dissipation Signal Waveforms

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches

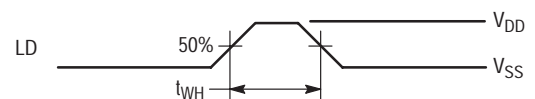
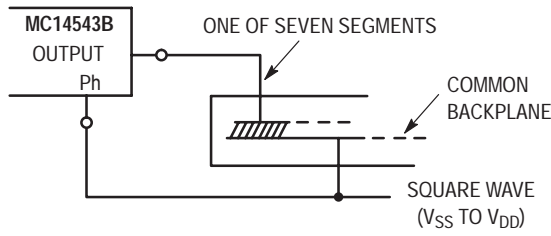


Figure 4. Dynamic Signal Waveforms

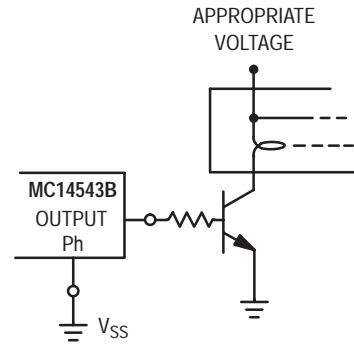
# MC14543B

## CONNECTIONS TO VARIOUS DISPLAY READOUTS

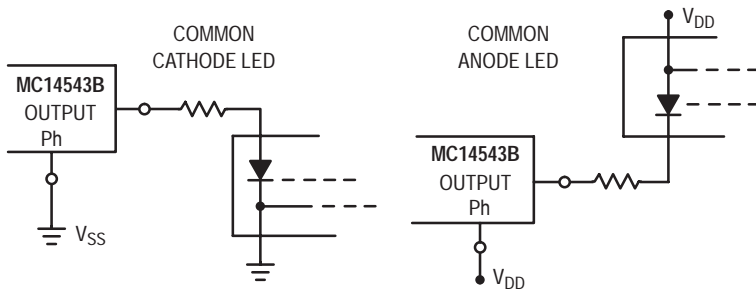
### LIQUID CRYSTAL (LC) READOUT



### INCANDESCENT READOUT

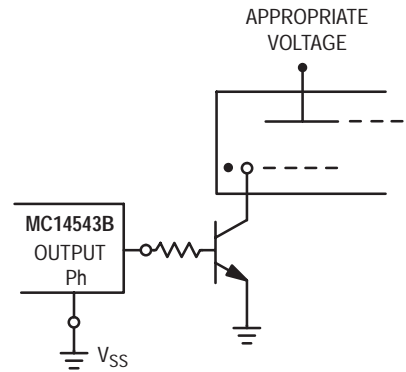


### LIGHT EMITTING DIODE (LED) READOUT

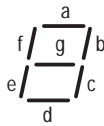


NOTE: Bipolar transistors may be added for gain (for  $V_{DD} \leq 10\text{ V}$  or  $I_{out} \geq 10\text{ mA}$ ).

### GAS DISCHARGE READOUT

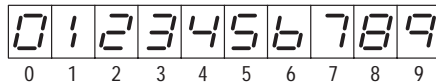


## CONNECTIONS TO SEGMENTS



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

## DISPLAY





# MC14549B, MC14559B

## Successive Approximation Registers

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when more than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog-to-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 2 Low-Power TTL Loads, 1 Low-Power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Chip Complexity: 488 FETs or 122 Equivalent Gates

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

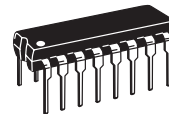
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ).



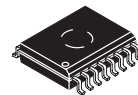
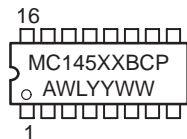
ON Semiconductor

<http://onsemi.com>

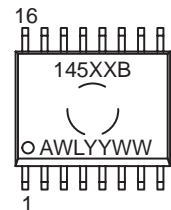
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
DW SUFFIX  
CASE 751G



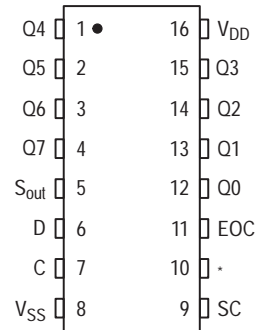
XX = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14549BCP	PDIP-16	25/Rail
MC14549BDWR2	SOIC-16	1000/Tape & Reel
MC14559BCP	PDIP-16	25/Rail
MC14559BDWR2	SOIC-16	1000/Tape & Reel

# MC14549B, MC14559B

## PIN ASSIGNMENT



\*For MC14549B Pin 10 is MR input.  
For MC14559B Pin 10 is FF input.

## MC14549B TRUTH TABLES MC14559B

SC	SC <sub>(t-1)</sub>	MR	MR <sub>(t-1)</sub>	Clock	Action
X	X	X	X		None
X	X	1	X		Reset
1	0	0	0		Start Conversion
1	X	0	1		Start Conversion
1	1	0	0		Continue Conversion
0	X	0	X		Continue Previous Operation

X = Don't Care t-1 = State at Previous Clock

SC	SC <sub>(t-1)</sub>	EOC	Clock	Action
X	X	X		None
1	0	0		Start Conversion
X	1	0		Continue Conversion
0	0	0		Continue Conversion
0	X	1		Retain Conversion Result
1	X	1		Start Conversion

# MC14549B, MC14559B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage <sup>(3.)</sup> (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source	I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
			5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
			10	-0.62	—	-0.5	-0.9	—	-0.35	—	
			15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink Q Outputs	I <sub>OL</sub>	5.0	1.28	—	1.02	1.76	—	0.72	—	mAdc
			10	3.2	—	2.6	4.5	—	1.8	—	
			15	8.4	—	6.8	17.6	—	4.8	—	
	Sink Pin 5, 11 only	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
15			4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package) (Clock = 0 V, Other Inputs = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 μA)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
10	—	10	—	0.010	10	—	300				
15	—	20	—	0.015	20	—	600				
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>							μAdc	
10	I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub>										
15	I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub>										

3. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @ V<sub>DD</sub> = 5.0 V  
 2.0 V min @ V<sub>DD</sub> = 10 V  
 2.5 V min @ V<sub>DD</sub> = 15 V

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L = 50) V_{DD} f$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in V, and f in kHz is input frequency.

5. The formulas given are for the typical characteristics only at 25°C.

# MC14549B, MC14559B

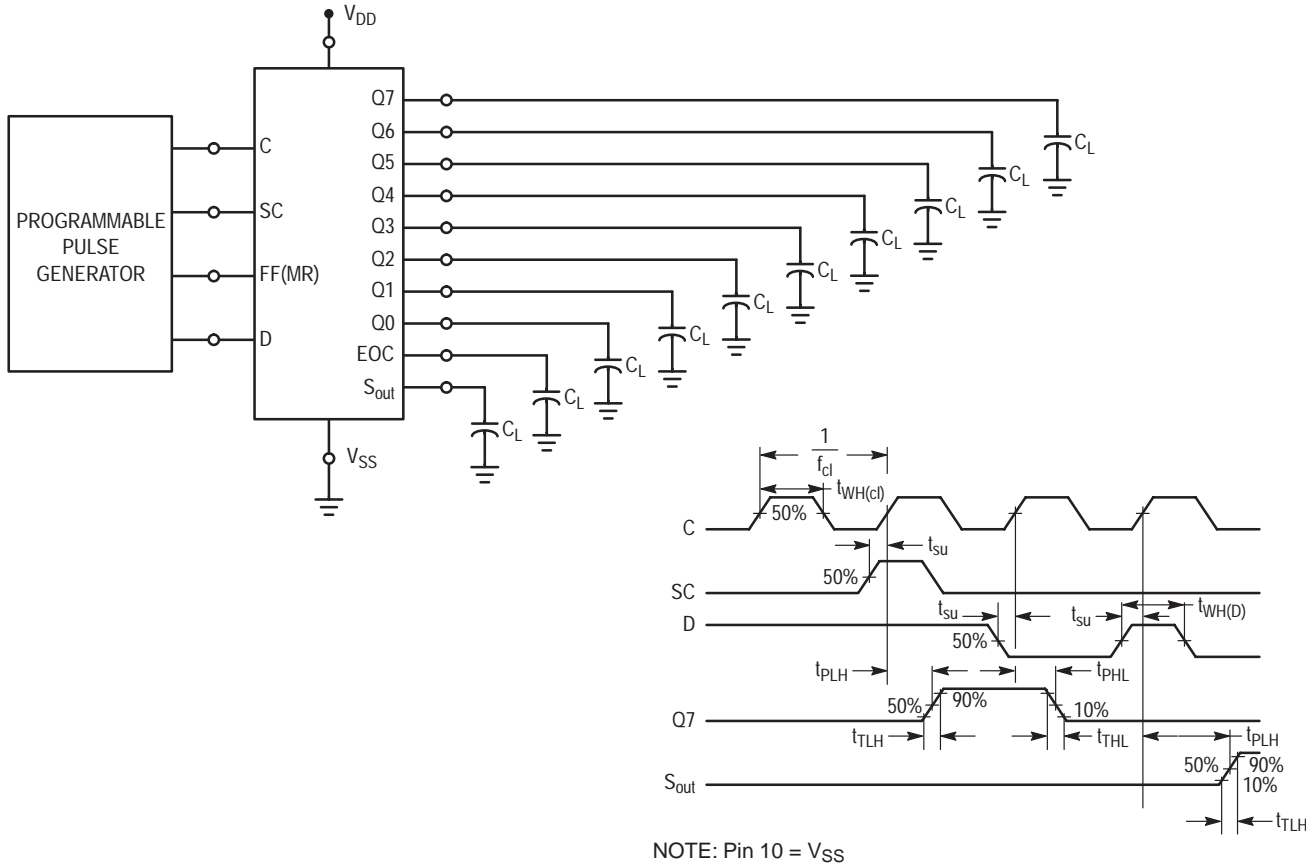
## SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$ Clock to S <sub>out</sub> $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 665 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 277 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 195 \text{ ns}$ Clock to EOC $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15	— — —  — — —  — — —	500 210 155  750 310 220  300 130 100	1000 420 310  1500 620 440  600 260 200	ns
SC, D, FF or MR Setup Time	$t_{su}$	5.0 10 15	250 100 80	125 50 40	— — —	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	700 270 200	350 135 100	— — —	ns
Pulse Width — D, SC, FF or MR	$t_{WH}$	5.0 10 15	500 200 160	250 100 80	— — —	ns
Clock Rise and Fall Time	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	— — —	15 1.0 0.5	$\mu\text{s}$
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	1.5 3.0 4.0	0.8 1.5 2.0	MHz

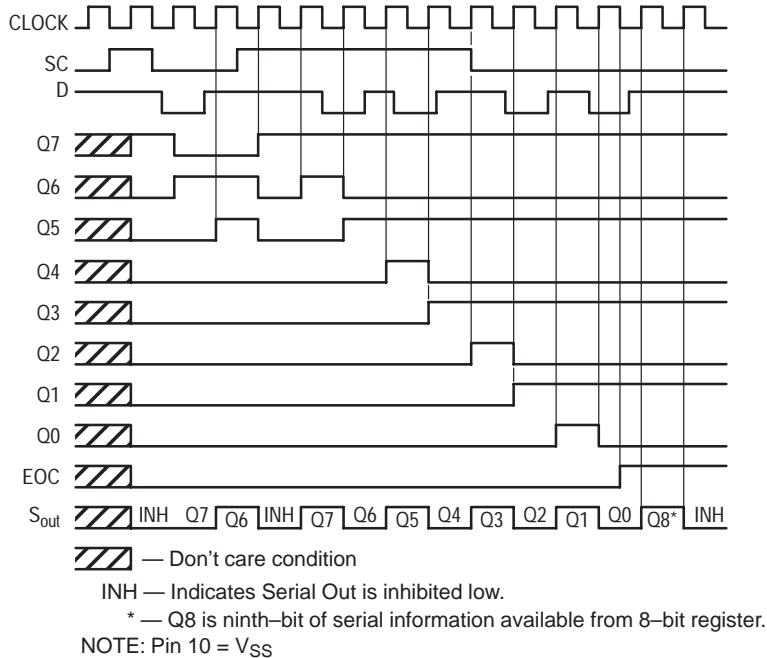
6. The formulas given are for the typical characteristics only.

# MC14549B, MC14559B

## SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



### TIMING DIAGRAM



# MC14549B, MC14559B

## OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the “free run” or “strobed operation” mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with  $EOC = 0$  (and with  $SC = 1$  for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after  $EOC = 1$  during externally strobed operation, provided  $SC = 1$ .

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

**C = Clock** — A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

**SC = Start Convert** — A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

**D = Data in** — Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

**MR = Master Reset (MC14549B Only)** — Resets all output to 0 on positive-going transitions of the clock. If removed while  $SC = 0$ , the circuit will remain reset until  $SC = 1$ . This allows easy cascading of circuits.

**FF = Feed Forward (MC14559B Only)** — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit

conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q1 and Q0 will still operate and must be disregarded.

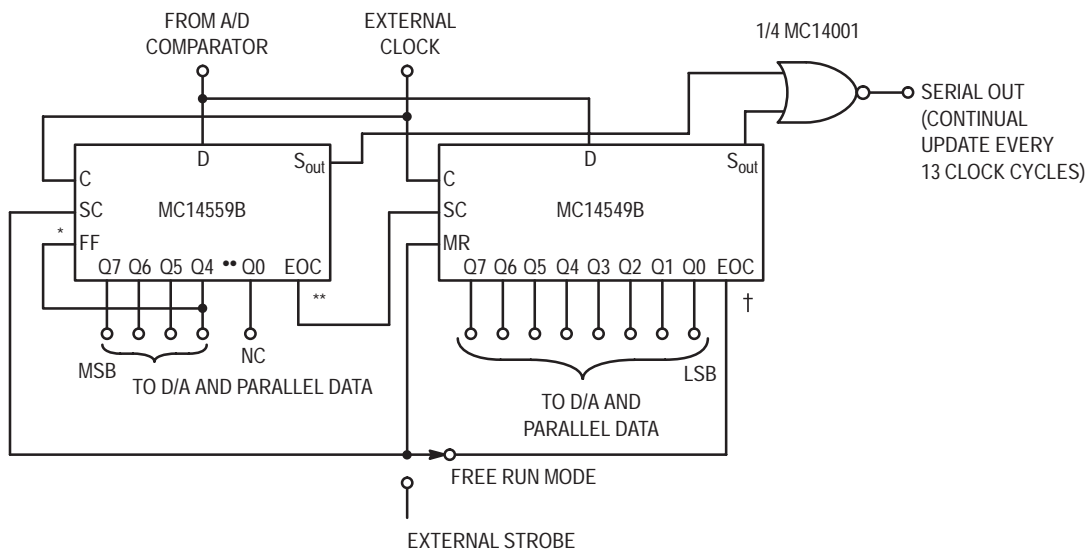
For 8-bit operation, FF is tied to  $V_{SS}$ .

For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out ( $S_{out}$ ) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while  $S_{out}$  of the MC14549B remains inhibited until the second clock cycle of its operation.

**$Q_n =$  Data Outputs** — After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

**EOC = End of Convert** — This output goes high on the negative-going transition of the clock following  $FF = 1$  (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

**$S_{out} =$  Serial Out** — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.



\* FF allows EOC to activate as if in 4-stage register.

\*\* Cascading using EOC guaranteed; no stable unfunctional state.

† Completion of conversion automatically re-initiates cycle in free run mode.

Figure 1. 12-Bit Conversion Scheme

TYPICAL APPLICATIONS

**Externally Controlled 6–Bit ADC (Figure 2)**

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

**Continuously Cycling 8–Bit ADC (Figure 3)**

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

**Continuously Cycling 12–Bit ADC (Figure 4)**

Because each successive approximation register (SAR) has a capability of handling only an eight–bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch–on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non–functional condition.

This 12–bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of the 12–bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

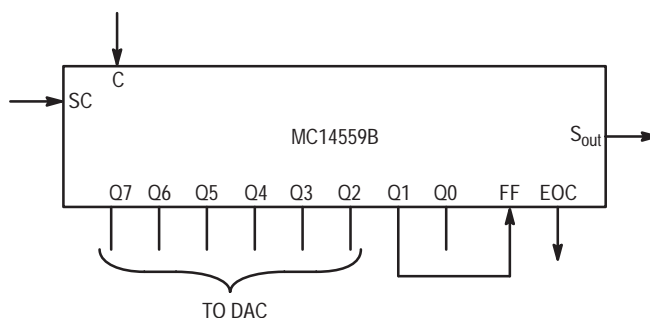


Figure 2. Externally Controlled 6–Bit ADC

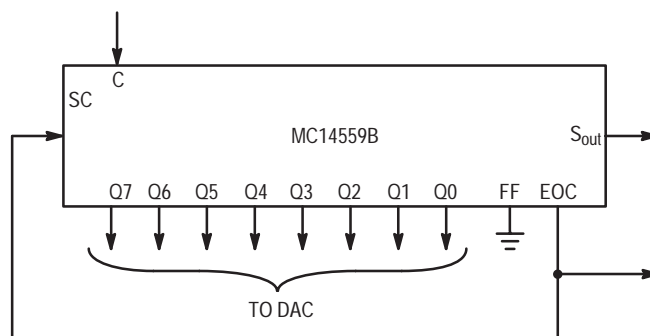


Figure 3. Continuously Cycling 8–Bit ADC

## MC14549B, MC14559B

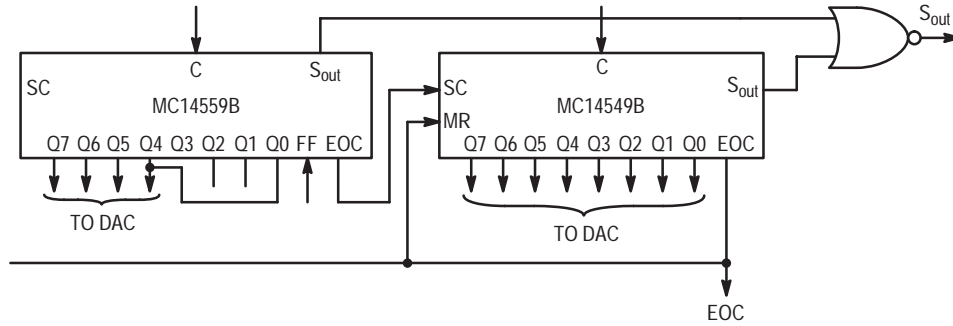


Figure 4. Continuously Cycling 12-Bit ADC

### Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

### Additional Motorola Parts for Successive Approximation ADC

**Monolithic digital-to-analog converters** — The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** — The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

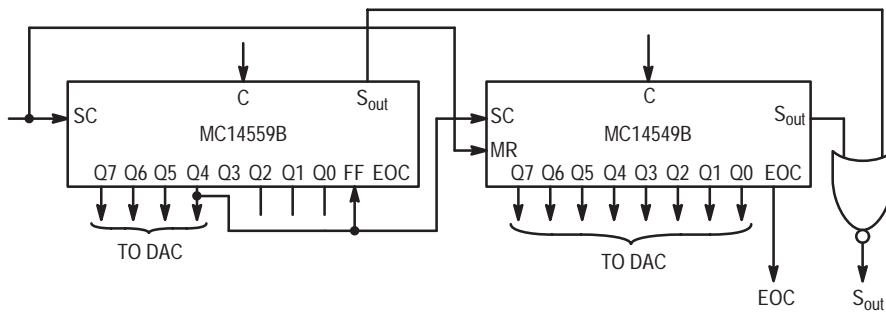


Figure 5. Externally Controlled 12-Bit ADC



# MC14551B

## Quad 2-Channel Analog Multiplexer/Demultiplexer

The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 to 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low Noise —  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  typical
- For Low  $R_{ON}$ , Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices
- Switch Function is Break Before Make

### MAXIMUM RATINGS (2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range (Referenced to $V_{EE}$ , $V_{SS} \geq V_{EE}$ )	- 0.5 to + 18.0	V
$V_{in}$ , $V_{out}$	Input or Output Voltage (DC or Transient) (Referenced to $V_{SS}$ for Control Input & $V_{EE}$ for Switch I/O)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package (3.)	500	mW
$T_A$	Ambient Temperature Range	- 55 to + 125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	- 65 to + 150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for control inputs and  $V_{EE} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$ ,  $V_{EE}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor

<http://onsemi.com>

**MARKING DIAGRAMS**

**PDIP-16 P SUFFIX CASE 648**

**SOIC-16 D SUFFIX CASE 751B**

**SOEIAJ-16 F SUFFIX CASE 966**

A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

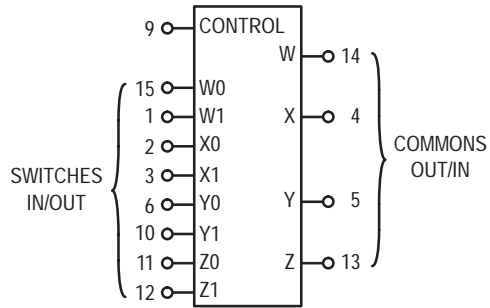
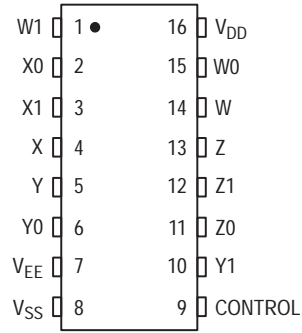
### ORDERING INFORMATION

Device	Package	Shipping
MC14551BCP	PDIP-16	2000/Box
MC14551BD	SOIC-16	48/Rail
MC14551BDR2	SOIC-16	2500/Tape & Reel
MC14551BF	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14551B

## PIN ASSIGNMENT



V<sub>DD</sub> = Pin 16  
V<sub>SS</sub> = Pin 8  
V<sub>EE</sub> = Pin 7

Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

NOTE: Control Input referenced to V<sub>SS</sub>. Analog Inputs and Outputs reference to V<sub>EE</sub>. V<sub>EE</sub> must be ≤ V<sub>SS</sub>.

# MC14551B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (4.)	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV (5.)	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>							μA

### CONTROL INPUT (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V<sub>EE</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch (5.) (Figure 3)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV (5.), V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 8)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

- Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
- For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14551B

## ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ , $V_{EE} \leq V_{SS}$ )

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ (6.)	Max	Unit
Propagation Delay Times Switch Input to Switch Output ( $R_L = 10 \text{ k}\Omega$ ) $t_{PLH}$ , $t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	35 15 12	90 40 30	ns
Control Input to Output ( $R_L = 10 \text{ k}\Omega$ ) $V_{EE} = V_{SS}$ (Figure 4)	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	350 140 100	875 350 250	ns
Second Harmonic Distortion $R_L = 10 \text{ k}\Omega$ , $f = 1 \text{ kHz}$ , $V_{in} = 5 V_{p-p}$	—	10	—	0.07	—	%
Bandwidth (Figure 5) $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})_{p-p}$ , $20 \text{ Log} (V_{out}/V_{in}) = -3 \text{ dB}$ , $C_L = 50 \text{ pF}$	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})_{p-p}$ , $f_{in} = 55 \text{ MHz}$	—	10	—	-50	—	dB
Channel Separation (Figure 6) $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})_{p-p}$ , $f_{in} = 3 \text{ MHz}$	—	10	—	-50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$ , Control $t_r = t_f = 20 \text{ ns}$	—	10	—	75	—	mV

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14551B

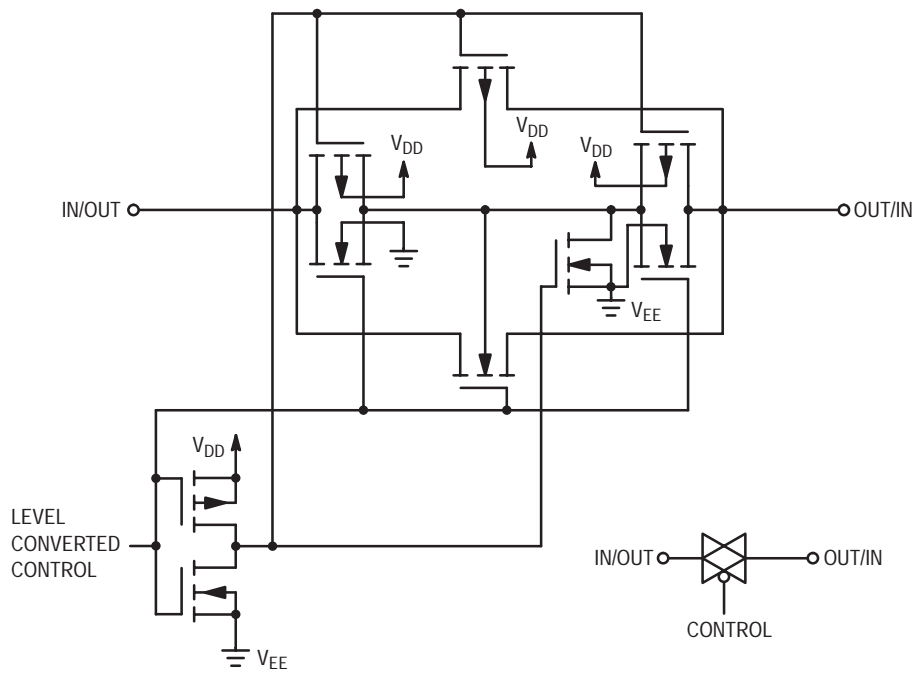


Figure 1. Switch Circuit Schematic

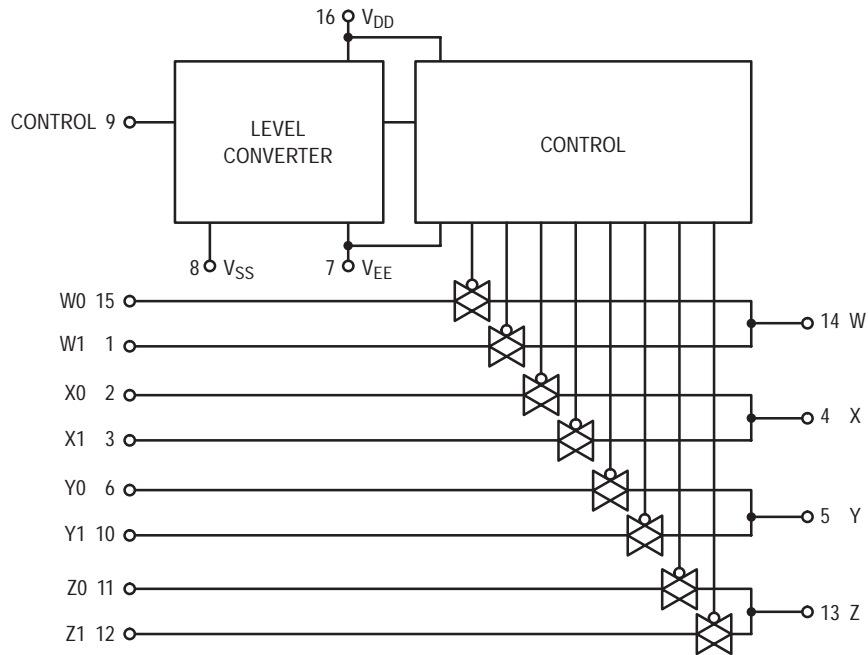


Figure 2. MC14551B Functional Diagram

# MC14551B

## TEST CIRCUITS

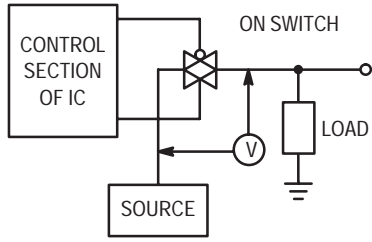


Figure 3.  $\Delta V$  Across Switch

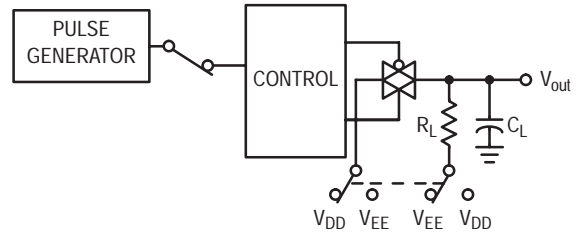


Figure 4. Propagation Delay Times, Control to Output

Control input used to turn ON or OFF the switch under test.

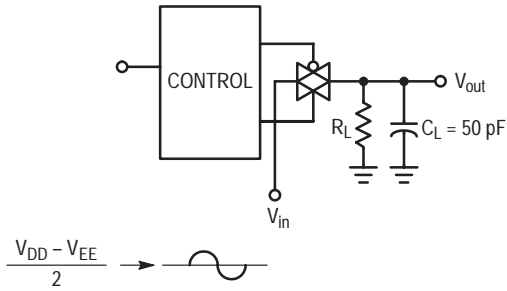


Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation

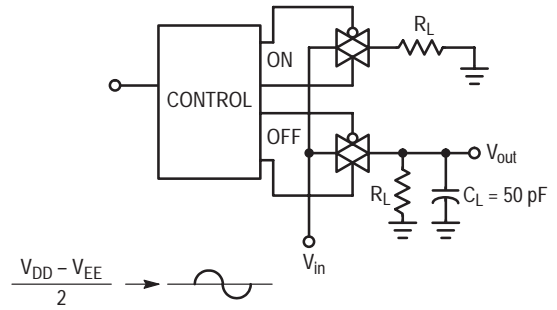


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

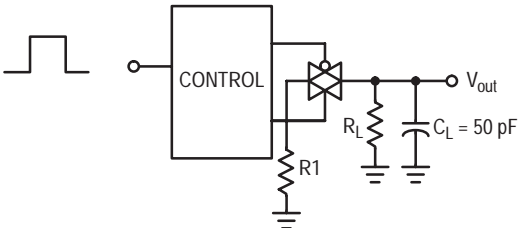


Figure 7. Crosstalk, Control Input to Common O/I

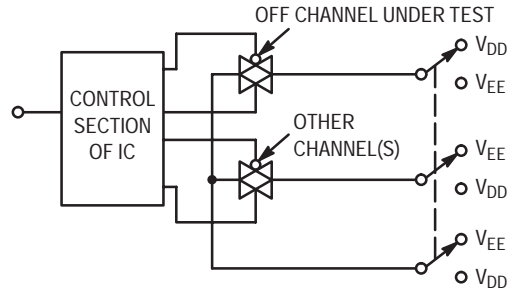


Figure 8. Off Channel Leakage

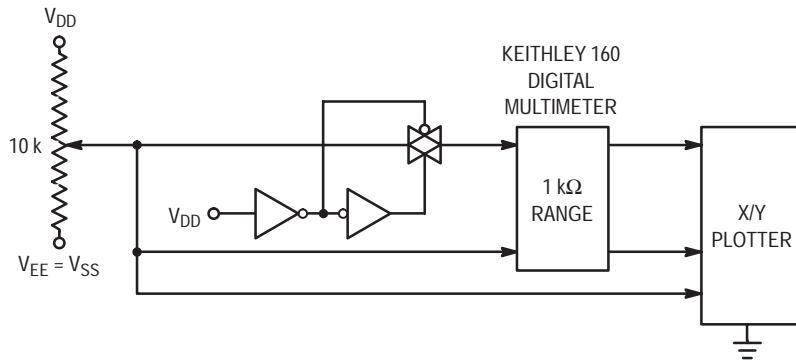


Figure 9. Channel Resistance ( $R_{ON}$ ) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

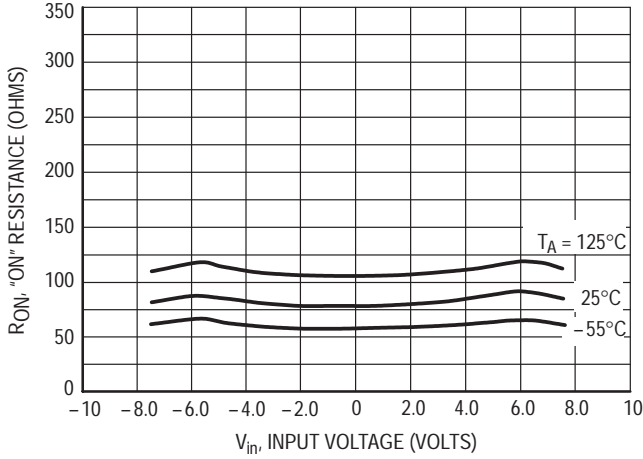


Figure 10.  $V_{DD}$  @ 7.5 V,  $V_{EE}$  @ -7.5 V

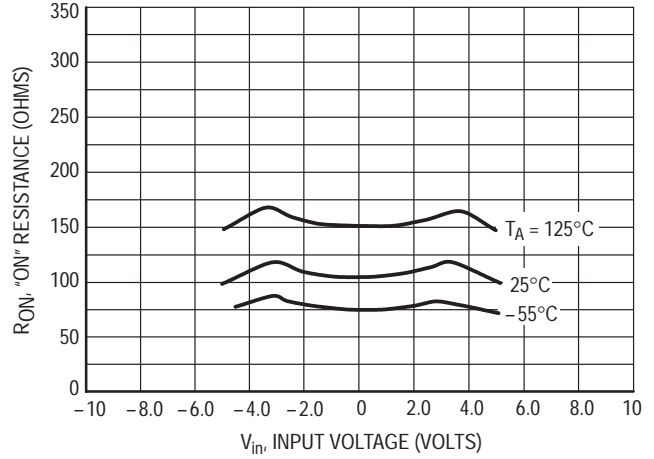


Figure 11.  $V_{DD}$  @ 5.0 V,  $V_{EE}$  @ -5.0 V

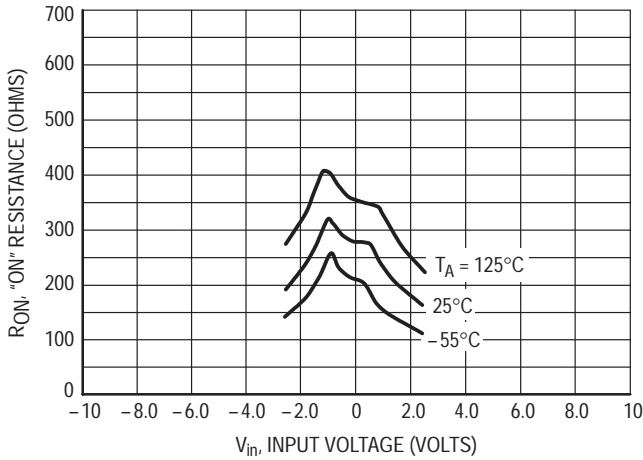


Figure 12.  $V_{DD}$  @ 2.5 V,  $V_{EE}$  @ -2.5 V

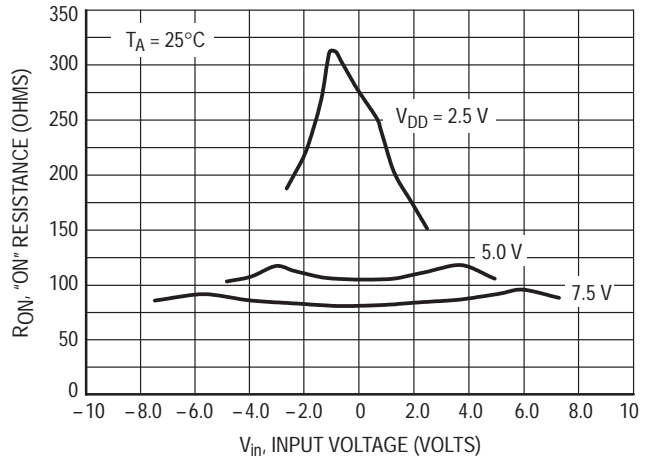


Figure 13. Comparison at 25°C,  $V_{DD}$  @ - $V_{EE}$

# MC14551B

## APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above V<sub>SS</sub>. The V<sub>EE</sub> voltage determines the maximum swing below V<sub>SS</sub>. For the example, V<sub>DD</sub> - V<sub>SS</sub> = 5 volt maximum swing above V<sub>SS</sub>; V<sub>SS</sub> - V<sub>EE</sub> = 5 volt maximum swing below V<sub>SS</sub>. The example shows a ± 4.5 volt signal which allows a 1/2 volt

margin at each peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to V<sub>EE</sub>. For example, V<sub>DD</sub> = +10 volts, V<sub>SS</sub> = +5 volts, and V<sub>EE</sub> = -3 volts is acceptable. See the table below.

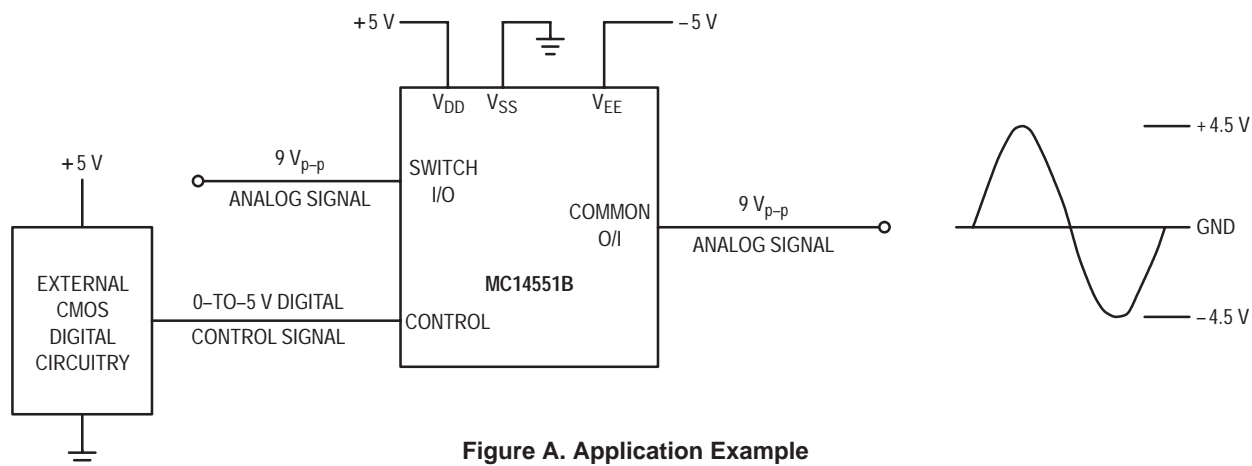


Figure A. Application Example



Figure B. External Schottky or Germanium Clipping Diodes

### POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	- 8	+ 8/0	+ 8 to - 8 = 16 V <sub>p-p</sub>
+ 5	0	- 12	+ 5/0	+ 5 to - 12 = 17 V <sub>p-p</sub>
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V <sub>p-p</sub>
+ 5	0	- 5	+ 5/0	+ 5 to - 5 = 10 V <sub>p-p</sub>
+ 10		- 5	+ 10/ + 5	+ 10 to - 5 = 15 V <sub>p-p</sub>



# MC14553B

## 3-Digit BCD Counter

The MC14553B 3-digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	+20	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

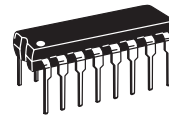
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



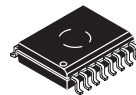
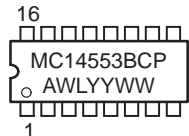
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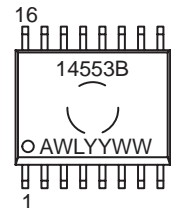
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
DW SUFFIX  
CASE 751G



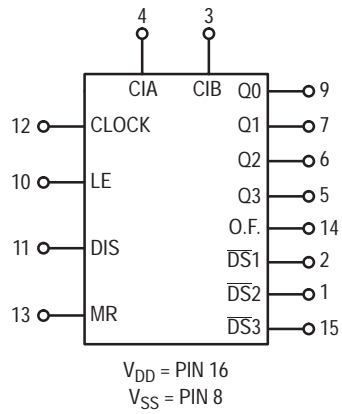
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14553BCP	PDIP-16	25/Rail
MC14553BDW	SOIC-16	47/Rail

# MC14553B

## BLOCK DIAGRAM



## TRUTH TABLE

Inputs				Outputs
Master Reset	Clock	Disable	LE	
0		0	0	No Change
0		0	0	Advance
0	X	1	X	No Change
0	1		0	Advance
0	1		0	No Change
0	0	X	X	No Change
0	X	X		Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max			
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—	
			10	9.95	—	9.95	10	—	9.95		—	
			15	14.95	—	14.95	15	—	14.95		—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5		—	
			10	7.0	—	7.0	5.50	—	7.0		—	
			15	11	—	11	8.25	—	11		—	
Output Drive Current (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source — Pin 3	I <sub>OH</sub>	5.0	-0.25	—	-0.2	-0.36	—	0.14	—	mAdc	
			10	-0.62	—	-0.5	-0.9	—	0.35	—		
			15	-1.8	—	-1.5	-3.5	—	1.1	—		
		Source — Other Outputs	I <sub>OL</sub>	5.0	-0.64	—	-0.51	-0.88	—	-0.36		—
				10	-1.6	—	-1.3	-2.25	—	-0.9		—
				15	-4.2	—	-3.4	-8.8	—	-2.4		—
	(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink — Pin 3	I <sub>OL</sub>	5.0	0.5	—	0.4	0.88	—	0.28	—	
				10	1.1	—	0.9	2.25	—	0.65	—	
				15	1.8	—	1.5	8.8	—	1.20	—	
		Sink — Other Outputs	I <sub>OL</sub>	5.0	3.0	—	2.5	4.0	—	1.6	—	
				10	6.0	—	5.0	8.0	—	3.5	—	
				15	18	—	15	20	—	10	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc		
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current (Per Package) MR = V <sub>DD</sub>	I <sub>DD</sub>	5.0	—	5.0	—	0.010	5.0	—	150	μAdc		
		10	—	10	—	0.020	10	—	300			
		15	—	20	—	0.030	20	—	600			
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.35 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.85 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.50 μA/kHz) f + I <sub>DD</sub>							μAdc		

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14553B

## SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Figure	Symbol	$V_{DD}$	Min	Typ <sup>(7.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	2a	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Clock to BCD Out	2a	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	$t_{PHL}$	5.0 10 15	— — —	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	$t_{PHL}$	5.0 10 15	— — —	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	$t_{su}$	5.0 10 15	600 400 200	300 200 100	— — —	ns
Removal Time Latch Enable to Clock	2b	$t_{rem}$	5.0 10 15	- 80 - 10 0	- 200 - 70 - 50	— — —	ns
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0 10 15	550 200 150	275 100 75	— — —	ns
Reset Pulse Width	2b	$t_{WH(R)}$	5.0 10 15	1200 600 450	600 300 225	— — —	ns
Reset Removal Time	—	$t_{rem}$	5.0 10 15	- 80 0 20	- 180 - 50 - 30	— — —	ns
Input Clock Frequency	2a	$f_{cl}$	5.0 10 15	— — —	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	$t_{TLH}$	5.0 10 15	No Limit			ns
Disable, MR, Latch Enable Rise and Fall Times	—	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5.0 4.0	$\mu\text{s}$
Scan Oscillator Frequency (C1 measured in $\mu\text{F}$ )	1	$f_{osc}$	5.0 10 15	— — —	1.5/C1 4.2/C1 7.0/C1	— — —	Hz

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14553B

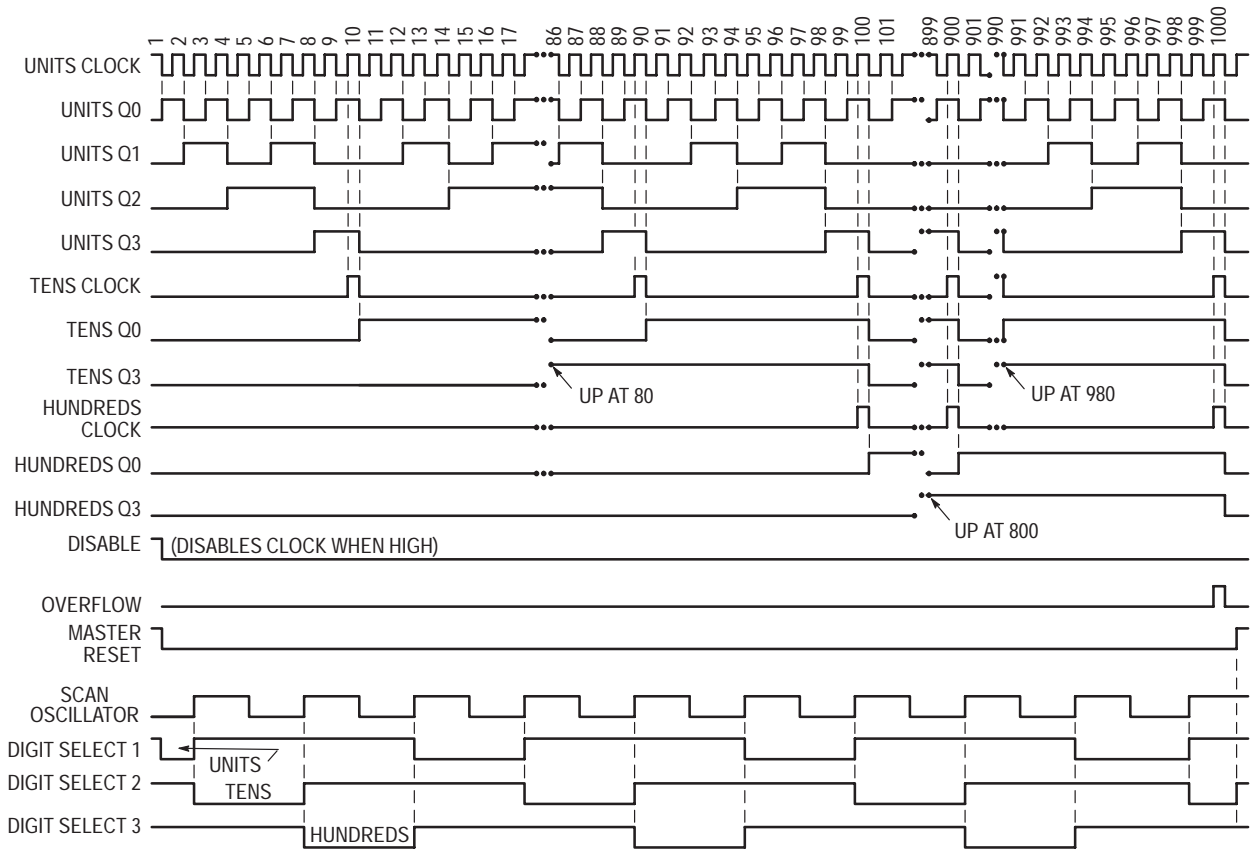


Figure 1. 3-Digit Counter Timing Diagram (Reference Figure 3)

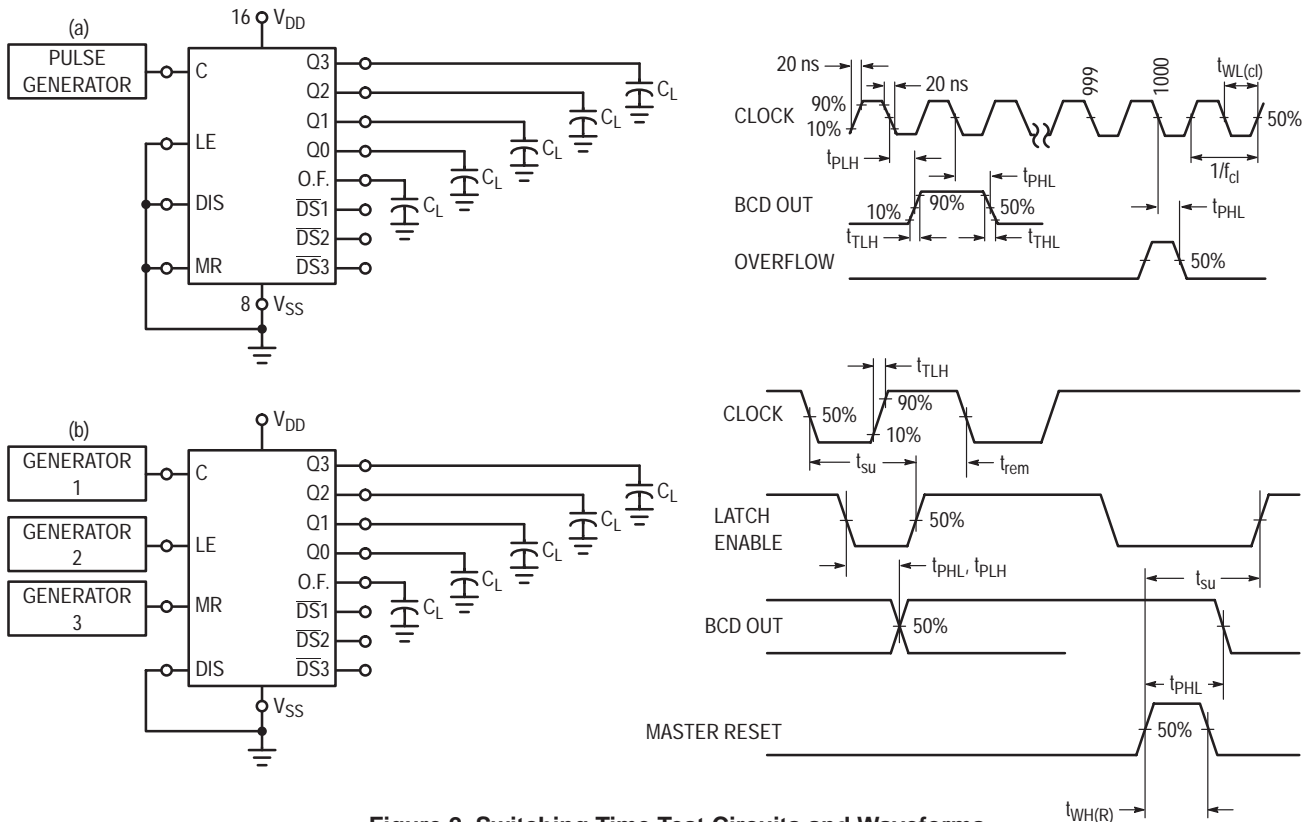


Figure 2. Switching Time Test Circuits and Waveforms

OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 3, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

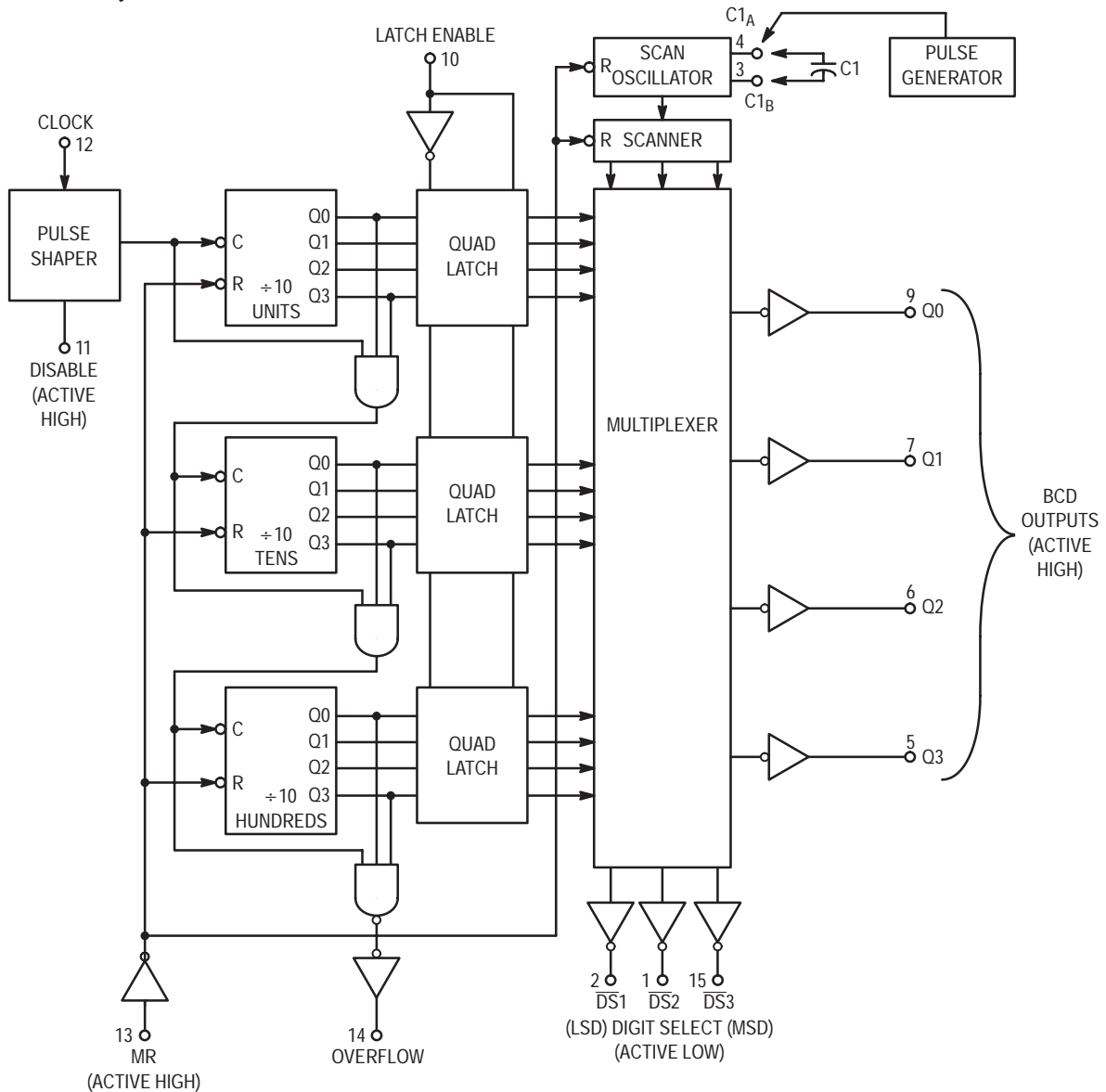


Figure 3. Expanded Block Diagram

# MC14553B

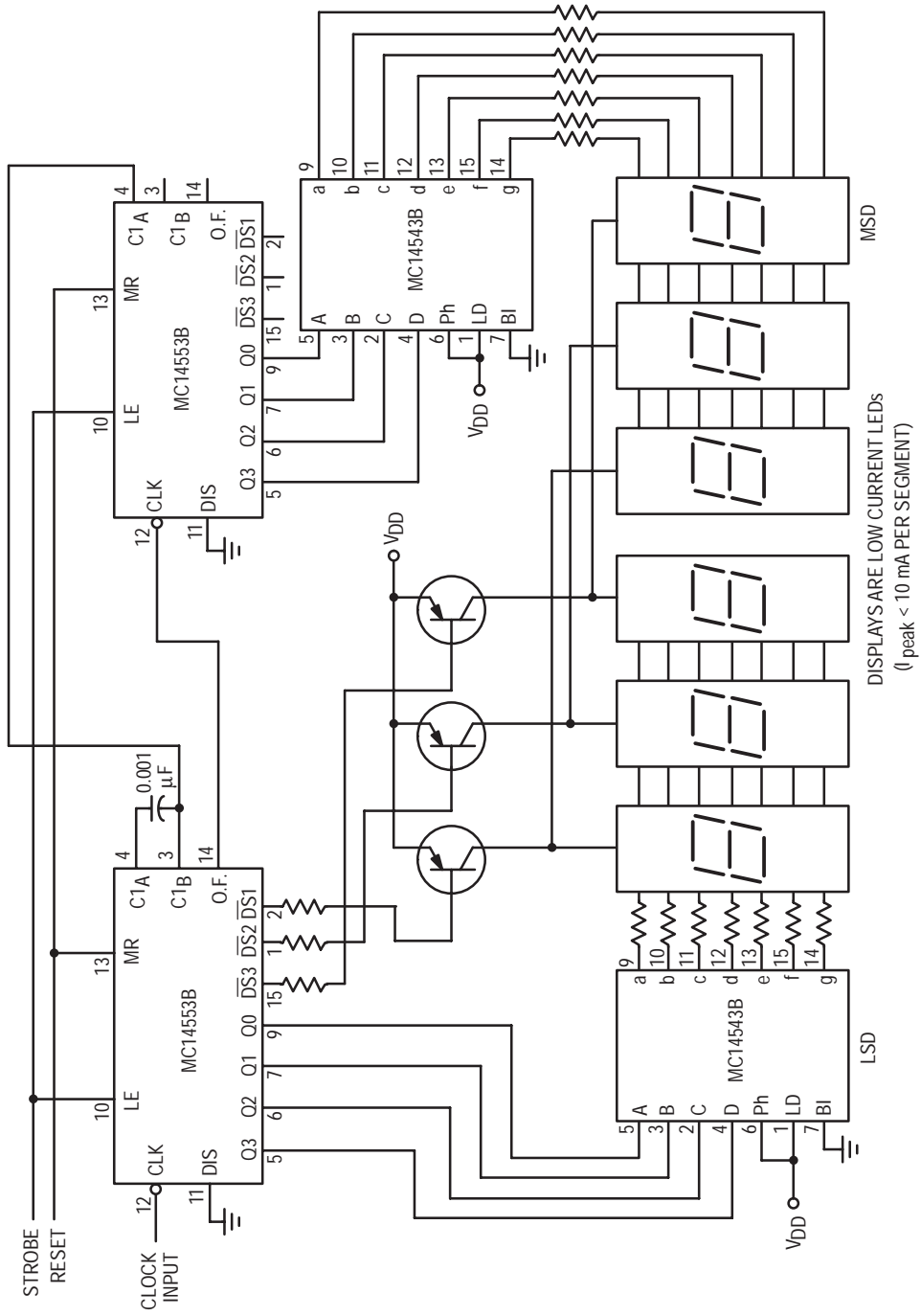


Figure 4. Six-Digit Display

# MC14555B, MC14556B

## Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the “high” state, and the MC14556B has the selected output go to the “low” state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

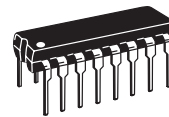
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



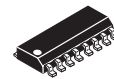
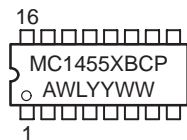
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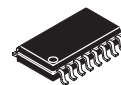
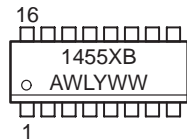
### MARKING DIAGRAMS



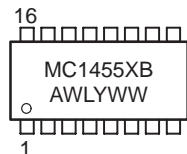
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



X = Specific Device Code  
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

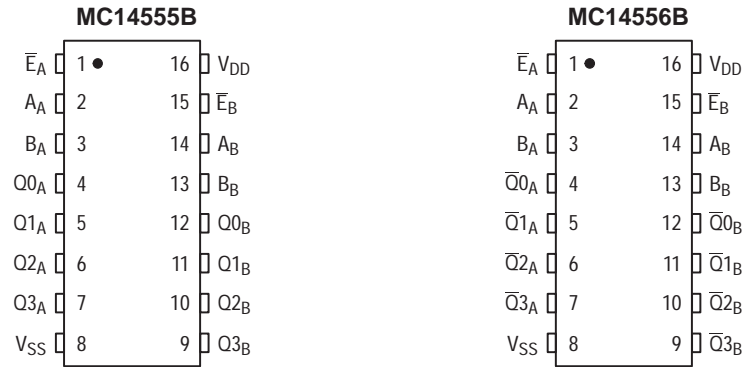
Device	Package	Shipping
MC14555BCP	PDIP-16	2000/Box
MC14555BD	SOIC-16	48/Rail
MC14555BDR2	SOIC-16	2500/Tape & Reel
MC14555BF	SOEIAJ-16	See Note 1.
MC14555BFEL	SOEIAJ-16	See Note 1.
MC14556BCP	PDIP-16	2000/Box
MC14556BD	SOIC-16	48/Rail
MC14556BDR2	SOIC-16	2500/Tape & Reel
MC14556BF	SOEIAJ-16	See Note 1.
MC14556BFEL	SOEIAJ-16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.



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## PIN ASSIGNMENTS

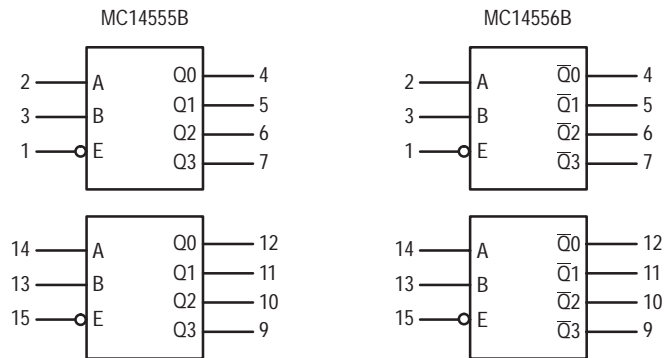


## TRUTH TABLE

Inputs			Outputs							
Enable	Select		MC14555B				MC14556B			
E	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

## BLOCK DIAGRAM



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.85 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.70 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.60 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

# MC14555B, MC14556B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — A, B to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	220 95 70	440 190 140	ns
Propagation Delay Time — E to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 52 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	200 85 65	400 170 130	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

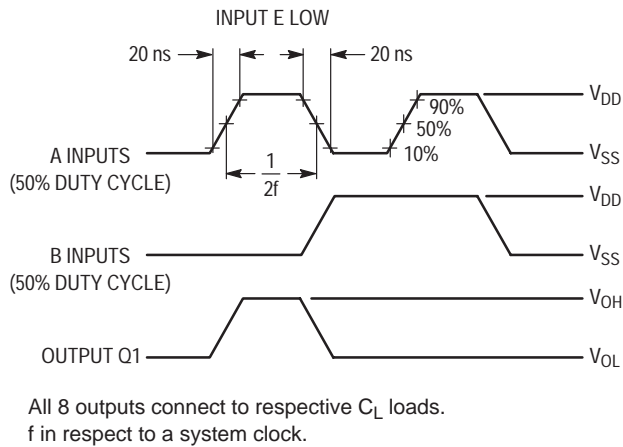


Figure 1. Dynamic Power Dissipation Signal Waveforms

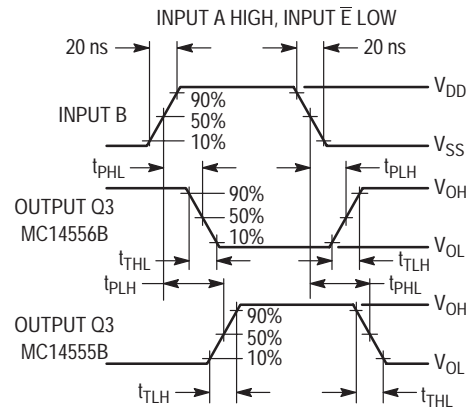
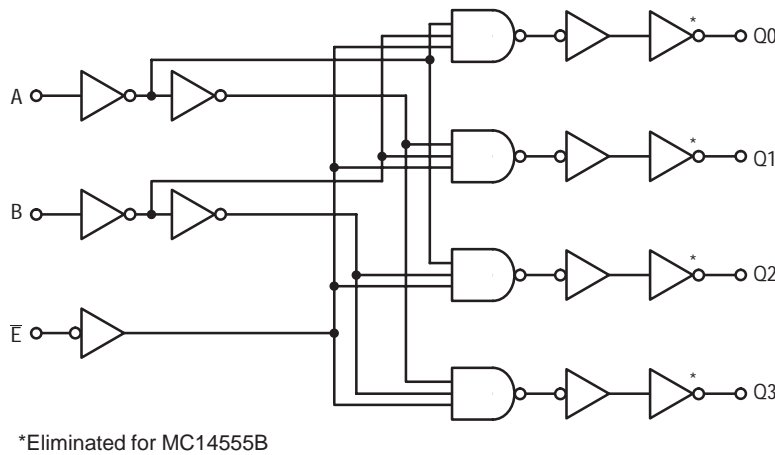


Figure 2. Dynamic Signal Waveforms

### LOGIC DIAGRAM (1/2 of Dual)



# MC14557B

## 1-to-64 Bit Variable Length Shift Register

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1–64 Bit Programmable Length
- Q and  $\bar{Q}$  Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or one Low–power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	–0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	–0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	–55 to +125	°C
$T_{stg}$	Storage Temperature Range	–65 to +150	°C
$T_L$	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

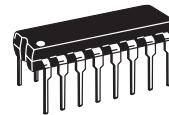
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



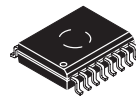
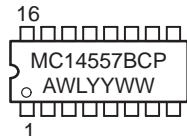
ON Semiconductor

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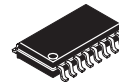
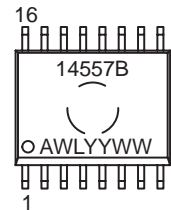
### MARKING DIAGRAMS



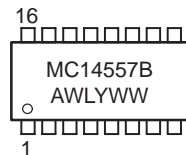
PDIP–16  
P SUFFIX  
CASE 648



SOIC–16  
DW SUFFIX  
CASE 751G



SOEIAJ–16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

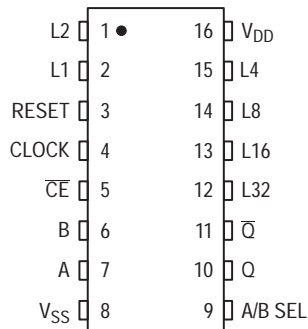
### ORDERING INFORMATION

Device	Package	Shipping
MC14557BCP	PDIP–16	2000/Box
MC14557BDW	SOIC–16	47/Rail
MC14557BDWR2	SOIC–16	1000/Tape & Reel
MC14557BF	SOEIAJ–16	See Note 1.
MC14557BFEL	SOEIAJ–16	See Note 1.

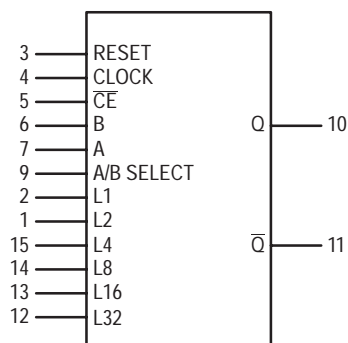
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14557B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

## TRUTH TABLE

Inputs				Output
Rst	A/B	Clock	CE	Q
0	0		0	B
0	1		0	A
0	0	1		B
0	1	1		A
1	X	X	X	0

Q is the output of the first selected shift register stage.

X = Don't Care

## LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1 Bit
0	0	0	0	0	1	2 Bits
0	0	0	0	1	0	3 Bits
0	0	0	0	1	1	4 Bits
0	0	0	1	0	0	5 Bits
0	0	0	1	0	1	6 Bits
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34 Bits
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	0	61 Bits
1	1	1	1	1	1	62 Bits
1	1	1	1	1	0	63 Bits
1	1	1	1	0	1	64 Bits

NOTE: Length equals the sum of the binary length control subscripts plus one.

# MC14557B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.75 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.50 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.25 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14557B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Rise and Fall Time, Q or $\bar{Q}$ Output $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay, Clock or $\bar{CE}$ to Q or $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5 10 15	— — —	300 130 90	600 260 180	ns
Propagation Delay, Reset to Q or $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 70 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5 10 15	— — —	300 130 95	600 260 190	ns
Pulse Width, Clock	$t_{WH(cl)}$	5 10 15	200 100 75	95 45 35	— — —	ns
Pulse Width, Reset	$t_{WH(rst)}$	5 10 15	300 140 100	150 70 50	— — —	ns
Clock Frequency (50% Duty Cycle)	$f_{cl}$	5 10 15	— — —	3.0 7.5 13.0	1.7 5.0 6.7	MHz
Setup Time, A or B to Clock or $\bar{CE}$ Worst case condition: $L1 = L2 = L4 = L8 = L16 = L32 = V_{SS}$ (Register Length = 1)  Best case condition: $L32 = V_{DD}$ , L1 through L16 = Don't Care (Any register length from 33 to 64)	$t_{su}$	5 10 15  5 10 15	700 290 145  400 165 60	350 130 85  45 5 0	— — —  — — —	ns
Hold Time, Clock or $\bar{CE}$ to A or B Best case condition: $L1 = L2 = L4 = L8 = L16 = L32 = V_{SS}$ (Register Length = 1)  Worst case condition: $L32 = V_{DD}$ , L1 through L16 = Don't Care (Any register length from 33 to 64)	$t_h$	5 10 15  5 10 15	200 100 10  400 185 85	- 150 - 60 - 50  50 25 22	— — —  — — —	ns
Rise and Fall Time, Clock	$t_r$ , $t_f$	5 10 15	No Limit			—
Rise and Fall Time, Reset or $\bar{CE}$	$t_r$ , $t_f$	5 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Removal Time, Reset to Clock or $\bar{CE}$	$t_{rem}$	5 10 15	160 80 70	80 40 35	— — —	ns

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.







# MC14562B

## 128-Bit Static Shift Register

The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Fully Static Operation
- Cascadable to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.

2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

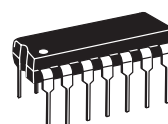
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



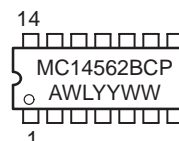
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### MARKING DIAGRAMS



PDIP-14  
P SUFFIX  
CASE 646



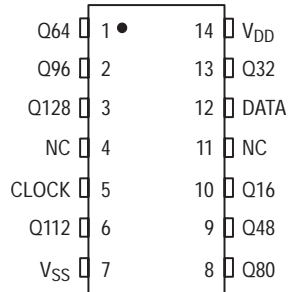
A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14562BCP	PDIP-14	25/Rail

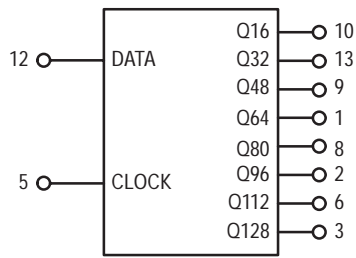
# MC14562B

## PIN ASSIGNMENT



NC = NO CONNECTION

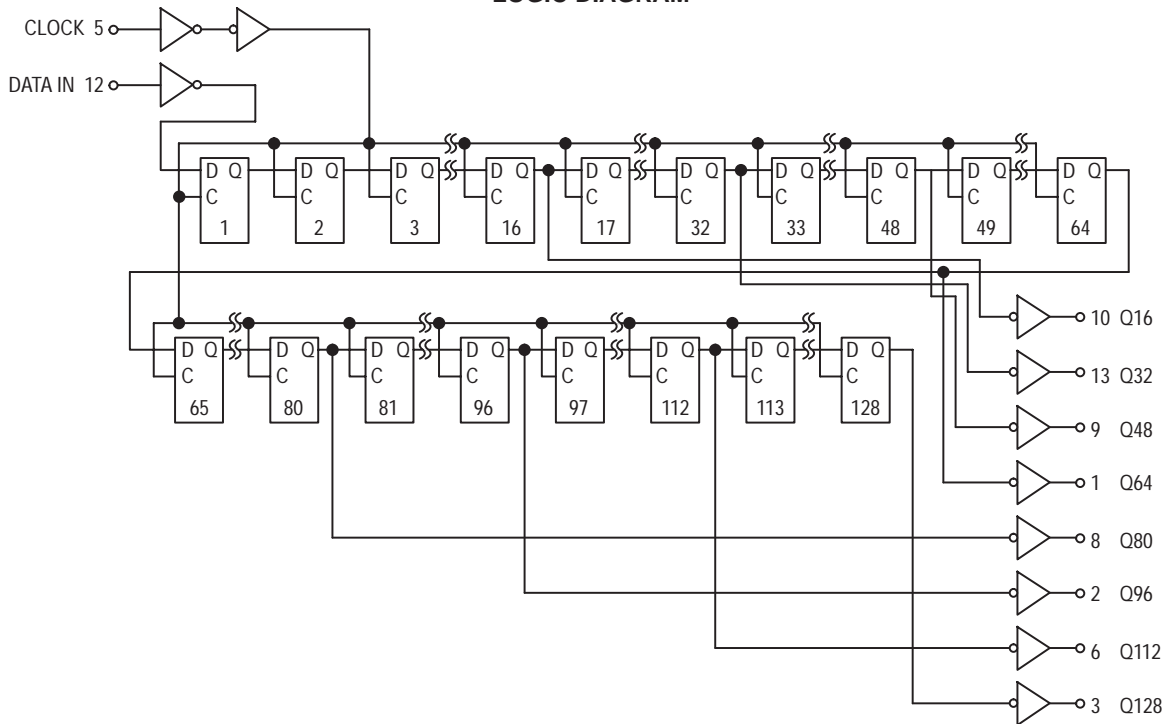
## BLOCK DIAGRAM



Pins 4 and 11  
not used.

V<sub>DD</sub> = PIN 14  
V<sub>SS</sub> = PIN 7

## LOGIC DIAGRAM



# MC14562B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 05 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.94 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.81 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.52 μA/kHz) f + I <sub>DD</sub>							μAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

# MC14562B

## SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ <sup>(7.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 515 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	600 250 170	1200 500 340	ns
Clock Pulse Width (50% Duty Cycle)	$t_{WH}$	5.0 10 15	600 220 150	300 110 75	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	1.9 5.6 8.0	1.1 3.0 4.0	MHz
Data to Clock Setup Time	$t_{su(1)}$	5.0 10 15	-20 -10 0	-170 -64 -60	— — —	ns
	$t_{su(0)}$	5.0 10 15	-20 -10 0	-91 -58 -48	— — —	ns
Data to Clock Hold Time	$t_{h(1)}$	5.0 10 15	350 165 155	263 109 100	— — —	ns
	$t_{h(0)}$	5.0 10 15	350 200 140	267 140 93	— — —	ns
Clock Input Rise and Fall Times	$t_r, t_f$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14562B

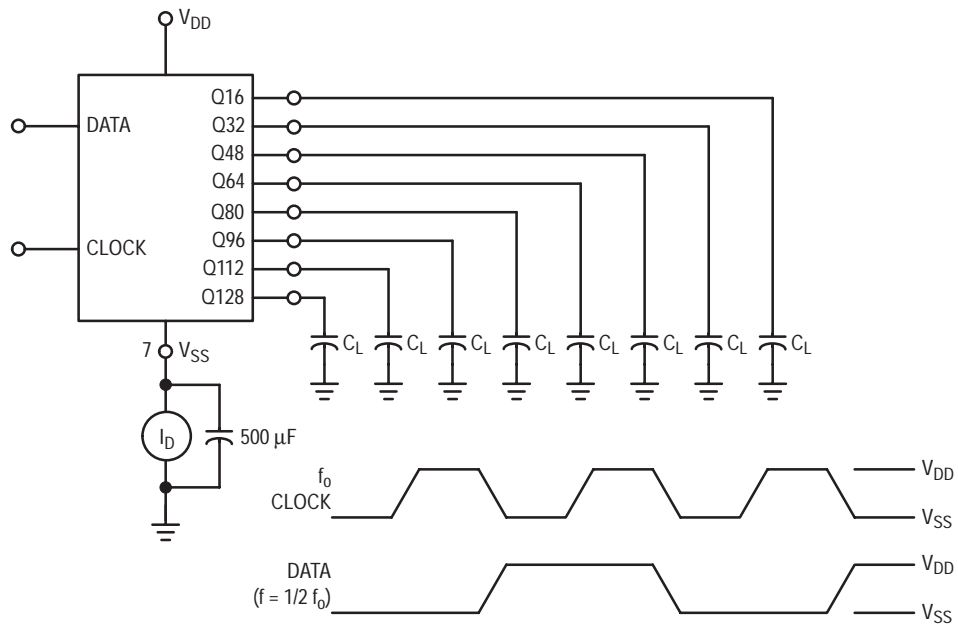
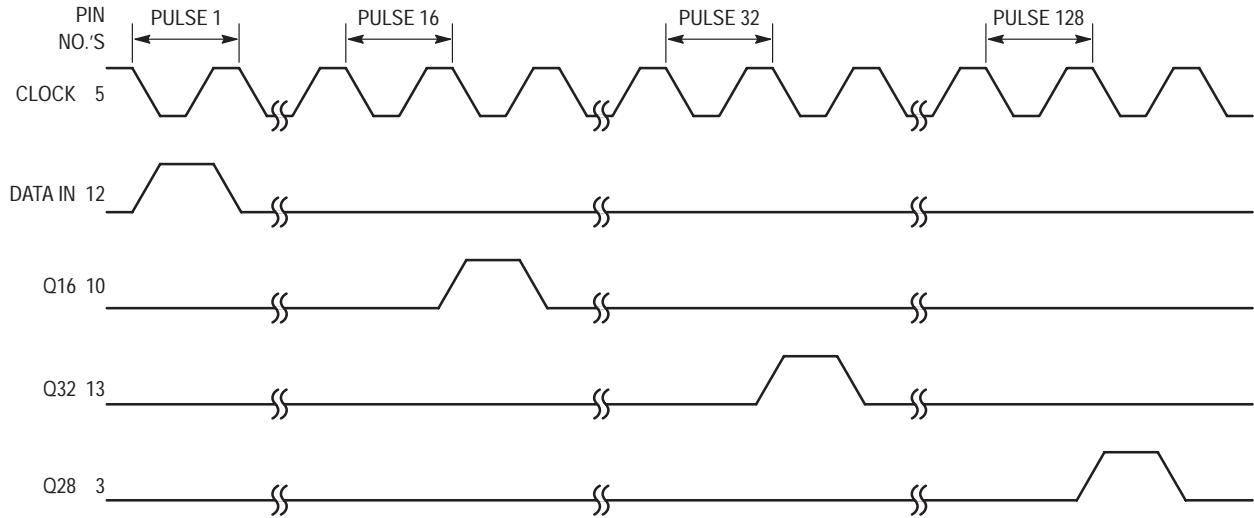


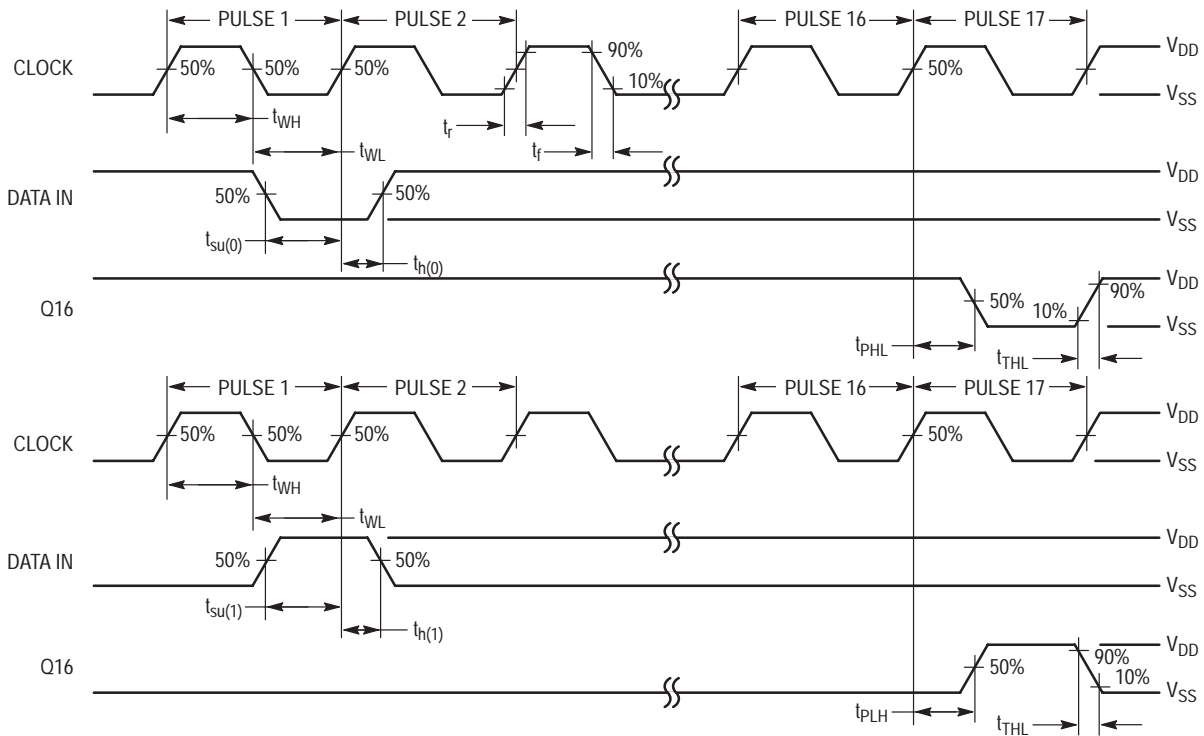
Figure 1. Power Dissipation Test Circuit and Waveforms

# MC14562B

## TIMING DIAGRAM



## AC TEST WAVEFORMS



NOTE: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

# MC14569B

## Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

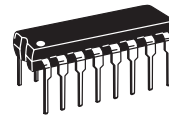
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



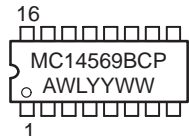
ON Semiconductor

<http://onsemi.com>

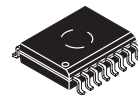
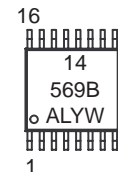
### MARKING DIAGRAMS



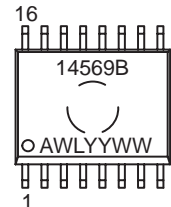
PDIP-16  
P SUFFIX  
CASE 648



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC-16  
DW SUFFIX  
CASE 751G



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

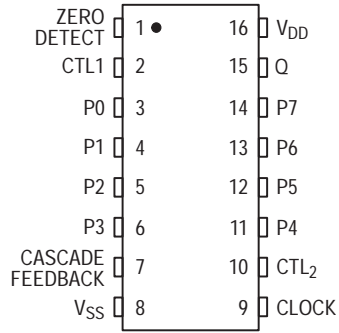
### ORDERING INFORMATION

Device	Package	Shipping
MC14569BCP	PDIP-16	2000/Box
MC14569BDT	TSSOP-16	96/Rail
MC14569BDW	SOIC-16	47/Rail
MC14569BDWR2	SOIC-16	1000/Tape & Reel

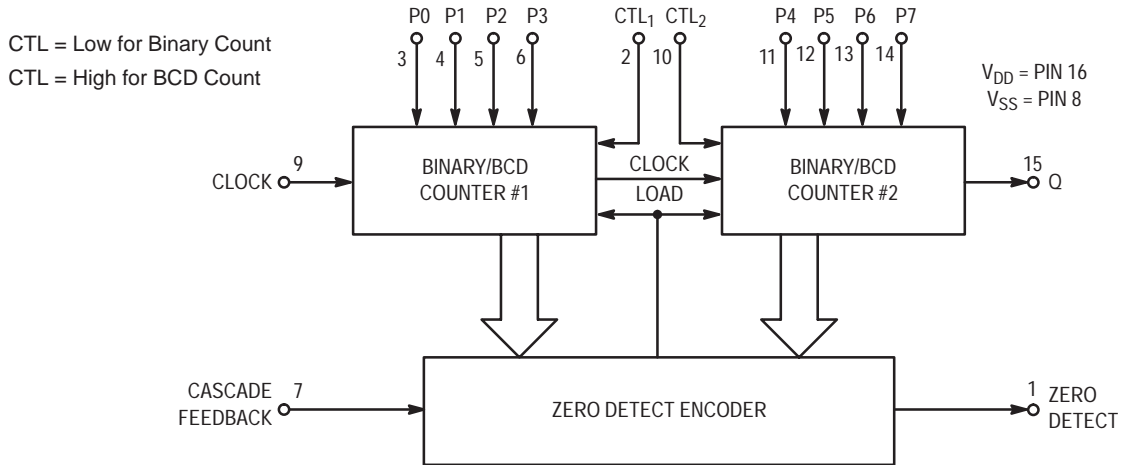


# MC14569B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



# MC14569B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (3.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current Source (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  Sink (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.58 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.20 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.95 μA/kHz) f + I <sub>DD</sub>							μAdc

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14569B

## SWITCHING CHARACTERISTICS\* ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit	
			Min	Typ (6.)	Max		
Output Rise Time	$t_{TLH}$	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Output Fall Time	$t_{THL}$	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Turn-On Delay Time Zero Detect Output  Q Output	$t_{PLH}$	5.0	—	420	700	ns	
		10	—	175	300		
		15	—	125	250		
	Q Output	$t_{PLH}$	5.0	—	675	1200	ns
			10	—	285	500	
			15	—	200	400	
Turn-Off Delay Time Zero Detect Output  Q Output	$t_{PHL}$	5.0	—	380	600	ns	
		10	—	150	300		
		15	—	100	200		
	Q Output	$t_{PHL}$	5.0	—	530	1000	ns
			10	—	225	400	
			15	—	155	300	
Clock Pulse Width	$t_{WH}$	5.0	300	100	—	ns	
		10	150	45	—		
		15	115	30	—		
Clock Pulse Frequency	$f_{cl}$	5.0	—	3.5	2.1	MHz	
		10	—	9.5	5.1		
		15	—	13.0	7.8		
Clock Pulse Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0	NO LIMIT			$\mu\text{s}$	
		10					
		15					

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14569B

## SWITCHING WAVEFORMS

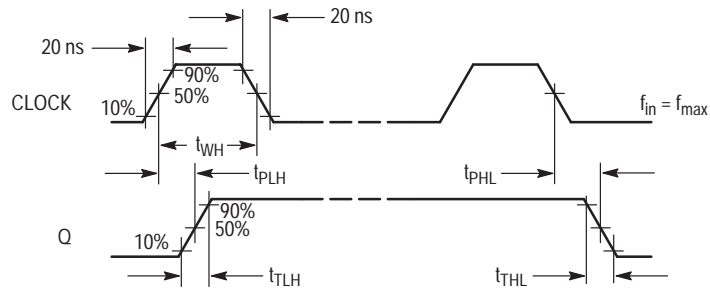


Figure 1.

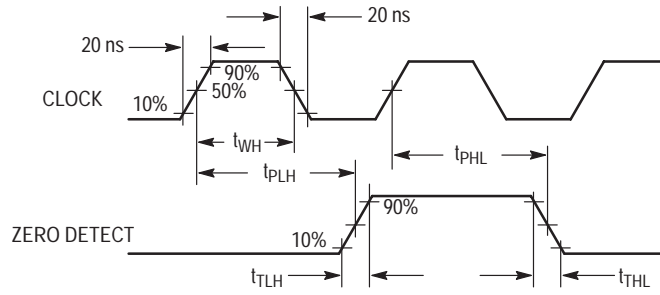


Figure 2.

# MC14569B

## PIN DESCRIPTIONS

### INPUTS

**P0, P1, P2, P3 (Pins 3, 4, 5, 6)** — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

**P4, P5, P6, P7 (Pins 11, 12, 13, 14)** — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

**Clock (Pin 9)** — Preset data is decremented by one on each positive transition of this signal.

### OUTPUTS

**Zero Detect (Pin 1)** — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q (Pin 15)** — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

### CONTROLS

**Cascade Feedback (Pin 7)** — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don’t cares.” Refer to Table 1 for output characteristics.

**CTL<sub>1</sub> (Pin 2)** — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

**CTL<sub>2</sub> (Pin 10)** — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

### SUPPLY PINS

**V<sub>SS</sub> (Pin 18)** — Negative Supply Voltage. This pin is usually connected to ground.

**V<sub>DD</sub> (Pin 16)** — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

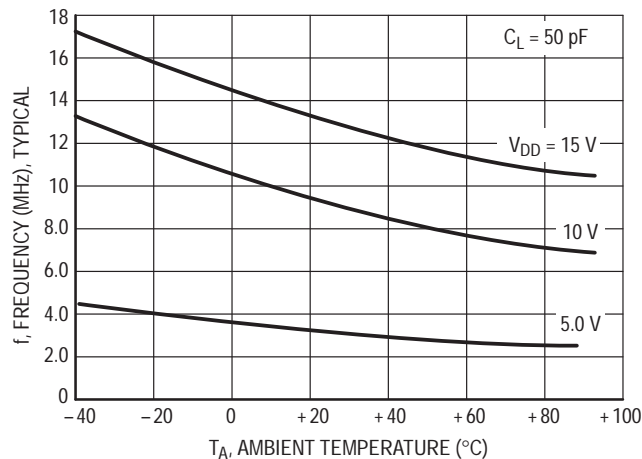
## OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V<sub>DD</sub>.





# MC14569B

**Table 3. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	1	1	0	0	1	19	X		
0	0	1	0	0	0	0	0	20	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	1	1	0	0	0	0	30	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	0	0	0	0	0	40	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	1	0	0	0	0	50	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	0	0	0	0	0	60	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	1	0	0	0	0	70	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓ Bit Value Counting Sequence	
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	0	0	0	0	90	90		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	1	1	1	0	0	0	0	150	150		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	1	1	1	1	0	0	1	159	159		
80	40	20	10	8	4	2	1				
Counter #2 Binary				Counter #1 BCD							

X = No Output (Always Low)

# MC14569B

**Table 4. Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2 <sup>7</sup> 128	2 <sup>6</sup> 64	2 <sup>5</sup> 32	2 <sup>4</sup> 16	2 <sup>3</sup> 8	2 <sup>2</sup> 4	2 <sup>1</sup> 2	2 <sup>0</sup> 1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)



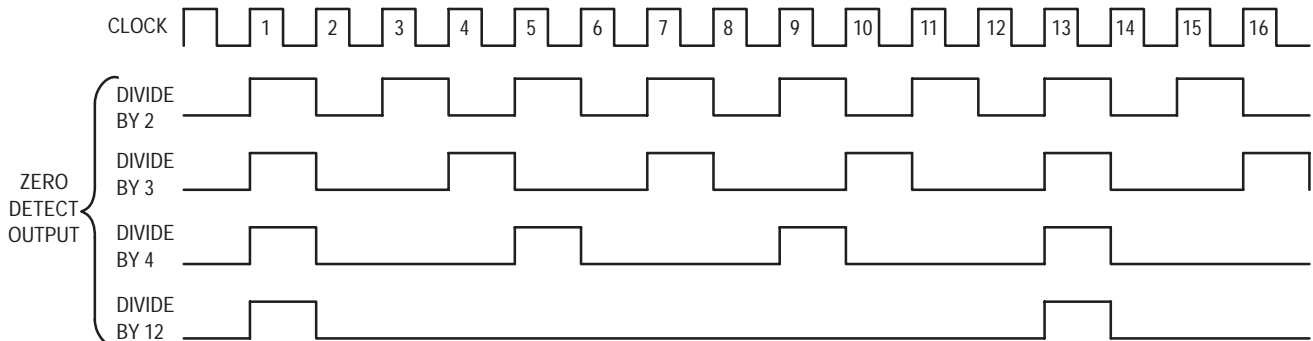
# MC14569B

**Table 5. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	100	100	Max Count illegal state Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	1	1	0	0	0	0	30	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	0	0	0	0	0	40	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	1	0	0	0	0	50	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	1	0	0	0	0	70	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓	
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	0	0	0	0	90	90		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	1	0	0	1	99	99		
80	40	20	10	8	4	2	1				Bit Value
Counter #2 BCD				Counter #1 BCD							Counting Sequence

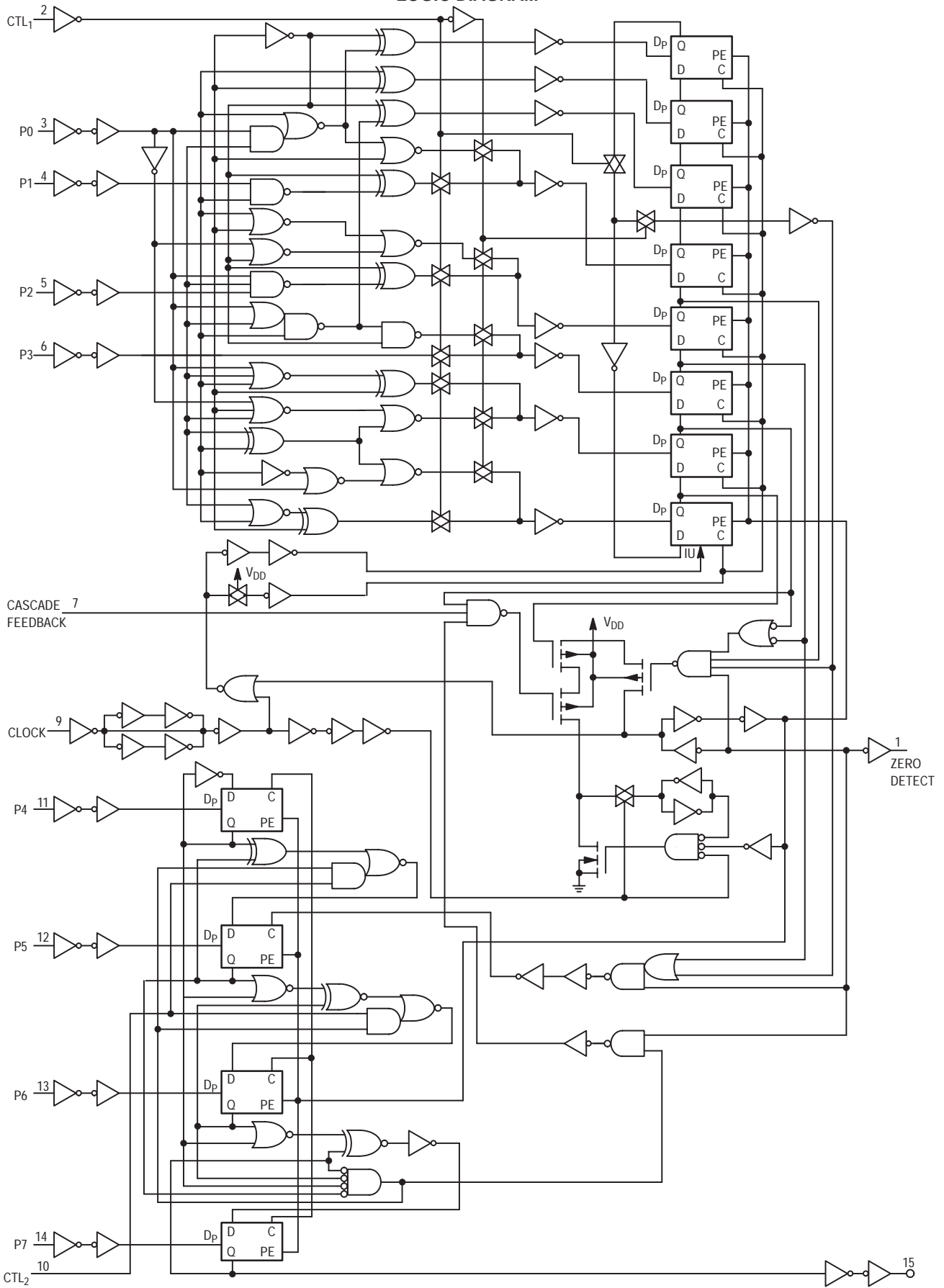
X = No Output (Always Low)

## TIMING DIAGRAM MC14569B



# MC14569B

## LOGIC DIAGRAM



# MC14569B

## TYPICAL APPLICATIONS

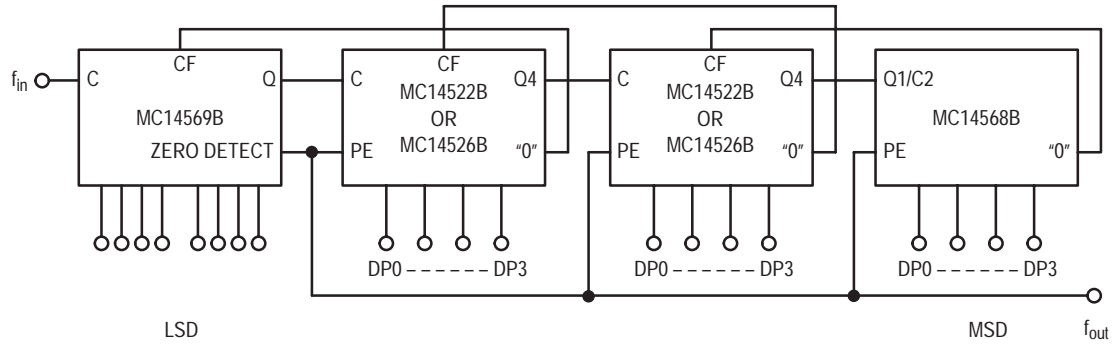
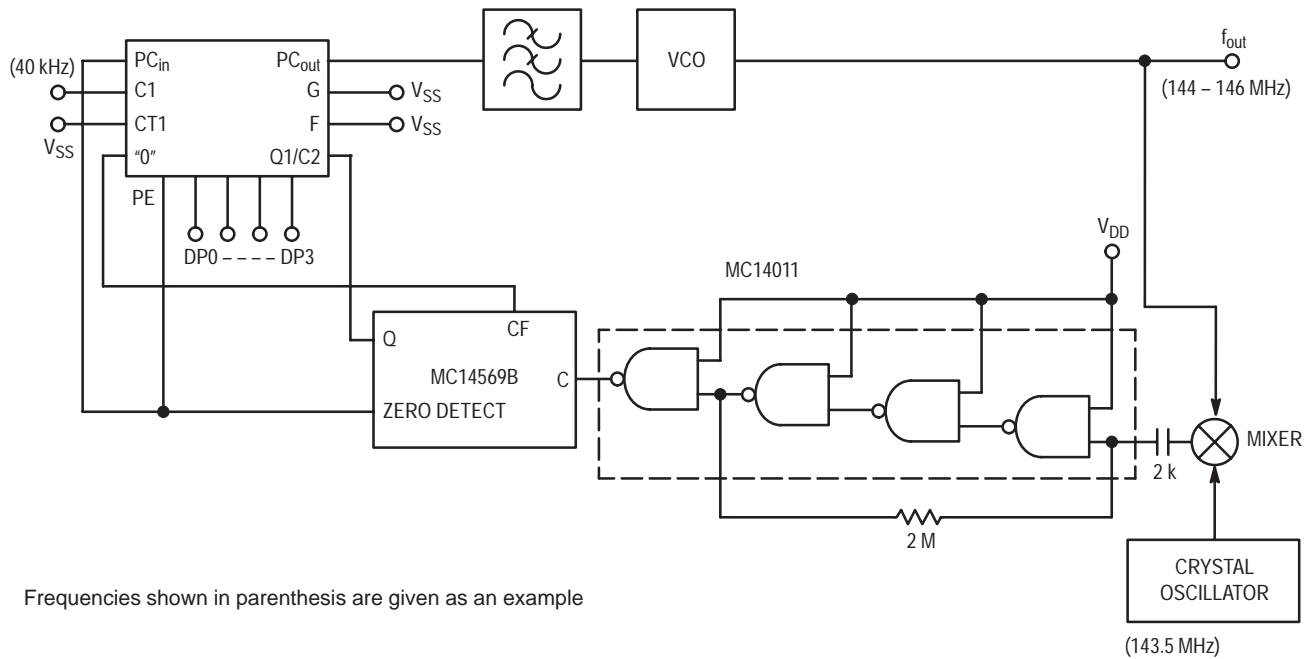


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B



Frequencies shown in parenthesis are given as an example

Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

# MC14572UB

## Hex Gate

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to  $V_{SS}$  Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to  $V_{DD}$  Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

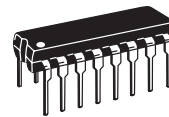
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



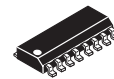
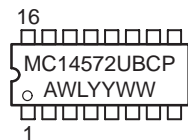
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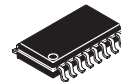
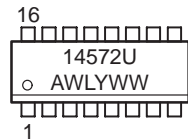


PDIP-16  
P SUFFIX  
CASE 648

### MARKING DIAGRAMS



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

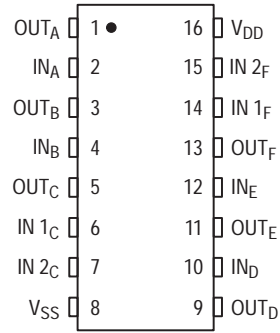
### ORDERING INFORMATION

Device	Package	Shipping
MC14572UBCP	PDIP-16	2000/Box
MC14572UBD	SOIC-16	48/Rail
MC14572UBDR2	SOIC-16	2500/Tape & Reel
MC14572UBF	SOEIAJ-16	See Note 1.
MC14572UBFEL	SOEIAJ-16	See Note 1.

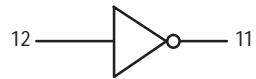
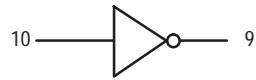
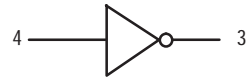
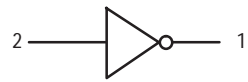
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14572UB

## PIN ASSIGNMENT

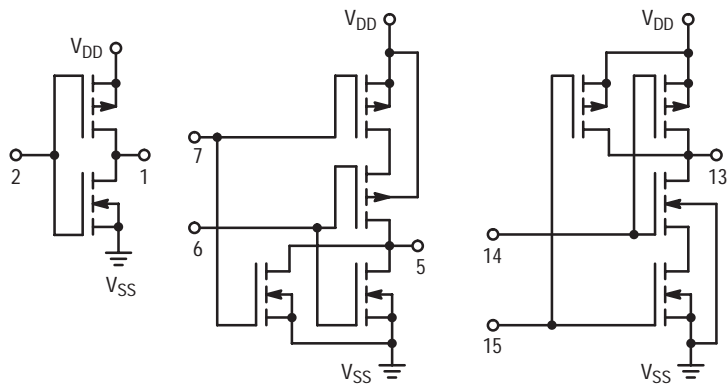


## LOGIC DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

## CIRCUIT SCHEMATIC



# MC14572UB

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
		10	—	2.0	—	4.50	2.0	—	2.0	
		15	—	2.5	—	6.75	2.5	—	2.5	
	"1" Level V <sub>IH</sub>	5.0	4.0	—	4.0	2.75	—	4.0	—	
		10	8.0	—	8.0	5.50	—	8.0	—	
		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.89 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.80 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.68 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.006.

# MC14572UB

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 17 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	90 50 40	180 100 80	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

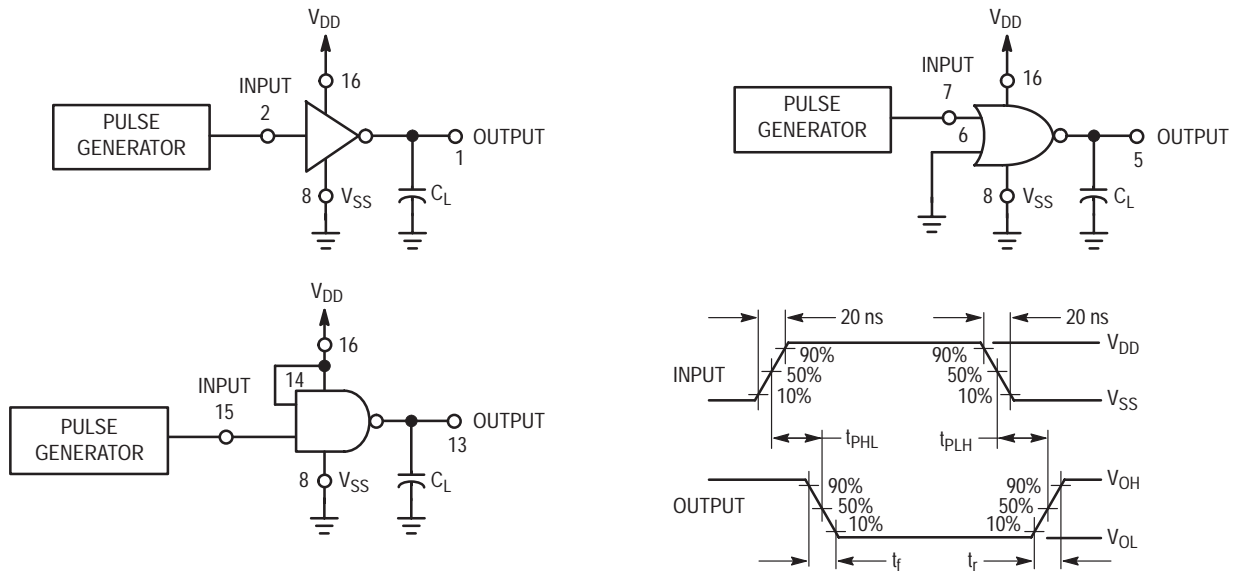


Figure 1. Switching Time Test Circuits and Waveforms

# MC14584B

## Hex Schmitt Trigger

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to “square up” slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic “P and D/DW” Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

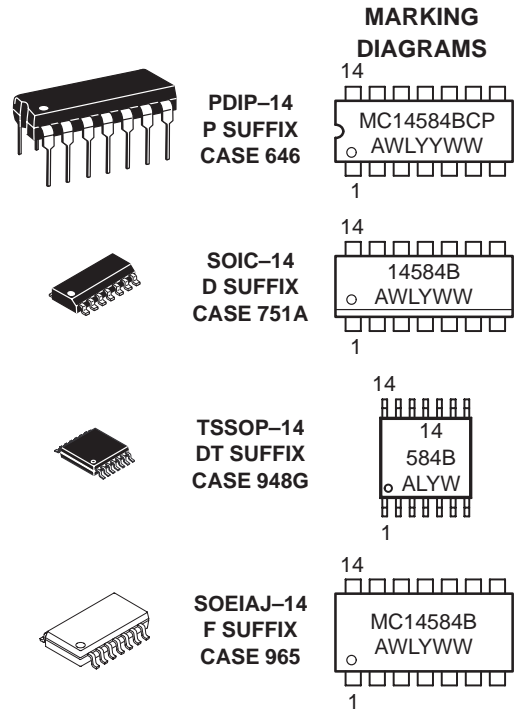
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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A = Assembly Location  
 WL or L = Wafer Lot  
 YY or Y = Year  
 WW or W = Work Week

### ORDERING INFORMATION

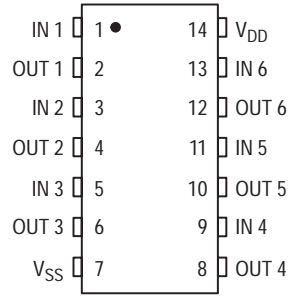
Device	Package	Shipping
MC14584BCP	PDIP-14	2000/Box
MC14584BD	SOIC-14	55/Rail
MC14584BDR2	SOIC-14	2500/Tape & Reel
MC14584BDT	TSSOP-14	96/Rail
MC14584BDTEL	TSSOP-14	2000/Tape & Reel
MC14584BF	SOEIAJ-14	See Note 1.
MC14584BFEL	SOEIAJ-14	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

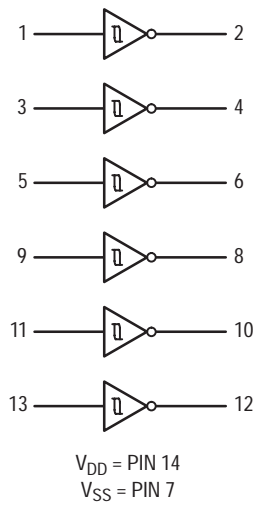


# MC14584B

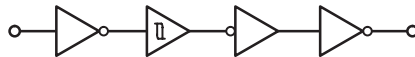
## PIN ASSIGNMENT



## LOGIC DIAGRAM



## EQUIVALENT CIRCUIT SCHEMATIC (1/6 OF CIRCUIT SHOWN)



# MC14584B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub>  V <sub>in</sub> = 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.5	—	0.0010	0.5	—	15	
		15	—	1.0	—	0.0015	1.0	—	30	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (3.6 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (5.4 μA/kHz) f + I <sub>DD</sub>							
Hysteresis Voltage	V <sub>H</sub> (7.)	5.0	0.27	1.0	0.25	0.6	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.3	0.7	1.2	0.25	1.2	
		15	0.77	1.7	0.6	1.1	1.5	0.50	1.4	
Threshold Voltage Positive-Going  Negative-Going	V <sub>T+</sub>	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
	V <sub>T-</sub>	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

7. V<sub>H</sub> = V<sub>T+</sub> - V<sub>T-</sub> (But maximum variation of V<sub>H</sub> is specified as less than V<sub>T+ max</sub> - V<sub>T- min</sub>).

# MC14584B

## SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (8.)	Max	Unit
Output Rise Time	$t_{TLH}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	$t_{THL}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	$t_{PLH}$ , $t_{PHL}$	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14584B

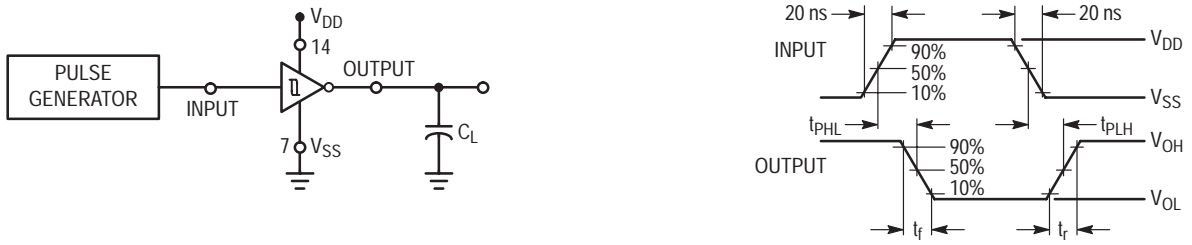
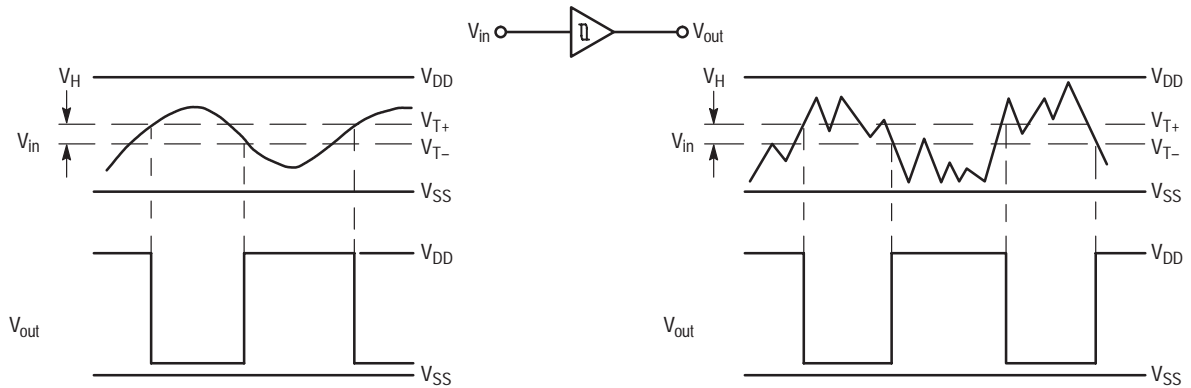


Figure 1. Switching Time Test Circuit and Waveforms



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 2. Typical Schmitt Trigger Applications

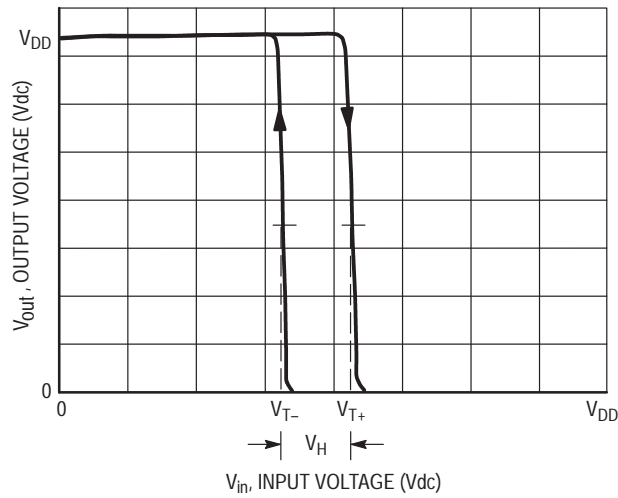


Figure 3. Typical Transfer Characteristics

# MC14585B

## 4-Bit Magnitude Comparator

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A < B, A = B, and A > B), and three outputs (A < B, A = B, and A > B). This device compares two 4-bit words (A and B) and determines whether they are “less than”, “equal to”, or “greater than” by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A > B), (A < B), and (A = B) to the corresponding inputs of the next significant comparator. Inputs (A < B), (A = B), and (A > B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU’s, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421–BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded – See Fig. 3

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>) (Note 2.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	–0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage Range (DC or Transient)	–0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient) per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 3.)	500	mW
T <sub>A</sub>	Ambient Temperature Range	–55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	–65 to +150	°C
T <sub>L</sub>	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

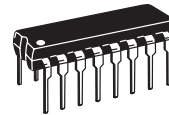
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.



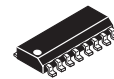
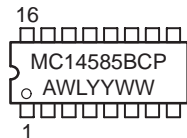
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<http://onsemi.com>

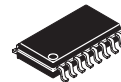
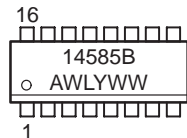


PDIP–16  
P SUFFIX  
CASE 648

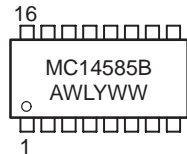
### MARKING DIAGRAMS



SOIC–16  
D SUFFIX  
CASE 751B



SOEIAJ–16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

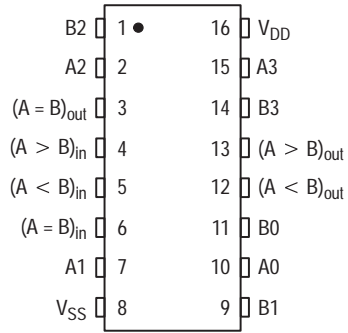
### ORDERING INFORMATION

Device	Package	Shipping
MC14585BCP	PDIP–16	2000/Box
MC14585BD	SOIC–16	48/Rail
MC14585BDR2	SOIC–16	2500/Tape & Reel
MC14585BF	SOEIAJ–16	See Note 1.

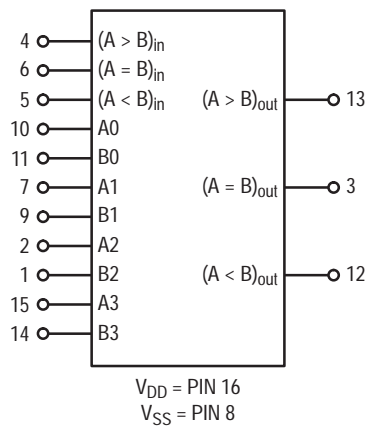
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14585B

## PIN ASSIGNMENT



## BLOCK DIAGRAM



## TRUTH TABLE (x = Don't Care)

Inputs							Outputs		
Comparing			Cascading						
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	x	x	x	x	x	x	0	0	1
A3 = B3	A2 > B2	x	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 > B1	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	x	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	x	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	x	1	1	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	x	x	x	1	0	0
A3 = B3	A2 = B2	A1 < B1	x	x	x	x	1	0	0
A3 = B3	A2 < B2	x	x	x	x	x	1	0	0
A3 < B3	x	x	x	x	x	x	1	0	0

# MC14585B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (4.)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	8.8	—	2.4	—	—		
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.2 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub>							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

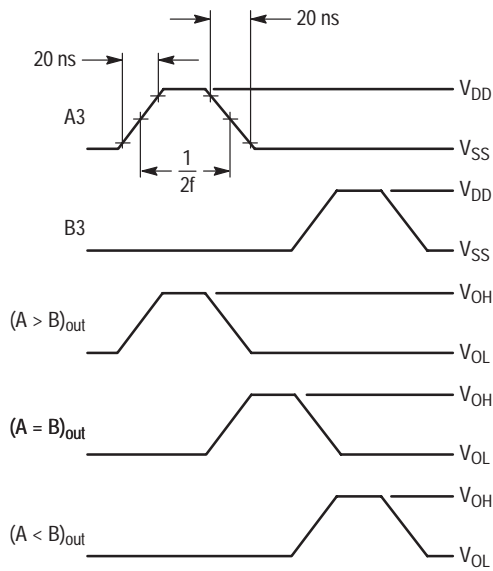
# MC14585B

## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-On, Turn-Off Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 345 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	430 180 130	860 360 260	ns

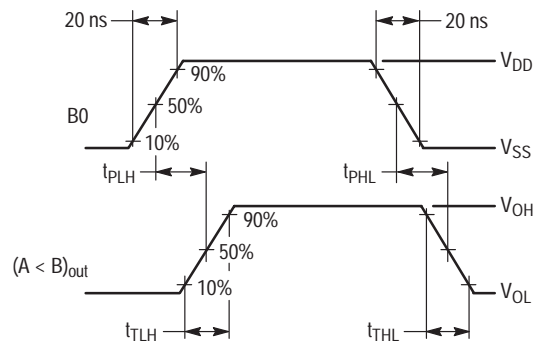
7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low.  
 f in respect to a system clock.

**Figure 1. Dynamic Power Dissipation Signal Waveforms**



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A<B) low.

**Figure 2. Dynamic Signal Waveforms**



# MC14585B

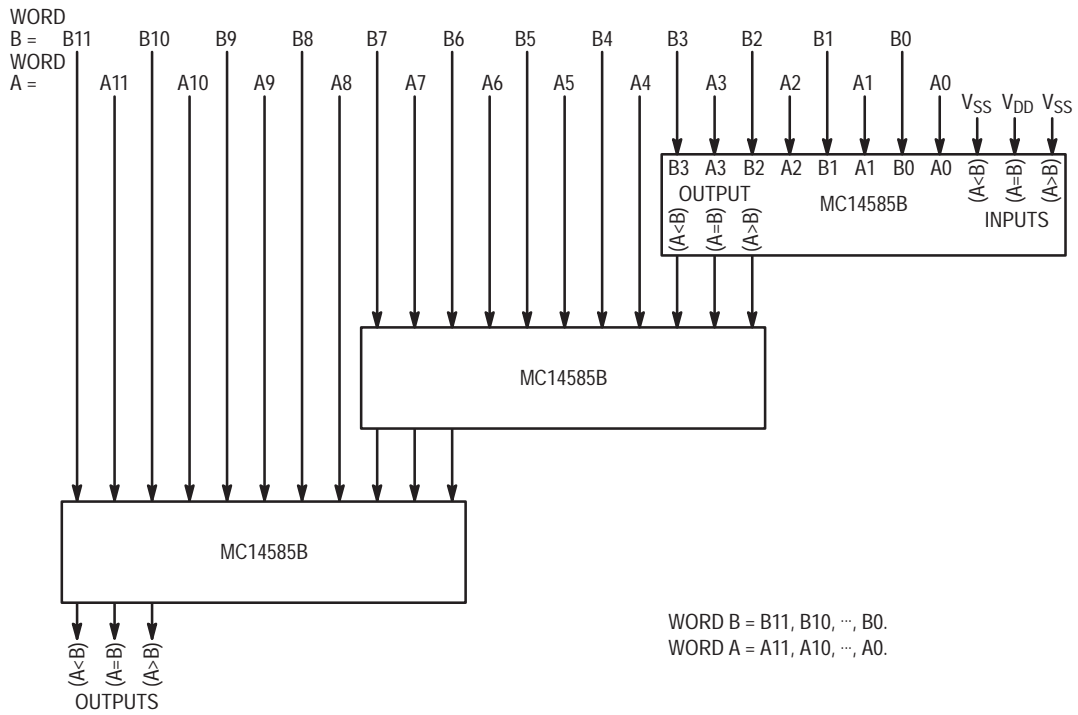
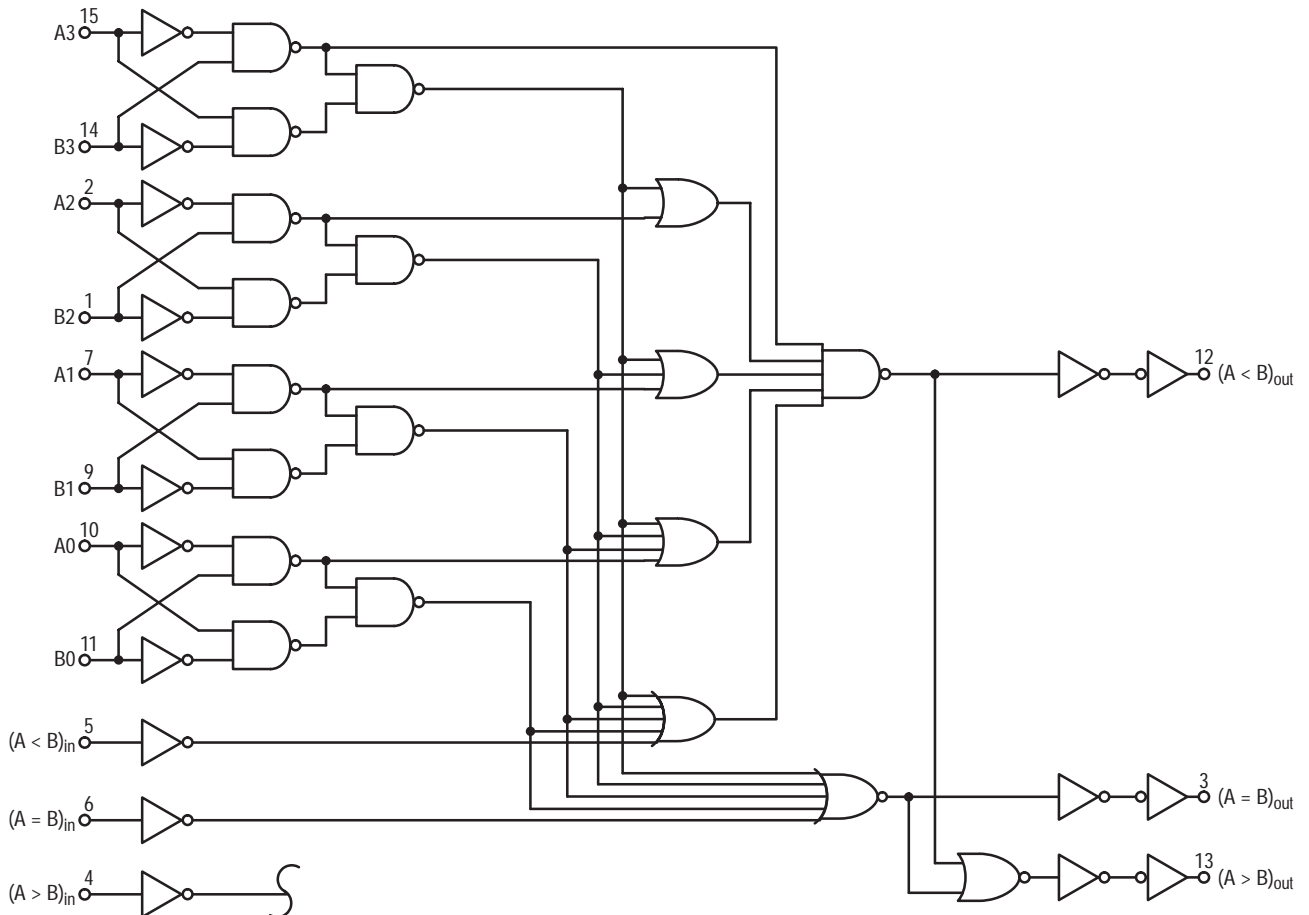


Figure 3. Cascading Comparators

## LOGIC DIAGRAM



# MC14598B

## 8-Bit Bus-Compatible Latches

The MC14598B is an 8-bit latch addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2.

All 8 outputs from the latches are available in parallel when  $\overline{\text{Enable}}$  is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin ( $\overline{\text{Enable}}$ ) TTL Compatible Input
- Open Drain  $\overline{\text{Full}}$  Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except  $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range

With Fanout as Follows:

- 1 TTL Load
- 4 LSTTL Loads

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

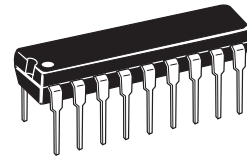
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range, Enable (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$V_{in}$	Input Voltage Range, All Other Inputs (DC or Transient)	-0.5 to $V_{DD} + 12$	V
$V_{out}$	Output Voltage Range, (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

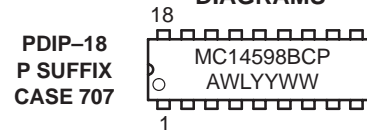


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### MARKING DIAGRAMS



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

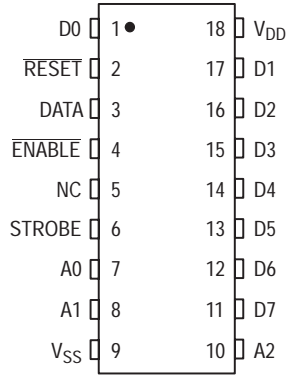
Device	Package	Shipping
MC14598BCP	PDIP-18	20/Rail

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

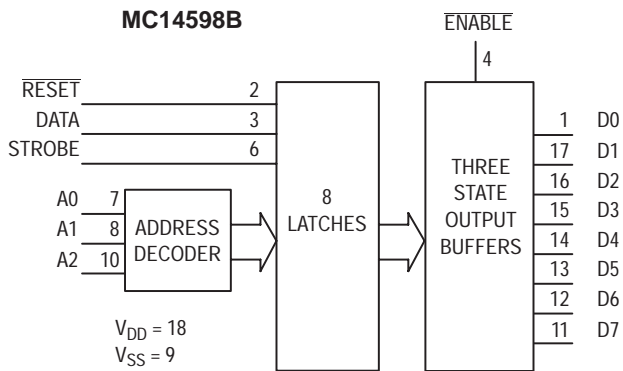
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

# MC14598B

## PIN ASSIGNMENT



## BLOCK DIAGRAMS



## OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedance
0	D <sub>n</sub>

D<sub>n</sub> = State of nth latch

NC = NO CONNECTION

# MC14598B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level  V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05		
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level  V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage <sup>(4.)</sup> — Enable "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	0.8	—	1.1	0.8	—	0.8	Vdc
		10	—	1.6	—	2.2	1.6	—	1.6	
15		—	2.4	—	3.4	2.4	—	2.4		
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level  V <sub>IH</sub>	5.0	2.0	—	2.0	1.9	—	2.0	—	Vdc
		10	6.0	—	6.0	3.1	—	6.0	—	
		15	10	—	10	4.3	—	10	—	
Input Voltage Other Inputs (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level  V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
15		—	4.0	—	6.75	4.0	—	4.0		
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level  V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (Full — Sink Only) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source  I <sub>OH</sub>	5.0	-1.0	—	-1.0	-2.0	—	-1.0	—	mAdc
		10	—	—	—	-6.0	—	—	—	
15		—	—	—	—	-12	—	—	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink  I <sub>OL</sub>	5.0	1.6	—	1.6	3.2	—	1.6	—	mAdc
		10	—	—	—	6.0	—	—	—	
		15	—	—	—	12	—	—	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Three-State Leakage Current	I <sub>TL</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current at an External Load Capacitance of 130 pF <sup>(4.)</sup>	I <sub>T</sub>	5.0 10	I <sub>T</sub> = (2.0 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (4.0 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (6.0 μA/kHz) f + I <sub>DD</sub>							μAdc

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

# MC14598B

## SWITCHING CHARACTERISTICS <sup>(5.)</sup> ( $T_A = 25^\circ\text{C}$ , $C_L = 130\text{ pF} + 1\text{ TTL Load}$ )

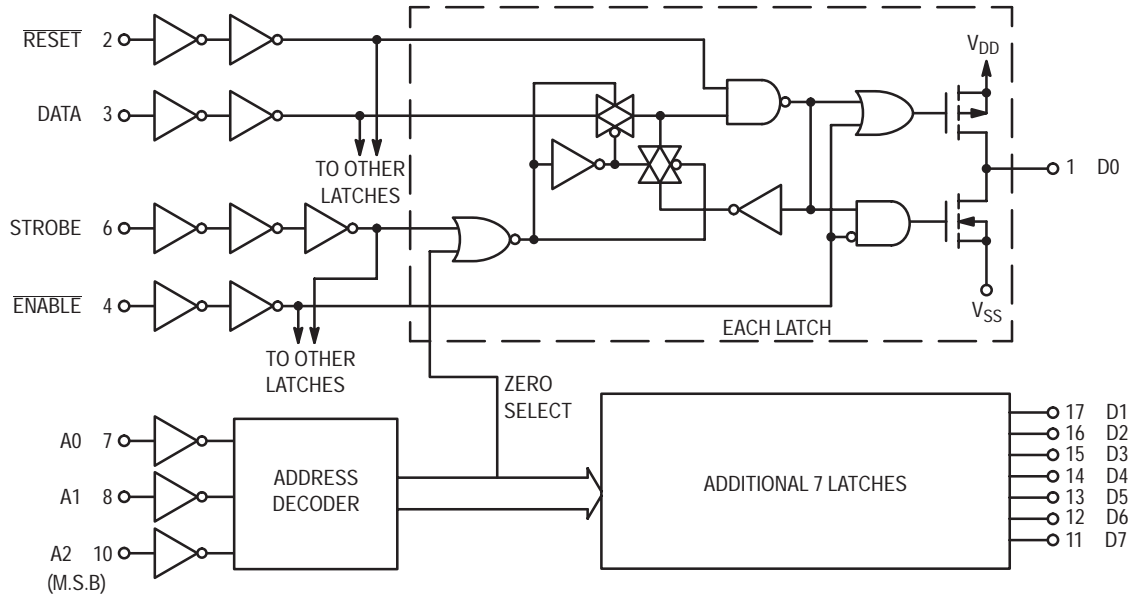
Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ <sup>(6.)</sup>	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (0.5\text{ ns/pF}) C_L + 35\text{ ns}$ $t_{TLH}, t_{THL} = (0.2\text{ ns/pF}) C_L + 25\text{ ns}$ $t_{TLH}, t_{THL} = (0.16\text{ ns/pF}) C_L + 20\text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time Enable to Output  Strobe to Output  $\overline{\text{Reset}}$ to Output	$t_{PLH},$ $t_{PHL}$	5.0	—	160	320	ns
		10	—	125	250	
		15	—	100	200	
		5.0	—	200	400	
		10	—	100	200	
		15	—	80	160	
		5.0	—	175	350	
		10	—	90	180	
		15	—	70	140	
Pulse Width Enable  Strobe  Increment  $\overline{\text{Reset}}$	$t_{WH},$ $t_{WL}$	5.0	320	160	—	ns
		10	240	120	—	
		15	160	80	—	
		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
		5.0	300	150	—	
		10	160	80	—	
		15	100	50	—	
Setup Time Data  Address	$t_{su}$	5.0	100	50	—	ns
		10	50	25	—	
		15	35	20	—	
		5.0	200	100	—	
		10	100	50	—	
		15	70	35	—	
Hold Time Data  Address	$t_h$	5.0	100	50	—	ns
		10	50	25	—	
		15	35	20	—	
		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Reset Removal Time	$t_{rem}$	5.0	20	– 25	—	ns
		10	20	– 15	—	
		15	20	– 10	—	

5. The formulas given are for the typical characteristics only at 25°C.

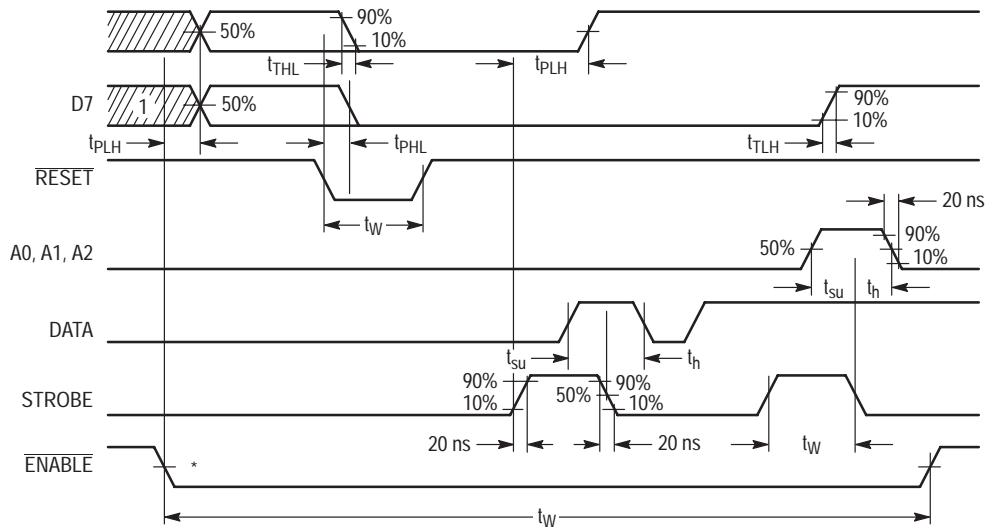
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14598B

## MC14598B FUNCTION DIAGRAM



## MC14598B TIMING DIAGRAM



\*1.4 V with V<sub>DD</sub> = 5.0 V

### NOTES:

1. High-impedance output state (another device controls bus).
2. Output Load as for MC14597B.

# MC14598B



**LATCH TRUTH TABLE**

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

\*= No change in state of latch

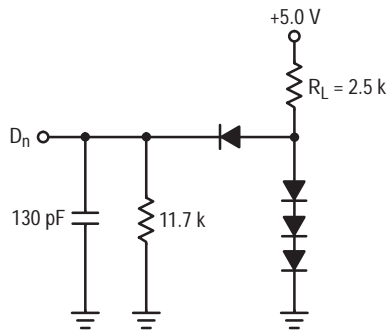
X = Don't care

**TRUTH TABLE FOR MC14597B**

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
	X	1	Count Up	—
	X	1	No Change	—
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

**TEST LOAD  
ALL OUTPUTS**



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# CHAPTER 7

## CMOS Reliability

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## RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of ON Semiconductor's reliability efforts.

### BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, useful life, and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality is reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. The useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.

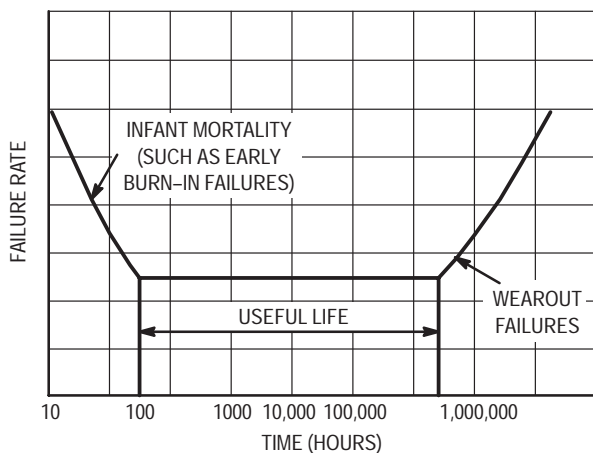


Figure 1.

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_0 = e^{-\lambda t}$$

where  $\lambda$  is the failure rate and  $t$  is time. Since  $\lambda$  is changing rapidly during infant mortality, the expression does not become useful until the random period, where  $\lambda$  is relatively constant. In this equation  $\lambda$  is failures per unit of time. It is

usually expressed in percent failures per thousand hours. Other forms include FIT (Failures in Time =  $(\%/10^3 \text{ hrs}) \times 10^{-4} = 10^{-9}$  failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to  $1/\lambda$  and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and  $\lambda$  is calculated using  $\chi^2$  distribution through the equation:

$$\lambda \leq \frac{\chi^2(x, 2r + 2)}{2nt}$$

$$\text{where } x = \frac{100 - \text{CL}}{100}$$

CL = Confidence Limit in percent

r = Number of rejects

n = Number of devices

t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher  $\lambda$  which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term  $(2r + 2)$  is called the degrees of freedom and is an expression of the number of rejects in a form suitable to  $\chi^2$  tables.

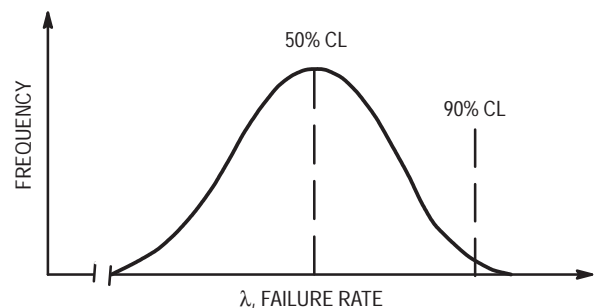


Figure 2.

The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While ON Semiconductor uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population, as sample size and test time are decreased, the  $\chi^2$  calculation produces surprisingly high values of  $\lambda$  for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\theta/kT}$$

where  $R(t)$  = Reaction rate as a function of time and temperature

$R_0$  = A constant

$t$  = Time

$\theta$  = Activation energy in electron volts

$k$  = Boltzman's constant

$T$  = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_0 e^{\theta/kT}$$

where  $t$  = time

$t_0$  = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted in log-linear paper with a slope expressed by  $\Theta$ .  $\Theta$  may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does not imply a high  $\Theta$ . Studies by Bell Telephone Laboratories have indicated that an overall  $\Theta$  for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in. Data taken by ON Semiconductor on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the

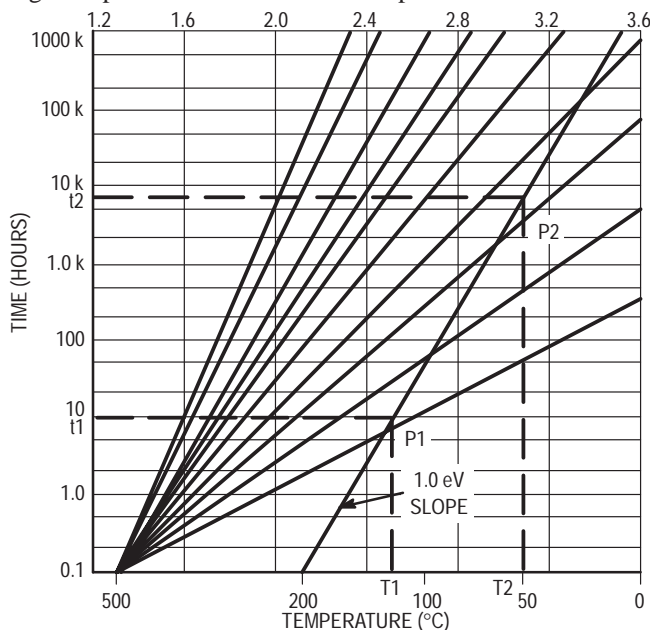


Figure 3. Normalized Time-Temperature Regressions for Various Activation Energy Values

devices will be used (Figure 3). For Discrete products, 0.7 eV is generally applied.

To accomplish this, the time in device hours ( $t_1$ ) and temperature ( $T_1$ ) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest ( $T_2$ ) and a line with a 1.0 eV slope is drawn through point P1.

Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours ( $t_2$ ). This number may then be used with the  $x^2$  formula to determine the failure rate at the temperature of interest. Assuming  $T_1$  of 125°C at  $t_1$  of 10,000 hours, a  $t_2$  of 7.8 million hours results at a  $T_2$  of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 0.1%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.0008%/1,000 hour failure rate, as illustrated in Figure 4.

Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted  $\lambda$ . A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only few significant wearout mechanisms: electromigration of circuit metallization, electrolytic corrosion in plastic devices and metal fatigue for Power devices.

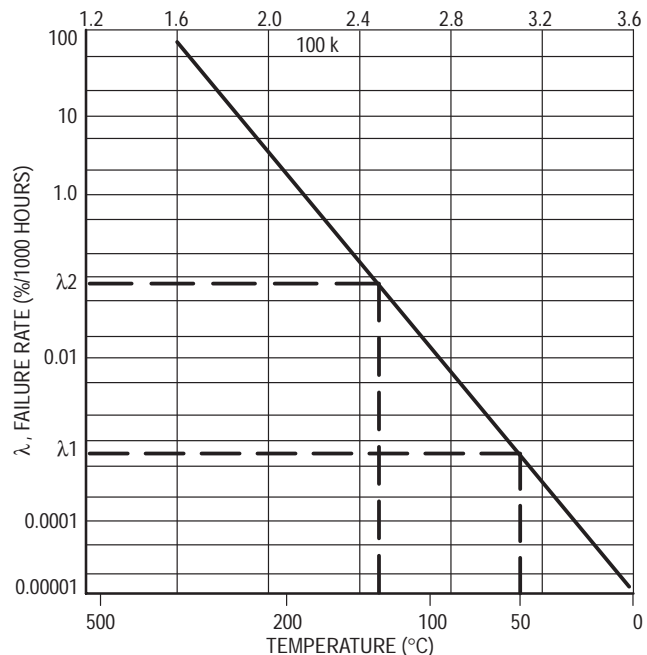


Figure 4. Failure Rate

For increased flexibility in working with a broad range of device hours, the time–temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

### THERMAL MANAGEMENT

Circuit performance and long–term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system’s ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or 
$$T_J = T_A + P_D(\bar{\theta}_{JA}) \quad (2)$$

where

- $T_J$  = maximum junction temperature
- $T_A$  = maximum ambient temperature
- $P_D$  = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$  = average thermal resistance, junction to case

$\bar{\theta}_{CA}$  = average thermal resistance, case to ambient

$\bar{\theta}_{JA}$  = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC or DESC for calculating a “practical” maximum operating junction temperature for MIL–M–38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case–to–ambient thermal resistance,  $\bar{\theta}_{CA}$ . (To some extent the device power dissipation can also be controlled, but under recommended use the  $V_{CC}$  supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the  $\bar{\theta}_{CA}$  thermal resistance term.  $\bar{\theta}_{JC}$  is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Thermal Resistance in Still Air								
Package Description								
No. Leads	Body Style	Body Material	Body W x L	Die Bonds	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	$\theta_{JC}$ (°C/Watt)	
							Avg.	Max.
14	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	6,400	38	61
16	DIL	Epoxy	1/4" x 3/4"	Epoxy	4096	12,100	34	54

**NOTES:**

1. All plastic packages use copper lead frames.
2. Body style DIL is “Dual–In–Line.”
3. Standard Mounting Method: Dual–In–Line Socket or P/C board with no contact between bottom of package and socket or P/C board.

**Figure 5. Thermal Resistance Values for Standard I/C Packages**

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature–controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\bar{\theta}_{JC}) \quad (3)$$

where  $T_C$  = maximum case temperature and the other parameters are as previously defined.

The maximum and average  $\bar{\theta}_{JC}$  resistance values for standard IC packages are given in Figure 5.

### AIR FLOW

The majority of users employ some form of air–flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Figure 6 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfm.

These figures show the proportionate increase in the junction temperature of each dual in–line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfm along the Z axis.

**Figure 6. Thermal Gradient of Junction Temperature (16–Pin Dual–in–Line Package)**

## OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

### Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$\text{Eq. (1) } T = (6.376 \times 10^9) e^{\left[ \frac{11554.267}{273.15 + T_J} \right]}$$

Where:  $T$  = Time in hours to 0.1% bond failure  
(1 failure per 1,000 bonds).

$T_J$  = Device junction temperature, °C.

And:

$$\text{Eq. (2) } T_J = T_A + P_D \theta_{JA} = T_A + \Delta T_J$$

Where:  $T_J$  = Device junction temperature, °C.

$T_A$  = Ambient temperature, °C.

$P_D$  = Device power dissipation in watts.

$\theta_{JA}$  = Device thermal resistance, junction to air,  
°C/Watt.

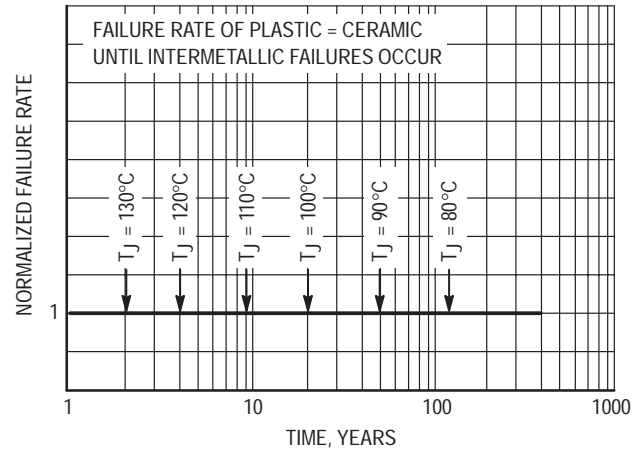
$\Delta T_J$  = Increase in junction temperature due to  
on-chip power dissipation.

Table 1 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

**Table 1. Device Junction Temperature versus Time to 0.1% Bond Failures**

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 1 is graphically illustrated in Figure 7 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.



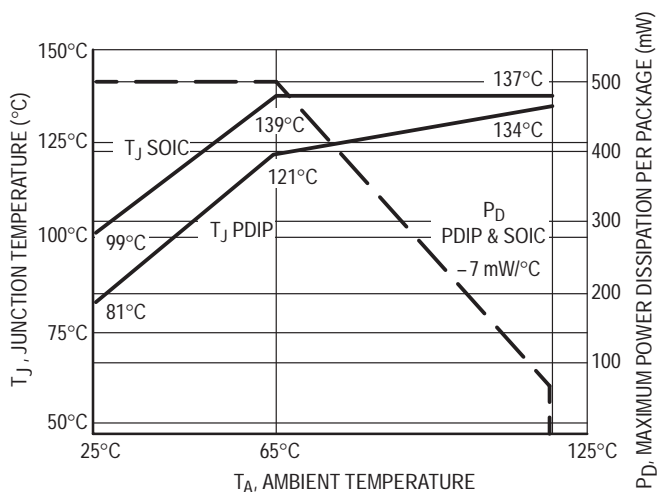
**Figure 7. Failure Rate versus Time Junction Temperature**

### Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 1 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 7.

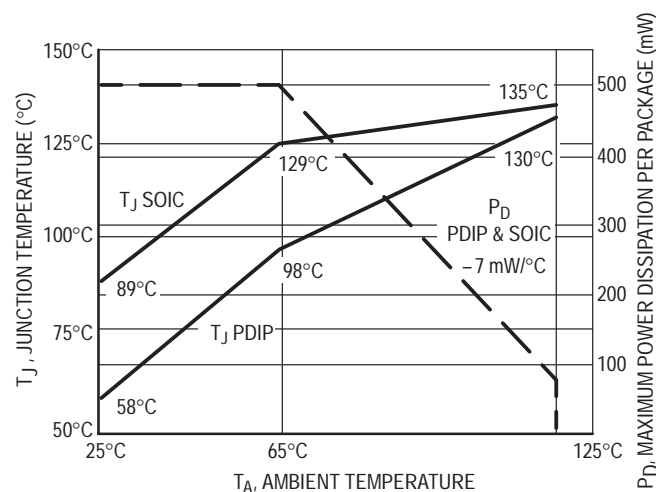
Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since  $\bar{\theta}_{CA}$  is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.



**Figure 8. Junction Temperature for Worst Case CMOS Logic Device**

This graph illustrates junction temperature for the worst case CMOS Logic device (MC14007UB) — smallest die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature,  $T_J$ , in a Dual-In-Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature,  $T_A$ . The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25 $^{\circ}\text{C}$  to 125 $^{\circ}\text{C}$ .



**Figure 9. Junction Temperature for Typical CMOS Logic Device**

This graph illustrates junction temperature for a CMOS Logic device (MC14053B) — average die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature,  $T_J$ , in a Dual-In-Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature,  $T_A$ . The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25 $^{\circ}\text{C}$  to 125 $^{\circ}\text{C}$ .

## **CHAPTER 8**

### **Equivalent Gate Count**

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# EQUIVALENT GATE COUNT

The following is a list of equivalent gate counts for some of ON Semiconductor's CMOS devices. In general for CMOS, the number of equivalent gates is equal to the total number of transistors on chip divided by four. This list includes only those devices with equivalent gate counts known at the time of this printing.

DEVICE	EQUIVALENT GATE COUNT	DEVICE	EQUIVALENT GATE COUNT
MC14001B	8	MC14081B	10
MC14001UB	4	MC14082B	8
MC14007UB	1.5	MC14093B	18
MC14008B	40	MC14094B	79
MC14011B	8	MC14099B	70
MC14011UB	4	MC14174B	43.5
MC14012B	7	MC14175B	39.5
MC14013B	16	MC14490	136.5
MC14014B	74	MC14503B	17
MC14015B	53	MC14504B	37.5
MC14016B	8	MC14511B	54
MC14017B	62.5	MC14512B	17.25
MC14018B	38.25	MC14514B	59
MC14020B	84	MC14515B	67
MC14021B	74	MC14516B	61
MC14023B	9	MC14517B	119
MC14024B	59	MC14518B	43.5
MC14025B	9	MC14520B	43.5
MC14028B	26	MC14526B	86
MC14029B	65.5	MC14528B	24
MC14040B	73	MC14532B	38.5
MC14042B	17.5	MC14536B	103
MC14046B	35	MC14538B	38
MC14049UB	3	MC14541B	93
MC14049B	9	MC14543B	52
MC14050B	6	MC14549B	122
MC14051B	48.5	MC14551B	35
MC14052B	38.5	MC14553B	147.5
MC14053B	38	MC14555B	21
MC14060B	73.5	MC14556B	25
MC14066B	13	MC14557B	232.5
MC14067B	65	MC14559B	122
MC14069UB	3	MC14562B	206
MC14071B	10	MC14569B	156
MC14073B	10.5	MC14572UB	4
MC14076B	32.5	MC14584B	18

# CHAPTER 9

## Packaging Information Including Surface Mounts

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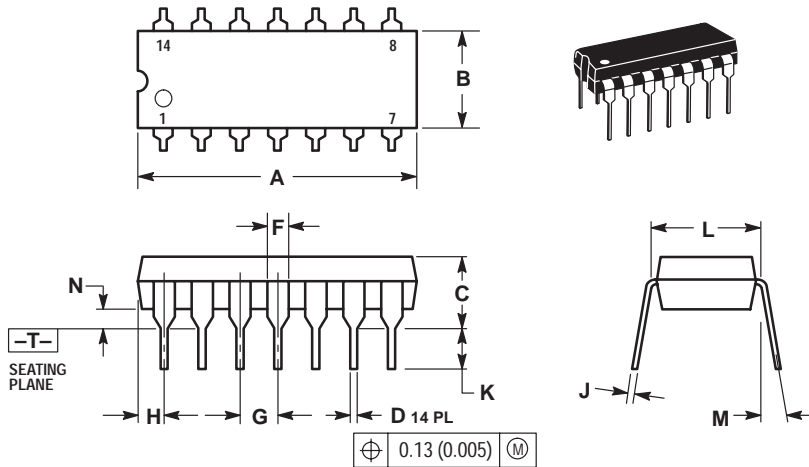


# PACKAGE DIMENSIONS

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "DT" (TSSOP). For example, to order a quad NOR gate, use MC14001BD.

## 14-Pin Packages

**PDIP-14  
P SUFFIX  
PLASTIC PACKAGE  
CASE 646-06  
ISSUE M**

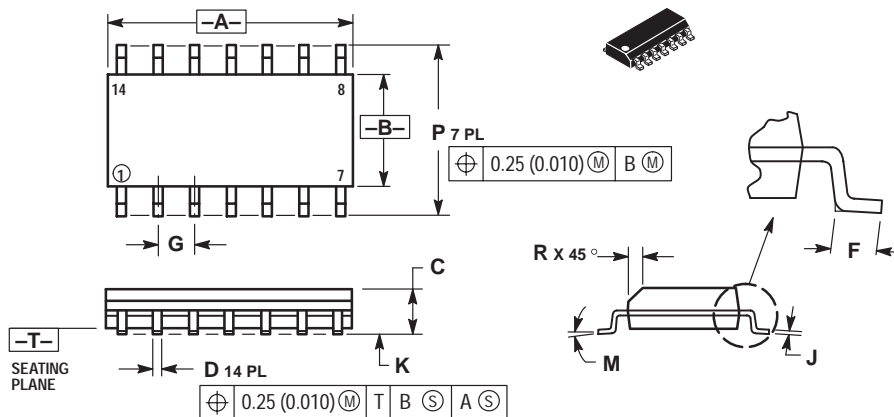


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

**SOIC-14  
D SUFFIX  
PLASTIC PACKAGE  
CASE 751A-03  
ISSUE F**



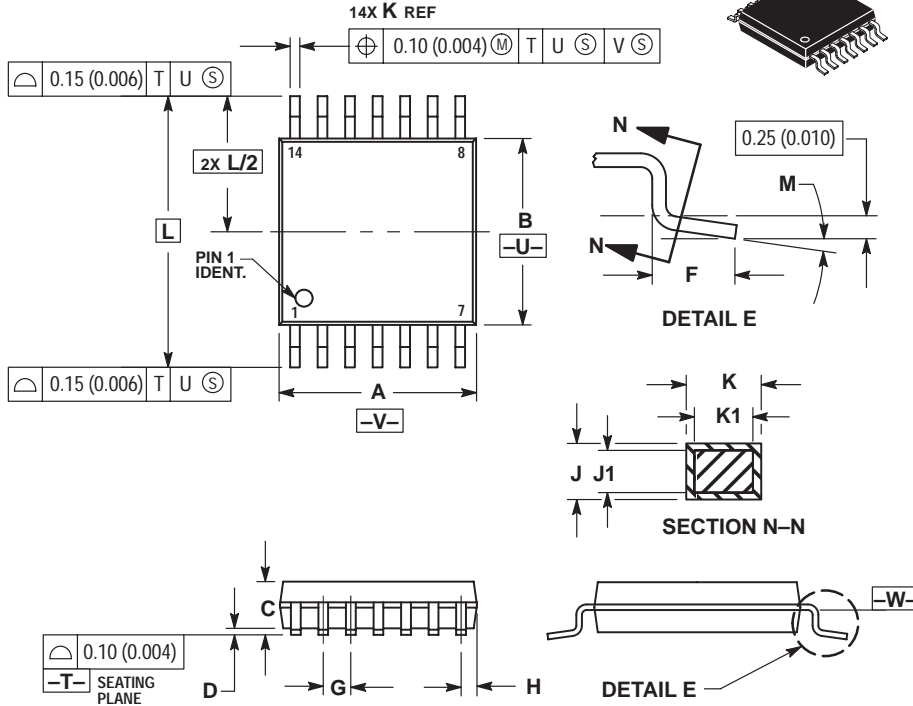
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

# 14-Pin Packages (continued)

## TSSOP-14 DT SUFFIX PLASTIC PACKAGE CASE 948G-01 ISSUE O

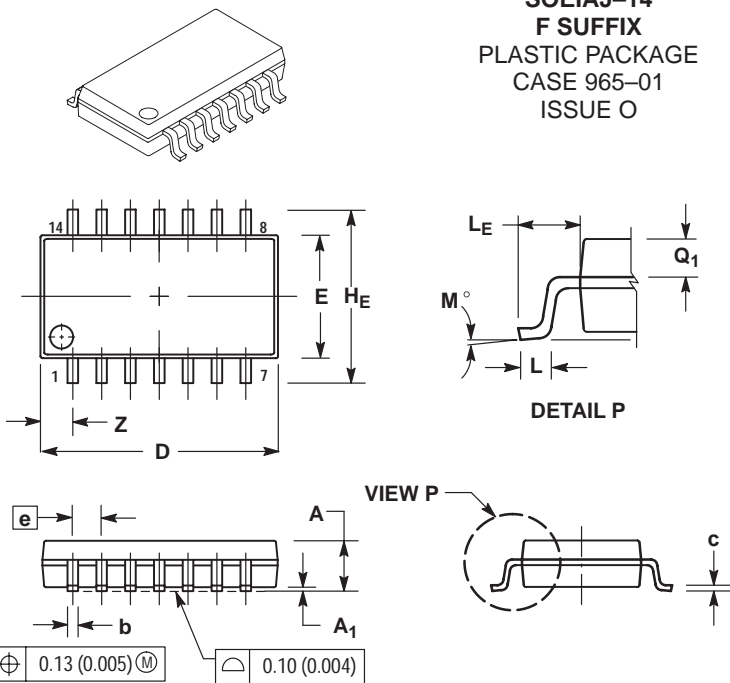


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## SOEIAJ-14 F SUFFIX PLASTIC PACKAGE CASE 965-01 ISSUE O



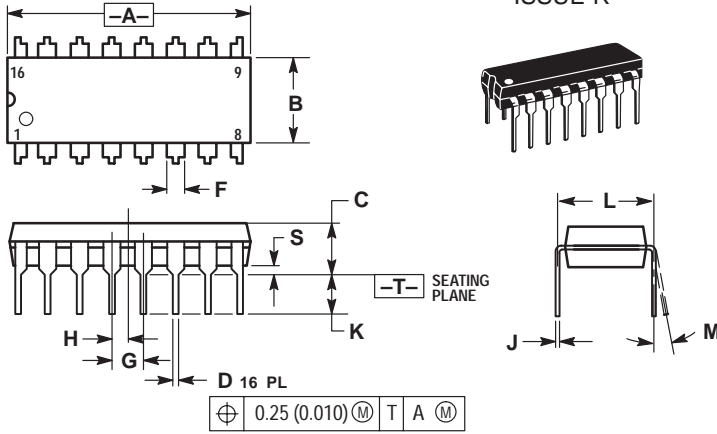
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

# 16-Pin Packages

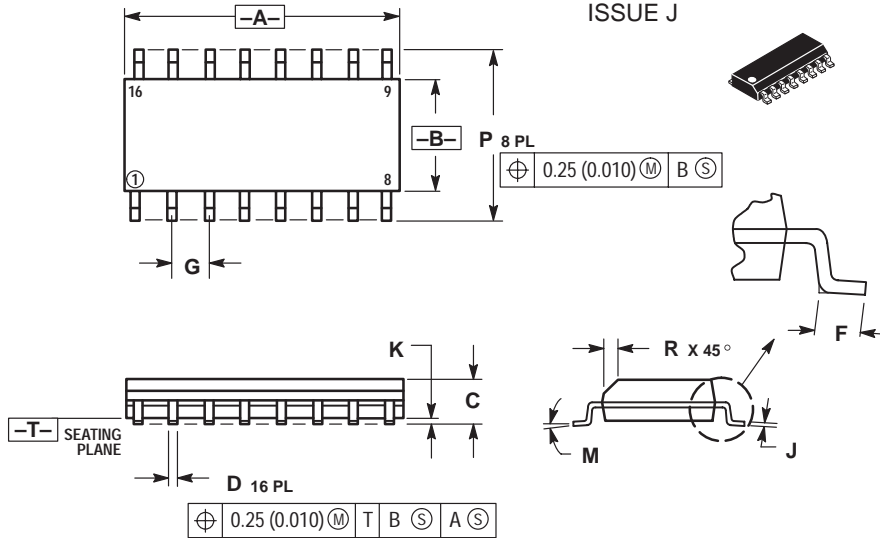
## PDIP-16 P SUFFIX PLASTIC PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

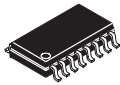
## SOIC-16 D SUFFIX PLASTIC PACKAGE CASE 751B-05 ISSUE J



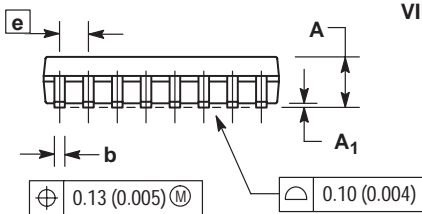
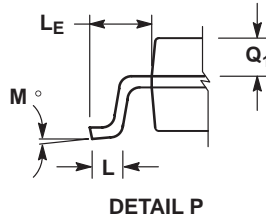
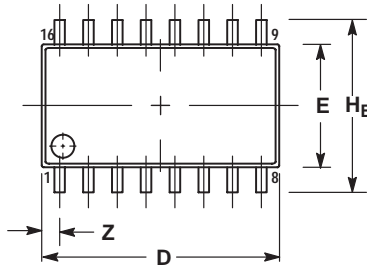
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# 16-Pin Packages (continued)



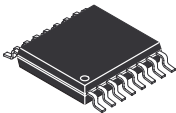
## SOEIAJ-16 F SUFFIX PLASTIC PACKAGE CASE 966-01 ISSUE O



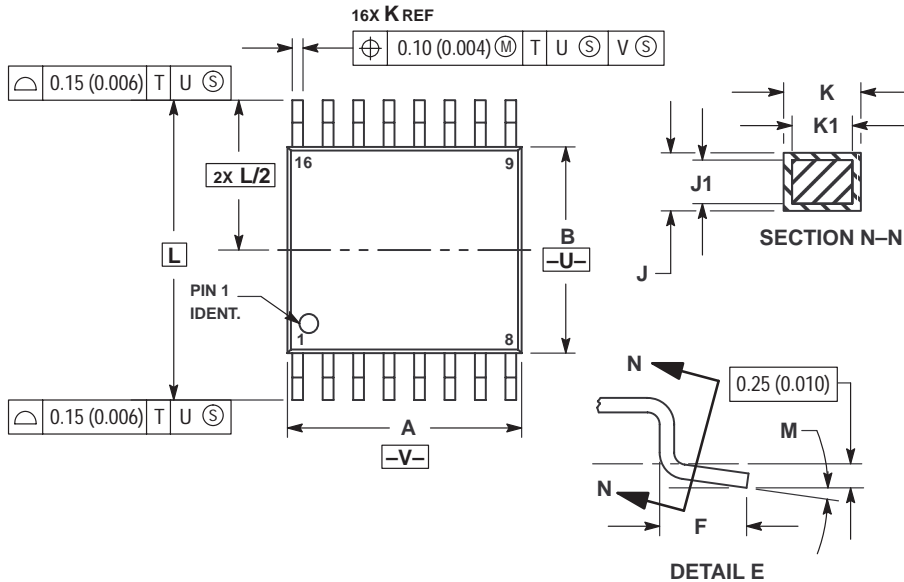
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>F</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031



## TSSOP-16 DT SUFFIX PLASTIC PACKAGE CASE 948F-01 ISSUE O



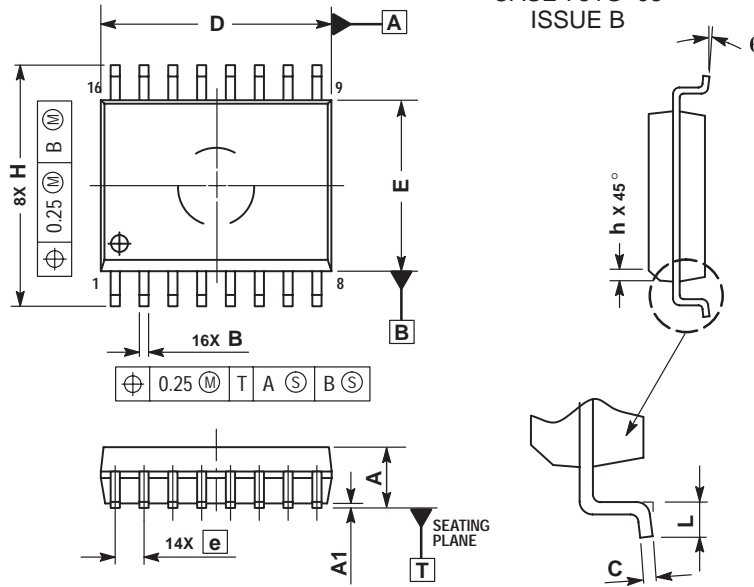
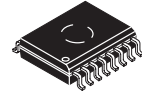
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J <sub>1</sub>	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K <sub>1</sub>	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

## 16-Pin Packages (continued)

### SOIC-16 DW SUFFIX PLASTIC PACKAGE CASE 751G-03 ISSUE B



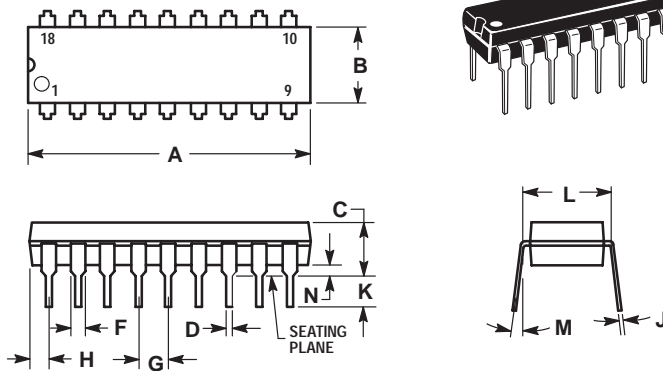
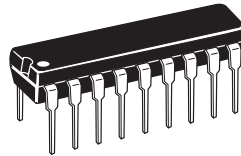
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
$\theta$	0°	7°

## 18-Pin Package

### PDIP-18 P SUFFIX PLASTIC PACKAGE CASE 707-02 ISSUE C



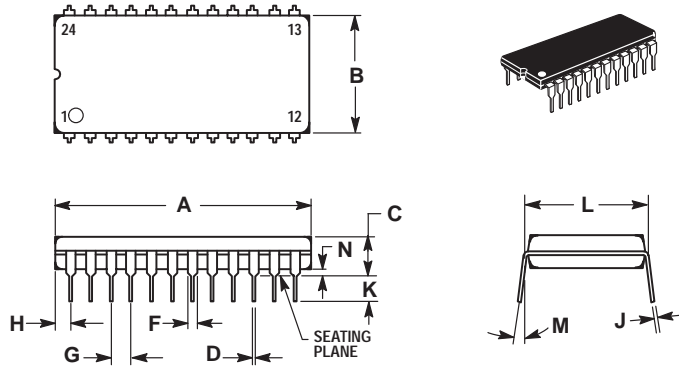
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

# 24-Pin Packages

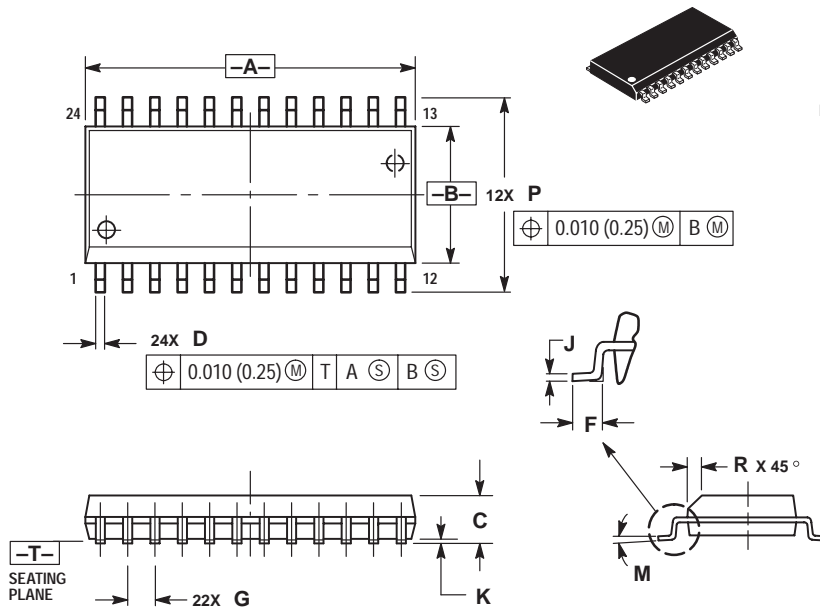
## PDIP-24 P SUFFIX PLASTIC PACKAGE CASE 709-02 ISSUE C



- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
  2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°		15°	
N	0.51	1.02	0.020	0.040

## SOIC-24 DW SUFFIX PLASTIC PACKAGE CASE 751E-04 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°		8°	
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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## ON SEMICONDUCTOR STANDARD DOCUMENT TYPE DEFINITIONS

### REFERENCE MANUAL

A Reference Manual is a publication that contains a comprehensive system or device-specific description of the structure and function (operation) of a particular part/system; used overwhelmingly to describe the functionality of a microprocessor, microcontroller, or some other sub-micron sized device. Procedural information in a Reference Manual is limited to less than 40 percent (usually much less).

### USER'S GUIDE

A User's Guide contains procedural, task-oriented instructions for using or running a device or product. A User's Guide differs from a Reference Manual in the following respects:

- \* Majority of information (> 60%) is procedural, in nature
- \* Volume of information is typically less than for Reference Manuals
- \* Usually written more in active voice, using second-person singular (you) than is found in Reference Manuals
- \* May contain photographs and detailed line drawings rather than simple illustrations that are often found in Reference Manuals

### POCKET GUIDE

A Pocket Guide is a pocket-sized document that contains technical reference information. Types of information commonly found in pocket guides include block diagrams, pinouts, alphabetized instruction set, alphabetized registers, alphabetized third-party vendors and their products, etc.

### ADDENDUM

A documentation Addendum is a supplemental publication that contains missing information or replaces preliminary information in the primary publication it supports. Individual addendum items are published cumulatively. Addendums end with the next revision of the primary document.

### APPLICATION NOTE

An Application Note is a document that contains real-world application information about how a specific ON Semiconductor device/product is used with other ON Semiconductor or vendor parts/software to address a particular technical issue. Parts and/or software must already exist and be available.

A document called "Application-Specific Information" is not the same as an Application Note.

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A Selector Guide is a tri-fold (or larger) document published on a regular basis (usually quarterly) by many, if not all, divisions, that contains key line-item, device-specific information for particular product families. Some Selector Guides are published in book format and contain previously published information.

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A Product Preview is a summary document for a product/device under consideration or in the early stages of development. The Product Preview exists only until an "Advance Information" document is published that replaces it. The Product Preview is often used as the first section or chapter in a corresponding reference manual. The Product Preview displays the following disclaimer at the bottom of the first page: "ON Semiconductor reserves the right to change or discontinue this product without notice."

### ADVANCE INFORMATION


The Advance Information document is for a device that is NOT fully MC-qualified. The Advance Information document is replaced with the Technical Data document once the device/part becomes fully MC-qualified. The Advance Information document displays the following disclaimer at the bottom of the first page: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

### TECHNICAL DATA

The Technical Data document is for a product/device that is in full production (i.e., fully released). It replaces the Advance Information document and represents a part that is M, X, XC, or MC qualified. The Technical Data document is virtually the same document as the Product Preview and the Advance Information document with the exception that it provides information that is unavailable for a product in the early phases of development (such as complete parametric characterization data). The Technical Data document is also a more comprehensive document than either of its earlier incarnations. This document displays no disclaimer, and while it may be informally referred to as a "data sheet," it is not labeled as such.

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