SM-H-88-1

Single-Density Disk Controller

Service Manual

585-9

ZENITH DATA SYSTEMS
SAINT JOSEPH, MICHIGAN 49085

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SETUP

The H-88-1 interface board allows the disk drive to communicate with the Computer. The H-88-1 plugs into pins P506 and P512 on the CPU board. See Figure 1-1. The flat cable connects to P803 on the interface board with the small triangle or marked edge up.

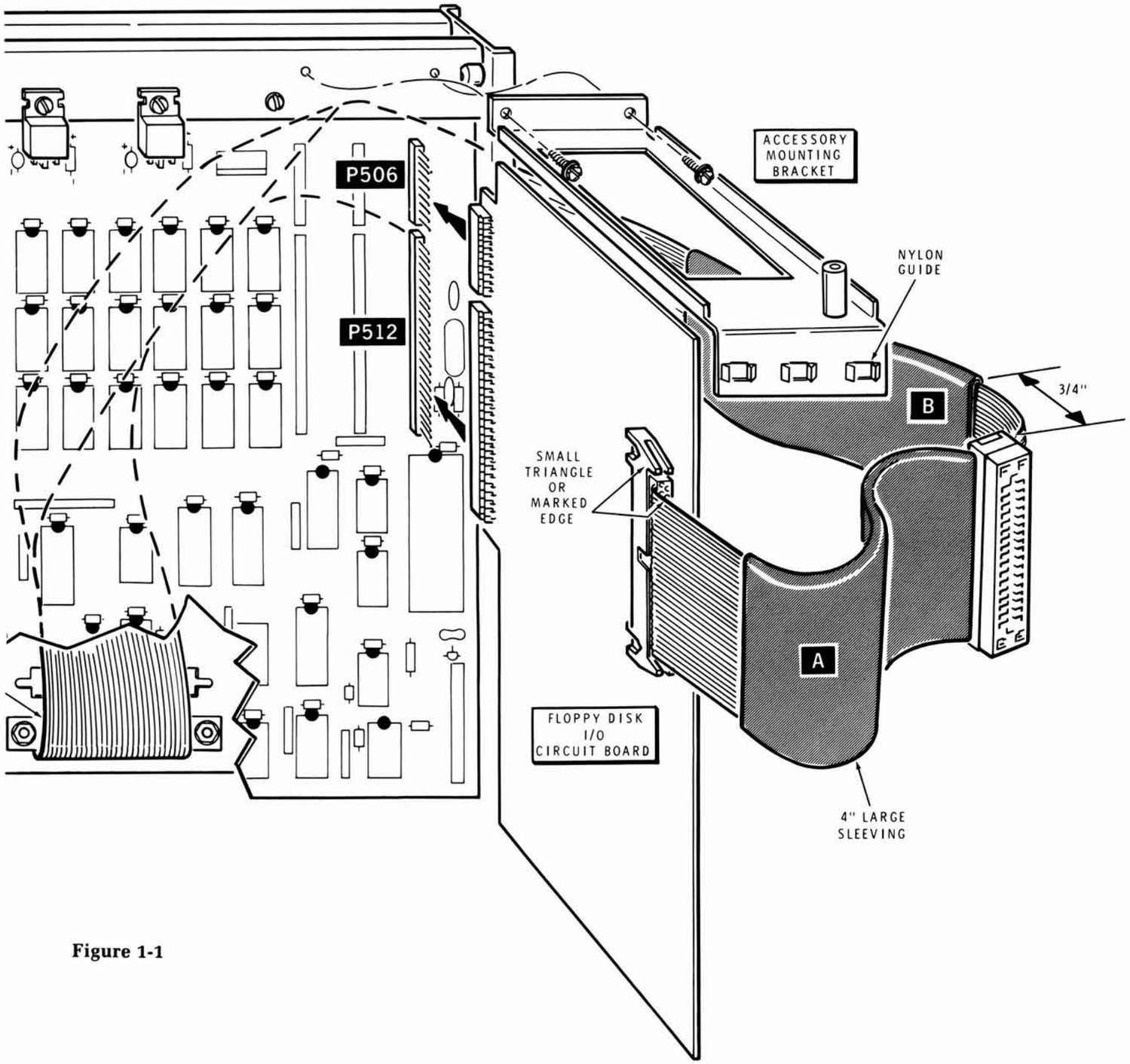


Figure 1-1

CONFIGURATION

To program a floppy disk unit, you may either bend out the proper leg on the programming module or cut the proper link. The advantage of bending out the leg is that the programming module may be returned to its original state.

If you are using the H-88-1, interface board, refer to Figure 1-2 (fold-out from this page) for programming the floppy disk unit.

If you are using the Z-89-37, interface board, refer to Figure 1-3 (fold-out from this page) for programming the floppy disk unit.

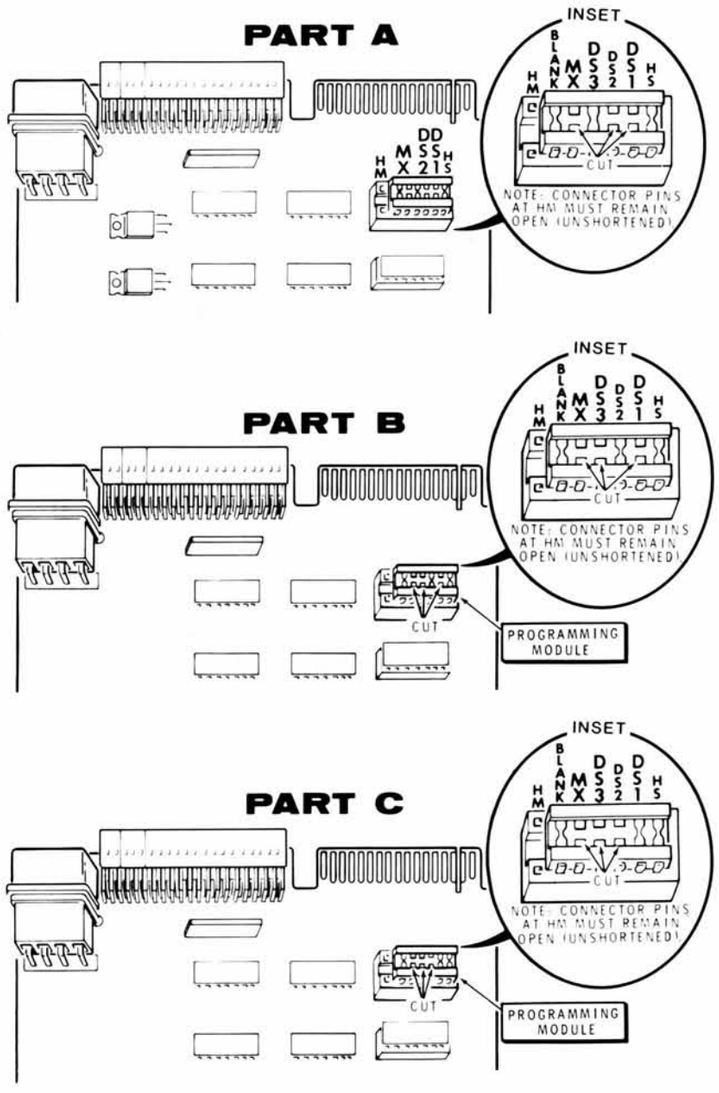


Figure 1-2

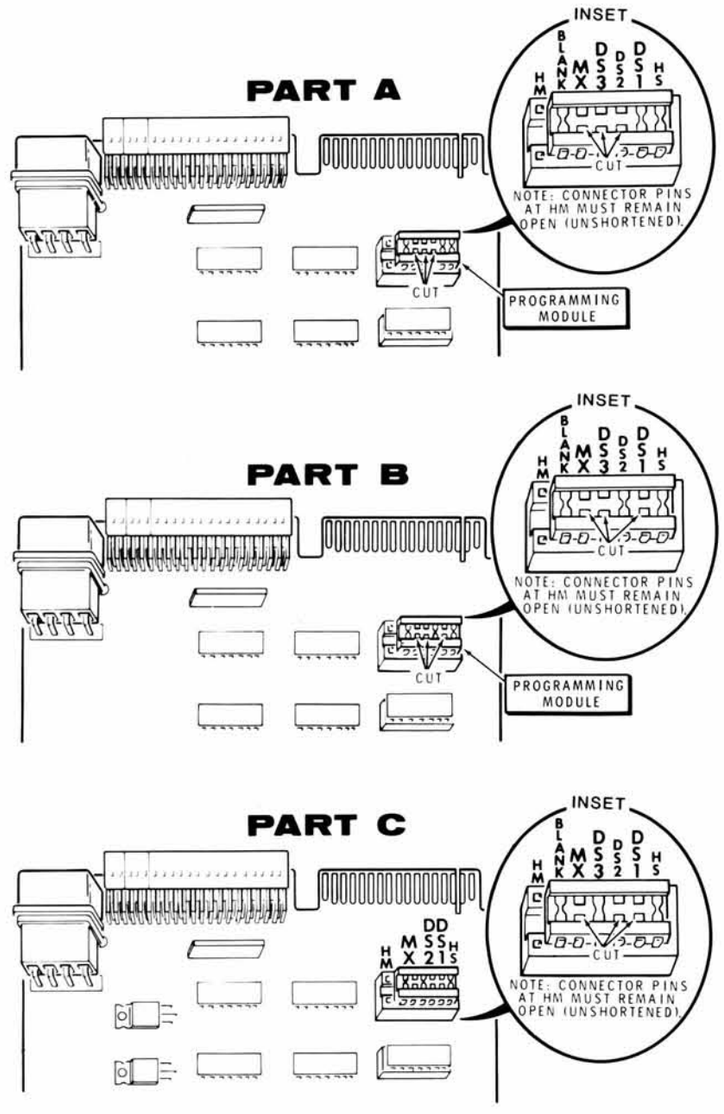


Figure 1-3

CIRCUIT DESCRIPTION

The floppy disk uses a storage format similar to a 45 rpm record. Each diskette is divided into 40 concentric tracks, with the outermost track labeled track 0 and the innermost track labeled track 39. Each track is further divided into ten sectors. Each sector stores 256 bytes of data plus checksum and address information to prevent data errors. The check character allows the system to be confident of the data integrity. The address information confirms that the head was moved to the desired track and that the correct sector has been found for a read or write operation.

There are eleven holes spaced around the center of the diskette for sector and index identification. Ten of the eleven holes are evenly spaced to indicate the start of a sector. The eleventh hole (the index hole) is spaced halfway between the sector 9 hole and the sector 0 hole. This uneven spread is recognized by the controller and informs the controller that the next sector hole corresponds to sector 0. This method of sectoring is known as hard sectoring. Since the diskette rotates at 300 rpm, the index hole is encountered every 200 milliseconds.

Information is stored on the diskette as serial magnetic flux changes. To prevent variations in rotational speed from impairing data accuracy, each serial bit is bracketed by a synchronizing bit. See Figure 2-1. A data pulse occurs if the data bit equals one and does not occur if the data bit equals zero. As mentioned previously, the data is recorded as a flux reversal. This is also shown in Figure 2-1.

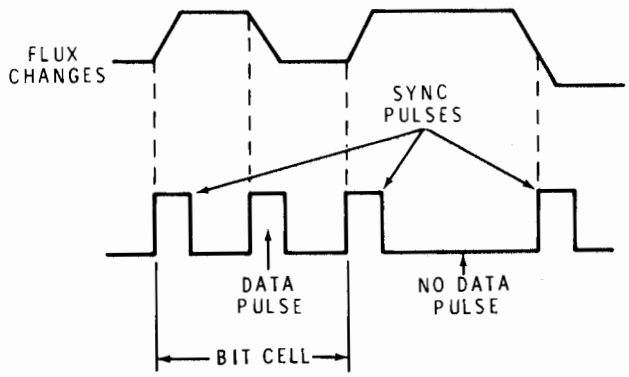


Figure 2-1

A byte of serial data written onto or read from a sector is defined as eight consecutive bit cells. See Figure 2-2. The most significant bit cell is defined as bit cell 0 and the least significant as bit cell 7. When a specific data bit is referred to (such as bit 3), it is with respect to the corresponding bit cell (bit cell 3).

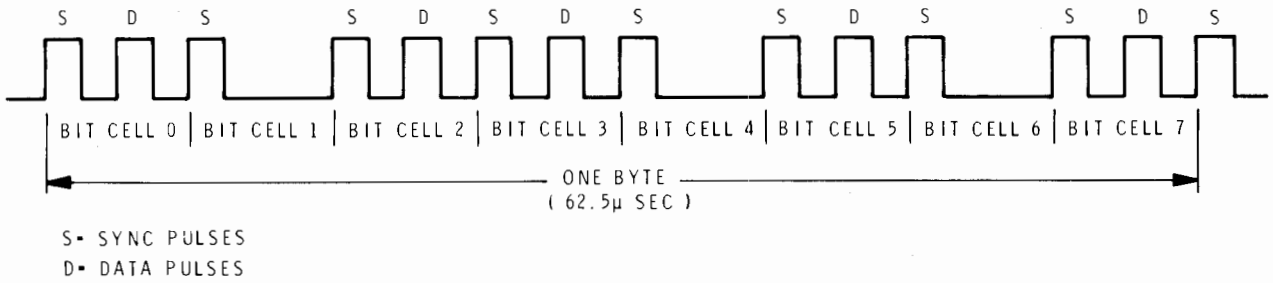


Figure 2-2

During a write operation, bit cell 0 of each byte is transferred to the disk drive first; while bit cell 7 is transferred last. Whenever data is read back from the drive, bit cell 0 of each byte is transferred first and bit cell 7 last. Figure 2-3 shows the information written on a sector.

USART U802 converts the serial data to parallel data and parallel data to serial data. However, the serial data format required by U802 is NRZ. Thus, it is necessary to convert the NRZ data to (to write) and from (to read) the bit cell format required by the floppy drive. This is accomplished by U812A, C, D; U813; and U816 for a write and U808; U815; U806D; U811A, B, C; and U812B for the read.

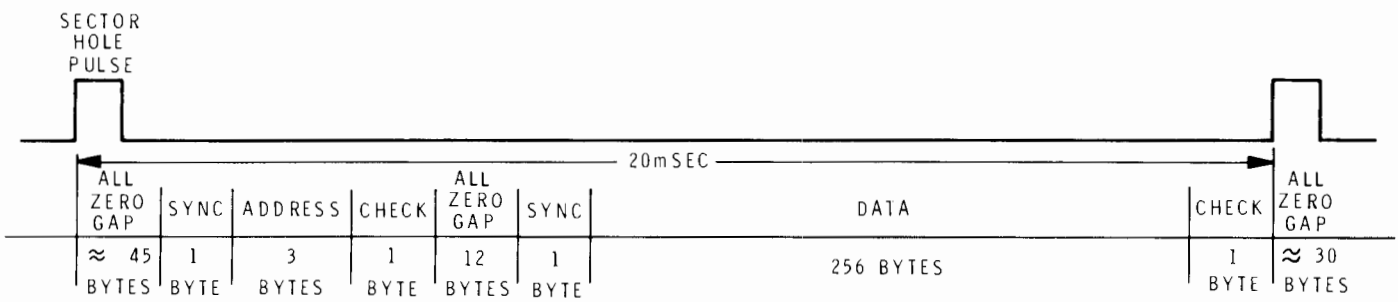


Figure 2-3

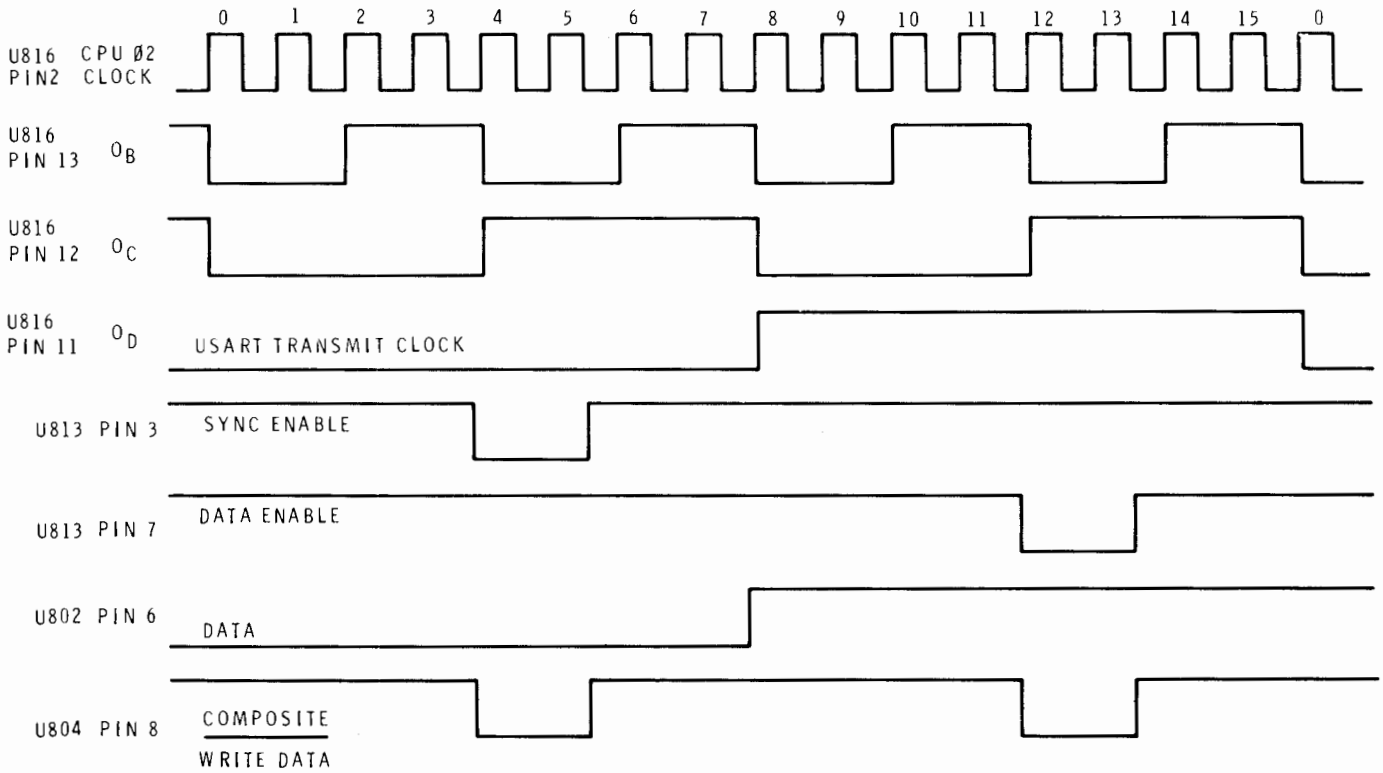


Figure 2-4

For the write operation, U816 divides the 2.048 MHz clock by 16. Its binary outputs are used by U813 which decodes the binary information into a 1-of-8 output. Each output is 0.977 μs in duration. See Figure 2-4. Output Q2 (pin 3) of U813 is the bit cell clock pulse and output Q6 (pin 7) is the data pulse. The QD output (pin 11) of U816 clocks the NRZ data from USART U802 and occurs every 7.678 μs. This defines the bit cell. The NRZ data is therefore synchronized with the 2.048 MHz system clock, and, consequently, the bit cell clock.

The data bit pulse is ANDed with the NRZ data by U812A to produce a pulse (pin 3 of U812A) if the NRZ is a "1" and no pulse if the NRZ data is a "0." This information is ORed with the bit cell clock by U812D to produce the composite bit cell data pattern required by the floppy drive. U804 gates the write data with the write gate in order to prevent any extraneous writing to the diskette unless the write gate is on.

The read data signal is conditioned by U806C and U808 to produce a very short (50 ns) active high pulse which occurs at the leading edge of both the bit cell data and clock pulses coming from the drive. U815 is a divide-by-12 counter that separates the data from the clock pulses.

Assume as a starting point that U815 has counted to 12 and the ENT and ENP inputs (pins 7 and 10) are low, preventing any further counting. At this point, the output of U806D is high. This allows the next pulse from the drive to reset U815 by U811D. Since all data strings start with a number of consecutive zero bytes (no data pulse), the counter will synchronize on the clock bit and not on the data bits. During the time between reset and count 12 (5.859 μs), data pulses are accepted. Therefore, the pulse is assumed to be a clock pulse.

When a valid data pulse is received, the R-S flip-flop (U811A and U811B) is set (pin 6 goes high). This signifies that the data bit was a "1." If no pulse was received within 5.859 μs after a clock pulse, then the R-S flip-flop is not set and the data bit was a "0."At this time, a 12 count has been reached and the data is toggled into the USART (U802). The next pulse from the drive is a clock pulse which resets counter U815 and the R-S flip-flop; thereby starting a new cycle.

U802, in addition to converting serial bytes to parallel during a read operation and parallel bytes to serial during a write operation, also searches for a synchronizing byte at the beginning of each data and address block on each sector. A read from port 176 resets U802 to the search character mode and forces a "0" on the output (pin 3) of R-S flip-flop U809A and U809B. The USART now compares each byte as it is input to the special character in its sync character holding register. When a match is made, the USART receiver returns to the byte mode and R-S flip-flop U809A and U809B is set to a "1." This informs the processor that the proper match was made.

Port 177 reads the floppy disk status and sync character match and controls the floppy disk with respect to its motor, track position, and write gate. Port 176 resets the USART to the search character mode and writes the search character to the USART. Port 175 reads and sets the USART status. Port 174 receives and transmits the data characters to the USART. The decoding for these various ports is accomplished by U814A, U814B, and U801. U803 latches the floppy control signals and U805 latches the floppy status signals.

QUICK CHECKS

- Check to see that the board is connected to the proper pins on the CPU board.
- Check to see that all pins are in the sockets.
- Check the flat harness for proper connection to the interface board and to the disk drive.

REPLACEMENT PARTS LIST

(Floppy disk controller board, part number HE 181-3392.)

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
RESISTORS		
R801	HE 6-151-12	150 Ω
R802	HE 6-151-12	150 Ω
R803	HE 6-151-12	150 Ω
R804	HE 6-151-12	150 Ω
R805	HE 6-151-12	150 Ω
CAPACITORS		
C801	HE 20-99	22 pF mica
C802	HE 21-164	.0015 μF ceramic
C803	HE 21-56	470 pF ceramic
C804	HE 21-56	470 pF ceramic
C805	HE 21-56	470 pF ceramic
C806	HE 21-56	470 pF ceramic
C807	HE 21-56	470 pF ceramic
C808	HE 21-56	470 pF ceramic
C809	HE 21-56	470 pF ceramic
C810	Not Used	
C811	HE 21-56	470 pF ceramic
C812	HE 21-56	470 pF ceramic
C813	HE 21-56	470 pF ceramic
C814	HE 21-56	470 pF ceramic

CIRCUIT Comp. No.	PART NUMBER	DESCRIPTION
Capacitors (Cont'd.)		
C815	HE 21-56	470 pF ceramic
C816	HE 21-56	470 pF ceramic
C817	HE 21-761	.01 μF ceramic
C818	HE 21-761	.01 μF ceramic
C819	HE 21-761	.01 μF ceramic
C820	Not Used	
C821	HE 21-761	.01 μF ceramic
C822	HE 21-761	.01 μF ceramic
C823	HE 21-761	.01 μF ceramic
C824	HE 21-761	.01 μF ceramic
C825	HE 21-761	.01 μF ceramic
C826	HE 21-761	.01 μF ceramic
C827	HE 21-761	.01 μF ceramic
COILS		
(13) L801-L813	HE 45-612	10 μH
CABLE		
—	HE 134-1144	Disk I/O cable

SEMICONDUCTOR IDENTIFICATION

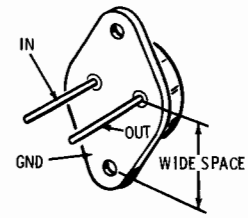
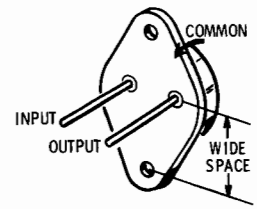
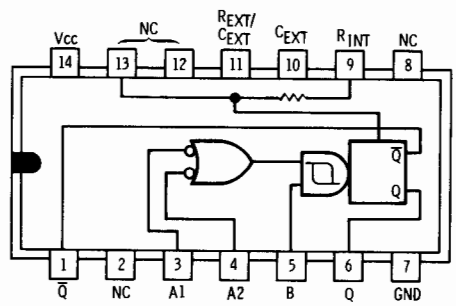
This section is divided into two parts: "Component Number Index" and "Part Number Index." The first section provides a cross-reference between semiconductor Component Numbers and their respective Part Numbers. The Component Numbers are listed in numerical order. The second section provides a lead configuration detail (basing diagram) for each semiconductor Part Number. The Part Numbers in the second section are also listed in numerical order.

COMPONENT NUMBER INDEX

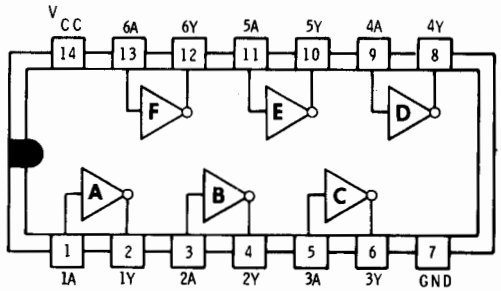
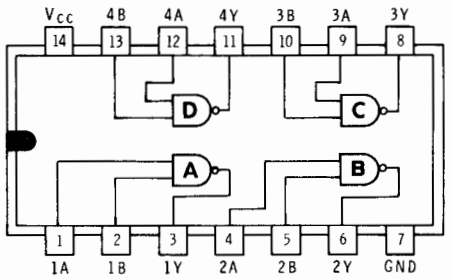
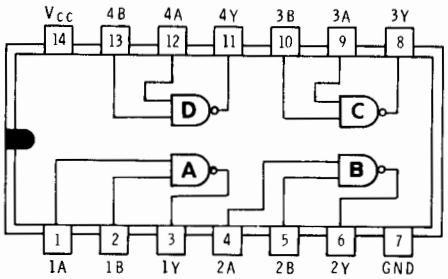
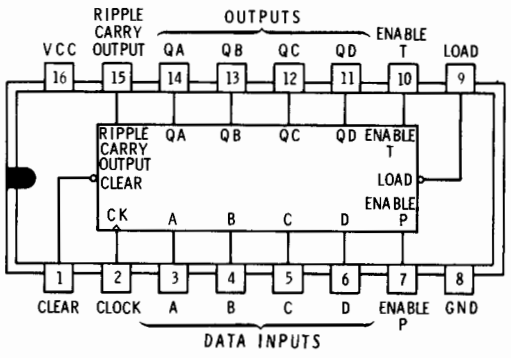
This index shows the Part Number of each integrated circuit.

CIRCUIT COMPONENT NUMBER	PART NUMBER
U801	HE 443-875
U802	HE 443-822
U803	HE 443-757
U804	HE 443-856
U805	HE 443-857
U806	HE 443-805
U807	HE 443-807
U808	HE 443-792
U809	HE 443-728
U810	HE 443-728
U811	HE 443-757
U812	HE 443-22
U813	HE 443-872
U814	HE 443-73
U815	HE 443-77

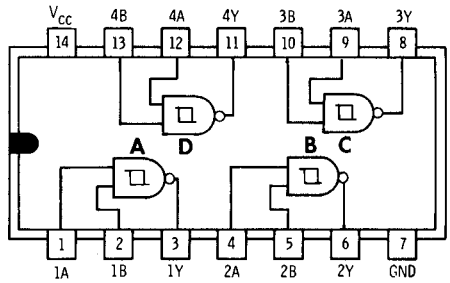
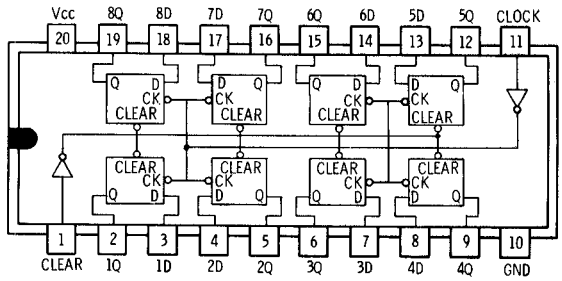
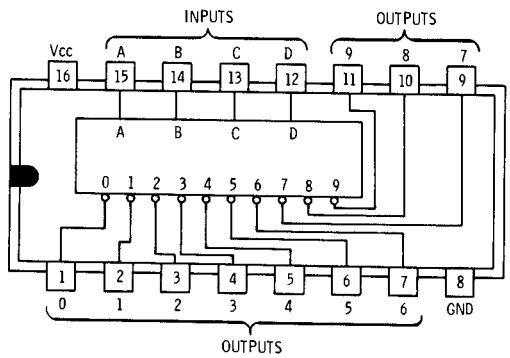
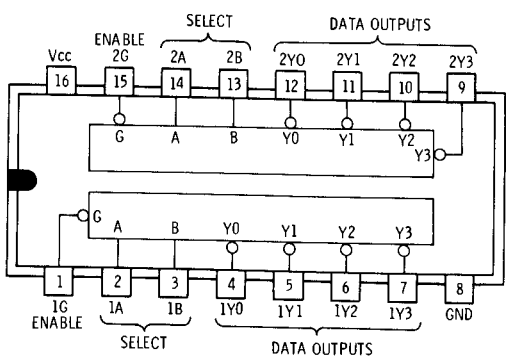
PART NUMBER INDEX

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 442-30	μA309K LM309	5-volt Regulator	
HE 442-650	78H12	+12 V, 5 A Regulator	
HE 443-22	74121	Monostable Multivibrator	

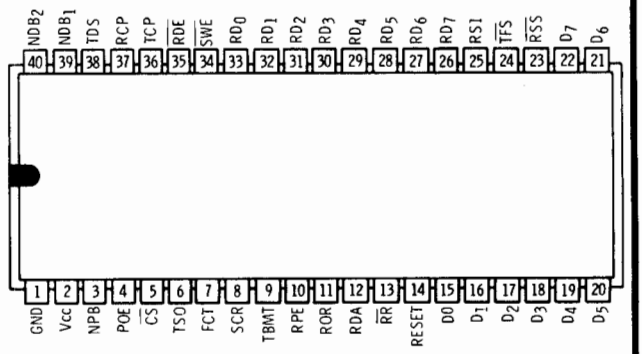
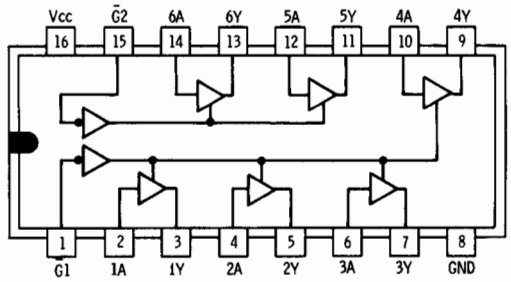
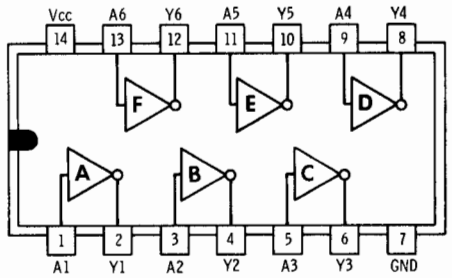
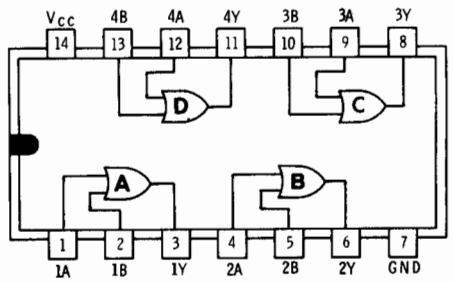
Part Number Index (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-73	7416	Line Driver	
HE 443-77	7438	Quadruple 2-Input Positive-NAND Buffers with Open-Collector Outputs	
HE 443-728	74LS00	Quad 2-Input NAND	
HE 443-757	74LS161	4-Bit Binary Counter	

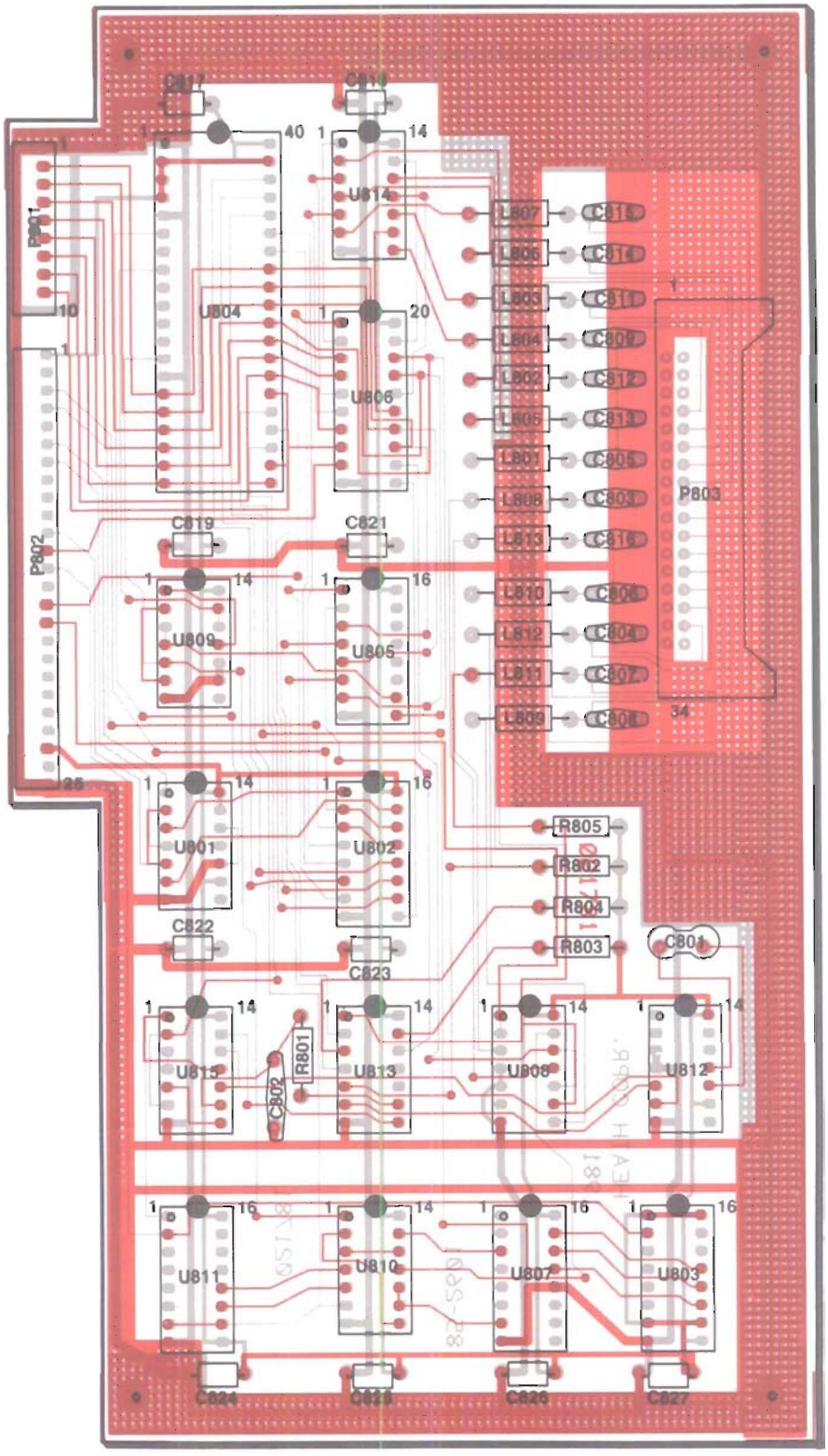
Part Number Index (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-792	74LS132	Quad 2-Input Positive-NAND Schmitt Triggers	
HE 443-805	74LS273	Octal D Flip-Flop with Clear	
HE 443-807	74LS42	BCD-to-Decimal Decoder	
HE 443-822	74LS139	Dual 2-to-4-Line Decoder	

Part Number Index (Cont'd.)

PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-856	S2350	Universal Synchronous Receiver/ Transmitter (USRT)	
HE 443-857	74LS367	Hex Bus Drivers	
HE 443-872	74LS14	Hex Schmitt-Trigger Inverters	
HE 443-875	74LS32	Quad 2-Input Positive OR Gates	

CIRCUIT BOARD X-RAY VIEW



SINGLE-DENSITY FLOPPY DISK CONTROLLER BOARD

Part number HE 181-3392. Shown from the component side.

SCHEMATIC OF THE ZENITH DATA SYSTEMS

SINGLE-DENSITY FLOPPY CONTROLLER
Model H-88-1

NOTES:

1. ALL RESISTORS ARE 1/4-WATT, 5% UNLESS MARKED OTHERWISE. RESISTOR VALUES ARE IN OHMS (K=1,000; M=1,000,000).
2. ALL CAPACITORS ARE IN µF UNLESS MARKED OTHERWISE.
3. ⏚ THIS SYMBOL INDICATES CIRCUIT BOARD GROUND.

Part of 585-9